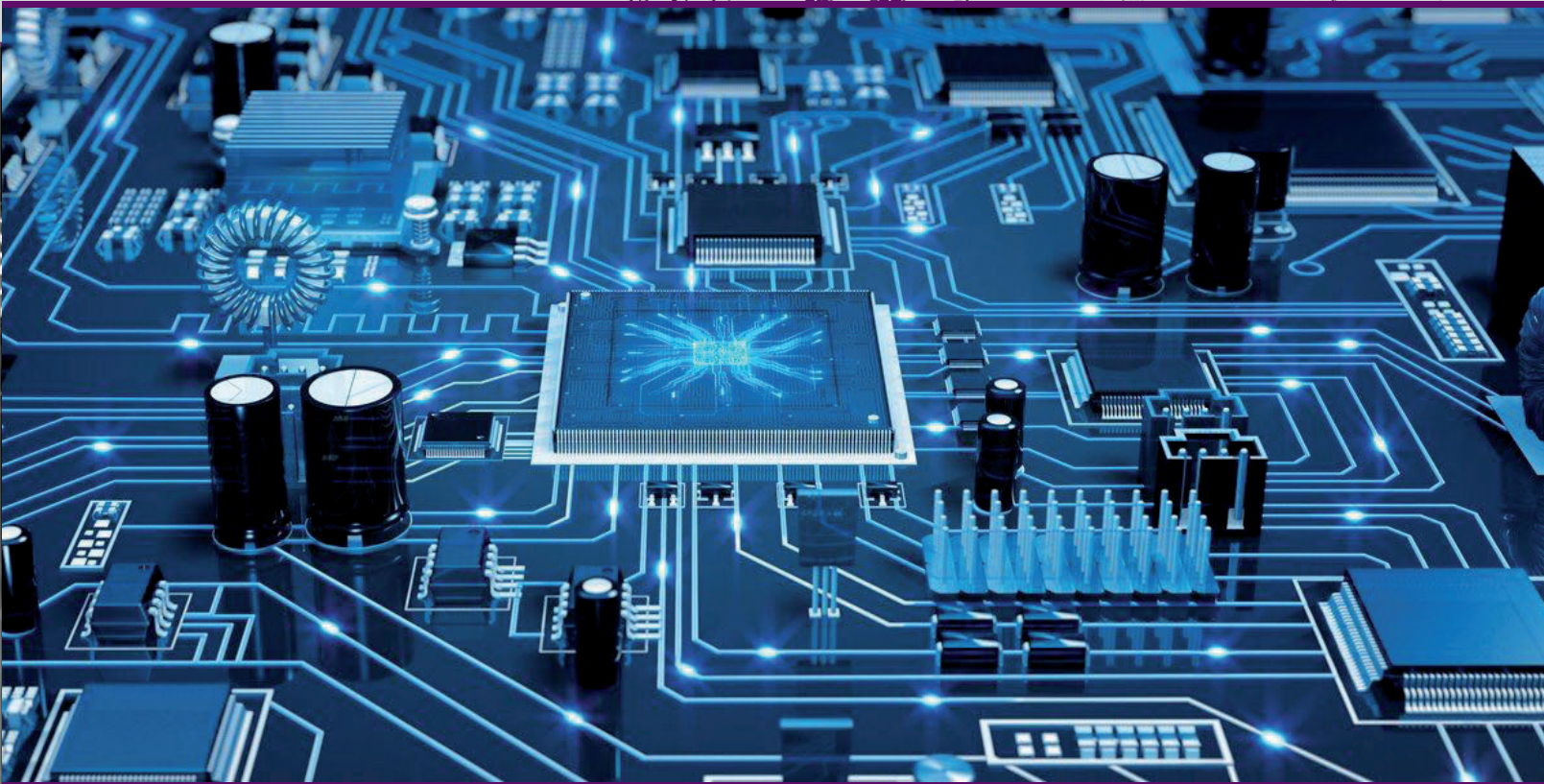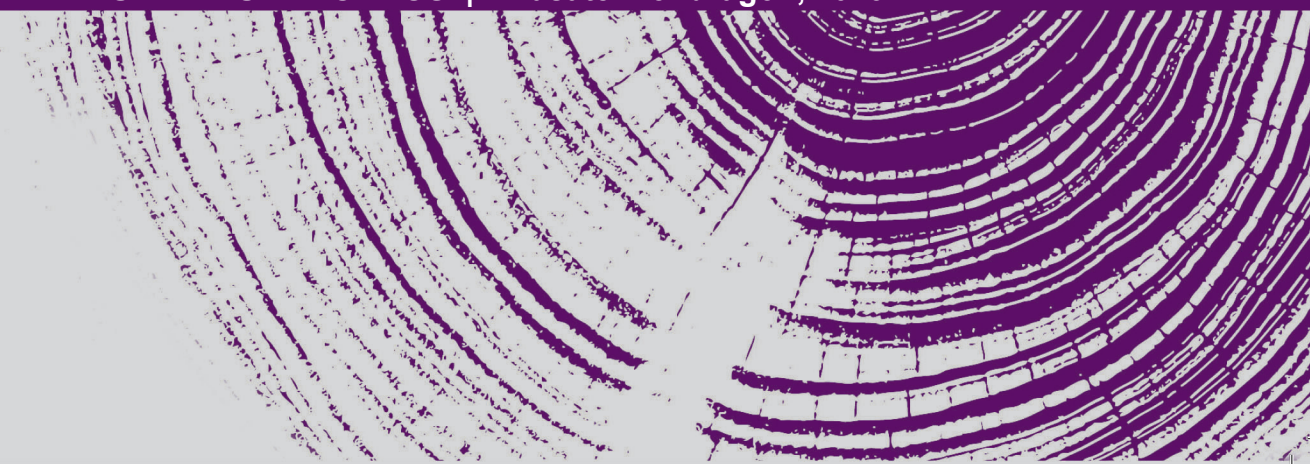**Mondragon
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DOCTORAL THESIS

SUITABILITY ANALYSIS, DESIGN AND PROTECTION OF AN ACTIVE MODULAR RECTIFIER ARCHITECTURE FOR A MORE ELECTRIC AIRCRAFT

UNAI ATUTXA OLMOS | Arrasate-Mondragón, 2023

Suitability Analysis, Design and Protection of an Active Modular Rectifier Architecture for a More Electric Aircraft

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Amaitzeko, eskerrak eman nahi nizkioke Igorri, Mondragon Unibertsitatean izan dudan ikuskatzaileari. Esan beharrik ez dago tesi hau honaino iritsi bada zuri esker izan dela. Ikasketak uztea pentsatuta nuen unean elkar ezagutu genuen, momentu zailean eta aurrean aldapa gora

luzeegia nuen unean. Baina une hartan ere aldapa hori igotzera animatu ninduzun, gaur egun ere egiten duzun moduan. Uste dut tesi honetan norbaitek errekonozimendu berezia merezi badu, hori zu zarela. Mila esker urte hauetan erakutsi didazunagatik. Irakasle, lankide eta lagun izateagatik. Zure laguntzagatik, zure dedikazioagatik, zure inplikazioagatik eta zure arduragatik. Potentzia elektronika beste begi batzuekin ikusten irakasteagatik. Denbora horretan lana aurrera ateratzeko behin eta berriz animatzeagatik eta oraindik ere hala ibiltzeagatik. Zalantzarik gabe, jarraitu beharreko adibide bat zara.

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Abstract

Title: *Suitability Analysis, Design and Protection of an Active Modular Rectifier Architecture for a More Electric Aircraft.*

Aiming to reduce the pollution caused by the traditional aircraft, strong research efforts are done towards the aircraft electrification to reduce the fuel usage. Thus, high efficiency, high power density and high reliability are some of the main characteristics expected from the future More Electric Aircraft (MEA), among others. In this context, the development of a High Voltage Direct Current (HVDC)-based aircraft distribution grid with bidirectional power flow capability results an interesting alternative to increase the distribution efficiency, reduce cable weight and provide bidirectional power-flow capability.

This PhD thesis focuses on replacing the conventional passive AC/DC converters for a high-efficient, high-power-dense, fault-tolerant and bidirectional active modular rectifier architecture which enhances the implementation of a HVDC primary distribution-based MEA Electric Power System (EPS). For that purpose, the potential active AC/DC topologies for the defined application are reviewed and their suitability in MEA applications has been studied. Afterwards, a topology evaluation is performed aiming to find the most suitable active AC/DC topology.

Based on the comparison results, three converter configurations are proposed which are used for designing three different active modular architecture which comply with the aviation standards. The three architectures are then compared in terms of efficiency, power density and reliability aiming to identify the most promising solution.

Finally, the resulting active modular architecture is integrated into the MEA power system to study its fault-tolerant capability. Thus, two different power system topologies are evaluated considering the integration of the active modular architecture with a proposed comparison methodology focused on efficiency, weight, survivability and fault clearing speed.

Keywords: More Electric Aircraft, AC/DC, Power Converter, Comparison, Protection, Electric Power System.

Laburpena

Izenburua: *Artezgailu-arkitektura aktibo modular baten egokitasun, diseinu eta babes analisia Hegazkin Elektrikoago Baterako.*

Ohiko hegazkinek eragindako igorpenak murrizteko helburuarekin, ikerketak egiten ari dira hegazkinen elektrifikazioaren alorrean, hegazkinek erregai gutxiago erabil dezaten. Horrela, asmoa da etorkizuneko Hegazkin Elektrikoagoak (MEA) efizientzia handia, potentzia dentsitate handia eta fidagarritasun handia edukitzea ezaugarri bereizgarri gisa. Testuinguru horretan, proposatzen da HVDC banaketan oinarritutako sistema elektriko bat garatzea, banaketan efizienteagoa izateko, guztirako pisua murrizteko eta ezaugarri gehigarriak - bi norabideko potentzia fluxua, esaterako - emateko aukera gisa.

Doktore tesi honen ardatza da AC/DC bihurgailu pasibo tradizionalaren ordez bihurgailu modular aktiboen arkitektura bat jartzea, HVDC banaketa sare bat ezarri ahal izateko eta efizientzia handia eta potentzia dentsitate handia eskaintzeko, gabeziak jasateko gai izateaz gain. Horretarako, AC/DC bihurgailu aktiboen topologiak berrikusi dira eta MEA aplikazioen testuinguruan duten bideragarritasuna aztertu da. Ondoren, konparaziorako azterketa bat egin da, hobekien egokitzen den AC/DC topologia aurkitzeko.

Konparazioaren emaitzetatik abiatuta, bihurgailuaren hiru konfigurazio desberdin proposatu dira, eta horiekin MEAren araudiari heltzen dioten hiru arkitektura modular diseinatu dira. Behin diseinatuta, hiru arkitektura horiek alderatu egiten dira aplikaziorako soluziorik egokiena aurkitzeko.

Azkenik, bihurgailu aktiboen arkitektura MEAren HVDC sistema elektrikoan txertatzen da, gabeziak jasateko duen gaitasuna aztertzeko. Horrela, bi sistema elektrikori buruzko azterketa konparatiboa proposatu da, biek arkitektura modular aktiboa integratuta dutela kontuan hartuta. Konparazioan proposatutako metodologia, azkenik, eraginkortasunaren, pisuaren, bizirauteko gaitasunaren eta gabezien ebakuazio abiaduraren emaitzak alderatzean oinarritzen da.

Hitz gakoak: More Electric Aircraft, AC/DC, Potentzia Bihurgailua, Konparatiba, Babes-Sistemak, Elektrizitate Sistema.

Resumen

Izenburua: *Análisis de Adecuación, Diseño y Protección de una Arquitectura Modular de Rectificación Activa para un Avión Más Eléctrico.*

Con el objetivo de reducir la emisiones causadas por el avión convencional, se están realizando investigaciones en la electrificación del avión para reducir su uso de combustible. De este modo, se pretende que el futuro Avión Más Eléctrico (MEA) se caracterice por una alta eficiencia, una alta densidad de potencia y una alta fiabilidad. Bajo este contexto, el desarrollo de un sistema eléctrico basado en distribución HVDC se propone como una alternativa capaz de mejorar la eficiencia en la distribución, reducir el peso total y proporcionar cualidades adicionales como un flujo de potencia bidireccional.

Esta tesis doctoral se centra en el reemplazo del convertidor pasivo AC/DC tradicional por una arquitectura de convertidores modulares activos que permita implementar un red de distribución HVDC y que ofrece una alta eficiencia, alta densidad de potencia y son capaces de soportar faltas. Para ello, se han revisado las diferentes topologías de convertidores AC/DC activos y se ha estudiado su viabilidad en el contexto de aplicaciones MEA. Después se ha realizado un estudio comparativo para encontrar la topología AC/DC que mejor se adapta.

Partiendo de los resultados de la comparativa, se han propuesto tres configuraciones de convertidor distintas con las cuales se diseñan tres respectivas arquitecturas modulares que se acogen a la normativa del MEA. Una vez diseñadas, estas tres arquitecturas se comparan para tratar de encontrar la solución más apuesta a la aplicación.

Finalmente, la arquitectura de convertidores activos se integra en el sistema eléctrico HVDC del MEA con el objetivo de estudiar su capacidad de tolerar faltas. Así, se ha propuesto el estudio comparativo sobre dos sistemas eléctricos diferentes considerando que ambos tienen integrado la arquitectura modular activa. La metodología propuesta en la comparativa, se centra finalmente en comparar los resultados de eficiencia, peso, capacidad de supervivencia y velocidad de evacuación de falta.

Palabras Clave: More Electric Aircraft, AC/DC, Convertidor de Potencia, Comparativa, Sitemas de Protección, Sistema Eléctrico.

Glossary

Acronyms

AC	Alternating Current
AEA	All Electric Aircraft
AEGART	Aircraft Electrical Generation System with Active Rectification and Health Monitoring
AFCB	Arc-Fault Circuit Breaker
APU	Auxiliary Power Unit
ATRU	Auto-Transformer Rectifier Unit
ATU	Auto-Transformer Unit
AVM	Average-Value Modeling
BBCU	Buck-Boost Converter Unit
BCRU	Battery Charger and Rectifier Unit
CF	Constant Frequency
CHB	Cascaded H-Bridge
CL	Consumer Loads
CO$_2$	Carbon Dioxide
DC	Direct Current
DM	Differential Mode
ECS	Environmental Control System
EHA	Electro-Hydraulic Actuator
EMA	Electro-Mechanic Actuator
EMC	Electromagnetic Compliance
EPS	Electric Power Systems
EU	European Union
FC	Flying Capacitor
FCL	Fault Current Limiter
FIT	Failure in Time
GaN	Gallium Nitride
GCU	Generator Control Unit
GPU	Ground Power Unit
HCB	Hybrid Circuit Breaker
HEA	Hybrid Electric Aircraft

HF	High Frequency
HV	High Voltage
HVAC	High Voltage Alternative Current
HVDC	High Voltage Direct Current
IDG	Integrated Drive Generator
IEA	International Energy Agency
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
IM	Induction Machine
IPCC	Intergovernmental Panel on Climate Change
LCS	Load Commutation Switch
LF	Low-Frequency
LV	Low Voltage
LVDC	Low Voltage Direct Current
MCB	Mechanical Circuit Breaker
MEA	More Electric Aircraft
MOET	More Open Electrical Technologies
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MOV	Metal-Oxide Varistor
MSS	Multi-pulse with Single-Switch
MTSI	Multi-pulse with Two-Switch Interleaved
MV	Medium Voltage
NASA	National Aeronautics and Space Administration
NPC	Neutral Point Clamped
NPP	Neutral Point Piloted
NSFCL	Non-Superconducting Fault Current Limiter
NVL	Non-Vital Load
PF	Power Factor
PFC	Power Factor Correction
PMSM	Permanent Magnet Synchronous Machine
POA	Power Optimized Aircraft
POR	Point Of Regulation
PWM	Pulse Width Modulation
RAT	Ram Air Turbine
RCCB	Remote Controlled Circuit Breakers
RMS	Root Mean Square
S-HCB	Superconducting-Hybrid Circuit Breaker
SFCL	Superconducting Fault Current Limiter
SG	Starter-Generator
Si	Silicon
SiC	Silicon Carbide
SPDU	Secondary Power Distribution Units

SRM	Switched Reluctance Machine
SSCB	Solid-State Circuit Breaker
STATCOM	Static Synchronous Compensator
SVPWM	Space Vector Pulse Width Modulation
TEC	Thermal Equivalent Circuit
TIMES	Totally Integrated More Electric Systems
TRU	Transformer Rectifier Unit
TVS	Transient Voltage Suppressor
UN	United Nations
VF	Variable Frequency
VL	Vital Load
WBG	Wide Band Gap
WIPS	Wing Ice Protection System

Greek Symbols

Variable	Description	Unit
α_T	Resistivity coefficient	ºC^{-1}
$\Delta T_\mathrm{h-amb}$	Temperature increase from ambient-to-heatsink	ºC
$\Delta T_\mathrm{j-amb}$	Temperature increase from ambient-to-junction	ºC
$\Delta T_\mathrm{j-c}$	Temperature increase from case-to-junction	ºC
$\Delta T_\mathrm{j-h}$	Temperature increase from case-to-junction	ºC
ΔI_L	Peak-to-peak DC inductor current ripple	A
Δi_L	Peak-to-peak AC inductor current ripple	A
ΔV_DC	Peak-to-peak voltage ripple on DC side	V
η	Efficiency	%
λ	Failure rate	FIT
λ_arch	FIT/cm^2 value obtained of the active modular rectifier architecture.	FIT
σ	Electrical conductivity	S/m

Latin Symbols

Variable	Description	Unit
A_Al	Cross-sectional area of the Nickle-plated aluminum cable	m
A_ins	Cross-sectional area of the cable insulator	m
B_1	Period of time after which a system (power device, converter, etc.) survives at 99 % probability	years
C_arc	Estimated arc capacitance of the fuse arcing period	F
C_link	Converter DC-link capacitance	F
C_sn	Snubber capacitance	F
D_buck	DC/DC duty cycle in buck mode operation	-
$\mathrm{DP_{PF}}$	Maximum Power Factor Design Point of the 2L$_\mathrm{C}$ converter	-
$\mathrm{DP_{Vol}}$	Minimum input filter volume Design Point of the 2L$_\mathrm{C}$ converter	-
E_C	Stored energy in a capacitor	J
E_cat	Datasheet melting i^{2}t or catalog energy of the fuse	A^{2}s
E_clear	Clearing i^{2}t energy of the fuse	A^{2}s
E_L	Stored energy in an inductor	J
E_melt	Accumulated melting i^{2}t energy of the fuse during operation	A^{2}s
f	Starter-Generator frequency	Hz

Variable	Description	Unit
f_{sw}	Switching frequency	kHz
$f_{\text{sw,max}}$	Maximum switching frequency	kHz
i_{DC}	Converter DC current	A
i_{f}	Fault current	A
i_{L}	Current flowing through an inductor	A
i_{fuse}	Current flowing through the fuse	A
i_{nom}	Nominal current	A
i_{ph}	Phase Root-Mean-Square current	A
i_{rated}	Rated current of a protection device at which starts its opening process	A
i_{trip}	Tripping current of the SSCB	A
L_{bus}	Stray inductance of the busbar	H
L_{cable}	Cable inductance	H
L_{cb}	Stray inductance of the connections to the busbar	H
L_{f}	Fault path inductance	H
L_{σ}	Stray inductance	H
l	Cable length	m
m	Modulation Index	-
N_{conv}	Number of converters	-
N_{dev}	Number of power devices	-
N_{f}	Number of kylocycles to failure of a power device	kylocycles
N_{rect}	Number of rectifiers converters	-
N_{st}	Number of STATCOM converters	-
P_{cond}	Average conduction losses	W
P_{conv}	Nominal converter power	W
P_{sw}	Average switching losses	W
r_{Al}	Nickle-plated aluminum cable radius	m
R_{arc}	Estimated arc resistance of the fuse arcing period	Ω
R_{bus}	Stray resistance of the busbar	Ω
R_{cable}	Cable resistance	Ω
R_{cb}	Stray resistance of the connections to the busbar	Ω
R_{DS}	Drain-to-source on-resistance	Ω
R_{sn}	Snubber resistance	Ω
$R_{\text{th,h-amb}}$	Heatsink-to-Ambient thermal resistance	ºC/W
$R_{\text{th,j-c}}$	Junction-to-Case thermal resistance	ºC/W
T_{amb}	Ambient temperature	ºC
t_{ext}	Extinction time of the fault current	s
T_{f}	Final temperature of the cable	ºC
T_{j}	Junction temperature of the power device	ºC
$T_{\text{j,max}}$	Maximum junction temperature of the power device	ºC

Variable	Description	Unit
T_{ref}	Reference temperature of the cable	ºC
$\mathrm{THD_i}$	Current Total Harmonic Distortion	%
$\mathrm{THD_v}$	Voltage Total Harmonic Distortion	%
V_{bd}	Breakdown voltage of the power device	V
V_{conv}	Phase Root-Mean-Square voltage at the converter terminals	V
V_{DC}	Output DC voltage of the rectifier	V
V'_{DC}	Output DC voltage of the DC/DC downstream the rectifier	V
V_{DS}	Drain-to-Source voltage	V
V_{fuse}	Voltage drop across the fuse	V
V_{L}	Inductor Voltage	V
V_{LL}	Line-to-line Root-Mean-Square voltage at the converter terminals	V
$\mathrm{Vol_h}$	Heatsink volume	cm^3
$\mathrm{Vol_p}$	Passive element volume	cm^3
V_{ph}	Phase nominal Root-Mean-Square voltage	V
V_{SSCB}	Voltage drop accross the Solid-State Circuit Breaker	V
$\mathrm{WTHD_v}$	Voltage Weighted Total Harmonic Distortion	%

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CHAPTER 1

Introduction

Abstract:

An introduction to the More Electric Aircraft concept and the significance of power electronics in the future electrified aircraft is presented in this chapter. The evolution of the aircraft electric power system is overviewed from the conventional aircraft to the up-to-date More Electric Aircraft with a special focus on power electronics. On this basis, the challenges and trends that power electronics must face for the development of the future aircraft are addressed, from which the motivation of this research work emerges. Finally, the research content of the Ph.D. thesis is outlined.

1.1   Moving Towards the More Electric Aircraft

Among the 17 major sustainable development goals outlined by the United Nations (UN) to be fulfilled by 2030, goal 13 is focused on taking urgent actions to fight climate change [1]. Taking into account the different existing global polluting sources, the transportation industry produces about 25 % of Carbon Dioxide (CO_2) global emissions and, in particular, the aviation industry produces around 2 % of global emissions [2–5]. In addition, considering that historically the air passenger traffic is yearly increasing about 5-6 %, an increment in global pollution could be expected in the coming years if no action is taken [1, 4, 6–8]. In fact, although the International Energy Agency (IEA) expects transportation emissions to be increased by 80 % by 2050, the Intergovernmental Panel on Climate Change (IPCC) pretends to reduce the current transportation CO_2 emissions by at least 50 % by the same date [2]. Thus, to achieve this last target, a substantial cut in transportation emissions is needed by means of developing and implementing more efficient solutions. Therefore, improved energy-efficient systems which reduce environmental impact become of extreme importance to achieve low contamination goals.

In the transportation context, a greater electrification of vehicles is pretended due to the higher efficiency, lighter weight and, thus, reduced environmental impact of electrical power systems [2, 7, 9, 10]. This trend has also affected the aviation industry where it is expected that 1 kg saved on each flight could save approximately 5400 tons of CO_2 and $ 4500 per year over a 20-year period for air civil traffic [3, 4, 11]. In fact, National Aeronautics and Space Administration (NASA) reported a technical paper which demonstrated that replacing traditional hydraulic, pneumatic and mechanical systems for lighter electrical technologies in a typical 200-seater aircraft could result in benefits like reducing the aircraft empty weight by 10 %, reducing the engine thrust by 13 %, and reducing the aircraft fuel burn in a 9 % [12].

Figure 1.1(a) presents an example of the engine energy demand for a typical Airbus A320 or Boeing B737 size conventional aircraft [2, 3, 9, 13, 14]. As depicted, in the conventional aircraft the engine not only produces the propulsive energy required for the aircraft to fly, but also the non-propulsive energy for feeding other aircraft subsystems. This non-propulsive energy demand is divided into four main types of energy, being pneumatic, hydraulic, mechanical, and electrical energy. Each energy type is used to power certain critical aircraft subsystems such as Wing Ice Protection System (WIPS) or Environmental Control System (ECS) in the case of pneumatic energy; actuation systems and landing gear extension employing hydraulic energy; fuel and oil pumps to engine using mechanical energy; and, avionics systems and lights applying electrical energy [1, 3, 9]. A well-known disadvantage of the aircraft architecture formed by these non-propulsive energy subsystems is that it tends to be heavy, bulky, inefficient and requires periodic maintenance [8, 12]. In addition, it is considered that the conventional aircraft architecture presents the following major drawbacks [8, 15–17]:

- The related features to a standard pneumatic system such as a low turbine efficiency due to the bleed valve for high-pressure air extraction located in the jet engine, the use of heavy and complex pipes, and a ducting running through the aircraft.

- The inherent composition of the hydraulic system which, apart from the added weight of

the pipes and pumps of this system, in case of malfunction forces the aircraft to land in order to remove the corrosive fluids and repair the system.

- The commonly seen leakage problems which are complex to find and result in a large time consumed to perform the repair.
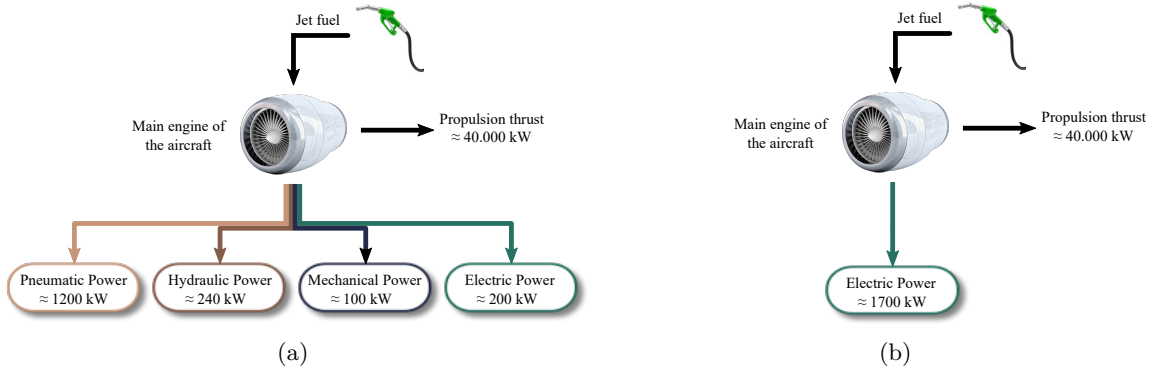

Figure 1.1 Example of the (a) power distribution of a conventional aircraft, and (b) power distribution of a More Electric Aircraft.

All these mentioned shortcomings which are inherent to pneumatic, hydraulic and mechanical subsystems are non-existent in a theoretical aircraft architecture where all the subsystems are fully electrified, that is, achieving a hydraulic-less and bleed-less aircraft architecture [16]. Thus, higher efficiency, fuel-saving, global warming emissions reduction, reduced noise and lower maintenance costs are expected from the aircraft electrification [1, 2]. In this context, the More Electric Aircraft (MEA) concept pretends to remove the use of other energy type but the electrical energy used in the aircraft subsystems as presented in Figure 1.1(b) [1, 2, 7, 8, 15, 17–19]. In other words, the propulsion remains traditional while the subsystems are electrified. This fact leads to an immense electrification of the aircraft which arises several challenges such as the increased electric power handling, the required system level safety and reliability, or the development of new high-efficient power electronic solutions which provide a reduced weight and volume compared to ones currently employed.

In this regard, initiatives and research projects are being taken in order to achieve the complete electrification of the aircraft subsystems while overcoming the current MEA concept related issues, such as the high weight and low power density of the existing power electronics, the integration of a higher number of electrified loads (which traditionally were hydraulic and pneumatic loads), providing a higher degree of safety and reliability, and improving the fuel-consumption efficiency [5, 10]. Although numerous initiatives exist, some leading examples are considered to be [19, 20]: Totally Integrated More Electric Systems (TIMES), which was concerned about the implementation of previously developed electrical systems into the aircraft; US Air Force MEA Program which investigated for providing more electrical capability to the fighter aircraft; Power Optimized Aircraft (POA), which was focused on the optimized management of electrical power in aircraft to reduce the non-propulsive power demand and fuel consumption while increasing the reliability and safety of onboard systems and reducing maintenance costs; and, More Open Electrical Technologies (MOET), which aimed to enable considerable changes in power management aboard commercial transport aircraft by means of developed power electronic progress at

that time.

Simply put, the aim of these initiatives, altogether with aviation industry, relies on developing high-efficient, reliable, fault-tolerant and high-power-dense aircraft electrical power systems and power electronic technologies which, additionally, reduce the aircraft fuel demand [4, 12, 18, 19]. As a result, the following benefits are expected from the future MEA in the coming years [2, 3, 7, 13, 16, 19, 21]:

- increased energy efficiency,
- reduced system volume and weight while targeting a 50% weight reduction in power electronics,
- increased reliability and fault-tolerant operation capability,
- eased maintenance,
- reduced engine-use on ground,
- improved controllability of power demand changes,
- system level optimisation and new capabilities such as providing advanced failure diagnostics and prognostics, and
- rapid and cost-effective implementation of developed technologies.

Furthermore, apart from aiming to reduce operational costs, reduce fuel burn and reduce the environmental impact, the MEA concept provides secondary benefits which boost the availability of the aircraft (considered as the main issue of late flights). In fact, it is estimated that approximately the 75% of flights are late due to system faults [3, 11]. According to [19], 50% fewer unexpected delays due to power system failures are expected by implementing the MEA concept. This fact is important because any unexpected "grounded" time is translated into significant cost increase for airlines [22]. Currently, modern electrical devices not only increase reliability, but they offer higher availability to the aircraft because of the possibility to isolate a subsystem in case of failure [11, 17, 23, 24]. It is stated in [3, 8, 11], indeed, that compared to hydraulic systems, whose fault probability is 100 times higher than the one of an electrical busbar, the possibility of isolation of electric subsystems becomes an advantage while a failure in hydraulic ones provokes a "No Go" fault.

At this point, it should be highlighted that even if several benefits are expected from the future MEA, the development and implementation of these benefits is driven by different technology enablers. On the one hand, the rapid and cost-effective implementation of the developed technologies will mainly depend on the easiness of the components manufacturing process and the price lowering of the required materials [19]. Similarly, the advancements in failure diagnostics and prognostics could be related to the development of fault-detection algorithms, faster measuring equipment and faster data processing capability of the employed electronics [2, 11, 22, 24]. Hence, these two MEA benefits can be considered as a result of the development of industrial products or data processing.

On the other hand, the research and development of innovative and advanced power electronics which provide the MEA with other features such as high efficiency, lower system weight and volume and, hence, higher power density, is pursued in this work. Power conversion results

key in this sense since it provides the possibility to efficiently adapt the generated power for its posterior distribution and load feeding. Furthermore, the implementation of a higher amount of power electronics could also be beneficial in terms of electrifying certain fuel-required aircraft flight stages like taxiing and, thus, reducing the engine-use on ground.

As a direct consequence of the development and implementation of more electrical technologies, the required electrical energy onboard the aircraft has significantly increased during the last decades (see Figure 1.2) [2, 3, 11, 13, 18]. It is worth to mention that, even if the MEA concept was brought in around World War II and has been developed as fast as enabling technologies have done during the last decades, it is the Airbus A380 and the Boeing B787 models the ones considered as the starting point for the modern MEA. The main reasons are the significant increased power generation and the increased electrification of heavy loads which are supplied by a High Voltage Direct Current (HVDC) bus. A summary of the key electrical features of both aircraft models is presented in Table 1.1. On the one hand, 600 kW of installed power capacity is provided in the Airbus A380 model and it also presents the first hydraulic-less architecture transition steps because of the electrification of the Electro-Hydraulic Actuator (EHA) and landing gear. On the other hand, the Boeing B787 model provides 1000 kW of electric power installed capacity and a bleed-less architecture. As a consequence, several heavy loads, such as the ECS or the WIPS, are electrified and the pneumatic systems are completely removed. As a result of the electrification development, the fuel consumption of the B787 model has been reduced by a 3 % compared to similar-sized conventional aircraft at cruise condition [17, 18, 23]. These innovations, among others, have supposed a key milestone in the MEA Electric Power Systems (EPS) development [1, 2, 4, 10, 16].
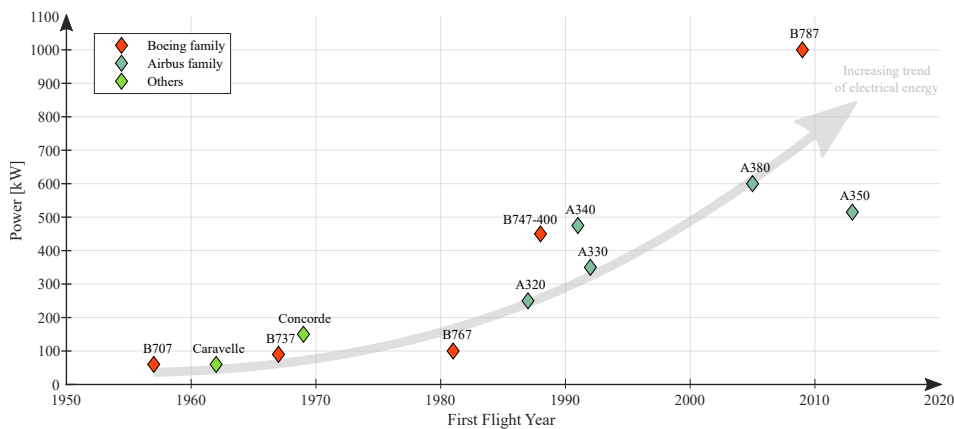
Figure 1.2 Outcome of the development of the MEA according to the growth of electrical onboard power need.

Table 1.1 Summary of the key electrical features of Airbus A380 and Boeing B787 MEA models.

Feature	A380	B787
Number of engines	4	2
Number of generators per engine	1	2
Generator power rating	150 kW	250 kW
Generator phase RMS voltage	115 V_{AC}	230 V_{AC}
HVDC distribution voltage	270 V_{DC}	$\pm$ 270 V_{DC}
Highlighted electrified loads	EHA, landing gear, electric thrust reverser	ECS, WIPS, Electric breaks

1.2 The Evolution from the Conventional Aircraft Power System to the Current More Electric Aircraft Power System

The aircraft EPS can be defined as a self-contained network which is formed by electric machines, power electronic converters, energy storage devices, protection systems, loads, etc. which are connected to different voltage level buses [1, 7, 16]. The standardized voltage levels are,

- $28\,V_{DC}$: used for low power loads like flight controls.
- $115\,V_{AC}$ at $400\,Hz$: used as the generation and common distribution voltage.
- $270\,V_{DC}$: used in military aircraft and some loads in the large commercial aircraft.

The electric power is generated by the electric machines and/or storage devices and adapted for distribution and load feeding by means of power electronic converters. With the development of the MEA concept more and more loads are being electrified onboard and, hence, not only a higher power handling capability of the aircraft EPS is expected but also a higher system complexity. That is to say, the more the aircraft is electrified, the higher the complexity of the EPS becomes [1, 2, 4, 25]. Figure 1.3 presents an example of simplified EPS architectures of both a conventional aircraft (based on B737 aircraft model) and a MEA (based on B787 model). Both architectures share similarities such as the two main engines, the three-phase paralleled generators, the Alternating Current (AC) distribution network and the Auxiliary Power Unit (APU). However, considerable differences can be observed such as the operating Root Mean Square (RMS) voltage level of the AC primary distribution bus, being $115\,V_{AC}$ in the conventional aircraft and $230\,V_{AC}$ in MEA, or the increased complexity of the network downstream the AC distribution bus.
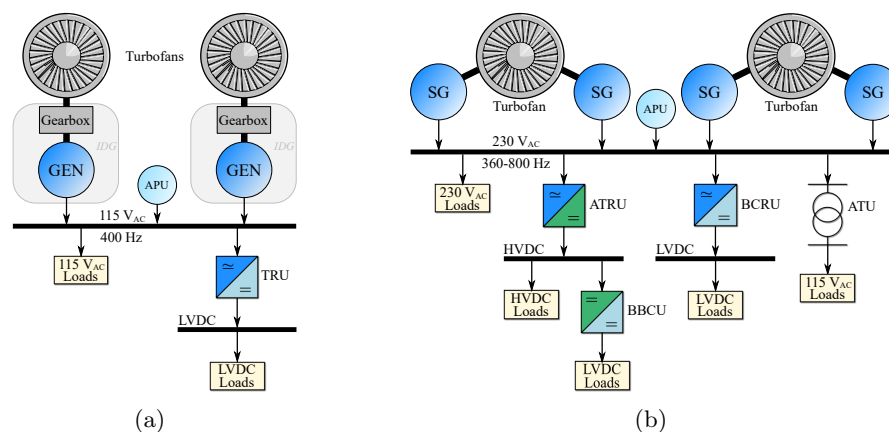
Figure 1.3 Simplified EPS schemas of (a) a conventional aircraft based on Boeing B737 model, and (b) a MEA based on Boeing B787 model.

1.2.1 The Power Generation Systems

In reference to the generation system, the conventional aircraft EPS in Figure 1.3(a) is based on $400\,Hz$ Constant Frequency (CF) and $115\,V_{AC}$ phase RMS voltage generation and distribution network [3, 4, 8, 18, 24]. Since the engine speed varies during the flight, the CF voltage is achieved

by locating a gearbox between the Variable Frequency (VF) engine shaft and the electric generator. This way, the mechanical speed and, hence, the electrical frequency of the generator stays constant on the aircraft's primary distribution AC bus [4, 10, 18, 22, 24]. It is worth to mention that, with the course of time, the later on developed AC CF generation systems such as the ones driven by Airbus A320, A340, A330 models or Boeing B747 and B767 models, not only provide more power capability, but also incorporate the generator and the gearbox joined into a unique piece called Integrated Drive Generator (IDG). The IDG ensures a higher power density than the former independent gearbox and generator systems [11, 18]. However, it is considered as a critical low reliability and low power density component due to the inherent mechanical moving parts related to the gearbox which, additionally, require from frequent maintenance [3, 18, 22].

Aiming to improve the IDG mechanical related issues, in the MEA EPS depicted in Figure 1.3(b) the gearbox is removed allowing the electric machine as a wideband VF generator operating in a variable frequency range between 360 and 800 Hz. This VF operation, which is proportional to the engine shaft speed, is also reflected in the AC primary distribution bus. Since the generator is directly coupled to the engine, not only the system reliability and efficiency are improved but also the overall generation system weight is reduced [4, 10, 11, 15, 16, 18, 19, 22, 24]. In fact, VF generation is considered as a key factor for higher output power management since allows increasing power generation without necessarily increasing weight [8, 12]. It is expected that VF generation will increase power generation reliability by a 50 % [19]. Nevertheless, existing issues and challenges related to advanced electromagnetic technology, high-speed voltage regulation and system protection to maintain high-level power quality over the wide output range have to be solved [19].

The employed electric machine in both conventional and MEA EPS, though, is the three-stage wound-field synchronous generator presented in Figure 1.4. The popularity of this electric machine relies on its inherent safety. Since the three-stage wound-field synchronous generator allows a direct control of the field by means of the Generator Control Unit (GCU) the excitation can be instantaneously removed and the machine is deenergised. Thus, this kind of machine can be instantaneously stopped in case of failure or abnormal operation, which provides a high reliability degree to the overall system. The main issue is that this machine requires from heavy rectifiers and filters to achieve a Direct Current (DC) excitation field and the regulated output voltage [11, 15, 18, 24].

With the development of B787 model, the additional feature of main engine electrical start is also provided by the three-stage wound-field synchronous machine when the engines are off and, hence, the aircraft is on ground [3, 11, 15, 17, 18, 22]. This concept, which conventionally was done using the pneumatic energy provided by the APU and required from high fuel consumption, is currently done by an inverter, thus supporting the bleed-less architecture idea. Hence, instead of generator, the term Starter-Generator (SG) is used for the three-stage wound-field synchronous machine due to its double operating function: *(1)* as in conventional systems, the machine works as a generator to supply aircraft loads when the main engine is operating; *(2)* when the aircraft engines are off, the machine is used in motoring mode to provide electrical start to the main engine while reducing fuel consumption.
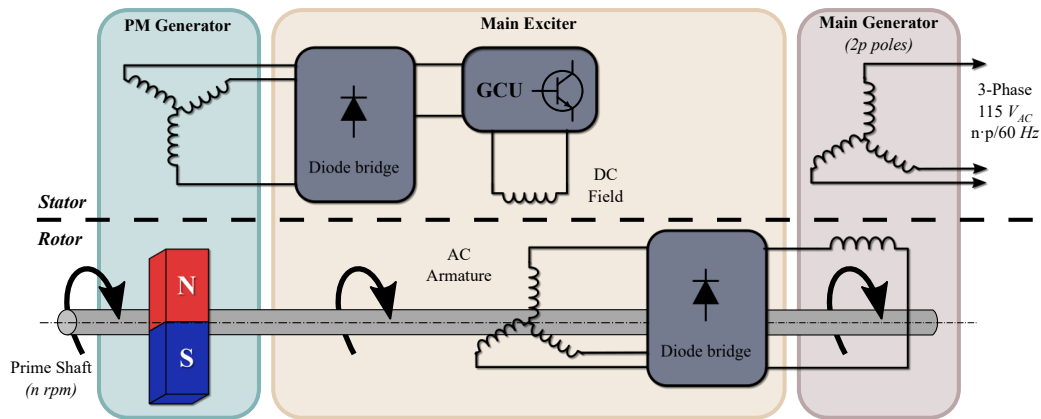
Figure 1.4 Schematic of the three-stage wound field synchronous machine.

It is worth to mention that, apart from the SG linked to the main engine, the APU and the Ground Power Unit (GPU) are also considered as additional power sources which provide power when the aircraft is on ground [4, 15, 22, 26]. Currently, the GPU can be a mobile APU car or an inverter fed by the airport electric grid which, typically, operates at $115\,V_{AC}$ and $400\,Hz$ [4]. The APU is a gas turbine that provides both pneumatic and electric power and it may also provide back-up hydraulic power [4, 22, 27]. The major drawbacks of the APU are its low efficiency (typically below $20\,\%$), high fuel consumption and high noise emissions [24, 27]. As previously mentioned, in the conventional aircraft the APU provides the main engine start capability through pneumatic power. In a bleed-less based MEA, though, since no pneumatic systems are implemented the APU only provides electric power through two large generators (for redundancy reasons) [4, 22]. Furthermore, the APU can also supply power when the aircraft is in the air under certain operating conditions including emergencies. Nevertheless, due to the reduced air density at high altitudes the power capability of the APU gets limited [15, 22]. In addition, a Ram Air Turbine (RAT) which resembles a small wind turbine deployed by the pilot could provide electric and/or hydraulic power under emergency conditions [15, 22, 26].

1.2.2 The Distribution Network and Power Conversion

Regarding the distribution network, a centralized structure is followed in the conventional EPS (see Figure 1.5(a)) [21, 22]. In this traditional approach, the power is generated by the IDGs close to the wings and routed to the cabin for protection and management before being routed individually to each load. Therefore, the relatively long distances existing between generation and consumption result in high losses, high weight and high rating of the conductors which, consequently, derive in high costs. The loads connected to this centralized distribution AC bus are classified into two types: the linear AC loads, which are principally fans for circulating the aircraft air and are fed at the same voltage and frequency level as the distribution bus [22, 24], i.e. $115\,V_{AC}$ and $400\,Hz$ and named as "*115 V_{AC} Loads*" in the Figure 1.3(a); and the Low Voltage (LV) loads which are fed in $28\,V_{DC}$ and are constituted by essential flight services such as communication and navigation [24, 28]. DC power could be obtained from a DC generator, however, the space limitations around aircraft engine and the required relatively long and heavy DC LV feeder cables (to connect the generator to the distribution bus) make DC generation

unfeasible. Hence, power conversion is needed in the conventional system to supply these $28\,\text{V}_{\text{DC}}$ loads from the $115\,\text{V}_{\text{AC}}$ - $400\,\text{Hz}$ power sources [24, 28].
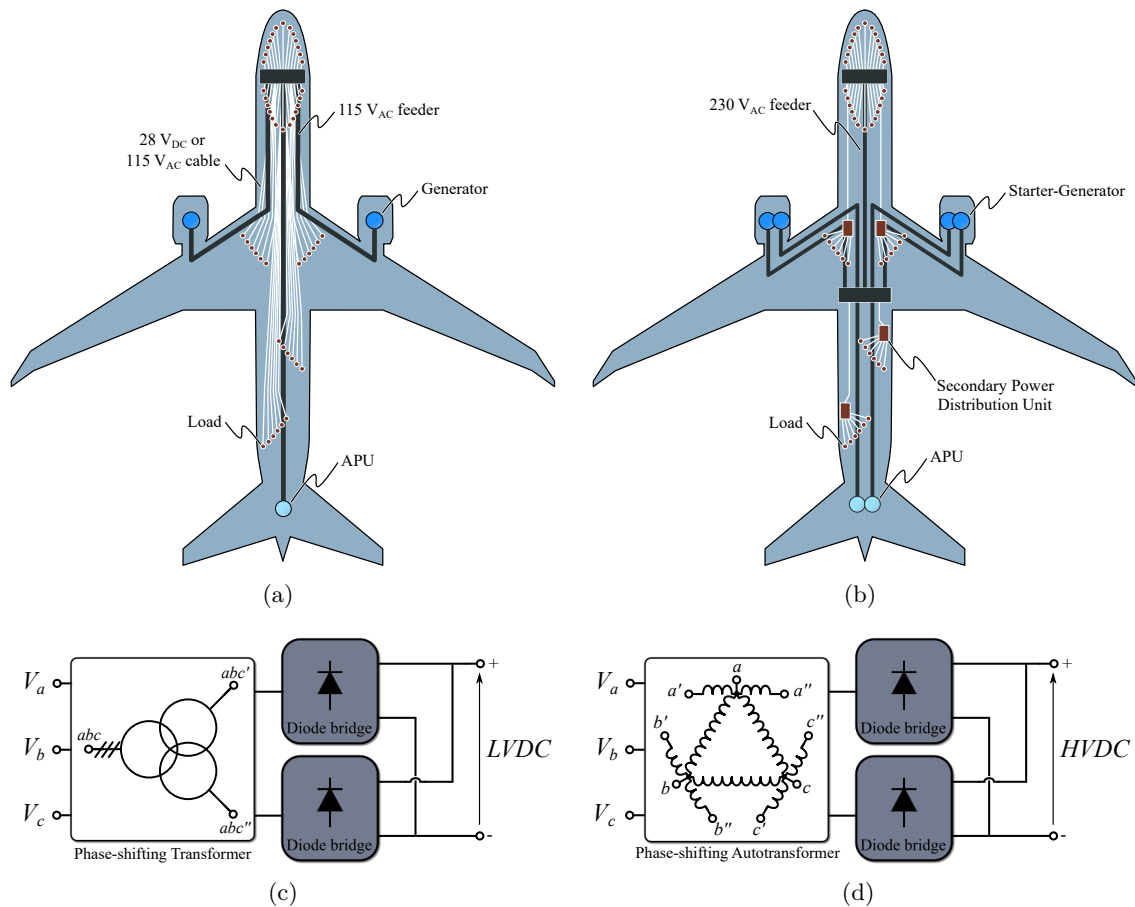
Figure 1.5 Schematics of (a) a centralized distribution-based EPS, (b) a decentralized distribution-based EPS, (c) a 12-pulse Transformer Rectifier Unit (TRU) example, and (d) a 12-pulse Autotransformer Rectifier Unit (ATRU) example.

The $115\,\text{V}_{\text{AC}}$ to $28\,\text{V}_{\text{DC}}$ power conversion is done by means of a Transformer Rectifier Unit (TRU) such as the one depicted in Figure 1.5(c) [1, 4, 8, 10, 22, 24, 28]. In the military standard MIL-STD-704F [29], the TRU is defined as a three-phase AC/DC isolated converter which works between the High Voltage Alternative Current (HVAC) and the Low Voltage Direct Current (LVDC) buses. This power converter is formed by a transformer, which provides galvanic isolation, and phase-shifted paralleled rectifier bridge systems [28]. This way, a multi-pulse configuration is achieved. Note that, in order to improve the power quality and meet the aviation standards, several phase-shifted diode bridges are employed achieving an 18-pulse, 24-pulse, or higher pulse number configurations. Although, high reliability and low complexity are the main benefits of these passive systems, a remarkable drawback is found in the employed low frequency transformer since it results in a large volume and weight, and hence, a low power density [4, 6, 10]. Therefore, if these drawbacks are combined with the inherent features of the centralized distribution network structure, a resulting low power density and high weight EPS must be assumed.

On the contrary, the recently furnished MEA decentralized distribution network depicted

in Figure 1.5(b), brings the advantage of a higher flexibility to generate and distribute power efficiently by means of power converters which are located close to the consumption point [1, 22]. The shorter distances between generation and consumption are translated into a reduced amount of cable in the aircraft and, thus, weight and volume savings [27]. Moreover, the increased generation and distribution voltage level to $230\,\text{V}_\text{AC}$, in the case of B787 or A350 models, results in a lower amount of current for the same power transferred and, hence, a lower amount of cable losses and a higher power distribution efficiency [4]. In fact, the conductors rating may also be reduced, and a lower aircraft total cost might be achieved. Consequently, a higher efficiency and a higher power density are obtained in a decentralized EPS compared to the conventional centralized one [22]. However, as previously mentioned, the more the aircraft is electrified the higher the complexity of the EPS.

The greater electrification of loads has led to a higher number of components downstream the AC distribution bus in the MEA EPS. As presented in Figure 1.3(b), not only AC loads and the TRU remain, but also the following components listed below are integrated.

- The *Auto-Transformer Unit (ATU)* is used to interconnect AC distribution (if needed). Thus, it allows to integrate a HVAC bus (such as $230\,\text{V}_\text{AC}$ bus in B787) while maintaining traditional $115\,\text{V}_\text{AC}$ loads of the conventional aircraft [1,2,24]. Compared to the traditional transformers, ATUs offer economic advantages because they share the common section of the High Voltage (HV) winding with the LV winding. In fact, an autotransformer is smaller than a transformer but with relatively similar features. Moreover, the use of a common winding which only carries the difference between LV and HV windings results in a lower copper loss. Hence, for the same amount of losses and current, the ATU contains less copper which is related to a lower system size [24,30,31]. However, the fact that ATUs do not provide galvanic isolation could be considered as a drawback in case of system fault.

- The *Auto-Transformer Rectifier Unit (ATRU)* is based on a phase-shifting autotransformer and a multi-pulse passive rectifier [1, 2, 8, 10, 24]. Therefore, the operating principle is the same as the previously explained TRU operation, but no galvanic isolation is provided. The main difference is that unlike the TRU, which supplies a $28\,\text{V}_\text{DC}$ LVDC bus and loads, the ATRU is used for supplying a HVDC bus and/or HVDC large loads. The established HVDC voltage, in this case, is obtained by directly rectifying the HVAC distribution voltage, being a $270\,\text{V}_\text{DC}$ bus for a $115\,\text{V}_\text{AC}$ distribution voltage as in A380, or a $\pm\,270\,\text{V}_\text{DC}$ bus for a $230\,\text{V}_\text{AC}$ distribution voltage as in B787 [2, 4]. Since supplying large power loads (several kilowatts) by means of the conventional LVDC $28\,\text{V}_\text{DC}$ bus implies a large distribution current and hence large distribution losses, the generated HVDC distribution bus by the ATRU results to be key in terms of efficient feeding of the large loads, such as the ECS or EHA, and increasing the EPS power density [4, 10, 17, 22, 26]

- Due to the existing storage devices in the MEA EPS, the conventional TRU provides an additional feature of operating as a battery charger. Thus, the name of this subsystem is modified to *Battery Charger and Rectifier Unit (BCRU)* in the MEA EPS [1, 11].

- Similarly to the BCRU, a *Buck-Boost Converter Unit (BBCU)* is used for interconnecting the HVDC and LVDC buses which is based in two DC/AC stages interconnected by a high frequency transformer providing galvanic isolation. Additionally, it might provide

bidirectional power flow capability and is used to charge/discharge the LVDC EPS batteries [2, 11, 20, 24].

The implementation of BCRUs, BBCUs, ATUs and ATRUs allows the possibility of supplying different voltage level buses and loads, both AC or DC, in the aircraft EPS [1, 24]. Therefore, power conversion becomes necessary on-board [21]. Moreover, apart from the presented power converters in the simplified B787 EPS schema in Figure 1.3, additional EPS components related to the EPS reliability exist. Among others, the implemented multiple buses that are found to fulfill the redundancies required and allow power transfer in case of emergency operation, the commonly employed tie-breakers to tie the multiple buses together, or other multiple switches and protection systems that are implemented to disconnect power sources, loads, and buses from the aircraft EPS [2, 8, 22, 26]. Figure 1.6 presents the described components in the developed MOET project EPS aiming to represent a closer image to reality about the complexity of the MEA EPS. Note that, even if in the figure the multiple bus concept is only represented in the HVAC distribution bus along with its respective tie-breakers, this concept is also applied to the other buses, i.e. HVDC and LVDC buses [2, 26].
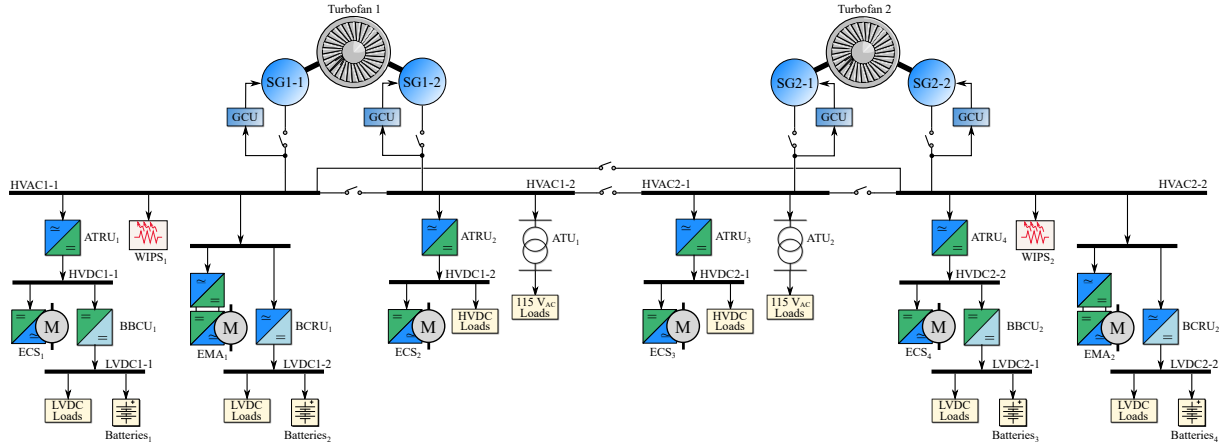
Figure 1.6 Simplified MEA EPS example base on the developed MOET project.

In this regard, the MEA EPS is considered as an isolated microgrid which shares similarities with ground-based microgrids due to the modern distribution network components and complexity. However, several differences have to be taken into account which are related to the aircraft application requirements such as [1, 8, 12, 15, 21]:

- the critical importance of the efficiency and power density which are related to the aircraft overall mass and fuel consumption along the lifetime of the aircraft,
- the increased safety and high reliability of supply requirement which is also related to inherent architectural choices like the architecture structure, the bus isolation and separation or the protection of the supply sources,
- the loads changing priority (landing gear, ECS, WIPS, etc.) during the different flight phases and the fact that some loads might be disconnected to feed the essential ones in case of system failure or power curtailment without compromising the grid stability,

Although these features are part of the existing MEA EPS, a higher improvement is still demanded for future models, for example, in terms of efficiency and power density. According

to [9, 18], the transition to a more electric architecture, the implementation of energy-efficient engines, the development of power electronics and the use of light-weight composite materials will result in a reduction of the operating costs of the nowadays considered the revolutionary MEA. This fact is not only connected to direct costs, such as fuel burn, but also to indirect costs, being maintenance and availability. In fact, since the presented B787 and MOET examples (Figure 1.3(b) and Figure 1.6, respectively) were defined in 2009, innovative EPS topologies and technologies are emerging so that higher weight can be saved while improving the existing EPS efficiency, reliability and safety [11, 20, 32]. In this context, promoting high-efficient and high power density aircraft EPSs has become a research focus [2–4, 9, 10, 15, 16, 24, 25]. The emerging developments concern not only the EPS itself but also its individual subsystems being, generation, distribution, power conversion and energy storage [8, 10, 15, 18].

1.3 The Future MEA Power System: Challenges and Trends

1.3.1 The Development of New Generation Concepts

As previously mentioned, currently the three-stage wound-field machine is used as variable frequency SG in modern MEA, i.e. A350, A380 and B787. The main issue of this machine is related to its inherent weight and volume because, as wound rotor technology with rotating diodes limits the machine speed, the optimization of the machine design in terms of space is considered as limited. What is more, their voltage control through excitation is relatively slow and could not satisfy the requirements of high-dynamic power electronic driven loads [15]. Therefore, research efforts are done to exploit new generation solutions. Essentially, the aim of developing new generation solutions is to boost the generation capability and power density features while maintaining electrical start possibility and high reliability and availability characteristics [3, 21]. In most cases, these new technologies deal with the implementation of active power electronic converters in the main path of energy flow, which enhance the replacement of conventional AC/DC converters [15, 22]. Permanent Magnet Synchronous Machine (PMSM), Induction Machine (IM) and Switched Reluctance Machine (SRM) are considered as suitable choices to substitute the three-stage wound field SG [15, 18, 21, 33].

PMSM is the preferable solution because it provides an excellent power density, high efficiency and well-established control strategies [18, 21, 22]. The use of this technology is indeed being increased for actuator drives due to its high efficiency throughout the full speed range and ease of refrigeration compared to classical wound machines [19]. In addition, the employment of a PMSM as direct wheel machine in A320 model is also under research for electric taxiing and/or energy recovery when landing, hence demanding bidirectional power flow operation [22, 33–35]. However, its inability to operate and high temperatures, medium reliability, medium fault-tolerance capability and high cost are considered as PMSM drawbacks. A higher level of reliability and fault-tolerance capability is presented by IM but without achieving PMSM power density levels. In the same way, SRM power density is not as high as PMSM's, but the simple rotor construction and its robustness permits SRM to operate in harsh envi-

ronments [18, 19]. The inherent fault-tolerance and high-speed operation capability make also this machine attractive for MEA applications, which in fact was employed in 2005 in Lockheed Martin F-22 model [10, 18]. However, its high torque ripple and the emitted acoustic noise are considered as notorious drawbacks [21].

A different concern related to generation systems focuses on the aircraft generation capability [4, 17, 18]. Due to the increasing electrification of loads, and hence power demand, any additional potential source of power generation results interesting for the future MEA EPS. On the one hand, the multi-spool concept is being investigated. Aircraft jet engines are typically based on more than one spool or shaft. The propulsion fan, low-pressure compressor stages and low-pressure turbine stages are connected to the low-pressure spool. Conversely, the high-pressure compressor and the high-pressure turbine stages are connected to the high-pressure spool. This concept constitutes a two-spool engine [22]. The higher speed of the high-pressure spool compared to the low-pressure spool speed results beneficial to allow smaller size generators. Consequently, since current modern aircraft use turbofan engines for propulsion, the electrical generators are located in the high-pressure spool of the turbofans [18, 22]. Nevertheless, the engine performance can be negatively affected if an increased shaft power extraction occurs at the high-speed shaft. Therefore, generating through multiple spools (i.e. taking advantage of both high-pressure and low-pressure spools) becomes a potential solution which, indeed, demands a higher number of power electronic converters [18, 22].

On the other hand, the hybridization of power sources with storage devices is also contemplated. Storage capacity and its contribution to the EPS peak power loads would allow to under-rate generation power sources [11, 15]. Fuel cell technology is considered as attractive due to their lightweight and lack of harmful emissions delivery. Further research is still needed for this technology which has already been demonstrated in smaller aircraft [15]. Current trends related to fuel cell technology focus on their integration in the aircraft system with other sources of energy so that the weight and size of the existing APUs is reduced owing to an additional piece of power electronics [15, 22]. The possibility of replacing the APU by fuel cells, batteries and supercapacitors is also contemplated due to the low efficiency of APUs [4, 10, 15, 17, 27, 32]. In terms of technology maturity, however, the multi-spool generation concept results easier to be implemented compared to the development of batteries or fuel cells which fulfill high-power demand requirements [11]. Consequently, a special focus should be put on the active power converters between generation and distribution.

1.3.2 The Development of New Generation Concepts

At the time that generation systems are being developed, the distribution network is also a point to be encouraged in order to ensure a high-efficient, reliable and effective power supply. Although the recent State-of-Art in this topic highlights the increased AC distribution voltage to $230\,\mathrm{V_{AC}}$, strong research focuses on the future possibility of implementing a HVDC primary distribution bus [1, 4–6, 15, 17, 18, 20, 22, 26, 27]. The arriving idea of HVDC power transferring in aircraft applications is, indeed, a relatively long-standing proposal. Some emerging standards even incorporate the regulated voltage levels of $270\,\mathrm{V_{DC}}$ and $540\,\mathrm{V_{DC}}$ (or $\pm\,270\,\mathrm{V_{DC}}$) as common

distribution voltages [9]. Note that these voltage levels are not expected to increase for the MEA due to the strong development of the isolation materials required according to the Paschen's Law [32].

Apart from the hybrid EPS of Figure 1.6, the EPS based on HVDC as primary distribution voltage in Figure 1.7 was also presented in MOET European Union (EU) project [4,20]. It was concluded that 270 V HVDC primary distribution for power transferring provides some crucial benefits compared to the conventional 115 V_{AC} distribution:

- the integration of a HVDC network eases the fact of paralleling power sources and makes the network more flexible;

- the reduction from 3 to 2 cables could result in cable weight saving;

- weight saving in powerful loads like Electro-Mechanic Actuator (EMA), EHA or WIPS due to the lack of a rectifier stage at equipment input;

- the possibility of on-board power management optimization is allowed thanks to energy recovering and storage solutions.
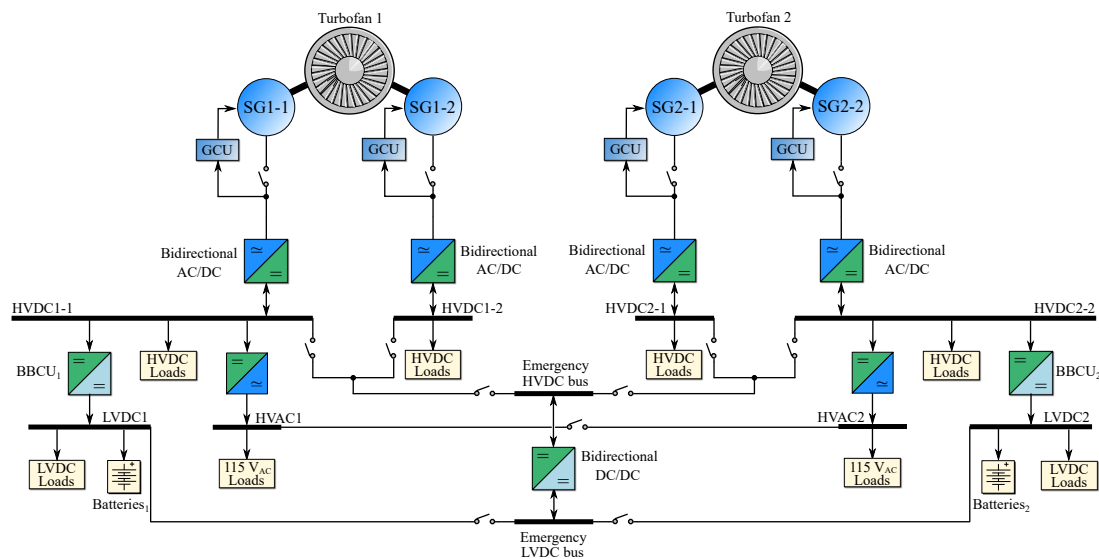
Figure 1.7 Developed HVDC primary distribution-based MOET EPS.

In line with the MOET research, in [26] the difference between the conventional 115 V_{AC} distribution and other HV distribution buses, being 230 V_{AC} HVAC or ± 270 V_{DC} HVDC, was investigated in terms of EPS weight and efficiency. It was reported that a major role in the optimization of the future EPS would be held by weight, efficiency, safety, reliability and cost. In this regard, it was calculated that, for a 10 kW load and assuming ± 270 V_{DC} HVDC distribution, the power transmission losses could be reduced about a 33 % with respect to the 230 V_{AC} HVAC distribution system and about a 67 % with respect to the conventional distribution system. Moreover, assuming that the aircraft aluminum fuselage is used as a return conductor, the HVDC distribution system could use a positive polarity single conductor and use the fuselage as ground, thus enabling a potential cable weight and costs reduction. In addition, the HVDC distribution system does not require reactive power compensation, which might also be related to a lower amount of current handling. The total weight of the on-board power converters

would also be influenced by the evolution to HV distribution power systems. Considering a total cabin power of 100 kW a weight saving of 242 kg was expected in HVAC system while the HVDC system integration resulted in 364 kg saving. The weight saving of the cargo and cabin feeders and the galley feeders was also analyzed assuming a decentralized architecture based on 6 secondary power distribution buses. The results showed a 50 % and a 60 % weight saving for cabin and cargo feeders for HVAC and HVDC distribution systems, respectively, and around a 25 % and a 50 % weight saving regarding galley feeders. As a result, it was concluded that implementing the HVDC primary distribution approach might result in potential benefits in terms of efficiency, weight savings and costs, although a research focus must be put into HVDC protection systems.

In [4] four different EPSs were evaluated in terms of weight. These power systems were described as: *EPS-A1* representing the conventional 115 V_{AC} and 400 Hz CF EPS, *EPS-A2* being the hybrid EPS of Airbus A380 with primary 115 V_{AC} and 360-800 Hz VF distribution and an additional 270 V_{DC} secondary distribution bus, *EPS-A3* exemplifying the hybrid EPS of Boeing B787 with primary 230 V_{AC} and 360-800 Hz VF distribution and an additional ± 270 V_{DC} secondary distribution bus, and *EPS-A4* symbolizing the ± 270 V_{DC} primary distribution based pure HVDC EPS. Considering *EPS-A1* as the baseline case, it was concluded that removing the gearbox resulted beneficial in terms of weight and efficiency in *EPS-A2 – EPS-A4*. Similarly, increasing the distribution voltage from 115 V_{AC} (in *EPS-A1* and *EPS-A2*) to 230 V_{AC} (in *EPS-A3*) or ± 270 V_{DC} (in *EPS-A4*) resulted in approximately a 35 % cable weight reduction. In addition, due to the fact that the switching power supplies suppose about the half of the aircraft EPS distribution weight, it was concluded that a lower amount of power conversion stages could be required if a HVDC distribution such as the one of *EPS-A4* was implemented, hence, enabling a significant weight reduction. Furthermore, the HVDC primary distribution would also ease the integration of alternative energy generation sources like batteries or fuel cells. The main drawback that was identified, though, was that the existing GPUs operate at 115 V_{AC} and 400 Hz and, therefore, an additional transformer would be required in *EPS-A3* and *EPS-A4* to allow for external feeding in ground operation. Since it is unlikely to force the airports to employ additional transformers because of the investment required, a weight increase was expected due to the installed transformers on-board. All in all, it was concluded that a high potential could be expected for HVDC primary distribution.

Similar oriented research but related to the weight saving impact of different HVDC distribution levels was conducted in [27]. ± 135 V_{DC}, 270 V_{DC}, ± 270 V_{DC} and 540 V_{DC} voltage levels were considered as suitable primary distribution choices. Among other characteristics, isolation of the SG side and 115 V_{AC} or 230 V_{AC} feedings were also considered. The study proposed a 115 V_{AC} decentralized distribution network with eight secondary power distribution boxes as benchmarking and exhibits the DC possibilities mentioned above, both considering a centralized and a decentralized operation. As a result of the study, the decentralized architectures presented higher weight savings than the centralized possibilities. Concretely, 270 V_{DC} architecture with 115 V_{AC} supply presented the best performance (28 % total saving) followed by the ± 270 V_{DC} with 230 V_{AC} supply (21 % total saving). The latter option presents the advantage of lighter generator cables but the disadvantage of needing a transformer for the 115 V_{AC} external feeding.

On the contrary, the first choice does not need a transformer but it considers the current return through the fuselage. In this case the neutral points of all generators must be isolated (including external) which is possible as per ISO 6858 requirements.

Thus, in relation to the previously presented research works, it is observed that a significant tendency exists related to the development of HVDC-primary distribution-based EPS due to the reduced overall weight and increased distribution efficiency [15]. As in the B787 HVAC-based distributed architecture, in the HVDC-based distributed EPS topology presented in Figure 1.8(a), the AC/DC converters and the primary distribution power buses are located close to the generators (with high power contactors and circuit breakers) while the HVDC power is transferred to the Secondary Power Distribution Units (SPDU) or management systems, which are located close to the loads [12, 15]. Thus, weight benefits are provided by cable harness optimization. These power distribution and management systems make use of available power providing fully automatic monitoring, control, protection, and switching of aircraft electrical loads under normal and emergency conditions.
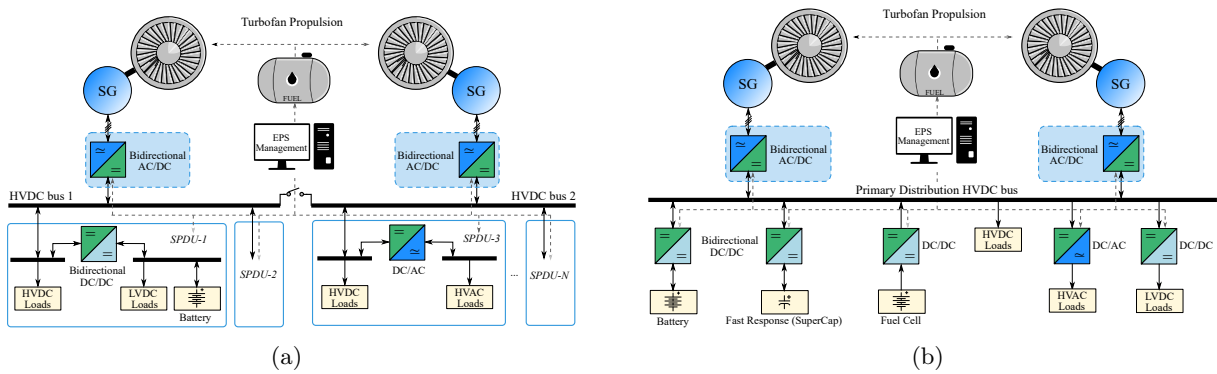

Figure 1.8 Simplified potential EPS architectures to be implemented in the future MEA based on a HVDC primary distribution bus, being (a) a distributed EPS and, (b) single-bus EPS.

A strong trend involving "*Single-bus*" theory, depicted in Figure 1.8(b), is also considered as potential future MEA EPS [8, 15, 36]. According to the structure of this EPS, a single HVDC distribution bus is implemented where all loads and power sources are connected. Thus, no multiple power buses nor SPDUs are found in this EPS approach. The single bus topology becomes possible as a result of the introduction of primary sources which are controlled by active Power Factor Correction (PFC) power converters. Key potential benefits involve the ease of establishing the optimal power and load allocations by means of decentralized droop control, and the ease of integration of alternative energy sources. As a result, a reduction of power source design ratings is achieved leading to an overall EPS weight reduction. Research challenges focus on ensuring compliance with power quality requirements and fault protection strategies.

In relation to the challenges on power quality and protections systems development, the evaluation of an innovative EPS structure approach, components layout and its protection strategy result an interesting research task. In fact, the distributed-based and the Single-bus-based approaches are the exclusive EPSs presented in literature for future aircraft applications. Based on the EPS structure evaluations performed for electric vessels [37, 38], an additional relatively simple EPS layout known as "*Ring-bus*" topology approach in Figure 1.9, could be considered for

aircraft applications. In this sense, a trade-off analysis should be required among the expected simplicity and high efficiency of the single-bus approach, compared to the higher reliability and reconfigurability degree in case of fault owing to a higher number of protection systems of the Ring-bus type approach [37]. In fact, the higher the number of protection systems, the lower the expected efficiency and higher weight of the power system. On the contrary, a higher number of protection systems might result beneficial to accurately isolate a system fault. Note that, due to the typically low impedance presented by DC distribution networks, the fault propagation speed is increased compared to AC distribution systems [37, 39–41]. Thus, a large voltage drop might be experienced throughout the whole aircraft distribution system making the conventional selectivity strategy of the protection systems unsuccessful [41, 42]. Consequently, different protection strategies and devices should be evaluated for a specific aircraft low impedance DC distribution network.
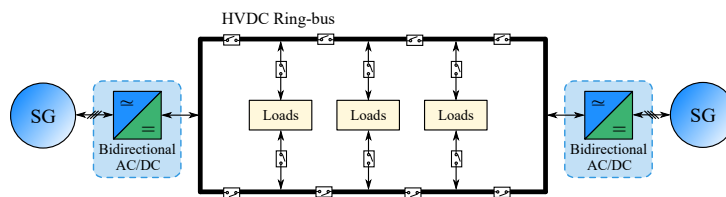

Figure 1.9 Ring-bus type schematic example.

It is worth to mention that, based on the single-bus EPS topology, and even if the current state of technology evolves towards the MEA concept and its architecture development, an additional trend in aerospace does exist towards greener aviation [7, 15, 43]. This trend is the electrification of the aircraft propulsion system, which is also going under research aiming to achieve an energy-efficient, less polluting and quieter aviation [10, 15, 18, 32, 44, 45]. In contrast to the required generation capability of several hundreds of kW in MEA, though, an extensive power generation capability of MegaWatt scale and distribution of kiloVolt scale will be needed to provide electric propulsion (note that no standard distribution requirements have been defined yet) [5,7,8,10,43]. The possibility of electric propulsion enables the aircraft operation dependence on kerosene to be reduced, or even eliminated, and the propulsive force is delivered by powering electrically driven propellers instead [46].

Hybrid-electric propulsion systems are being studied for future larger commercial Hybrid Electric Aircraft (HEA). A simplified power system schema of the HEA is presented in Figure 1.10(a). This power system combines a gas turbine or internal combustion systems with electrical power generation and storage systems, and commonly an electrically driven fan or propeller. Thus, additional electric energy can be used for assisting acceleration while reducing fuel consumption. Besides, if high electric power is demanded, a bidirectional flow of power is possible between the storage systems and electrical propulsion machines. The all-electric-propulsion-based power systems (see Figure 1.10(b)), on the contrary, are based only on electrical power which is generated in storage systems such as fuel cells, batteries or capacitor systems [7, 10]. The lack of technology development (i.e. electrical power generation capability) as well as the volume of power conditioning equipment and the advanced control required make the development of these concepts still unfeasible, especially for commercial and civil transporta-

tion applications [10, 19]. Key technology challenges for the electrically propelled All Electric Aircraft (AEA) and HEA follow the lead of MEA concept in terms of improving the efficiency and power density of power electronic converters and in boosting the EPS protection and fault tolerance, among others [7, 10, 16, 26].
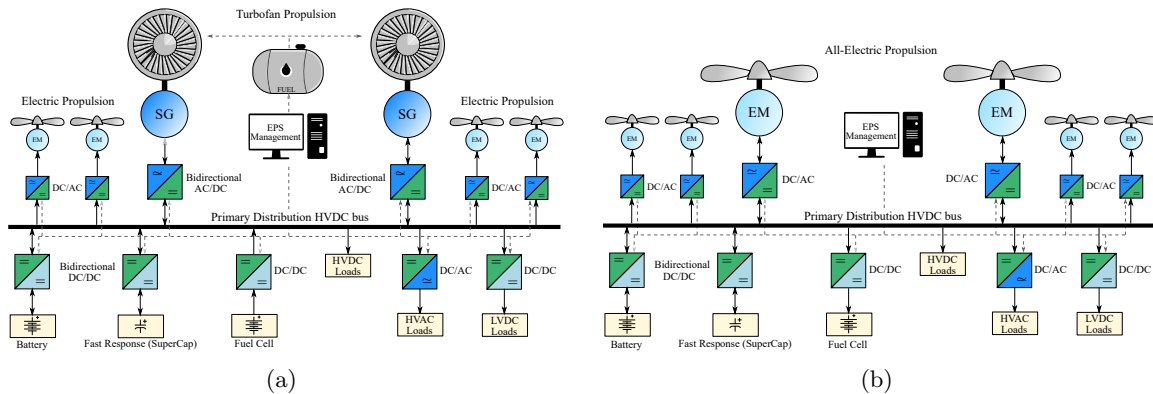

Figure 1.10 Examples of the simplified EPS schema of (a) the HEA and, (b) the AEA

1.3.3 The AC/DC Power Electronic Converter in the Future MEA

Due to the inevitable aircraft EPS electrification and the HVDC distribution grid integration, the AC/DC power converter becomes a research focus in order to achieve the future MEA concept implementation. Unquestionably, the AC/DC rectification is one of the demanded applications to integrate voltage controlled HVDC networks, increase the overall system efficiency, reduce the EPS weight and, ease the EPS maintenance while increasing availability [12]. In fact, the AC/DC rectifier can be considered as a critical path from SGs to loads and, thus, becomes one of essential research areas [14, 17, 26, 47]. Furthermore, taking into account the advancement of future technologies and a robust HVDC distribution network establishment, the use of high power density electrical components so that the AC/DC rectification stage is able to drive the majority of aircraft subsystems is expected to become feasible. According to [7] the expected road-map that power electronic converters will follow, and hence, the AC/DC power converter, is presented in Figure 1.11.

As previously described, in the existing MEA power systems, the HVDC bus is generated by a passive ATRU [2,15,22]. This system is featured by its low costs, high reliability, and simplicity [48]. Its low power density and non-controlled output voltage, though, demand the development of new technologies that satisfy the operating, power quality, and harmonic requirements of aviation standards, such as MIL-STD-704F or DO-160G [49].

Therefore, in pursuance of enabling the implementation of a HVDC primary distribution-based EPS, as in Figure 1.8, 1.9 and 1.10, and the replacement of the bulky unidirectional passive ATRU, active PFC rectifiers are considered as a potential option to encourage aircraft electrification [15,21,22,50]. Compared to passive solutions, active PFC converters are featured for improved power quality and reduced weight and volume. Additionally, continuous progress under the MEA concept not only requires the inclusion of advanced power electronic designs, but

also innovative concepts, such as the electrification of the propulsion system employing bidirectional power flow rectifiers for future aircraft power systems (see Figure 1.8) [10,18,22,32,44,45]. However, a literature gap can be found regarding the implementation active rectifiers while complying with the existing aviation standard operation requirements, which are based on the passive ATRU operation. Although several active rectifier designs and comparative analysis among different topologies can be found in literature [45,48,51], the presented converters do not fulfill the with the standardized input/output voltage requirements, being $115\,\mathrm{V_{AC}}$ to $270\,\mathrm{V_{DC}}$ or $230\,\mathrm{V_{AC}}$ to $\pm270\,\mathrm{V_{DC}}$ rectification scenario depending on the manufacturer. Thus, a suitability analysis of active rectifiers becomes necessary to verify their future potential in aircraft applications. Moreover, the achievable power, efficiency, power density and reliability/availability of these active rectifier topologies are, currently restricted by state-of-the-art technologies [50].
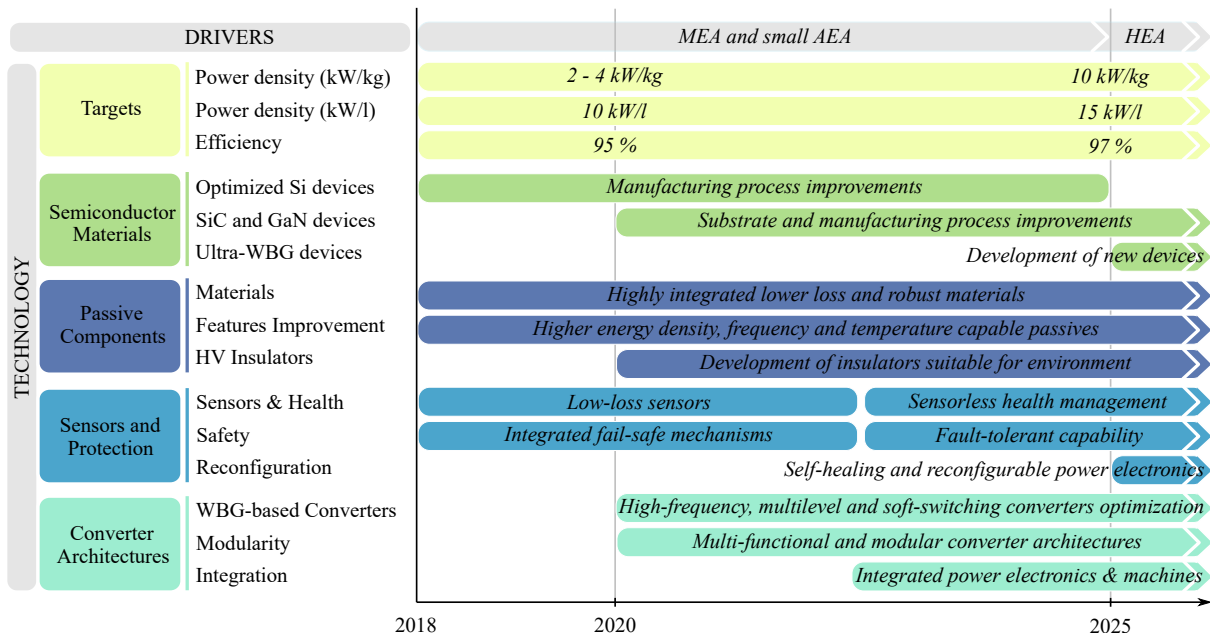
Figure 1.11 Road-map of power electronic converters for the coming years.

In this context, it is believed that implementing Wide Band Gap (WBG) semiconductor technologies will be advantageous, due to increased converter efficiency. Among the benefits provided by WBG devices, such as Silicon Carbide (SiC) or Gallium Nitride (GaN), a low on-resistance and a faster switching capability compared to traditional Silicon (Si) devices can be found [5, 18, 24, 47, 52–58]. Therefore, apart from achieving low conduction and low switching losses, other features, such as a higher efficiency, lower cooling effort, and a reduced volume for passive elements can be expected from WBG-based converters. Additionally, the higher and more efficient switching speed capability can be accomplished with lower difficulty power quality requirements, without employing bulky filters.

In addition, among the major challenges, the design of an active power converter rated at a high power, in order to supply the increasing electrified aircraft power demand, is considered to be a complex task [4, 18, 50]. According to [59], important power demand fluctuations can occur in large MEA loads, such as the ECS, during the flight mission. Besides, the power demand profiles of the large loads are typically different one from each other. Hence, dedicating

a single power converter per load results in several drawbacks related to reliability (the power converter loss implies the load loss), high costs and a low utilization ratio considering that loads are intermittent [59, 60]. Thus, parallel operation and modular converter approaches are encouraged, aiming, for instance, to achieve an increased overall converter architecture power rating with a high degree of redundancy [10, 32, 50, 61]. In addition, it is considered that a higher degree of modularization permits the possibility of designing a fault-tolerant systems [8]. One example is presented in Figure 1.12, in which a modular architecture viable design is assumed to be achieved without compromising the safety and reliability criteria while fulfilling the aircraft operational requirements [32].
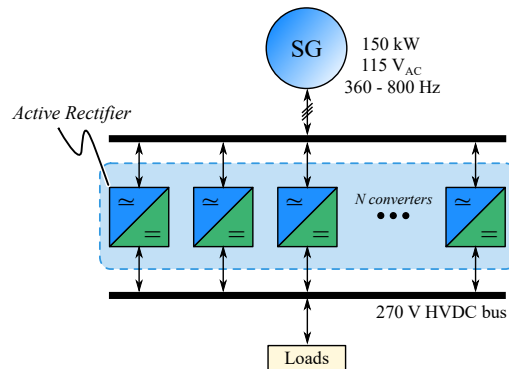

Figure 1.12 Simplified example of the proposed bidirectional active modular rectifier architecture.

In this context, not only the suitability of active rectifiers in MEA applications should be verified, but also the integration of these power converters into a modular architecture which apart from complying with aviation standards provides a high degree of reliability and fault-tolerance operation. Currently, few information is available regarding modular converter architectures for MEA and/or electrically propelled aircraft. In [61], parametric design studies and analysis are presented regarding a HEA considering distributed propulsion and physics-based models of electrical machines, power converters, batteries, solid-state circuit breakers and cables. Bidirectional power converters between SG and the distribution system are considered and a modular approach is mentioned for these converters, but neither their architecture structure nor the converter design are detailed. The suitability of high-power active rectifier for HEA is presented in [50]. However, a 3 kV DC voltage bus is considered in order to achieve high power rating. Further, the architecture and converter AC input filter design and power quality fulfillment are not contemplated. Therefore, due to the lack of modular converter architecture designs for aircraft applications, research and development of innovative and reliable power converter architectures with prominent features of high power aside from diminished mass and volume is required for future MEA [18, 50].

1.4 Thesis Motivation and Objectives

Based on the coming development of the future MEA architecture in terms of the required high efficiency, high power density, compact and reliable power conversion and distribution, the motivation of this thesis is to answer the questions regarding the suitability and implementation

of an active modular rectifier architecture in the future MEA. Thus, a comprehensive analytical design and comparative analysis among different active modular rectifier architectures in terms of efficiency, power density (referred to volume) and reliability is presented in order to find the most suitable architecture option. Aiming to ensure a high reliability of supply, an analysis regarding the architecture protection is also performed and simulated. Therefore, the main objectives of this research work are summarized as follows:

(1) Provide an overview of the MEA EPS in order to understand the importance of the AC/DC rectifier and the migration to an HVDC-based distribution system in the future aircraft EPS and define the coming challenges to be faced.

(2) Verify analytically the suitability of active rectifier topologies in current MEA applications and their advantageous implementation with respect to the existing State-of-Art ATRU technology.

(3) Design and compare different active modular rectifier architectures in order to find the most suitable option in terms of efficiency, power density and reliability while fulfilling the existing aviation standards.

(4) Analyze and simulate a protection strategy for the active modular rectifier architecture which ensures a high reliability of DC power supply to the HVDC primary distribution bus without compromising the aircraft DC-side EPS.

1.5 Outline of the Document

Figure 1.13 illustrates the structure of this document which, indeed, is aligned with the research work accomplished. The contents of each chapter are described in the following.

⟶ Within this introductory **Chapter 1**, a literature review of the evolution of the aircraft EPS is summarized, presenting the coming challenges of future MEA regarding generation, power conversion and distribution. In this context, the challenges related to the AC/DC rectifier have been identified in order to implement a high-efficient and high-power-dense HVDC primary distribution-based EPS which provides additional capabilities such as bidirectional power for motoring applications. The performed review leads to the motivation and objectives of this research work which are further analyzed in the following chapters.

⟶ Among the AC/DC rectifier challenges, **Chapter 2** proposes the suitability study for replacing the traditional and unidirectional passive ATRU by a bidirectional active power converter which fulfills the existing aviation operating requirements. A State-of-Art related to the potential AC/DC topologies to replace the ATRU is presented from which, by means of a technical approach, a comparative analysis is performed to identify the most interesting AC/DC topology.

⟶ In **Chapter 3**, the integration of an active rectifier topology into a modular active rectifier architecture which complies with the aviation standards is treated. Three different converter configurations are proposed for forming a bidirectional active modular rectifier architecture. Thus, the proposed potential three configuration-based architectures are designed and compared in a higher detail comparison framework which focuses on efficiency,

power density (referred to volume), reliability and complexity parameters. Then, the resulting active modular architecture is simulated in steady-state operation and its potential challenges for implementing it into the MEA EPS are identified.

⟶ The DC-side protection of the proposed active modular rectifier architecture is studied in **Chapter 4**. The existing DC protection devices are reviewed and a discussion among the suitable protection devices to be employed in aircraft applications is provided. The proposed active modular architecture is simulated under fault condition to verify the suitability of the suitable DC protection devices. In addition, aiming to enhance the proposed active modular architecture implementation into the MEA EPS and analyze its behavior to external faults, an evaluation of two EPSs is done by means of a proposed methodology which evaluates the distribution efficiency, weight, survivability and fault clearing speed of each architecture under different fault scenarios. Thus, the complete system behavior under normal and fault operation is studied and the implementation of the active modular architecture under the proposed protection scheme is verified.

⟶ Finally, **Chapter 5** summarizes the main conclusions of this research work as well as the main scientific contributions. Furthermore, a proposal of the potential future research lines is described to further continue the investigations on the integration of the active modular rectifier architecture in the electrified aircraft.

Ch. 1 - Introduction

Ch. 2 - Suitability Analysis of Active Rectifier Topologies in MEA Applications

Ch. 3 - Comparative Analysis of Active Modular Rectifier Architectures Integrated in MEA

Ch. 4 - Protection and Integration of the Active Modular Architecture into the MEA EPS

Ch. 5 - Conclusions
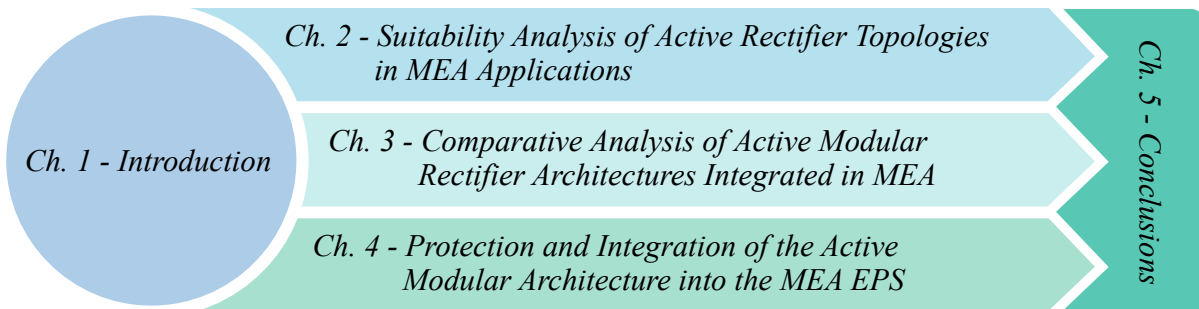
Figure 1.13 Description of the document structure.

CHAPTER **2**

Suitability of Active Rectifier Topologies in MEA Applications

Abstract:

In pursuance of enabling the implementation of a high-efficient and high-power-dense HVDC primary distribution-based EPS, and the replacement of the bulky unidirectional passive ATRU, active rectifiers are considered as a potential option to encourage aircraft electrification. Thus, the suitability of active rectifiers fulfilling the operating requirements of MEA applications is studied in this chapter. On the basis of a literature review and classification of AC/DC rectifiers, active rectifier topologies result the preferable option to replace the traditional ATRU. However, under the premise of the existing standardized input and output voltage operating requirements, based on ATRU operation, controllability limitations can be found for active rectifier topologies if unity power factor operation is desired.

Thus, two different converter operating possibilities are proposed to avoid the controllability limitations: (1) employ two-stage configuration based on an AC/DC and a downstream DC/DC which operates at unity power factor, and (2) employ a single-stage configuration with a lowered power factor operation. Considering these two scenarios, the performance of the potential active rectifier topologies is benchmarked against the one of the conventional ATRU aiming to identify the most suitable solution to be implemented in MEA applications.

2.1   Application Requirements and Operating Scenario

Research surrounding high-efficient and high-power-dense EPS for aircraft applications encourages the migration to HVDC primary distribution-based power systems [1, 15, 17, 20, 27]. In the up-to-date existing commercial MEA models, i.e. Airbus A380 and Boeing B787, the HVDC distribution bus is generated by a passive ATRU and used for supplying the recently electrified large loads such as the ECS in B787 model or the EHA and EMA in the A380 [2, 15, 22]. The ATRU is featured by its low costs, high reliability, and simplicity [48]. However, aiming to establish a high-efficient primary HVDC distribution-based network, the low power density and non-controlled output voltage characteristics of the ATRU demand the development of new technologies that satisfy the operating, power quality, and harmonic requirements of aviation standards, such as MIL-STD-704F or DO-160G [49]. Thus, based on aviation standards and in order to properly select a rectifier topology for replacing the ATRU, a comparative analysis is required among different potential rectifier topologies. Furthermore, the analysis should be framed in a standardized rectification scenario between the ones employed in A380 and B787 MEA models, being $115\,V_{AC}$ SG voltage to $270\,V_{DC}$ HVDC distribution voltage or $230\,V_{AC}$ SG voltage to $\pm\,270\,V_{DC}$ HVDC distribution voltage, respectively.

These two rectification scenario approaches were applied to a distributed aircraft power system and evaluated in terms of weight in [4, 27]. On the one hand, it was concluded that applying the higher voltage level rectification scenario, i.e. $230\,V_{AC}$ to $\pm\,270\,V_{DC}$, could be beneficial in terms of cable weight. On the other hand, since the airport GPU operates at $115\,V_{AC}$ and $400\,Hz$, an additional transformer would be required to allow for external feeding in ground operation. Since installing this transformer in the airport GPU would result an additional investment for the airport, which is unlikely to happen, the contemplated possibility was to assume the transformer installation on-board the aircraft and hence, an increased power system weight could be expected in this sense. Overall, [27] concluded that an additional $7\,\%$ weight saving could be expected from the $115\,V_{AC}$ to $270\,V_{DC}$ rectification scenario approach, and thus, it is selected as the operating scenario in this research work. Furthermore, the $115\,V_{AC}$ to $270\,V_{DC}$ rectification scenario is the one currently standardized in [29, 62]. It must be remarked, though, that even if some figure of merits could change depending on the rectification scenario, it is expected that the analysis performed in this research work could also be extrapolated to the higher $230\,V_{AC}$ to $540\,V_{DC}$ ($\pm\,270\,V_{DC}$) rectification approach.

Beyond the selection of the rectification scenario, the future challenges that the selected AC/DC topology must face should also be considered as an application requirement, being [7, 12, 18]:

- Achieving an operating efficiency equal or greater than $97\,\%$.
- Operating with a regulated output voltage level.
- Be able for governing the increasing amount of generated power efficiently.
- Providing small input current harmonics to minimize losses and high input Power Factor (PF) to minimize reactive power handling.
- Operating in a wide VF range.

- And, if possible, allow engine start by bidirectional power flow capability.

Note that, the features related to input/output voltage operating scenario, power quality (referred to Current Total Harmonic Distortion, THD_i) and VF range operation are already described in DO-160G aviation standard [62]. These requirements are summarized in Table 2.1.

Table 2.1 Application requirements and future targets.

Parameter	Value	Unit
Nominal phase RMS voltage, V_{ph}	115	V
Steady-state phase RMS voltage	100 - 122	V
Steady-state SG frequency, f	360 - 800	Hz
Power Factor, PF	0.85 lagging - 1	-
Input current distortion, THD_i	≤ 3	%
V_{DC}	270	V
Steady-stateDC voltage	250 - 280	V
SG & Architecture power rating	150	kW
Targeted efficiency, η	97	%
Power flow	Bidirectional	-

Moreover, since the defined input/output voltage operating scenario is already employed in Airbus A380 commercial model, an EPS formed by four SGs with a power rating per SG of 150 kW has been considered in this research work [2, 4, 10, 18, 22]. Note that this nominal SG power should also be transferred by the AC/DC conversion stage to the HVDC distribution bus. In this context, a modular converter approach is assumed to transfer all the SG power from generation to distribution. This way, the fact of implementing a converter being a single point of failure is avoided and a high degree of reliability and redundancy of power supply is achieved. An example of modular rectifier redundancy is illustrated in Figure 2.1.
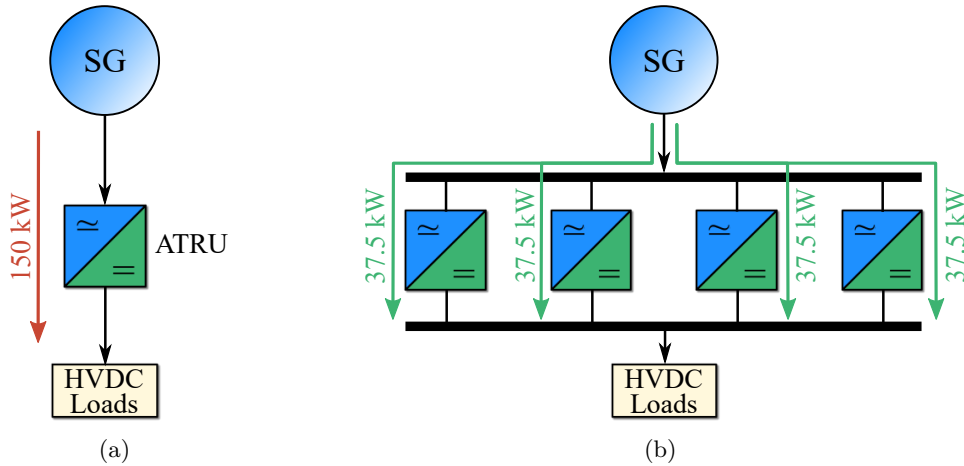
Figure 2.1 (a) Schematic of an AC/DC converter. (b) Operating output DC voltage range of three-phase AC/DC rectifiers depending on V_{conv}. Unity PF is considered for hybrid and active rectifiers.

In Figure 2.1(a) only a single converter is used for transferring all the SG power to the loads. Hence, if this ATRU fail, no power could be transferred. That is, the ATRU is considered as a single point of failure. In aircraft applications, though, "*four parallel feeding paths*" are typically

assumed to accomplish the reliability and redundancy purposes in communication systems or other powered subsystems, such as flight controls and actuators in the A380 [63, 64]. This way, if a converter module fails, the 75 % of the SG power is still available. Therefore, if this concept is applied to the AC/DC conversion stage linked to the SG, four converter modules could be assumed to transfer 150 kW SG power rating (see Figure 2.1(b)). This fact leads to a first approach of 37.5 kW nominal power per converter module.

2.2 Classification of the AC/DC Rectifier Topologies

Numerous rectifier topologies can be found in literature such as the ones presented in the review research works of [6, 49, 65–68]. In order to cover a wide range of potential topology possibilities, a literature review and classification of the potential AC/DC topologies for the defined MEA application is considered as the initial point to focus on. This way, the pros and cons of the potential topologies can be analyzed and a proper topology selection can be done for the defined application.

The classification of the potential topologies presented in the following is based on a simplification of the one presented in [6, 49] and is graphically depicted in Figure 2.2. Therefore, it must be remarked that depending on the classification criteria, the review of the existing AC/DC topologies could be different to the one presented in this work. For example, since no galvanic isolation is required in this application, the topologies associated to this feature have not been considered due to their presumable high weight. As illustrated in the figure, the considered rectifier topologies are classified into three main groups, being passive converters, hybrid converters and active converters.
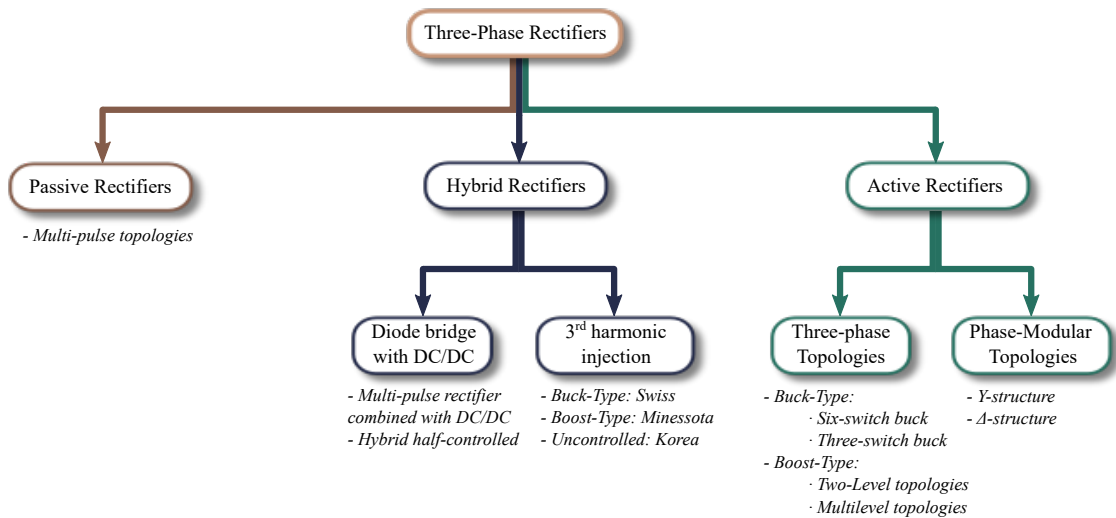
Figure 2.2 Simplified classification of potential rectifier topologies for the defined MEA application.

Passive converters such as the ATRU are based on mains-commutated diodes and passive filters for sinusoidal current and voltage shaping. The fact of being operated with non-controlled diodes results in a lack of output voltage regulation control and in Low-Frequency (LF) harmonics in the input current. Hybrid converters contain mains-commutated diodes and active power

devices which, altogether, make hybrid converters present either partially controlled input currents and/or output voltages. Among the main drawbacks the higher number of power devices is found, which may lead to higher conduction losses than passive rectifiers. On the contrary to both of the previous converter types, active converters are based in active power devices and, hence, they can exhibit a controlled output voltage and sinusoidally shaped input currents.

Particularly, due to the output voltage control characteristic of hybrid and active converters, the topologies contained in these last two groups could also be further subclassified into *buck-type* and *boost-type* rectifiers. It is worth to mention that, aiming to provide output voltage control: *(1)* boost-type rectifiers require the DC bus voltage to be larger than the input terminals line-to-line voltage and, *(2)* buck-type rectifiers, on it behalf, require the DC bus voltage to be lower than the terminals line-to-line voltage [69, 70].

These last two concepts are graphically presented by Figure 2.3. Concretely, Figure 2.3(a) presents an example which graphically describes what the line-to-line RMS converter terminals voltage, V_{LL}, and the output DC voltage, V_{DC}, of an AC/DC power converter are. Note that V_{LL} is related to the converter phase-to-neutral RMS terminals voltage, V_{conv}, as $V_{\mathrm{LL}} = \sqrt{3} \cdot V_{\mathrm{conv}}$. Thus, in accordance to [49, 69, 70], the subclassification depicted in Figure 2.3(b) places boost-type converters in the red area providing a minimum output voltage of $V_{\mathrm{DC}} > \sqrt{2} \cdot V_{\mathrm{LL}} = \sqrt{6} \cdot V_{\mathrm{conv}}$, and, buck-type converters in blue area providing a maximum voltage of $V_{\mathrm{DC}} < \sqrt{9/2} \cdot V_{\mathrm{conv}}$.
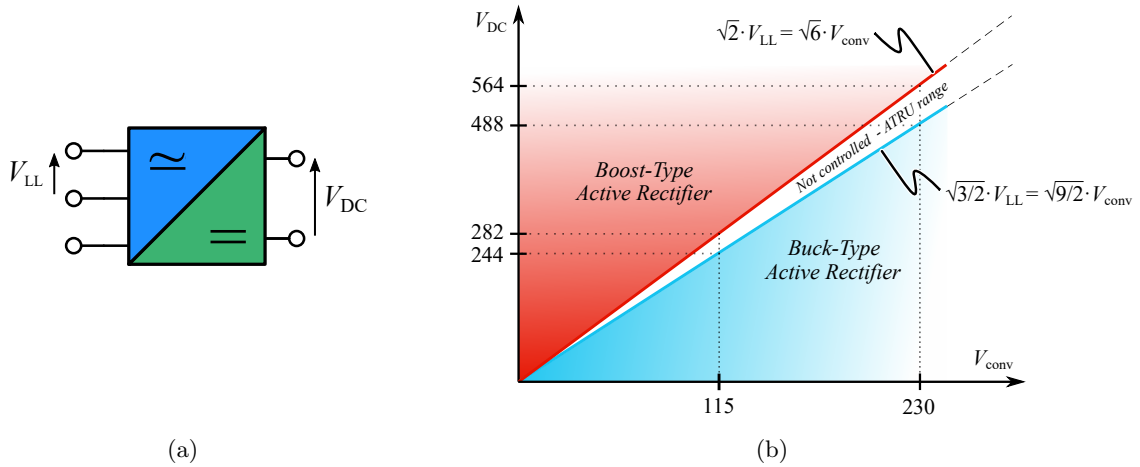
Figure 2.3 (a) Schematic of an AC/DC converter. (b) Operating output DC voltage range of three-phase AC/DC rectifiers depending on V_{conv}. Unity PF is considered for hybrid and active rectifiers.

In this regard, special attention should be given to the defined steady state output voltage between $250\,\mathrm{V_{DC}}$ and $280\,\mathrm{V_{DC}}$ for the specified input voltage of $115\,\mathrm{V_{AC}}$ in Table 2.1. This output DC voltage range, typical for passive ATRU operation indeed, is identified as an uncontrolled output voltage range for hybrid and active rectifiers in Figure 2.3(b) (either buck-type or boost-type) when operating at unity PF [48, 49]. Therefore, both output voltage characteristic topologies are considered in the classification.

It is worth to mention that, in an attempt to cover the uncontrolled voltage range with hybrid and active rectifiers, an additional DC/DC stage must be employed to achieve an output voltage of $270\,\mathrm{V_{DC}}$ [49]. Existing alternatives to implementing the second power stage involve

the three-phase extension of buck-boost, Flyback, Cuk- or Sepic-converters. However, due to the high complexity of the resulting circuits, these approaches are yet considered for theoretical interest and consequently are not considered in this work [49].

2.2.1 Passive Rectifiers

Considering the up-to-date HVDC bus of modern MEA, passive rectifiers constitute the currently employed rectifier technology, i.e. the ATRUs described in Chapter 1. As previously mentioned, these power converters are featured by a purely mains-commutated rectification performance, based on diode bridges, and phase-shifting transformers. The reason of using phase-shifting transformers is that several converter stages can operate in parallel or in series in order to reduce or partially eliminate the low-frequency input current harmonics.

Thus, these rectifiers are typically known as multi-pulse rectifiers [49]. In fact, 12-, 18- or even 36-pulse multi-pulse configurations can be found in aircraft industry [2,31]. Typically, the 12-pulse configuration depicted in Figure 2.4(a) is preferred because of a simple configuration and a smaller autotransformer compared to other higher multi-pulse configurations. However, a trade-off exists between the increased power quality achieved by a high pulse configuration, its inherent increased winding complexity, heat dissipation and weight [31]. Note that the 6-pulse rectifier, formed uniquely by a diode bridge, is not contemplated for aircraft applications because it creates unacceptable levels of power distortion (THD$_i \approx 30\,\%$) and cannot meet the power quality requirements of aviation standards [31,49].
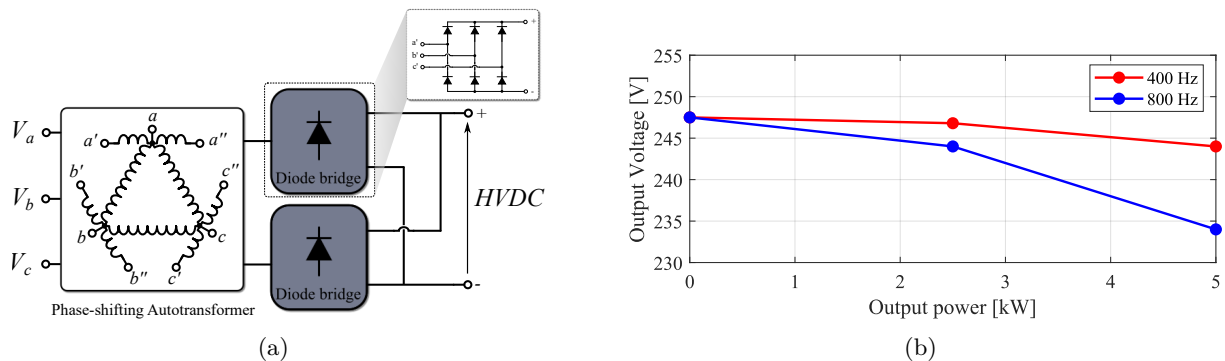
Figure 2.4 (a) Schematic of a 12-pulse multi-pulse configuration rectifier, and (b) an example of its output voltage value depending on the SG frequency and output power (assuming an input L of $500\,\mu$H) [48].

Among the main benefits of ATRUs, the fact that they do not need from control electronics is found. Thus, passive systems are featured by a very low realization effort, high reliability and great robustness. These features are the main reason for employing multi-pulse systems in the existing MEA models to provide the aircraft EPS with DC power [2,6,31,71]. Additionally, the usually employed relatively low input filter inductance values make passive rectifiers exhibit a relatively high PF ($\approx 0.9 - 0.95$) due to the low phase-shift between SG voltage and converter input fundamental voltage waveforms [49].

On the other hand, the lack of control electronics, make the output voltage of the passive rectifiers to be uncontrolled and dependent on their input voltage, i.e. V_{LL} in Figure 2.3. In [48],

an example of the lack of output voltage control is presented (see Figure 2.4(b)). Here, it is described that the output voltage of a 12-pulse rectifier varies depending on the output DC power and the SG frequency, f. Therefore, if the input voltage decays, it is expected for the converter and distribution power losses to rise since, for a certain amount of transferred power, a relatively low output voltage and increased output current will flow.

Furthermore, due to the required filtering passive components, i.e. inductors and capacitors, for output voltage smoothing and mains current shaping, the multi-pulse rectifier tends to be heavy and bulky, resulting in a low power density ($\approx 2 - 4\,\text{kW/kg}$) and high system weight for aircraft applications [7, 71]. As a real design example, [72] presents a 12-pulse ATRU featuring a nominal power of $20\,\text{kW}$, a weight of $14.5\,\text{kg}$ and a $11.7\,\text{l}$ volume. Hence, the power density of this converter referred to weight and volume is $1.38\,\text{kW/kg}$ and $1.8\,\text{kW/l}$ respectively. Similarly, the 12-pulse prototype described in [71] achieves a nominal power of $10\,\text{kW}$ while its weight and volume are reported to be $4.4\,\text{kg}$ and $3.74\,\text{l}$, respectively. Hence, the power density of this prototype is calculated as $2.27\,\text{kW/kg}$ when referred to weight or $2.67\,\text{kW/l}$ when referred to volume.

As a synthesis, the ATRU is penalized by the lack of output voltage control, the expected high low-frequency current harmonics content and the reported power density values which stay far below the $10\,\text{kW/kg}$ and $15\,\text{kW/l}$ targeted by MEA initiatives for year 2025 [7]. Consequently, even if multi-pulse rectifiers are now employed in aircraft EPS, enhanced technologies are needed to avoid weight and harmonic drawbacks demanded in aircraft applications [6, 7, 31, 46]. However, in order to ensure the profitability and suitability of replacing the ATRU, this must be considered as benchmarking technology for comparing with new possibilities.

2.2.2 Hybrid Rectifiers

The combination of active power semiconductors with a passive rectifier results in a hybrid rectifier [6]. Thus, a hybrid rectifier is considered to be a mains-commutated and forced-commutated circuit. A clear benefit of implementing an active circuit is the possibility of reducing the low-frequency filter components by implementing high-frequency active power devices. This fact permits reducing the weight of the converter, and hence, the power density is increased. It is worth to mention that even if a hybrid rectifier, typically, permits a sinusoidal shaping of the mains current and output voltage regulation characteristics, some hybrid rectifier topologies might present limitations to fulfill both characteristics [6].

A simple strategy to form a hybrid rectifier, which maintains the low complexity and high reliability of the passive rectifiers, relies on combining a multi-pulse rectifier and a downstream high switching frequency DC/DC active power stage (see Figure 2.5(a)). Thus, the Multi-pulse with Single-Switch (MSS) hybrid rectifier is formed. With this topology, output voltage control at almost sinusoidal input current shape is provided owing to a low number of active semiconductors added and a relatively simple control [6, 71, 73]. Hence, it might be considered as an interesting approach to upgrade the behavior of the passive multi-pulse topology.

An additional improvement for this topology, which is proposed in [48, 71, 73] and depicted

in Figure 2.5(b), employs a Multi-pulse with Two-Switch Interleaved (MTSI) topology. This way, not only current ripple of the input inductors is reduced, but also the current stress of the power devices in the downstream DC/DC stage. Note that, in this case, the power devices of the DC/DC power stage are doubled and that an additional control effort is required to avoid current unbalances between the interleaved DC/DC converters [48, 73].
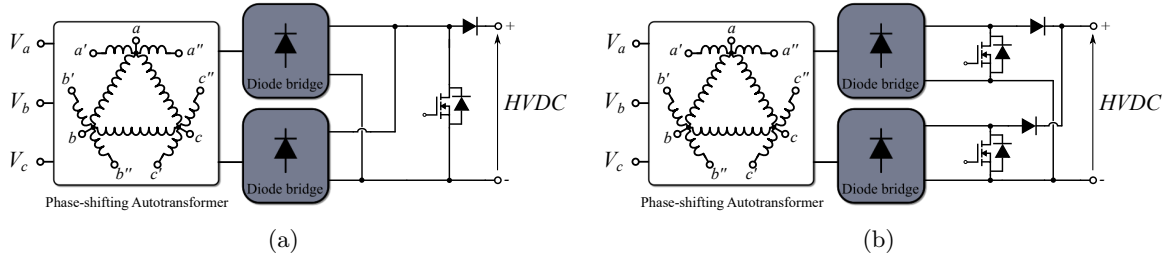
Figure 2.5 Hybrid rectifier systems formed by (a) a multi-pulse configuration and a downstream DC/DC boost stage, and (b) a multi-pulse configuration and downstream interleaved DC/DC boost stage

A different perspective for improving the inherent low power quality of passive systems relies on combining a diode bridge and the third harmonic injection concept [6, 49, 74]. The aim of this concept is to inject current (either by means of a passive or an active circuit) always into the phase which would not carry current in the case of conventional diode bridge rectification [49]. As a result, zero mains current period are avoided and all three phases are shaped achieving a sinusoidal current flow [6, 49]. Figure 2.6 presents some of the hybrid rectifier topologies employing the third harmonic injection concept.

Figure 2.6 Hybrid rectifier topologies employing the third harmonic current injection concept, being (a) Minnesota rectifier, (b) hybrid third harmonic current injection PFC rectifier, (c) Swiss rectifier, and (d) Korea rectifier.

In case a passive network is desired for the third harmonic current injection, the Minnesota rectifier depicted in Figure 2.6(a) can be employed [6, 49, 74]. This rectifier topology presents a controlled output voltage and achieves also sinusoidal shape input currents. To do so, it uses two cascaded boost converters at the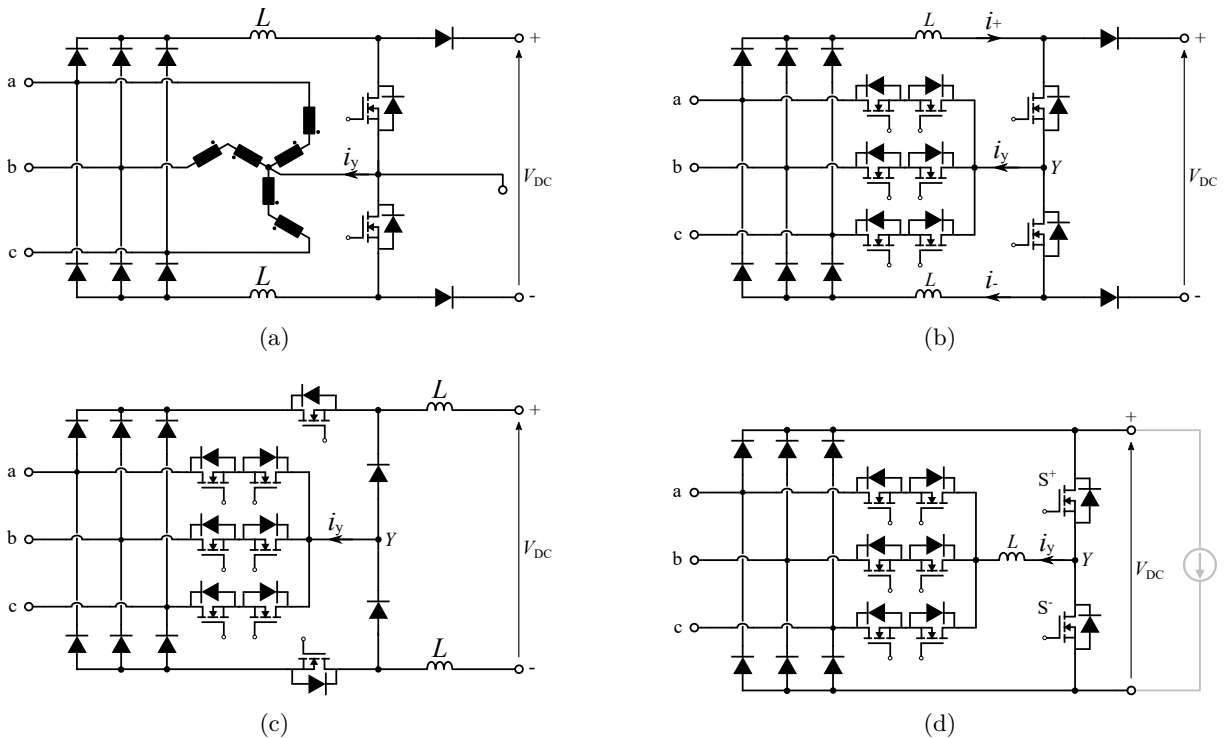 output of the diode bridge and a third harmonic current injection transformer. Thus, the feedback current, i_Y, is injected into the three-phases by means of the transformer. One of the major drawbacks of this topology, as in passive systems, is the bulky, low-frequency transformer which presents a relatively high weight [6, 49, 74]. Since this fact is considered crucial for aircraft applications, active current injection solutions could be preferable.

In this regard, the Hybrid Third Harmonic Current Injection PFC rectifier in Figure 2.6(b) substitutes the transformer of Minnesota rectifier by three bidirectional power transistors, i.e. two semiconductor devices in anti-series per phase, which form the active current injection network [49]. The currents in the positive and negative DC buses (i_+ and i_-) can be controlled independently and the difference, i_Y, is then fed back through the active current injection network. By injecting the latter current into the phase that would not carry current, a sinusoidal current shape can be assured for all main phases.

A similar concept is presented by Swiss rectifier in Figure 2.6(c) [49, 75, 76]. The main difference relies on replacing the cascaded DC/DC boost converters by cascaded DC/DC buck ones. Hence, the three bidirectional switches as active third harmonic current injection are also used in this topology [77]. Swiss topology provides sinusoidal mains input currents although due to its buck-type characteristic nature, low-pass filtering is needed due to the presented discontinuous currents at the converter input. In order to provide sinusoidal currents this converter is limited to pure ohmic mains behavior [49].

Another alternative employing the Hybrid Third Harmonic Current Injection PFC Rectifier is possible if the two inductors of the positive and negative buses are lumped together into a single inductor lying in the current injection path (see Figure 2.6(d)) [6, 49, 78]. In this case the output diodes are eliminated due to the fact that a simultaneous switching on of the S$^+$ and S$^-$ transistors would lead to a short-circuit. This topology presents a relatively low implementation effort, but it does not provide output voltage control [6, 49]. The output voltage is determined by the diode bridge, exhibiting a six-pulse shape. Thus, this topology presents the output voltage limitation previously mentioned and a second power stage would be needed to provide output voltage control. In addition, the topology permits to impress sinusoidal mains phase currents only for constant power loads [6, 49]. Since this topology does not provide the full functionality of a PFC rectifier but provides the function of a passive rectifier with active filter, this topology is called Hybrid Third Harmonic Current Injection Active-Filter Rectifier [49]. It is also known as Korea rectifier [6]. Hence, this topology might result interesting for applications where constant load power is demanded but not for aircraft applications where power demand is variable and even unpredictable.

Apart from the third harmonic injection concept, a possible choice arises from the extension of a single-phase boost rectifier to the three phases. This topology, depicted in Figure 2.7, is known as hybrid half-controlled rectifier [49]. A major drawback of this topology is that due to

the lack of bridge-symmetry (different semiconductors in the positive side and the negative side of the leg) the sinusoidal input currents cannot be impressed within the entire mains period. The functionality of this system, however, is considered to be focused on output voltage regulation [49].
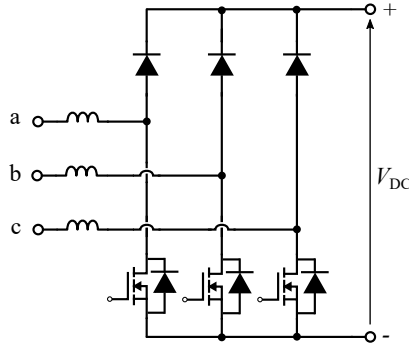

Figure 2.7 Hybrid half-controlled rectifier schema.

2.2.3 Active Rectifiers

The integration of active power semiconductors into the bridge-legs of the passive rectifiers results in active PFC rectifiers. Active systems are featured for containing switching frequency passive components, a forced-commutation characteristic and permitting output voltage regulation [6, 49, 69, 70]. In fact, if high frequency commutation is assumed, a relatively high power quality is ensured by active rectifiers while maintaining low volume filtering components [49]. Therefore, active systems provide reduced input current harmonics and increased power density. However, since passive rectifiers may offer relatively high PF values, it is considered that only a slight improvement in PF is achieved by active systems (PF> 0.99 at the rated operating point is typically targeted). It must be remarked though, that a slight improvement in power factor might be a significantly large difference if a high amount of power is handled (i.e. $> 100\,\text{kW}$) [49].

According to the classification schema in Figure 2.2, active rectifiers can be classified into single-phase and three-phase rectifiers. The single-phase rectifiers, known also as phase-modular rectifiers, provide the opportunity to develop a three-phase rectifier applying phase-modular rectifier knowledge. The individual phase modules can either be connected in star deploying Y-connected rectifier as in Figure 2.8(a), or between the phases displaying Δ-connected rectifier as in Figure 2.8(b). Note that, independently of the configuration, the connection of three individual converters implies to control three different output voltages and to ensure the balance of symmetrical loading of the mains. Moreover, an additional DC/DC stage providing galvanic isolation per module is needed to unify the three individual output voltages and allow the supplying of a single load. Another related issue to these rectifiers compared to three-phase rectifiers is that they need from large capacitors in the individual DC-links of the modular systems due to the pulsating power flow, typical for single-phase rectifiers. Overall, phase-modular rectifiers show good results but, as an additional second DC/DC isolated power stage is needed for each phase, these rectifiers are not the leading technology to achieve highest power density [6].
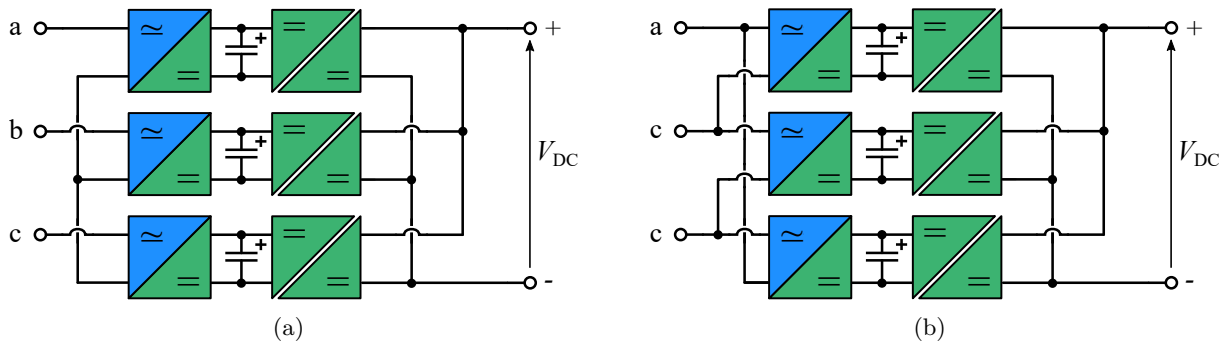
Figure 2.8 Schematic of phase modular rectifier systems. (a) represents a Y-rectifier structure, while, (b) represents a Δ-rectifier structure.

The three-phase rectifier topologies, however, perform a direct energy conversion from the three-phase AC-mains to a single DC-bus [6]. Furthermore, assuming symmetrical three-phase mains, a continuous power flow occurs resulting in a reduced current stress of the rectifiers output capacitor [6]. Depending on the topology output DC voltage, active three-phase rectifiers can be divided into two groups, being the previously explained buck-type and boost-type active rectifiers.

Active buck-type characteristic rectifiers are derived from the diode rectifier circuits with the inductor located in the DC side. By providing the diode bridge with additional turn-off elements (so that bridge and phase symmetry are maintained), the selection of the mains phases connected to the DC side can be achieved [49]. In the case of the active Six-Switch Buck-type PFC rectifier Figure 2.9(a), a power transistor is added in anti-series to each diode of bridge. This extension enables a full voltage-independent controllability of the power transfer. The formed unidirectional bipolar blocking switch, though, makes this topology present discontinuous input currents which by proper modulation and after low-pass filtering result in sinusoidal mains currents [49]. Hence, a relatively high filtering effort must be assumed to meet aircraft application standards [6,69,70]. In addition, bidirectional power flow cannot be achieved unless extending the topology with anti-parallel transistors to the diodes [49].
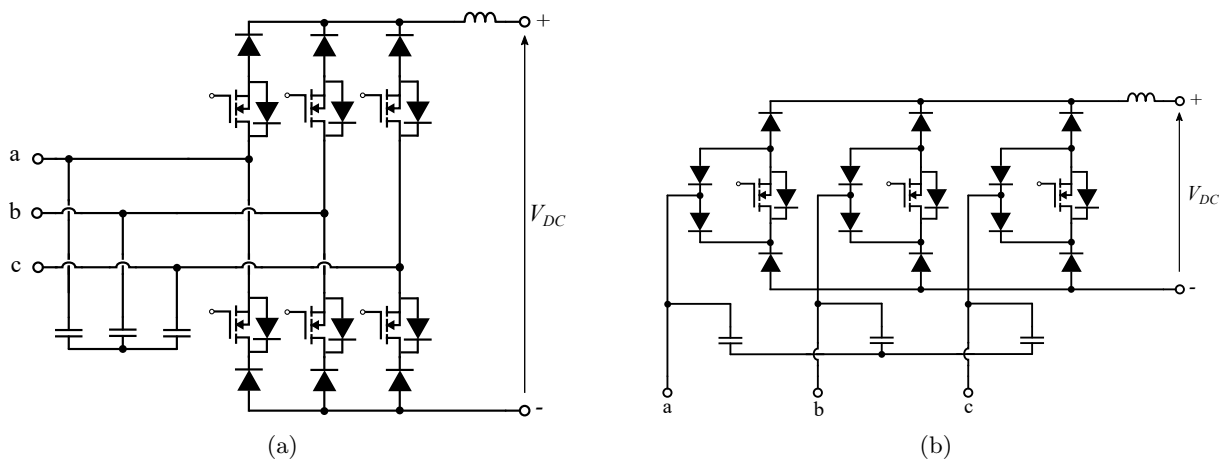

Figure 2.9 Schematics of buck-type characteristic active rectifiers, being (a) the six-switch buck-type rectifier, and (b) the three-switch buck-type rectifier.

The selection of conducting phases is also possible if four-quadrant switches are arranged on the AC side of the bridge rectifier [49]. This alternative results in the Three-Switch Buck-type rectifier topology (see Figure 2.9(b)). Note that even if this topology contains a lower number of transistors, it also contains a higher number of diodes. Therefore, higher conduction losses are expected in this topology compared to six-switch buck- type rectifier [49].

Regarding boost-type active rectifiers, an industrially well-known active PFC rectifier topology is presented in Figure 2.10. Applying bridge symmetry concept to the hybrid half-controlled rectifier, i.e. replacing the three positive bridge half diodes by three transistors, the Six-Switch Active PFC rectifier topology, also known as Two-Level Boost topology is achieved [49]. On the contrary to hybrid half-controlled rectifier, the Two-Level Boost topology allows for voltage regulation and sinusoidal current impression in all sections of mains period. In fact, for a switched-on transistor the current flows either through the transistor or its anti-parallel diode and thus, in each phase, a voltage formation independent of the current is allowed [49]. Therefore, the Two-Level Boost topology allows the impression of sinusoidal phase currents of any phase displacement relative to the mains voltage. Thus, the possibility of anti-phase current impression referred to mains voltage is also provided, i.e. bidirectional power flow capability [6, 49, 69, 70].
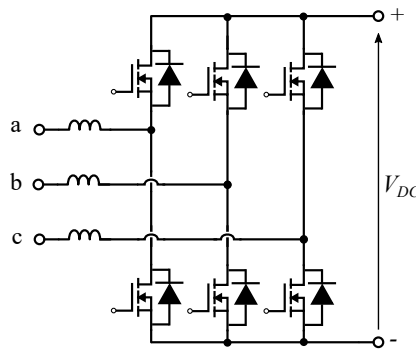
Figure 2.10 Schematic of Two-Level Boost rectifier topology.

Furthermore, the Two-Level Boost topology is considered as a relatively simple topology in terms of structure and control, which, despite functionality, does not need from additional component to provide bidirectional characteristic unlike unidirectional topologies [45, 48, 49, 51]. Moreover, Two-Level Boost rectifier can still operate even if a mains phase failure occurs, which defines this topology as flexible and robust. However, among the main drawbacks, the fact that a shoot-through of a bridge-leg could result in a short circuit of the DC voltage is found [6, 49]. The circuit is, thus, of particular interest since is considered the most common three-phase boost rectifier as it is widely used in industry in applications such as supplying the DC-link of variable speed drives as rectifier and vice versa in case of inverter operation [6, 49].

An interesting approach of boost-type rectifier named Δ-switch rectifier is presented in [6, 49, 74, 79] for MEA applications. This topology, depicted in Figure 2.11(a), presents a hybrid structure due to the four-quadrant switches added in delta-connection to the passive diode bridge. However, it is considered as an active PFC rectifier circuit because, unlike in hybrid rectifier systems, the commutation of the diode bridge occurs at the switching frequency [49]. In fact, since the four-quadrant switches enable the possibility of influencing the conduction state

of the diode bridge, the AC-voltage formation control is permitted by means of Pulse Width Modulation (PWM). As in Two-Level Boost topology, the Δ-switch rectifier can also deal with mains phase failure [49]. In this case, the two bidirectional switches related to the phase that failed have to be disabled. Therefore, a single-phase PFC rectifier circuit will be formed which would still allow the output voltage control and sinusoidal impression of the mains currents. Besides, due to its natural structure no short-circuit of the DC voltage is possible [6].

If the delta-connection of the bidirectional switches is rearranged into a star-connection, the Y-switch rectifier is formed (see Figure 2.11(b)). Thus, this topology maintains the AC-voltage formation and phase displacement characteristics of Δ-switch rectifier. A major drawback of this topology, though, is that presents the connection of two bidirectional switches (four power devices) in series and thus, it tends to present higher conduction losses compared to Δ-switch rectifier [6]. An interesting approach emerges from Y-rectifier topology which relies on connecting the star-point of the Y-switch arrangement to a capacitively midpoint M of the output voltage forming, therefore, a three-level Vienna (multilevel) converter (which is later on presented). Thus, for the relatively high number of power devices that is employed in Δ-switch and Y-switch rectifiers, multilevel active rectifier topologies are considered to be higher potential solutions.
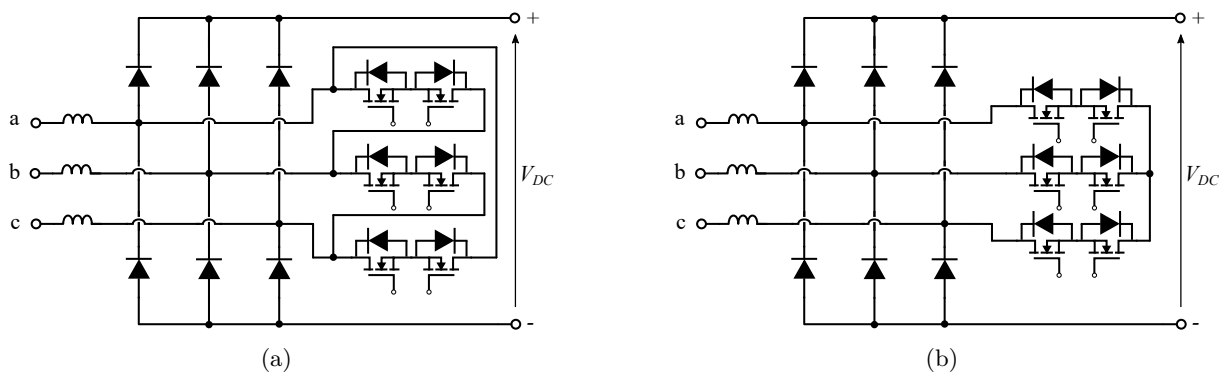
Figure 2.11 Schematic of two-level hybrid structure-based topologies, being (a) Δ-switch rectifier, and (b) Y-switch rectifier.

The fundamental philosophy of a multilevel topology relies on using a higher amount of semiconductor devices linked to lower amplitude DC sources to perform the power conversion while synthesizing a staircase V_{LL} voltage waveform [67,80]. A graphical representation example of this concept is depicted in Figure 2.12 where the generated V_{LL} waveforms of a two-level, three-level and five-level converters are displayed. Note that, the higher the voltage levels, the greater the voltage waveform quality due to the closer form to a sinusoidal wave. Therefore, a reduced filtering effort is expected from multilevel topologies resulting a higher power density input filter compared to the one of the topologies presenting a two-level voltage feature [6, 49, 81, 82].

The fact that the rated voltage of a power device depends mainly on the DC voltage source amplitude it is connected to, results also beneficial to multilevel topologies. The main reason is that, for a considered DC bus voltage level V_{DC}, while the whole bus voltage amplitude is blocked by a power device in a two-level topology, in the case of a three-level topology the blocked voltage level per device is halved, resulting in $V_{\mathrm{DC}}/2$ [6, 49, 80]. Analogously, in the case of a five-level topology, the blocked voltage is again halved to $V_{\mathrm{DC}}/4$.
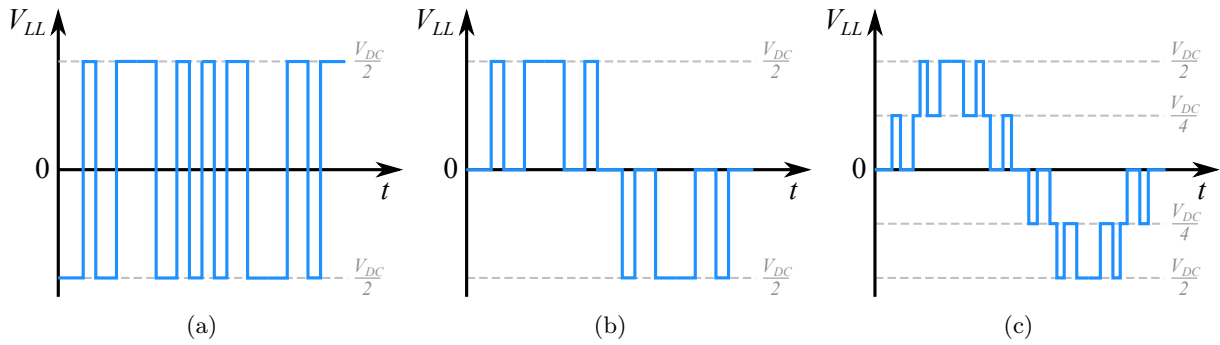
Figure 2.12 Examples of different synthesized line-to-line voltage level characteristics at the converter AC terminals. (a) Two-level, (b) three-level, and (c) five-level voltage characteristic waveforms.

From the contrary perspective, for the same voltage blocking capability of a semiconductor, a higher voltage level can be synthesized by multilevel topologies. Thus, multilevel topologies have typically been employed in Medium Voltage (MV) networks and other applications such as MV gas turbine starters or HVDC transmission [67, 80]. The fact of containing a higher number of power devices, though, results typically in a lower converter reliability and an increased cost and complexity because of the semiconductor related gate-driver circuit required [80, 81]. Nevertheless, as the price of semiconductors diminishes and the power quality standards become more restrictive, the use of multilevel topologies as active rectifiers gets strength in lower voltage rated applications such as aircraft [45, 67].

Traditional multilevel converter topologies are Neutral Point Clamped (NPC) converter, Cascaded H-Bridge (CHB) converter and Flying Capacitor (FC) converter [67]. It is worth to mention that, due to the inherent phase-modular structure of CHB topology, a second DC/DC stage providing galvanic isolation is required for active power transferring and hence, is no longer considered in this research work. Thus, only the schematics of NPC and FC topologies are presented in Figure 2.13.

Figure 2.13 Schematic of (a) Neutral Point Clamped (NPC) multilevel topology, and (b) Flying Capacitor (FC) multilevel topology.

Among the three-level traditional topologies, the NPC topology Figure 2.13(a) is considered as a simple circuit structure which is commonly applied for medium-/high-voltage applications [45, 67]. Although the MEA grid can be considered as a low-voltage application (<1 kV), NPC topology might potentially provide high benefits in terms of power quality. Moreover, this topology can provide bidirectional po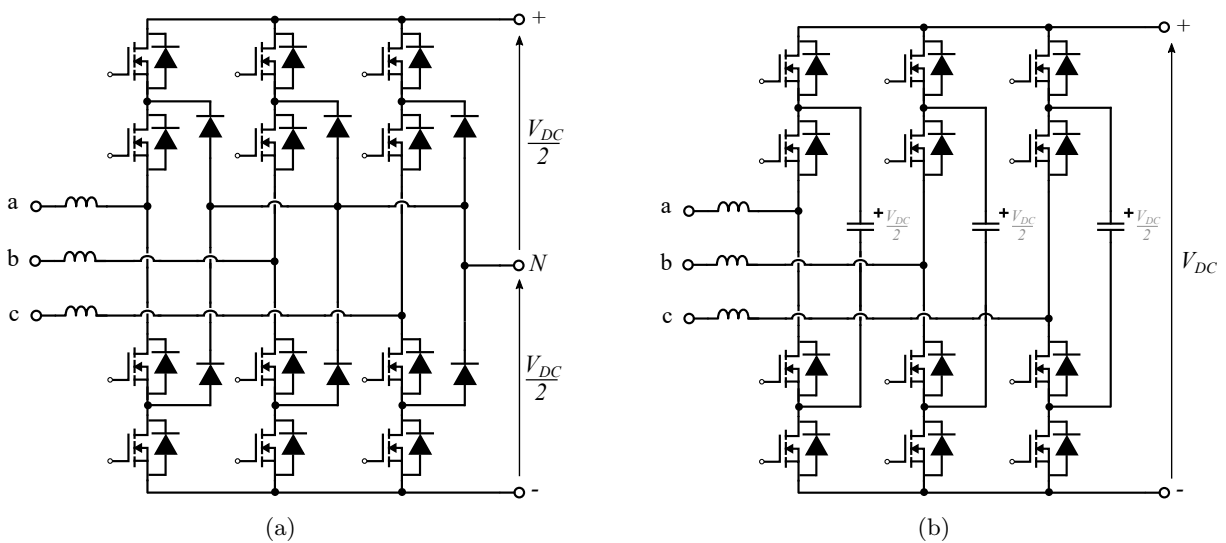wer flow, which is considered as a positive capability for the desired application. Note that this topology has already been tested as inverter operation in Aircraft Electrical Generation System with Active Rectification and Health Monitoring (AEGART) EU project [3, 45, 83].

The three-level FC topology, depicted in Figure 2.13(b), is also considered as a traditional multilevel converter topology with bidirectional power flow capability [67]. It contains a lower number of semiconductors than NPC topology since the clamping diodes of each phase-leg are replaced by a capacitor [67, 80, 84]. Although it is considered to be a simple topology, the main drawbacks of FC are related to the typical large volume of the phase capacitors and the required high switching frequencies in order to keep these capacitors properly balanced. In fact, it is considered as a low industrial penetration topology because of these reasons [67].

In terms of unidirectional three-level topologies, the Vienna rectifier, presented in Figure 2.14(a), is considered to be an industrially well-known topology with a high potential in aircraft applications [6, 48, 49, 69]. This three-level topology maintains AC-voltage and phase displacement characteristics of Δ-switch rectifier although its displacement is significantly reduced to pure ohmic mains behavior when $V_{DC} < 2 \cdot \sqrt{2} \cdot V_{LL}$ [49]. Similarly to Δ-switch rectifier case, Vienna rectifier can still operate when a phase loss occurs maintaining the output voltage control and impressing sinusoidal input currents in the remaining phases [49]. A short-circuit of the DC voltage is also not possible in this topology. Additional functionally equivalent structure configurations are presented in [6, 49] although the one presented in Figure 2.14(a) presents lower conduction losses. Note that, unlike in other three-level topologies, this Vienna configuration stresses the diodes of the bridge to the total DC bus value even if the switched voltage maintains halved.
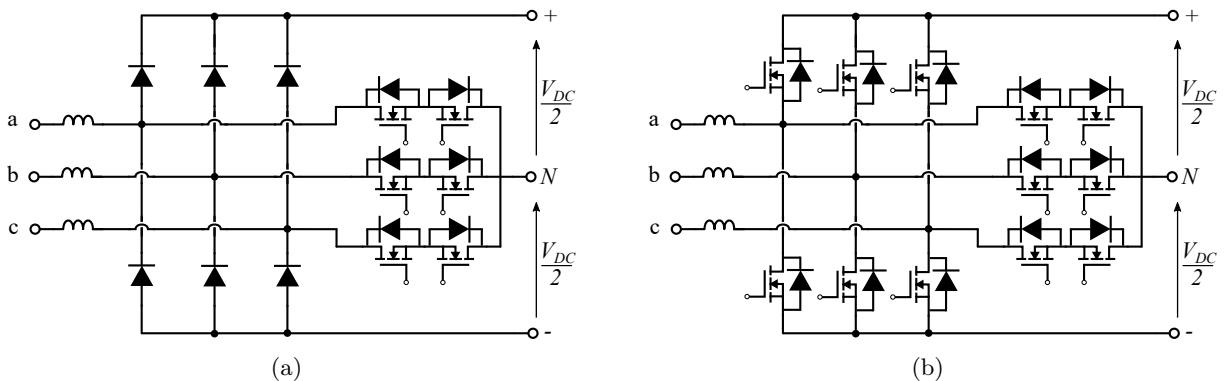

Figure 2.14 Schematics of (a) Vienna rectifier, and (b) T-Type rectifier topologies.

Phase displacement range of Vienna rectifier can be improved by replacing the diodes of the bridge by active turn-off power transistors as presented in Figure 2.14(b). In fact, bidirectional power flow is permitted in this derived topology known as T-Type or Neutral Point Piloted

(NPP) topology [6, 51, 67]. Hence, T-Type topology allows a voltage formation independent of the current but providing a three-level voltage formation.

Apart from these well-known three-level topologies, higher-level topologies could be analyzed in order to reduce the input filter volume owing to a higher number of semiconductors employed and, hence, higher complexity and cost [67, 80]. However, a five-level three-phase rectifier system for aircraft applications is mentioned in [6] which presents no significant benefits for the currently standardized voltage levels of the aircraft. In fact, the higher the voltage levels of the multilevel topology, the higher the number of DC-link capacitors that have to be properly balanced, which might suppose a high implementation effort with high complexity [6, 81, 85]. Therefore, the multilevel converters that present a voltage formation characteristic higher than three-levels are not considered in this work due to their inherent increased complexity, cost, and low benefits obtained for aircraft applications.

2.3 Suitability Analysis of Active Rectifiers in the MEA

2.3.1 Discussion on AC/DC Rectifier Topologies and Preselection

As previously described, the currently employed passive ATRU presents several disadvantages such as the lack of output voltage control or the expected low power density due to the employed bulky passive elements. Therefore, advanced and/or improved technologies are demanded in aircraft applications which avoid the high weight and high harmonic content drawbacks of passive rectifier. In this regard, hybrid rectifiers and active rectifiers are presented as potential solutions to overcome these drawbacks. However, the suitability of hybrid and active rectifier topologies must be compared to the traditional ATRU in order to verify that a technology step-forward can be achieved. The fundamental characteristics of the mentioned passive, hybrid and active rectifiers are summarized in Table 2.2.

Table 2.2 Summary of the characteristics of passive, hybrid and active rectifier topologies.

	Passive	Hybrid	Active
Turn-off devices	No	Yes	Yes
Controlled V_{DC}	No	Yes (may be limited)	Yes
Current shaping	Passive elements	PWM	PWM
Additional inductive elements	Autotransformer	Only Minnesota	No
Expected power density	Low	Low/Medium	High
Preselection	Benchmarking	No	Yes

Hybrid rectifies, present either partially shaped input currents or partially controlled output voltages. The combination of active semiconductors with a passive diode bridge benefits hybrid rectifier topologies so that the input power quality characteristic van be improved with respect to the passive rectifiers. However, the larger number of semiconductors employed, which may lead to a higher amount of power losses compared to passive rectifiers, result penalizing for hybrid topologies.

Few solutions of hybrid systems can be found in literature which match with the predefined ATRU application requirements in Table 2.1. In [73] the "multi-pulse with DC/DC" approaches, i.e. the MSS in Figure 2.5(a) and the MTSI in Figure 2.5(b), were compared in terms of current ripple, total losses and converter efficiency for 10 kW output power. It was concluded that the MTSI resulted preferable over MSS due to the lower input current ripple achieved (approximately 3 times lower), lower total losses and, consequently, a higher efficiency (around a 0.2 %). However, the fact of maintaining the LF magnetic materials and adding a second power stage resulted in a low power density topology. In fact, for the presented 10 kW prototype, a weight of 8.2 kg and a volume of 6.43 l were reported. Therefore, a power density of 1.21 kW/kg and 1.55 kW/l is concluded, which is still far below the expected power density for the future MEA power converters. In relation to the "Third Harmonic Current Injection Concept" topologies, a Swiss rectifier was designed in [77] aiming to verify its compliance with aviation standard requirements. Although a low THD_i value was achieved ($< 5 \%$), the presented model did not fulfill the input/output voltage operating requirements since, for an input voltage of 115 V_{AC}, the targeted output voltage was 150 V. In addition, due to the inherent diode bridge structure of hybrid systems, none of these systems provided bidirectional power flow capability. Since currently no bidirectional power flow is provided by ATRUs, this fact will not be an issue at the current point in time. However, its applicability in future models demanding bidirectional power flow will limit the suitability of these topologies in a medium-/long-term.

On the contrary to hybrid systems, active rectifier systems exhibit a controlled output voltage and sinusoidally shaped input currents and, additionally, they might allow bidirectional power flow operation depending on the converter topology. Besides, as a result of the forced-commuted elements at high switching frequencies, the additional passive bulky elements of passive and hybrid systems can be eliminated. Thus, a higher power density is expected form these systems.

Particularly, active rectifiers are strongly encouraged in recent literature for MEA SG applications. In fact, several active rectifier designs and comparative analysis can be found aiming to identify the most suitable active rectifier topology. However, the active rectifier topologies presented in these analyses do not fulfill with the input/output voltage operating conditions of aviation standards. In [48], multi-pulse, Two-Level Boost rectifier and Vienna rectifier topologies are compared in terms of weight and volume while supplying a 5 kW MEA load. However, even if a 115 V_{AC} input voltage is assumed, the analysis does not consider the required output voltage requirements of the standards, i.e. 270 V_{DC}, for active topologies. While multi-pulse topology presents an uncontrolled output voltage (limited from 250 V_{DC} to 280 V_{DC}), a 350 V_{DC} output voltage is assumed for active rectifiers. The work presented in [51] compares Two-Level Boost and T-Type topologies for a SG application considering an output voltage of $\pm$ 270 V_{DC}. In this case, though, the input voltage does not correspond to the 230 V_{AC} of present-day ATRU operating conditions but to a maximum of 190 V_{AC}. A similar scenario is found in [45] for NPC and Two-Level Boost topologies. Other research works such as [47, 69, 70, 83, 84, 86–90] present different studies about different active rectifiers based power losses analysis, power quality analysis, control schemes, reliability performance, and/or input filter designs in aircraft applications. However, they do not fulfill the currently standardized passive rectification operating requirements or provide all of the emerging requirements, such as bidirectional power flow capability.

In this regard, the suitability of active rectifier topologies, either buck-type or boost-type, must be demonstrated. Moreover, due to the wide gamut of active topologies designed and compared for aircraft applications in literature, it can be concluded that there is no straightforward topology choice. Specially because the proposed benchmarking analysis with ATRU up-to-now do not share the same input/output operating conditions for ATRU and active topologies. Thus, considering the application requirements and the $115\,\text{V}_\text{AC}$ to $270\,\text{V}_\text{DC}$ operating scenario, a discussion and preselection of the potential buck-type and boost-type topologies for the benchmarking analysis is presented in the following.

On the one hand, among the major drawbacks of buck-type rectifier topologies the presented discontinuous input currents is found [6, 49, 69, 70]. Thus, a relatively high harmonic distortion is expected, and a large filtering effort must be assumed to achieve a high input power quality operating condition. Compared to the Six-Switch Buck rectifier, the Three-Switch Buck rectifier topology presents the half of active semiconductors. However, regardless the number of active power transistors, a simple control is expected in both topologies. In this case, the full controllability by Six-Switch Buck rectifier makes this topology preferable between the buck-type topologies. Moreover, although the natural power flow of both topologies is unidirectional (with reactive power compensation possibility), the metamorphosis of the Six-Switch Buck converter into bidirectional is as simple as adding anti-parallel transistors to the anti-series diodes (forming a matrix converter).

On the other hand, the fact of requiring a downstream converter results disadvantageous for buck-type rectifiers compared to the boost-type ones. Due to the fact of needing to boost the output voltage from $244\,\text{V}_\text{DC}$ (or lower) to the targeted $270\,\text{V}_\text{DC}$, a higher amount of power losses produced by the second DC/DC stage is expected because of the inherent higher DC current. Thus, all these considerations, summarized in Table 2.3, make buck-type converters seem not suitable for the desired application in MEA.

Table 2.3 Summary of the characteristics related to the active PFC buck-type topologies.

	Six-Switch Buck	Three-Switch Buck
N° of power devices	12	15
Control	Simple	Simple
Expected THD$_\text{i}$	High	High
Power flow	Unidirectional	Unidirectional
Preselection	No	No

Regarding boost-type active rectifiers, whose features are summarized in Table 2.4, a relatively high potential is predicted for Two-Level Boost topology. Its simplicity, maturity and low number of semiconductor devices make this topology promising for MEA applications [6, 45, 47–49, 51, 69, 70, 84]. Moreover, considering future MEA trends, the bidirectional power flow capability of Two-Level Boost rectifier could provide main engine start or even allow hybrid- or all-electric propulsion. Δ-switch and Y-switch rectifiers provide high reliability although lower efficiency is expected due to the higher number of semiconductors [6, 49, 74]. Moreover, their inherent input diode bridge limits these two topologies to provide uniquely unidirectional power

flow. Consequently, Δ-switch and Y-switch rectifiers are ruled out from the gamut. Furthermore, their higher number of semiconductors with respect to the Two-Level Boost topology could present higher benefits if a mature and proven multilevel topology is assumed [6, 67, 80].

Table 2.4 Summary of the characteristics related to the active PFC boost-type topologies.

	Two-Level	**Δ-Switch**	**Y-Switch**	**Vienna**	**T-Type**	**NPC**	**FC**
Nº of power devices	6	12	12	12	12	18	12
AC-Voltage Levels	2	2	2	3	3	3	3
Control	Simple	Medium	Medium	Complex	Complex	Complex	Simple
Expected THD$_i$	Low	Low	Low	Very low	Very low	Very low	Very low
Power flow	Bidirec.	Unidirec.	Unidirec.	Unidirec.	Bidirec.	Bidirec.	Bidirec.
Preselection	Yes	No	No	No	Yes	Yes	No

Among three-level topologies, the Vienna rectifier is considered to be a topology with high potential in aircraft applications [6,48,49,69]. However, the reduced reactive power compensation and the unidirectional power flow limitation of Vienna rectifier make this topology not suitable for the defined application. Conversely, these limitations can be avoided if the input diodes are replaced by forced commuted semiconductors. The resulting T-Type topology, which provides bidirectional power flow capability, is then considered as a potential topology in this research work [6,47,51,67].

Similarly to the Two-Level Boost topology, the simple circuit structure of NPC topology, its maturity, and the provided bidirectional power flow capability make this topology a promising solution, as already demonstrated, for MEA applications [45, 47, 67, 83, 84]. Due to its three-level characteristic and higher number of power devices, though, this topology presents a higher complexity control and implementation compared to two-level topologies.

The FC topology contains a lower number of semiconductors than NPC topology because the clamping diodes of each phase-leg are replaced by a capacitor [67, 80, 84]. Nevertheless, the larger number of capacitors results in an expected more expensive and bulky structure than the one of NPC topology [80]. Thus, even if the simpler control of FC topology is expected compared to the other three-level topologies, the lowest power density can also be expected. Therefore, FC topology is not further contemplated in this work.

To sum up, Two-Level Boost, NPC and T-Type topologies are the potential solutions preselected to verify the suitability of active rectifiers in aircraft SG applications and perform a benchmarking analysis with the conventionally employed passive ATRU. At this point, it is worth to mention that even if high potential is expected for these active topologies in MEA applications, the up-to-date performed studies do not consider both the rectifier input and output requirements of aviation standards. Therefore, in order to provide a fair benchmarking analysis in terms of equal operating conditions, the suitability of active rectifier operating at the input/output voltage operating scenario of aviation standards, i.e. $115\,V_{AC}$ to $270\,V_{DC}$, must be analyzed first.

2.3.2 Suitability Analysis of Active Boost-Type Rectifiers and Operating Limitations

The schematic of the boost-type AC/DC converter in Figure 2.15(a) can be represented by means of the simplified single-phase circuit in Figure 2.15(b). Assuming that only the fundamental harmonics of voltage and current in the single-phase circuit are considered and that the cable resistance is neglected, the typical operating possibilities of an AC/DC converter are depicted in the phase diagrams of Figure 2.15(c), 2.15(d) and 2.15(e). These figures represent the general rectifier phasor diagram, the rectifier phasor diagram operating at unity PF and the inverter phasor diagram operating at unity PF, respectively [91].
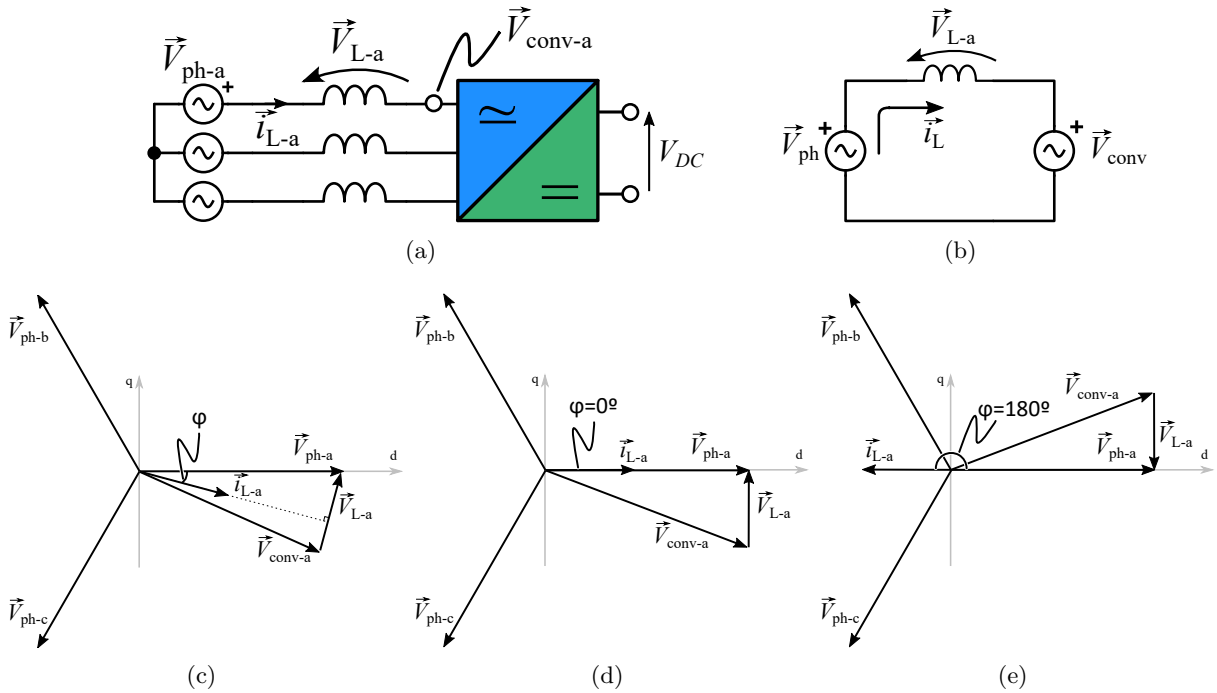
Figure 2.15 (a) Representation of a boost-type power converter converter connected to the SG-grid and (b) its simplified phase circuit considering the fundamental voltage harmonic waveform. Three simplified phasor diagrams are presented being (c) the general phasor diagram, (d) rectifier operation at unity PF, and (e) inverter operation at (minus) unity PF.

On the one hand, these phase diagrams are typically described and analyzed by the following mathematical equation:

$$V_{\text{conv}}^2 = (V_{\text{ph}} - V_{\text{L}} \cdot \sin(\varphi))^2 + (V_{\text{L}} \cdot \cos(\varphi))^2 \tag{2.1}$$

where V_{ph} represents the SG phase RMS voltage in in Table 2.1, $\cos(\varphi)$ refers to the converter operating PF, and V_{L} symbolizes the inductor RMS voltage. Note that, as previously explained, in order to achieve the maximum system efficiency PF = 1 is targeted to avoid reactive power handling. In this case, (2.1) is simplified as follows,

$$V_{\text{conv}} = \sqrt{V_{\text{ph}}^2 + V_{\text{L}}^2} \tag{2.2}$$

Therefore, it can be concluded that when unity PF operation is targeted, $V_{\text{conv}} > V_{\text{ph}}$. Thus, considering that $V_{\text{ph}} = 115\,\text{V}_{\text{AC}}$ and according to (2.2) and the presented limits in Figure 2.3(b), $V_{\text{conv}} > 115\,\text{V}_{\text{AC}}$ and, hence, $V_{\text{DC}} > \sqrt{6} \cdot V_{\text{conv}} = \sqrt{6} \cdot 115\,\text{V}_{\text{AC}} = 282\,\text{V}_{\text{DC}}$. This fact reveals the main reason of the employed input/output voltage levels in the previously presented literature designs which do not fulfill the standard operating requirements ($115\,\text{V}_{\text{AC}}$ input voltage and $270\,\text{V}_{\text{DC}}$ output voltage). Consequently, adding a DC/DC stage is proposed in this research work forming a *two-stage configuration* as a potential solution to fulfill both input/output operating requirements of aviation standards. This way, the output V_{DC} of the active rectifier is then adapted by means of a buck converter to $270\,\text{V}_{\text{DC}}$. This concept is presented in Figure 2.16 where the targeted $270\,\text{V}$ are achieved at the DC/DC output voltage, V'_{DC}.
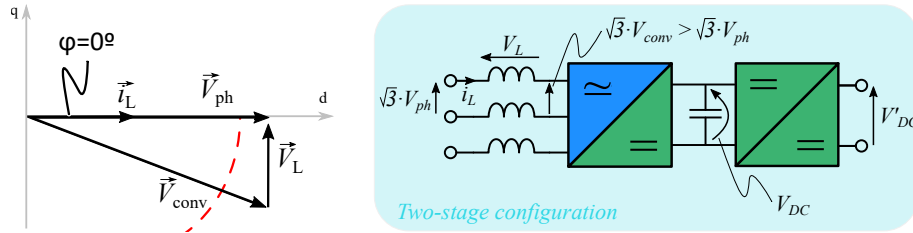

Figure 2.16 Phasor diagram and two-stage converter configuration when operating at unity PF.

On the other hand, a different solution is proposed in this work which relies on worsening the operating PF (PF < 1) of the AC/DC converter so that a *single-stage configuration* rectifier is achieved. This perspective is based on the Modulation Index, m, of active boost rectifiers defined in (2.3) [91]. If this equation is rearranged as in (2.4), the synthesized V_{conv} value for a defined V_{DC} and m is deduced.

$$m = \frac{\sqrt{2} \cdot V_{\text{conv}}}{\dfrac{V_{\text{DC}}}{2}} \qquad (2.3)$$

$$V_{\text{conv}} = \frac{m \cdot V_{\text{DC}}}{2\sqrt{2}} \quad . \qquad (2.4)$$

Thus, according to (2.4), the standardized DC bus voltage of $270\,\text{V}$, and considering that a maximum linear value of $m = 1.15$ can be implemented, a single-stage configuration rectifier could be achieved only if $V_{\text{conv}} < 110\,\text{V}_{\text{AC}}$. This value is represented by means of a red dashed line in Figure 2.16 in order to express this mathematical limitation graphically. Thus, this fact supposes that, if unity PF is targeted and the implementation of a single-stage configuration is aimed, V_{ph} must be lower than $110\,\text{V}_{\text{AC}}$, which does not correspond to the nominal $115\,\text{V}_{\text{AC}}$ voltage of aviation standards.

Based on the general phasor diagram, though, an alternative solution for achieving a single-stage rectifier not presented in previous literature is proposed in this work. The proposed solution is based on (2.1) and relies on reducing the operating PF to a value lower than unity so that $V_{\text{conv}} < 110\,\text{V}_{\text{AC}}$ is achieved. This concept is graphically represented in Figure 2.17 where it can be observed that V_{conv} vector matches with the $110\,\text{V}_{\text{AC}}$ red dashed line limit. Thus, considering the worst PF operating condition case in Table 2.1, in which the active rectifier performs at PF = 0.85 lagging, it is assumed that $V_{\text{conv}} \leq 110\,\text{V}_{\text{AC}}$ condition is fulfilled, and

therefore, no additional converter is required downstream for achieving the targeted $270\,\mathrm{V_{DC}}$. Note that, even if a higher PF could be assumed, the worst allowed operating PF is selected in order to squeeze the operating limits of aviation standards for active rectifiers and evaluate their potential in aircraft applications, i.e. PF = 1 against PF = 0.85. The possibility of increasing the PF of single-stage rectifiers is treated in higher detail and solved in Chapter 3.
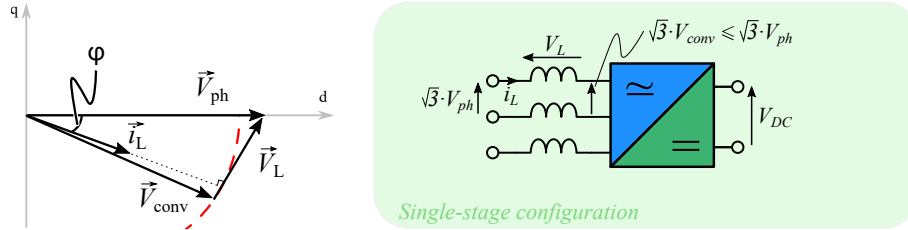

Figure 2.17 Phasor diagram and single-stage converter configuration when operating at a PF lower than unity.

Although the two-stage concept in Figure 2.16 results in a relatively simple configuration, the overall converter efficiency is decreased by the additional second power stage. Moreover, a larger number of passive elements and semiconductors is needed and, therefore, the reliability of the converter might be reduced. These issues are avoided with the solution presented in Figure 2.17. However, the suitability of this concept must be weighed against the fact of operating at a relatively low PF such as the 0.85 lagging limit allowed in Table 2.1. In fact, the implicit increased phase current results in higher losses of the AC/DC power stage and, hence, a decreased efficiency. Furthermore, operating at a PF lower than unity means that the aircraft AC grid is polluted with reactive power and, hence, reactive power compensation might be required. From the SG side perspective, the demanded reactive power can be corrected by means of an additional input capacitor bank at the converter input. The increased converter volume, however, should be compared to the additional DC/DC stage of the two-stage configuration concept. In this context, a comparison among the potential active PFC topologies is required which, in addition, evaluates the suitability of both concepts presented in Figure 2.16 and Figure 2.17.

2.4   Comparison Framework for the Topology Assessment

In relation to the topology comparison, efficiency, power density, reliability, weight and volume are the most crucial characteristics to be evaluated in the aviation context. These features are partly related to the topology, the employed semiconductor and the operating switching frequency, f_{sw}. Therefore, based on these parameters, a quantitative analysis of the preselected Two-Level Boost, NPC and T-Type topologies is pretended which, additionally, evaluates each topology assuming the proposed two-stage configuration (operating at PF = 1) and single-stage configuration (operating at PF = 0.85) conceptual scenarios. This way, a comparative analysis can be performed among active topologies and the ATRU to evaluate the most suitable topology for the defined MEA application.

Following the proposed topology comparison methodology in [92], the essence of the analysis procedure performed in this work is based on the following inputs:

- A simplified simulation model of the converter under study and its associated modulation pattern.

- The operating conditions of the simulation model defined by the application requirements in Table 2.1 and the proposed rectification scenarios, i.e. PF = 1 and PF = 0.85.

- The electrical and thermal characteristics of the employed semiconductor.

Regarding the outputs, considering the application requirements and the MEA efficiency and power density future targets, in this topology comparison the following output parameters are evaluated due to their close relation to efficiency, power density, reliability, weight and volume:

- Topology efficiency, $\eta\left(f_{\mathrm{sw}}\right)$.
- Voltage Total Harmonic Distortion, $\mathrm{THD_v}\left(f_{\mathrm{sw}}\right)$.
- Voltage Weighted Total Harmonic Distortion, $\mathrm{WTHD_v}\left(f_{\mathrm{sw}}\right)$.
- Temperature increase from case-to-junction, $\Delta T_{\mathrm{j-c}}\left(f_{\mathrm{sw}}\right)$.
- The maximum achievable switching frequency, $f_{\mathrm{sw,max}}$.

Simply put, the comparison procedure is summarized as follows: *(1)* by means of the defined inputs, and an interactive simulation process is performed which extracts the current and voltage waveforms of the simulated topology for the defined application requirements, i.e. V_{DC}, PF, f_{sw}, etc.; *(2)* then, in a second analysis step and for comparative purpose, the evaluation outputs are defined as a function of the f_{sw}, which is the common parameter in all of outputs [92].

Note that, the employed f_{sw} directly affects in the semiconductor power loss performance which, indeed, is also related to the topology η, $\Delta T_{\mathrm{j-c}}$ and, hence, achievable $f_{\mathrm{sw,max}}$. It must be remarked that, as specified in Table 2.1, the efficiency should be higher than 97 % in order to ensure that the aircraft future targets are fulfilled.

Similarly, the higher the f_{sw}, the higher the input power quality and, thus, a direct relation to the harmonic pollution is concluded. Particularly, the input power quality results, which pretend to measure the required filtering effort, are evaluated by the terminals voltage waveform $\mathrm{THD_v}$ and $\mathrm{WTHD_v}$. The former index gives a simple perception about the waveform harmonic pollution and hence, it can be used to compare the filtering requirement. The latter index gives an improved perception of the waveform harmonic pollution by using the order of each harmonic content as its weight factor. Thus, the lower the $\mathrm{WTHD_v}$ the lower the LF harmonics to be filtered and, hence, the lower filter volume expected.

The number of power devices and the $\Delta T_{\mathrm{j-c}}$, on their behalf, not only provide a first approach about the cooling requirement, but they are also related to the reliability of the devices due to the influence of temperature effects on the expected lifetime and wear-out performance [93, 94]. Other deep evaluations such as costs related analysis are not quantitatively considered in this comparison.

It is worth to mention that, since a high power density converter is pursed, a high f_{sw} is desired to reduce the volume of the passive elements and, thus, the volume of the input filter. In this regard, the implementation of WBG semiconductor technology in MEA applications becomes a research interest. SiC and GaN are the most promising technologies currently. Among

the benefits provided by WBG devices over the traditional Si devices, a lower on resistance than the Si Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) and a faster switching capability than the Si Insulated Gate Bipolar Transistor (IGBT) can be found [18,52–58]. Hence, not only lower conduction and switching losses are expected from WBG devices, but also a higher efficiency, lower cooling effort, reduced volume for passive elements and a higher power density from WBG-based converters. Therefore, not only the topology but also the semiconductor selection becomes an important task in this assessment. Thus, a topology-semiconductor pair analysis must be performed to evaluate the potential of the different semiconductor technologies in each preselected topology.

2.4.1 Semiconductor Device Selection and Characterization

Due to the operating input/output voltages of the defined application, i.e. $115\,V_{AC}$ to $270\,V_{DC}$, $650\,V$ blocking voltage Si MOSFET, Hybrid IGBT and SiC MOSFET semiconductors are considered in the topology-semiconductor pair evaluation. Note that power devices with a lower blocking voltage could have been considered in the case of Si MOSFET and Hybrid IGBT but no lower blocking voltage rating SiC semiconductors are found in the market. Thus, the same blocking voltage rating is selected for all technologies to provide a fair comparison. GaN devices have not been included in the analysis due to the fact that they presents a lower current rating than SiC technology. It is worth to mention that a $37.5\,kW$ converter power rating ($108\,A$ phase-RMS) is considered as an initial approach due to the "*four converter path*" modularization assumed for the $150\,kW$ power of the SG.

The selected semiconductors, presented in Table 2.5, are *IXFK120N65X2* Si MOSFET [95], *IGW75N65H5* Si IGBT [96] and *GC50MPS06-247* Schottky SiC Diode [97] as Hybrid IGBT and *SCTW90N65G2V* SiC MOSFET [98]. Note that even if the voltage and current rating of the selected devices result similar in magnitude, other electrical and thermal characteristics might be very different depending on the semiconductor technology. On the one hand, the electrical characteristics, being mainly semiconductor conduction and switching characteristics, define the power losses of the semiconductor device for specified converter operating conditions. On the other hand, considering the semiconductor power losses, the semiconductor Junction-to-Case Thermal Resistance, $R_{th,j-c}$, and the Maximum Junction Temperature, $T_{j,max}$, are the features that limit the semiconductor power handling capability.

Table 2.5 Selected semiconductor models and relevant characteristics.

Semiconductor Model	Rated Voltage	Rated Current ($T_C = 25\,°C$)	Rated Current ($T_C = 100\,°C$)	$T_{j,max}$	$R_{th,j-c}$
SiC Diode *GC50MPS06-247*	$650\,V$	$143\,A$	$96\,A$	$175°\,C$	$0.33\,°C/W$
Si IGBT *IGW75N65H5*	$650\,V$	$120\,A$	$75\,A$	$175\,°C$	$0.38\,°C/W$
Si MOSFET *IXFK120N65X2*	$650\,V$	$120\,A$	$85\,A$	$150\,°C$	$0.1\,°C/W$
SiC MOSFET *SCTW90N65G2V*	$650\,V$	$119\,A$	$90\,A$	$200\,°C$	$0.31\,°C/W$

At this point, it must be mentioned that, for the selected power devices, the efficiency of

the selected AC/DC topologies does not reach the minimum efficiency target ($> 97\%$) when operating at $37.5\,\text{kW}$ and high switching frequencies unless power device parallelization is assumed. Thus, in order to avoid the parallelization of power devices and its respective issues with unbalanced currents, the number of converter modules is doubled from four to eight. Thus, as a second approach of the modular converter architecture design and for comparative purposes, a nominal converter power of $18.75\,\text{kW}$ is defined. With power devices selected, their electrical characterization becomes necessary since it is considered as one of the inputs for the previously mentioned simulation models. Thus, the conduction and switching characterization of each semiconductor, depicted in Figure 2.18, is done based on its corresponding datasheet. Note that in order to establish a safe margin in terms of heat dissipation and avoid the converter burnout, the worst-case junction temperature figures are harnessed [99].
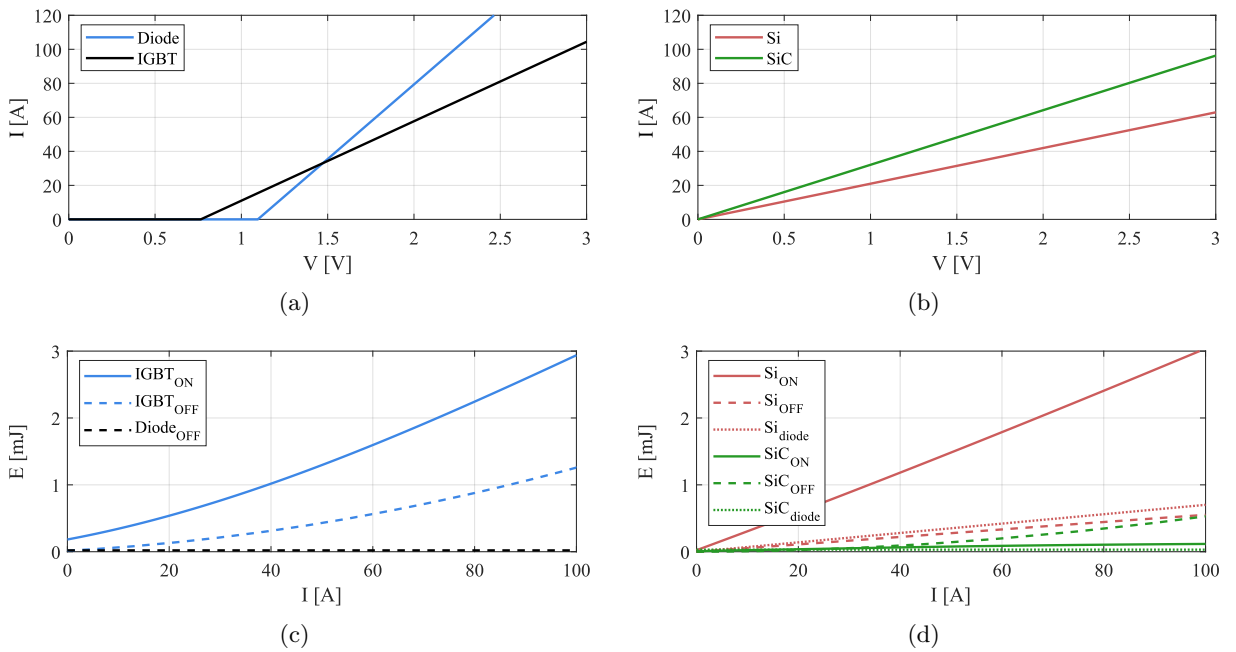

Figure 2.18 Electrical characterization of the selected semiconductors, being (a) the V-I output characteristic of the Hybrid IGBT, (b) the V-I output characteristic of the MOSFET devices, (c) the switching energy characteristic of the Hybrid IGBT and (d) the switching energy characteristic of MOSFET devices.

The conduction characteristic of a power device is defined by its V-I output datasheet characteristic. However, due to the complex non-linear shape of these figures, a linear simplification has been assumed in order to easily calculate the device voltage drop with respect to its conducting current as explained in the following.

- **Diode and IGBT:** In the case of the SiC Schottky Diode and the IGBT, depicted in Figure 2.18(a) the conduction output characteristic of the datasheet is modeled a voltage source in series with a resistor. Thus, the simplified output characteristic of these two devices is defined as,

$$V_{\text{SD}}(i) = V_{0,\text{Diode}} + R_{\text{on,Diode}} \cdot i \ , \ \ V_{\text{CE}}(i) = V_{0,\text{IGBT}} + R_{\text{on,IGBT}} \cdot i \tag{2.5}$$

where V_{SD} and V_{CE} refer to the voltage drop of the devices while conducting current

(from anode to cathode in the case of the diode and from collector to emitter in the case of the IGBT), V_0 represents the threshold voltage of the semiconductor, i refers to the instantaneous current flowing through the device, and R_{on} represents the internal conduction resistance.

- **MOSFET:** In the case of MOSFET devices, either Si or SiC, the conduction output characteristic is simplified as a resistor (see Figure 2.18(b)). Hence,

$$V_{DS}(i) = R_{DS} \cdot i \tag{2.6}$$

where V_{DS} refers to the voltage drop of the device from drain to source and R_{DS} represents the internal conduction resistor. Note that, since MOSFET are bidirectional devices, it has been assumed that the current (either positive or negative) flows through the MOSFET channel and, hence, no diode conduction losses are assumed when a MOSFET is employed.

With the conduction characteristic of the power devices defined, the instantaneous conduction losses are calculated as,

$$P_{cond}(i) = V_{dev}(i) \cdot i \tag{2.7}$$

where (2.5) or (2.6) are introduced in V_{dev} depending on the semiconductor device. Consequently, the average conduction losses, P_{cond}, are calculated as the mean value of the instantaneous conduction losses, $P_{cond}(i)$, throughout the mains period.

Regarding the switching characteristics, the characterization of the dissipated energy with respect to the switched current is required. Again, depending on the semiconductor device and the information of the datasheets, different characterization approaches have been performed. The results of the characterized switching energy curves are depicted in Figure 2.18(c) and 2.18(d).

- **IGBT and SiC MOSFET:** The datasheets of these devices already display the on and off switching energy curves. However, these curves have to be scaled to the blocking voltage level under study. In order to model the on and off switching energy curves, E_{on} and E_{off}, respectively, a third order function is employed [92] Thus,

$$E(i) = (k_1 \cdot i^3 + k_2 \cdot i^2 + k3 \cdot i + k_4) \cdot \frac{V_{DC}}{V_{DD}} \tag{2.8}$$

where k_1, k_2, k_3 and k_4 are scaling factors, V_{DD} refers to the blocking voltage assumed in the datasheet and, V_{DC} the defined bus voltage.

- **Diode:** Typically, the switching on energy is considered as negligible for a diode and, hence, so it is considered in this work for the SiC schottky diode and the MOSFET body diode. Hence, $E_{D,on} = 0$ is assumed. The switching off energy, $E_{D,off}$, though, is related to the reverse recovery charge of the diode, Q_{rr}, and the blocking voltage of the semiconductor which, in this case, is V_{DC}.

$$E_{D,off} = \frac{1}{4} \cdot Q_{rr} \cdot V_{DC} \ . \tag{2.9}$$

- **Si MOSFET:** Unlike with the other transistors, the datasheet of the Si MOSFET does

not provide the switching energy curves and, therefore, these have to be estimated [100]. In order to simplify the switching energy curves modeling, it has been assumed that the selected Si MOSFET is featured as a fast switching and low power device. Accordingly, the switching energy curves are related to the switching process of a MOSFET device. Figure 2.19 presents the typical circuit employed for MOSFET switching loss estimation, and the switching on and off transient-related curves of the power device.

When the device turns on, the estimated energy loss is related to the dissipated power during the current rise time and the voltage fall time (see Figure 2.19(b)). These time values are, indeed, related to the gate charge and gate current and hence, calculated as,

$$t_{\mathrm{ri}} = \frac{Q_{\mathrm{GS}}}{I_{\mathrm{avg,GS}}} = \frac{Q_{\mathrm{GS}} \cdot R_{\mathrm{G}}}{V_{\mathrm{DR}} - \dfrac{V_{\mathrm{plateau}}}{2}} \tag{2.10}$$

$$t_{\mathrm{fv}} = \frac{Q_{\mathrm{GD}}}{I_{\mathrm{avg,GD}}} = \frac{Q_{\mathrm{GD}} \cdot R_{\mathrm{G}}}{V_{\mathrm{DR}} - \dfrac{V_{\mathrm{plateau}}}{2}} \tag{2.11}$$

where t_{ri} is the current rise time, t_{fv} is the drain to source voltage fall time, R_{G} corresponds to the gate resistor and V_{DR} to the applied driver voltage. V_{plateau}, represents the plateau voltage and, Q_{GS} and Q_{GD}, the gate-to-source charge and the gate-to-drain charge, respectively, which depend on the switching current value.
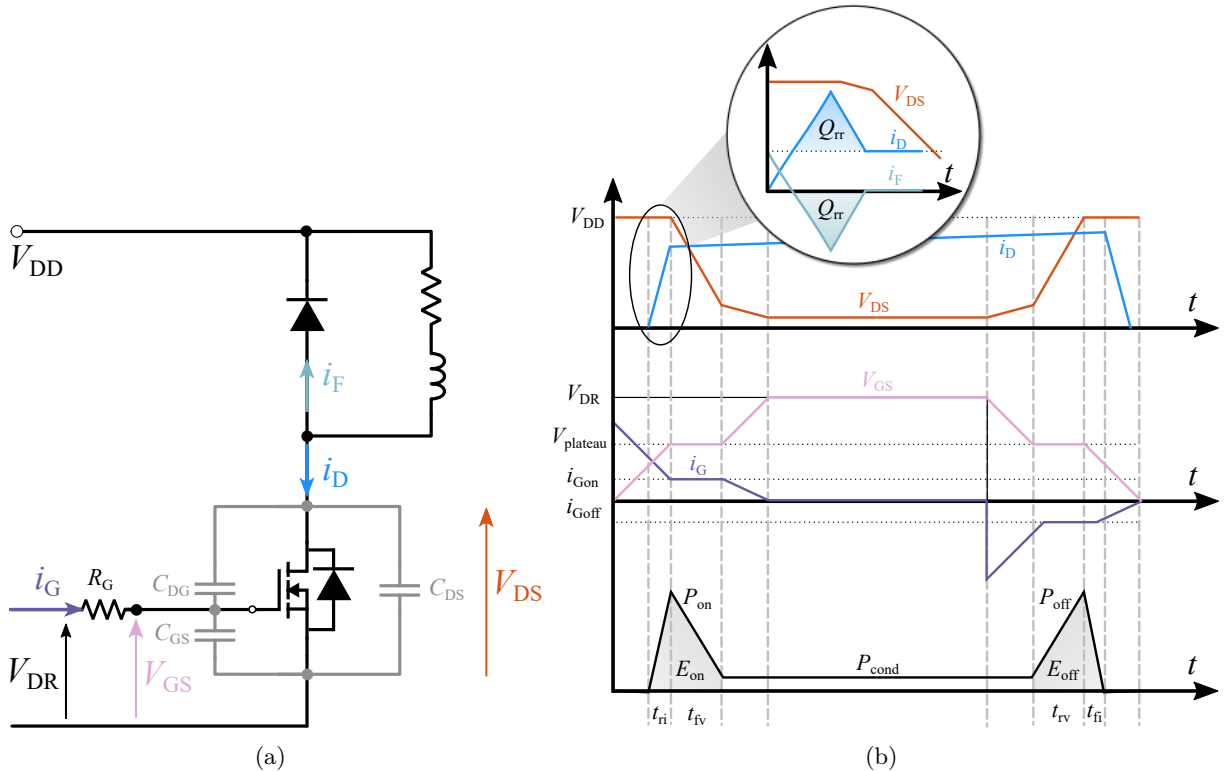

Figure 2.19 (a) MOSFET characterization circuit with an inductive load, and (b) switching transients of the power MOSFET.

In addition, assuming that a quarter of the body diode reverse recovery energy is dissipated during the turn-off process of the Si body diode as in (2.9) [100], the other three-quarter

parts are considered are assumed to be dissipated by the MOSFET when it turns on. Thus, the switching on energy loss value of the Si MOSFET is calculated as in (2.12),

$$E_{\mathrm{on,Si}} = \frac{1}{2} \cdot i \cdot V_{\mathrm{DD}} \cdot (t_{\mathrm{ri}} + t_{\mathrm{fv}}) + \frac{3}{4} \cdot Q_{\mathrm{rr}} \cdot V_{\mathrm{DD}} \ . \tag{2.12}$$

Conversely, when the device turns off,

$$t_{\mathrm{rv}} = \frac{Q_{\mathrm{GD}}}{I_{\mathrm{avg,GD}}} = \frac{Q_{\mathrm{GD}} \cdot R_{\mathrm{G}}}{V_{\mathrm{plateau}}} \tag{2.13}$$

$$t_{\mathrm{fi}} = \frac{Q_{\mathrm{GS}}}{I_{\mathrm{avg,GS}}} = \frac{Q_{\mathrm{GS}} \cdot R_{\mathrm{G}}}{\dfrac{V_{\mathrm{plateau}}}{2}} \ . \tag{2.14}$$

It is worth to mention that, since the instantaneous switching losses are also calculated by simulation method (either for E_{on} and E_{off} of every semiconductor technology), the instantaneous power switching losses, $P_{\mathrm{sw}}(i)$, are calculated using the simulation sample time, t_{sample}, as,

$$P_{\mathrm{sw}}(i) = \frac{E}{t_{\mathrm{sample}}} \tag{2.15}$$

where E corresponds to E_{on} or E_{off}, depending on the switching transient. Thus, the average switching losses, P_{sw}, are calculated as the mean value of $P_{\mathrm{sw}}(i)$ throughout the whole mains period.

2.4.2 Definition of the Simulation Models and Considerations

As previously mentioned, the comparison methodology applied in this work requires from simulation models to analyze the current and voltage waveforms related to each topology [92]. Thus, the simplified models depicted in Figure 2.20(a) have been adopted for active topologies which consider the main following assumptions:

- The semiconductors are considered to be ideal switches.
- The DC bus voltage is considered to be an ideal voltage source and, consequently, the voltage ripple is neglected.
- The AC-side, that it the SG, is modeled as three ideal current sources which do also neglect the current ripple and permit to modify the operating PF. Thus, the phase current RMS value, (i_{ph}), of the current sources is defined as,

$$i_{\mathrm{ph}} = \frac{P_{\mathrm{conv}}}{3 \cdot V_{\mathrm{ph}} \cdot \cos(\varphi)} \tag{2.16}$$

in which for the converter nominal conditions: $P_{\mathrm{conv}} = 18.75\,\mathrm{kW}$, $V_{\mathrm{ph}} = 115\,\mathrm{V}$ and $\cos(\varphi)$ represents the PF operating scenario. Thus, if $\cos(\varphi) = 1$, $i_{\mathrm{ph}} = 54.34\,\mathrm{A}$ and $\cos(\varphi) = 0.85$, $i_{\mathrm{ph}} = 63.94\,\mathrm{A}$.

- The efficiency (η) calculation is based on the conduction and switching losses of the em-

ployed semiconductor.

$$\eta = \frac{P_{\text{conv}}}{P_{\text{conv}} + \sum(P_{\text{cond}} + P_{\text{sw}})} \cdot 100 \geq 97\,\% \tag{2.17}$$

where P_{cond} and P_{sw} correspond to the average conduction and switching losses, respectively.

- The power quality calculation, i.e. THD_{v} and WTHD_{v}, is based on the simulated converter terminals V_{LL} waveform and calculated as,

$$\text{THD}_{\text{v}} = \frac{\sqrt{\sum_{h \geq 2}^{\infty} V_{\text{h}}^2}}{V_1} \tag{2.18}$$

$$\text{WTHD}_{\text{v}} = \frac{\sqrt{\sum_{h \geq 2}^{\infty} \left(\frac{V_{\text{h}}}{h}\right)^2}}{V_1} \tag{2.19}$$

where V_{h} is the RMS voltage value of the hth harmonic frequency component, being V_1 the fundamental frequency voltage RMS value. These calculations do not actually express the harmonic pollution on the AC current, but they can be used to estimate the required filtering effort so that the current harmonic limits are fulfilled.

- The thermal limits of the converter are defined according to the datasheet characteristics of the semiconductor. Thus, since different semiconductor technologies are modeled, the maximum admissible junction temperature is defined as $T_{\text{j,max}} - 15\,^{\text{o}}\text{C}$ for each power device in Table 2.5. Note that a safety margin of $15\,^{\text{o}}\text{C}$ is established to avoid the semiconductor burnout.

- Since a high switching frequency is targeted with respect to the SG frequency, the junction temperature ripple is considered as negligible, and a steady-state thermal model based on the datasheet $R_{\text{th,j-c}}$ is considered to calculate the $\Delta T_{\text{j-c}}$ of the semiconductors. Thus,

$$\Delta T_{\text{j-c}} = (P_{\text{cond}} + P_{\text{sw}}) \cdot R_{\text{th,jc}} \tag{2.20}$$

Thus, the average junction temperature, T_{j}, which must be below $T_{\text{j,max}} - 15\,^{\text{o}}\text{C}$, is calculated as,

$$T_{\text{j}} = \Delta T_{\text{j-c}} + T_{\text{c}} \tag{2.21}$$

where T_{c} represents the case temperature value, typically defined as $80\,^{\text{o}}\text{C}$. Therefore, no cooling system is considered in this stage.

- Space Vector Pulse Width Modulation (SVPWM) pattern has been assumed for all topologies and $m = 1.13$ to ensure the minimum conduction and blocking times of the employed semiconductor.

Similarly, most of the previous assumptions have also been considered for the DC/DC stage in Figure 2.20(b). In this case, though, two main modifications have been done due to the difference between AC/DC and DC/DC power stages, being:

- The high DC voltage side, that is the AC/DC rectifier output voltage V_{DC}, is modeled

with a voltage DC source.

- The low DC voltage side, i.e. $270\,V_{DC}$ bus side, is modeled as a DC current source.
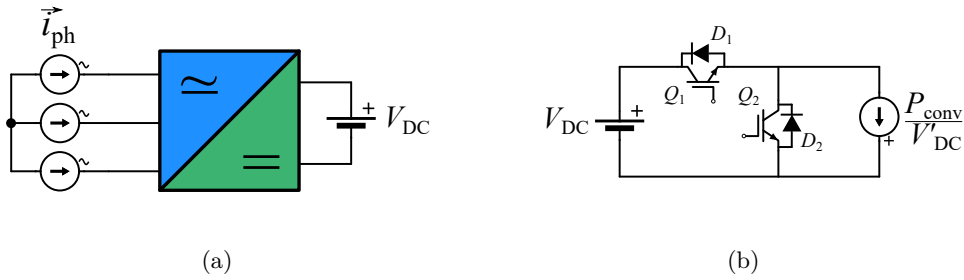

<div align="center">(a)   (b)</div>

Figure 2.20 Simplified models of (a) active rectifier topologies, and (b) DC/DC topology

Note that, in both models of Figure 2.20, the current source defines the power flow direction, and hence, the operation mode of the simulated converter, being rectifier or inverter. An important point to remark when employing these models is the different operating conditions of the analyzed power converters when operating at unity PF or at 0.85 lagging PF.

When the AC/DC converter is operating at unity PF a second power stage is needed to reduce the boosted rectifier output voltage V_{DC} to the targeted $270\,V_{DC}$. In this context, the rectifier output voltage V_{DC}, which is the middle DC bus voltage between AC/DC and DC/DC stages in the two-stage configuration, plays a critical role in the converter design. Under the guise of designing a high-efficient and compact converter, a maximum input inductor voltage of $V_L = 20\,\%\cdot V_{ph}$ is assumed aiming a reduced V_{DC} value and, hence, switching losses. Thus, assuming the worst case operating scenario of DO-160G, where $V_{ph} = 122\,V$ and $f = 800\,Hz$, and applying (2.2) and (2.4), a middle DC bus voltage value of $312\,V_{DC}$ is calculated for $m = 1.13$. This middle DC bus voltage, used as voltage source value in the models of Figure 2.20, is then reduced to the targeted $270\,V_{DC}$ by the second stage buck converter. Therefore, the overall two-stage power converter efficiency, η_{tot}, is determined by the aggregate of the efficiency of both power stages.

$$\eta_{tot} = \eta_{AC/DC} \cdot \eta_{DC/DC} \tag{2.22}$$

Unlike at unity PF operation, when the AC/DC converter is operating at 0.85 lagging PF there is no need of a second power stage, and thus, the output voltage V_{DC} in Figure 2.20(a) is directly fixed at $270\,V_{DC}$.

On the contrary to the previously presented models of active rectifiers, the model of the passive rectifier is not described in [92]. However, considering the previously described assumptions for active rectifier models and the 12-pulse ATRU designed in [48,71], a simplified model of the ATRU, presented in Figure 2.21, is defined for the benchmarking analysis. Thus, as in the previous models, several assumptions have been considered in order to provide a simulation model close to the real models presented in [48,71]:

- The first 6 assumptions of active rectifier simulation models, being ideal switches, power losses distribution symmetry, efficiency calculation, power quality calculation, the thermal converter thermal limit definition and the temperature increase calculation are still applied.

- The autotransformer is considered to be an ideal transformer that provides a phase displacement of $30\,^{\circ}$ between the input voltages of "*Diode bridge 1*" and "*Diode bridge 2*".

- The line inductance, L, represented in Figure 2.21, is calculated by scaling the calculation in [71] in terms of power, being,

$$L = \frac{3}{2} \cdot \frac{\hat{V}_{\mathrm{ph}}^2}{2\,\omega\,P_{\mathrm{conv}}} \tag{2.23}$$

where a line inductance of $188\,\mu\mathrm{H}$ is calculated for a $10\,\mathrm{kW}$ ATRU apart from for fulfilling current harmonics. This fact is also fulfilled in [48] for the same aviation standards but a different converter power. Thus, for the defined $P_{\mathrm{conv}} = 18.75\,\mathrm{kW}$,

$$L = 188\,\mu\mathrm{H} \cdot \frac{10\,\mathrm{kW}}{18.75\,\mathrm{kW}} = 100\,\mu\mathrm{H} \quad . \tag{2.24}$$

- The DC load is considered to be an ideal current source.
- The AC-side, that is the SG, is modeled as three ideal voltage sources.
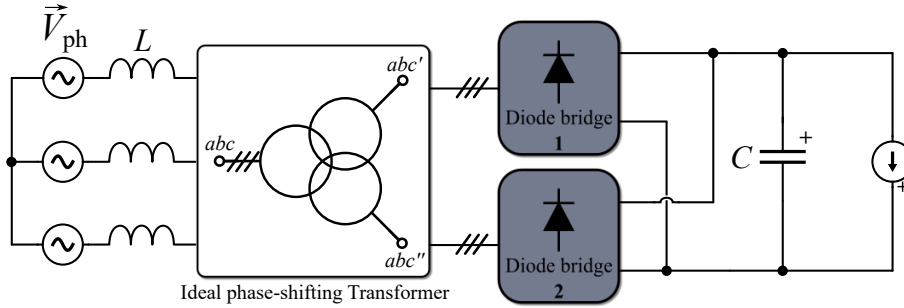- The operating PF is a result of the provided simulation model.

Figure 2.21 Simplified model of the ATRU.

2.5 Active Topologies Evaluation and Benchmarking with a Conventional ATRU

Based on the characterized semiconductor models and the simplified simulation models, the evaluation and of active rectifiers and comparative analysis with ATRU is presented in this section. Thus, the topology-semiconductor selection is performed first in order to enhance the efficiency and power density potential of the preselected topologies for the evaluation, i.e. Two-Level Boost, NPC and T-Type topologies. Afterwards, an efficiency analysis per topology considering the different operating scenarios is presented, being PF = 1 operation and PF = 0.85 operation for the two-stage and single-stage configuration, respectively. Finally, the converter with the highest potential in terms of efficiency are finally benchmarked with the ATRU.

2.5.1 Evaluation of the Active Topology - Semiconductor Pairs

As previously mentioned, the DC/DC power stage is considered as crucial point to analyze in this comparison since it constraints the performance of the first power stage. The relatively high

currents to be handled are reflected in the semiconductors power losses and hence, efficiency. In fact, although this converter is only considered when the AC/DC stage operates at unity PF (either in rectifier or inverter operation) the power losses of this stage should also be considered in terms of the latter cooling system design. Figure 2.22(a) represents the simulated DC/DC converter and the corresponding waveforms to each semiconductor in "buck mode" (rectifier operation). Note that the depicted waveforms are representative of employing the Hybrid IGBT power device to clearly express the current flowing through the power devices.
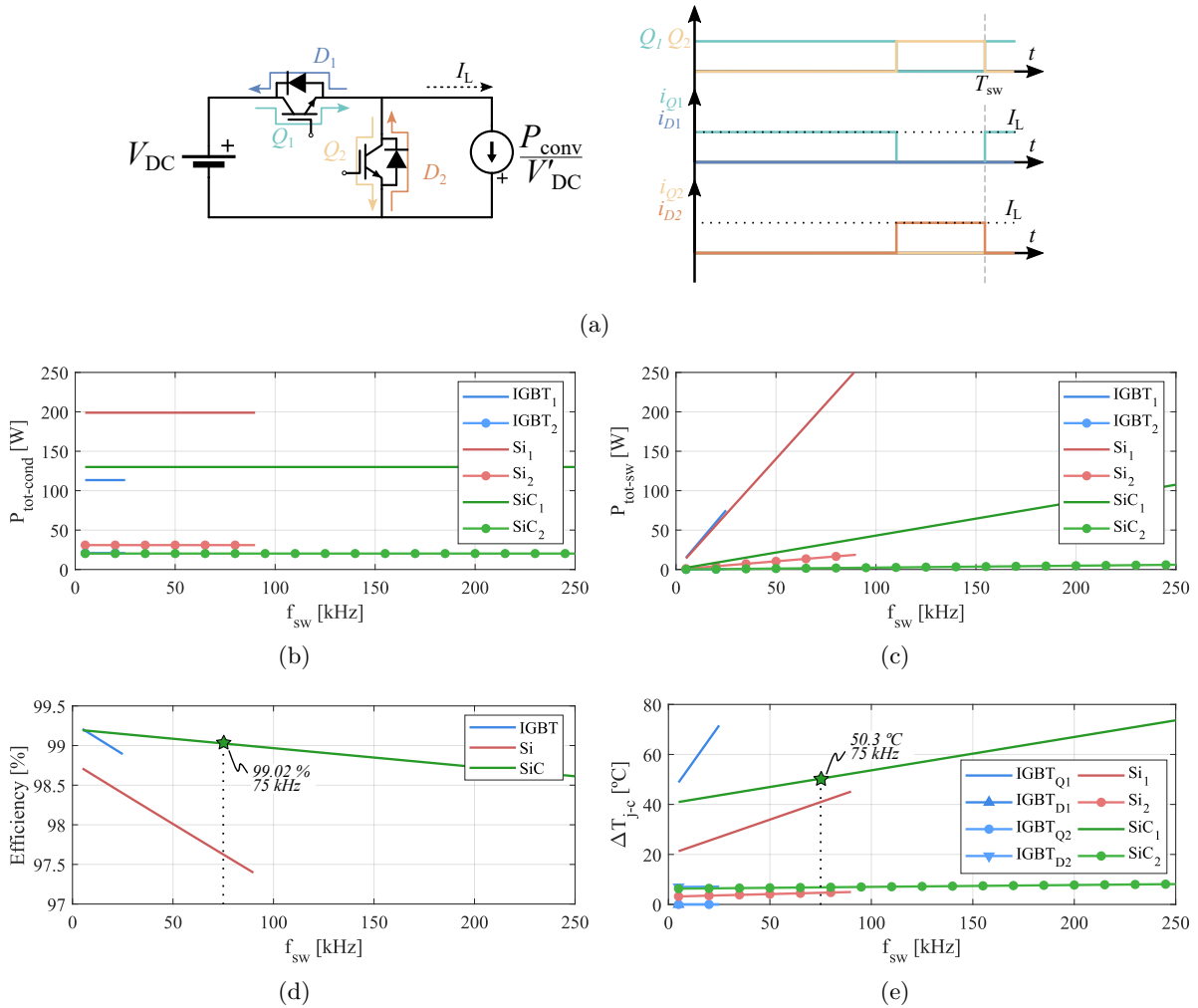

Figure 2.22 (a) Representation of the simulated DC/DC and the current waveforms of the devices. The simulation results for each power device are presented in (b) for P_{cond}, (c) for P_{sw}, (d) for η and (e) for ΔT_{j-c}.

From the verified simulation results of the DC/DC stage as buck converter and boost converter (AC/DC inverter operation) it is concluded that "*buck mode*" operation results to be the worst-case operating condition for the devices. Concretely, for the transistor Q_1 which operates at a higher duty cycle, D_{buck}, which is calculated as [101],

$$D_{buck} = \frac{V_{out}}{V_{in}} = \frac{V'_{DC}}{V_{DC}} = \frac{270\,V}{312\,V} = 0.865 \ . \tag{2.25}$$

When the DC/DC converter operates in buck operation, device 1 not only dissipates a higher

amount of conduction losses but also the switching losses corresponding to the transistor (Q_1), which is why "*buck mode*" results to be the worst-case operating mode. The switching power losses corresponding to the device 2, on the contrary, correspond to the losses of the diode, which are certainly lower compared to the switching losses of the transistor. Nevertheless, during "*boost mode*" operation, device 1 switching losses are reduced to the body diode switching losses and hence, its overall dissipated power loss is decreased.

Overall, from the results in Figure 2.22, it is concluded that the selected SiC MOSFET presents the higher potential in order to achieve a high f_{sw} and, hence, a high power density of the DC/DC stage. Not only low P_{cond} are achieved with the SiC MOSFET compared to the ones of the Si MOSFET, but also a relatively close P_{cond} value to the ones of the IGBT (see Figure 2.27(a)). In terms of switching losses, though, the SiC MOSFET takes advantage over the IGBT as presented in Figure 2.27(b). Consequently, even if it does not present the best thermal results in Figure 2.27(c), it is the SiC MOSFET the one that presents the highest efficiency performance. Note that the ΔT_{j-c} is calculated according to the power losses of the device and the datasheet $R_{th,j-c}$ value, for which the Si MOSFET one is reported as approximately three times lower than for the SiC MOSFET.

Aiming to define the DC/DC f_{sw} value, and thus the DC/DC η and ΔT_{j-c} values for the latter comparative analysis, the influence of the f_{sw} on the value of the passive elements has been studied. According to [101], the passive elements of a buck converter, being the inductor, L, and the capacitor, C, are defined as,

$$L = \frac{(V_{DC} - V'_{DC}) \cdot V'_{DC}}{V_{DC} \cdot f_{sw} \cdot \Delta I_{L}} \tag{2.26}$$

$$C = \frac{(1 - \dfrac{V'_{DC}}{V_{DC}}) \cdot V'_{DC}}{8 \cdot L \cdot f_{sw}^2 \cdot \Delta V_{DC}} \tag{2.27}$$

being ΔI_{L} and ΔV_{DC} the output current and output voltage ripples, respectively. In accordance to (2.26) and (2.27), the expected value of the inductance and the capacitance have been illustrated in Figure 2.23 assuming a ΔI_{L} of 10 % and a ΔV_{DC} of 2.22 % as specified in DO-160G.
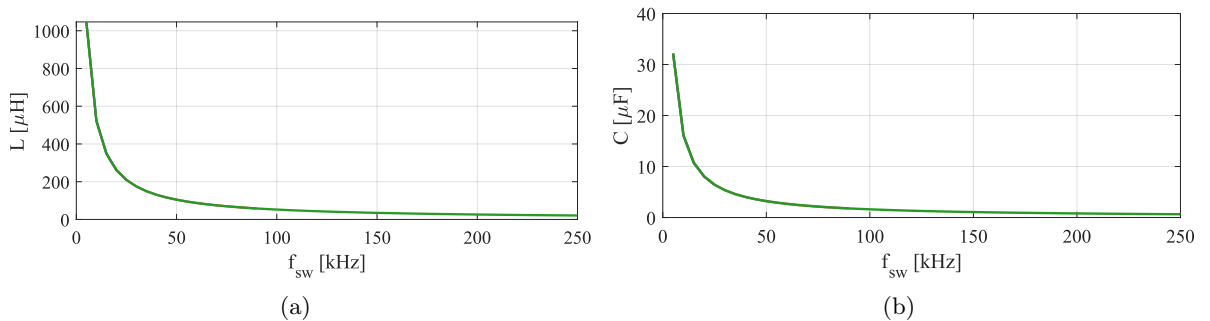

Figure 2.23 (a) Calculated value of passive elements depending on the converter f_{sw}. (a) Output inductor, L, value, while (b) represents the output capacitor, C, value.

According to the illustrated results, the larger the f_{sw}, the lower the value of the passive

elements, and hence, the lower the expected volume. In this context, SiC MOSFET technology is selected as the most suitable to achieve the highest frequency possible. However, beyond the "*knee*" of both curves ($\approx 75\,\text{kHz}$), reducing the value of the passive elements significantly supposes a considerable increase in the switching frequency. Thus, a $75\,\text{kHz}$ switching frequency is defined for the DC/DC stage which, consequently, leads to a $99\,\%$ efficiency of this power stage due to the $151\,\text{W}$ and $34\,\text{W}$ of the total P_{cond} and the total P_{sw}, respectively. In addition, a $\Delta T_{\text{j}-\text{c}}$ of $50.3\,^{\circ}\text{C}$ is also calculated. These key parameters regarding the DC/DC stage are summarized in Table 2.6.

Table 2.6 Summary of the defined operating point for the DC/DC power stage.

Parameter	Value
η	$99\,\%$
f_{sw}	$75\,\text{kHz}$
Total P_{cond}	$151\,\text{W}$
Total P_{sw}	$34\,\text{W}$
$\Delta T_{\text{j}-\text{c}}$	$50.3\,^{\circ}\text{C}$

Regarding the AC/DC topologies, the same analysis in terms of semiconductor technology suitability has been performed for Two-Level Boost, NPC and T-Type topologies. Their respective analysis results are presented in Figure 2.24, Figure 2.25 and Figure 2.26. Note that, as in the DC/DC case, the presented current waveforms of the power devices correspond to the ones of the Hybrid IGBT. It is worth to mention that, since buck operation mode results constraining in the DC/DC stage, the topology-semiconductor pair analysis presented in the following only describes the rectifier mode operation. In addition, only PF $= 1$ operation (assuming $V_{\text{DC}} = 312\,\text{V}$) is presented because a clear trend on the topology-semiconductor pair performance can be observed.

From the power losses analysis results, it is concluded that conduction losses are dominant in this application for the considered power semiconductor devices. Thus, hybrid IGBT and SiC MOSFET technologies result to be advantageous in this domine. However, the switching losses of the Hybrid IGBT double the switching losses of SiC MOSFET, which leads to a higher efficiency result for the latter device. Therefore, SiC MOSFET technology is preferable to achieve a high f_{sw}, reduced value of the passive elements and a high power density converter. Note that this trend occurs for the three active rectifiers. Consequently, SiC MOSFET *ST-SCTW90N65G2V* and *GeneSiC-GC50MPS06-247* Schottky Diodes have been considered for the presented active rectifiers. Similarly, *GeneSiC-GC50MPS06-247* Schottky Diode is considered for the ATRU power losses evaluation.
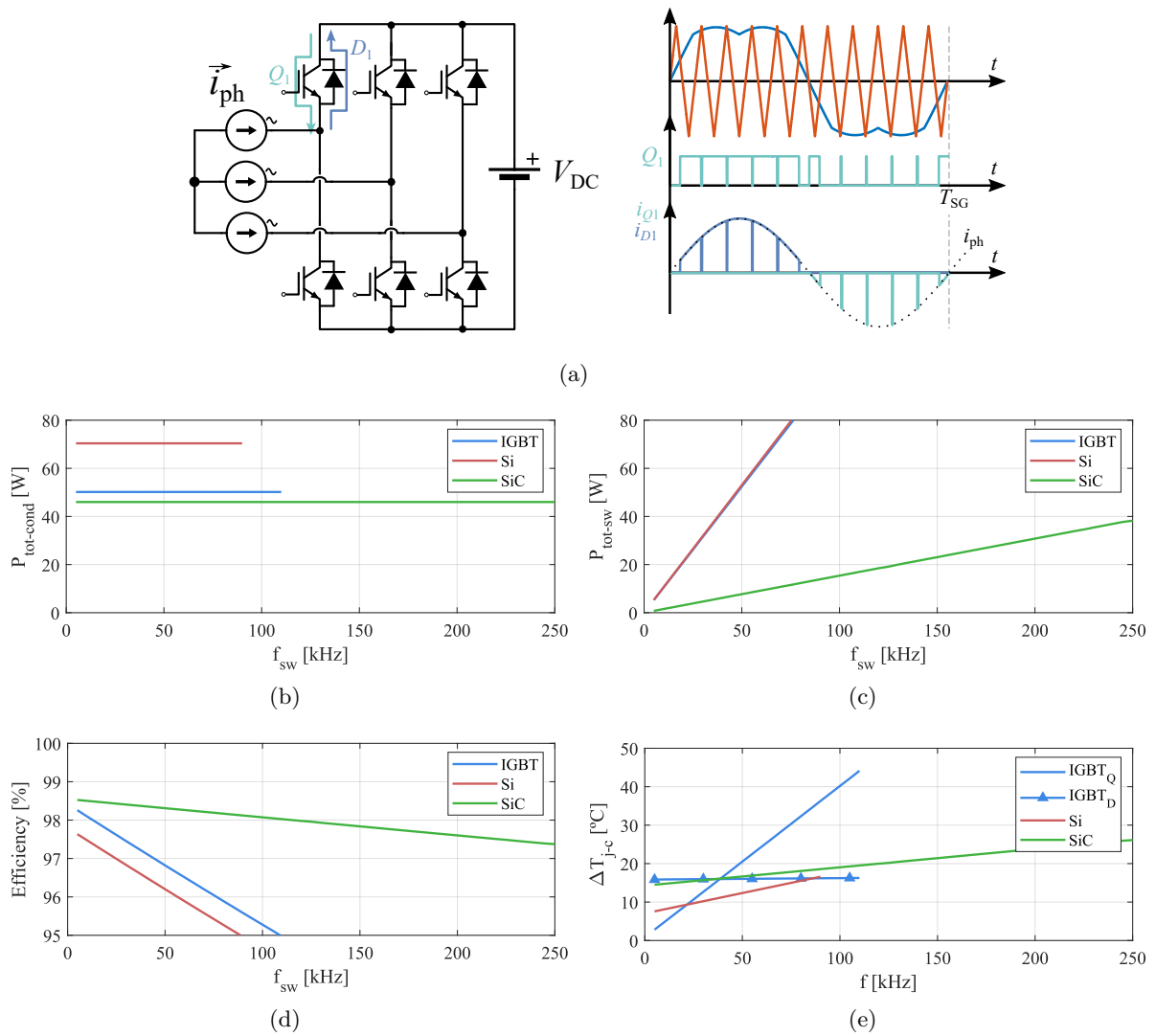
Figure 2.24 (a) Schematic representation of the Two-Level Boost AC/DC model and the current waveforms of the devices. The simulation results for each power device are presented in (b) for P_{cond}, (c) for P_{sw}, (d) for η and (e) for ΔT_{j-c}.

(a)

(b)

(c)

(d)

(e)

Figure 2.25 (a) Schematic representation of the simulated NPC AC/DC model and the current waveforms of the devices. The simulation results for each power device are presented in (b) for P_{cond}, (c) for P_{sw}, (d) for η and (e) for $\Delta T_{\text{j-c}}$.
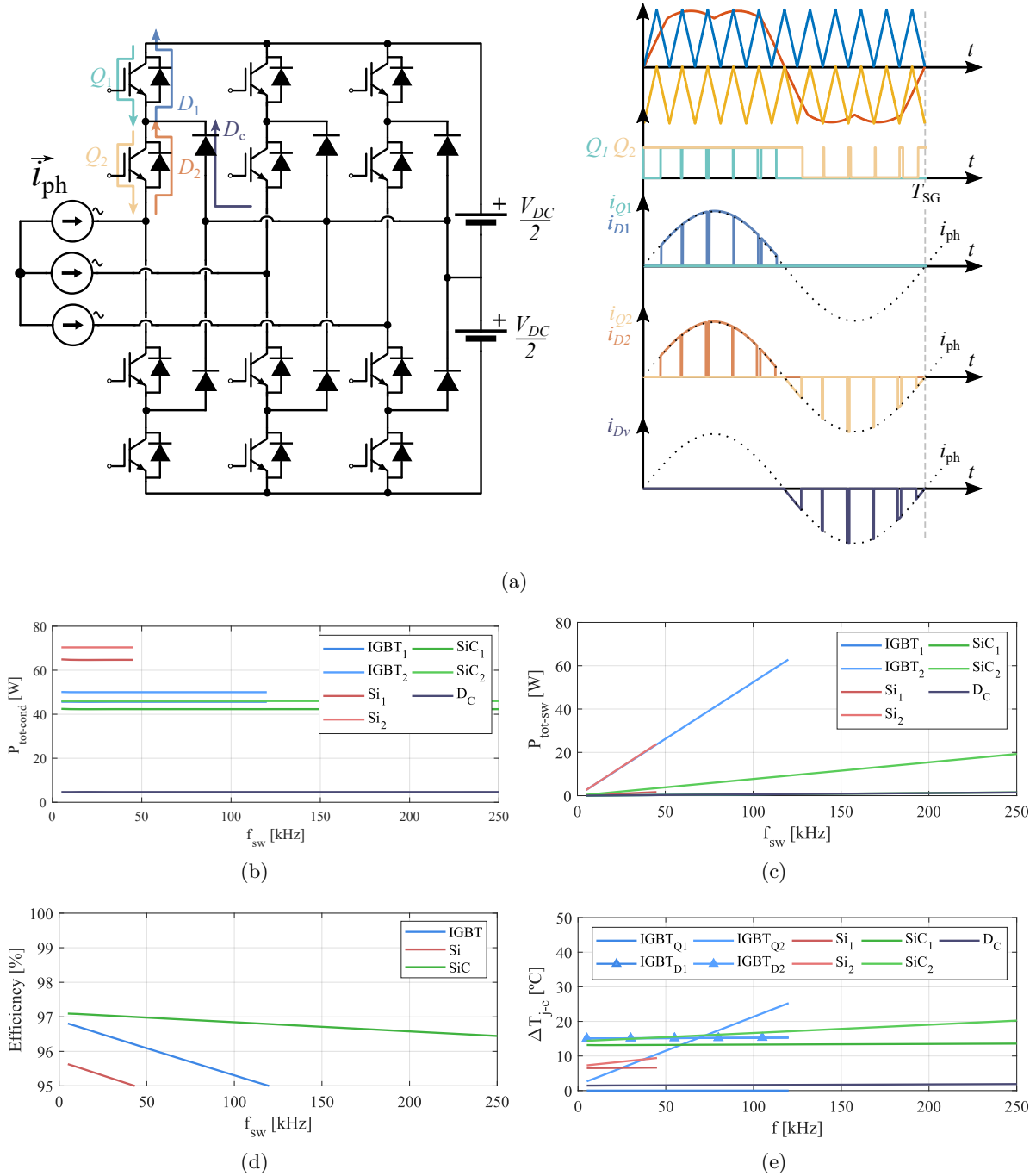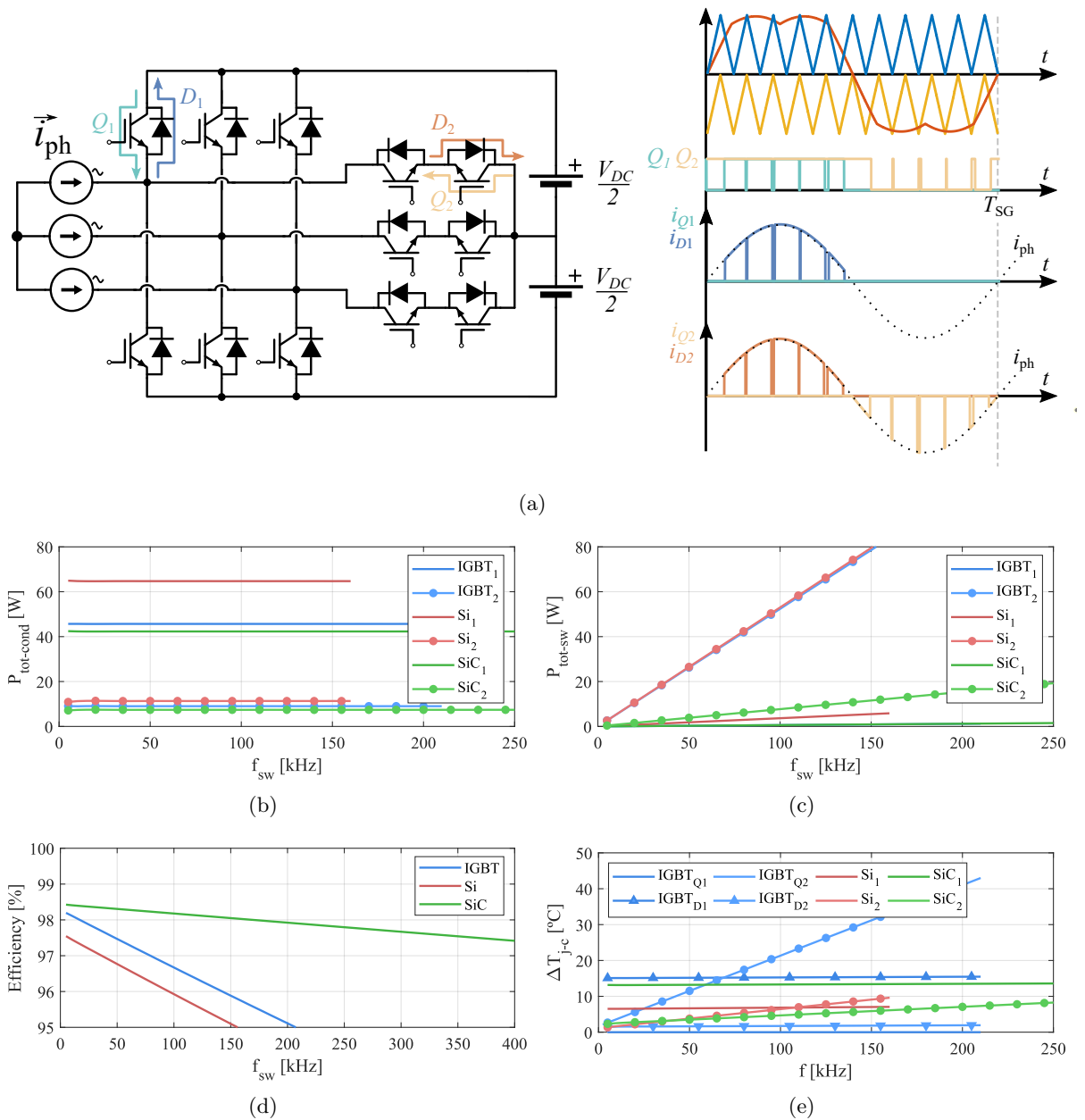
Figure 2.26 (a) Schematic representation of the simulated T-Type AC/DC model and the current waveforms of the devices. The simulation results for each power device are presented in (b) for P_{cond}, (c) for P_{sw}, (d) for η and (e) for $\Delta T_{\mathrm{j-c}}$.

2.5.2 Evaluation of the Active Topologies Operating at PF = 1 and PF = 0.85

Along with the topology-semiconductor selection, the suitability of the two-stage and single-stage concepts must be evaluated. Thus, the objective of this evaluation is to verify that the preselected topologies, i.e. Two-Level Boost, NPC and T-Type topologies, fulfill the efficiency targets in any of the operating scenarios. In this regard, Figure 2.27 shows the results of the two-stage and single-stage configurations considering that,

- when the AC/DC topologies operate at PF = 1, V_{DC} = 312 V and, hence, a second DC/DC power stage is required for achieving a 270 V DC bus voltage. In order to express the effect of adding a DC/DC stage in terms of efficiency, the results of the AC/DC stage, named as "*PF = 1*", and the results of the overall two-stage converter, named as "*two-stage*", are presented. Note that an efficiency of $\eta_{DC/DC}$ = 99 % has been considered for the latter option as previously calculated in Table 2.6.
- When the AC/DC topologies operate at PF = 0.85, V_{DC} = 270 V. Thus, no additional DC/DC is required for this converter and a single-stage configuration is assumed.
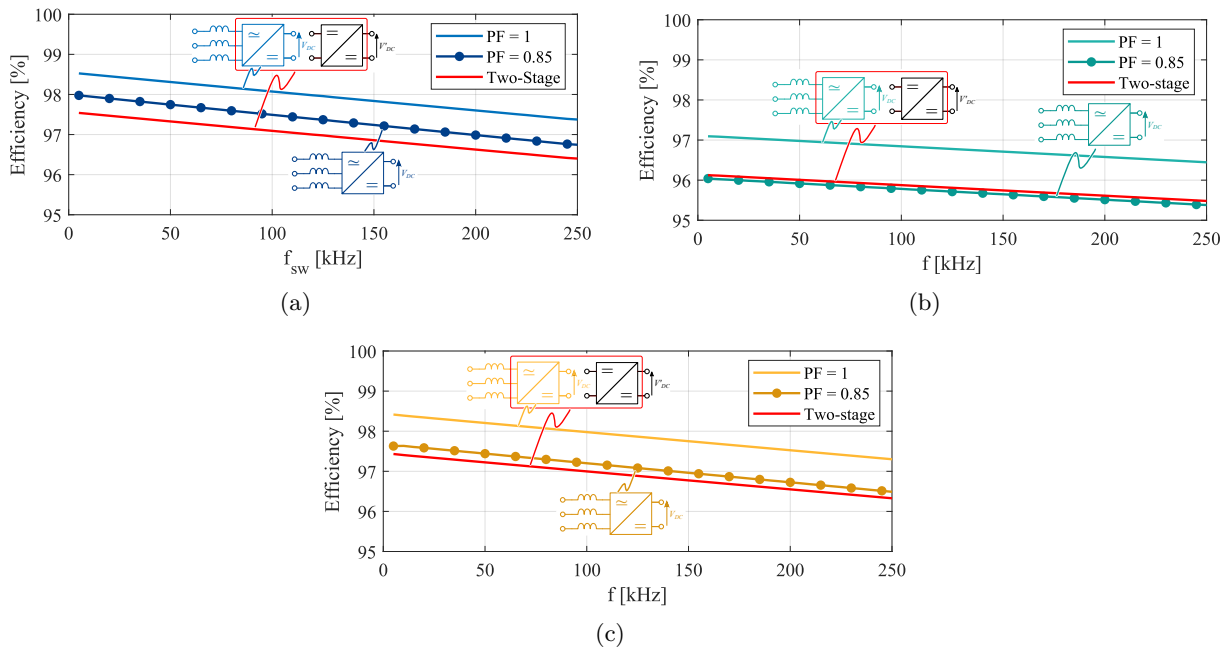

Figure 2.27 Efficiency results of both two-stage and single-stage configurations for (a) Two-Level Boost, (b) NPC, and (c) T-Type topologies.

From the results, it is observed that Two-Level Boost and T-Type topologies present an efficiency ≥ 97 % in both single-stage and two-stage configurations. The NPC-based configurations, conversely, exhibit the lowest efficiency results and do not achieve the minimum efficiency target of 97 %. The main reason is that, on the contrary to the other topologies, the NPC topology possesses two serialized power devices (see Figure 2.25(a)) and, due to the fact that conduction losses are predominant, the efficiency of NPC-based configurations is dramatically diminished. In fact, even the AC/DC stage operating at PF = 1 on its own vaguely reaches an efficiency value superior to 97 %. Therefore, the NPC configurations will no longer be considered for the benchmarking analysis.

2.5.3 Benchmarking Analysis and Results

As previously mentioned, the performance of the ATRU and active topologies can be evaluated by means of the efficiency, η, which should be higher than 97 %, the terminals voltage waveform power quality results, i.e. the THD_v and the $WTHD_v$, the number of power devices, the maximum temperature difference between their junction and case, that is ΔT_{j-c}, and the maximum achievable switching frequency, f_{sw}.

Furthermore, in order to provide a simplified benchmarking evaluation, nominal conditions have been considered in this section. Thus, all the topologies are operated at $P_{conv} = 18.75\,kW$ and $f = 400\,Hz$. Note that assuming a different value of AC grid frequency for the comparison, between 360 Hz and 800 Hz of the permitted range in Table 2.1, could lead to different results in terms of power quality. However, the fact of targeting a switching frequency which is much higher than the SG frequency makes this difference in the power quality results negligible.

Figure 2.28 represents the results of the performance analysis of the topologies in terms of efficiency, power losses and temperature increase. As presented in Figure 2.28(a), operating at a relatively low PF results beneficial in terms of efficiency for Two-Level Boost and T-Type single-stage topologies. Similar efficiency results can be found for both topologies (either operating as two-stage and single-stage) which, in addition, present relatively close efficiency values ($\approx 1\,\%$) to ATRU at relatively high f_{sw} ($\approx 80 - 100\,kHz$).

It must be remarked that, due to the expected bidirectional power flow of active rectifiers, inverter operation mode, depicted in Figure 2.28(b), has also been considered to identify the critical operating condition, i.e. 97 % efficiency limit and $f_{sw,max}$ at either operating mode. Note that the power devices commutation pattern, and hence P_{sw}, might vary depending on the power flow and converter topology. In this regard, even if as previously demonstrated P_{cond} result dominant in the proposed comparative analysis, the increased P_{sw} of T-Type topology when operating as an inverter limit its switching capability (see the difference between Figure 2.28(e) and 2.28(f)). This fact is presented in Figure 2.28(b) where the minimum 97 % efficiency limit is achieved at lower f_{sw} values for T-Type configurations compared to their respective Two-Level Boost configurations. It is worth to mention that single-stage configurations do also result advantageous in terms of efficiency in inverter mode with respect to their counterpart two-stage configurations. Concretely, single-stage Two-Level Boost topology shows the best performance.

Consequently, although operating with a single-stage converter and a PF lower than unity implies polluting the AC grid with reactive power, a high potential is presented in terms of efficiency. Furthermore, not only the number of power devices is reduced compared to the two-stage topology but also a lower ΔT_{j-c} is achieved. The main reason is that, in the case of two-stage topologies, the highest amount of power losses per device occurs at the DC/DC power stage and, consequently, so does the ΔT_{j-c}. This fact is reported in Table 2.7, where a summary of the analysis (considering rectifier mode) is provided. As previously mentioned, this temperature increase could result harmful in terms of reliability. Thus, although not considered at this analysis stage, the parallelization of DC/DC converters results to be an interesting solution for reducing the increased thermal stress of two-stage configuration converters.
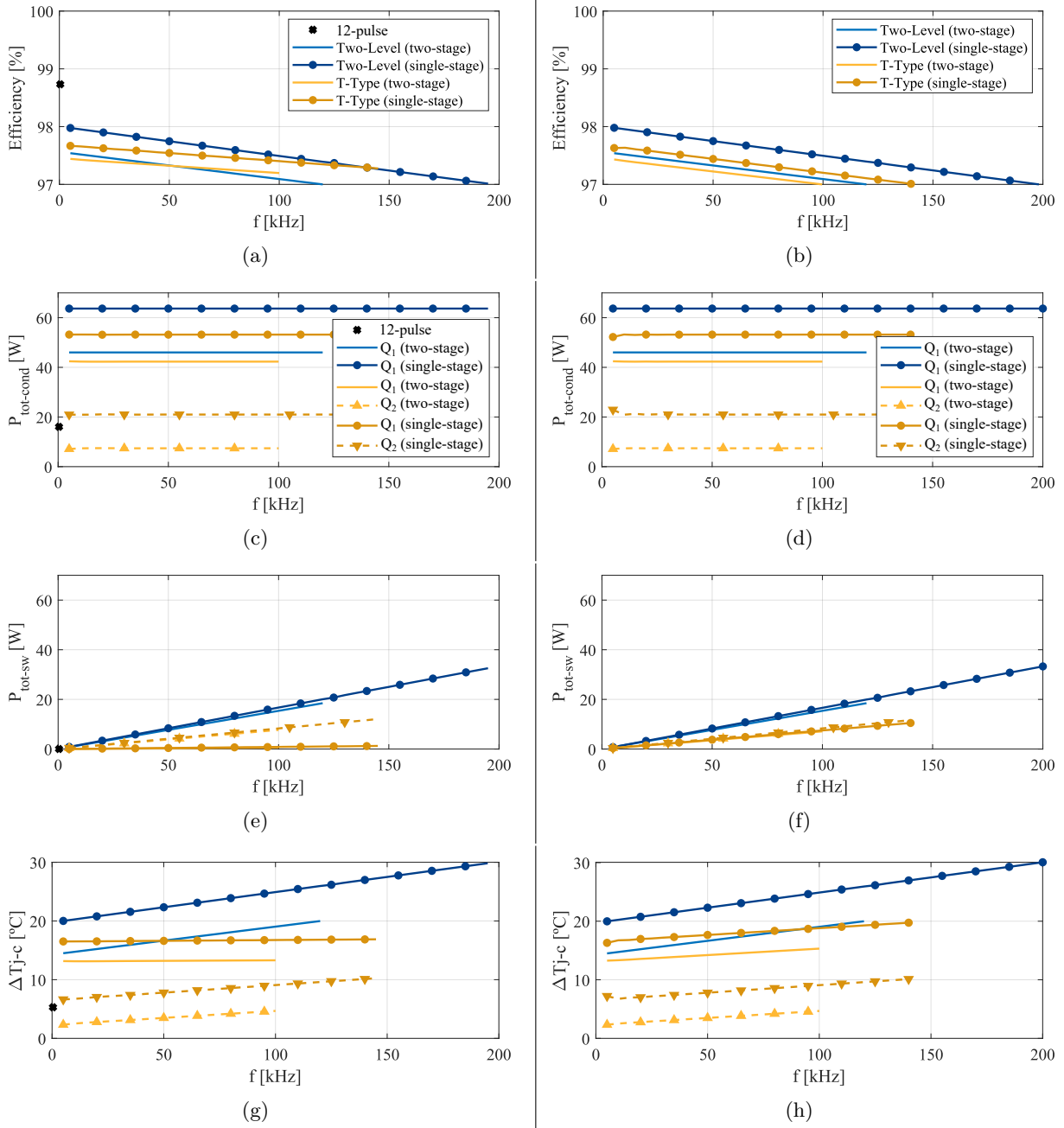
Figure 2.28 Performance analysis results of (a) efficiency in rectifier mode operation, (b) efficiency in inverter mode operation, (c) total P_{cond} per device in rectifier mode operation, (d) total P_{cond} per device in inverter mode operation, (e) total P_{sw} per device in rectifier mode operation, (f) total P_{sw} per device in inverter mode operation, (g) $\Delta T_{\text{j}-\text{c}}$ per device in rectifier mode operation, and (h) $\Delta T_{\text{j}-\text{c}}$ per device in inverter mode operation. Note that the results (c)-(h) only contemplate the AC/DC power stage results.

Table 2.7 Summary of the comparison analysis results in rectifier mode at the last simulated f_{sw} value.

	ATRU	Two-Level Boost		T-Type	
Operating PF	> 0.95	1	0.85	1	0.85
Nº of MOSFETs	-	8	6	14	12
Nº of Diodes	12	-	-	-	-
$f_{\text{sw,max}}$ [kHz]	-	120	195	100	145
Total P_{cond} [W]	193	$276 + 151$	382	$292 + 151$	445
Total P_{sw} [W]	0.2	$111 + 34$	196	$50 + 34$	79
Maximum $\Delta T_{\text{j}-\text{c}}$ [ºC]	5.3	51	30	51	17

With respect to the power quality results, even if a lower THD$_{\text{v}}$ is exhibited by the topologies which present a three-level voltage characteristic compared to the Two-Level topology (see Figure 2.29(a)), key information about power quality can be obtained from the WTHD$_{\text{v}}$ results in Figure 2.29(b). In this context, the Two-Level Boost topology benefits from a high switching frequency operation capability. The weight of harmonics above $80 - 100\,\text{kHz}$ results in relatively low filtering effort for this topology and a comparable WTHD$_{\text{v}}$ to three-level topologies is presented. Furthermore, above $100\,\text{kHz}$, the WTHD$_{\text{v}}$ value of the Two-Level Boost topologies appears to be four times lower than the value presented by the ATRU.
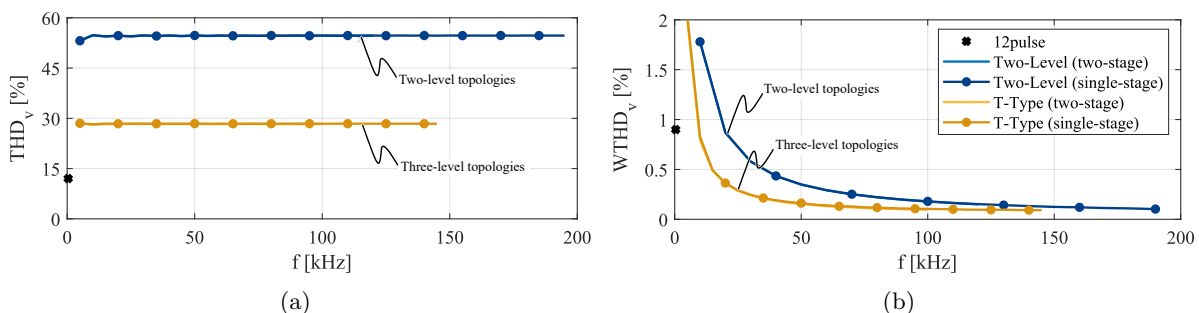
Figure 2.29 Power quality results, being (a) the THD$_{\text{v}}$ and (b) the WTHD$_{\text{v}}$.

Therefore, due to its relatively high efficiency, low filtering effort required, low number of power devices and simplicity, Two-Level Boost configurations are the preferred topologies for this application. Precisely, the single-stage configuration presents a greater potential in terms of efficiency and simplicity. The fact of presenting not only a lower number of power devices but also a decreased thermal and blocking voltage stress compared to the two-stage configuration results in an expected higher reliability. However, the relatively low PF operation implies polluting the grid with reactive power. Thus, improved solutions must be analyzed in order to avoid reactive power handling and achieve unity PF at the SG connection point.

It must be remarked though, that the performed analysis in this chapter represents a first step of the suitability of active rectifier topologies in MEA applications. However, the fact of implementing a power converter onboard an aircraft requires from a deeper analysis in terms of complying with aviation standards. Consequently, the development of both $18.75\,\text{kW}$ two-stage and single-stage optimized configurations into a $150\,\text{kW}$ rectifier architecture while fulfilling aviation standards becomes a research focus.

2.6   Summary

This chapter has presented the suitability of active rectifier topologies in MEA applications in order to replace the traditional ATRU. The imposed rectification scenarios by up-to-date aviation standards such as DO-160G or MIL-STD-704F, being $115\,V_{AC}$ to $270\,V_{DC}$ or $230\,V_{AC}$ to $\pm\,270\,V_{DC}$ depending on the manufacturer, are based on passive ATRU technology operation. These input/output voltage requirements, though, result in controllability limitations for active rectifier topologies. In this regard, the mathematical limits for active rectifiers operation have been analyzed and two main possibilities have been proposed for implementing boost-type active rectifiers in the existing $115\,V_{AC}$ to $270\,V_{DC}$ rectification scenario: *(1)* a two-stage configuration, i.e. an AC/DC converter followed by a downstream DC/DC converter, in order to implement a unity PF operating active rectifier; and, *(2)* a single-stage configuration which only employs an AC/DC converter owing to a lower PF operation such as the 0.85 lagging PF limit established in aviation standards.

Considering these two scenarios, Two-Level Boost, T-Type and NPC topologies are evaluated and benchmarked with passive ATRU technology assuming a $18.75\,kW$ converter nominal power. From the comparative results, it is demonstrated that active topologies present a great potential to replace the traditional ATRU technology. Furthermore, due to its relatively high efficiency, low filtering effort required, low number of power devices and simplicity, Two-Level Boost configurations are preferred for this application. Concretely, single-stage configuration presents greater potential in terms of efficiency and simplicity for the employed SiC MOSFET power device. Furthermore, this configuration not only presents a lower number of power devices but also a decreased average junction temperature compared to the two-stage configuration due to the higher amount of power losses per semiconductor dissipated by the DC/DC stage. Note that, the related power loss and temperature increase issues of the DC/DC stage could be improved if phase-leg parallelization is assumed. On the negative side of the single-stage configuration, operating at a $PF < 1$ implies polluting the grid with reactive power. Since unity PF is preferred at the connection point to the SG to avoid reactive power handling and achieve a higher efficiency, both single-stage and two-stage configuration topologies should be integrated into an active rectification architecture and assessed at this operating condition.

Comparative Analysis of Active Modular Rectifier Architectures Integrate in MEA

Summary:

The implementation of a two-level boost active rectifier in an active modular architecture structure complying with DO-160G aviation standard is aimed in this chapter. Based on a technical approach and considering the performed analysis of the difficulties and limitations of implementing two-stage and single-stage active rectifier topologies in the previous chapter, three different converter-configuration-based architecture alternatives are proposed and evaluated. The proposed converter configurations in this work, being the two-stage configuration, the single-stage with capacitor bank configuration, and the single-stage with static synchronous compensator configuration, are focused on achieving unity PF on the AC aircraft grid-side in order to avoid the reactive power pollution. The design of each active modular architecture is presented, and a wide comparison framework is proposed focusing on efficiency, power density (referred to volume), and reliability with the aim of identifying the most suitable architecture among the three proposed potential solutions.

3.1   Proposed Converter Configurations operating at unity PF for the Active Modular Architecture Development

In the preceding chapter, the suitability of active rectifiers in MEA applications was studied. Due to the imposed passive ATRU based input/output voltage requirements by up-to-date aviation standards, i.e. a $115\,V_{AC}$ input voltage and a $270\,V_{DC}$ output voltage, operating at unity PF while fulfilling the operating voltage requirements resulted impracticable for active rectifier topologies due to the output voltage controllability limitations. This fact, led to the development of alternative converter configurations. Thus, a two-stage configuration, being an active rectifier operating at unity PF followed by a downstream DC/DC converter, and a single-stage configuration, being an active rectifier operating at a 0.85 lagging PF, were proposed to fulfill the voltage operating requirements. In addition, two-level boost, NPC, and T-type topologies were compared as the potential employable active rectifiers (considering both two-stage and single-stage operating scenarios) and benchmarked with a 12-pulse ATRU considering a $18.75\,kW$ nominal power. As a result of the analysis, the suitability of active rectifiers was verified by using both configurations. Moreover, two-level boost configurations had the highest efficiency and a high power quality at relatively higher switching frequencies due to implementation of WBG technology.

Verifying the suitability of an active rectifier module is not the only challenge in aviation context, though. In fact, the parallel active modular rectifier operation aiming to achieve an increased overall architecture power rating such as the $150\,kW$ rated power of the SG of Airbus A380 with high efficiency, high power density and a high degree of redundancy is considered to be a research focus in recent literature [10, 32, 50, 61]. A graphical description of this concept is presented in Figure 3.1 below.
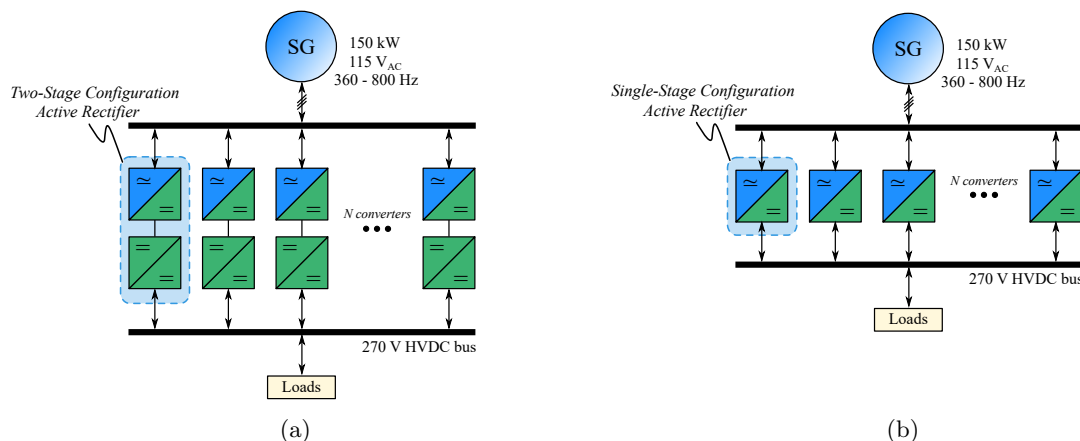
Figure 3.1 Simplified schematic of an active modular architecture based on (a) two-stage configuration converter modules, and (b) single-stage configuration modules.

In this regard, even if the resulting two-level rectifier based two-stage and single-stage configurations of the previous chapter presented a similar efficiency and power quality performance, remarkable power density differences could be found in the overall modular rectifier architecture

due to the implementation of second power stage or not. Consequently, in order to select the most suitable converter configuration choice for forming the 150 kW 8-converter-based active modular rectifier architecture, the integration of these configurations into a modular architecture and their comparison becomes a necessary task. It is worth to mention that, in order to achieve high efficiency and avoid reactive power handling, unity PF operation is desired in the aircraft AC grid side and, hence, in the connection to the SG. Thus, it is assumed that the active modular rectifier architecture implemented must operate at unity PF.

In this context, the two-stage configuration described in the preceding chapter, presented in Figure 3.2(a) and named from now on as $2L_2$ configuration, benefits from operating at unity PF. Although this concept appears to be a relatively simple configuration, the overall converter efficiency and power density are penalized by the downstream second power stage.
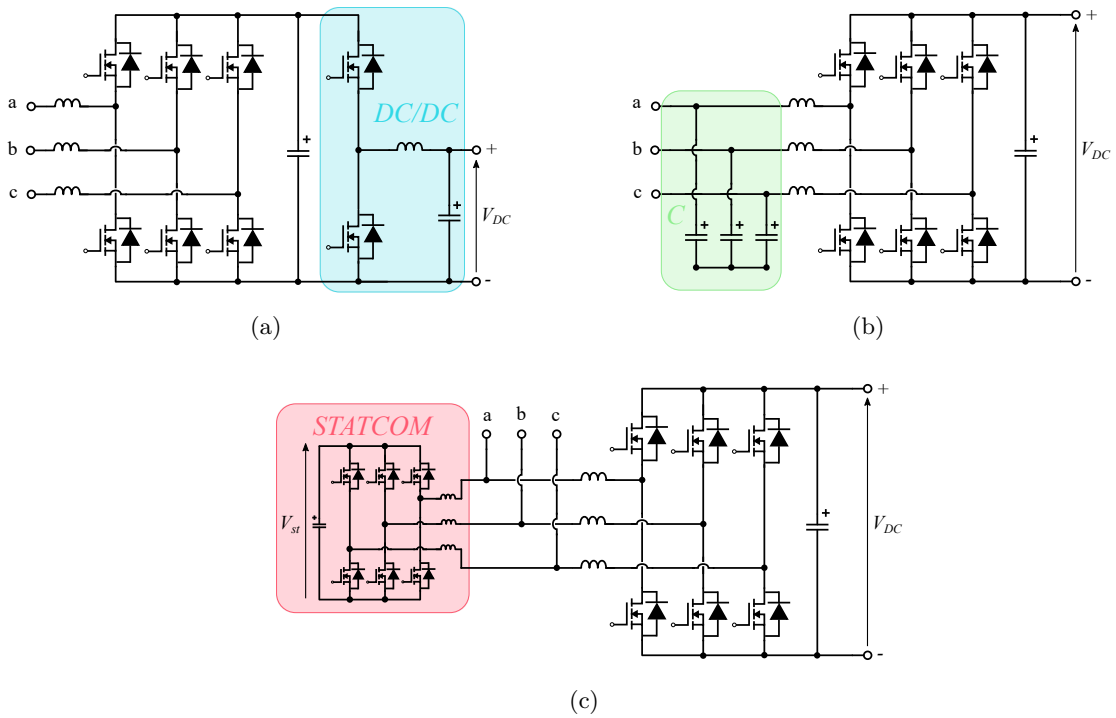

Figure 3.2 Schematics of the (a) two-stage $2L_2$ configuration, and the single-stage configurations with PF compensation, being (b) $2L_C$ and (c) $2L_{st}$ configurations.

In the case of the single-stage configuration, a 0.85 lagging PF is considered in the previous chapter due to the fact that this PF value represents the minimum operating PF limit of DO-160G standard. However, the direct connection of this converter configuration to the SG implies reactive power handling, which is not the desired operating scenario. Therefore, aiming to reduce the reactive power to be compensated at the converter terminals, increasing the operating PF of the single-stage configuration from the standardized minimum value of 0.85 lagging to the maximum possible value becomes a research task. It is worth to mention that this analysis, though, still involves the use of a minimum reactive power for achieving single-stage operation. Therefore, PF compensation becomes crucial for the single-stage configuration for achieving unity PF at the connection point to the SG.

On the one hand, the compensation of the lowered PF operation of single-stage configuration is proposed to be done by means of an input capacitor bank. This configuration concept, named $2L_C$ and represented in Figure 3.2(b), not only achieves unity PF operation at the SG connection point, but also improves the filtering characteristic, providing a second order LC filter. Thus, even if the $2L_C$ single-stage configuration has not been contemplated in the existing literature of aircraft applications, it is proposed as a potential option to be employed due to its inherent simplicity and expected single-stage configuration high efficiency. Furthermore, the thermal stress issues related to the second power stage of the $2L_2$ configuration are avoided in the $2L_C$ configuration. Regarding the power density, though, a relatively large volume could be expected for the $2L_C$ configuration due to the additional input capacitor bank. Note that the added capacitor bank should be designed to compensate the reactive power requested in the whole grid frequency range of nominal operating conditions, i.e. from 360 to 800 Hz. This fact, as later on described in higher detail in Chapter 3.3.2, results to be a downside of the $2L_C$ configuration. The main reason is that designing the capacitor bank for the maximum reactive power request operation, which is at 360 Hz, leads to lower converter operating PF at higher frequencies as a result of the needless amount of the capacitive current delivered.

Since the excessive capacitive current delivered by the capacitor bank at high SG frequencies leads to the converter performance worsening, the fact of implementing a "*variable capacitor*" might result beneficial. This way, the "*variable capacitor*" adjusts its reactive current delivery according to the SG frequency aiming to provide the minimum reactive current required for achieving single-stage operation. Hence, the maximum PF converter operation is maintained throughout the whole frequency range. Thus, the idea of replacing the input capacitor bank by a Static Synchronous Compensator (STATCOM) is put forward to form an additional converter configuration to be evaluated. Among the benefits of this configuration concept, depicted in Figure 3.2(c) and named as $2L_{st}$, no additional reactive power is handled as in $2L_C$ configuration and higher efficiency values might be achieved owing to a higher number of power converters and a lower overall power density architecture. However, an additional number of power converters might not be a drawback if the STATCOMs, which are disconnected from the distribution bus and establish their own individual higher DC voltage bus, were analogous to the rectifiers. Therefore, the STATCOMs could also operate as active rectifiers in case of a rectifier failure and, hence, provide a higher redundancy degree to the active rectification architecture.

To sum up, even if $2L_2$, $2L_C$, and $2L_{st}$ configurations achieve unity PF on the connection point to the SG, the selection of the most suitable converter configuration for implementing an active modular architecture is not straightforward. Due to the different attributes that surround each topology, a comparative analysis is required among the different architectures, which focuses on critical aspects related to the aviation context [7, 102], being efficiency, power density, reliability, and the proper architecture configuration design.

3.2 Comparison Framework for Active Modular Architectures

3.2.1 Efficiency Estimation

The efficiency calculation of the different architectures is based on the proposed evaluation methodology proposed in Chapter 2.4. Therefore, based on the application requirements in Table 2.1 and the simplified simulation models, the P_{cond} and P_{sw} of the power devices are evaluated according to the SiC MOSFET *ST-SCTW90N65G2V* semiconductor selected in the previous chapter and the converter operating conditions of each configuration (later on described and calculated in high detail). In this case, though, the aggregate of all the architecture semiconductor power losses are considered, and hence, the overall architecture efficiency, η_{arch}, is calculated as

$$\eta = \frac{P_{\mathrm{arch}}}{P_{\mathrm{arch}} + \sum(P_{\mathrm{cond}} + P_{\mathrm{sw}})} \cdot 100 \geq 97\,\% \tag{3.1}$$

where P_{arch} refers to the overall architecture transmitted active power, hence, 150 kW based on the Airbus A380 model [2, 22]. It is worth to mention that, from the application requirements of Table 2.1, a minimum of 97 % efficiency was targeted for the active rectification architecture.

3.2.2 Volume Estimation

The cooling system and passive elements are the main contributors to the overall converter weight and volume [102]. Estimations of the converter volume can be performed based on proportional parameters, such as the stored energy for passive components or the thermal resistance for the heat sink [102–104]. Thus, a comparative approach of the power density of the converters and, hence, architectures, could be obtained.

Cooling System Volume

According to [104], the volume of a converter heatsink, $\mathrm{Vol_h}$, is inversely proportional to its thermal resistance as,

$$\mathrm{Vol_h} = k_h \cdot \frac{N_{\mathrm{conv}}}{R_{\mathrm{th,h-amb}}} \tag{3.2}$$

where k_h corresponds to the volumetric thermal resistance of the specific heat sink type in $\mathrm{cm^3 \cdot {}^\circ C/W}$, and $R_{\mathrm{th,h-amb}}$ represents the thermal resistance from the heat sink to ambient in $^\circ\mathrm{C/W}$. With the aim of considering the volume of the overall architecture cooling system, the number of converters is introduced in the formula as N_{conv}. Note that, since the same heatsink type is assumed for the comparative analysis, the volumetric resistance can be neglected for comparative intentions.

Considering the semiconductor power losses evaluation in Chapter 2.4, the thermal models represented in Figure 3.3 are employed in order to calculate $R_{\mathrm{th,h-amb}}$. Figure 3.3(a) presents the simplified vertical cross-sectional view of a power semiconductor device and its Thermal Equivalent Circuit (TEC) which considers the following assumptions:
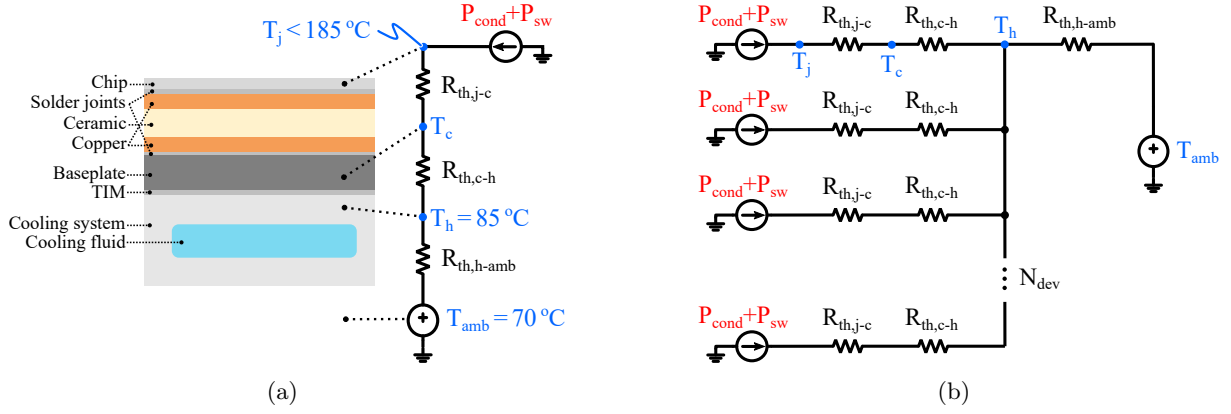
(a) (b)

Figure 3.3 Simplified analogy of (a) a power device TEC based on it vertical cross-sectional view, and, (b) the considered converter TEC for a specified number of devices, N_{dev}.

- For safety reasons, the achievable maximum junction temperature is defined as $15\,^{\circ}\text{C}$ lower than the datasheet temperature and, hence, is limited to $185\,^{\circ}\text{C}$.

- Water-cooling is assumed as in [105] in order to achieve a high power density architecture. Note that natural convection and forced air cooling might have a thermal resistance derating, that is a $R_{\text{th,h-amb}}$ value increase, around $40\,\%{-}50\,\%$ due to the lower density of the air at aircraft cruise operation heights [106].

- Based on the water-cooling system specifications of *IQ-evolution Gmbh* (see Figure 3.4 below) in [107], a temperature increase from ambient to heatsink, $\Delta T_{\text{h-amb}}$, of $15\,^{\circ}\text{C}$ is defined. Particularly, this heatsink is based on a 3D-metal-printed cooler which permits the the connection of the discrete SiC MOSFETs at both sides of the plate.
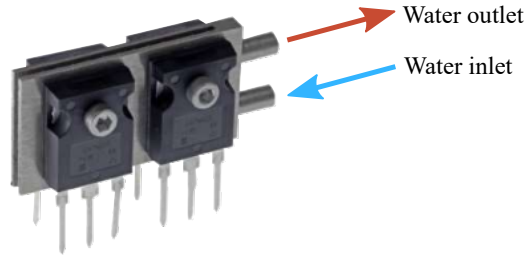

Figure 3.4 Example of the custom-sized water-cooling heatsink of IQ Evolution Gmbh considering four discrete power devices [107].

- An ambient temperature, T_{amb}, of $70\,^{\circ}\text{C}$ is assumed according to the worst-case temperature in [28, 62].

- Due to the high difference between the f_{sw} and the fundamental SG frequency f (more than 10 times), the junction temperature ripple (caused by the switching frequency) of the power semiconductor devices becomes negligible. Thus, instead of the transient impedances, only the thermal resistances are considered in this comparison.

Thus, based on this steady-state thermal model, the TEC of a converter is depicted in Figure 3.3(b) assuming that all the power devices are attached to the same heatsink. Consequently,

the thermal resistance from the heatsink-to-ambient is calculated as,

$$R_{\text{th,h-amb}} = \frac{\Delta T_{\text{h-amb}}}{\sum(P_{\text{cond}} + P_{\text{sw}})} \quad . \tag{3.3}$$

Volume of the Passive Components

In terms of passive elements, in [102, 103] the volume of a passive element, Vol_{p}, is proportionally related to its stored energy, E_{p}:

$$\text{Vol}_{\text{p}} = k_{\text{p}} \cdot E_{\text{p}} \tag{3.4}$$

where k_{p} represents a volumetric coefficient in dm^3/J of the passive element. Since this coefficient depends on the manufactured passive element structure and type, assumed to be equal for each architecture, it is neglected to provide a simplified analysis. In fact, even if different geometric structures and materials were used to manufacture passive elements, the dependency of volume with energy was verified in practice in [103].

The following expressions represent the stored energy for a capacitor, E_{C}, and an inductor, E_{L}:

$$E_{\text{C}} = \frac{1}{2} \cdot C \cdot \hat{V}^2 \tag{3.5}$$

$$E_{\text{L}} = \frac{1}{2} \cdot L \cdot \hat{i}_{\text{L}}^2 \tag{3.6}$$

where C and L represent the capacitance and inductance values, respectively; $\hat{V}$ expresses the capacitor peak voltage value, and $\hat{i}_{\text{L}}$ the peak current value flowing through the inductor.

3.2.3 Reliability Estimation

Power semiconductors are recognized as the most fragile components in terms of power converter reliability [94, 108, 109]. The failure rate of these components, which is a function of time, is commonly correlated to the bathtub curve in Figure 3.5 describing the different stages of the component lifetime [108]. In the early stages of the lifetimes of the devices, the failure rate is high due to the production quality fluctuations.
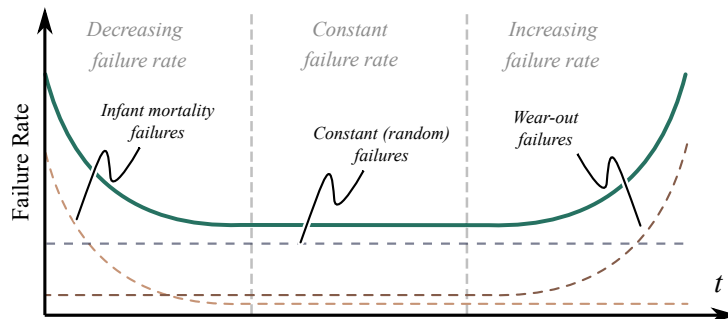

Figure 3.5 Example of a power device bathtub curve.

Regarding the useful life of the power device, its failure rate is considered constant and related to cosmic ray-induced failures [99, 108]. The origin of these failures come from highly

energetic atomic particles, which collide with the atoms of the power device, causing electric charges to be deposited in it. These charges, combined with high electric fields during a reverse blocking mode may result in a streamer of electrons producing a sudden device destruction due to the short-circuiting of a phase-leg [99].

In the last stage of the lifetime of the power device, failures are caused by wear-out of the chip and its package, known as wear-out failures [108]. These failures occur as a result of the electrothermal fatigue caused by the thermal cycling of the devices and the time-varying mission profile of the converter which, in this case, is linked to the flight stages of the aircraft in Figure 3.6 [94, 99, 110]. The mission profile represents all relevant conditions that the converter will be exposed to in the intended application, i.e., the altitude, ambient temperature, and output power, so that the stress that withstands the power device can be estimated by means of the lifetime model of the device.
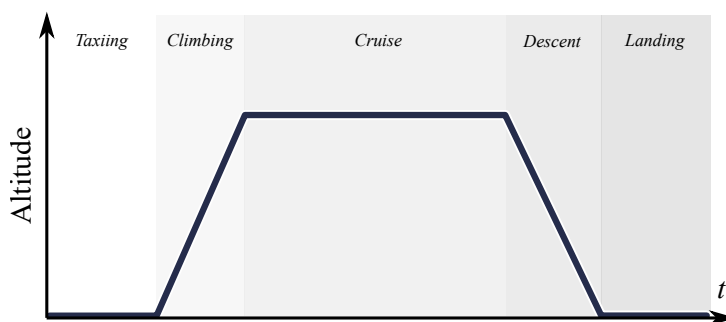

Figure 3.6 Flight stages of an aircraft mission.

Due to the lack of a standardized mission profile representative of aircraft applications, in this work, a simplified mission profile based on the one described in [99] is adopted and defined in Table 3.1. This way, it is considered a 1-hour flight at cruising altitude in which the active modular architecture operates at $150\,\text{kW}$ nominal power. It is also assumed that the aircraft performs six flights per day throughout the whole year.

Table 3.1 Simplified mission profile assumed for the wear-out failure reliability analysis.

Parameter	Value	Unit
Cruise time	1	h
Altitude, h	30,000	ft
Architecture operating power	150	kW
Flights per day	6	flight/day
Operating days per year	365	days

Cosmic Ray Failure Rate

Typically, the reliability of a component related to the cosmic ray-induced failures is expressed by its λ, being $\lambda = 1\,\text{FIT} = 1/10^{-9}\,\text{h}$. A Failure in Time (FIT) corresponds to, statistically, one failure per one billion hours of operation. The failure rate value of a power device is

mainly influenced by its reverse blocking voltage and the cosmic ray flux intensity [99, 108, 111]. In this work, the architecture failure rate estimation employed is based on the International Electrotechnical Commission (IEC) standard 62396-4 (referenced for high voltage power devices in aircraft applications) [99].

Taking into account the experimentally obtained curve in [111–113] for SiC MOSFETs, presented in Figure 3.7, the FIT/cm^2 of each device is calculated applying a curve fitting algorithm and employing the power device operating V_{DS}/V_{bd} ratio, being V_{DS} the MOSFET Drain-to-Source blocking voltage, and, V_{bd} the MOSFET breakdown voltage. In this context, it is assumed that the V_{bd} value is 1151 V for the selected 650 V rated SiC MOSFET according to the experimentally tested breakdown voltage results in [114].
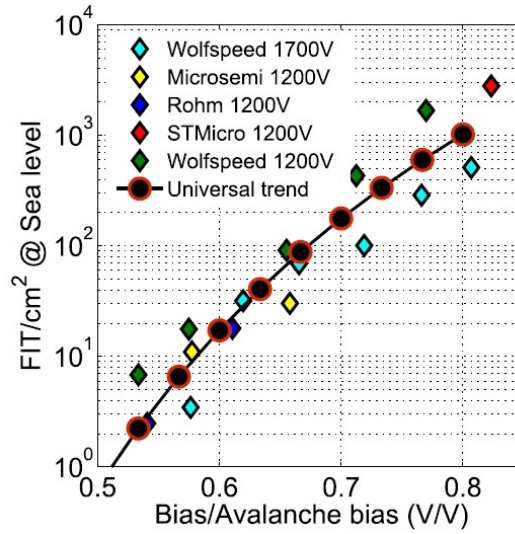

Figure 3.7 FIT/cm^2 universal curve [113].

Afterwards, considering that the neutron flux intensity at 30,000 ft (mission profile cruise altitude) is higher than at sea level conditions, i.e., the universal curve conditions, the FIT/cm^2 value is scaled using the altitude factor in [115, 116]. Thus,

$$\lambda_h = \lambda_0 \cdot exp\left(\frac{1 - \left(1 - \dfrac{h}{44300}\right)^{5.26}}{0.143}\right) \tag{3.7}$$

where λ_0 refers to the FIT/cm^2 value obtained in the universal curve at sea level (see Table 3.2), and, λ_h the estimated value at cruising altitude, h.

Table 3.2 Sea level FIT/cm^2 rates from the universal curve considering a semiconductor breakdown voltage of $V_{bd} = 1151$ V.

Configuration	V_{DS}	λ_0	λ_h
2L$_C$ & 2L$_{st}$	270 V	$3.38 \cdot 10^{-5}$ FIT	0.0046 FIT
2L$_2$	312 V	$1.74 \cdot 10^{-4}$ FIT	0.0239 FIT
2L$_{st}$	459 V	0.0304 FIT	4.1705 FIT

In order to obtain the power device FIT value, λ_h is multiplied by the power device chip area. However, since the same power device is assumed in all of the configurations, the FIT/cm^2 can be employed for comparison purposes. Additionally, the calculated FIT/cm^2 rates are valid for a semiconductor during blocking mode. Therefore, a scaling factor should be applied that corresponds to the percentage of the time spent in blocking mode of the power device [99]. Thus,

- a 50 % for the power devices of the AC/DC stage.
- A 13.5 % and 86.5 % for the upper and downer power devices in the DC/DC stage of 2L$_2$ converter, respectively, according to a duty cycle of 0.865 in "*buck-mode*".

Once the FIT/cm^2 value of each power device is calculated and scaled, λ'_h, the FIT value for the whole architecture, λ_{arch}, is obtained summing up the scaled FIT values of all the devices in the architecture:

$$\lambda_{\text{arch}} = \sum \lambda'_h \ . \tag{3.8}$$

Wear-Out Performance Analysis

Caused by the cyclic power losses, thermal cycling is identified as the most important stressor that affects the reliability of power devices in terms of wear-out failure [94, 109]. Moreover, since the thermal stress depends on the power device mission profile, previously described in Table 3.1, a mission profile-based reliability evaluation is applied in this research work [94, 99, 109].

Based on the calculations of P_{cond} and P_{sw} described in Chapter 2.4 for the defined mission profile and as a consequence of the employed electrothermal model in Figure 3.3, the average T_{j} of the different power devices is determined. Thus, in order to determine the number of kilocycles to failure of a power device due to thermal cycling, N_{f}, a lifetime model is used, which is presented in [109, 110] for MOSFET power devices, based on the Coffin–Manson Law. The employed lifetime model, already used in literature for the evaluation of SiC MOSFET lifetimes in [117–119] is expressed as,

$$N_{\text{f}} = \alpha \cdot (\Delta T_{\text{j−amb}})^{-\beta} \tag{3.9}$$

where $\Delta T_{\text{j−amb}}$ represents the temperature rise from ambient to junction, and, α and β are fitting parameters defined as $5 \cdot 10^{11}$ and 5.3 in [110], respectively. Consequently, based on the achieved average T_{j} in a mission, the number of cycles, i.e. missions, that a power device can experience before suffering a wear-out failure is calculated.

Note, however, that the obtained result in (3.9) concludes a fixed value for the number of cycles to failure. If this was true, this calculation would ideally suppose the exact failure in time of the power devices that were operating at the same conditions, and hence, experienced ideally the same thermal stress. Nevertheless, there are some uncertainties in the performed analysis that should be considered, such as [94, 99, 109]:

- The MOSFET lifetime model and the fitting parameters employed derived from testing data in [110] which might not exactly represent the lifetime model of the selected power device and, hence, the number of cycles to failure N_{f};

- The thermal and electrical parameters of the power devices, which could vary due to the manufacturing process resulting in unequal power loss distribution and, thus, unequal $\Delta T_{\text{j-amb}}$ among the devices; or,

- The simplified mission profile, which could vary with the flight time, the climate change and load conditions and, hence, result in a different achieved $\Delta T_{\text{j-amb}}$ for a power device per mission.

As a consequence of the existing uncertainties, a sensitivity analysis is also performed by means of a Monte Carlo simulation, so that the reliability can be expressed in statistical values rather than fixed (see Figure 3.8).
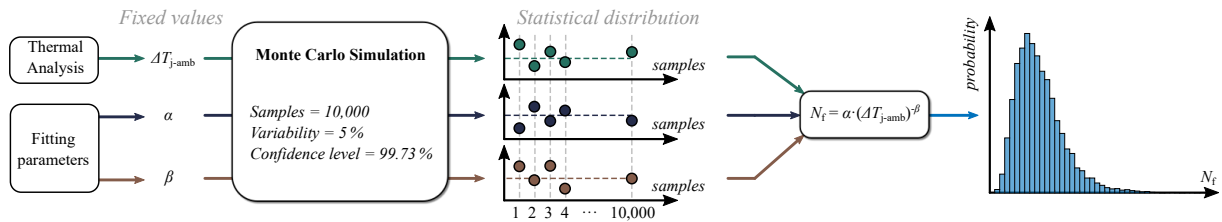

Figure 3.8 Example of Monte Carlo simulation results for N_f, considering the variation for $\Delta T_{\text{j-amb}}$, α and β from which a probability density function (pdf) is obtained.

The Monte Carlo simulation method is typically employed for modeling a phenomenon with significant degrees of uncertainty. Thus, this simulation method is based on randomly varying certain inputs, i.e. for the presented lifetime model α, β and $\Delta T_{\text{j-amb}}$, in order to evaluate their effect on the output of the lifetime model, that is N_f. This way, as presented in Figure 3.8, considering a 5% variability of the uncertain inputs and 10^5 population samples (i.e. missions) according to [109], the Monte Carlo simulation is used to provide a statistical measure of the cycles to failure Nf of a power device. Thus, a probability density function (pdf) of N_f can be obtained.

Afterwards a "*lognormal*" distribution fitting is applied and the cumulative distribution function (cdf) of each device, $F_{\text{dev}}(t)$ is extracted. The cfd represents the integral function of the pdf and, therefore, the unreliability of the device for a number of cycles performed. Thus, considering a series connected reliability model in which any device failure leads to the failure of the architecture, the architecture cdf, $F_{\text{arch}}(t)$, is calculated as,

$$F_{\text{conv}}(t) = 1 - \prod \left(1 - F_{\text{dev}}(t)\right) \tag{3.10}$$

$$F_{\text{arch}}(t) = 1 - \prod \left(1 - F_{\text{conv}}(t)\right) \tag{3.11}$$

where $F_{\text{conv}}(t)$ represents the converter cdf. Examples of the architecture, converter, and device cdf are presented in Figure 3.9(a). In order to acquire a high reliability indicator for the comparison [94, 102], the B_1 cycle to failure parameter is extracted from the resulting architecture unreliability curve, $F_{\text{arch}}(t)$. This parameter represents the number of repeat mission profiles after which the architecture survives at 99%, which, after applying the mission profile data (cycles per year), can be estimated in a period of years (see Figure 3.9(b)).
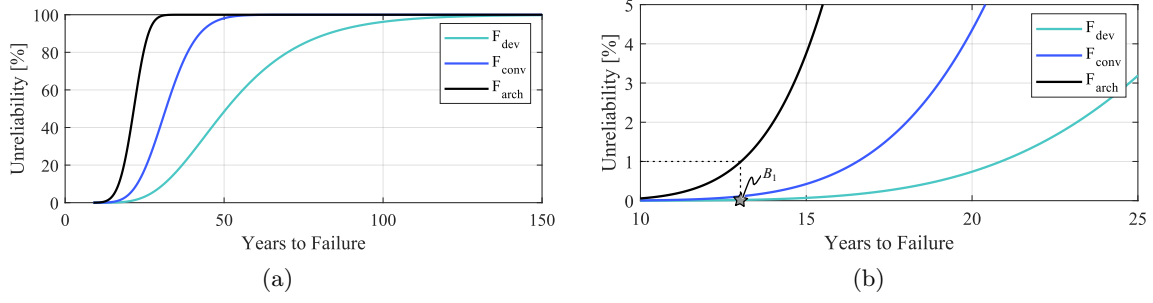
Figure 3.9 (a) Unreliability curves for an architecture formed by identical converters based on a single device type, and, (b) zoomed curves where the B_1 parameter is presented.

3.3 Converter Configuration and Architecture Design

Aiming to design the architectures related to $2L_2$, $2L_C$, and $2L_{st}$ converter configurations, the following concepts are considered:

- The presented architectures are designed to fulfil the efficiency targets and operating requirements in Table 2.1 as well as the power quality and harmonic requirements, both LF and High Frequency (HF), in DO-160G [62]. The LF and HF harmonic requirements are represented in Table 3.3 and Figure 3.10, respectively.

Table 3.3 Current harmonic limits for balanced three-phase electrical equipment.

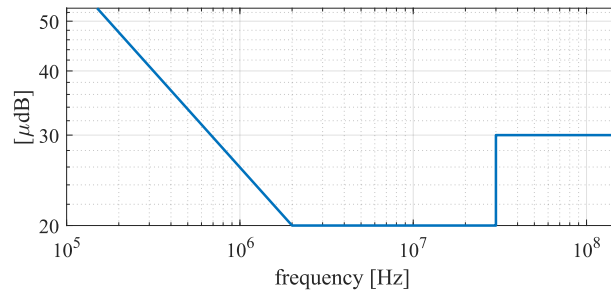| Harmonic Order	Limits
3rd, 5th, 7th	$i_3 = i_5 = i_7 = 0.02 \cdot i_1$
Odd triplen harmonics ($h = 9,\, 15\, 21, ..., 39$)	$i_h = 0.1 \cdot i_1/h$
11th	$i_{11} = 0.1 \cdot i_1$
13th	$i_{13} = 0.08 \cdot i_1$
Odd non-triplen harmonics 17, 19	$i_{17} = i_{19} = 0.04 \cdot i_1$
Odd non-triplen harmonics 23, 25	$i_{23} = i_{25} = 0.03 \cdot i_1$
Odd non-triplen harmonics 29, 31, 35, 37	$i_h = 0.3 \cdot i_1/h$
Even harmonics 2 and 4	$i_h = 0.01 \cdot i_1/h$
Even harmonics > 4 ($h = 6,\, 8\, 10 ... 40$)	$i_h = 0.0025 \cdot i_1$

Figure 3.10 Maximum level of conducted radio-frequency interference.

- The operating PF of the power converters is analyzed by the equation describing the phase

diagrams in Chapter 2 (Figure 2.15), being,

$$V_{\text{conv}}^2 = (V_{\text{ph}} - V_{\text{L}} \cdot \sin(\varphi))^2 + (V_{\text{L}} \cdot \cos(\varphi))^2 \tag{3.12}$$

where $\cos(\varphi)$ refers tot he operating PF and, V_{L} symbolizes the inductor RMS voltage, which can be expressed as,

$$V_{\text{L}} = 2\pi f L i_{\text{L}} = 2\pi f L \cdot \frac{P_{\text{conv}}}{3 \cdot V_{\text{ph}} \cos(\varphi)} \tag{3.13}$$

being, f the SG frequency in Table 2.1, i_{L} the RMS current flowing through the input filter inductor, and, P_{conv} the converter nominal power, that is $18.75\,\text{kW}$.

It is worth to mention that, in the case of 2L_{C} and 2L_{st} single-stage configurations (PF < 1), the higher the operating PF, the lower the reactive power to be compensated and, hence, higher efficiency. If (2.4) and (3.12) are merged, the maximum operating PF of these topologies can be obtained depending on V_{L} for a fixed m,

$$\cos(\varphi) = \sqrt{1 - \left(\frac{V_{\text{ph}}^2 + V_{\text{L}}^2 - \left(\frac{m \cdot V_{\text{DC}}}{2\sqrt{2}}\right)^2}{2 V_{\text{ph}} V_{\text{L}}}\right)^2} \tag{3.14}$$

A graphical representation of (3.14) is depicted in Figure 3.11 where the maximum operating PF is represented in a black dashed line for $m = 1.13$.
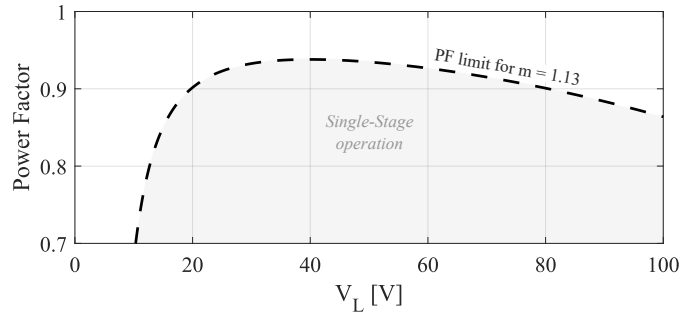

Figure 3.11 Operating PF limit of a single-stage converter.

- SVPWM pattern is assumed and a maximum $m = 1.13$ to ensure the minimum conduction and blocking times of the employed semiconductor as in the preceding chapter.

- From the previous chapter, a $f_{\text{sw}} \approx 80 - 100\,\text{kHz}$ is targeted for the AC/DC power converters aiming to achieve a relatively low filtering effort. Similarly, a $f_{\text{sw}} \approx 75\,\text{kHz}$ is targeted for the DC/DC power stage of the 2L_2 converter. The possibility of achieving these switching frequency values at an expected nominal power of $18.75\,\text{kW}$ is analyzed by means of a thermal analysis based on the simplified converter models in Chapter 2.4 and a steady-state thermal model described in Figure 3.3. This way, the converter $f_{\text{sw,max}}$ is obtained depending on the transmitted P_{conv} while maintaining an efficiency result of $\geq 97\,\%$. The fact of considering the steady-state thermal model during the analysis, prevents from exceeding the maximum permissible T_{j} value of the employed semiconductors

and, hence, a converter burn-out. Thus, the maximum permissible temperature increase from ambient-to-junction can be defined as,

$$\Delta T_{\mathrm{j-amb}} = (T_{\mathrm{j-max}} - 15\,^{\circ}C) - T_{\mathrm{amb}} = 185\,^{\circ}C - 70\,^{\circ}C = 115\,^{\circ}C \ . \tag{3.15}$$

- Due to restrictive harmonic limitations imposed, a Differential Mode (DM) LCL filter is considered for this application [62, 120] where the grid-side inductance corresponds to an assumed SG synchronous inductance of $L_{\mathrm{SG}} = 93.5\,\mu\mathrm{H}$, calculated as in [121],

$$Z_{\mathrm{SG}} = 3 \cdot \frac{V_{\mathrm{ph}}^2}{S} \tag{3.16}$$

$$L_{\mathrm{SG}} = \frac{Z_{\mathrm{SG}}}{2\pi f} \tag{3.17}$$

where Z_{SG} represents the synchronous impedance of the SG, S represents the apparent power of the SG deduced for a 0.8 PF and f the SG frequency. Since the SG inductance forms part of the LCL filter, an LC filter is assumed for each power converter configuration.

The power quality ($\mathrm{THD_i} \leq 3\,\%$) and HF harmonic requirements must be fulfilled at the Point Of Regulation (POR), i.e. the point where the active modular architecture is connected to the SG. This concept is represented in Figure 3.12(a), where a considered number of synchronized converters, N_{conv}, are connected to the POR. Due to the N_{conv} converter parallelization, the filter inductance and capacitance for the ideal LCL filter of the overall architecture are defined as L/N_{conv} and $C \cdot N_{\mathrm{conv}}$, respectively. Thus, based on the transfer function of the equivalent single-phase LCL filter in [122], the transfer function of the architecture LCL filter is defined as,

$$H(s) = \frac{i_{SG}}{V_{conv}} = \frac{1}{s^3 \frac{L}{N_{conv}} C N_{conv} L_{SG} + s\left(\frac{L}{N_{conv}} + L_{SG}\right)} =$$

$$= \frac{1}{s^3 L C L_{SG} + s\left(\frac{L}{N_{conv}} + L_{SG}\right)} \ . \tag{3.18}$$
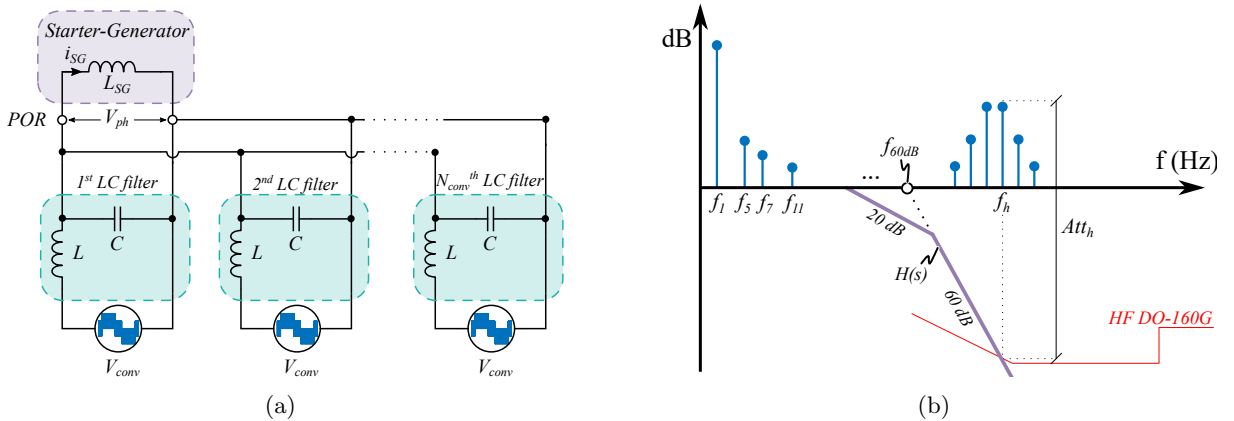

Figure 3.12 (a) Simplified single-phase architecture equivalent circuit for the HF harmonic filtering analysis, and, (b) graphical example of the transfer function $H(s)$.

Special attention should be paid to the third order filter term in (3.18), which presents a 60 dB/decade asymptote as illustrated in the Figure 3.12(b) example, since its cut-off frequency is determined by the term "LCL_{SG}". Therefore, independent of the number of converters connected to the POR, the cut-off frequency of 60 dB/decade asymptote is maintained constant. This fact provides the possibility of defining the input filter capacitor for HF harmonics filtering without considering N_{conv}.

According to the third order term, the capacitor value which defines the filter 60 dB/decade asymptote is given by,

$$C = \frac{1}{(2\pi f_{\text{60dB}})^3 \cdot LL_{\text{SG}}} \tag{3.19}$$

where f_{60dB} is the cut-off frequency of the 60 dB/decade asymptote and is defined as,

$$Att_{\text{h}} = 60 \cdot \log\left(\frac{f_{\text{h}}}{f_{\text{60dB}}}\right) \tag{3.20}$$

$$f_{\text{60dB}} = \frac{f_{\text{h}}}{10^{\left(\frac{Att_{\text{h}}}{60}\right)}} \quad . \tag{3.21}$$

Note that this cut-off frequency is defined for a required attenuation, Att_{h}, at a frequency f_{h} for the hth frequency harmonic (see Figure 3.12(b)). This required attenuation is, indeed, defined by the fraction between $V_{\text{conv}-\text{h}}$ voltage waveform component and the conducted emissions current harmonic limit, i_{h}, at the hth harmonic for category M equipment in DO-160G [62, 87, 123]. In other words, the input filter impedance at the frequency f_{h}. Thus,

$$Att_{\text{h}} = 20 \cdot \log\frac{V_{\text{conv}-\text{h}}}{i_{\text{h}}} + 6\,dB \quad . \tag{3.22}$$

where the additional 6 dB correspond to the safety margin defined in DO-160G [62,87,123].

- The DC-link capacitor, C_{link}, of the three configurations is defined for a specific peak-to-peak switching voltage ripple, ΔV_{DC}, according to [124]. Hence,

$$C_{link} = \frac{\hat{i}_{\text{L}}}{4\,f_{\text{sw}} \cdot \Delta V_{\text{DC}}} \quad . \tag{3.23}$$

where f_{sw} represents the power converter switching frequency and $\hat{i}_{\text{L}}$ the peak current flowing through the converter input filter inductance, L. Note that, according to aviation standards [29,62], ΔV_{DC} is defined as 2.22 %·V_{DC}.

3.3.1 Two-Stage Configuration-Based Archictecture - 2L$_2$

A simplified example of the considered 2L$_2$ architecture is presented in Figure 3.13. This architecture is based in the two-stage configuration and contains a relatively small input filter for fulfilling harmonic requirements.

Since the 2L$_2$ configuration is ideally operating at unity PF, the rectifier output voltage V_{DC}, which is the middle DC bus voltage between AC/DC and DC/DC stages, plays a critical role in the converter design. As defined in Chapter 2.4.2 in higher detail, a middle DC bus voltage

value of $312\,\mathrm{V}$ is calculated aiming a reduced amount of switching losses and, thus, design a high-efficient $2L_2$ converter. According to [101], this middle DC bus voltage is then reduced to the targeted $270\,\mathrm{V_{DC}}$ by a buck converter D_{buck} of 0.865 using (2.25).
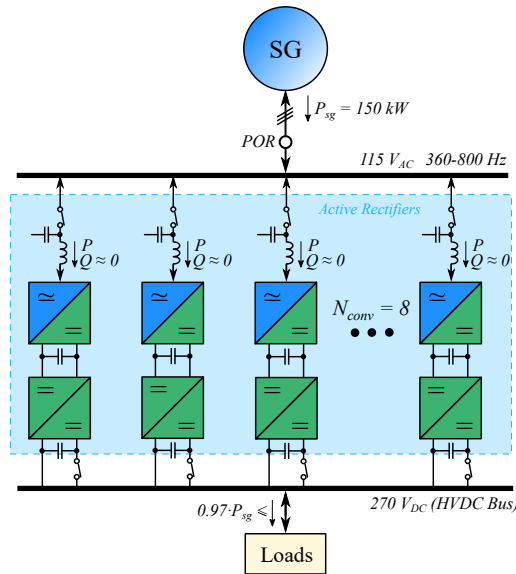

Figure 3.13 Simplified schema of the proposed active modular $2L_2$ architecture structure.

With the input/output voltage operating conditions of both power stages specified, a thermal analysis should be performed in order to verify the high switching frequency capability of the AC/DC ($\approx 80\text{-}100\,\mathrm{kHz}$) and the DC/DC ($\approx 75\,\mathrm{kHz}$) power stages while achieving a $\geq 97\,\%$ overall converter efficiency. Note that the worst-case operating condition of both power stages should be identified not only for verifying that the efficiency target is fulfilled at any normal operating condition, but also to avoid the converter burn-out due to the semiconductor heating.

In the case of the DC/DC, in which the duty cycle varies according to the DC input and output voltages, it can be assumed that there is only one operating scenario since both input and output voltages are considered as fixed, being $312\,\mathrm{V}$ and $270\,\mathrm{V}$, respectively. Thus, assuming a minimum of $99\,\%$ efficiency for this power stage, a thermal analysis is performed to evaluate the possibility of achieving a $f_{\mathrm{sw}} \approx 75\,\mathrm{kHz}$. The graphical results of the thermal analysis are presented in Figure 3.14.
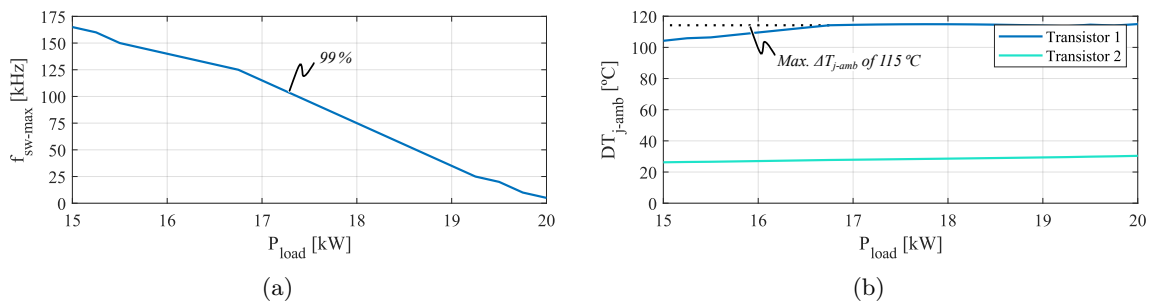

Figure 3.14 Thermal analysis results of the DC/DC power stage ($\eta = 99\,\%$), being (a) the achievable $f_{\mathrm{sw,max}}$ depending on the transmitted power and (b) the $\Delta T_{\mathrm{j-amb}}$ per device.

According to Figure 3.14(a), it is not possible to fulfill the specified efficiency and switching

frequency targets for a transferred nominal power of 18.75 kW. The main reason is that the $\Delta T_{\mathrm{j-amb}}$ of the "*transistor 1*" in Figure 3.2(a) reaches the imposed thermal limit of 115 ℃ and, hence, the converter will operate close to a burn-out condition for a switching frequency higher than 45 kHz. Alternatively, several solutions are proposed and discussed in the following:

(1) Reducing the DC/DC f_{sw}: this possibility implies reducing the P_{sw} of the DC/DC stage. As a result, not only the efficiency of the DC/DC stage is increased, but also the $\Delta T_{\mathrm{j-amb}}$ of the "*transistor 1*" is decreased, which results to be the limiting factor for 18.75 kW nominal power. However, as it has been explained in Chapter 2.5.1 with higher detail, P_{cond} result dominant in this case. Therefore, the fact of reducing the f_{sw} does not cause a substantial impact in the $\Delta T_{\mathrm{j-amb}}$ of the DC/DC stage, while it actually has it in terms of increasing the size of the passive elements (see Figure 3.15). In fact, reducing the limiting 45 kHz f_{sw} to the half results in a $\Delta T_{\mathrm{j-amb}}$ decrease of roughly 5 ℃ owing to almost doubling the value of the passive elements and, hence, volume. Consequently, transferring 18.75 kW while operating with low f_{sw} is not considered as a suitable option.
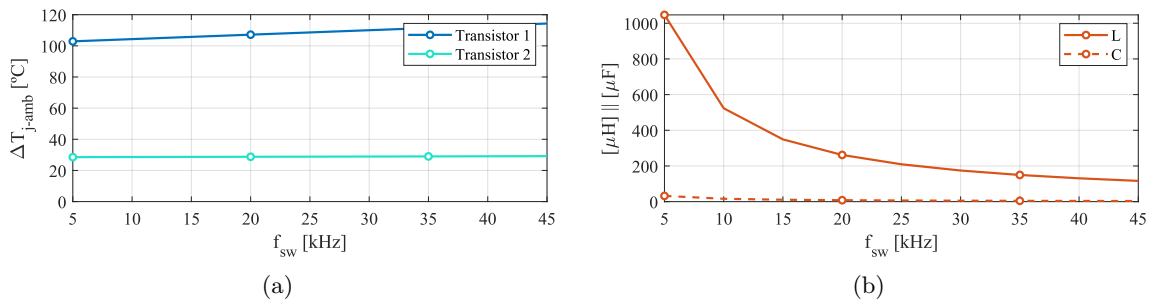

(a) (b)

Figure 3.15 Results of the DC/DC stage when operating at 18.75 kW presenting (a) $\Delta T_{\mathrm{j-amb}}$ of the devices and (b) the value of the passive elements.

(2) Reducing the P_{conv}: A different alternative relies on reducing the converter nominal power to, for example, 15 kW. According to Figure 3.14, the targeted f_{sw} of 75 kHz could be reached if P_{conv} is reduced to 15 kW (a maximum of ≈ 160 kHz is achievable, indeed), although the N_{conv} will be increased to 10. Therefore, the number of power devices, N_{dev}, of the overall architecture, considering both AC/DC and DC/DC stages, is increased with this alternative from $(6 + 2) \cdot 8 = 64$ to $(6 + 2) \cdot 10 = 80$. Advantageously, as presented in Figure 3.16, the efficiency of the DC/DC is increased to 99.2 % and, besides, the $\Delta T_{\mathrm{j-amb}}$ is reduced by 20 ℃, which provides certain margin with respect to the 115 ℃ limit.
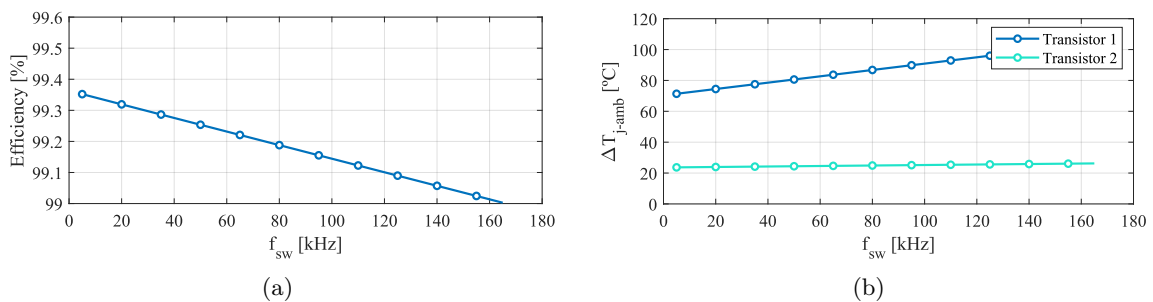

(a) (b)

Figure 3.16 Results of the DC/DC stage when operating at 15 kW (a) efficiency and (b) the $\Delta T_{\mathrm{j-amb}}$ per device.

(3) Implementing 2 parallel phase-legs: since the P_{cond} are dominant for the selected
operating scenario, paralleling semiconductors as in Figure 3.17 becomes a potential solu-
tion. Particularly, the P_{cond} present a quadratic relation to the current flowing through
the MOSFET. Thereby, the implementation of two paralleled phase-legs, which supposes
halving the current per semiconductor, causes a reduction of the conduction losses by a
factor of four. The results of a thermal analysis considering this possibility is presented in
Figure 3.18. As a result, a 99.4 % efficiency of the DC/DC power stage can be achieved at
the initially targeted f_{sw} of 75 kHz and, additionally, the $\Delta T_{\text{j−amb}}$ is reduced to $\approx 45\,^{\circ}$C.
On the negative side, even if N_{conv} is not increased, N_{dev} rises from 64, when considering
the 8 AC/DC and single-leg DC/DC converters, to 80 due to the doubled number of power
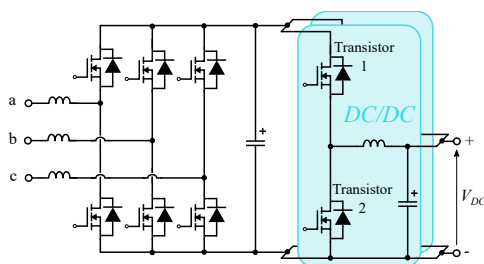devices in the DC/DC stage.

Figure 3.17 Schematics of the two-stage 2L$_2$ converter configuration with paralleled DC/DC.

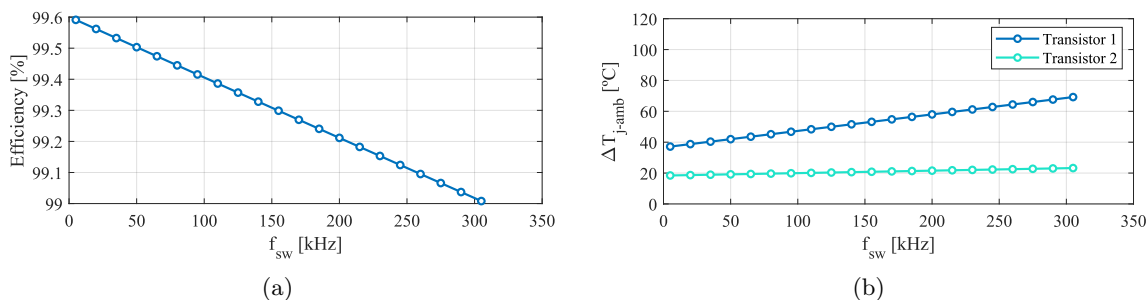(a)   (b)

Figure 3.18 Results of the paralleled DC/DC stage when operating at 18.75kW presenting (a) efficiency and (b)
the $\Delta T_{\text{j−amb}}$ per device

From the proposed alternatives, *solution 2* (reducing the nominal power to 15 kW) and
solution 3 (paralleling the DC/DC phase-leg while maintaining a nominal power of 18.75 kW)
present the same outcome in terms of number of semiconductors. Nevertheless, the former option
presents a 0.2 % lower efficiency and almost the double thermal stress, which is translated into a
shorter lifetime of the component in terms of wear-out failure probability. Therefore, paralleling
the DC/DC stage is considered as a higher potential option for the 2L$_2$ converter. It is worth
to mention that this solution might involve a higher implementation effort due to the fact of
paralleling power devices. This concept, though, will not be treated in this research work.
Neither will be treated other concepts related to paralleling power devices such as interleaving
operation.

Following the analysis of the DC/DC stage, the high switching frequency capability of the
AC/DC stage should be analyzed which, in this case, is targeted to be 80-100 kHz for achieving a

reduced filtering effort. Note that, since the overall converter efficiency is targeted as $\geq 97\%$ and the DC/DC stage supposes a 99.45%, a minimum efficiency value of 97.54% must be obtained in the AC/DC power stage at the worst-case operating condition.

In this regard, Table 3.4 presents a simplified analysis of the operating conditions of the AC/DC stage assuming the input voltage range variation of the application requirements in DO-160G, i.e. from $100\,V_{AC}$ to $122\,V_{AC}$, being $115\,V_{AC}$ the nominal case. Thus, using (2.16) the RMS phase current is calculated for each input voltage condition assuming unity PF operation and a nominal power of $18.75\,kW$. As a result, it is concluded that the worst-case operating condition occurs when $V_{ph} = 100\,V$ and the phase current achieves the highest value of $62.5\,A$.

Table 3.4 Case studies for identifying the worst-case operating condition for the AC/DC stage of $2L_2$ converter.

Case	V_{ph}	i_{ph}	Notes
1	$100\,V$	62.5	"Worst-case operation". Maximum $i_{ph} \rightarrow$ Maximum losses.
2	$115\,V$	54.35	Nominal conditions .
3	$122\,V$	51.22	"V_{DC} calculation case".

Based on *case 1* in Table 3.4, the results of the AC/DC thermal analysis are graphically depicted in Figure 3.19. Concretely, the maximum switching frequency that the AC/DC power stage can reach while maintaining an AC/DC stage efficiency of over 97.54% is found to be $\approx 95\,kHz$. This maximum switching frequency value, however, indicates a first approach value due to the fact that unity PF operation has been assumed.
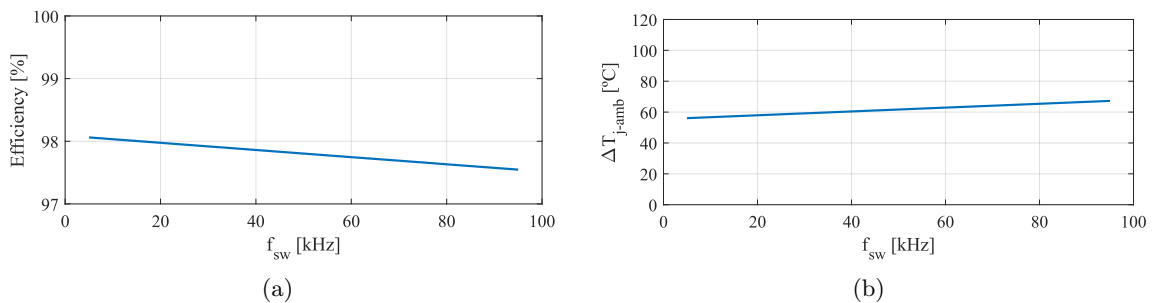

(a)

(b)

Figure 3.19 Thermal analysis results of the AC/DC power stage in which (a) presents the efficiency results, and (b) presents the temperature jump from junction to ambient for the employed power device.

Considering that the AC/DC stage has a LC input filter for fulfilling the harmonic requirements, the actual operating PF will slightly decrease and not be unity due to the reactive current delivered by the input filter capacitor. Consequently, a switching frequency of $80\,kHz$ is defined for the AC/DC power stage aiming to ensure the fulfillment of the efficiency target. Furthermore, according to the previously defined converter operating conditions for the middle DC bus voltage calculation ($V_{ph} = 122\,V$, $V_L = 20\%\cdot V_{ph}$ and $f = 800\,Hz$), the maximum value for the input filter inductor can be defined by reshaping (3.13) as,

$$L_{max} \leq \frac{V_L}{2\pi f i_L} = \frac{0.2 \cdot V_{ph}}{2\pi f \cdot \dfrac{P_{conv}}{3 \cdot V_{ph} \cdot \cos(\varphi)}} = \frac{0.3 \cdot V_{ph}^2}{\pi f P_{conv}} \quad . \tag{3.24}$$

In this regard, with the AC/DC stage f_{sw} defined and aiming for a compact input filter design, a sweep analysis based on the current ripple, Δi_L is performed to define both the input filter inductor, L, and capacitor, C. According to [125], the relation between L and Δi_L can be defined as,

$$L = \frac{V_{DC}}{6 \cdot f_{sw} \cdot \Delta i_L} \quad . \tag{3.25}$$

Consequently, the filter C is designed for each L value (and hence, Δi_L) in order to fulfill DO-160G harmonic requirements (see Figure 3.20(a)). If this design concept is translated to the stored energy by both passive components (using (3.5) and (3.6)), the minimum volume input filter design can be achieved. Thus, the ripple sweep analysis results related to the stored energy, depicted in Figure 3.20(b), reveal that the minimum stored energy in the input filter is achieved when a 9 % current ripple is targeted assuming nominal operating conditions, i.e. $V_{ph}= 115$ V, $f_{sw}= 80$ kHz and $P_{conv}= 18.75$ kW. Note that no lower current ripple value is presented in the analysis because the calculated maximum L of 94.75 μH in (3.24) is exceeded. The DM filtering results for the designed input filter are presented in Figure 3.21, and the electrothermal analysis results are summarized in Table 3.5. Aiming to represent the filtering results in terms of power quality, the SG current THD_i is also included in the table.
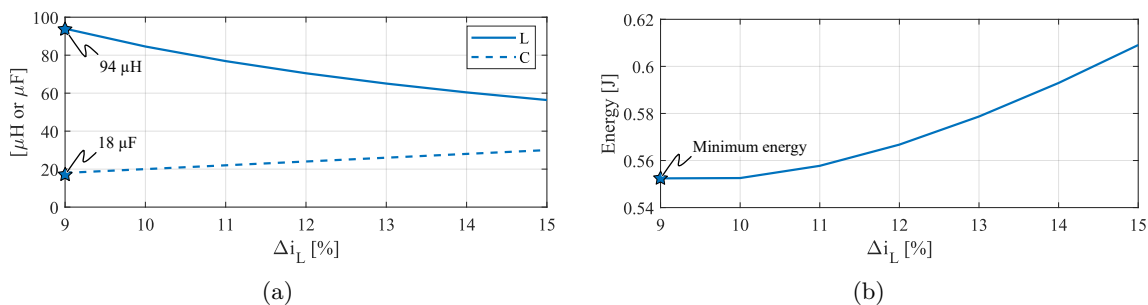

Figure 3.20 Current ripple sweep analysis results presenting (a) the value of the input filter element for fulfilling the LF and HF harmonic requirements, and (b) the stored energy in the passive elements.
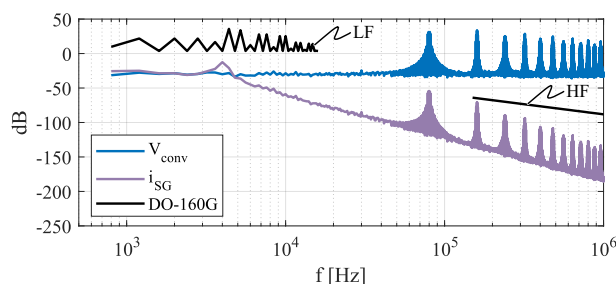

Figure 3.21 DM input filter results of 2L$_2$ architecture for fulfilling LF and HF requirements.

Table 3.5 Summary of the design parameters of $2L_2$, $2L_C$, and, $2L_{st}$ architectures.

	$2L_2$	$2L_C$	$2L_{st}$
Converter Nominal Power, P	18.75 kW	15 kW	18.75 kW
N° of SiC MOSFET, N_{dev}	10	6	6
N° of Converters, N_{conv}	8	10	$8+3$
AC/DC Switching Frequency, f_{sw}	80 kHz	100 kHz	80 kHz
SG Current Distortion, THD_i	0.05 %	0.03 %	0.13 %
SG Inductance, L_{SG}	93.5 μH	93.5 μH	93.5 μH
Input Filter Inductance, L	94 μH	233.32 μH	191.4 μH
Input Filter Capacitance, C	18 μF	69.94 μF	19 μF
DC bus Capacitance, C_{link}	44.73 μF	40.2 μF	52.18 μF
AC/DC Stage Output Voltage, V_{DC}	312 V	270 V	270 V & 459 V
DC/DC Stage Output Voltage, V'_{DC}	270 V	-	-
DC/DC Switching Frequency, f_{sw}	75 kHz	-	-
DC/DC Inductance, L_{dc}	139.6 μH	-	-
DC/DC Capacitance, C_{dc}	1.07 μF	-	-
Max. ΔT_{j-amb}	55.13 °C	61.55 °C	58.73 °C
Heatsink Thermal Resistance, R_{h-amb}	0.027 °C/W	0.034 °C/W	0.032 °C/W

3.3.2 Single-Stage with Capacitor Configuration-Based Architecture - $2L_C$

Contrary to the two-stage configuration case, the $2L_C$ architecture benefits from a simplified single-stage architecture structure, as presented in Figure 3.22. Simply put, the power converters employed in this architecture operate at a PF lower than unity which, in order to achieve unity PF at the POR, is then corrected by means of the input filter capacitor bank.
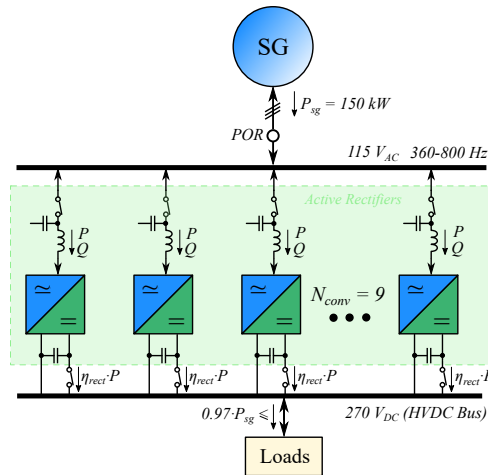
Figure 3.22 Simplified schema of the proposed active modular $2L_C$ architecture structure.

Regarding the power converter performance, the higher the operating PF, the lower the reactive power to be compensated by the input filter capacitor banks, and hence, higher efficiency. Thus, based on (3.14) and considering the highest achievable efficiency as the design criterion, the maximum PF point of the curve is selected as the Design Point (DP_{PF}) of the power converters, that is 0.938 when $V_L = 39.87$ V as presented in Figure 3.23 below.
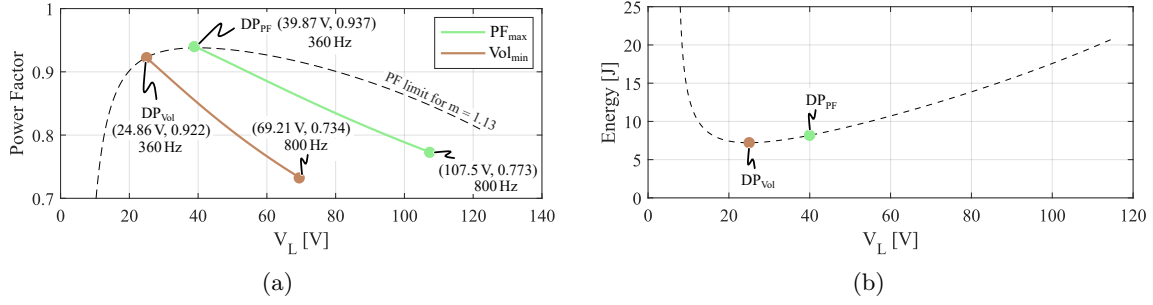
Figure 3.23 (a) 2L$_\text{C}$ configuration PF operating curves based on "*maximum PF*" and "*minimum volume*" design points, and (b) total stored energy in the passive elements of the input filter related to the PF limit curve.

With the design point selected, defining the passive elements for the input filter becomes the next task. In this case, aiming to provide reactive power compensation by means of the input filter throughout the whole frequency range, i.e. from 360 Hz to 800 Hz, the design point should also be the minimum reactive power demand operating point. In this context, special attention should be paid to the input filter capacitor, C, whose delivered current is defined as,

$$i_\text{C} = \frac{V_\text{ph}}{X_C} = 2\pi f C \cdot V_\text{ph} \ .$$ (3.26)

From (3.28), it is concluded that the higher the frequency, the higher amount of capacitive current delivered (assuming fixed C and V_ph values). Since this capacitive current is, indeed, the reactive current used for PF compensation, a SG frequency of 360 Hz must be assumed at the design point.

Therefore, all the required data are known for designing the input filter inductor, L, and the input filter capacitor, C. Based on the design point data (V_L= 39.87 V, $\cos(\varphi)$ = 0.938, V_ph= 115 V and f= 360 Hz), equation (3.13) is rearranged for calculating L as,

$$L = \frac{3 \cdot V_\text{L} V_\text{ph} \cos(\varphi)}{2\pi f P_\text{conv}} \ .$$ (3.27)

Similarly, (3.28) is rearranged for calculating the required capacitor value for reactive power compensation as,

$$C = \frac{i_\text{C}}{2\pi f \cdot V_\text{ph}} = \frac{i_\text{L} \cdot \sin(\varphi)}{2\pi f \cdot V_\text{ph}} = \frac{P_\text{conv} \cdot \tan(\varphi)}{6\pi f \cdot V_\text{ph}^2} \ .$$ (3.28)

Thus, both L and C can be calculated depending on P_conv and the selected design point data in the "*PF - V$_L$ limit curve*" represented in Figure 3.23(a).

At this point, it should be taken into account that, unlike to the previous 2L$_2$ input filter design case in which the minimum volume components are calculated for HF harmonic fulfill-ment, in the 2L$_\text{C}$ design, L and C are defined according to the PF - V$_\text{L}$ limit curve for achieving single-stage converter operation and unity PF operation at the POR. Nevertheless, using (3.27) and (3.28) and assuming the 150 kW architecture nominal power, the PF - V$_\text{L}$ limit curve can be translated into a "*E - V$_L$ limit curve*" by applying (3.5) and (3.6). As a result, the E - V$_\text{L}$ limit

curve is depicted in Figure 3.23(b), in which the minimum total stored energy in the passive elements is achieved when $V_L = 24.86\,V$. This point, hence, represents the minimum input filter volume design point (DP$_{Vol}$) and, hence, considered as an additional design criterion. Note that this point is also reflected in Figure 3.23(a), being the point $(V_L, PF) = (24.86\,V, 0.922)$.

Therefore, considering both design criteria, the fact that 2L$_C$ converters can fulfill the efficiency target at the worst-case operating condition must be verified. In this regard, analyzing the converter operating behavior depending on the design point selected, that is the operating PF of the 2L$_C$ converter, becomes a priority.

If V_{ph} is aligned with the d axis in the d-q rotational frame (thus, $\hat{V}_{ph} = V_d$), the RMS inductor current can be divided into i_d and i_q representing the active power RMS current and the reactive power RMS current flowing through the converter inductor, respectively.

$$i_d = i_L \cdot \cos(\varphi) \;\; , \;\; i_q = i_L \cdot \sin(\varphi) \tag{3.29}$$

Therefore, i_L can also be defined as,

$$i_L = \sqrt{i_d^2 + i_q^2} \;\; . \tag{3.30}$$

Since i_d is associated P_{conv},

$$i_d = \frac{2}{3} \cdot \frac{P_{conv}}{\sqrt{2} \cdot V_d} = \frac{P_{conv}}{3 \cdot V_{ph}} \;\; . \tag{3.31}$$

The reactive current i_q, though, is associated to the delivered capacitor current. Thereby,

$$i_q = i_C = 2\pi f C \cdot V_{ph} \;\; . \tag{3.32}$$

By means of (3.31) and (3.32), the operating PF at the 2L$_C$ converter terminals can be calculated as,

$$PF = \cos\left(\arctan\left(\frac{i_q}{i_d}\right)\right) \;\; . \tag{3.33}$$

As a result of equations (3.13), (3.29) - (3.33), the operating PF curve is represented in Figure 3.23(a) for the operating SG frequency range, i.e. from $V_L = 39.89\,V$ at $360\,Hz$ to $V_L = 107.54\,V$ at $800\,Hz$ in the case of selecting DP$_{PF}$, and from $V_L = 24.86\,V$ at $360\,Hz$ to $V_L = 69.21\,V$ at $800\,Hz$ in the case of selecting DP$_{Vol}$.

Following this lead, the operating PF of 2L$_C$ converters is calculated for the different SG operating voltage scenarios, being $100\,V$, $115\,V$ (nominal conditions) and $122\,V$, based on V_{ph}, f and P_{conv} aiming to identify the converter worst-case operating condition. A graphical representation for each V_{ph} scenario is presented in Figure 3.39(a) and Figure 3.39(b) for DP$_{PF}$ and DP$_{Vol}$, respectively, in which the maximum operating PF limit assuming a maximum modulation index of $m = 1.13$ is depicted in dashed lines.

In addition to presented operating PF curves under different V_{ph} scenarios, the converter i_L value related to these operating PF curves can be calculated. The calculations for both DP$_{PF}$ or DP$_{Vol}$ design are depicted in Figure 3.24(c) and Figure 3.24(d), respectively, depending on

the SG frequency. This way, the worst-case operating condition can be graphically identified as
the maximum current operating point in the figures. Note that, aiming to represent the current
magnitude of each operating scenario, per unit (p.u.) values have been employed normalized to
its respective design point. Thus, 1 p.u. corresponds to the current of the selected $2L_C$ design
point, i.e. i_L @($V_L = 39.87$ V, $\cos(\varphi) = 0.938$, $V_{ph} = 115$ V, $f = 360$ Hz) for DP_{PF}, and, i_L
@($V_L = 24.86$ V, $\cos(\varphi) = 0.922$, $V_{ph} = 115$ V, $f = 360$ Hz) for DP_{Vol}.
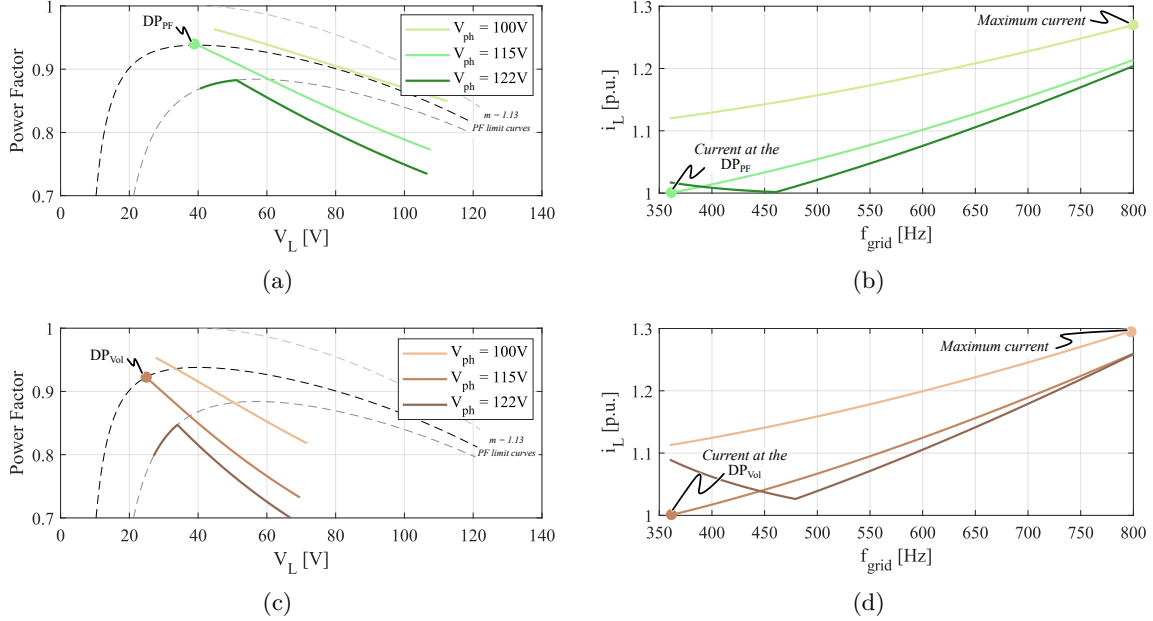

(a)

(b)

(c)

(d)

Figure 3.24 Design conditions of $2L_C$ rectifier for 100 V$_{AC}$, 115 V$_{AC}$ and 122 V$_{AC}$ phase input voltages being
(a) DP_{PF}-based PF operation, (b) the RMS current flowing through the input filter inductor normalized to the
DP_{PF} current, (c) DP_{Vol}-based PF operation, and, (b) the RMS current flowing through the input filter inductor
normalized to the DP_{Vol} current.

From Figure 3.24(c) and Figure 3.24(d), it is observed that the worst-case operating sce-
nario is presented when $V_{ph} = 100$ V$_{AC}$, and $f = 800$ Hz scenario occurs for both cases since
i_L increases approximately by 27% and 30% with respect to DP_{PF} and DP_{Vol} design points,
correspondingly. Consequently, based on these worst-case operating points, a thermal analysis is
performed for each design point criterion aiming to identify the achievable $f_{sw,max}$ depending on
P_{conv} while maintaining the targeted $\geq 97\%$ efficiency. The results of the analysis are presented
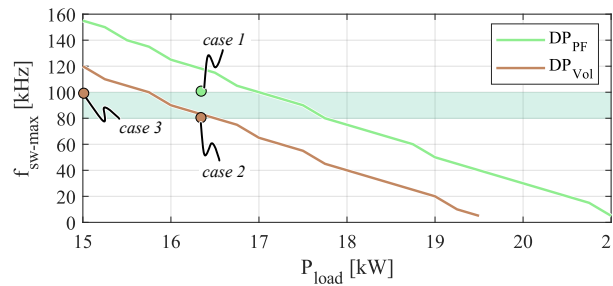in Figure 3.25 below.

Figure 3.25 Worst-case operating condition based thermal analysis results for $2L_C$ converter when targeting the
maximum PF design (DP_{PF}) and the minimum input filter volume design (DP_{Vol}).

As previously mentioned, a converter $f_{\mathrm{sw}} \approx 80 - 100\,\mathrm{kHz}$ is desired in order to achieve a reduced filtering effort. This range of interest has also been colored in green in Figure 3.25 in order to represent the potential converter, and thus architecture, design option. Therefore, it can be concluded that for the selected semiconductor no design possibility emerges for the expected 18.75 kW nominal converter power design. However, three suitable case studies are found relatively close to the thermal limit in the figure which, owing to a higher number of converters, fulfill the efficiency target at the desired switching frequency range. The selected case studies, identified in the figure as "*case 1*", "*case 2*" and "*case 3*", are summarized in Table 3.6. Note that, even if a fourth DP$_{\mathrm{PF}}$-based case could also be considered assuming a 15 kW nominal and 100 kHz switching frequency, the maximum achievable switching frequency for this case study reaches 150 kHz. Thus, for the selected semiconductor the converter design will be excessively oversized and, hence, is not considered as an interesting solution.

Table 3.6 Potential case studies for the 2L$_{\mathrm{C}}$ architecture design obtained from the thermal analysis.

Case	Design Point	P_{cond} [kW]	f_{sw} [kHz]	L [μH]	C [μF]	C_{link} [μF]	N_{conv}
1	DP$_{\mathrm{PF}}$	16.33	100	342.25	68.63	44.5	9
2	DP$_{\mathrm{Vol}}$	16.33	80	209.87	77.7	55.7	9
3	DP$_{\mathrm{Vol}}$	15	100	233.32	69.94	40.2	10

Aiming to select the most suitable design for the 2L$_{\mathrm{C}}$ converter among the three case studies, the influence of the selected design point criterion is analyzed at architecture level. In this context, DP$_{\mathrm{Vol}}$-based designs are expected to benefit from a lower architecture volume. Similarly, the DP$_{\mathrm{PF}}$-based design should be advantageous in terms of efficiency because of the increased operating PF at nominal conditions and, hence, a lower amount of power losses and a subsequent lower temperature increase could be expected.

Aiming to present relevant comparative results among the three case studies, Figure 3.26 presents the normalized results of the overall stored energy in each case study architecture, E_{arch}, and the normalized average $\Delta T_{\mathrm{j-amb}}$ achieved of a power device operating at each architecture. E_{arch} has been calculated using (3.5) and (3.6) for the passive elements L, C and C_{link} in Table 3.6 (calculated as in (3.23), (3.27) and (3.28)) considering the worst-case current condition previously described, and the maximum voltage for the capacitors, that is $\hat{V}_{\mathrm{ph}} = 122\,\mathrm{V}$ for C and $V_{\mathrm{DC}} + \Delta V_{\mathrm{DC}} = 270\,\mathrm{V} + 5.4\,\mathrm{V}$ for C_{link}. As for the calculation of $\Delta T_{\mathrm{j-amb}}$, the TEC described in Figure 3.3 has been employed and the worst-case nominal condition has been assumed, that is $V_{\mathrm{ph}} = 115\,\mathrm{V}$ and $f = 800\,\mathrm{Hz}$.

From the results, a lower E_{arch} is observed in the DP$_{\mathrm{Vol}}$-based designs. Concretely, a 0.12 p.u. or 12 % volume reduction is achieved from *case 1* to *case 3*. It is worth to mention that, in *case 2* and *case 3* almost similar E_{L} and E_{C} is achieved while a significant difference is observed in $E_{\mathrm{C-link}}$. The main reason of this difference arises from the fact higher f_{sw} of the converters in *case 3* and, hence, a lower C_{link} for the same nominal power could be obtained according to (3.23). For its part, the similarity in E_{L} and E_{C} occurs due to the fact that the same design point has been employed for both case studies. Therefore, the fact of paralleling the L and C for all the converters, in either case study, leads to the same result, which is the calculation of (3.27)

and (3.28) assuming the architecture nominal power of $150\,\text{kW}$. Note that a slight difference is found in E_L since the lower the f_sw, the higher the current ripple and, hence, the higher peak current flowing through the inductor for a defined nominal power.
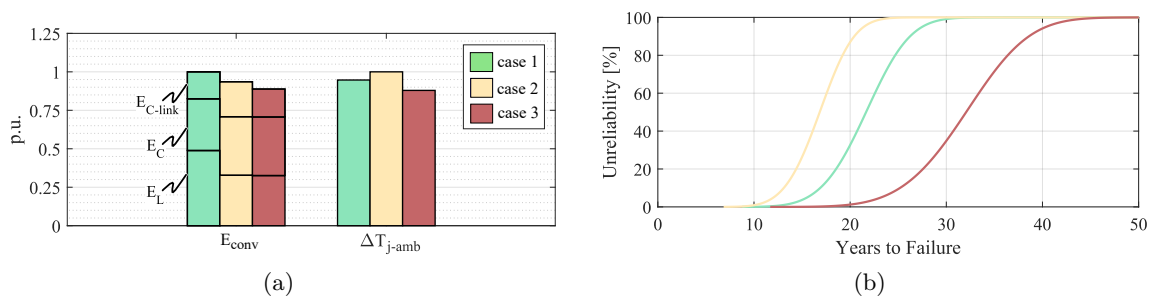

Figure 3.26 Comparative results of the three case studies for 2L_C architecture design presenting (a) the overall architecture volume of the passive elements and the $\Delta T_{\text{j}-\text{amb}}$ of the operating power devices, and (b) the expected unreliability curves of the architectures according to the achieved $\Delta T_{\text{j}-\text{amb}}$.

In relation to the $\Delta T_{\text{j}-\text{amb}}$ of the power devices, even if a higher f_sw is considered for the same converter nominal power, *case 1* results advantageous over *case 2* because of the higher operating PF, being PF $= 0.773$ for *case 1* and PF $= 0.734$ for *case 2*. However, the most advantageous solution results to be *case 3* because of the downgrading in the P_conv. The fact that a lower amount current is being conducted by the power devices in *case 3* results not only in a lower $\Delta T_{\text{j}-\text{amb}}$, but also in a longer expected lifetime. Thus, as presented in Figure 3.26, the $15\,\text{kW}$ DP_Vol-based architecture design results in the most reliable 2L_C architecture design for the selected semiconductor. In fact, for a $1\,\%$ of unreliability (B_1), the lifetime of the architecture is approximately doubled with respect to the *case 1* and *case 2* designs.

Consequently, the $15\,\text{kW}$ DP_Vol-based architecture design is considered as the most promising solution among the three case studies because of the lower expected volume and higher reliability. Thus, the design parameters and electrothermal analysis results of the selected 2L_C architecture are calculated for the worst nominal conditions and summarized in Table 3.5. Note that this operating condition occurs when, at nominal operating conditions the input capacitor bank delivers excessive reactive current leading to a reduced operating PF of the power converters, i.e., $P_\text{conv} = 15\,\text{kW}$, $V_\text{ph} = 115\,\text{V}_\text{AC}$, PF $= 0.73$ and $f = 800\,\text{Hz}$.

The inherent large passive element values required for PF correction are translated into an over filtering effort, as presented in Figure 3.27, which allows to reduce the f_sw and increase the converter efficiency. Thus, aiming to squeeze the filtering capability and according to the thermal analysis results in Figure 3.25, another design possibility could be contemplated in DP_Vol curve by reducing the f_sw down to $20\,\text{kHz}$ and increasing the P_cond to $18.75\,\text{kW}$. Hence, the number of converters could also be reduced from 10 (if $P_\text{conv} = 15\,\text{kW}$) to 8 (if $P_\text{conv} = 18.75\,\text{kW}$). This design consideration, though, results in a larger amount of energy stored in the passive elements, especially in the DC-link capacitor (see Figure 3.28). In fact, as presented in Figure 3.28, the overall stored converter energy, E_conv, of the $18.75\,\text{kW}$ converter design is expected to be $0.55\,\text{p.u.}$ larger than the one stored in the $15\,\text{kW}$ converter design. Note that, in this case, the stored energy values are normalized to the $18.75\,\text{kW}$ converter stored energy. Therefore, while

4.5 p.u. stored energy is calculated for the 15 kW converter-based architecture, the energy of the 18.75 kW converter-based architecture is 8 p.u. Therefore the 18.75 kW design possibility is ruled out because of the significantly increased volume and 15 kW DP$_{Vol}$-based architecture is selected as the preferred choice.
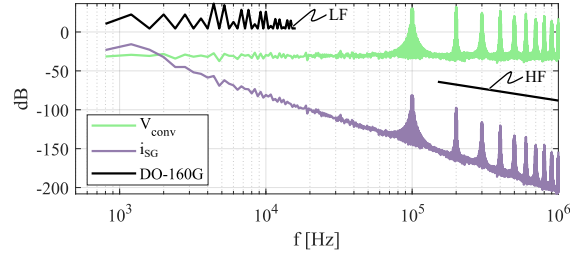

Figure 3.27 DM input filter results of 2L$_C$ architecture for fulfilling LF and HF requirements.
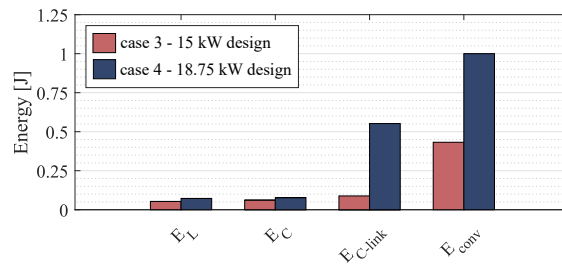

Figure 3.28 Comparison of the stored energy in the passive elements for 15 kW-100 kHz and 18.75 kW-20 kHz 2L$_C$ converter designs.

3.3.3 Single-Stage with STATCOM Configuration-Based Architecture – 2Lst

Aiming to improve the performance of 2L$_C$ architecture, whose consumed reactive power is imposed by the capacitance value and the SG frequency, an alternative structure is proposed in this section which replaces the large input capacitor bank by a STATCOM that behaves as a "*variable capacitor*" (see the architecture schema of Figure 3.29). This way, a relatively small input filter is designed for fulfilling the harmonic requirements while the reactive power required for allowing the single-stage operation of the rectifiers is provided the STATCOMs. Hence, in terms of the 2L$_{st}$ architecture, while the active rectifier focuses on transferring the SG active power to the 270 V$_{DC}$ bus, the STATCOM is disconnected from the distribution bus and establishes its own DC-link voltage for providing reactive power.

A clear difference between 2L$_C$ and 2L$_{st}$ configuration-based architectures is that, in the latter one, the reduction of the input filter volume is achieved owing to a higher number of power converters, which are the STATCOMs. This fact could lead to a higher complexity in the system implementation due to the higher amount of electronics related. However, a higher number of power converters might result in a potential benefit in terms of providing the architecture with a higher degree of redundancy. If both, the active rectifier and STATCOM, are identically designed (passive elements, semiconductors, heat sink, etc.) an architecture with a higher redundancy degree, in case of a power converter failure, can be achieved. In fact, by means of the DC bus voltage control, a power converter could be connected to the DC distribution bus to transmit

active power (rectifier operation) or be disconnected to establish its own higher DC bus voltage and compensate reactive power (STATCOM operation). Therefore, if each additional converter could operate as either a rectifier, which transfers active power, or as a STATCOM for reactive power compensation, functional redundancy is also supported.
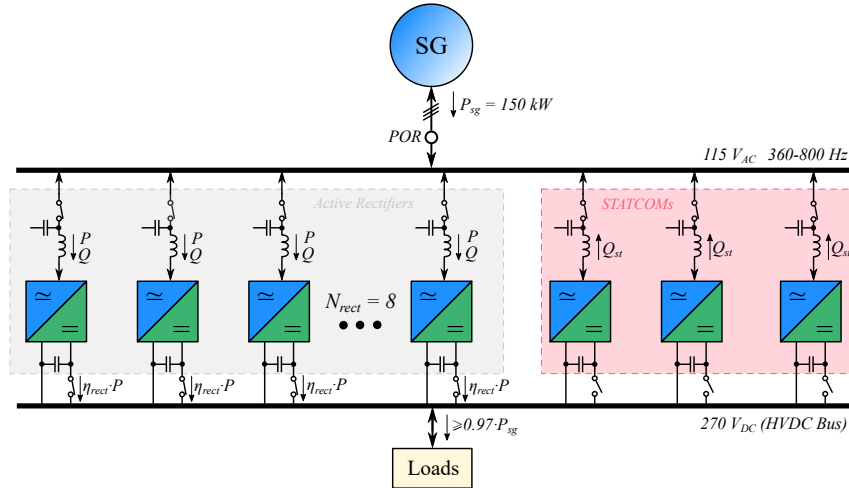

Figure 3.29 Simplified schema of the proposed active modular $2L_{st}$ architecture structure.

In relation to the active rectifier design, in this proposal the reactive power absorbed by the active rectifier is targeted to be the minimum required to achieve single-stage operation. Hence, since the filter capacitor is minimized to fulfill the harmonic requirements, the operating PF of the active rectifier is the maximum possible during its operation (see Figure 3.30). It has to be taken into account, though, that designing the power converter for operating at a single PF point at nominal power should not be possible since the V_L value changes with f. For example, if the active rectifier is operating at a defined (V_L, PF) point and f increases, i_L should be decreased to achieve the same V_L value and maintain the same operating (V_L, PF) point. In fact, to maintain the same PF value, both the active and reactive power absorbed by the active rectifier should be decreased. Note that maintaining the active power at nominal power and decreasing the reactive power implies varying the operating PF of the active rectifier.
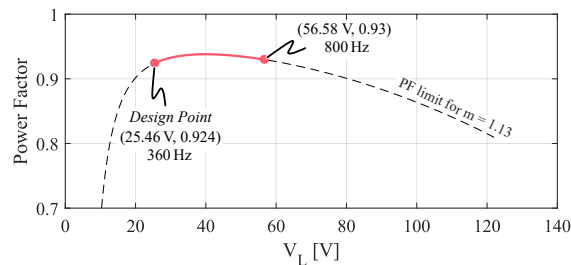

Figure 3.30 $2L_{st}$ configuration PF operating curve.

In this context, the active rectifier is designed to operate throughout the PF range depicted in the curve of Figure 3.30. This PF range describes the maximum average value of the PF points between $V_L = [25.46, 56.58]$ V which are directly related to the SG frequency range between 360 and 800 Hz.

Regarding the design of the passive elements, a similar approach to the $2L_C$ case is followed due to the single-stage configuration nature. In this case, though, the maximum reactive power demand operating point is selected from the defined PF range as the active rectifier design point (see Figure 3.30), i.e., $(V_L, \text{PF}) = (25.46\,\text{V}, 0.924)$. Hence, assuming $f = 360\,\text{Hz}$, the design point data ($V_{ph} = 115\,\text{V}$, $V_L = 25.46\,\text{V}$ and $\cos(\varphi) = 0.924$) and using (3.27), the converter input filter inductance, L, can be calculated depending on the P_{cond} value. Subsequently, the input filter capacitor C is defined for fulfilling the harmonic requirements using (3.19)-(3.22). It is worth to mention that, as later on explained, the voltage spectra introduced in (3.22) corresponds to the one of the STATCOM. The main reason is that the STATCOM establishes a higher DC bus voltage and, hence, generates higher amplitude voltage harmonics at the AC terminals when switching.

Aiming to design a compact input filter while fulfilling the 97 % efficiency target, the $2L_{st}$ rectifier ideal PF behavior is analyzed for the different V_{ph} conditions, that are $100\,\text{V}_{AC}$, $115\,\text{V}_{AC}$ and $122\,\text{V}_{AC}$, in order to identify the worst-case operating condition. Note that, in this case, the reactive power demanded by the rectifier is provided by the STATCOM, which operates as a variable capacitor. Therefore, (3.12) can be rearranged using (2.4), (3.13) and (3.29) so that the demanded reactive power by the active rectifier, i_q, is calculated as,

$$i_q = \frac{V_{ph} - \sqrt{\left(\dfrac{m \cdot V_{DC}}{2\sqrt{2}}\right)^2 - (2\pi f L i_d)^2}}{2\pi f L} \quad . \tag{3.34}$$

As a result, the required reactive current can be calculated depending on V_{ph}, f and L (and hence, P_{conv}). Thereby, the operating PF is calculated by introducing (3.31) and (3.34) in (3.33). A graphical representation of the rectifier operating PF is presented in Figure 3.36(a) where it can be observed that, when transferring the rated converter power, the $2L_{st}$ rectifier operates following the maximum PF limit curve for the defined m of 1.13.
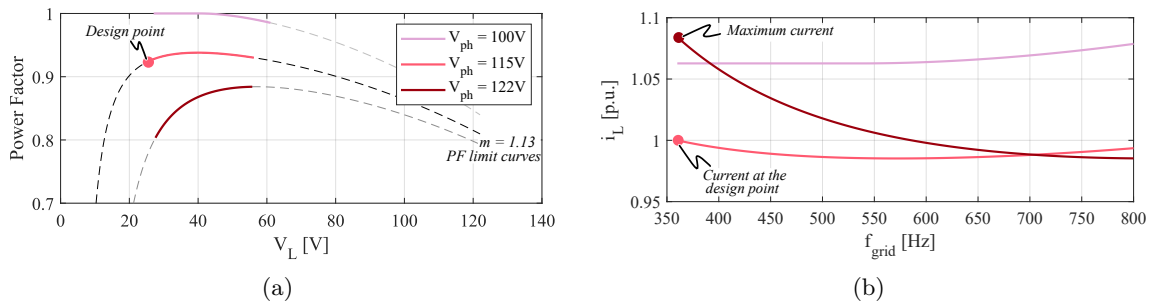
Figure 3.31 (a) Ideal PF operating limits of $2L_{st}$ rectifier for $100\,\text{V}_{AC}$, $115\,\text{V}_{AC}$ and $122\,\text{V}_{AC}$ phase input voltages and $270\,\text{V}_{DC}$ output voltage, and, (b) the RMS current flowing through the input filter inductor for each V_{ph} scenario throughout the SG frequency range normalized to the $2L_{st}$ design point current.

In the same manner, the inductor current calculation is performed using (3.30), (3.31) and (3.34) and represented in Figure 3.36(b) considering a normalization with respect to the $2L_{st}$ rectifier design point. From the results in Figure 3.31, it is concluded that the worst-case operating condition occurs when $V_{ph} = 122\,\text{V}$ and $f = 360\,\text{Hz}$ due to the 8.4 % current increase

with respect to the design point current. Thus, the maximum semiconductor losses can be expected at this operating condition.

As previously explained, even if the active rectifier and the STATCOM is the same converter, the STATCOM is disconnected from the 270 V distribution bus and, hence, it establishes its own DC bus voltage. Under the approach of the same maximum current for both rectifier and STATCOM operations, the DC bus voltage for the STATCOM is defined as 459 V using (3.12) and assuming $V_{\mathrm{ph}} = 122\,\mathrm{V}$, $\cos(\varphi) = 0$ and $f = 800\,\mathrm{Hz}$. As the selected semiconductor is rated at 650 V blocking voltage, the difference between the semiconductor voltage rating and the STATCOM DC-link steady-state voltage is established in 1.42 times (≈ 1.5 times), being an acceptable limit for aviation applications [51].

It is worth to mention that the fact of designing a power converter which can operate either as active rectifier or as a STATCOM implies that two different DC voltage levels have to be handled, that are 270 V or 459 V. Therefore, the amplitude of the generated harmonics when switching will differ depending on the operating mode. The larger the DC bus voltage, the larger the amplitude of the generated harmonics. Thus, due to the increased DC voltage bus level of STATCOMs, the voltage spectra of the STATCOM terminals is considered in (3.22) for the worst-case attenuation calculation and, hence, input filter capacitor sizing using (3.19) and (3.21).

From these design considerations, the thermal analysis is performed assuming the worst-case operating condition for both the active rectifier and the STATCOM (see Figure 3.32 below). As expected, the STATCOM operation results a constraining factor in defining the f_{sw} of the converter due to the higher DC bus voltage and, hence, higher P_{sw} for the same maximum current. Since a f_{sw} of $100\,\mathrm{kHz}$ is desired for achieving a compact converter, a nominal power of $18.75\,\mathrm{kW}$ ($18.75\,\mathrm{kVAr}$ in the case of STATCOM) due to the STATCOM operation thermal analysis results.
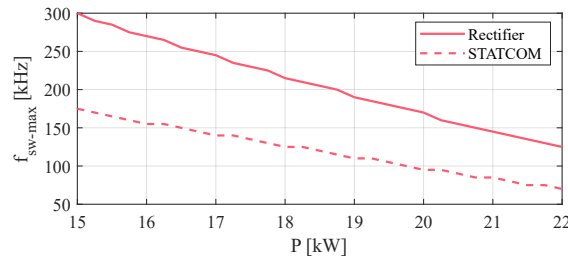
Figure 3.32 Thermal analysis results of the designed converter when operating as rectifier or as STATCOM.

With the defined power rating value, eight active rectifiers of $18.75\,\mathrm{kW}$ are considered in this architecture for transferring the $150\,\mathrm{kW}$ nominal power of the SG. In the case of STATCOMs, though, the required number of STATCOMs, N_{st}, is calculated as,

$$N_{\mathrm{st}} = ceil\left(\frac{N_{\mathrm{rect}} \cdot (i_{\mathrm{q}} - i_{\mathrm{C}})}{i_{\mathrm{L-max}} + i_{\mathrm{C}}}\right) \quad . \tag{3.35}$$

being N_{rect} the number of rectifiers, i_{q} the reactive current demanded per rectifier calculated in (3.34), i_{C} the delivered reactive current by the input filter capacitors (calculated as in Fig-

ure 3.32), and, i_{L-max} the maximum current supplied by the STATCOM flowing through the input filter inductance, i.e. the worst-case operating current previously mentioned.

From (3.35), it is observed that by increasing the input filter capacitor, and thus, i_C: *(1)* the demanded reactive current to the STATCOM can be decreased according to the numerator; and, *(2)* the delivered maximum reactive current by a STATCOM can be increased according to the denominator. Hence, N_{st} can also be decreased by increasing C.

In this regard, Figure 3.33 presents the power losses defined by the $2L_{st}$ architecture at the worst nominal conditions ($V_{ph} = 115\,V$ and $f = 360\,Hz$) depending on the input filter capacitance, where the first capacitance value represents the C required for harmonic fulfillment. Note that, increasing C, though, it also means increasing the overall architecture volume of the passive elements. In addition, reducing N_{st} results in a higher thermal stress per STATCOM due to the increased losses. Since the highest thermal stress is given in the STATCOM, the input filter capacitance is increased up to $19\,\mu F$ while N_{st} is maintained to be 3 (see Figure 3.33). Thus, the design and electrothermal analysis results of the architecture are summarized in Table 3.5 and the "oversized" DM filtering results in Figure 3.34. Note that, aiming to squeeze the overfiltering effort, reduce the thermal stress, and increase the architecture efficiency, f_{sw} is decreased to $80\,kHz$.
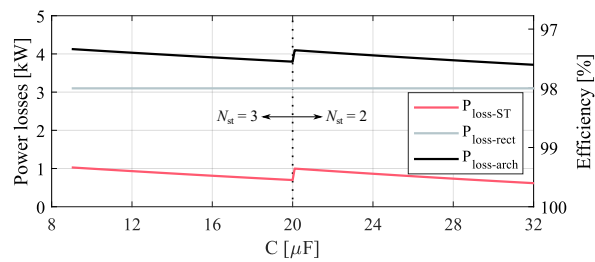
Figure 3.33 The $2L_{st}$ architecture efficiency depending on the C value (operating at $V_{ph} = 115\,V$ and $f = 360\,Hz$).
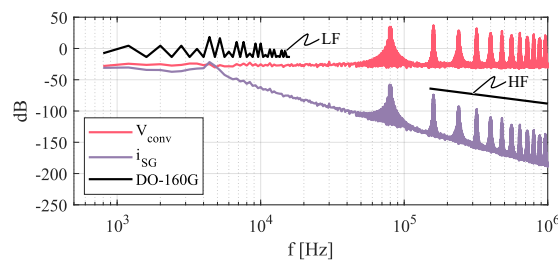
Figure 3.34 DM input filter results of $2L_{st}$ architecture for fulfilling LF and HF requirements.

3.4 Comparative Analysis Among Different Architectures

Based on the presented $2L_2$, $2L_C$, and $2L_{st}$ architecture designs, this section provides a comparative analysis in order to decide the most suitable active modular architecture for the defined MEA application. Thus, following the evaluation parameters described in Chapter 3.2, the selected architectures are compared in Figure 3.35 in terms of efficiency, power density (referred

to volume) and reliability according to the nominal worst-case operating condition of each architecture. The presented results are normalized between 0 and 1 values for comparative purpose, where, for each compared parameter, the obtained maximum value is considered to be 1. Furthermore, the axes of the figure are established to represent a unified evaluation criterion, being the outer side of the spider-chart the better performance. For example, the higher the B_1 the larger reliability or the larger the $1/E$ the lower the expected volume of the passive elements. Note that power quality is not considered in the analysis due to the fact that the three architectures fulfill both LF and HF harmonic requirements and, indeed, a $THD_i < 1\%$ is achieved (see Table 3.5).
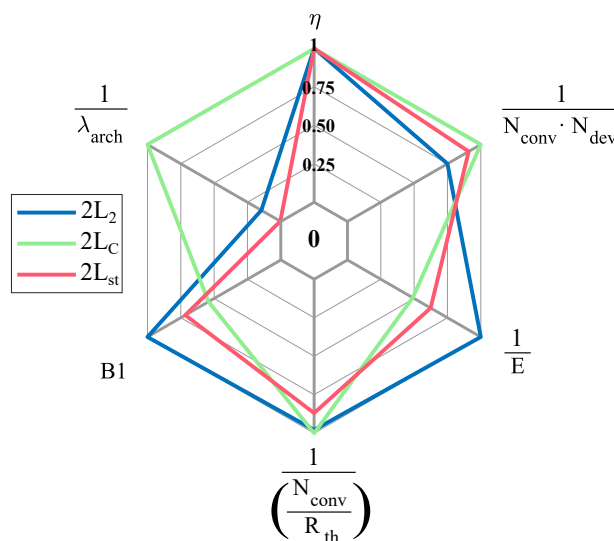

Figure 3.35 Normalized comparative analysis among the designed $2L_2$, $2L_C$ and $2L_{st}$ architectures.

In terms of efficiency, almost no difference can be found among the three topologies when operating close to nominal power values. It is worth to mention that, when operating at relatively low power values (approximately below a third of the rated power), $2L_C$ and $2L_{st}$ architectures present efficiency values below 97% due to the reactive power consumed. This fact is presented in Figure 3.36 where the efficiency of $2L_2$, $2L_C$ and $2L_{st}$ architectures is presented when operating at both SG frequency range ends of the nominal conditions, i.e. *(1)* $V_{ph} = 115\,V$, $f = 360\,Hz$, and *(2)* $V_{ph} = 115\,V$, $f = 800\,Hz$. While the reactive power consumed by $2L_C$ architecture is imposed by the input filter PF corrector capacitor bank, in the case of $2L_{st}$ architecture, though, the STATCOMs could be switched off to increase the architecture efficiency above 97%, owing to reactive power handling.

Regarding the design, $2L_C$ architecture is the most simple and cost-effective in terms of overall semiconductor number $1/(N_{conv} \cdot N_{dev})$. The stored energy in the passive elements, represented as $1/E$, and the expected lifetime, B_1, however, become the main drawbacks of this topology (see Figure 3.35). The $2L_2$ architecture results beneficial not only in this context, but also in the cosmic-ray related reliability aspects. A low FIT/cm^2 $(1/\lambda_{arch})$ is expected from this architecture and, advantageously, the largest architecture lifetime can be expected according to the highest result of B_1, which means the largest expected reliability in terms of wear-out failures until the probability of failure goes beyond 1%. Nevertheless, operating with a paralleled

DC/DC stage (per converter) increases the complexity of this architecture. Due to the higher thermal stress and blocking voltage of the STATCOM in $2L_{st}$ architecture, a lower reliability degree is expected from the overall architecture compared to the $2L_2$ architecture, especially in terms of FIT/cm^2, i.e. $1/\lambda_{arch}$. However, this issue could be improved by employing a higher voltage rating power device in the STATCOM and, hence, increase B_1 and $1/\lambda_{arch}$ parameters. A higher blocking voltage ratio will improve the reliability in terms of FIT/cm^2 and increase the STATCOM power device's current rating and, thus, reducing the thermal stress will increase the architecture lifetime. In addition, since the operating STATCOM could operate as active rectifiers, in case of power converter failure, three additional functional redundancies are provided by $2L_{st}$ architecture.
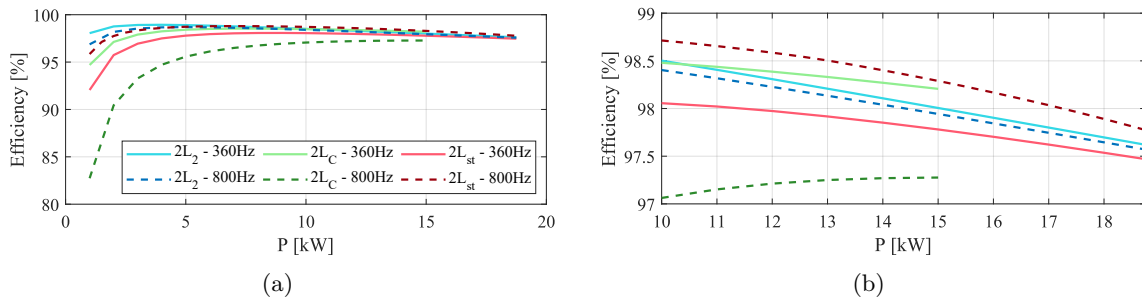
Figure 3.36 (a) Efficiency results of $2L_2$, $2L_C$ and $2L_{st}$ architectures when operating at nominal conditions and both frequency range ends, and (b) zoomed results.

If a power converter of the $2L_{st}$ architecture failed, the grid PF would be diminished while the active power could be maintained at maximum. On the contrary, if a power converter failed in $2L_2$ and $2L_C$ architectures, the delivered active power would decrease. Consequently, three additional redundancies should be added to $2L_2$ and $2L_C$ to provide the same redundancy degree of the $2L_{st}$. Thus, in order to evaluate the influence of additional redundancies in the architecture volume, costs, and complexity, an additional normalized analysis is presented in Figure 3.37, focusing on the volume of the passive elements, the cooling system volume, and the number of power devices. Note that, in this case, the closer the depicted results are to the zero value, the lower the cost and volume, and hence, the better.

Figure 3.37 Normalized comparative analysis among $2L_2$, $2L_C$ and $2L_{st}$ architectures when three redundancies are considered.

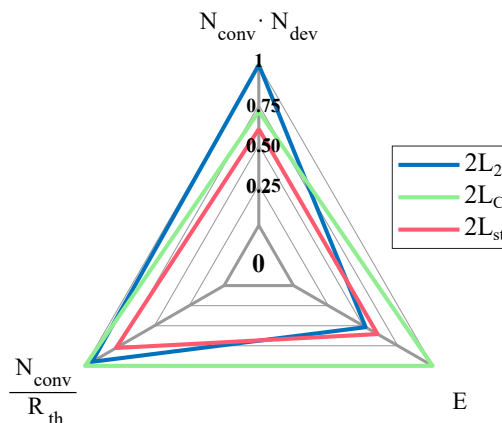As a result, the three additional redundancies in the $2L_C$ architecture are counterproductive in terms of the passive elements volume, E. Regarding complexity and costs, $2L_2$ architecture is the one hindered by an overall number of power devices, which almost doubles the required ones by the $2L_{st}$ architecture. In this context, $2L_{st}$ architecture is the most cost-effective architecture, while maintaining a relatively low volume when three redundancies are considered. Therefore, $2L_{st}$ architecture is considered the most suitable architecture for the defined application.

3.5 $2L_{st}$ Architecture Simulation and Challenges

3.5.1 Simulation Analysis and Results

From the architecture comparison and selection, a simulation analysis of the modeled $2L_{st}$ architecture (see Figure 3.38) is presented in this section using *PLECS* software. This way, the provided analysis regarding the single-stage operation and the presented design concepts can be verified as well as the PF compensation by the STATCOMs at the POR.
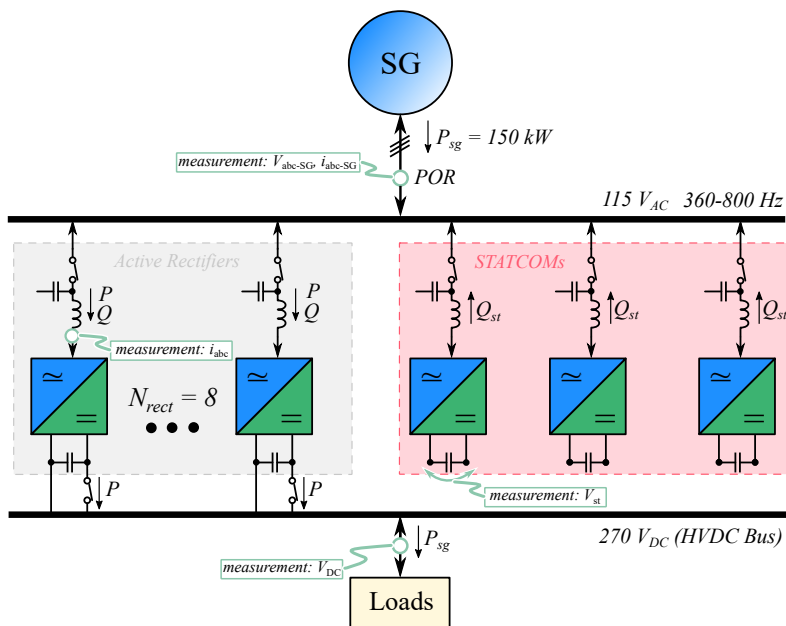
Figure 3.38 Simplified $2L_{st}$ active modular architecture model and considered measurements for the control loops of the converters.

It is worth to mention that, aiming to provide a simplified analysis, only the results regarding steady-state operation at full nominal architecture power, that is 150 kW, is presented. Furthermore, several assumptions have been considered:

- With the objective of reducing the computational effort required for simulating the whole $2L_{st}$ architecture in steady-state operation, the switching power converters are replaced by non-switching Average-Value Modeling power converters (see Appendix A for higher detail). Consequently, the voltage and switching ripples produced by switching effects are neglected.

- A closed loop control, which is depicted in Figure 3.39, has been employed with an inner i_{dq} current loop and an outer V_{DC} loop for both the rectifiers and STATCOMs. However, several differences can be found depending on the converter operation.

On the one hand, a common bus voltage reference of 270 V, V_{DC} *, is used for the rectifiers. Thus, the output DC voltage of each converter is measured and the average value among the measures is calculated and introduced in the feedback loop. The STATCOMs, on their behalf, stay disconnected from the primary distribution bus and, hence, their voltage reference of 459 V is compared only with their individual output voltage.

On the other hand, contrarily to the common DC bus voltage reference, the reactive current reference, $i_{q-conv}*$, is compared individually for each rectifier at its terminals aiming to establish single-stage operation. A common $i_{q-SG}*$ is established in the case of STATCOMs, though, which is used for ensuring unity PF operation at the POR. Thus, $i_{q-SG}*$ is compared with the average value of the measured i_q at the STATCOM terminals.

(a)

(b)
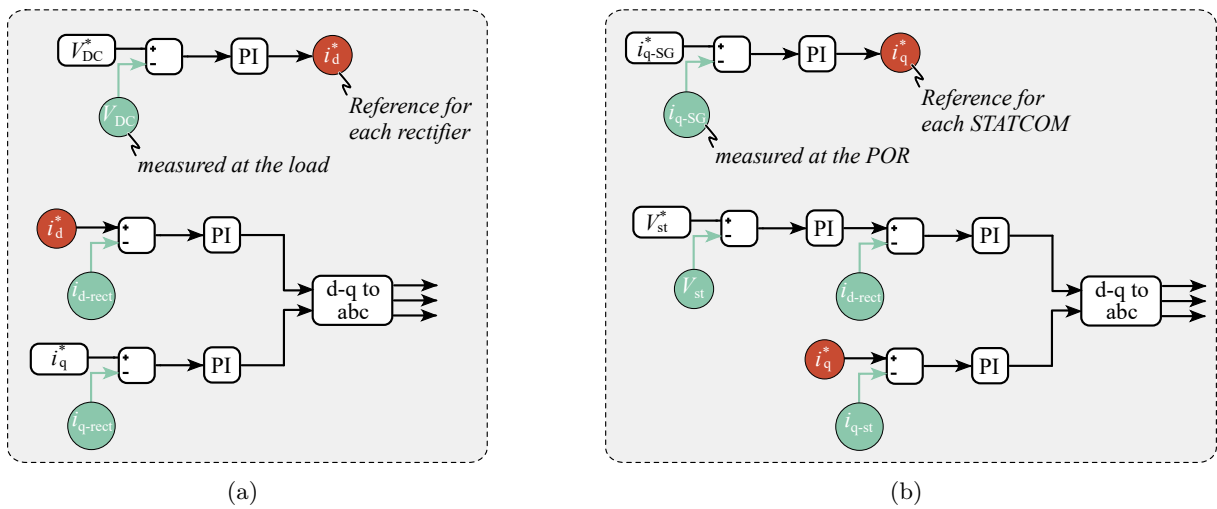
Figure 3.39 Closed Loop control for (a) rectifier operation and (b) STATCOM operation

With the presented simplifications, the steady-state operation results of the active modular rectifier architecture are presented in Figure 3.40 aiming to demonstrate that: *(1)* unity PF operation at the POR is achieved (see the top-side graph presenting the phase voltage and current waveforms of the SG); *(2)* single-stage operation is achieved for transferring 150 kW to the DC bus while operating at both frequency range ends, i.e. 360 Hz and 800 Hz; Single-stage operation is presented in the figure in the middle while the full DC power transferred is observed in the figure at the bottom. Note that Figure 3.40(a) presents the simulation results at 360 Hz while the simulation results at 800 Hz are presented in Figure 3.40(b).
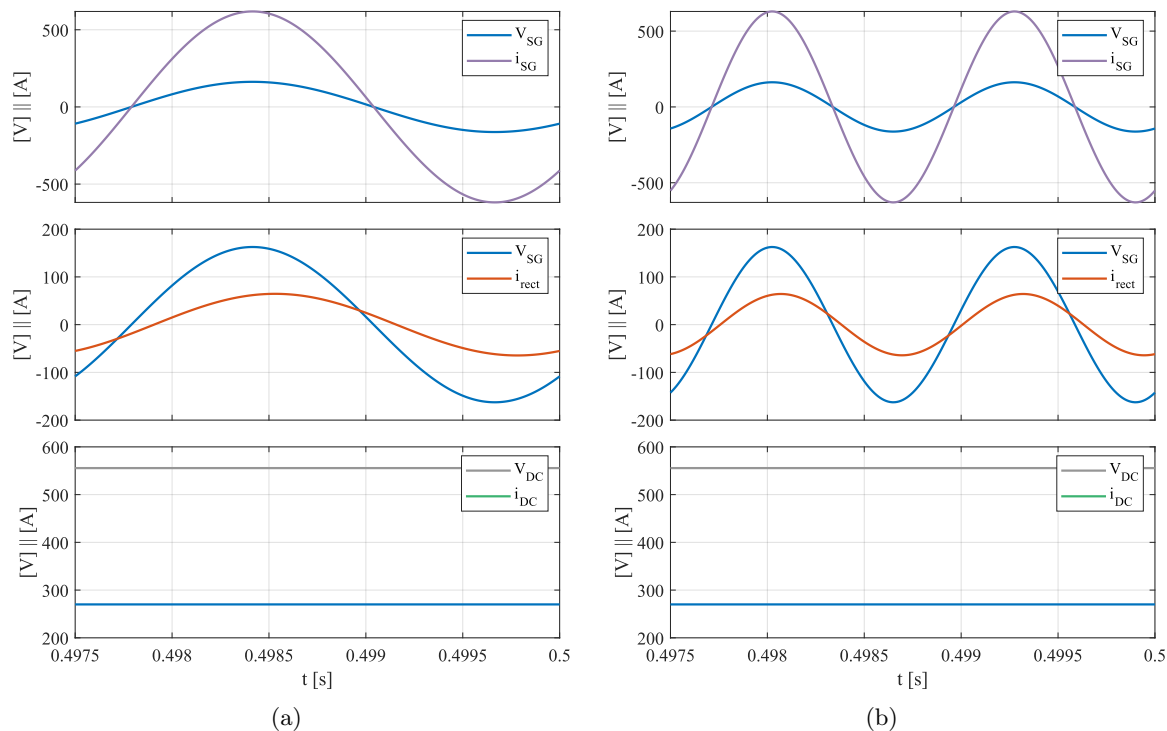
Figure 3.40 Simulation results of the 2L$_{\text{st}}$ architecture when operating at full 150 kW power and (a) $f = 360$ Hz SG frequency, and (b) $f = 800$ Hz.

3.5.2 Experimental Analysis of the Converter Operating PF

Aiming to verify the analyzed theoretical concepts such as the two-stage configuration at unity PF and the single-stage configuration in a real scenario, an experimental validation has been done (as a "proof-of-concept") based on an existing *Ikerlan S. Coop.* lab-prototype. Furthermore, due to the lack of a SG for performing the "proof-of-concept" as in a real aircraft scenario, the Spanish electric grid has been used as power generation source. The features of the experimental scenario are summarized in Table 3.7.

Table 3.7 Summary of the features of the experimental scenarios employed to demonstrate the theoretical two-stage and single-stage configurations.

Parameter	Two-Stage Configuration	Single-Stage Configuration
P_{conv}	18.75 kW	18.75 kW
V_{ph}	230 V$_{\text{AC}}$	230 V$_{\text{AC}}$
AC frequency	50 Hz	50 Hz
Operating PF	1	0.85
Input Filter Inductance, L	5 mH	5 mH
V_{DC}	624 V$_{\text{DC}}$	540 V$_{\text{DC}}$

Considering that the input phase RMS voltage of the Spanish grid is 230 V$_{\text{AC}}$, the Boeing B787 rectification scenario, i.e. 230 V$_{\text{AC}}$ to 540 V$_{\text{DC}}$, has been assumed. Note that this voltage levels represent the double as the one of the considered aircraft scenario, i.e. 115 V$_{\text{AC}}$, to

270 V$_{\text{DC}}$, and , hence, the controllability as well as the operating PF limits are equivalent.

In this context, Figure 3.41(a) presents the casuistry of the two-stage configuration which, adapted to the Spanish grid context, operates at unity PF while establishing a 624 V$_{\text{DC}}$ bus voltage (see V_{conv} in the figure). Thus, the previously defined 312 V$_{\text{DC}}$ are doubled in this case due to the doubled input voltage. Similarly, Figure 3.41(b) represents the single-stage configuration casuistry. Concretely, the 2L$_{\text{st}}$ rectifier conditions are experimentally verified. Thus, based on the input 230 V$_{\text{AC}}$, the power converter establishes a 540 V$_{\text{DC}}$ bus voltage while achieving a 0.92 PF lagging at its terminals.
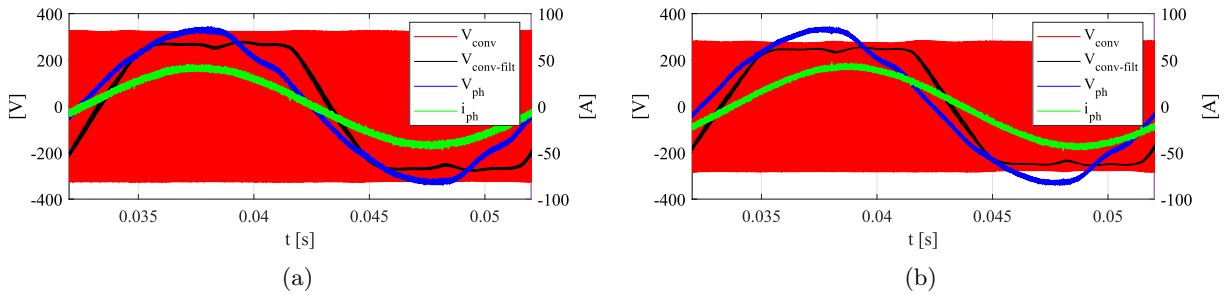
Figure 3.41 Experimental "proof-of-concept" analysis of the two-stage and single-stage configuration concepts. (a) Voltage and current waveforms of the two-stage configuration. (b) Single-stage voltage and current waveforms.

To verify the calculated PF curve limits, the operating PF of the experimental 2L$_{\text{st}}$ converter has been increased. Thus, it demonstrated that the converter starts to overmodulate when operating at PF values beyond the established limits. In this case, Figure 3.42 shows the experimental results of the lab prototype in which overmodulation is appreciated at the end of the depicted cycle when operating at a PF = 0.95. Note that in this case, a relatively high PF value to start overmodulation (above the assumed 0.92 limit) might be reached because a higher modulation index is achieved with the prototipe device, i.e. $m = 1.15$, which increases the operating PF - V_{L} curve of the converter.
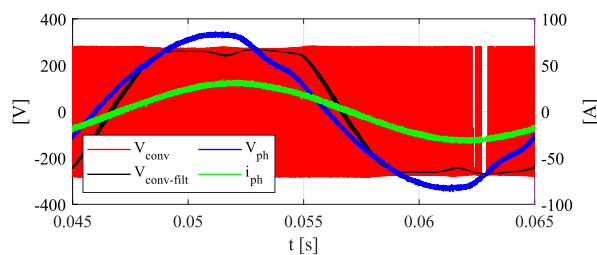
Figure 3.42 Experimental "proof-of-concept" analysis of the single-stage configuration concept presenting overmodulation when the operating PF is increased beyond the mathematical limits.

3.5.3 Active Modular Rectifier Architecture Related Challenges

With the theoretical design and operation verified by simulation and an experimental analysis, the following topics are identified as potential challenges for the continuous development of the architecture in the MEA context:

- **Integration in the aircraft EPS:** once the active modular architecture designed, its

integration into the MEA EPS becomes a research interest. In fact, as it is done in this research work, a strong research effort is being done to migrate to an aircraft EPS which supports the HVDC-based primary distribution network. Concretely, a migration to the single-bus EPS topology is typically encouraged because of its simplicity, lower amount of cable and, hence, expected high power density. However, with the increase in the electrified aircraft loads, the EPS protection and the reliability of supply and load feeding do also become important factors to be considered. Thus, other HVDC-based EPS topologies could also be evaluated such as the ones employed in vessel applications. The existing topologies such as the ring-bus type or the single-bus topologies, provide different characteristics in terms of weight, number of protection systems, redundancy and protection coordination. Consequently, evaluating other potential EPS for the coming MEA in which the active modular architecture can be integrated results to be a potential interest to be performed in this work.

- **Fault-analysis and protection:** in relation to the research effort on the alternative MEA EPS to be implemented, the reliable operation of the $2L_{st}$ architecture as well as the protection systems to be employed do also play a crucial role. A strong trend is observed in literature regarding the use of Solid-State Circuit Breaker (SSCB)s for protecting rectifiers, busbars and loads. hese systems, however, not only present a relatively high amount of losses but also a relatively high cost compared to other traditional solutions such as the fuse or the mechanical circuit breaker. Hence, employing a SSCB per converter of the active modular architecture, for instance, could result in a diminished conversion efficiency and an excessive implementation cost. Therefore, the evaluation of the protection systems to be employed so that a fault-tolerant $2L_{st}$ active modular architecture is achieved becomes also a research task to be done in this work.

- **Post-fault reconfiguration and functional redundancy of the STATCOMs:** As previously mentioned, one of the main benefits of the $2L_{st}$ architecture is the functional redundancy provided by the STATCOMs. Thus, if a rectifier fails, it is expected that one of the converter modules changes its operating mode from STATCOM to rectifier. This way, all the DC loads can still be fed even if a rectifier fails, but owing to a lower PF at the POR. Since this concept is also linked to the $2L_{st}$ protection research task, the STATCOM reconfiguration is also considered as an interesting research point to be analyzed.

3.6 Summary

The continuous development of aircraft electrification has led toward the research and development of innovative and reliable electric drive architectures. Considering the up-to-date $115\,V_{AC}$ input and a $270\,V_{DC}$ output rectification scenario, three active rectifier configurations were proposed to replace the traditional ATRU technology. However, identifying the most suitable configuration for implementing an active modular architecture is not a straightforward decision, due to the different attributes that surround each configuration. Thus, a comparison framework is proposed, which evaluates efficiency, reliability, and power density (referred to architecture volume), which are considered crucial parameters in aircraft applications.

The design criteria of $2L_2$, $2L_C$, and $2L_{st}$ architectures are presented and comparisons among the three architectures are performed. The three architectures are designed to fulfill the operating, power quality and harmonic requirements of aviation standards. Thus, the three architectures achieve an efficiency above 97 % when operating at nominal conditions and a high power quality (referred to as THD_i below 1 %). The $2L_C$ architecture is the simplest, but also the bulkiest in terms of stored energy. In addition, the fact of suffering from higher thermal stress makes this architecture less attractive than the other proposals in terms on wear-out failures. The $2L_2$ architecture, on the contrary, stands as the most compact architecture. Moreover, the highest reliability in terms of wear-out failures is achieved by this architecture. This fact is achieved by means of paralleling the DC/DC stage legs, which, inherently, is translated into an increased complexity. The $2L_{st}$ architecture presents potential results in terms of complexity and volume. However, the higher DC bus voltage and thermal stress of the STATCOM penalizes the architecture in terms of reliability. This issue could be solved by employing a higher voltage rating power device and, therefore, improving reliability parameters. In addition, the fact that the active rectifier and STATCOM are identical converters provides the architecture with a higher redundancy degree compared to the other proposals. In fact, a different paradigm of the comparative analysis is observed if three redundancies are considered in every architecture as already provided by $2L_{st}$ architecture.

The three additional redundancies emphasize the large volume related to the stored energy in $2L_C$ architecture. Additionally, a relatively large number of power devices is required for the $2L_2$ architecture (almost doubled with respect to the $2L_{st}$ architecture) which, indeed, can be translated to larger costs and complexity apart from the previously assumed parallel operation of the devices in the DC/DC stage. Consequently, the $2L_{st}$ architecture is preferred not only because lower complexity and costs are expected, but because a relatively low volume is achieved while providing high efficiency, high power quality, and a high redundancy degree.

Furthermore, on the one hand, a simplified simulation model of $2L_{st}$ architecture is presented aiming to demonstrate the proposed theoretical concepts of the single-stage performance and PF compensation at the POR at steady-state operation. Therefore, verify that the operating requirements of the aviation standards imposed during the active modular architecture design are fulfilled. On the other hand, several leads of future work for integrating the active modular architecture into the aircraft EPS are discussed from which, in accordance to the reliability and redundancy issues demanded in MEA literature, researching on the fault-operation and protection systems related to the aircraft EPS gets strength. In fact, depending on the Aircraft EPS topology employed, i.e. radial-, ring- or distributed-topology, the fault-protection strategy might be different and, hence, the most suitable combination should be found for integrating the designed active modular rectifier architecture.

CHAPTER 4

Protection and Integration of the Active Modular Architecture into the MEA EPS

Summary:

The integration of the 2Lst active modular rectifier architecture into a fault-tolerant MEA HVDC primary distribution-based EPS the research focus of this chapter. Thus, a literature review about the DC short-circuit fault challenges and protection systems is conducted, from which fuses and SSCBs are selected as the most promising technologies to perform a successful protection coordination. Afterwards, the implementation of these protection devices into the 2Lst architecture is studied aiming to perform later on a DC EPS system-level fault-protection analysis. Here, the proposed STATCOM-to-rectifier operation after 2Lst converter fault is also verified by simulation. Since the DC EPS topology does also have an impact on the energy distribution efficiency, overall aircraft weight and fault behavior, a comparison between the state-of-art multi-bus approach and the ring-bus approach is performed based on these three characteristics. Thus, both EPS topologies are designed and compared under a comparison methodology proposed in this work based on efficiency, weight, survivability and fault clearing speed.

4.1 HVDC-Based EPS Topologies and Protection Challenges

A comparison of three potential active modular rectifier architectures for MEA applications was performed in the previous chapter. Due to the different structural attributes related to each potential architecture solution, being a second DC/DC stage in the $2L_2$ configuration-based architecture, the PF compensation input filter capacitor bank in the $2L_C$ configuration-based and the PF compensation STATCOMs in $2L_{st}$ configuration-based architecture, a comparison framework was proposed for the comparative analysis focused on efficiency, power density (referred to volume) and reliability characteristics.

Considering that, apart from the operating active rectifiers, 3 additional converters are implemented in the architecture for redundancy purposes, $2L_{st}$ architecture resulted to be the most promising solution for MEA applications due to its lower complexity and costs expected, relatively low volume, high efficiency and power quality, and a high redundancy degree offered by the identical design between active rectifiers and STATCOMs. Moreover, a simulation model of the active modular architecture was presented aiming to demonstrate the developed theoretical calculations. Finally, a discussion on the potential issues related to the integration of $2L_{st}$ modular architecture into the MEA for establishing a primary HVDC distribution-based EPS was provided. From the discussion, it was concluded that the DC EPS topology as well as the protection devices to be employed play a crucial role for, on the one hand, integrating the $2L_{st}$ architecture into the proper EPS and, on the other hand, achieving an EPS featured by high efficiency, power density and reliability.

In this regard, it is known that the future implementation of an $270\,\text{V}$ HVDC distribution-based EPS in the MEA bring several advantages such as a reduced amount of cable, leading to an expected lower weight and a higher EPS power density, or a greater EPS simplicity because of the reduced number of power conversion stages, among others [40]. In addition, a high power distribution efficiency is provided by HVDC distribution-based EPSs which, typically, are featured as low impedance distribution networks. However, the fact of being a low impedance distribution network does also result challenging when referring to DC short-circuit faults and their management [37, 40, 126]. Especially, in applications such as MEA where a compact DC EPS is expected and, hence, the fault current might propagate throughout the whole EPS at relatively small times causing catastrophic damages. The main cause of the fast propagation is, indeed, the low impedance of the EPS and, more precisely, the low inductance. As represented in Figure 4.1, the fault current increase, di/dt, depends on the inductance voltage, V_L, which under short circuit condition is approximately the bus voltage, V_{DC}, and the fault path inductance value, L_{fault}. Thus, the lower the EPS inductance, the higher the di/dt.
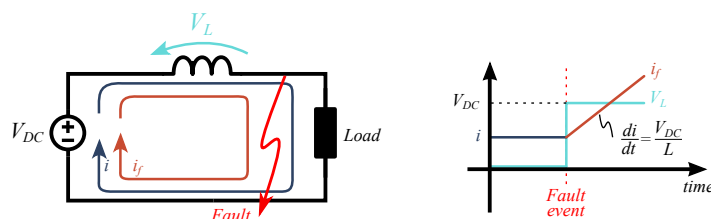

Figure 4.1 Simple circuit example describing the currents during normal and short-circuit operation.

In this work, the generation system for the DC EPS is proposed to be composed by the SG interconnected with the $2L_{st}$ active modular architecture designed in the preceding chapter. Based on this approach, a DC short-circuit fault can be featured by two main responses [37, 40] on the one hand, the immediate transient discharge of the DC-link capacitors across the DC bus, and, on the other hand, the steady-state discharge current from the power generating sources, being the SGs, as it is depicted in Figure 4.2. This effect is typically described by a four-stage process [37, 40, 64]:

Stage 1: In the first stage, the DC-link capacitors across the EPS discharge right away the fault occurs and, hence, the DC-link voltage is reduced. During this capacitive discharge instant, a huge surge fault current flows through the EPS to the fault path. Note that this massive current, on its behalf, might produce thermal damage to the elements in the fault current path (including the proper dc-link capacitor itself), mechanical damage due to the magnetic forces generated on conductors, and even overvoltage damage because of the existing parasitic inductances of the circuit.

Stage 2: Secondly, the SG starts to feed the fault current after the DC-link voltage level descends below the line-to-line voltage and the freewheeling diodes are forward-biased. At this stage, the transistors could be turned-off because of the overcurrent protection.

Stage 3: Thirdly, the SG is in short-circuit condition due to the conducting freewheeling diodes.

Stage 4: Finally, a steady-state fault current is established which flows from the SG to the fault location and whose value depends on the fault impedance.

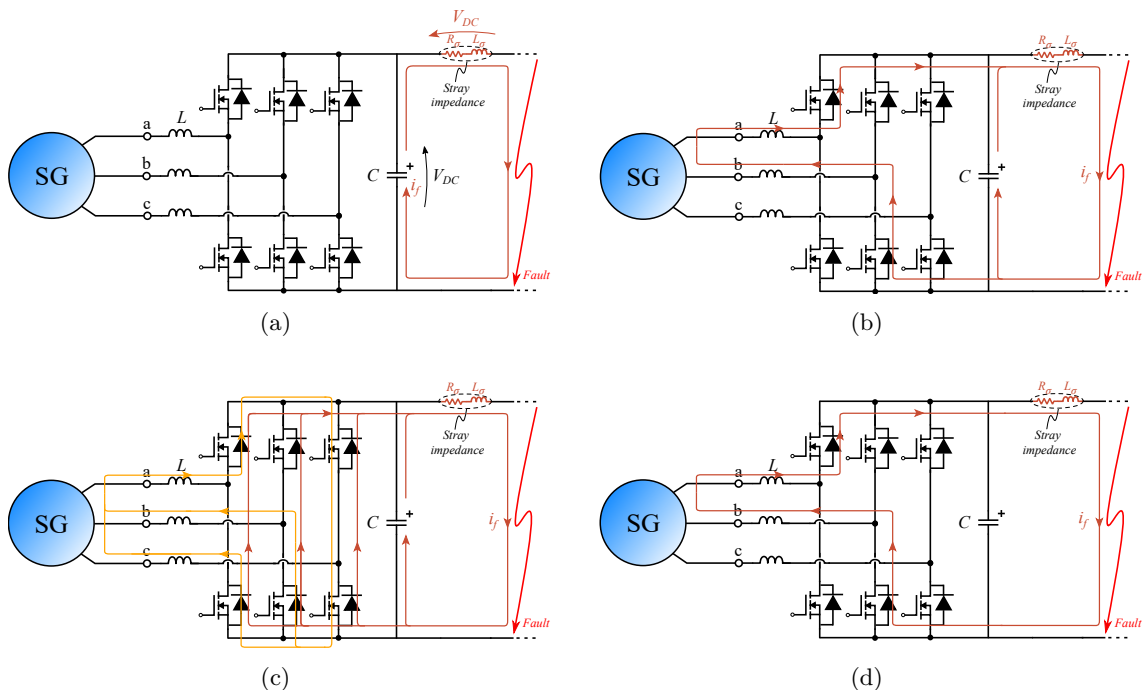**Figure 4.2** Representation of the DC short-circuit current stages, being (a) stage 1, (b) stage 2, (c) stage 3, and (d) stage 4.

The concept of avoiding this fault evolution and its consequent generated damage is defined as DC short-circuit fault management. Concretely, the short-circuit fault management involves three main processes, being fault detection, fault isolation and post-fault reconfiguration [37, 40].

Fault detection and isolation are required in order to discriminate the faulty part or section of the distribution network from the healthy one. Thus, the healthy section stays protected and unaffected by the DC fault. The prime challenges to fault detection and fault isolation processes, essentially, are liable to the DC short-circuit current nature, which is characterized by the following [15, 37, 39, 40, 42, 64, 127]:

- **A fierce transient discharge:** In a DC power system, the short-circuit current is typically limited by an extremely low impedance. Thus, when a DC short-circuit emerges, a fast increase in the whole distribution system current and decrease in voltage occur. Particularly, this huge surge in the fault current is originated by the discharge of the DC-link capacitors that are located throughout the distribution system. Due to the fact that the rise time of the fault current is very low (reaching hundreds of amps values in the order of microseconds), an extraordinarily low fault-detection time is required for the fault detection algorithms. As a consequence of this time constraint, a poor coordination between the different protection algorithms and protection systems might be expected for fault isolation.

- **Lack of current zero crossing:** On the contrary to AC systems, in which a sinusoidal current flows through them, a positive DC value current is flowing through a DC distribution network. Therefore, when a DC fault occurs, the fault current constantly increases up to the limited value defined by the distribution network impedance. This fact is considered as the "biggest hurdle" for fault isolation and the traditional protection devices.

  Concretely, the Mechanical Circuit Breaker (MCB) is the typical protective device employed in the conventional $115\,\mathrm{V_{AC}}$ aircraft EPS due to its high efficiency and simplicity [128]. Although its operating principle is later on explained in higher detail (Chapter 4.2) it is important to understand that, aiming to break the fault current, the MCB opens its contacts after a relatively long time after fault detection. During this time an arcing current is formed across the contacts which is extinguished when the current zero crossing happens. Therefore, since the zero current crossing does not occur in DC short-circuit faults, alternative protection devices and techniques should be developed for DC distribution EPS.

Some research studies demonstrate that it is possible to use AC commercial devices, like fuses or the improved MCB example of Figure 4.3(a), to protect some loads in a DC power system [15, 39]. However, with the increasing growth in the EPS of the MEA, the maximum fault currents are becoming larger than any time in the past and, hence, higher and faster short-circuit breaking capacity is demanded for the circuit breakers [129]. More recent aircraft models have already replaced the traditional MCB by a SSCB as the example in Figure 4.3(b) [10, 23, 127, 128]. The SSCB, which is based on power semiconductor devices operation, provides benefit of achieving faster opening times owing to higher costs, volume and lower efficiency [39, 42, 130]. Other research methods include the possibility of replacing the MCB by a Hybrid Circuit Breaker (HCB), depicted in Figure 4.3(c) [1, 15]. This hybrid approach is expected to maintain a high efficiency performance as the MCB while improving its opening time thanks to the semiconductors in the main breaking branch. Note that, even in the opening time is

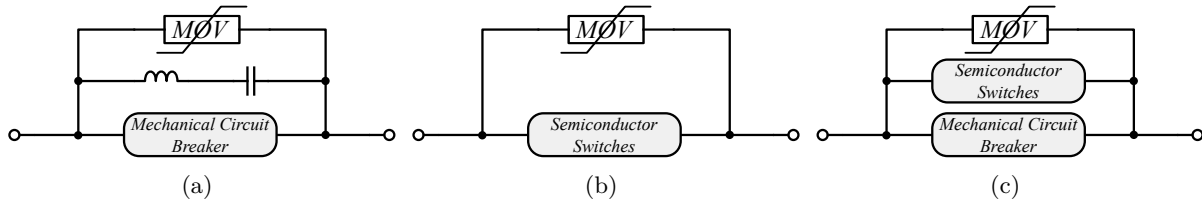improved with respect to the MCB, the HCB is not as fast as the SSCB and it is not an economical solution.

Figure 4.3 Simplified examples of the different circuit breakers under research for MEA applications. (a) MCB. (b) SSCB. (c) HCB.

Therefore, the development and introduction of fast and economical protection devices becomes a research task to be addressed not only to improve the previously mentioned fault detection and isolation related issues, but also to encourage the implementation of the $2L_{st}$ modular architecture into a reliable HVDC distribution-based MEA EPS [128]. Furthermore, it has to be taken into account that the circuit breakers connect different elements of the EPS such as generator, supply buses or loads. Therefore, they also become of great importance when referring to the EPS reconfiguration after the fault is isolated [1, 37]. Essentially, the reconfiguration capability permits to ensure a continuous and, hence, reliable supply. For example, if a specific load cannot be supplied because of a feeder malfunction, the circuit breakers modify the feeding path by reconfiguration. At this point, it is important to bear in mind that in the case of a SG, rectifier, busbar, or load failure, not only the employed circuit breakers allow the possibility of reconfiguration but also the proper EPS topology structure in which the $2L_{st}$ active modular architecture is implemented [37, 38].

Currently, the literature regarding the future MEA EPS advocates for the Single-bus DC EPS topology in Figure 4.4 [8, 15, 36]. However, a lack of literature is found regarding the implementation or suitability of other DC EPS topologies different to the single-bus approach, or even a comparison among them. In this regard, the evaluation and study of different potential DC EPS candidates for MEA EPS becomes a research focus which has not been treated previously in literature, especially under a common or standardized evaluation methodology. Following the lead of vessel applications, which do also target the implementation of compact and reliable DC EPS as in MEA, the most common topologies to be considered for the analysis are the Single-bus and Ring-bus [37, 38, 40, 131]. Additional topologies are also considered for vessel applications, such as the Breaker-and-Half, Dual-Ring-bus or Solid-State Transformer Isolated topologies, but they are typically featured as relatively complex and/or heavy topologies with an excessively high number of protection devices and, hence, they are not considered to be of interest for MEA applications [38, 131].

The Single-bus (or DC common bus) topology, presented in Figure 4.4(a), is considered as the simplest HVDC distribution-based EPS topology [8, 15, 37, 42]. This EPS topology describes a radial-type distribution approach in which all the distributed power generation sources and loads are connected to a common DC bus. Thus, its inherent simplicity and its expected low amount of cable for distributing the generated power, make this EPS topology a potential candidate in terms of high efficiency and high power density for being implemented in the future MEA.
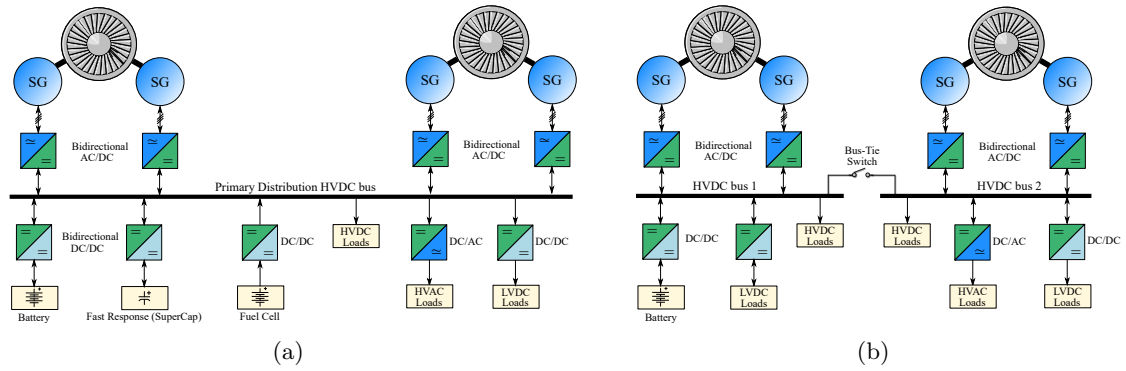
Figure 4.4 HVDC distribution-based EPS topology examples: (a) single-bus EPS and (b) multi-bus EPS with a bus-tie switch.

Besides the expected benefits of the single-bus approach, the critical issues to be investigated in relation to this topology result to be related with the fault management and fault protection strategies [8, 15, 36]. In fact, among all the existing possible fault locations in an EPS, a bus fault could derive into a catastrophic failure if only a single-bus is available for power distribution. Note that implementing a unique distribution bus supposes an insufficient post-bus-fault reconfiguration capability [37]. Therefore, the separation of buses as shown in the example of Figure 4.4(b) is currently considered as a stringent design requirement so that a high reliability and redundancy degree are achieved. This way, if a bus fault occurs, the faulty bus can be isolated by the bus-tie switch while the remaining non-faulty bus is unaffected [8, 37].

In this context, a high bus isolation and post-fault reconfiguration capability can be expected from the Ring-bus topology [37, 38, 40, 42]. In this topology approach, depicted in Figure 4.5(a), the HVDC distribution bus runs across the perimeter of the aircraft providing a possibility for the power generation systems and loads to be connected to both sides of the distribution ring. Thus, a higher number of cable meters is expected, which is translated into a lower efficiency, owing to a higher reliability. Note that typically only the loads which are strictly necessary for fulfilling the aircraft mission, known as vital loads, are connected to both sides of the ring. This way, the reliability concerning the feeding of these vital loads is increased.
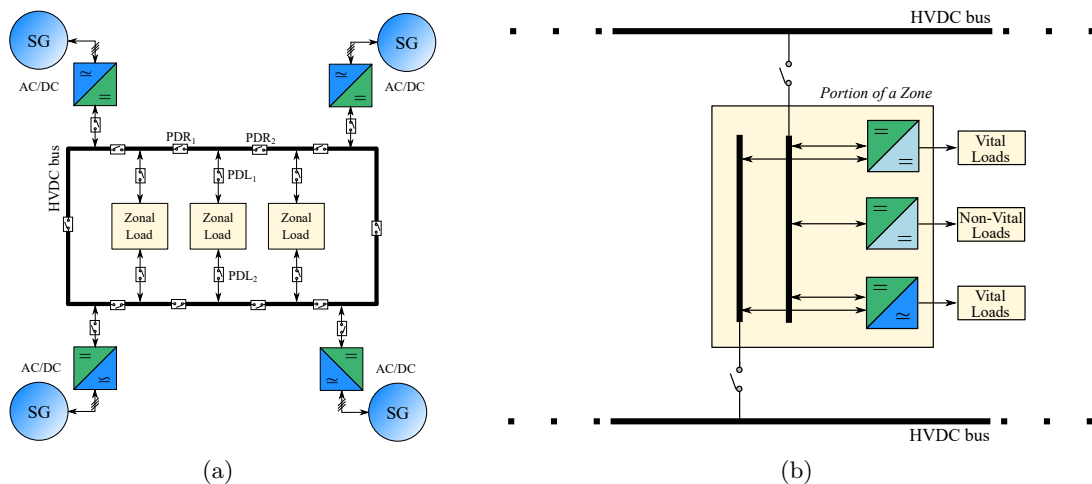

Figure 4.5 (a) Simplified example of Ring-bus EPS topology and (b) a simplified schematic of a Zonal DC Load.

The main reason of this "load connection criterion" relies on the fact that, apart from the protection devices of the load (PD_{L1} & PD_{L2} in the figure), two additional protective devices are required for each connection to the ring to avoid a fault propagation (PD_{R1} & PD_{R2}). Therefore, connecting a high number of loads to both sides could be disadvantageous not only in term of complexity due to the high number of protection devices required, but also because of the added weight due to these protection devices and the load-ring interconnecting cables [37]. An interesting alternative to reduce the number of protection devices as well as the amount of cable used in the Ring-bus topology, is to sectionalize the aircraft into several DC zones [37]. Thus, as in the example of Figure 4.5(b), each zone comprehends the loads that are relatively close to each other to reduce the amount of cable and maintains the "load connection criterion" so that a vital load is connected to both sides of the ring and a non-vital load is connected only to one side.

With two DC EPS topology concepts put on the table, performance differences in terms of efficiency, weight, reliability, reconfigurability and costs can be expected between each other. As previously stated, a key factor affecting these features is how the EPS is protected and the type of protective devices employed. Since different benefits and drawbacks can be found among the existing protective devices, i.e. operating speed, breaking current capability, weight, etc., a literature review of the existing protection devices and the protection technologies under research is provided in the following.

4.2 Protection Devices for the Aircraft EPS

Considering the aviation context, in which efficiency, power density and reliability are extremely important features, the employed protection devices not only have to ensure the reliable energy distribution throughout the aircraft EPS, but they do also have to go in line with these features. In this regard, the following characteristics are typically evaluated when referring to protection devices [17, 130, 132]:

- **The contact- or on-state resistance:** since the protection device is constantly conducting the current of the equipment to be protected, the minimum contact- or on-state resistance is desired in order to reduce the conduction losses and achieve a high distribution efficiency.
- **Operating speed:** on the one hand, the switching speed of the device plays a crucial role because it directly influences the short-circuit current value to be interrupted. Thus, the faster the better in order to avoid interrupting large short-circuit current values. Note that, here, the fault detection does also play an important role. On the other hand, the extinction time is important in order to avoid the fault propagation or a sympathetic tripping of another protection device throughout the EPS.
- **The number of switching operations:** Aiming to reduce the need for maintenance during the aircraft lifetime, it is recommended that the nominal switching operations of the employed protection device hurdles 10,000 operations. It is worth to mention if a short-circuit occurs, the post-fault EPS operation is treated as an extreme emergency condition.

Thus, a mandatory check and maintenance of the safety equipment is performed when the aircraft grounds and, if necessary, the protection device is replaced.

- **Galvanic isolation:** this feature is typically required in all HV grids in order to establish a fail-safe mode of the equipment, i.e. converter, load, busbar, feeder or even the proper breaker, and ensure a full galvanic isolation safety for the crew and maintenance works.

- **EMC resistance:** During the prototype design, it should be ensured that the protection device is not affected by electromagnetic interference. The main reason is that interference by power converters and atmospheric influences might occur during the flight.

- **Explosion risk:** Considering the compactness of the application, it is possible that the location of some protection devices lies close to the fuel storage or other inflammable object. Thus, the installed protection device should not afford any risk explosion.

Several protection devices such as fuses, mechanical component-based breakers or solid-sate technology-based breakers can be found in literature. However, when referring to the aircraft, the suitability of each component should be evaluated considering the features mentioned above [10, 17]. In fact, the technology employed is key to achieve a high-efficient and reliable aircraft EPS. Thus, aiming to provide a discussion on the suitable protection devices to be employed in the aircraft EPS, a high detail description of the different protection devices is provided in the following.

4.2.1 Fuses

The fuse is a single-use protection device which operates against overcurrent faults. It is formed by an element consisting in a heat-absorbing metallic conductor within a pair of contacts, and a cartridge to carry this fuse element [39, 130]. Its simple operating principle is based on the heating effect produced by the carrying electric current. When electric current flows through a conductor, which has an inherent resistance, the power loss generated because of its resistance is dissipated in the form of heat, i.e. the Joule Effect. In this context, two operating conditions can be identified for the fuse [130, 133, 134]:

- Under normal operating conditions, while the fuse is conducting current, the heat produced by the resistance of the fuse is easily dissipated to the environment.

- Under faulty operation, i.e. short-circuit operation or prolonged overload operation, the current flowing through the fuse exceeds the power dissipation capability of the fuse. This power dissipation capability is typically described by the i^2t curve, which essentially represents the energy per ohm that the fuse can dissipate until melting. An example of a i^2t curve is presented in Figure 4.6. Note that the larger the fault current value the lesser the melting time of the fuse. Hence, excessive heat is generated which melts the conducting element of the fuse and breaks the circuit. Thus, an arc is generated between the two contacts of the fuse element until the fault current is extinguished.

Due to this simple operating principle, the fuse is considered as a simple protection device which, besides that, provides additional features such as the fact of being low cost, low weight, and low volume device. Regarding the disadvantages, the two main drawbacks of the fuse are

its single-use operation, which implies replacing it manually after operation, and its lack of discrimination between a transient condition and a permanent fault [10, 17, 39, 130, 133, 134]. Thus, two types of fuses can be found in order to protect the system with respect to a transient condition or a permanent fault: time-delay fuses and fast-acting fuses.
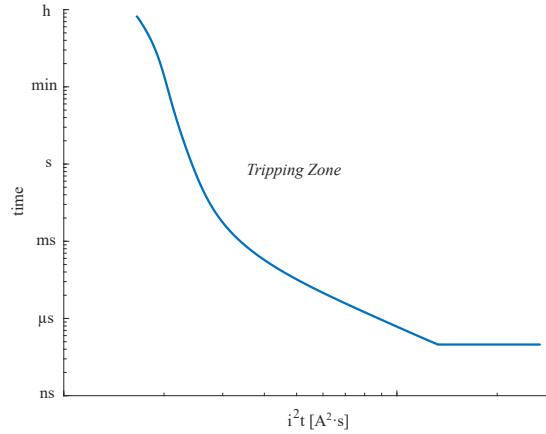

Figure 4.6 Example of an i^2t fuse melting curve.

Time-delay fuses are implemented for protecting against transient inrush currents, which are high-frequency current peaks that arise when some loads, like starting motors, are energized [130]. Fast-acting fuses, on the contrary, are used to protect a system against a permanent fault such as a short-circuit. Thus, fast-acting fuses are the ones typically employed to protect the output of power converters, for example [130, 134, 135].

4.2.2 Mechanical Circuit Breakers

The MCBs are those which employ mechanical moving parts to interrupt the current flow when a fault event occurs [127, 130]. These devices are considered as the traditional devices used in aircraft application due to their long history and, indeed, are the most typical protection devices used in $28\,\mathrm{V_{DC}}$ and $115\,\mathrm{V_{AC}}$ aircraft EPSs [10, 128].

Its operating principle is based on a magnetothermal component which opens the circuit according to a i^2t curve [127, 128]. Therefore, the MCB opens when the maximum current limit has been achieved or, in case of overload current, when the maximum thermal limit has been achieved. During the process of reacting to a fault, the moving contact (or bimetal) starts the separation and, due to the reduced contact area and increased current density, an arc plasma is generated between contacts. Note that even if the contacts are distant, the generated arc keeps the fault current flowing through it. The fault current, and hence the proper arc, is extinguished when the current gets to zero amps [39, 130]. It must be remarked that, in the case of a DC circuit, though, the fault current does not present a zero-crossing waveform unlike in an AC circuit [37–39, 42].

In order to reduce the impact of the arc and produce an artificial zero-crossing current waveform, the most typical solutions proposed in literature are the ones presented in Figure 4.7 [39, 127, 130]. These solutions rely on adding to the MCB either a passive current switching

network as in Figure 4.7(a), or an active switching network as in Figure 4.7(b). In both cases, the protection element is formed by the conduction branch in which the MCB is found, a series resonant circuit branch, and an energy absorbing branch in which, typically, a Metal-Oxide Varistor (MOV) is used to dissipate the stored energy in the line.
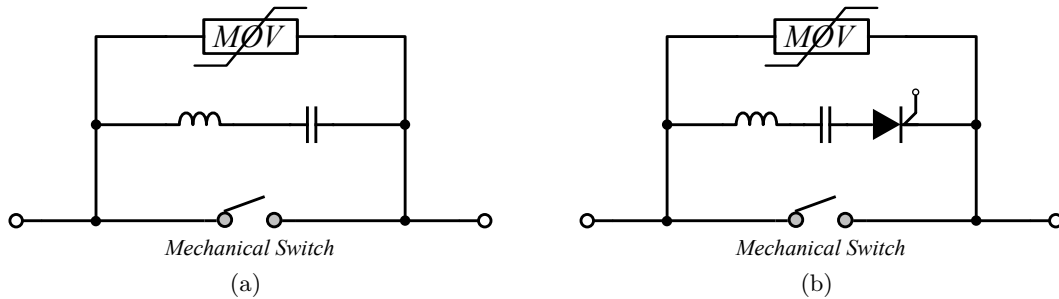

Figure 4.7 MCB protection device with (a) a passive resonance network, and (b) an active resonance network.

In the MCB with passive resonance network of Figure 4.7(a), an inductor and a discharged capacitor are connected in series in the resonant circuit branch. During normal operation, the current flows through the low-resistance (few $\mu\Omega$) mechanical switch. However, when fault condition comes up and the MCB is opened, the generated arc voltage starts to commute the current to the series resonant circuit branch. Thus, an increasing sinusoidal current starts to flow through the series resonance branch generating, in consequence, a zero-crossing current in both MCB and series resonant branches. As a result, the MCB interrupts the generated zero-crossing current flowing through it. It must be remarked that this process might be delayed several milliseconds due to the inherent slow response time of the mechanical moving parts [39,127,130].

Once the current branch-commuting and MCB switching-off processes occur, the voltage across the MCB keeps increasing due to the accumulating charge in the capacitor of the series resonant branch. Finally, once a certain voltage level is achieved, the energy-absorbing branch is energized and the current flows through the MOV until all the stored energy in the line is dissipated and hence, the fault current is extinguished.

Particularly, the MOV behaves as a variable resistance which is negatively proportional to its applied voltage (seeFigure 4.8). This way, when zero voltage is applied to the MOV its resistance is maximum and, contrarily, the MOV resistance is minimum when the applied voltage is the clamping voltage [39, 127, 130]. Therefore, once the MOV is energized, the voltage across it is maintained at a reasonably constant with a progressive decreasing value until all the stored fault energy in the line inductance is dissipated [127].

Contrarily to the MCB with passive resonance network, in the MCB with active switching network presented in Figure 4.7(b) the capacitor of the series resonant branch is already pre-charged prior to the MCB opening. Therefore, when the MCB opens, the series resonant branch is switched on and the capacitor delivers a negative current equal in magnitude to the fault current in order to generate a zero-crossing current at that instant.

Among the main benefits of the MCBs presented in Figure 4.7, the low on-state conduction losses, the device simplicity and the low implementation cost are highlighted. These advantages,

however, must be weighed against the relatively low fault clearing time ($\geq 1\,\text{ms}$), the produced aging due to the produced arc when interrupting the fault current, their lack of remote control, which means that they must be located close to the cabin controls unless additional monitoring is used, and the fact that they cannot protect against arc faults due to their short time of duration, which may cause catastrophic damage to wires or induce the ignition of isolating materials or fuel located close to the arc fault spot [39, 130, 136].
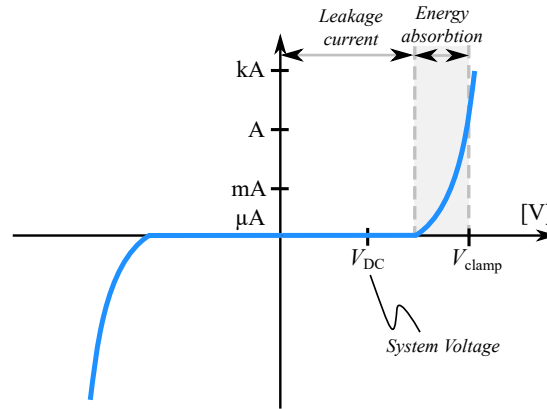

Figure 4.8 Typical I-V characteristic of a MOV.

On the one hand, in order to detect arc faults and protect the system against the damages that might be caused, an Arc-Fault Circuit Breaker (AFCB) has been developed [10, 128]. This device presents the same protection type as the traditional MCB with the additional protection to arc faults by employing advanced electronics. To provide this extra feature, the current is measured in submillisecond time intervals and, by means of algorithms and current patterns, it determines if an arc fault is occurring. If it is the case, the AFCB interrupts the current flow avoiding critical failures. Moreover, depending on the complexity of the employed algorithms for the AFCB, the arc faults and other similar signals like the ones of inrush currents during normal operation could be distinguished [128].

On the other hand, the lack of remote control of traditional MCBs is solved by employing Remote Controlled Circuit Breakers (RCCB) [128]. This protection device is, indeed, typically found in the up-to-date aircraft EPS to protect AC loads such as EHA [137]. The RCCB, which merges the functionalities of a relay and a circuit breaker, behaves similarly to the traditional MCB but, unlike them, remote switching control is provided by RCCB due to the internal electronic circuits. Additionally, these integrated electronic circuits do also improve the traditional magnetothermal functionality of the MCB, and consequently, the problem of aging presented by this last technology due to the thermal cycles through the bimetal is reduced. It is also reported to be a cheaper device than the traditional MCB [128].

Lastly, aiming to reduce the risk of explosion provoked by the generated arc when opening the mechanical switch, a vacuum interrupter could be used [17, 130]. Due to the inherent harsh environment of aircraft applications, a vacuum interrupter looks like a more suitable option since it provides an impressive dielectric strength and it is not affected by the reduced pressure of high heights. However, a relatively high weight must be assumed when employing these circuit breakers because of the motor drives required for moving the contact in the vacuum.

4.2.3 Solid-State Circuit Breakers

The SSCBs are considered to be the development trend of the protection devices for the up-to-date aircraft EPS [130,138]. As depicted in Figure 4.9, the SSCB employs power semiconductor devices in the main conduction branch instead of mechanical moving parts for the fault current interruption as in the MCB. Typically, IGBTs and Integrated Gate-Commutated Thyristor (IGCT)s are recommended as the power devices to be employed due to their low conduction losses. Particularly, IGCTs generate lower conduction losses but, since their assembly and control requirements are more complex, IGBTs are preferred [10, 39, 128, 130]. In addition, recent research efforts are also focused on using WBG devices in SSCB applications due to their improved conduction characteristic, light weight and reduced cooling requirements [127, 139–141].
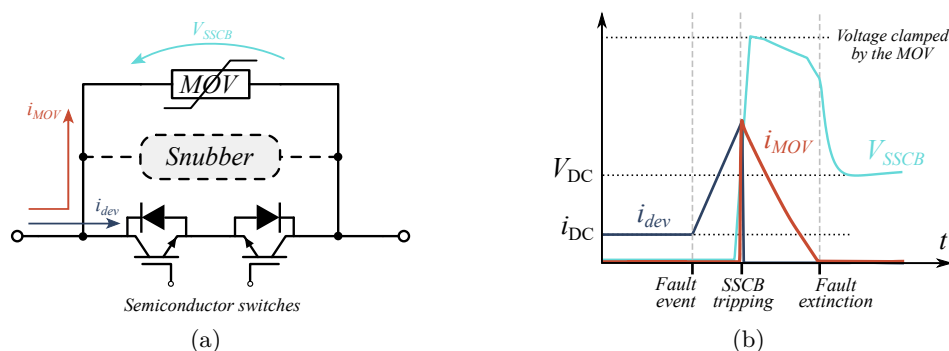
Figure 4.9 (a) Simplified schematic of a typical SSCB, and (b) its ideal switching current and voltage waveforms during fault interruption.

As a result of employing power semiconductors in the main branch, the SSCB not only is capable of reproducing the i²t behavior of the MCB by means of control, but also to achieve a faster operating speed ($\leq 100\,\mu s$) and control accuracy compared to the MCB. Moreover, the SSCB provides additional benefits such as remote control, diagnostics of the fault, wiring reduction and arcing protection. In fact, since no arc is generated when the semiconductor switches interrupt the fault current, no arc-related degradation of the protection device occurs, and the life cycles of the protection device are increased compared to the MCB. As a result, they are also considered as higher reliability devices [10, 21, 40, 126, 127, 129, 138].

On the negative side of the SSCB protection devices, their high cost, the relatively high conduction losses presented, and the mandatory overvoltage protection necessity are found [10, 17, 40, 126, 130]. The fact of employing semiconductor devices on the main conduction branch not only makes the SSCBs more expensive, but also supposes assuming a relatively high amount of conduction losses due to its proper on-state resistance ($\geq 1\,\mathrm{m\Omega}$)), which is much higher than the ones of the MCB devices (few $\mu\Omega$). As a consequence, a bulky cooling system is typically needed for dissipating these power losses.

Moreover, due to the limited power dissipation capability of the power semiconductor devices, an energy absorbing branch containing a MOV or a Transient Voltage Suppressor (TVS) diode, for example, has to be considered for the current extinction. Note that, when the power devices

are turned-off, the fault current is deviated to the energy absorbing branch and is built up as a voltage clamped across the SSCB and, hence, across the power devices (see Figure 4.9(b)). This fact results of special interest in the SSCB because the clamping voltage imposed by the MOV is the one that drives the fault current extinction time and, therefore, part of the overall operating speed or fault clearing time of the SSCB. Simply put, the larger the MOV clamping voltage, the larger the negative di/dt and, hence, the shorter the fault current extinction time.

However, the fact that the MOV is in a branch connected to the circuit in which the fault current starts to flow when the SSCB opens leads to the appearance of parasitic inductances. Therefore, although the energy absorbing device, i.e. MOV or TVS, is used to clamp the voltage across the SSCB, the sudden opening of the SSCB might be translated into an excessive overvoltage due to the parasitic inductance. Consequently, special attention should be paid to the parasitic overvoltage generated since it might breakdown the power device if no action is taken. Thus, an additional snubber circuit branch could be employed to protect the circuit from the overvoltage condition [17, 39, 127, 130].

Typically, the snubber circuits are non-dissipative circuits which focus on loss minimization and quick voltage suppression. In [127], the capacitor (C) snubber, the resistor-capacitor (RC) snubber and the resistor-capacitor-diode (RCD) snubber depicted in Figure 4.10 are presented as potential solutions for SSCB applications.
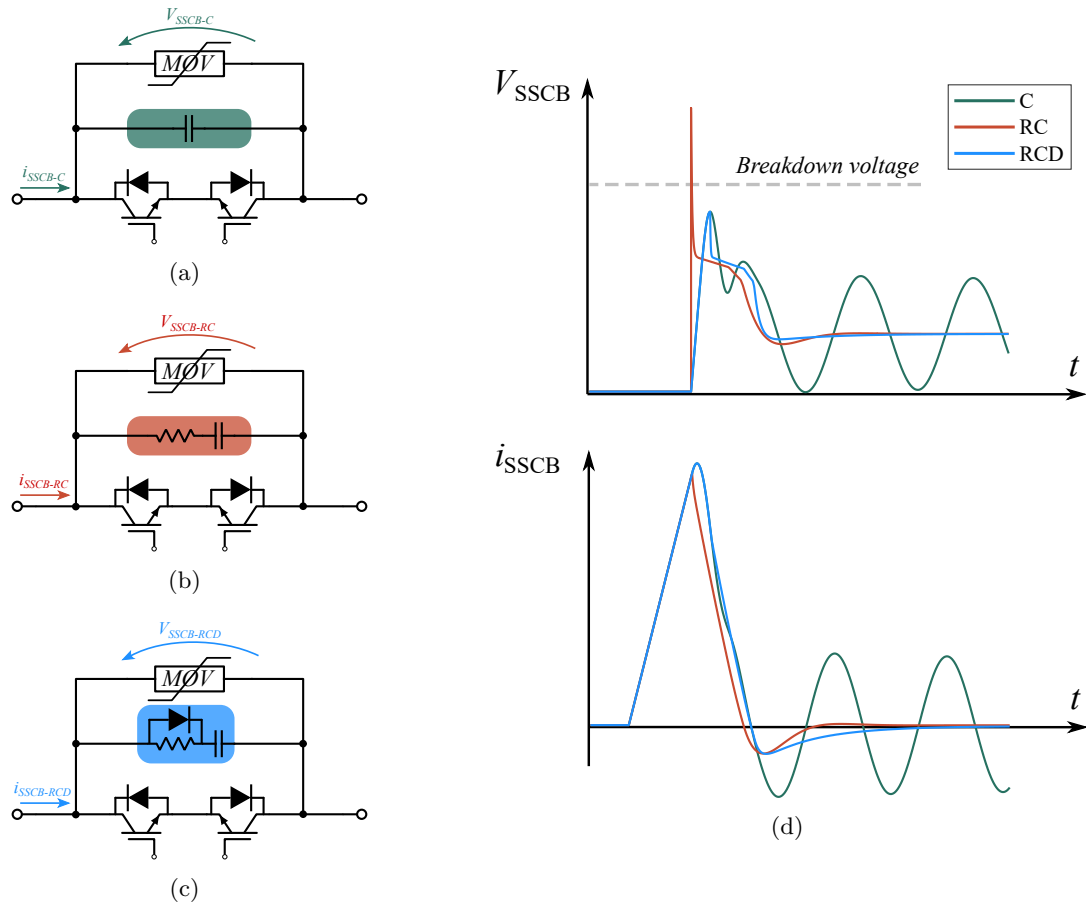

Figure 4.10 Examples of snubbers applicable for a SSCB with a MOV, being (a) C snubber, (b) RC snubber and (c) RCD snubber, and (d) their respective voltage and current waveforms when applying them to the SSCB.

As illustrated in Figure 4.10(a) and 4.10(d), the charging of the C snubber not only lowers the voltage rise rate, but also reduces the peak voltage across the semiconductor switches. However, the stored energy in the capacitor might cause oscillations due to the existing resonance between the line inductance and the proper capacitor. In addition, it may cause a high current discharge if the SSCB is back turned-on.

The additional series resistor of the RC snubber in Figure 4.10(b) can diminish these issues since it can damp the oscillations and limit the turn-on current of the SSCB after fault extinction. Nevertheless, when the SSCB turns-off, the voltage drop of the resistor manifests across the power semiconductors causing a high risk of exceeding the breakdown voltage of the power semiconductors.

Finally, the RC snubber is upgraded by adding a diode in parallel to the snubber resistor as illustrated in the RCD snubber in in Figure 4.10(c). This way, when the SSCB turns-off, the fault current flows through the diode so that the resistor-caused voltage spike is avoided and the capacitor charges and limit the voltage rise rate. In addition, the resistor not only damps the oscillations caused by the resonance of the line inductance and the snubber capacitor, but also limits the turn-on current of the SSCB. Therefore, even if the RCD snubber requires a higher number of components its described capabilities make it the most suitable option for SSCB applications.

4.2.4 Hybrid Circuit Breaker

The HCB is considered as a protection device which merges the best features of MCBs and SSCBs into a single device. In fact, as presented in Figure 4.11, the HCB makes use of a fast-mechanical switch in the main conduction branch so that high efficiency is achieved, and power semiconductors as main breaker branch so that faster interruption times than the ones of the MCB are achieved too. Therefore, this protection device aims to overcome the disadvantages presented by MCBs and SSCBs [37, 39, 126, 130].

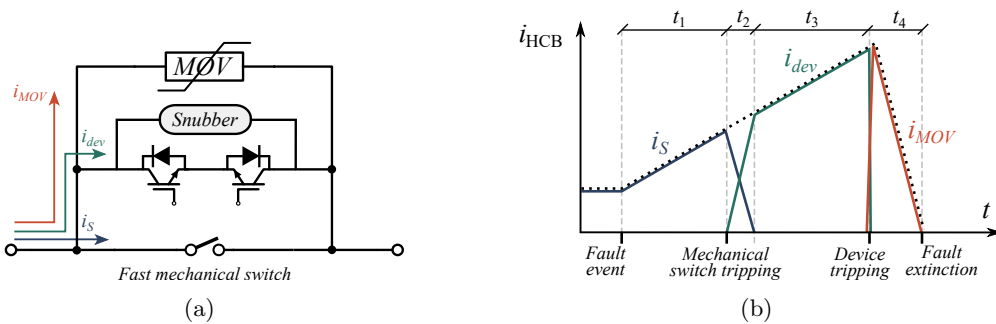**Figure 4.11** (a) Schematic of the HCB and (b) its typical current waveform during normal operation and fault clearing process.

During normal operating condition, the current flows through the main conduction branch containing a fast mechanical switch (see i_s in Figure 4.11). Thus, when the fault occurs (and it is detected), the main breaker branch is commanded to close, i.e. the power devices, and

the fast mechanical switch is commanded to open. This stage is represented as t_1 period in Figure 4.11(b). As soon as the fast mechanical switch opens, an arc is generated between its contacts which, due to the fact of establishing an arc voltage larger than the voltage drop of the power devices, naturally commutes the current from the main conduction branch to the main breaker branch in t_2 time. During t_3, the power devices of the main breaker keep conducting the fault current until the fast mechanical switch is able to block the full voltage and, thus, during t_4 the fault current is interrupted imitating the process of the SSCB explained in the previous section. Therefore, when the main breaker opens the current path is established through the snubber circuit, and consequently, the voltage across the HCB starts increasing until the MOV is energized. At this point, the voltage is clamped and the fault current is conducted through the MOV leading to its subsequent extinction [39, 130].

In this operating context, this type of HCB results to be high-efficient and reduces the cooling requirements compared to the SSCB because there are no power devices in the main conduction branch. Nevertheless, the mechanical switch opening time and the naturally current commutation process extend the overall fault clearing making the HCB slower than the pure SSCB [39, 126, 130]. Besides, few benefit will be obtained compared to the MCB in terms of component lifetime due to the arc generation when the fast mechanical switch is opened [17, 39].

It is worth to mention that the fault interruption process previously explained and corresponds to a naturally switched HCB which, typically, is valid in relatively LV applications. However, in the case of a HCB employed high voltage applications like the one in Figure 4.12, the total voltage drop of the series power devices in the main breaker branch can be increased up to hundreds of volts. Since this fact makes it complex for the arc voltage to increase to that level in less than a millisecond, a Load Commutation Switch (LCS) is typically employed.
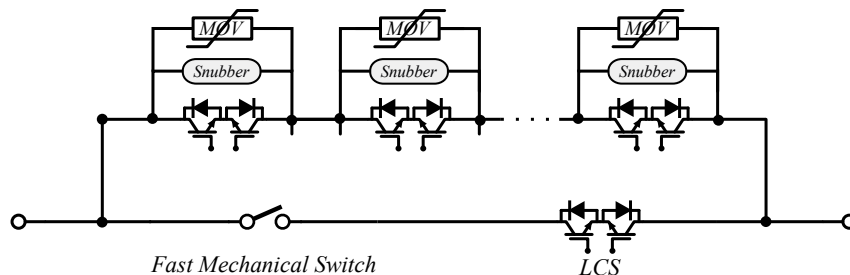
Figure 4.12 Example of the schematic of a typical HCB used for HV applications.

The LCS, typically formed by two LV rating anti-series power devices, is the one in charge to perform the current commutation from the main conduction branch to the main breaker. Thus, since the current of the main conduction branch is interrupted by the LCS, the fast mechanical switch starts to open without generating an arc, which results beneficial in terms of degradation of the mechanical contacts [39, 130]. Conversely, the LCS located in the main conduction branch implies the fact of current flowing power semiconductors during normal operation. Therefore, for the $270\,\mathrm{V_{DC}}$ aircraft applications, this HCB+LCS configuration is expected to present a similar efficiency characteristic and cooling requirement to the SSCB and, therefore, it might have no benefit with respect to the SSCB [17, 39, 130].

4.2.5 Fault Current Limiters

Aiming to prevent the damage caused by the short-circuit fault, a Fault Current Limiter (FCL) is considered to be an interesting option. Concretely, the FCL is used to limit the maximum fault current transient value when a fault occurs. Therefore, it should be designed to handle the significant amount of energy that must be dissipated during the limitation process [142, 143]. It must be remarked that a FCL cannot act as a circuit breaker, but it can reduce the fault current to an acceptable level so that a circuit breaker can operate in a faster and more reliable manner [144]. Typically, the FCL is divided into two main groups: *(1)* Non-Superconducting Fault Current Limiter (NSFCL) and Superconducting Fault Current Limiter (SFCL) [142].

Figure 4.13 presents three examples of typical NSFCLs. As presented in the figure, the NSFCLs are based on simple arrangements between passive elements and semiconductors. Thus, among the main benefits, a relatively low implementation effort and a low cost might be expected [142]. Nevertheless, one of the major drawbacks is the fact that even the simplest configuration uses power semiconductors during normal operation and, therefore, generates conduction power losses. Thus, few benefits with respect to the previously described SSCB can be expected from NSFCLs in terms of efficiency, volume and, depending on the topology employed, even cost.

(a)   (b)   (c)
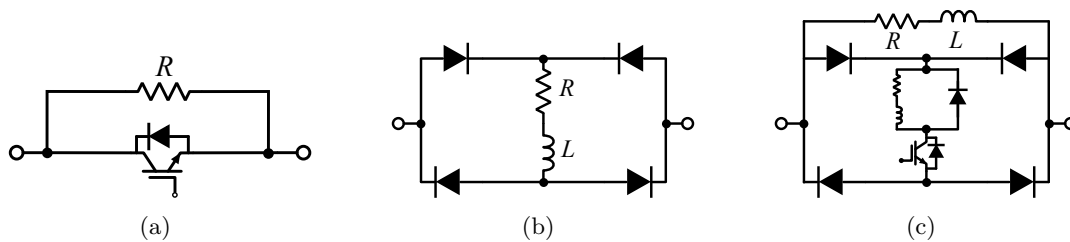
Figure 4.13 Examples of NSFCLs, being (a) the Series Dynamic Braking Resistor (SDBR) topology, (b) the DC-Link Fault Current Limiter (DFCL), and (c) the Bridge-Type Fault Current Limiter (BFCL).

A completely different approach is presented by SFCLs in terms of efficiency and power losses. In fact, SFCLs are featured for: *(1)* presenting a negligible conduction resistance during normal operation, which is translated into a $\approx 100\,\%$ efficiency, and *(2)* presenting an immense resistance during faulty conditions [142, 143]. In addition, due to the inherent physical characteristics of the superconductor material, the SFCL is allows to quickly limit the fault current and thus reduce the stress on circuit breaker considerably [143]. Among the existing SFCL topologies, the most simple and commonly studied topologies are the Resistive SFCL (R-SFCL), The inductive Shielded SFCL (I-SFCL) and the Saturated Iron Core SFCL (SI-SFCL), which are presented in Figure 4.14 [132, 142–144].

(a)   (b)   (c)
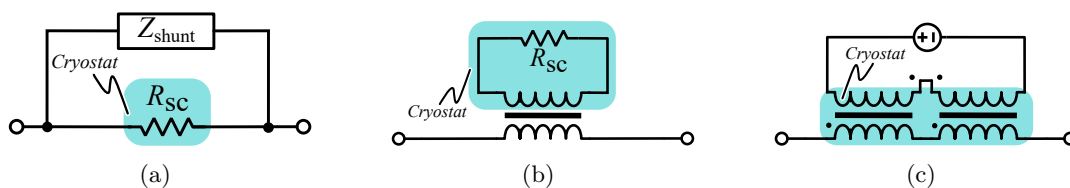
Figure 4.14 Schematic of SFCL topologies, being (a) R-SFCL, (b) I-SFCL and (c) SI-SFCL.

In the case of the R-SFCL, depicted in Figure 4.14(a), the conduction-resistance of the superconductor, R_{sc}, results negligible during normal operation. This negligible resistance, though, increases quickly after the short-circuit fault current exceeds the critical current of the superconductor, which is then quenched [143].

The I-SFCL presented in Figure 4.14(b), on its behalf, is based on combining the transformer operation with superconducting elements [142, 143]. It has a conventional primary winding, w_1, and a secondary winding, w_2, connected to a superconducting resistance. During normal operation, the flux in the primary side can be neglected because the induced current in the secondary side is lower than the critical current of the resistive superconducting element. Note that, unlike in the R-SFCL topology, a residual impedance comprising resistance of the primary winding, R_{w1}, and the parasitic inductance, L_{w1}, exist [143]. Therefore, a certain amount of power losses can be expected during its normal operation [142]. When the short circuit occurs, the current through primary side of I-SFCL increases and, as a result, a current through the superconducting element in the secondary side starts to flow and it is quenched. The superconducting resistance is transferred to the primary winding by the factor of $k_2 = (w_1/w_2)^2$ and, consequently, the impedance of I-SFCL is increased, limiting the fault current [143].

Finally, the SI-SFCL in Figure 4.14(c) takes advantage of the magnetic properties of the iron so that it can change the reactance of the power line [143]. When operating in normal conditions, the bias current in the coils saturates the core and both iron cores present a low permeability. Hence, the primary winding behaves as an air core inductor and presents a relatively small RL impedance. Therefore, a certain amount of power losses can also be expected during the normal operation of SI-SFCL [142]. When the short-circuit occurs, the iron core desaturates and the permeability as well as the presented impedance increase, limiting the fault current [143].

Due to the fact that a high efficiency is demanded in aircraft applications, the I-SFCL and the SI-SFCL result no longer interesting in this work because of the expected power losses dissipated during normal operation. Thus, the R-SFCL, which is becoming a more mature technology, could result a potential applicable option if its inherent "ideal" efficiency and fast-increasing-resistance benefits could be merged into a circuit breaker functionality such as the Superconducting-Hybrid Circuit Breaker (S-HCB) presented in Figure 4.15 [132]. This way, the superconductor material could be used as a natural commutation switch to conduct the current from a mechanical switch branch to the main semiconductor branch as it is done by the arc-based HCB [132].
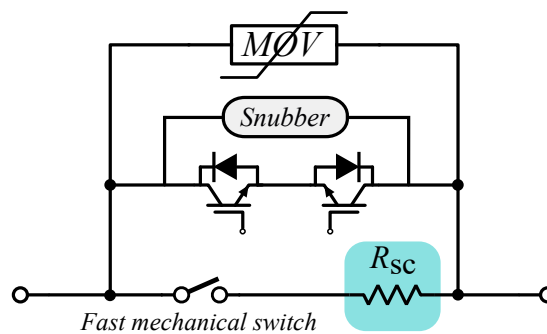

Figure 4.15 Superconducting Hybrid Circuit Breaker example.

4.2.6   Discussion on the Protection Systems for the EPS Subsystems

The presented literature review throughout this section describes the different protection alternatives that might be employed in a DC distribution grid. Although some of them, like the fuses or MCBs, are considered as mature technology, other technologies like the SFCLs are still going through an evolution process. Moreover, each protection device has its own advantages and disadvantages and, hence, a discussion among them is required when considering in a concrete application such as the low impedance DC distribution network expected in future MEA. In this regard, Table 4.1 summarizes the critical features of the previously described protection devices aiming to provide a discussion in the following.

Table 4.1 Summary of the main characteristics of the potential protection devices.

	Fuse	**MCB**	**SSCB**	**HCB**	**S-HCB**
Power Losses	Negligible	Negligible	High	Negligible	Negligible
Operating Speed	$< 0.1\,\mathrm{ms}$	$> 1\,\mathrm{ms}$	$< 0.1\,\mathrm{ms}$	$< 1\,\mathrm{ms}$	$< 1\,\mathrm{ms}$
Remote Control	No	Might have	Yes	Yes	Yes
Size	Very Small	Small-Medium	Large	Large	Very Large
Weight	Very Low	Low	High	Medium	Very high
Cost	Low	Low	High	High	Very high
Expected lifetime	Long	Short	Long	Long	Unknown
Maintenance	Yes	Yes	No	Yes	Yes
Others	- Single use device. - Not able to distinguish between transient and permanent fault.	- Generates an arc when opening	- Bulky heatsink required (might be smaller with WBG).	- Generates an arc when opening	- Additional implementation effort and energy are required for cryogenics.

As previously mentioned, the MCBs represent the conventional protection devices employed in the AC distribution-based aircraft EPS [10, 128]. Due to their simplicity, low cost and "*ideal*" efficiency, i.e. $\approx 100\,\%$, research efforts have been done to integrate these protection devices into the DC EPSs. However, the fast increase of the fault current and the inherent high opening time of the MCBs, make these protection devices unsuitable for HVDC applications [10, 39, 128, 130]. Moreover, it is more difficult to extinguish the formed arc when opening and, as a consequence, it is expected for the useful life of the MCBs to be worsened.

During the last decades, several MCB models have been developed to improve some of the MCB structure related drawbacks. Among others, AFCB for arc fault detection, the RCCB for solving the lack of remote control, or vacuum interrupters to avoid the risk of explosion due to the generated arc when interrupting the fault current [10, 39, 128, 130]. However, while these improvements are positively valued for AC protection, research efforts are being routed towards other alternatives for DC EPS protection [130]. Thus, MCBs will no longer be considered in this work as protection devices to be employed in the DC EPS.

Following the lead of maturity, low weight, low cost and simplicity features, fast DC fuses

emerge as a promising solution for DC EPS protection [10, 17, 130, 133, 135]. Since the time (or i^2t) required to blow a fast fuse results to be minimal, this type of protection device results ideal for low impedance DC networks in which the fault current increases at an extraordinary speed [39, 130, 145]. Thus, fuse is considered in this work as a potential option to be implemented in an aircraft EPS in which sensitive elements like converters, feeders, batteries and loads want to be protected.

One of the main drawbacks of the fuse is that it can only be used once and, hence, it has to be replaced after it is blown [10, 39, 130, 145]. The fact of being a single-use device, however, might not be considered as an actual issue since it is expected that the aircraft will have to pass a ground-check after a fault occurrence [63]. Contrarily, being a single-use device prohibits the possibility for reconfiguration, which it is considered as crucial for ensuring a high reliability of supply [130]. This idea makes the fuse useful for protecting generating sources or loads which, indeed, after failure will not be rearmed, but it also makes the fuse unsuitable for bus-tie operation in which the rearming and reconfiguration possibilities result interesting. Thus, other alternatives should be evaluated as bus-tie protection device.

In this regard, the SSCBs, which have gained popularity for aerospace applications, are a promising solution to overcome fuse limitations [21, 42, 128]. They can achieve similar or even faster fault interrupting operating speeds than fuses with the additional feature of rearming capability [39, 130]. Therefore, the SSCBs are also faster operating devices than MCBs and, since the current interruption is made by semiconductors switching, no arc is generated when interrupting the fault current, which leads to an increasingly long lifetime of the devices [21]. In fact, using power semiconductor devices provides the SSCB with additional benefits such as remote control, programming an i^2t curve as the one of MCBs and, thanks to the constant development of new power semiconductor devices like SiC MOSFET, a compact SSCB design and a faster operation [15, 21, 39, 129, 130].

On the negative side, employing semiconductor devices in the conduction branch of the circuit breakers implies assuming power losses during normal operation (on-state conduction). Thus, a relatively low efficiency and bulky cooling system must be assumed when employing a SSCB [39, 130]. Note that these features can be improved by oversizing the employed semiconductor device owing to a higher device cost, especially if WBG devices are implemented. The increased device cost but reduced weight, though, could result beneficial in terms of overall SSCB cost due to the fact that an extra kilogram supposes around $\$\,4500$ per year for the airlines [3, 4, 11].

In addition to the power losses drawback, it has to be taken into account that the power semiconductors are also voltage sensitive devices. Thus, due to the induced voltage that appears across the stray inductance when energizing the energy absorbing branch, voltage rating of the semiconductors should be chosen significantly higher that the DC bus voltage, which indeed, increases the SSCB costs [39].

Considering the SSCB drawbacks, the HCB results an interesting alternative to increase the distribution efficiency in the EPS locations or feeders in which the SSCB will constantly be handling power. In fact, the naturally switched HCBs have negligible conduction losses during normal operation, shorter operating times than the MCBs, and do not require special

cooling equipment as SSCBs [130]. Nevertheless, several research challenges have to be faced to enhance the implementation of HCBs in the aircraft EPS [39, 130, 132]. Among others, the more remarkable ones are considered to be the costs, which could be similar to the SSCB, and the reduction of the clearing time, which is downgraded due to the opening of the mechanical switch employed. The latter issue might be overcome by employing a S-HCB, but the protection device costs will be surged and, with the up-to-date volume and weight characteristics of the state-of-art technology in superconductors, the power density of the overall protection device will be diminished [142].

To sum up, fuses and SSCBs are considered in this work as the currently most promising solutions for MEA applications. Concretely, the high efficiency, simplicity, economical, and operating speed features make fuses to be appropriate devices for protecting the DC EPS subsystems that are constantly generating/demanding power such as the power converters of the $2L_{st}$ active modular architecture, feeders and loads. The SSCBs should also be evaluated to protect these systems but they might result low-efficient devices if no current overrating is assumed. Thus, it is preferred to employ SSCBs as bus-tie switches which, ideally, will no conduct current during normal operations.

It should be taken into account, though, that no galvanic isolation is offered by fuses (unless when they are already blown) and SSCBs. Therefore, an additional element has to be assumed in series with these protection devices, that is, a MCB or a relay which allows the connection and disconnection of the subsystem to be protected. In this context, considering that the EPS generation sources (both SGs and batteries) and loads are interfaced by active power converters, either AC/DC, DC/AC or DC/DC, the active power semiconductors could be switched-off so that no current has to be interrupted. This way, a simple relay could be employed in series with the fuse or the SSCB for providing galvanic isolation during normal operation [126, 130].

4.3 Protection of the $2L_{st}$ Active Modular Architecture

4.3.1 Simplified $2L_{st}$ Architecture Model for Short-Circuit Simulations

As it has been discussed, both fuse and SSCB protection devices look suitable for protecting the active power converters of the $2L_{st}$ architecture. Aiming to identify the most suitable solution, it becomes necessary to model the fault behavior of the $2L_{st}$ architecture as well as the fault clearing processes of the protection devices. This way, not only to the benefits and drawbacks of the fuse and the SSCB during a converter fault operation can be analyzed, but also to a deeper understanding about the DC fault severity in aircraft applications can be provided [128, 136, 138].

According to the DC fault characteristics described at the beginning of this chapter, the DC fault is mainly featured by two main responses: *(1)* the fast discharge of the DC-link capacitors, and the *(2)* steady-state fault current fed by the power generating sources. Considering that the first response can already damage the EPS components before achieving the steady-state fault current, it is expected for the protection devices to operate during this first transient and suppress the quick fault current enlargement before causing catastrophic damage. This concept,

indeed, permits the possibility of simplifying the 2L$_{st}$ active modular architecture defined in the preceding chapter as explained in the following.

On the one hand, focusing on the first DC fault transient, i.e. the DC-link capacitor discharge, means that the SG AC side grid and the components related to the simulation of AC voltages and currents can be neglected, being, the SG, the AC passive elements, and cables. On the other hand, as depicted in Figure 4.16(a), if normal operating conditions are assumed, only 8 out of the 11 converters which form the 2L$_{st}$ active modular architecture are transferring active power to the DC EPS. This fact permits to avoid the simulation of the 3 STATCOMs and reduce the simulation effort. Consequently, the 2L$_{st}$ architecture schema can be simplified to the equivalent circuit presented in Figure 4.16(b) in which the element to be considered are the active rectifiers connected to the busbar, their protection devices and the parasitic impedances related to the proper busbar and the busbar-converter interconnection [146].

(a)

(b)
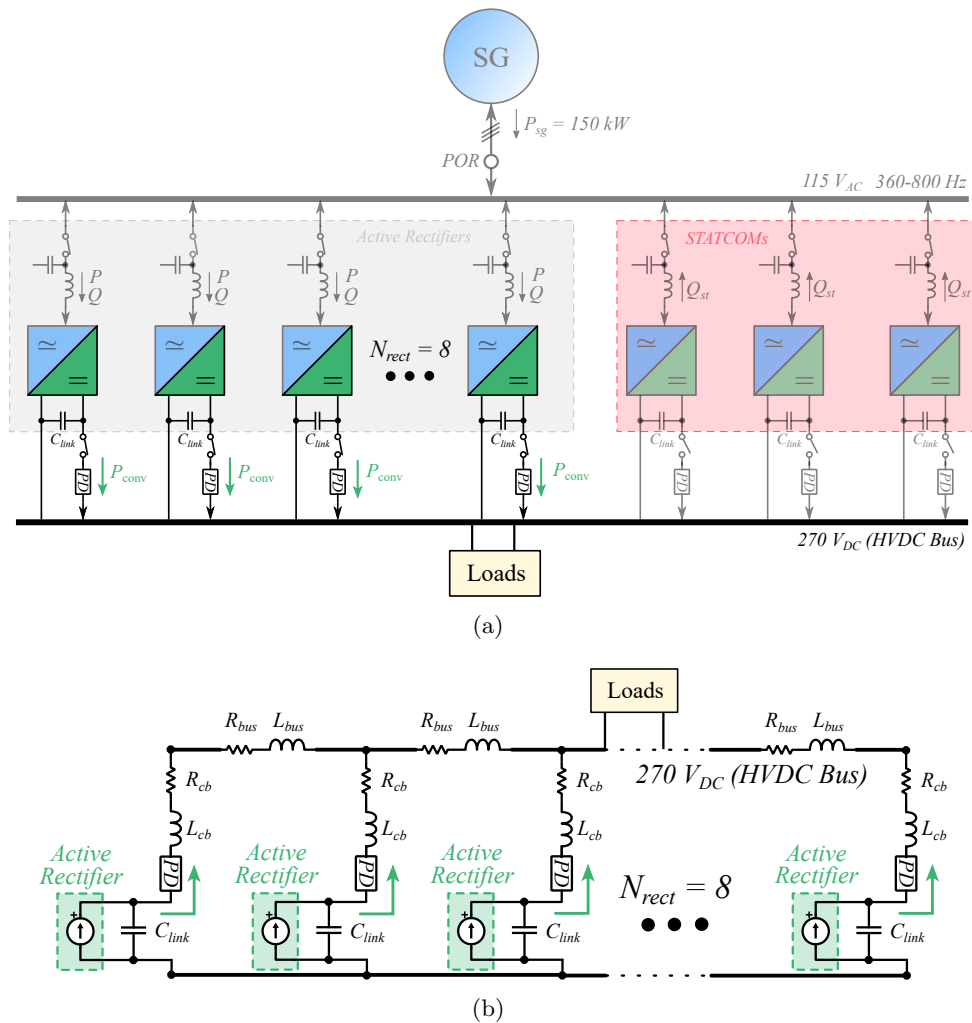
Figure 4.16 Schematic of the 2L$_{st}$ active modular architecture with the DC-side protection devices and (b) simplified model of the 2L$_{st}$ architecture considering the parasitic elements.

Therefore, the equivalent circuit is presented as a series-parallel RLC impedance combination related to the parasitic impedances, the DC-link capacitors of the active rectifiers and eight DC current sources which represent the active power feeding of the active rectifiers into the DC

EPS [21, 146, 147]. The passive elements which make the model up are listed in Table 4.2 below.

Table 4.2 Summary of the characteristics related to active PFC buck-type topologies.

Parameter	Value
Busbar stray resistance, R_{bus}	$83\,\mu\Omega$
Busbar stray inductance, L_{bus}	$55\,\text{nH}$
Stray resistance of the connection to the bus, R_{cb}	$30\,\mu\Omega$
Stray inductance of the connection to the bus, L_{cb}	$500\,\text{nH}$
Converter DC-link capacitance, C_{link}	$76\,\mu\text{F}$

Concretely, R_{bus} and L_{bus} parameters correspond, respectively, to experimentally obtained resistance and stray inductance busbar values of other project which are used in this work as reference values. Similarly, R_{cb} and L_{cb} represent an approximation of the experimentally obtained resistance and the stray inductance of the performed connections between the converters and the busbar. Additionally, aiming to simplify the simulation a single resistor is included for representing a $150\,\text{kW}$ load, that is the power to be fed by a 2L_{st} active modular architecture.

It is worth to mention that the C_{link} represents the DC bus capacitor value designed in the previous chapter for the 2L_{st} converters. However, it has been increased from $53\,\mu\text{F}$ to $76\,\mu\text{F}$ to provide a decoupling effect between the converter and the HVDC bus. Note that, due to the switching of the power converters, overvoltage shoots occur due to the stray inductances in the DC bus which can lead to the power device destruction [148]. In this regard, the bus capacitor is designed to decouple the switching loop from the DC stray inductances and, thus, take over the overshoot caused by the stray inductances. According to [148], the decoupling capacitor, C_{dec}, is calculated as,

$$C_{\text{link}} \geq C_{\text{dec}} = \frac{L_{\sigma} \cdot i_{\text{DC}}^2}{\Delta V_{\text{DC}}^2} = \frac{(L_{\text{cb}} + L_{\text{bus}}) \cdot i_{\text{dc}}^2}{\Delta V_{\text{DC}}^2} = 75.54\,\mu\text{F} \approx 76\,\mu\text{F} \tag{4.1}$$

where L_{σ} represents the stray inductance causing the overshoot (being in this case the sum of L_{cb} and L_{bus}), i_{DC} corresponds to the DC converter current when operating at $18.75\,\text{kW}$ nominal power, and ΔV_{DC} refers to the $2.22\,\% \cdot V_{\text{DC}}$ voltage ripple permitted in the application according to aviation standards [29, 62].

In order to analyze the architecture behavior when a converter fault occurs, converter 1 is short-circuited without any protection devices considered (see Figure 4.17(a)). As depicted in Figure 4.17(b), as soon as the fault occurs the voltages and currents of the RLC circuit start to resonate. Particularly, the bus voltages oscillate around zero, which is the short-circuit voltage, and the currents keep oscillating towards the steady-state fault current.

Special attention should be paid to the zoomed fault results in Figure 4.17(c) which show how the C_{link} voltage level of each converter decays to zero in approximately $30\,\mu\text{s}$, except for the short-circuited converter whose voltage decays to zero instantaneously. Note that the DC bus voltage decay is translated into a high short-circuit current which, for the assumed 2L_{st}

architecture parameters, supposes a peak fault current of approximately 7300 A. Therefore, the results reveal that it is desired to employ a protection device which operates before the fault time reaches 30 μs. In this context, the fuse and SSCB models are described in the following so that, in a latter simulation, their effectiveness for protecting the 2L$_{st}$ architecture converters can be analyzed [134, 135].
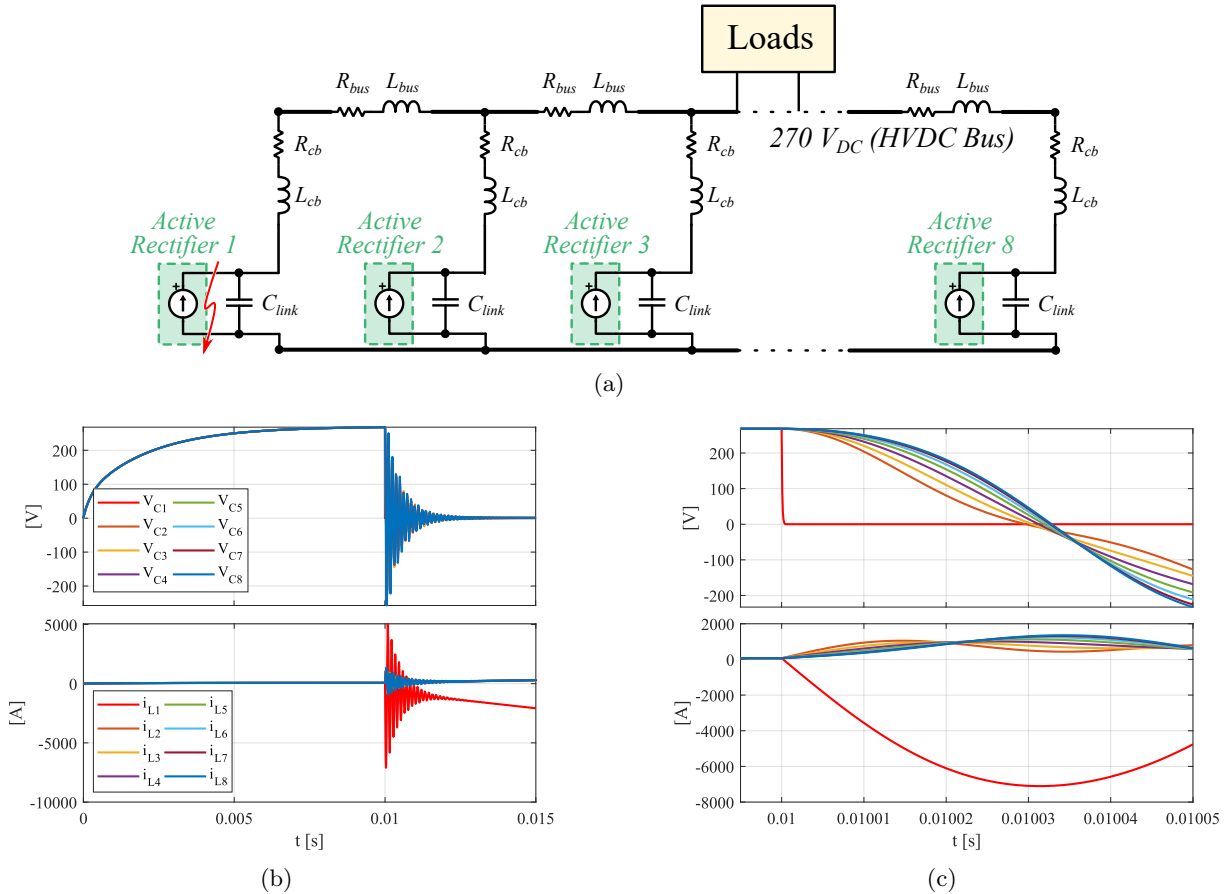
Figure 4.17 (a) Simplified schematic of the 2L$_{st}$ architecture with a fault occurring in converter 1. (b) Voltage and current waveforms before and after the fault event and (c) zoomed waveforms.

4.3.2 Fuse Model

The fuse performance is featured by two main time periods: the pre-arcing or melting time, and the arcing time. The difference between these two periods in terms of fuse voltage, V_{fuse}, and fuse current, i_{fuse}, waveforms is graphically shown in Figure 4.18(a) for a typical fuse blowing [133–135]. During the melting time, which starts when the fuse rated current is exceeded, the voltage across the fuse is maintained approximately at zero volts while the current keeps increasing until the conducting element melts and, thus, the melting time is ended. At that instant, however, the current is not instantaneously turned to zero, but a relatively high voltage arc is created which becomes into an increasing resistance into the current path until the current is extinguished and, hence, the fault is cleared.

In this context, the fuse behavior can be modeled with the two parallel branch-based equiva-

lent circuit presented in Figure 4.18(b) [134,135]. The branch on the top, used during the normal operation and melting time, is defined by a normally closed ideal switch, S_{f1}, whose resistance is considered as negligible. The branch on the bottom is defined by a normally opened ideal switch, S_{f2}, in series with a resistor, R_{arc}, and a capacitor, C_{arc}, which are used to emulate the arcing time behavior of the fuse. In addition, an ammeter and an algorithm are employed in the model to constantly measure the current flowing through the fuse and switch the operating branches of the fuse model. Thus, the fuse state can be switched from normal or melting operating state ($S_{f1} = 1$ and $S_{f2} = 0$) to arcing operating state ($S_{f1} = 0$ and $S_{f2} = 1$) and finally to a blown fuse state ($S_{f1} = 0$ and $S_{f2} = 0$). Note that the melting process as well as R_{arc} and C_{arc} parameters have to be characterized for representing the melting, arcing and clearing behavior of the fuse.
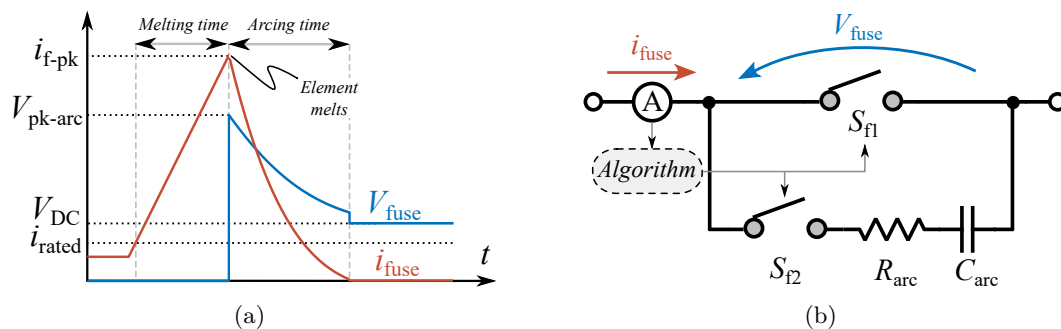
Figure 4.18 (a) Typical waveforms of the fuse operation and (b) the modeled fuse equivalent circuit.

Although the fuse behavior and its related parameters could be experimentally characterized, the timeless effort that requires this process leads to energy-based modeling procedures. The energy-based procedures, already employed and experimentally validated in [134, 135], provide the easiness of modeling a fuse by means of its datasheet parameters. In this work, the following fuse-related DC parameters are used from the datasheet for the fuse selection and characterization [133–135, 149]:

- **Rated voltage, V_{rated}:** Represents the maximum voltage at which the fuse is designed to operate. It is worth to mention that, even if this parameter is not considered for the fuse characterization, it has to be ensured that the voltage rating of the fuse is larger than the application voltage. This way the formation of arcs between the fuse terminals due to possible overvoltages is avoided when the fuse is already blown.

- **Current breaking capacity:** Refers to the maximum fault current that a fuse can clear. Hence, in order to provide satisfactory protection by the fuse, its current breaking capacity should be larger than the available fault current of the system.

- **Rated current, i_{rated}, and the time-current (t-i) curve:** The i_{rated} of the fuse is defined as the DC steady-state current that can be conducted through the fuse. Note that the melting process starts as soon as $i_{fuse} > i_{rated}$. Thus, for the cases in which a possible overloading condition is expected (such as a $2L_{st}$ converter failure), an overrating of the fuse is selected assuming a $\approx 20 - 30\%$ current margin so that the fuse features are not worsened, for instance, a $100\,A$ rated fuse for $70\,A$ nominal DC current.

In this context, the melting time required for a fuse to blow is described graphically by the

time-current (t-i) curve in the datasheet. However, this datasheet curve is tested at certain laboratory conditions and, due to the fact that the fuses are thermally sensitive protection devices, additional parameters such as the ambient temperature or the altitude that cause a derating of the t-i curve of the fuse should be considered [137, 150]. An example of this concept is presented in Figure 4.19(a) below.
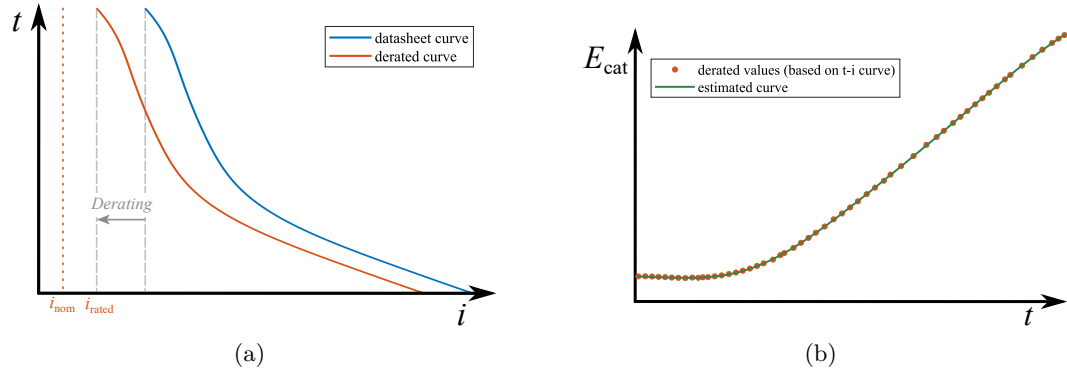

(a)   (b)

Figure 4.19 Examples of (a) the fuse t-i curve of a datasheet and its derating, and (b) the estimated E_{cat}-t curve for a fuse during melting operation.

- **Melting i^{2}t or catalog energy, E_{cat}:** Expresses the heat energy dissipated by a fuse from the instant in which when the rating current is exceeded up to the time in which the fuse melts. Although the datasheet provides the minimum melting i^{2}t value, a higher precision of the E_{cat} for different fault times can be obtained if the time current curve is transformed to a E_{cat}-time curve. This way, from the previously derated t-i curve a high number of points is selected and, with each of them, the corresponding E_{cat} value is calculated as,

$$E_{\text{cat}}(t_{\text{melt}}) = i_{\text{f}}^2 \cdot t_{\text{melt}} \tag{4.2}$$

where t_{melt} represents the time required to melt the fuse for a specific fault current value, i_{f}. The result of this calculation (for several points) is represented graphically in Figure 4.19(b) by means of a E_{cat}-t dotted line curve. Note that the minimum E_{cat} value (if no derating is applied) corresponds to the "*Melting i^{2}t*" energy typically described in the fuse datasheet.

In addition, in order to provide the fuse model algorithm with a simpler E_{cat} calculation based on the simulation fault time, t_{f}, a curve-fitting calculation is applied by means of the Matlab curve fitting application [134]. Thus,

$$\log(E_{\text{cat}}(t_{\text{melt}})) = p_1 \cdot (\log(t_{\text{f}}))^9 + p_2 \cdot (\log(t_{\text{f}}))^8 + p_3 \cdot (\log(t_{\text{f}}))^7 + p_4 \cdot (\log(t_{\text{f}}))^6 + p_5 \cdot (\log(t_{\text{f}}))^5$$
$$+ p_6 \cdot (\log(t_{\text{f}}))^4 + p_7 \cdot (\log(t_{\text{f}}))^3 + p_8 \cdot (\log(t_{\text{f}}))^2 + p_9 \cdot (\log(t_{\text{f}})) + p_{10} \tag{4.3}$$

where $p_1, p_2, \ldots p_{10}$ parameters correspond to the curve fitting values given by Matlab. It is worth to mention that a 9$^{\text{th}}$ order logarithmic polynomial regression model is used because it presents a lower approximation error than other regression models like linear, (no-logarithmic) polynomial or Gaussian. The result of (4.3) is also presented in Figure 4.19(b), where a good agreement with the datasheet-based values of (4.2) is observed. Note that for the estimated curve, $E_{\text{cat}} = 10^{(\log(E_{\text{cat}}))}$ is applied.

- **Total clearing i²t energy, E_{clear}:** Refers to the maximum let-through i²t energy that is withstood by the fuse to extinguish the fault. Therefore, it is expected for the fuse E_{clear} to be smaller than the fusing i²t of the device to be protected, for example the semiconductor fusing i²t or the cable fusing i²t. It is worth to mention that this value is typically given in the fuse datasheet when tested at the device rated voltage. However, in order to scale the E_{clear} of the rated voltage to the application voltage, a correction factor, F_{clear}, of the datasheet is applied which expresses the derating of the E_{clear} with respect to the application voltage, i.e. V_{DC}. Thus,

$$E_{\text{clear}}\left(V_{\text{DC}}\right) = E_{\text{clear}}\left(V_{\text{rated}}\right) \cdot F_{\text{clear}} \tag{4.4}$$

- **Peak Arc Voltage ($V_{\text{pk}-\text{arc}}$) curve:** At the beginning of the arcing period, the resistance of the arc produces an instantaneous peak voltage that appears across the fuse terminals. This $V_{\text{pk}-\text{arc}}$ value is typically presented by the manufacturers as a peak arc voltage curve, that is the $V_{\text{pk}-\text{arc}}$ which might be generated by the fuse at different operating voltages below the V_{rated} of the fuse.

Bearing in mind the last four features of the fuse datasheet, the fuse model is characterized by means of a two-step simulation process described in the following [133–135]:

Step 1: On the first step, the fault is simulated so that the i_{fuse}, which is monitored by the ammeter in series with the fuse circuit, starts to increase through the S_{f1} branch. Here, it is assumed that the fuse resistance does not vary with the increasing fuse temperature. Once the i_{rated} is exceeded, the melting energy, E_{melt}, is calculated as

$$E_{\text{melt}} = \int_{t_0}^{t_{\text{f}}} i_{\text{f}}^2 \cdot dt \;\;, \tag{4.5}$$

being t_0 and t_{f} the initial time at which $i_{\text{f}} > i_{\text{rated}}$ and the fault time at which the integral calculation stops, respectively. Thus, it is considered that the fuse melts when, for a given t_{f}, the accumulated E_{melt} is higher than the estimated $E_{\text{cat}}\left(t_{\text{f}}\right)$ in (4.2). At this point, in which S_{f1} is turned-off and S_{f2} turned-on, the melting time is ended and the peak fault current value, $i_{\text{f}-\text{pk}}$, is saved for the second simulation step (see Figure 4.18(a)).

It is worth to mention that, for a short duration faulty condition in which E_{melt} does not surpass E_{cat}, the E_{melt} value is held for a certain amount of time and, if no increase in E_{melt} is perceived, its value is instantaneously reduced to zero. This could be the situation of a short overloading condition in which it is not expected the fuse blowing, for example.

Step 2: On the second step, which corresponds to the arcing period behavior, the R_{arc} and C_{arc} are defined. Note that, when this step starts S_{f1} is turned-off and S_{f2} turned-on and, hence, the time dependent generated arc voltage across the fuse, $v_{\text{arc}}(t_{\text{arc}})$, can be calculated as,

$$v_{\text{arc}}(t_{\text{arc}}) = v_{R_{\text{arc}}}(t_{\text{arc}}) \cdot v_{C_{\text{arc}}}(t_{\text{arc}}) \tag{4.6}$$

where t_{arc} is the arcing time. Since the peak arc voltage value, V_{pk-arc}, occurs at the beginning of the arcing period, in which $v_{C_{arc}}(t_{arc} = 0) = 0$ and $i_f(t_{arc} = 0) = i_{f-pk}$, the R_{arc} can be calculated according to Ohm's Law, the datasheet V_{pk-arc} and i_{f-pk}. Therefore,

$$R_{arc} = \frac{V_{pk-arc}}{i_{f-pk}} \quad . \tag{4.7}$$

Moreover, since the fuse arc period behavior is modeled as an RC branch, the current flowing through the fuse during this period can be described as,

$$i_{arc} = i_{f-pk} \cdot e^{-\frac{t_{arc}}{R_{arc} \cdot C_{arc}}} \quad . \tag{4.8}$$

Consequently, the i²t energy during the arc period, E_{arc}, can be calculated as,

$$E_{arc} = \int_0^{t_{arc}} i_{arc}^2 \cdot dt = \frac{R_{arc} \cdot C_{arc} \cdot i_{f-pk}^2}{2} \quad . \tag{4.9}$$

Therefore,

$$C_{arc} = \frac{2 \cdot E_{arc}}{R_{arc} \cdot i_{f-pk}^2} = \frac{2 \cdot (E_{clear} - E_{melt})}{R_{arc} \cdot i_{f-pk}^2} \quad . \tag{4.10}$$

To end with the second step, once the current is extinguished during the arc period, both S_{f1} and S_{f2} are opened and, hence, the fuse is considered as blown.

A key conclusion of this two-step process is that it is not only used for modeling the fuse, but also for operating it. Simply put, the i_{fuse} is constantly measured by means of the ammeter located in the main circuit and, if $i_{fuse} > i_{rated}$, the algorithm employs the two-step process for operating the fuse. A graphical representation of the two-step process and, hence, the algorithm operation is presented in Figure 4.20 below.
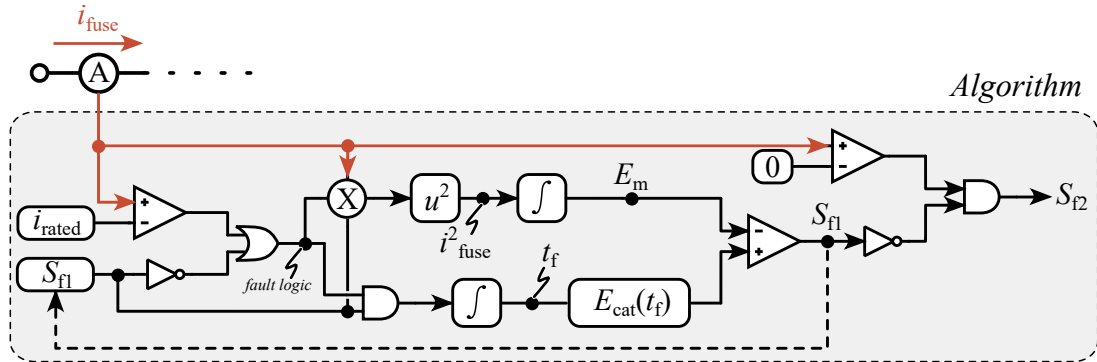
Figure 4.20 Employed algorithm for fuse simulation based on the two-stage process.

4.3.3 Solid-State Circuit Breaker Model and Design Criterion

Considering the bidirectional power flow of the 2L$_{st}$ architecture converters, Figure 4.21(a) below presents the schematic of the proposed SSCB model to be employed in this work. As shown in the figure, the SSCB is composed by two transistors in anti-series, each of them with an anti-parallel diode, an energy absorbing branch containing a MOV for fault current extinction

and a RCD snubber circuit branch for reducing the voltage stress of the transistors during fault current interruption [41, 126].

(a)

(b)

(c)

(d)

(e)

(f)
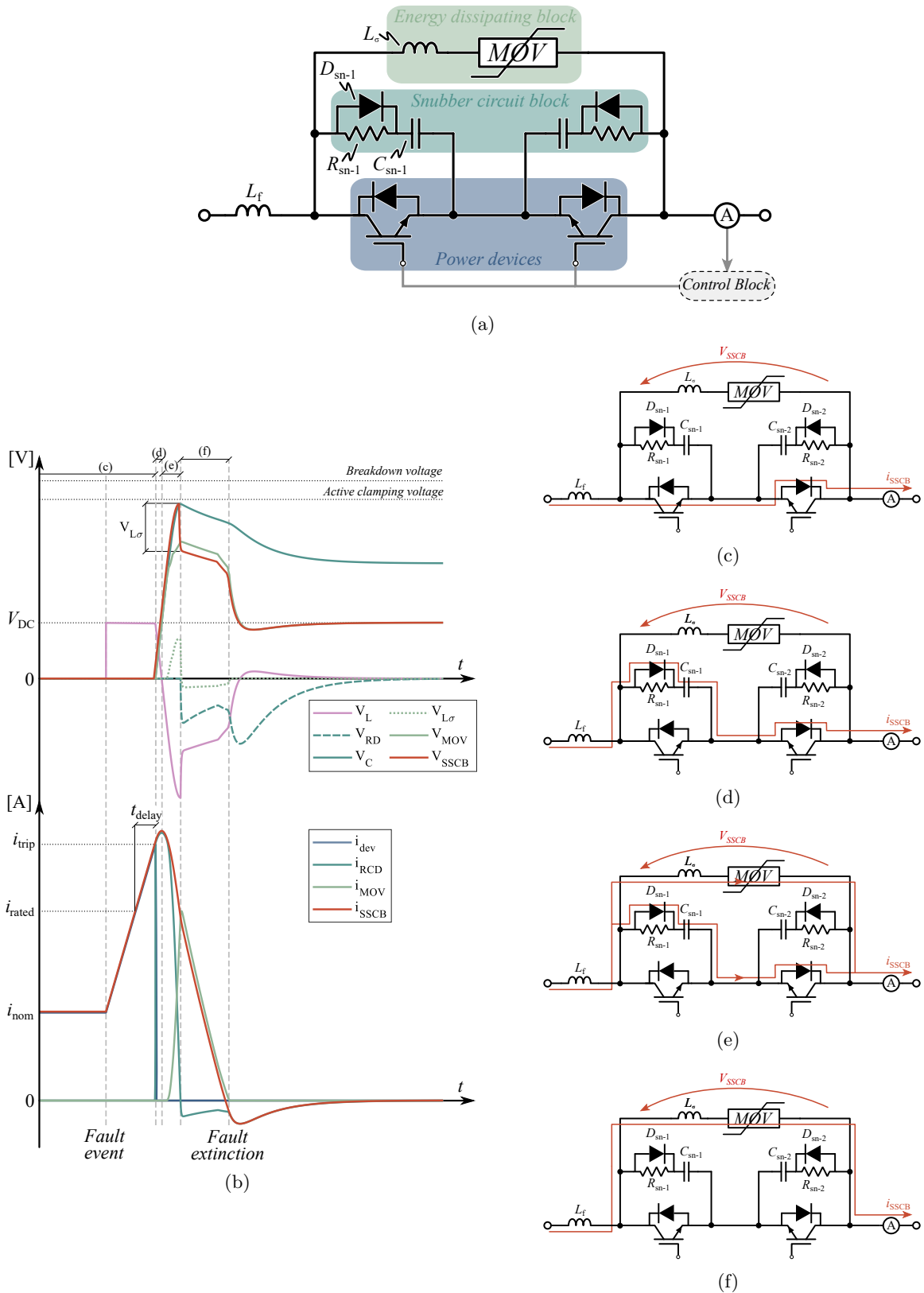
Figure 4.21 (a) Schematic of the employed SSCB model and (b) its operating current and voltage waveforms representative of the current path throughout the SSCB during (c) normal operation and fault operation before tripping, (d) post-tripping first transient, (e) post-tripping second transient and (f) fault current extinction.

As depicted in Figure 4.21(a), the SSCB model is divided into 4 main blocks which are described in the following. Note that current and voltage waveforms of the SSCB during the fault clearing process are graphically described in Figure 4.21(b) and that the current paths during this process are represented in Figure 4.21(c)-4.21(f).

- **Power devices:** It includes the power devices of the SSCB main conduction branch. Therefore, these power devices conduct the current during normal operation and while the current is increasing after the fault occurs (see Figure 4.21(b) and 4.21(c)).

 It is worth to mention that if a high-precision SSCB simulation is targeted, the physical model of these power devices should be considered so that the turn-off process is modeled. Aiming to simplify the SSCB model and reduce the simulation time, ideal power devices are assumed here [136,138]. This way, the selection of the power device to be employed is left out of the simulation and a comparison among different power semiconductors can be done by means of an efficiency-weight-cost analysis at the end of the SSCB design process.

- **Control Block:** This block is used to model the control of the turn-on and turn-off signals of the power devices. For that purpose, an ammeter is located at one of the sides (input or output) of the SSCB to constantly measure the current flowing through it. This way, by means of this control block and the measured current, the possibility of implementing a i^{2}t tripping curve is allowed so that the power devices are turned-off when a current threshold of the implemented i^{2}t curve has been exceeded [126,136,138]. Note that, due to the fact that in this work only the short-circuit protection behavior has been analyzed, a unique rated current value, i_{rated}, is determined for performing an instantaneous tripping (see the control block in Figure 4.22). This value is defined as the double of the nominal current of the SSCB, i_{nom}, to ensure that the power device is safely opened while it is saturated [126]. Therefore, when the short-circuit occurs and the fault current, i_f, exceeds i_{rated}, the SSCB commands the power devices to open.

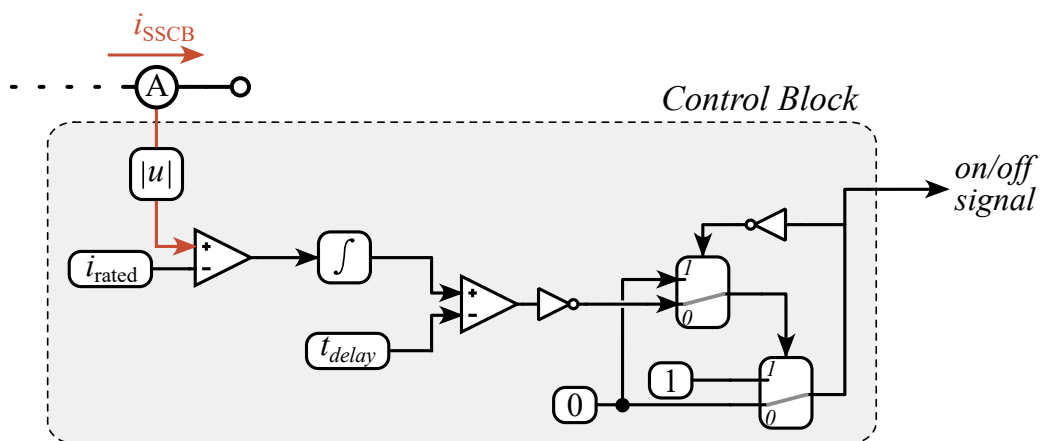**Figure 4.22** Control Block of the SSCB for short-circuit protection model assuming a tripping time delay.

It must be remarked that, even if i_f exceeds i_{rated}, the time for detecting the fault and sending the "*turn-off*" signal to the power devices is not actually instantaneous and, hence, the real current value at which the SSCB trips, i_{trip}, is larger than the predefined i_{rated}

(see Figure 4.21(b)) [126]. Concretely, this current fault difference, Δi_f, is defined as,

$$\frac{di_f}{dt} = \frac{V_L}{L_f} = \frac{V_{DC}}{L_f} \tag{4.11}$$

$$\Delta i_f = \frac{V_{DC}}{L_f} \cdot t_{delay} \quad . \tag{4.12}$$

Consequently,

$$i_{trip} = i_{rated} + \Delta i_f = i_{rated} + \frac{V_{DC}}{L_f} \cdot t_{delay} \quad . \tag{4.13}$$

where t_{delay} expresses the time spent since the fault is detected up to moment at which the power devices open.

Therefore, it is crucial to keep t_{delay} at minimum possible so that i_{trip} does not increase excessively and power device gets desaturated [126]. Essentially, this t_{delay} is composed by the addition of the current transducer delay, the measurement processing delay and the turn-off delay of the driver and the power device. Based on [126], a t_{delay} of $2.77\,\mu s$ is assumed and implemented in the control block by means of an integrator and a comparator (see Figure 4.22).

Finally, it is worth to mention that once the fault current exceeds the SSCB rated current, i.e. the turn-off signal is sent, the power devices are not turned-on back again unless a voluntary reset is performed.

- **Energy dissipating block:** This block represents the model of the energy absorbing branch used for the fault current. Particularly, a MOV has been used in this work which is selected so that, according to its datasheet values: *(1)* at the expected SSCB i_{trip} the MOV presents a desired clamping voltage, and *(2)* it permits a minimum of 10,000 operations. With MOV selected, the existing model in *PLECS* simulation software is used which is characterized by simply introducing the V-I datasheet values of the selected MOV.

As previously mentioned, the MOV is featured by a non-linear relation between the clamped voltage across it, V_{MOV}, and the current flowing through it, i_{MOV}. This relation results particularly interesting since, as depicted in Figure 4.21(b), while the MOV is conducting the fault current, V_{MOV} can be approximated as invariant and, hence, so can be done with the voltage across the SSCB [127]. This fact plays a critical role for fault extinction since if a fairly constant V_{MOV} is assumed, the fault current decrease is described as,

$$\frac{di_f}{dt} = \frac{V_{DC} - V_{MOV}}{L_f} \quad . \tag{4.14}$$

Therefore, the extinction time of the fault current, t_{ext}, can be estimated to be,

$$t_{ext} = \frac{L_f}{V_{MOV} - V_{DC}} \cdot i_{trip} \quad . \tag{4.15}$$

Figure 4.23 represents a graphical example of (4.15) for different V_{MOV} clamping voltages and fault inductances assuming, for instance, a i_{trip} of $500\,A$. It can be graphically seen that the higher the V_{MOV}, the lower the t_{ext}. However, assuming a relatively high V_{MOV} might

suppose to use a higher voltage rating semiconductor which can withstand the clamped voltage across it. In addition, it must be taken into account, that a stray inductance, L_σ, exists between the power devices and the MOV which provokes a voltage surge across the SSCB. Thus, aiming to consider this design condition, a L_σ of 400 nH between the power devices and MOV has been assumed for representing the worst-case scenario of the surge voltage [126].
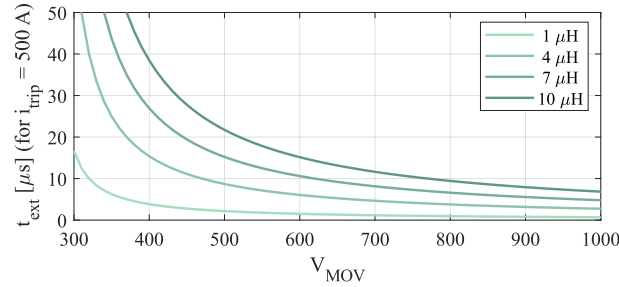

Figure 4.23 Estimated current extinction time depending on the approximated invariant MOV clamping voltage.

- **Snubber circuit block:** As a consequence of the stray inductance between the energy absorbing branch and the power devices, a RCD snubber circuit is added to the simulation model so that the voltage stress of the power devices is reduced. The RCD snubber presents a fault current conduction right after the power devices trip (see Figure 4.21(b) and 4.21(d)). Thus, during this first transient after tripping, $C_{\text{sn}-1}$ charges so that the voltage across the SSCB increases smoothly. Once $V_{\text{SSCB}} > V_{\text{DC}}$, the second transient starts in which the current starts to decrease and is naturally switched to the energy absorbing branch (see Figure 4.21(b) and 4.21(e)). Note that in this loop no stray inductance has been considered to simplify the simulation [126]. In this regard, the two main components to be sized for the SSCB model are the resistor, R_{sn}, and the capacitor, C_{sn}. D_{sn}, on its behalf, is modeled as an ideal diode. On the one hand, the C_{sn} is sized by means of simulation method so that it absorbs the energy of L_{f} and L_σ and, thus, the voltage surge ($V_{\text{L}\sigma}$) that appears at the end of the second transient in Figure 4.21(b) is maintained below the power device voltage rating (and below the active clamp of the power device) [126].

On the other hand, the R_{sn}, is sized under two main criteria: *(1)* to limit the C_{sn} discharge current, and *(2)* to avoid current and voltage oscillations typical from an underdamped RLC circuit. As shown in Figure 4.21(b), once the fault current is extinguished by the MOV, a residual current is observed which represents the capacitive discharge. Under this operating condition, the capacitor is discharged by means of an RLC circuit as the one presented in Figure 4.24(a) below.

Therefore, three main responses can be expected from this RLC circuit: an underdamped response, a critically damped response, and an overdamped response [37, 145]. Consequently, aiming to achieve an overdamped response so that no resonances are introduced in the circuit, the R_{sn} should be minimally sized as,

$$R_{\text{sn}} \geq \frac{2 \cdot L_{\text{f}}}{\sqrt{L_{\text{f}} \cdot C_{\text{sn}}}} \quad . \tag{4.16}$$
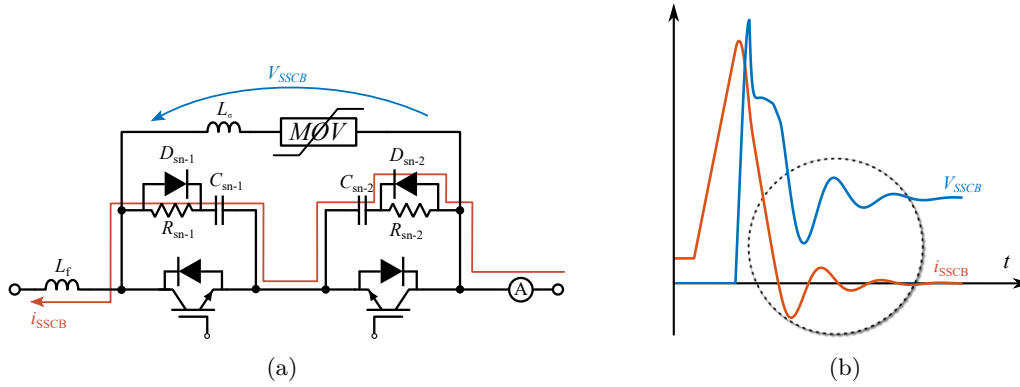
Figure 4.24 (a) Capacitor discharge path after fault extinction and (b) the resulting voltage and current waveforms across the SSCB.

It is worth to mention that, in this work, the R_{sn} is doubled with respect to the value achieved by (4.16). The main aim is avoiding the oscillations that might be created due to the resonance between C_{sn} and L_f, which might be uncertain. An example of the circuit response when R_{sn} has a lower value than the one described in (4.16).

The first sizing criterion, though, refers to the capacitive discharge in the case the SSCB is rearmed. Once the fault is extinguished, the C_{sn} might be charged with several hundreds of volts above the bus voltage value. Therefore, if the fault is cleared and the power devices can be back switched on, a RC capacitive discharge current flows through the power device which could burn out the power semiconductor if the R_{sn} is designed to be especially low.

4.3.4 Evaluation of the Fuse and SSCB for 2L$_{st}$ Architecture Protection

With both fuse and SSCB protection devices modeled, their implementation for protecting the 2L$_{st}$ is evaluated. Thus, Figure 4.25 below shows the short-circuit evaluation scenario, i.e. converter 1 short-circuited, in which each of the 2L$_{st}$ is equipped with a protection device (*PD* in the figure), being a SSCB or a fuse.
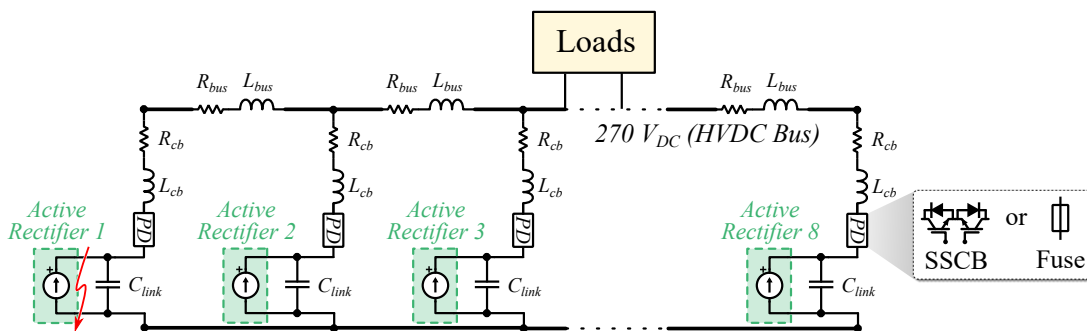
Figure 4.25 Schematic of the protected 2L$_{st}$ active modular architecture with converter 1 short-circuited.

Due to the high di/dt characteristic of the short-circuit current, a full SSCB protection for the 2L$_{st}$ architecture might result complex in terms of fault detection and device coordination. Note that, if the SSCBs are rated at the double of the nominal converter current value, for example, being approximately 140 A the SSCB rated current for a 18.75 kW sized converter, and

assuming a 2.77 μs fault detection delay, the short-circuit fault is detected when its value reaches approximately 1200 A (see $i_{rated-1}$ and i_{trip-1} in Figure 4.26(b)). This current value might not be tricky to interrupt for the SSCB of converter 1, but the main issue is that the delivered capacitive currents of the close neighboring converters (converters 2, 3 and 4) do also surpass the i_{rated} value before the fault extinction time. Thus, false tripping of healthy converters could be expected if the SSCBs overcurrent protection is implemented for a too low value.
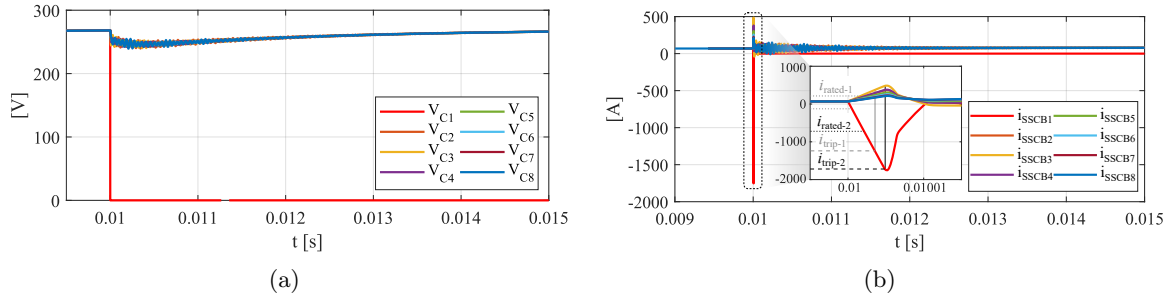
Figure 4.26 Short-circuit fault behavior of the 2L$_{st}$ architecture when converter 1 is short circuited and SSCBs are employed as protection devices. (a) Architecture voltage. (b) Short-circuit currents.

Another alternative relies on establishing a higher SSCB rated current such as the typically seen 10 times the nominal current in literature. In this case, the 700 A rated current, depicted in Figure 4.26(b) as $i_{rated-2}$, is defined as a tripping threshold high enough so that the neighboring SSCBs do not trip. However, the assumed time delay of 2.77 μs make the actual tripping current, i_{trip-2}, to be $\approx$ 1700 A.

In this sense, even if overcurrent protection results effective, as demonstrated in Figure 4.26(b) for the designed SSCB in Table 4.3, a significantly higher current rating power device should be assumed. Essentially, a power device (either IGBT or SiC MOSFET) that could interrupt such a high magnitude short-circuit current which, indeed, represents 25 times the SSCB nominal current. Therefore, an especially high cost and complexity is expected for the SSCB protection-based 2L$_{st}$ architecture. An alternative to employing such high overcurrent tripping and high rated power devices could be to employ another fault detection technique and/or achieve a faster fault detection and operation time lower than the assumed 2.77 μs. Currently, this achievement results complex according to the existing State-of-Art technology, but it is considered as an interesting for future research.

Table 4.3 SSCB model parameters for the converters of the 2L$_{st}$ architecture.

Parameter	Value
Nominal power of the SSCB, P_{nom}	18.75 kW
i_{nom}	70 A
i_{rated}	700 A
i_{trip}	1700 A
MOV Model	*SMOV43-SV181*
R_{sn}	5 Ω
C_{sn}	2 μF

In this regard, the fuse-based overcurrent protection does not require from fault detection, which could be advantageous in such low impedance short-circuit scenarios. Based on the fuse simulation model described, the "*littlefuse - PSR030US0100*" fast-fuse is selected for the architecture evaluation which presents the datasheet- and estimated-characteristics described in Table 4.4. The results of the fuse-based protection are presented in Figure 4.27.

Table 4.4 Fuse model parameters for the converters of the 2L$_{st}$ architecture.

| Parameter	Value
Fuse Model	PSR030US0100
V_{rated}	600 V
i_{rated}	100 A
V_{pk-arc}	775 V
Min. melting i^{2}t	435 A^2·s
Clearing i^{2}t	1535 A^2·s
Estimated R_{arc}	0.1174 Ω
Estimated C_{arc}	430 μF
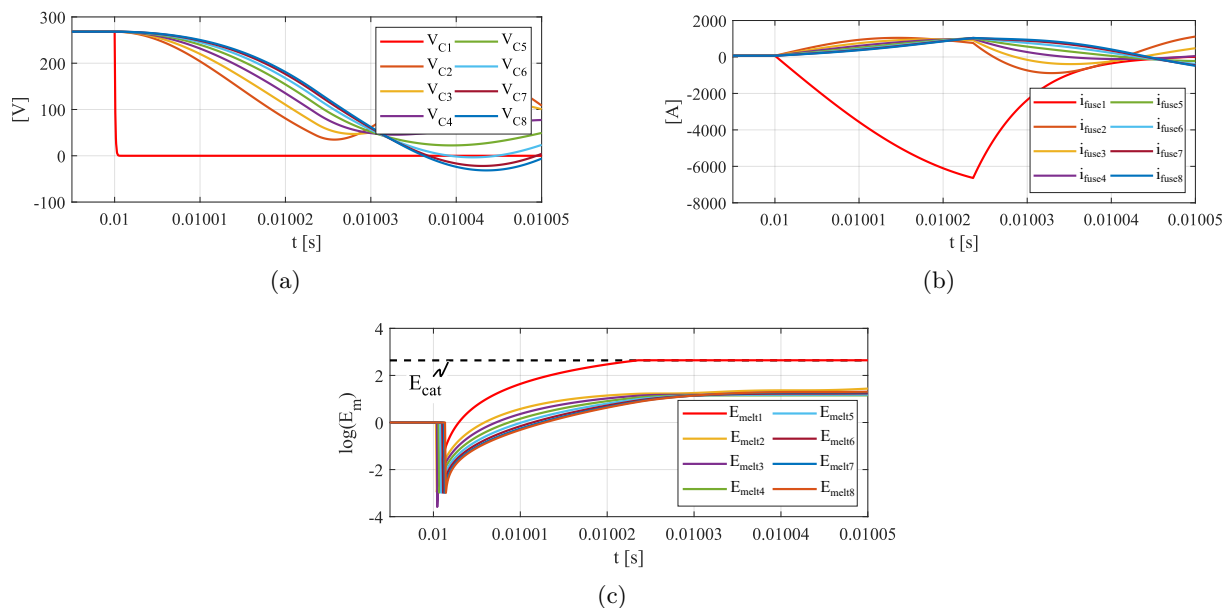
Figure 4.27 Short-circuit fault behavior of the 2L$_{st}$ architecture when converter 1 is short circuited and Fuses are employed as protection devices. (a) Architecture voltage. (b) Short-circuit currents.(c) E_{melt} of the fuses.

As presented in the figure, the fuse-based protection operates successfully. A zoomed imaged is presented in Figure 4.27(a) and 4.27(b) for clarification of the voltage and current waveforms of the system. As soon as the fault event occurs, the DC bus voltage decreases and the DC current increases. However, fuse 1 is melted in a relatively short time ($\approx 23\mu$s), which permits to start the arcing and isolate the fault in an overall time of $\approx 50\mu$s (see Figure 4.27(b)). In addition, even if in the case of the healthy converters $i_{fuse} > i_{rated}$ occurs, the melting i^{2}t energy is never reached, i.e. $E_{melt} < E_{cat}$ remains and, hence, no false tripping occurs. This last fact is depicted in Figure 4.27(c), where it can be observed how the melting energy of the fuses protecting the healthy converters stays far away from reaching the catalog energy value.

It is worth to mention that, due to the fact that in this simplified analysis the input DC filter capacitors of the loads distributed across the aircraft EPS have not been considered, the reported converter fault modeling approach presents an unreal fault scenario which will always be worse than the real fault scenario. As reported in [151], having additional capacitors not only provide a higher bus voltage inertia, but also provide additional fault energy which make the fuse of the faulty converter to blow in a shorter time. Thus, the presented scenario ensures the viability of the fuse-based 2L$_{st}$ active modular architecture protection. Under these circumstances, it is intended to integrate the fuse-based protected 2L$_{st}$ architecture into the MEA DC EPS.

4.3.5 Functional Redundancy of the STATCOM for the 2L$_{st}$ Architecture

Apart from ensuring the reliable operation of 2L$_{st}$ architecture, the additional benefit of functional redundancy should also be verified. As mentioned in the preceding chapter, a clear benefit of the 2L$_{st}$ active modular architecture is that, since the active rectifier and the STATCOM are equally designed, functional redundancy can be provided during operation. Note that, to verify this analysis the complete 2L$_{st}$ architecture has to be considered. The schematic process of the provided functional redundancy by a STATCOM is presented in Figure 4.29.
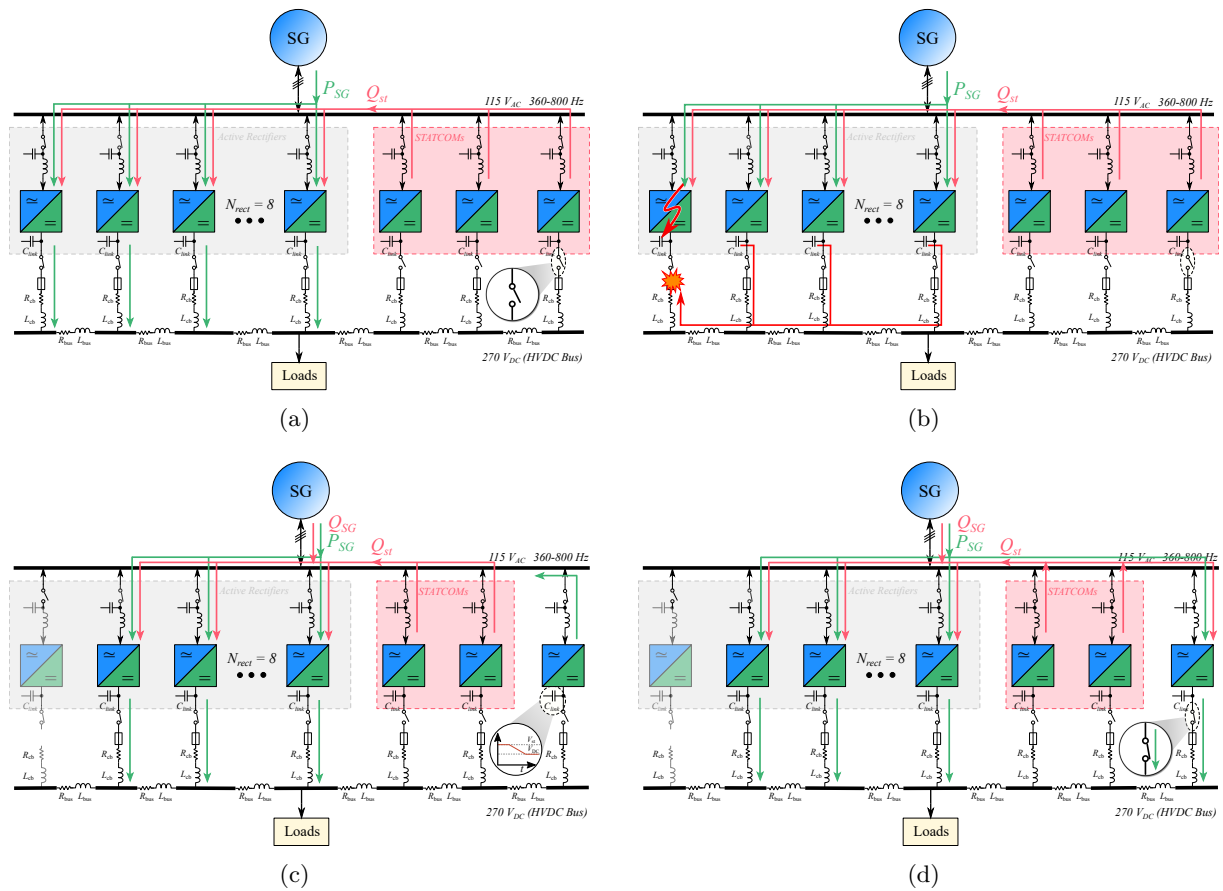

Figure 4.28 Schematic representation of a converter module changing from STATCOM to rectifier operation after a converter fault. (a) STATCOM operation (normal condition). (b) DC fault occurring in a rectifier and fuse blowing. (c) Energy delivery and bus voltage reduction after the fault is cleared. (d) Connection to the HVDC distribution grid and rectifier operation.

As presented in Figure 4.28(a), during normal conditions the SG deliver the active power to
the rectifiers, while the STATCOMs deliver the reactive power to achieve single-stage operation.
Note that, at this condition the STATCOMs are not connected to the HVDC distribution grid.

When a rectifier fault occurs, such as the one depicted in Figure 4.28(b), the DC-link capac-
itors are quickly discharged and the protection fuse is blown and, thus, the fault is isolated. It
is at that moment when one of the $2L_{st}$ STATCOMs, which is delivering reactive power to the
AC grid, diminishes its individual bus 459 V voltage to the distribution 270 V by delivering the
stored power in the DC capacitor to the AC grid (see Figure 4.28(c)). Then, the DC contactor
is closed so that the converter module starts to operate in rectifier mode and, as illustrated in
Figure 4.28(d), starts to transfer active power to the grid.

The simulation results of the STATCOM functional redundancy process are presented in
Figure 4.29. Note that, for this analysis, the average model of Chapter 3.5 of the $2L_{st}$ architecture
has been used, but including the DC side stray elements.
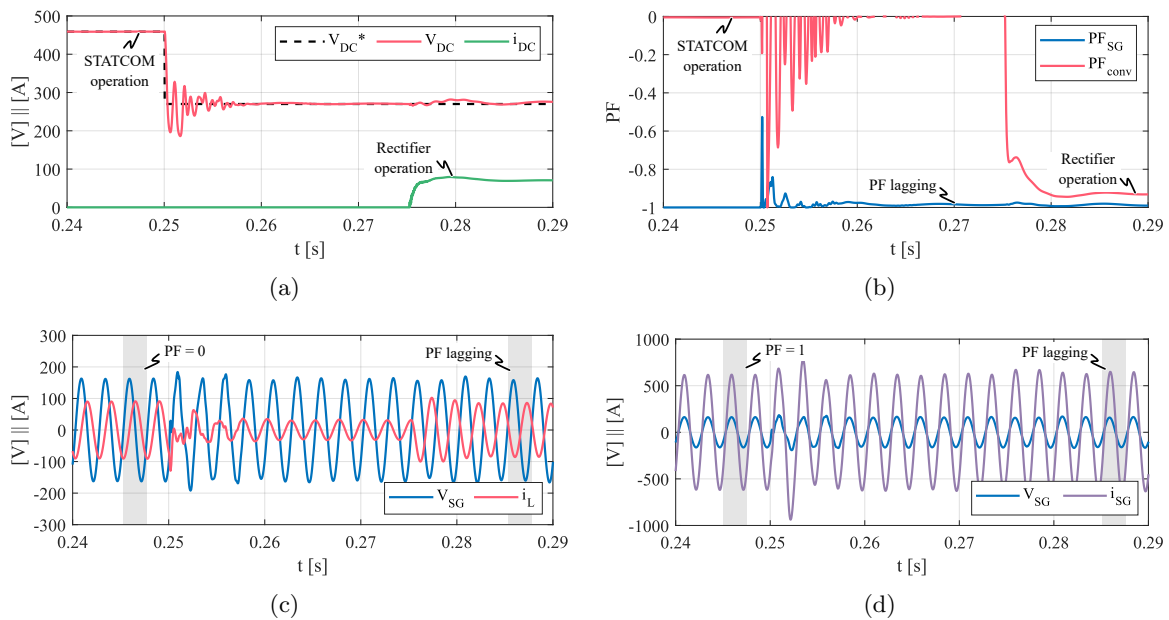
Figure 4.29 Functional redundancy results presenting post-fault reconfiguration of a converter module from
STATCOM operation to rectifier operation after a rectifier fault. (a) DC voltage and current of the reconfigu-
ration converter. (b) PF of the reconfiguring converter and the SG. (c) Phase A AC current and voltage of the
reconfiguring converter and (d) phase A SG current and voltage.

As presented in Figure 4.29(a), the converter operates as a STATCOM until the fault occurs
in $t = 0.25$ s. Thus, until the fault happens its bus voltage is 459 V and no DC current is
transferred to the HVDC bus. Consequently, its operating PF is 0 as depicted in Figure 4.29(b).
As soon as the fault occurs (including detection and isolation), the control loops are changed to
the ones of a rectifier and, hence, the DC bus voltage is diminished to 270 V. In this context,
the reconfiguring converter delivers active power to the AC grid to decrease its bus voltage from
459 V to 270 V and, then, waits until the connection to the HVDC distribution bus is performed
(assumed to be ≈ 15 ms). At that time ($t \approx 0.275$ s), the reconfiguring converter starts to
operate as a rectifier and transfers energy to the HVDC grid (see the increasing DC current
in Figure 4.29(a)). This idea can also be observed in Figure 4.29(b) and Figure 4.29(c), in

which the AC current of the (now) rectifier increases and its PF establishes at 0.942 to achieve single-stage operation.

Finally, Figure 4.29(d) shows the SG phase A voltage and current, V_{SG} and i_{SG}, respectively. The simulation reveals how the SG operates at unity PF before the fault occurrence, being V_{SG} and i_{SG} in phase. After the post-fault reconfiguration occurs, i.e. the converter changes from STATCOM operation to rectifier operation, no reactive power compensation enough is provided by the remaining STATCOMs to achieve unity PF at the POR. Therefore, V_{SG} and i_{SG} are not in phase anymore, and the operating PF of the SG decreases from 1 to 0.98. Note that the operating PF of the SG is also presented in Figure 4.29(b).

Therefore, the post-rectifier-fault reconfiguration is verified in this analysis which, particularly, demonstrates the successful "*equal rectifier and STATCOM design*" concept proposed in the preceding chapter. At this point, it has to be mentioned that the AC-side related studies are no longer analyzed in this work. Consequently, the integration study of the $2L_{st}$ architecture into the MEA EPS will only consider the simplified RLC + DC sources model of the $2L_{st}$ architecture with the fuse-based protection integrated.

4.4 Proposed Methodology for Evaluating the DC EPS Topologies and their Protection

Aiming to enhance the use of the $2L_{st}$ architecture in the MEA, its integration into the aircraft EPS becomes necessary. In fact, although in the previous section its fault-tolerant capability to an internal fault, i.e. rectifier fault, and its reconfiguration has been verified, the operating behavior against external fault should also be analyzed. Thus, the fault behavior as well as the proper EPS topology in which the $2L_{st}$ architecture is integrated gets special relevance. As stated at the beginning of this chapter, several DC EPS topologies exist that have been proposed as compact and reliable DC distribution systems like the ones employed in aircraft. Among others, the radial type or the ring-bus type can be found as literature proposals. However, few literature can be found regarding comparative analysis or comparison methodologies for identifying the appropriate EPS topology for MEA applications. Thus, in this section a methodology for comparing different aircraft EPS is proposed. The projected methodology, which is based on a simplified mixed analytical and simulation analysis, is based on the different DC microgrid features evaluated in literature and the protective design criteria [4, 37–39, 131, 147, 152]. In this context, the proposed methodology aims to quantify the critical characteristics related to an aircraft EPS, that are efficiency, reliability, weight and simplicity. For that purpose, the EPS is sized initially in terms of power generation capability, power sources and loads location and the load-shedding scheme under SG fault operation. This last factor reveals how the power generation is redistributed to feed the aircraft loads while avoiding a mismatch between power generation and consumption. Therefore, it presents an additional operating condition which, as later on demonstrated, results to be the nominal condition required for the protection devices sizing.

4.4.1 Definition of the Aircraft EPS Structure: Location of the Power Sources and Loads

As previously mentioned, the distributed radial-type EPS topology using SSCB protection devices of B787 aircraft represents the currently employed modern MEA EPS. This B787 structure is presented in Figure 4.30(a), where the power sources and loads are depicted based on $[1, 21, 147, 153, 154]$.
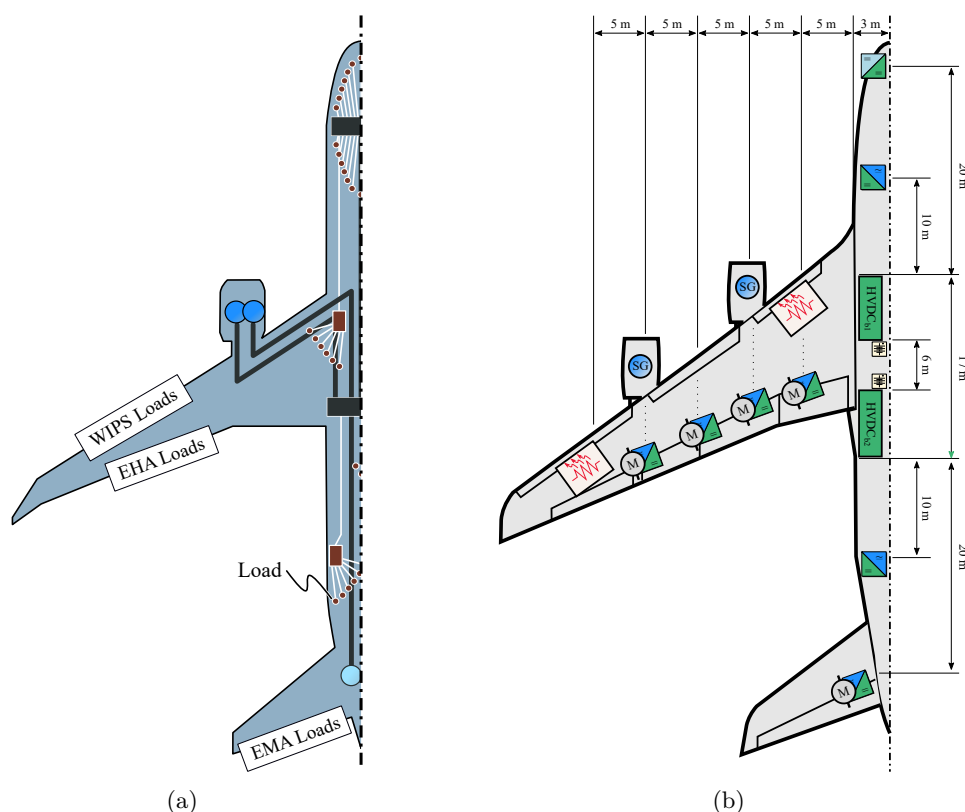
Figure 4.30 Simplified schematics of (a) B787 including the generation sources and loads, and (b) the proposed extrapolated structure (based on A380) for the evaluation of the EPS topologies.

Thus taking the B787 EPS structure as baseline, i.e. the approximate locations of the power sources and loads, a simplified structure is proposed in Figure 4.30(b) for the evaluation of the EPS topologies which assumes the following $[147, 153, 154]$:

- Aircraft half-symmetry is assumed for the locations of the power sources and loads.
- 4 SG are considered (1 per engine) as in the Airbus A380, each of it connected to a $2L_{st}$ active modular rectifier architecture designed in the preceding chapter. These subsystems and their AC cabling interconnection, though, will not be considered in the analysis since they are fixed for all the EPS topologies and, hence, they will not have any influence on the comparative analysis. Thus, the simplified $2L_{st}$ active modular architecture model of the previous section is assumed for the DC power sources in Figure 4.30(b) named as $HVDC_{b1}$, $HVDC_{b2}$, $HVDC_{b3}$, $HVDC_{b4}$.
- Even if several scattered loads can be found in the through the aircraft (see Figure 4.30(a)), it is assumed that the same type of loads, such as $28\,V_{DC}$ loads or AC Consumer Loads

(CL), are grouped at the single feeding point. Thus, the aircraft EPS subsystems and interconnections to be considered are significantly reduced as presented in the proposed structure of Figure 4.30(b). The power ratings of the grouped loads are defined according to the data in [17, 21, 61, 153] per half aircraft and summarized in Table 4.5.

Table 4.5 Summary of the considered aircraft load features for the EPS comparison.

Load	Amount	Power [kW]	Feeding Voltage [V_{DC}]	Location
Avionics	1	10	28	Cockpit
EHA	4	20	270	Wing
EMA	1	10	270	Tail
WIPS	2	15 || 75	270	Wing
CL	2	25	270	Cabin

It must be remarked that the presented loads are interfaced by power converters (except for the WIPS). Thus, the downstream connections and loads of these interfacing converter are assumed to be equal for each EPS topology and, hence, will not be treated in the efficiency and weight comparative analysis. Furthermore, aiming to simplify the fault analysis, all the loads in Table 4.5 are modeled as resistors representing the consumed power of the load with a $0.5\,\mathrm{mF}$ capacitor in parallel as input filter [64]. An exception is done with WIPS which is simply modeled as a resistor as reported in [64, 155, 156].

- The presented aircraft measures and load distances are based on the construction drawings of the A380 MEA presented in Appendix B.

With these assumptions and based on the simplified schema in Figure 4.30(a), the different EPS topologies should be sized, designed and compared.

4.4.2 Definition of the Load-Shedding Scheme

Establishing an EPS structure, i.e. measures and sources and loads locations, provides an initial lead for designing and sizing the EPS-topology-based distribution network. Nevertheless, a reliable EPS distribution network should also ensure the continuous power supply from the sources to loads. This perception is typically fulfilled during normal operating conditions but, during faults and post-fault operation, a substantial discrepancy between power generation and consumption might occur. In fact, the generation-load imbalance could result in a complete system black-out and, therefore, the EPS should not only be sized but also protected considering this event [37, 38, 153].

A potential solution to protect the EPS against generation-load imbalance scenarios relies on implementing a load-shedding scheme [37, 131, 153]. The load-shedding scheme, on its behalf, discriminates each load as Vital Load (VL) or Non-Vital Load (NVL). The VLs are considered as critical for fulfilling the aircraft mission and cannot be shed under no circumstances. On the contrary, the NVLs are defined as the loads that are allowed to be shed if the power generation capability is insufficient [37, 153, 154]. From the represented loads in Figure 4.30(a), the avionics, WIPS in de-icing mode, EMAs and EHAs are considered as VLs, while the CL and WIPS in

anti-icing mode are considered as NVLs [153]. In addition, the load-shedding scheme should also represent a shedding priority according to the aircraft mission and the fault severity [37, 154]. Therefore, by defining a load-shedding scheme not only the power generation and demand can be matched for normal and faulty scenarios, but also the major power requirements for sizing the protection systems and cabling of the aircraft EPS are identified [147, 153].

In this regard, due to the lack of a standardized load-shedding scheme and fault scenario representative of aircraft applications, the scheme described in [153] is adopted and described in Table 4.6. Thus, three different operating scenarios are evaluated in this work being normal condition scenario, one SG fault scenario, and 2 SG fault scenario. The number of SG available as well as the power generated per SG for each operation mode is also represented for identifying the power transfer through the cables and protection systems and, hence, element sizing. It is worth to mention that the 2 SG failure scenario represents 1 engine failure in [153], which is actually based on B787 and contains 2 SG per engine.

Table 4.6 Considered load-shedding scheme for EPS subsystems sizing.

Loads	Normal scenario	1 SG failure scenario	2 SG failure scenario
Avionics, EHA, EMA	No load-shedding		
WIPS	Anti-icing mode	De-icing mode	
CL	No load shedding		50 % load
Available SG	4	3	2
Power per SG	150 kW	120 kW	130 kW

According to the load shedding profile in Table 4.6, during normal operation no load-shedding occurs because the four SGs are available and, hence, all of them operate at full power to supply the necessary 600 kW EPS loads. If 1 SG fails some loads have to be shed, though. Note that, in this case, the power that should be delivered by the faulty generator, i.e. 150 kW, must be delivered by the remaining ones so that a mismatch between generation and consumption does not occur. Consequently, the WIPS anti-icing mode is reduced to de-icing, which supposes 60 kW less power consumption per WIPS load. This way, the overall power demand of the EPS is reduced from 600 kW to 360 kW and, thus, 120 kW per SG are delivered.

In the case of 2 SG failure, and additional load should be shed since the power demand of the previous case, i.e. 360 kW, result in an overloading condition for only 2 SG. Thus, a 50 % of the NVL consumer loads are shed. In addition, it assumed that the remaining consumer loads (50 kW) and the de-icing mode WIPS (60 kW) do not operate at the same time so that, in the worst case, a power demand of 260 kW is demanded by the EPS loads, being the 200 kW technical loads (avionics, EHAs and EMAs) plus the 60 kW WIPS in de-icing mode. Note that the WIPS operating time is approximately 10 minutes, which should not affect the comfort of the passengers in terms of consumer loads shedding, and permits not to overload the remaining 2 SGs, which generate 130 kW each.

Summarizing, the defined load-shedding scheme mainly drives the element sizing of the EPS, i.e. cabling and protection devices. Taking this premise into account, the EPS efficiency should

be estimated considering normal operations, 1 SG failure and 2 SG failure. The EPS weight, by contrast, should be estimated considering the worst-case operating condition of a certain element, i.e. maximum power transferred by cable or protection device, according to the load-shedding profile scenarios.

4.4.3 EPS Efficiency Estimation

Aiming to estimate the EPS efficiency under the load-shedding profile circumstances, the expected nominal efficiency values of the elements across the distribution network are defined in Table 4.7 [5, 61].

Table 4.7 SSCB design parameters for the converters of the 2L$_{st}$ architecture.

Subsystem	Efficiency
SSCB	99 %
Fuse	$\approx 100\,\%$
DC cable	$\geq 99\,\%$

In this regard, the efficiency of a single subsystem during operation, η_{ss}, is defined as,

$$\eta_{ss} = \frac{P_{ss-nom}}{P_{ss-nom} + P_{ss-loss}} = \frac{P_{ss-nom}}{P_{ss-transf}} \tag{4.17}$$

where P_{ss-nom} corresponds to the nominal power of the analyzed single subsystem (i.e., a cable or a protection device) and $P_{ss-loss}$ refers to the power losses generated by that subsystem. Note that the sum of these two power values form the transferred power by a single subsystem, $P_{ss-transf}$.

At a higher EPS level, though, the generated power of the EPS, P_{EPS}, is distributed to the loads by means of n subsystems of the same kind to operating in parallel. For example, $150\,\mathrm{kW}$ load power flowing through n cables feeding n loads of different power ratings. Thus, the overall efficiency of this stage, η_{stage}, that is several subsystems operating in parallel, is defined as,

$$\eta_{stage} = \frac{P_{EPS}}{P_{ss-transf_1} + P_{ss-transf_2} + ... + P_{ss-transf_n}} \quad . \tag{4.18}$$

This fact is important because the power of the EPS might go through different operating stages before reaching the load as in the simplified example depicted in Figure 4.31. Consequently, the overall efficiency of the EPS, η_{EPS}, is defined as the multiplication of the efficiency of each subsystem intervening in the distribution process, being,

$$\eta_{EPS} = \eta_{stage-1} \cdot \eta_{stage-2} \cdot ... \eta_{stage-n} \quad . \tag{4.19}$$
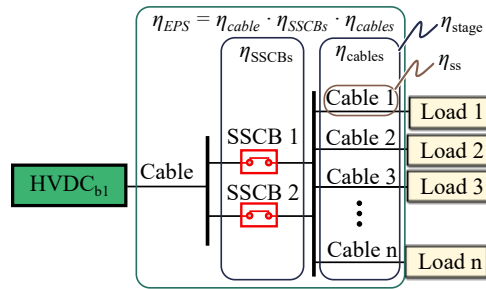
Figure 4.31 Simplified example describing the efficiency calculation considerations for an arbitrary EPS based on a single power source (active modular architecture).

On the other hand, for a given efficiency value of a single subsystem in Table 4.7, (4.17) can be rearranged to calculate the power losses of that subsystem as,

$$P_{\text{ss}-\text{loss}} = \frac{(1 - \eta_{\text{ss}}) \cdot P_{\text{ss}-\text{nom}}}{\eta_{\text{ss}}} \quad . \tag{4.20}$$

This calculation results of special interest for the SSCBs and cables of the EPS distribution network because they can be sized for a targeted efficiency value.

(1) In the case of the SSCBs, for which only conduction losses (P_{cond}) are considered [126,127], its power loss at nominal power rules the device sizing such that,

$$P_{\text{SSCB}-\text{cond}} = P_{\text{SSCB}-\text{loss}} = V_{\text{SSCB}} \cdot i_{\text{nom}} = V_{\text{SSCB}} \cdot \frac{P_{\text{SSCB}-\text{nom}}}{V_{\text{DC}}} \tag{4.21}$$

$$V_{\text{SSCB}} = \frac{P_{\text{SSCB}-\text{loss}}}{P_{\text{SSCB}-\text{nom}}} \cdot V_{\text{DC}} = \frac{1 - \eta_{\text{SSCB}}}{\eta_{\text{SSCB}}} \cdot V_{\text{DC}} = 2.73 \, \text{V} \quad . \tag{4.22}$$

Where i_{nom} corresponds to the nominal SSCB current when at nominal power $P_{\text{SSCB}-\text{nom}}$, η_{SSCB} represents the 99 % targeted efficiency in Table 4.7 and V_{SSCB} refers to the voltage drop across the SSCB when switched-on, that is the voltage drop across the power devices. Therefore, according to (4.22) a maximum overall voltage drop of 2.73 V across any SSCB is expected when conducting its i_{nom}. As a result, once the power device is selected, its V-I output characteristic is used to calculate the device efficiency under the different load-shedding profile scenarios.

(2) In the case of a cable, its power loss is directly linked with the proper resistance of the cable, R_{cable}, which is defined by Joule Effect as,

$$R_{\text{cable}} = \frac{P_{\text{cable}-\text{loss}}}{i_{\text{cable}}^2} = \frac{P_{\text{cable}-\text{loss}} \cdot V_{\text{DC}}^2}{P_{\text{cable}-\text{nom}}^2} = \frac{(1 - \eta_{\text{cable}}) \cdot V_{\text{DC}}^2}{\eta_{\text{cable}} \cdot P_{\text{cable}-\text{nom}}} \tag{4.23}$$

where i_{cable} is the current flowing through the cable, and the power rating of the cable, $P_{\text{cable}-\text{nom}}$, is equivalent to the power rating of the load to be fed in Table 4.5. Thus, depending on the load to be fed, the efficiency of a certain cable might vary according to the load-shedding profile.

Consequently, based on the targeted efficiency values in Table 4.7, the elements of the distribution network are sized and the efficiency of the EPS topology is analyzed under the different

load-shedding profile scenarios.

4.4.4 EPS Weight Estimation

Depending on the EPS topology, different amount of cable, number of protection devices or
even different power distribution reconfigurations after fault might be found. Consequently, the
power rating of the protection devices and cables might vary from topology to topology, which
directly affects to the EPS topology weight. In this regard, Table 4.8 summarizes the relevant
data considered for the EPS weight estimation according to [5, 61, 139, 157].

Table 4.8 Relevant data for the weight calculation of the EPS cables and protection devices.

SSCB data	
Power density	30 kW/kg
Fuse data	
Weight	0.15−0.5 kg
Cable data	
Cable material	Nickle-plated aluminum
Cable material density, ρ_{Al}	3100 kg/m^3
Cable isolation rating	600 V
Electrical conductivity, σ	32 MS/m
Reference temperature, T_{ref}	20 ºC
Final temperature, T_{f}	125 ºC
Resistivity coefficient, α_{T}	0.0039 ºC^{-1}
Insulator thickness, d_{ins}	350 μm
Insulator density, ρ_{ins}	1300 kg/m^3

In the case of the SSCB protection device, no predesign is initially required since the expected
power density in Table 4.8 and the power rating of the proper device are used for calculating its
weight as,

$$Weight_{\text{SSCB}} = \frac{P_{\text{SSCB−nom}}}{30 \, kW/kg} \quad . \tag{4.24}$$

Aiming to verify if the targeted power density is an achievable realistic value the cooling
requirements of the SSCB, i.e. the required $R_{\text{th,h−amb}}$, can be estimated. This estimation,
indeed, permits to compare different SSCB alternatives such as IGBT-based or SiC MOSFET-
based SSCBs. For that purpose, the maximum Temperature increase from heatsink-to-junction,
$\Delta T_{\text{j−c}}$ of each conducting device in the TEC, depicted in Figure 4.32, is initially calculated:

$$\Delta T_{\text{j−h,dev}} = T_{\text{j−max}} - T_{\text{h}} = P_{\text{cond−dev}} \cdot (R_{\text{th,j−c}} + R_{\text{th,c−h}}) = P_{\text{cond−dev}} \cdot R_{\text{th,j−h}} \quad . \tag{4.25}$$

Note that, if IGBT-Diode semiconductor devices are used, the P_{cond} as well as the thermal
resistances $R_{\text{th,j−c}}$ and $R_{\text{th,c−h}}$ might differ for each device, i.e. $P_{\text{cond−dev}_1} \neq P_{\text{cond−dev}_2}$ and
$R_{\text{th,j−h}_1} \neq R_{\text{th,j−h}_2}$. In the case of employing MOSFET devices, this difference is neglected since

it is assumed that the SSCB current flows through the MOSFET channel. Thus,

$$\Delta T_{\text{h}-\text{amb}} = P_{\text{SSCB}-\text{loss}} \cdot R_{\text{th,h}-\text{amb}} = (P_{\text{cond}-\text{dev}_1} + P_{\text{cond}-\text{dev}_2}) \cdot R_{\text{th,h}-\text{amb}} \tag{4.26}$$

$$R_{\text{th,h}-\text{amb}} = \frac{min(T_{\text{j}-\text{max,dev}} - \Delta T_{\text{j}-\text{h,dev}}) - T_{\text{amb}}}{P_{\text{SSCB}-\text{loss}}} \tag{4.27}$$

where T_{amb} refers to the defined application ambient temperature of $70\,^{\circ}\text{C}$ and $T_{\text{j}-\text{max,dev}}$ expresses the maximum datasheet junction temperature of the power device with a $15\,^{\circ}\text{C}$ safety margin. By means of these calculations, an interesting and simple approach to analyze different SSCB solutions is presented.
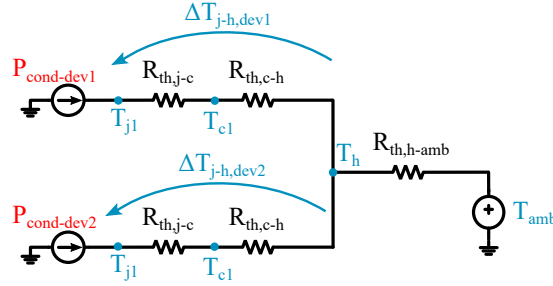

Figure 4.32 Simplified example describing the efficiency calculation considerations for an arbitrary EPS based on a single power source (active modular architecture).

Similarly to the SSCB, the fuse manufacturer provides the weight of the fuse to be employed and, hence, no calculation nor predesign is required.

On the contrary to the protection devices, a predesign for the distribution cables is required so that the cable weight can be calculated. As a simple estimation approach the cable volume calculation is calculated which, combined with the cable material density, leads to the cable weight result. Essentially, the resistance of a cable, R_{cable}, is defined by its temperature-dependent electrical conductivity, σ, and the cable structural parameters, i.e. the material cross-sectional area, A_{Al}, and the cable length, l [5, 61, 110, 146]. Thus,

$$R_{\text{cable}} = \frac{l}{\sigma \cdot A_{\text{Al}}} \cdot (1 + \alpha_{\text{T}} \cdot (T_{\text{f}} - T_{\text{ref}})) \tag{4.28}$$

where α_{T} expresses the linear characteristic of the σ variation considering the relation between T_{ref} and T_{f} of the cable material. These values are described in Table 4.8. It is assumed that the cables are naturally cooled [5, 61, 157].

Since the cable length is obtained from the structure model and the EPS topology employed, the cross-sectional area of a cable can be finally defined as,

$$A_{\text{Al}} = \frac{l}{\sigma \cdot R_{\text{cable}}} \cdot (1 + \alpha_{\text{T}} \cdot (T_{\text{f}} - T_{\text{ref}})) \quad . \tag{4.29}$$

Merging this last equation with (4.23),

$$A_{\text{Al}} = \frac{l}{\sigma} \cdot (1 + \alpha_{\text{T}} \cdot (T_{\text{f}} - T_{\text{ref}})) \cdot \frac{\eta_{\text{cable}} \cdot P_{\text{cable}-\text{nom}}}{V_{\text{DC}}^2 \cdot (1 - \eta_{\text{cable}})} \quad . \tag{4.30}$$

A graphical example of (4.30) is presented in Figure 4.33. On the one hand, it can be observed in the figure that, for an arbitrary cable length of 20 m, the higher the $P_{\text{cable−nom}}$ the larger A_{Al}. In the same way, increasing the targeted cable efficiency is translated into a lower cable resistance which, again, increases the cable area. Although not depicted, a similar trend could be observed if, instead $P_{\text{cable−nom}}$, the cable length was modified due to the fact that A_{Al} is also proportional to l.
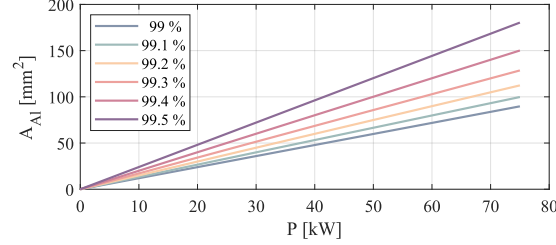

Figure 4.33 Calculated Nickle-Plated Aluminum 20 m length cable area depending on the cable rated power and targeted cable efficiency.

Note that increasing the conductor area does also influence the insulator cross-sectional area which, as depicted in Figure 4.34, represents the external layer of the cable and, therefore, must also be considered in the cable weight calculation. Aiming to calculate its cross-sectional area, the Nickle-Plated Aluminum inner conductor radius, r_{Al}, has to be defined first. Hence, assuming that the inner conductor cross-sectional area has a circular shape,

$$r_{\text{Al}} = \frac{A_{\text{Al}}}{\pi} \quad . \tag{4.31}$$
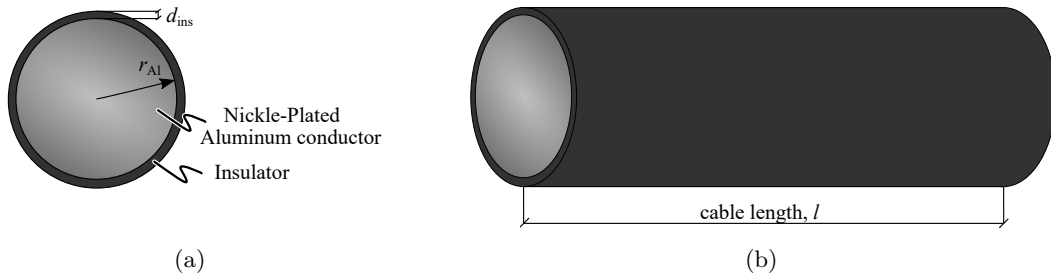
Figure 4.34 Illustration of (a) the cross-sectional area of a cable and (b) the cable length.

Consequently, the cross-sectional area of the insulator, A_{ins}, is calculated as,

$$A_{\text{ins}} = \pi \cdot \left((d_{\text{ins}} + r_{\text{Al}})^2 - r_{\text{Al}}^2 \right) \tag{4.32}$$

where d_{ins} corresponds to the insulator thickness described in Table 4.8.

Finally, the overall weight of a cable is calculated considering the volume of the inner conductor material volume, the insulator volume and their respective material densities. Hence,

$$Weight_{\text{cable}} = l \cdot A_{\text{Al}} \cdot \rho_{\text{Al}} + l \cdot A_{\text{ins}} \cdot \rho_{\text{ins}} \quad . \tag{4.33}$$

A graphical example of (4.33) is presented in Figure 4.35, where the cable weight for different rated power values and cable lengths is depicted assuming a 99 % cable efficiency. Note that the selected cable lengths correspond, approximately, to two time the distances (considering the positive and negative poles of the cables) assumed between HVDC buses and loads in the EPS structure of Figure 4.30(b).
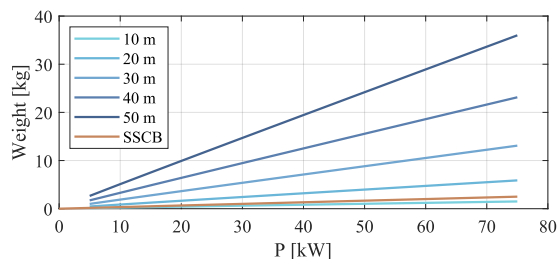

Figure 4.35 Estimated cable weight for different cable length values and expected SSCB weight according to the 30 kW/kg power density.

As expected, the larger the $P_{\text{cable}-\text{nom}}$ and the l, the larger the weight of the cable. In addition, the expected weight of the SSCB according to the targeted 30 kW/kg power density in Table Table 4.8 is also illustrated. Since the targeted efficiency of the SSCB is also a 99 %, Figure 4.35 reveals that, for the considered scenario, the overall EPS weight will be mainly driven by the weight of the cables. Consequently, a first weight comparison approach of the EPS topologies can be performed only considering the cable weight.

4.4.5   Fault Clearing Operating Speed

According to the aviation context, not only efficiency and power density are of crucial importance but also the reliability. Hence, when referring to DC EPS distribution systems, the concept of reliability of supply gains strength. Thus, if a fault occurs, isolating and clearing the fault as fast as possible becomes important to: *(1)* avoid the fault propagation throughout the EPS causing fatal damage, and *(2)* maintain the healthy part of the system operating correctly [37, 64]. Beyond that, aviation standards demand that the system fault has been cleared before 7 s and that the DC-link bus voltages do not reach a negative value [29, 62].

When a DC short-circuit fault occurs, the charged DC-link capacitors of the connected converters, being the rectifiers of the active modular architecture or loads, act as high fault-current sources [64]. The fault severity, however, will not only be influenced by the energy delivered by these capacitors, but also by the fault impedance from the capacitors (or fault energy sources) to the fault location. This fault impedance is typically defined by the low impedance of the distribution network cables. Therefore, apart from the cable arrangement, the impedance of the EPS cables have to be defined for analyzing the behavior of the system against the different faults [17].

Several electrical models exist for representing the impedance of a power distribution cable (or a power transmission line) [146]. These models, presented in Figure 4.36, differ essentially in the modeling complexity. The simplest model, depicted in Figure 4.36(a), is the one em-

ployed for short-length transmission lines ($< 250\,\mathrm{km}$), while the more complex ones, illustrated
in Figure 4.36(b) and 4.36(c), are the ones used to characterize the long-distance transmission
lines ($> 250\,\mathrm{km}$). Considering the DC EPS compactness in aviation systems and the inherent
relatively short cable distances of the EPS, such as the maximum of approximately $25\,\mathrm{m}$ in
the proposed EPS structure in Figure 4.30(b), it is typical to characterize a cable according to
the series RL impedance model in Figure 4.36(a) which does not consider any parasitic capac-
itance [64, 146]. Therefore, an RL model characterization is adopted for cables in this work in
which the R_{cable} is calculated according to the targeted distribution efficiency, using (4.23), and
the inductance, L_{cable}, is calculated according to the conductor geometry in [146, 158].
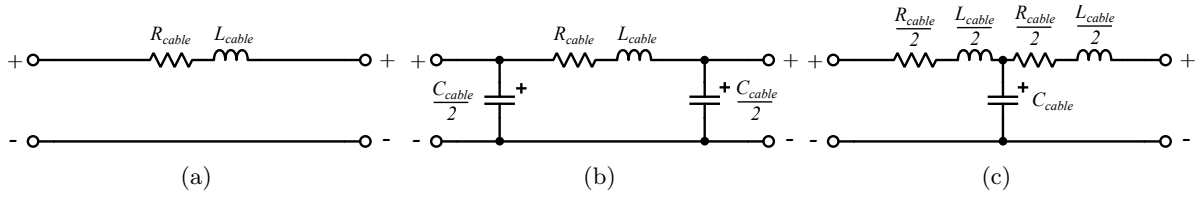

Figure 4.36 Typical representations of power transmission lines, being (a) the RL model, (b) the π model and,
(c) the T model.

Particularly, the L_{cable} estimation is usually considered as a relatively complex calculation
since not only the inductance of the proper conductor has to be considered, known as partial
inductance, but also the effect of other conductors over the one the estimation is being calculated
for, i.e. the mutual inductance. In the following, the mathematical expressions used for calcu-
lating the total inductance of cables [146, 158] is presented, for which the required geometrical
parameters are depicted in Figure 4.37 below.
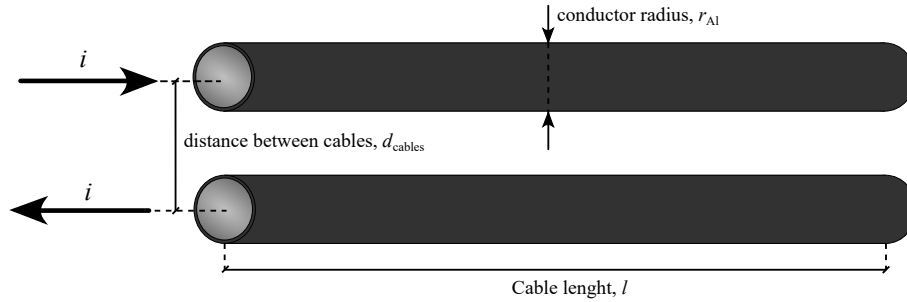
Figure 4.37 Description of the cable geometry for the parasitic inductance calculation.

In the case of cable wires, the self-partial inductance, L_{p}, is calculated as,

$$L_{\mathrm{p}} = \frac{\mu_0}{2\pi} \cdot l \cdot \left[\ln\left(\frac{2\,l}{r_{\mathrm{Al}}} \right) - \frac{3}{4} \right] \tag{4.34}$$

where $\mu_0 = 4\pi \cdot 10^{-7}$ H/m is the vacuum magnetic permeability and l and r_{Al} represent the
Nickle-plated aluminum wire length and radius, respectively.

The mutual inductance, M_{p}, for two paralleled cables of the same length is defined as,

$$M_{\mathrm{p}} = \frac{\mu_0}{2\pi} \cdot l \cdot \left[\ln\left(\frac{1}{d_{\mathrm{cable}}} + \sqrt{1 + \frac{l^2}{d_{\mathrm{cable}}^2}} \right) - \sqrt{1 + \frac{l^2}{d_{\mathrm{cable}}^2}} + \frac{d_{\mathrm{cable}}}{l} \right] \tag{4.35}$$

where d_{cable} corresponds to the distance between the center of both cables, hence, $d_{\text{cable}} \geq 2 \cdot r_{\text{Al}}$.

It is worth to mention that, even if the partial and mutual inductances of two parallel wires are calculated as in (4.34) and (4.35), respectively, the overall cable inductance, L_{cable}, depends on the direction of the current flowing through those cables. Thus, if the currents flow in opposite directions (as assumed in this case), the overall cable inductance (considering the positive and negative poles) is calculated as,

$$L_{\text{cable}} = 2 \cdot (L_{\text{p}} - M_{\text{p}}) \approx 2 \cdot \frac{\mu_0}{2\pi} \cdot l \cdot \left[\ln \left(\frac{d_{\text{cable}}}{r_{\text{Al}}} \right) + \frac{1}{4} \right] \quad . \tag{4.36}$$

Note that, aiming to simplify the theoretical calculations and considering the lowest impedance condition for fault analysis, that is the minimum L_{cable}, it assumed that the cables are close together so that the distance between them is expressed as $d_{\text{cable}} = 2 \cdot (r_{\text{Al}} + d_{\text{ins}})$.

On the basis of the cables depicted in Figure 4.35 for the weight analysis (using $(4.30) - (4.33)$, Figure 4.38(a) below presents a demonstration of the expected inductances in those cables (4.36). Note that, using (4.11), each cable inductance value can be directly linked to a di/dt in case of failure (see Figure 4.38(b)).
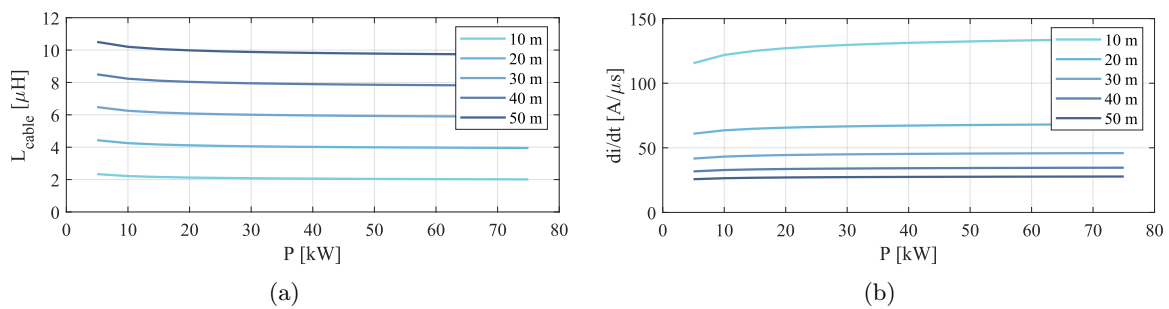

Figure 4.38 (a) Estimated inductances for different cable lengths and power ratings, and (b) their related di/dt.

At this point, aiming to fault clearing operating behavior of each EPS topology under different scenarios, three main faults are analyzed by simulation method:

(1) **$2L_{\text{st}}$ converter fault:** The protection successfulness against this fault represents, at the same time, the successful integration of the $2L_{\text{st}}$ active modular architecture into the EPS topology.

(2) **Busbar fault:** The busbar fault represents the minimum inductance fault for any fault energy source. Thus, the highest di/dt scenario is expected which, consequently, could lead to the fastest DC-link capacitors discharge.

(3) **$WIPS_2$ load fault:** Since this load is located at 25 m form the HVDC busbars, a minimum of 50 m cable (depending on the EPS topology) is required to feed this load considering the positive and negative poles. Thus, the highest impedance path is expected in this load is short-circuited, and hence, the lowest di/dt as presented in Figure 4.38. Note that it is assumed that the load contains a fuse as protective device. Thus, considering the nominal load power of 75 kW ($\approx$ 278 A in nominal conditions) and the minimum steady-state DC bus voltage of 240 V, a 315 A rated fuse (*Littlefuse - PSR030US0315*) is selected for the

WIPS$_2$ load.

In this regard, the *fault clearing time*, which should be below 7 s according to the aviation standards, is considered as an interesting metric to be measured in simulation for a comparative analysis among different EPS topologies [38]. Moreover, the fact that the DC-link voltage does not go below zero volts must be ensured for considering a successful fault clearing operation. Note that the protection systems employed as well as the protection scheme described in the next section play a critical role.

Furthermore, the *time until recovery* after the fault is isolated and the system reconfigured is also considered as an important metric. This parameter reflects the time after fault required for restoring the EPS operation "*back to normal*", i.e., the time required until the distribution voltage goes back to 270 V $_{DC}$ [38].

4.4.6 Reliability and Protection Coordination

Typically, three main features define the effectiveness of a protection scheme: *selectivity*, *sensitivity* and *reliability*.

The concept of *selectivity* refers to the operating priority of the protection devices from the fault point upstream the EPS [39], [144], [152]. The example in Figure 4.39 explains this concept by means of a radial DC grid line in which one rectifier feeds two DC/DC converters. In the example, the DC-link bus capacitance of the rectifier is denoted as C_{link}, while the input filter capacitances of the DC/DCs are named as C_1 and C_2. Similarly, the protecting devices are defined as PD$_{rect}$, PD$_1$ and PD$_2$ for the rectifier, DC/DC$_1$ and DC/DC$_2$, respectively.
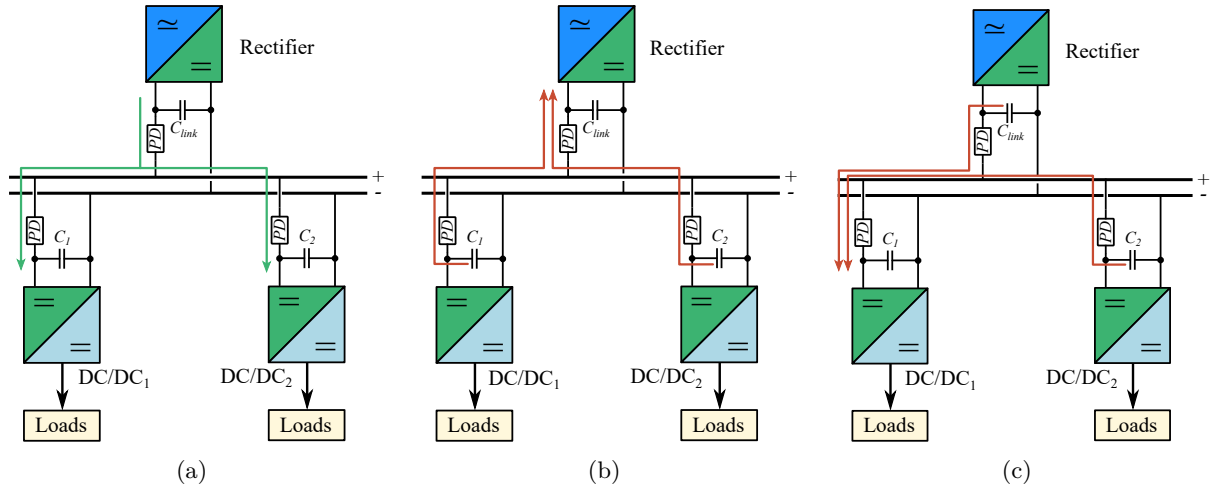
Figure 4.39 Example of imposed selectivity in a simple radial grid for three protection devices during (a) normal operation (b) rectifier fault and (c) load DC/DC converter fault.

During normal operation (Figure 4.39(a)), the rectifier feeds both loads, and no protection device acts. In the case of the rectifier failure depicted in Figure 4.39(b), C_1 and C_2 start to feed the fault. At this point, it is expected that PD$_{rect}$, while PD$_1$ and PD$_2$ should not act. Similarly, if a load fault as the one of DC/DC$_1$ presented in Figure 4.39(c) occurs, C_{link} and

C_2 feed the fault. Consequently, a successful selectivity makes PD_1 to operate while PD_{rect} and
PD_2 stay intact. Therefore, it is pretended that a protection device does not operate when a
fault occurs outside its respective zone.

The concept of *sensitivity* refers to the fact of detecting the fault. Thus, it is expected that
a protection device should operate when either a low impedance fault like a DC short circuit or
a high impedance fault like a long duration overcurrent occurs [39, 41].

When protection device selectivity and sensitivity are correctly adjusted for the protection
devices along the EPS, it can be said that the protection scheme provides a good *reliability* and
that a nice coordination among the protection devices exist [38, 39, 42, 152]. On the contrary,
if a correct balance between sensitivity and sensitivity is not achieved, more than one device
could trip when not necessary. This phenomenon, named as *sympathetic tripping*, could occur
if, for example, the discharge current of C_2 is significantly large so that PD_2 device acts in
Figure 4.39(c) [145, 152].

In this regard, the protection scheme employed in the EPS does also play a crucial role to
achieve a good reliability and nice coordination among protection devices. Conventionally, AC
EPSs employ unit or non-unit protection schemes to achieve a selective operation and protection
device coordination. However, since in DC EPSs the fault current increases much quicker than it
does in AC systems, it becomes tedious to properly apply these protection schemes [37, 42, 159].

Unit protection protects a specific zone by means of measuring the current and voltage values
at both line-ends and will not operate for faults external to this zone [37, 42, 64, 159]. Modern unit
protection schemes propose the use of communication channels among the different devices so
that a highly effective protection can be provided. However, the main implementation challenge
of these schemes in DC EPSs relies on the fact that communication time delays exist among the
devices, which may result in non-accurate (or low speed) tripping decisions.

The non-unit protection, on the contrary, uses locally measured current and voltage values
and applies a time grading operation so that the selective operation is enabled by intentional time
delays [37, 42, 64, 159]. These intentional time delays are, typically, in the order of milliseconds.
Therefore, this kind of selective application is also difficult to be employed because, in the DC
EPSs, especially, in compact EPS such as the one of the aircraft, faster fault current rise and
lower time available for fault isolation is available.

In this context, the demonstrated protection scheme in [38, 41, 151] is applied in this work.
This protection scheme, which is defined for a 2 DC bus-based radial-type DC EPS, is based on
the following three-level protection coordination:

(1) **Fast action (first level):** When a fault occurs throughout the distribution system, the
buses are separated by the bus-tie switches (SSCBs) so that the healthy side of the EPS
remains unaffected. This action may last up to several tens of microseconds.

(2) **Medium action (second level):** feeder and load protection by means of fuses or SSCBs.
This action may last up to several milliseconds.

(3) **Slow action (third level):** The AC power supply is protected by means of control
techniques, fuses or SSCBs. This action may last up to several seconds.

As previously mentioned, the AC side is not the focus of this research work. Therefore, the protection scheme considered is only focused in fulfilling correctly only the first two levels of the described protection scheme. Note that, as in [41], the fast action (or first level protection bus-tie SSCB trip) is assumed to be driven by overcurrent technique.

4.4.7 Survivability After Fault and Reconfigurability

The *Survivability* of the EPS is also considered an important metric in this analysis. This concept refers to the maximum loads that can be serviced considering the fault condition and priority order of the load shedding profile. Therefore, *Survivability* indicates the overall ability of the system to deliver and distribute power despite suffering fault damage [147].

Aiming to provide a simple measure of survivability, in this work a fraction of the loads that are fed with respect to the total aircraft loads is considered. Thus, as previously described in Table 4.5, 28 loads are considered for the complete aircraft EPS, being 2 avionics, 4 consumer loads, 4 WIPS (de-icing), 4 WIPS (anti-icing), 8 EHAs, 2 EMAs and 4 batteries. This simple math identifies the loads that cannot be fed due to the lack of generation capacity or due to the lack of connectivity in case of fault. In this context, according to the load shedding profile, the loads listed in Table 4.9 are expected to be fed or available. Note that if a busbar fault occurs, the same parameters as a SG failure are considered.

Table 4.9 Expected loads to be available according to the load-shedding profile scenarios.

Operating condition	Expected number of survivable loads	Notes
Normal conditions	28	
1 SG fault (or busbar)	24	Anti-icing WIPS removed
2 SG fault (or busbar)	20	Anti-icing WIPS and CLs removed

In this context, maximizing the survivability is considered as an important task for critical applications such as aircraft. According to [64], the survivability of the aircraft EPS to fault transients can be improved by four main general approaches:

(1) Designing the network components to resist fault transient conditions.

(2) Placing suppression devices like snubbers across the network to diminish the severity of the fault transient to an acceptable level.

(3) Providing functional redundancies for the network subsystems so that, if a subsystem is affected by the fault transient, a back-up subsystem is available.

(4) Installing a fast-acting protection scheme and protection devices aiming to isolate the fault event before it propagates throughout the EPS.

Ideally, a mix between the four options should be applied. However, the option applied for maximizing or improving the survivability of the EPS does also depend on the application requirements. In the MEA context, the first three options could suppose a significant increase in the aircraft weight. Therefore, the fourth option is the most preferable, especially, if fast action

protection devices like fuses and SSCBs are available. Note that this last option is assumed to be applied in accordance to the preselected protection devices and the protection scheme.

Due to the critical importance of safety in aircraft applications, though, option 3 is extensively applied [63, 64]. In fact, as previously mentioned, "*four feeding paths*" are typically assumed for VLs in aircraft applications [63]. Thus, aiming to maximize the survivability of the EPSs to be compared, four feeding paths are also assumed for VLs in this work.

4.4.8 Simplicity

The simplicity of the EPS protection systems is merely defined by the number of devices employed and the needed (or not) communication among the different protection devices of the EPS. Thus, a good protective scheme, in terms of simplicity, implies: *(1)* the operation of a low number of protection devices when a fault occurs, meaning high selectivity, and *(2)* the fact that no exhaustively fast communication is required among protective devices so that false tripping does not occur, meaning low dependence in centralized communication [37, 38, 152].

4.5 Design and Modeling of the DC EPS Topologies

With the EPS comparison methodology described, designing the different DC EPS topologies becomes the next task on the list. In this context, the Single-bus and Ring-bus topologies are designed bearing in mind the proposed EPS structure and targeting high efficiency, high power density and high reliability characteristics. Thus, although the efficiency and power density features are mainly driven by cable arrangement and the EPS structure, i.e. power sources and loads location, the reliability feature is close related to the protection devices employed and, hence, good fidelity simulation models of the protection devices are required.

4.5.1 Multi-Bus Type DC EPS Design

As previously mentioned, a strong research trend in MEA focuses on developing a Single-bus DC EPS approach due to its inherent simplicity, expected low weight and high efficiency. However, because of the existing risk of black-out and low reconfiguration capability, especially when a bus fault occurs, a Multi-bus EPS approach as the one presented in Figure 4.40 is preferred.
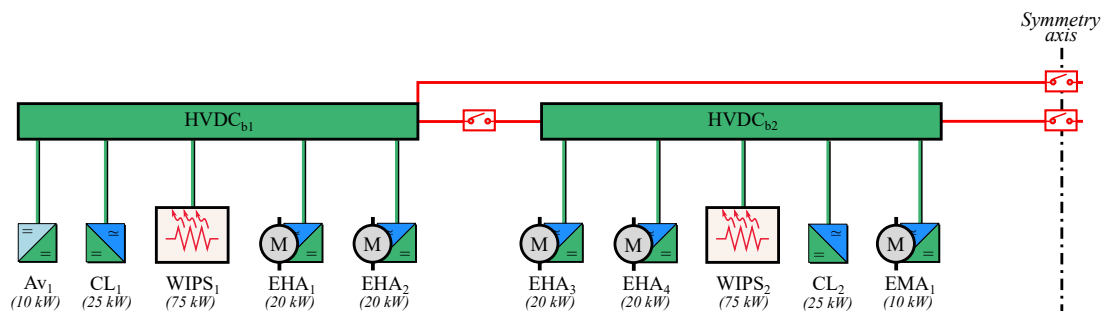

Figure 4.40 Simplified half aircraft schema of the HVDC Multi-bus type EPS.

Based on the defined aircraft structure in Figure 4.30(b) and the described load-shedding profile in Table, a power delivery symmetry among the four HVDC buses is assumed in this Multi-bus EPS design. Thus, on the one hand, the total amount of consumed power by the downstream loads of each HVDC bus during normal operation, corresponds to the power generation capability of the HVDC bus, i.e. 150 kW. On the other hand, an equivalent delivered power division among technical loads (VLs focused on flight controls like Avionics, EHAs and EMAs), WIPS, and CL is done for each HVDC bus.

Following this symmetry design criterion, the similar amount of cable is targeted for each HVDC bus with the aim of simplifying the EPS fault analysis. Thus, based on the distances among the HVDC buses and loads in the EPS structure, the cable connections for half aircraft ($HVDC_{b1}$ and $HVDC_{b2}$ buses) are depicted in Figure 4.41. Note that protection devices are not depicted for greater clarity about cable arrangement. Essentially, the "*normal operation*" cables are depicted in green color while the black color cables represent a "*fourth path*" for the VLs in order to maximize the EPS survivability. This way, a VL in $HVDC_{b1}$, for instance, can be fed by: *(1)* the proper $HVDC_{b1}$ during normal operation, *(2 & 3)* the bus-tie connections of the neighboring $HVDC_{b2}$ and $HVDC_{b3}$ buses in case of SG_1 failure, and *(4)* the "*four path*" connection by means of an alternative cable to $HVDC_{b2}$ in case of bus $HVDC_{b1}$ failure.
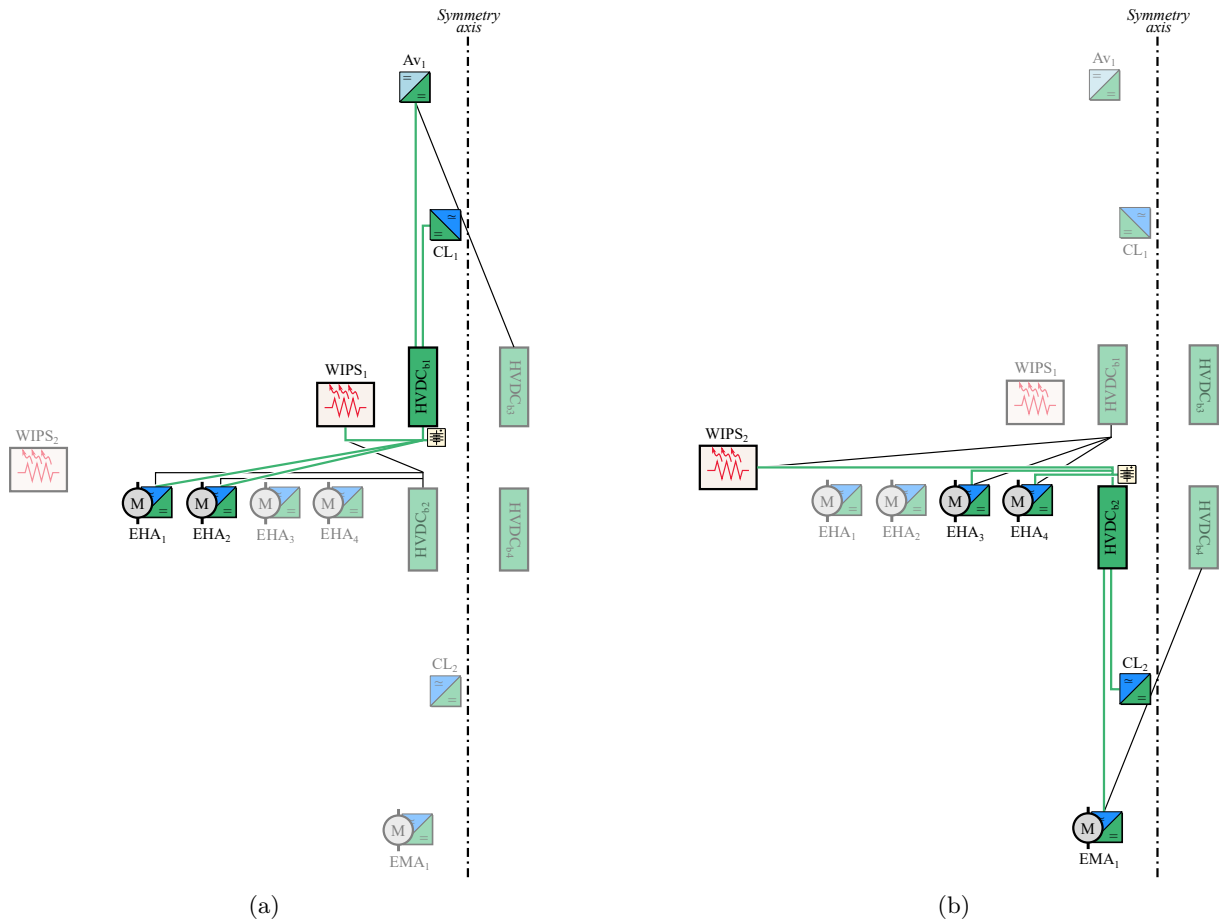

Figure 4.41 Schematic of cable connections for (a) $HVDC_{b1}$ which is symmetrical to $HVDC_{b3}$, and (b) $HVDC_{b2}$ which is symmetrical to $HVDC_{b4}$. Normal connections are represented by the green lines while the four path of VLs for emergency operations is represented by means of the black line.

Based on the proposed cable connection approach in Figure 4.41 above, the cable distances are summarized in Table 4.10. In the table, the cables representing the fourth path of the VLs are also listed and identified with the subscript "*p4*". Note that, considering both positive and negative poles between the busbar and the connected load by means of a cable, the actual cable length is the double of the distance represented in the table. In addition, the power rating of each cable is also described which, indeed, corresponds to the nominal power of the load to be fed (see the power ratings of each load in Figure 4.40). In the case of the bus-tie cable, though, a different power sizing approach has been considered which is linked to the defined load-shedding profile and described in the following.

Table 4.10 Cable distance and power rating required for the different aircraft loads and the summary of the calculated cable parameters for a cable efficiency of 99.5 %.

Cable	Distance [m]	Power [kW]	r_{Al} [mm]	Weight[kg]	R_{cable} [mΩ]	L_{cable} [μH]
Bus-Tie Switch						
Bus-tie cable	6	65	5.45	3.68	5.6	2.41
HVDC$_{b1}$						
Av$_1$ cable	20	10	3.9	6.43	36.6	8.23
Av$_{1-p4}$ cable	20.88	10	4	6.43	36.6	8.58
WIPS$_1$ cable	5	75	5.9	2.95	4.9	2.01
WIPS$_{1-p4}$ cable	7.81	75	6.7	7.13	4.9	3.01
EHA$_1$ cable	20.88	20	5.7	13.7	18.3	8.38
EHA$_{1-p4}$ cable	20	20	5.6	12.58	18.3	8.04
EHA$_2$ cable	16.16	20	5	8.25	18.3	6.53
EHA$_{2-p4}$ cable	15	20	4.8	7.13	18.3	6.08
CL$_1$ cable	10	25	4.4	3.99	14.7	4.08
HVDC$_{b2}$						
CL$_2$ cable	10	25	4.4	3.99	14.7	4.08
EHA$_3$ cable	10	20	3.9	3.22	18.3	4.12
EHA$_{3-p4}$ cable	11.66	20	4.3	4.35	18.3	4.77
EHA$_4$ cable	5	20	2.8	0.83	18.3	2.12
EHA$_{4-p4}$ cable	7.81	20	3.5	1.98	18.3	3.24
WIPS$_2$ cable	25	75	12	71.63	4.9	9.72
WIPS$_{2-p4}$ cable [1]	25.1	75 (15)	12.2 (5.5)	75.73 (15.61)	4.9 (24.4)	9.99 (10.34)
EMA$_1$ cable	20.88	20	5.7	13.7	18.3	8.38

As previously defined, during normal operating conditions power generated by a HVDC bus is the same as the power consumed by its downstream connected loads, which is 150 kW. Ideally, under this operating condition there is no power flowing through the SSCBs as defined in Figure 4.42(a).

In the case of a SG failure, the HVDC bus connected to the faulty SG stops to deliver active power. However, the VLs connected to this bus have to be fed to fulfill the aircraft mission. Therefore, aiming to avoid the mismatch between generation and consumption, anti-

---

[1]The values between parenthesis represent the cable values after applying the cable rated power derating.

icing WIPS loads (60 kW per HVDC bus) are shed according to the load-shedding profile. Thus, the power consumed by the loads of each architecture (including the idle one) is reduced to 90 kW. Consequently, according to the example in Figure 4.42(b) and assuming an equal 120 kW power generation per available HVDC bus, 45 kW have to be supplied by the SSCB lines which connect the two neighboring buses to the idle one.
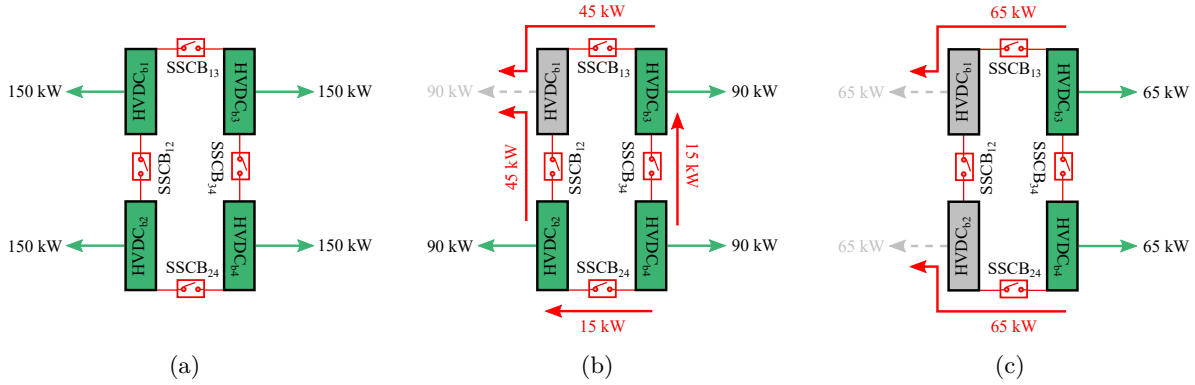

Figure 4.42 Simplified schematic to represent the amount of power transferred by the bus-tie switches (SSCBs) during (a) normal operation, (b) 1 SG failure operation and (c) 2 SG failure operation.

The worst-case operating condition, i.e. maximum power transfer by a SSCB, is given when two SG fault occur (see Figure 4.42(c)). During this operating scenario, the 25 kW consumer loads are also shed so that, in the worst case, a maximum of 65 kW is demanded by the VLs of each HVDC bus. Consequently, the remaining SGs must deliver a total of 130 kW, being 65 kW for their proper VLs and the remaining 65 kW the ones to be transferred through the SSCB to the neighboring idle bus. As a result, the bus-tie switch is rated at 65 kW and so it is rated the cable at which it is connected.

Once the cable distances (or lengths) and power ratings are defined, the weight of each cable can be calculated using $(4.30)-(4.33)$ for a defined efficiency target. Since a high distribution efficiency is desired ($> 99\%$) the cable weight is analyzed for a efficiency range between 99 % and 99.8 %. It must be taken into account that the higher the targeted efficiency, the better for transmitting power but also the higher cable weight expected.

Figure 4.43(a) presents the graphical result of the total EPS cable weight for a targeted efficiency range between 99 % and 99.8 %. From the figure, it is observed that targeting a 99.5 % of cable efficiency presents a nice trade-off between the overall EPS cable efficiency and cable weight values. In fact, it is observed that beyond this point, for each 0.1 % of efficiency increased a minimum increase of 25 % of the overall weight has to be assumed. Therefore, the cable related parameters reported in Table 4.10, that are R_{cable} using (4.23), L_{cable} using (4.36) and the cable weight and diameter, are calculated for 99.5 % cable efficiency. It is worth to mention, that although the cable radius is represented in the table, this parameter is shown to provide the certainty that the designed EPS is composed of cables with logic sizing values. In reality, commercial cables should be employed which could have a larger diameter and, consequently, a lead to a larger overall weight.

Aiming to provide a graphical analysis on the cable weight data, the individual cable weight

value is represented in Figure 4.43(b) for half of the aircraft, i.e. the cables represented in
the cable arrangement in Figure 4.41 and listed in Table 4.10. It can be clearly highlighted
that the highest cable weight values are achieved by WIPS$_2$ and WIPS$_{2\text{-}p4}$ cables due to the
distance between the load and the HVDC bus ($\approx 25\,\mathrm{m}$) and the fact that they are the highest
power rating cables, which transfer $75\,\mathrm{kW}$. Concretely, WIPS$_{2\text{-}p4}$ cable results to be the largest
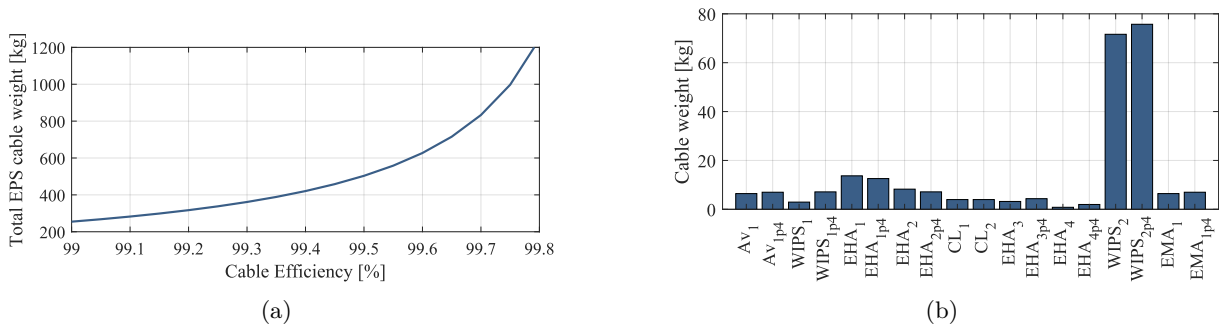in weight.

(a)

(b)

Figure 4.43 (a) Results of the overall cable weight of the EPS depending on the targeted efficiency, for which
(b) represents the individual cable weight result for a 99.5 % cable efficiency.

It should be taken into account that WIPS$_{2\text{-}p4}$ cable is actually used only for emergency
operations when: *(1)* WIPS$_2$ cable fails or, *(2)* when a HVDC$_{b2}$ busbar fault occurs. Therefore,
a low WIPS$_{2\text{-}p4}$ cable use is expected and desired, which means that no fault has occurred.
In addition, if HVDC$_{b2}$ fails, the load shedding profile of "*1 SG failure condition*" should be
applied, which means that the anti-icing WIPS load is shed. Thus, it is proposed to apply a
power derating to this cable, so that the nominal power rating is decreased from $75\,\mathrm{kW}$ (WIPS
anti-icing mode) to $15\,\mathrm{kW}$ (WIPS de-icing mode). This way, a lower overall EPS cable weight
can be achieved owing to a lower survivability degree. Hence, with the applied derating, if
WIPS$_2$ cable fails it becomes compulsory to operate WIPS$_2$ load in de-icing mode due to the
WIPS$_2$ cable derating applied. The consequent results to the EPS overall cable weight after the
derating is applied are presented in Figure 4.44, in which an overall EPS cable weight decrease
of $\approx 33\,\%$ is achieved.

(a)

(b)

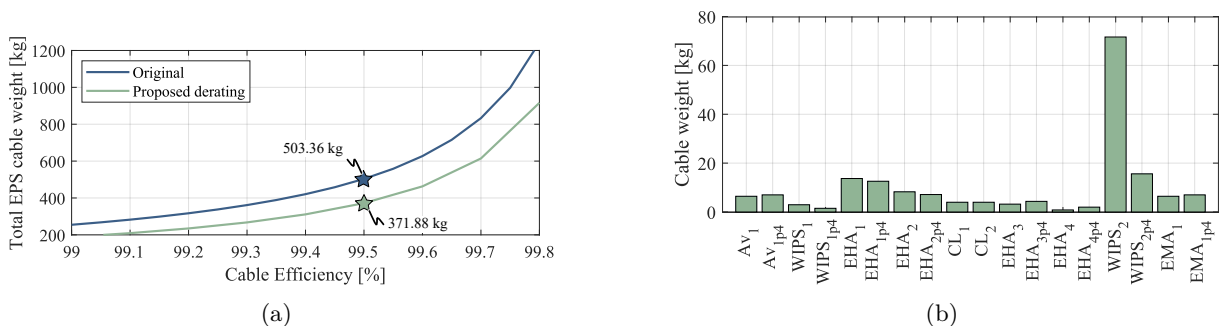**Figure 4.44** (a) Results of the overall cable weight of the EPS (considering the WIPS$_2$ cable derating) depending
on the targeted efficiency, for which (b) represents the individual cable weight result for a 99.5 % cable efficiency.

Another advantage of the proposed derating applied to the WIPS$_2$ cable is that it influences
the EPS in terms of weight, but it does not have a negative repercussion in the EPS efficiency.

Moreover, the efficiency analysis is done based on the defined load-shedding profile, i.e. normal operation, 1 SG failure and 2 SG failure. Thus, the "*four path*" related cables are not considered in this estimation.

Contrarily, the SSCBs which interconnect the four HVDC buses are. Therefore, aiming to analyze the EPS efficiency under the different load-shedding profile scenarios it is interesting to design the SSCB and select its power device so that an approximate estimation of the SSCB efficiency can be done. Regarding the design, the following parameters in Table 4.11 are calculated according to the simulation model previously presented:

Table 4.11 65 kW SSCB design characteristics.

Parameter	Value
P_{nom}	65 kW
i_{nom}	240.75 A
i_{rated}	481.5 A
R_{cable}	$5.6\,\text{m}\Omega + 2 \cdot 30\mu\Omega$
L_{cable}	$2.41\mu\text{H} + 2 \cdot 0.5\mu\text{H}$
i_{trip}	720.8 A
$R_{\text{cable}-\text{min}}$	$5.66\,m\Omega\,/2$
$L_{\text{cable}-\text{min}}$	$3.41\mu\text{H}\,/2$
$i_{\text{trip}-\text{max}}$	920.13 A
Device Rating	1200 V
MOV Model	*SMOV43-SV181*
R_{sn}	$5\,\Omega$
C_{sn}	$2\,\mu\text{F}$

As described in Chapter 4.3.3, the SSCB rated current is defined as the double of the nominal current of the SSCB. However, due to the assumed time delay of $2.77\,\mu\text{s}$ until tripping, the SSCB tripping current is larger than the rated one. In this context, two main fault scenarios (and impedances) have been considered for the SSCB design:

(1) the bus-tie cable impedance previously calculated in Figure 4.10 plus two times the impedance formed by the cable connections ($R_{\text{cb}} = 30\,\mu\Omega$ and $L_{\text{cb}} = 500\,\text{nH}$), named as "*Z*". Note that the SSCB is assumed to be located at the middle of the Bus-Tie cable and, hence, the calculated cable is actually divided in two parts. This fault impedance could be approximately the one appearing if, for example, one of the rectifiers of a HVDC busbar fails as presented in Figure 4.45(a).

(2) The half of the previous case impedance, i.e. "Z/2", assuming that the fault occurs at the input or output of the SSCB as presented in Figure 4.45(b). This fault impedance, indeed, corresponds to the minimum impedance and therefore to the expected maximum tripping current value, $i_{\text{trip}-\text{max}}$.

Based on these scenarios, the power device voltage rating is defined as well as the expected MOV clamping voltage for extinguishing the fault in a lower time than the fuse melting time ($\approx 25\,\mu\text{s}$). Thus, based on Figure 4.46(a), in which the V_{MOV} required for a defined t_{ext} is described, it is concluded that:
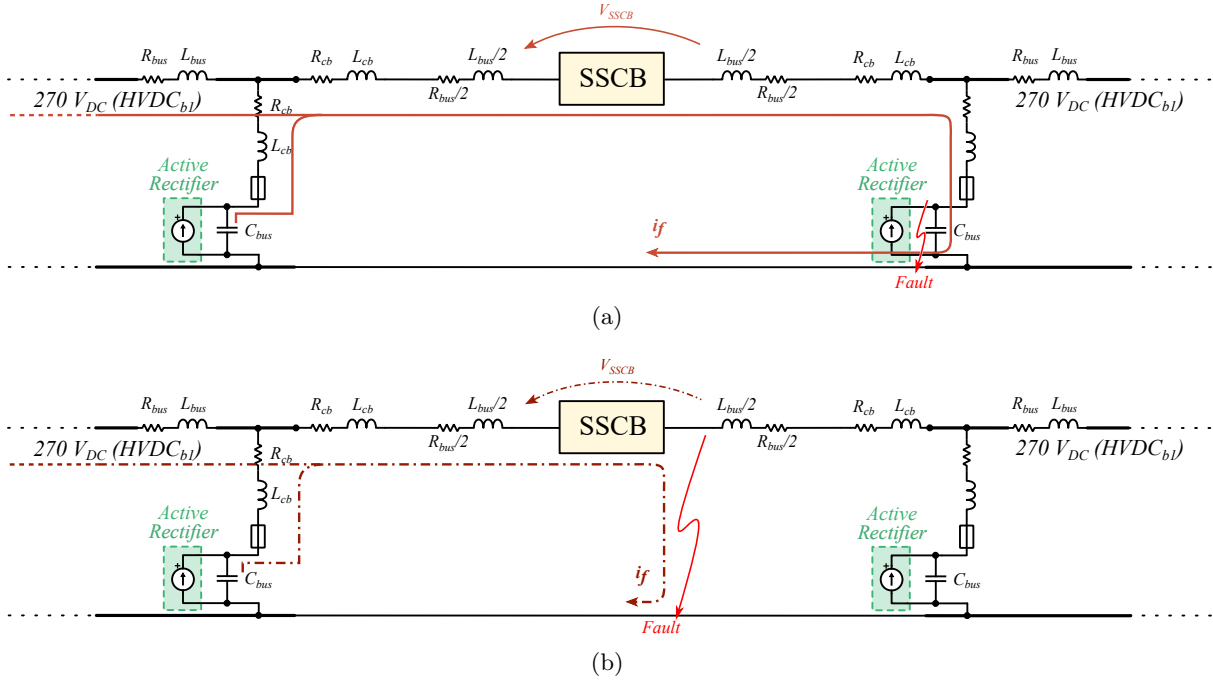
(a)

(b)

Figure 4.45 Simplified schematic of the considered fault tripping cases for the SSCB design, being (a) a fault at the end of the bus-tie cable, and (b) a fault at the input or output of the SSCB.

- Employing 650 V power devices is not a suitable option, since the power device active clamp for device protection, typically at 200 V lower than the rated voltage like 450 V ($\pm 10\,\%$ assuming manufacturing tolerances), leaves out a low margin for the V_{MOV} (for which a $\pm 10\,\%$ should also be considered) plus the overvoltage that the stray inductance might produce.

- 900 V devices could be a suitable option but, still, if it is wanted to clear the bus-tie fault current before the fuse melting time and considering an active clamp voltage of 700 V $\pm 10\,\%$, still a reduced margin for the MOV clamping voltage is left which should be, at least, 500 V $\pm 10\,\%$.

- Implementing 1200 V rated power devices is considered as the best option for this application. In fact, it represents a nice trade-off between the matureness of the 1200 V power modules, and the voltage margin that is left out between the active clamping (assuming it at 1000 V $\pm 10\,\%$) and a relatively high V_{MOV} like 650V $\pm 10\,\%$, which permits the fault current extinction time below $10\,\mu$s.
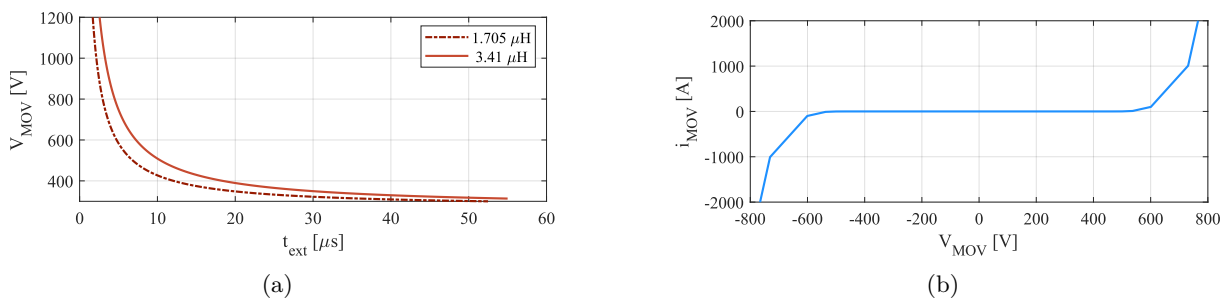

(a)

(b)

Figure 4.46 (a) Estimated t_{ext} depending on V_{MOV}, and (b) the selected MOV V-I characteristic.

As a result, *SMOV43S-V181* is selected which presents the V-I characteristic in Figure 4.46(b). Thus, with this MOV characteristic and the assumed stray inductance of $400\,\mathrm{nH}$, the snubber capacitor is defined as $2\,\mu\mathrm{F}$ by iteration simulation method so that the peak voltage caused by the stray capacitance does not achieve the minimum assumed active clamping voltage value of $900\,\mathrm{V}$. As demonstrated in Figure 4.47, with this capacitor value a high MOV energizing speed is achieved which permits to clear the fault in less than $10\,\mu\mathrm{s}$ after the power devices tripping occur. In addition, the established voltage margins result successful, which means that the fact of activating the active clamp of the power devices is avoided. Finally, a $R_{\mathrm{sn}} > 2.5\,\Omega$ is expected according to (4.16) and the expected cable impedance in Table 4.11. Thus, aiming to reduce the risk of occurring resonances (in the case of larger impedance faults) and limit the C_{sn} discharge current, which after fault clearing stays charged at almost $600\,\mathrm{V}$, $R_{\mathrm{sn}} = 5\,\Omega$ is selected.
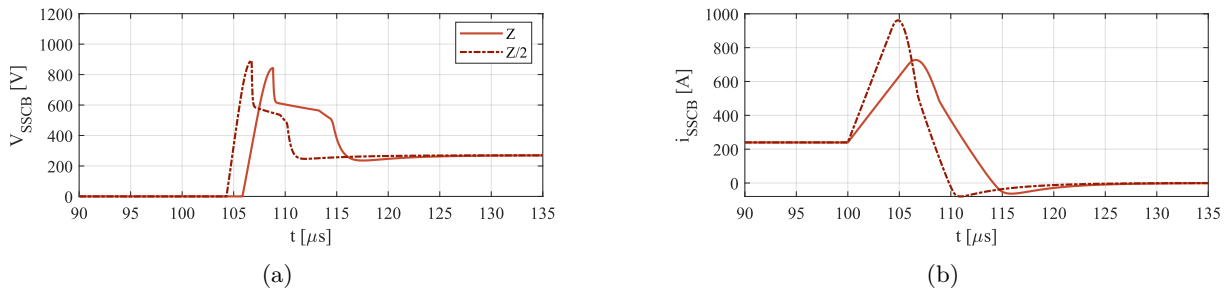

(a)   (b)

Figure 4.47 Bus-Tie SSCB design results (a) when considering the overall inductance between two HVDC buses ($3.41\,\mu\mathrm{H}$), and (b) when considering the half of the inductance between two buses ($3.41\,\mu\mathrm{H}\,/2$).

Regarding the power device selection, the $99\,\%$ targeted efficiency results a key parameter. As described in (4.22), an overall voltage drop of $2.73\,\mathrm{V}$ across the SSCB is deduced from (4.22) when conducting the nominal current, i.e. $240.75\,\mathrm{A}$ for $65\,\mathrm{kW}$. In this regard, the two power device alternatives are proposed in Table 4.12, being an IGBT and a SiC MOSFET. The approximated output V-I characteristic of the devices are depicted in Figure 4.48(a). Note that these approximations are done at the worst-case operating temperature of the devices, i.e. at the maximum junction temperature, $T_{\mathrm{j,max}}$, described in Table 4.12 for IGBT and SiC MOSFET, and at the lowest temperature ($25\,^{\circ}\mathrm{C}$) for the anti-parallel diode of the IGBT. Based on these curves characteristic, the estimated efficiency of the power devices is calculated using (4.17) and presented in Figure 4.48(b). The estimated heatsink thermal resistance, $R_{\mathrm{th,h-amb}}$, calculated using (4.27), is also reported as an indicative of the cooling requirement of the SSCB.

Table 4.12 Proposed power device alternatives and relevant data for designing the Bus-Tie SSCB.

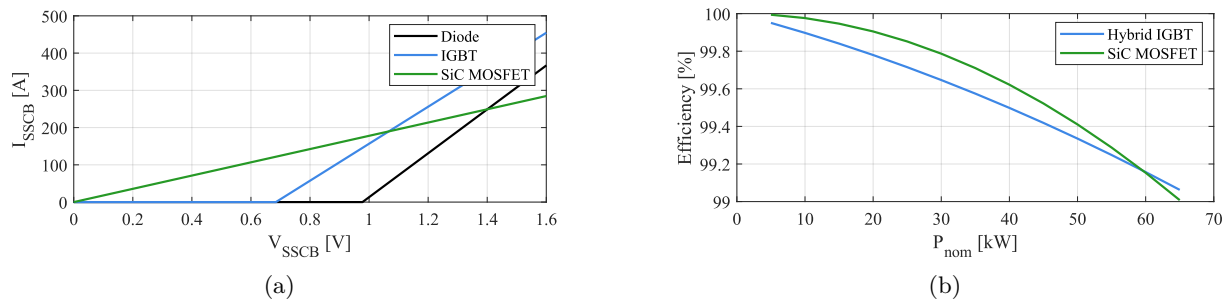| Parameter	IGBT-Diode	SiC MOSFET
Model	-	Wolfspeed -
Rating	1200 V - 600 A	1200 V - 425 A
$T_{\mathrm{j,max}}$	150 °C	175 °C
Weight	340 g	175 g
Cost	258 € + 4.5 k€·0.165 = 1000 €	833 €
$R_{\mathrm{th,h-amb}}$	0.0493 °C/W	0.0624 °C/W

Figure 4.48 (a) Output V-I characteristic of the selected devices, and (b) their estimated efficiency depending on the conducted current.

The IGBT device is presented, initially, as a relatively low-cost opportunity compared to the SiC MOSFET. In fact, the market value of the former device is around 3 times lower than one of the latter one. However, in aircraft applications the weight is considered such crucial that the estimated yearly $4500\,\$/\text{kg}$ save should be taken into account. Thus, the lower weight of the SiC MOSFET makes this last device as a better option. In fact, the selected SiC MOSFET presents a lower cooling requirement when operating at nominal conditions, and hence, a lower heatsink volume and weight is expected too. Furthermore, although relatively similar efficiency results are obtained, the fact the presented efficiency is greater for the SiC device than for the IGBT during almost all the power operating range makes this power device preferable. Therefore, based on SiC MOSFET efficiency data, and the defined load-shedding profile operation, the overall EPS efficiency results are presented in Figure 4.49 below.
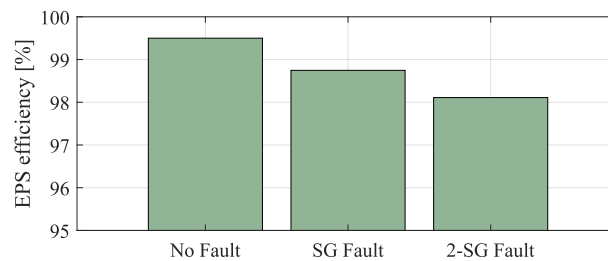
Figure 4.49 EPS efficiency results according to the load-shedding profile scenarios.

Fault Behavior Analysis

Finally, with all the multi-bus EPS components designed, the operation of the protection scheme against several fault occurrences is tested, being Figure 4.50 the results for a 2L_{st} converter fault, Figure 4.51 the results for a busbar fault, and Figure 4.52 the results for a WIPS_2 fault.

Figure 4.50(a), 4.50(c) and 4.50(e) show the behavior of the system against a 2L_{st} converter fault. From a top-level view it can be observed that, on the one hand, the fault occurs at $t = 0.012$ and that normal operating conditions are achieved in HVDC_{b1} ($V_{\text{DC}} = 270\,\text{V}$) at $t = 0.015$. On the other hand, the fact that no sympathetic tripping occurs among the 2L_{st} converter fuses can be observed.

As depicted in the zoomed to Figure 4.50(b), as soon as the converter fault occurs, the C_{link}

voltage is decreased to zero and the output current starts to negatively increase, which means that the fault current is going from the $HVDC_{b1}$ to the converter (fault location). In this case, Figure 4.50(d) and 4.50(f) show the operating behavior of the protection systems against the fault. As described by the protection scheme, the bus-tie switches are disconnected first so that the fault current does not propagate through them to the neighboring buses. Thus, once the faulty section of the EPS (section corresponding to $HVDC_{b1}$) is isolated, the fault is extinguished by the fuse in approximately 65 μs.

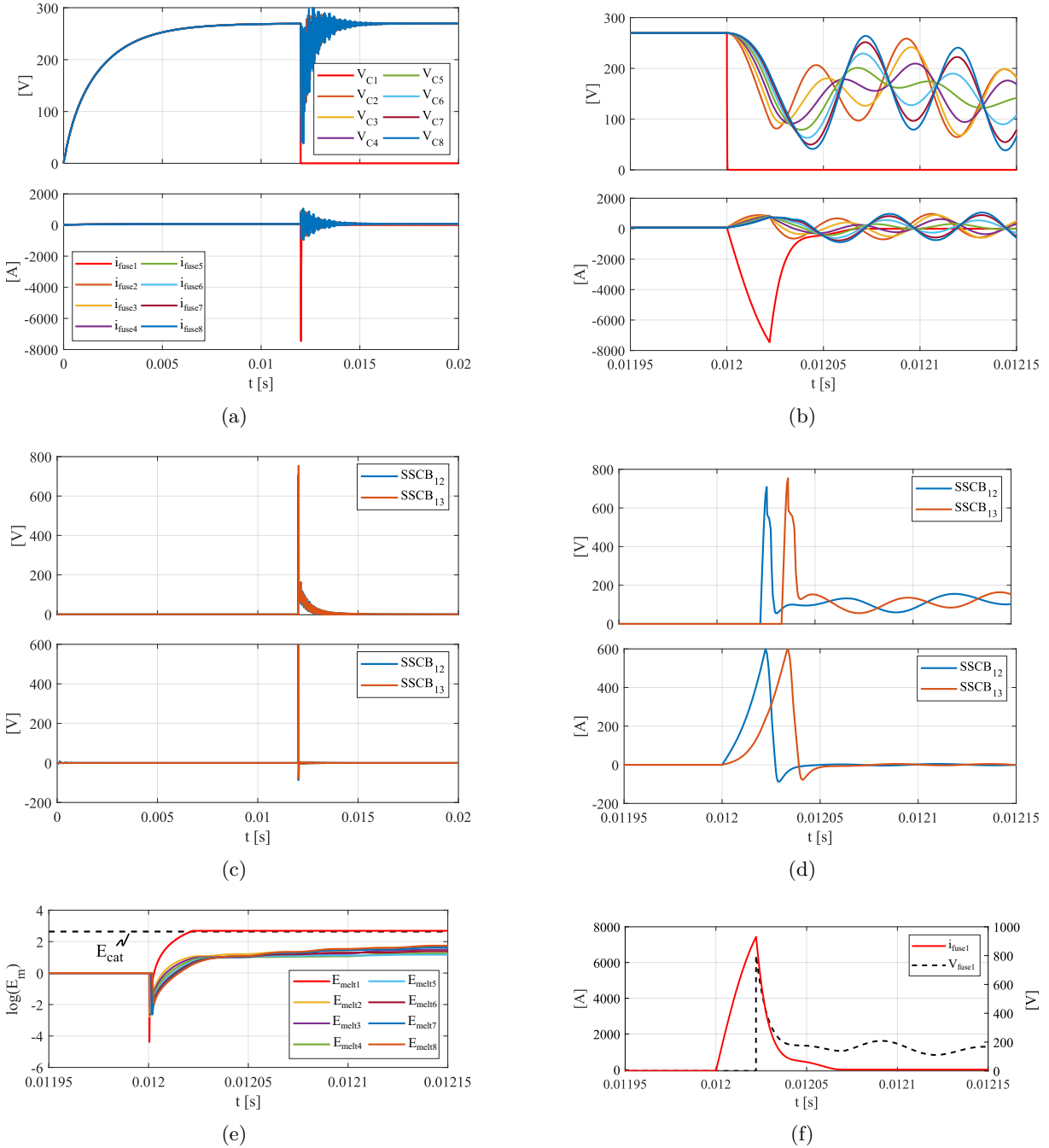**Figure 4.50** Multi-bus EPS simulation when a converter of the $2L_{st}$ active modular architecture fails. (a) C_{link} voltage and fuse current waveforms of the 8 $2L_{st}$ converters and (b) a zoomed view. (c) $SSCB_{12}$ and $SSCB_{13}$ voltage and current waveforms and (d) a zoomed view. (e) Melting energy of the $2L_{st}$ architecture fuses and (f) zoomed voltage and current waveforms of fuse 1 operation.

Once the fault is extinguished, the $HVDC_{b1}$ reestablishes the bus voltage value to $270\,V_{DC}$ and the voltages across the $SSCB_{12}$ and $SSCB_{13}$ decreases to zero. This last fact results interesting because, from the reconfigurability point of view, if after the fault (and SSCB tripping) the voltage across the SSCB decays to zero means that the fault has been cleared, the bus voltage reestablished, and that the reconnection of the healthy EPS sections to the one that suffered the fault is possible.

Finally, the fact that no sympathetic tripping occurs among the architecture fuses is presented in Figure 4.50(e). Particularly, the fuse located in the faulty converter branch is the one that extinguishes the fuse while the others heat up but without reaching the catalog energy. Consequently, a successful fault clearing operation is concluded for EPS against a $2L_{st}$ converter fault.

Aiming to analyze the EPS behavior when a bus fault occurs, a fault has been simulated in $HVDC_{b1}$. Concretely, in the terminals of the $SSCB_{12}$ cable connection. The results of the simulation are depicted in Figure 4.51.

The top-level view of the fault behavior is presented in Figure 4.51(a), 4.51(c) and 4.51(e) As soon as the busbar fault occurs, the bus voltage level starts to oscillate around zero volts. Since the fault occurs at the terminals connecting $HVDC_{b1}$ and the $SSCB_{12}$ cable, i.e. in $HVDC_{b1}$ to $HVDC_{b2}$ cable, the quick voltage decay, produces relatively high currents flowing from $HVDC_{b2}$ to the fault point in $HVDC_{b1}$. Particularly, this fault location makes $SSCB_{12}$ to act at a relatively low time, extinguishing the fault current flowing from $HVDC_{b2}$ to $HVDC_{b1}$ in $15 - 20\,\mu s$ (see Figure 4.51(d)).

In the case of $SSCB_{13}$, though, larger time is required to isolate $HVDC_{b1}$. This fact, however, is a consequence of the larger impedance found in the path from $SSCB_{13}$ to the fault location. In this context, it is assumed that $SSCB_{13}$ is the last device isolating the fault, which makes an overall fault clearing time of $\approx 50\,\mu s$. At this point, the EPS behavior against bus-fault, i.e. low impedance fault is considered successful.

It is worth to mention that, since the fuses cannot voluntarily trip, Figure 4.51(e) shows how the eight fuses of the $2L_{st}$ architecture will heat-up until blowing while the converters feed the fault with increasing DC currents. This issue, however, could be avoided if in case of overcurrent the power devices of the converters will be switched-off. In this case, the capacitors will simply discharge, and the fuse blowing could be avoided.

A clear difference when busbar fault occurs with respect to the previous $2L_{st}$ fault converter case is that the voltages across the SSCBs do not go back down to zero (see Figure 4.51(c)). In fact, the voltage across them maintains at $270\,V$, which means that the fault is still present and, hence, reconnection might not be possible.

(a)

(b)

(c)

(d)

(e)

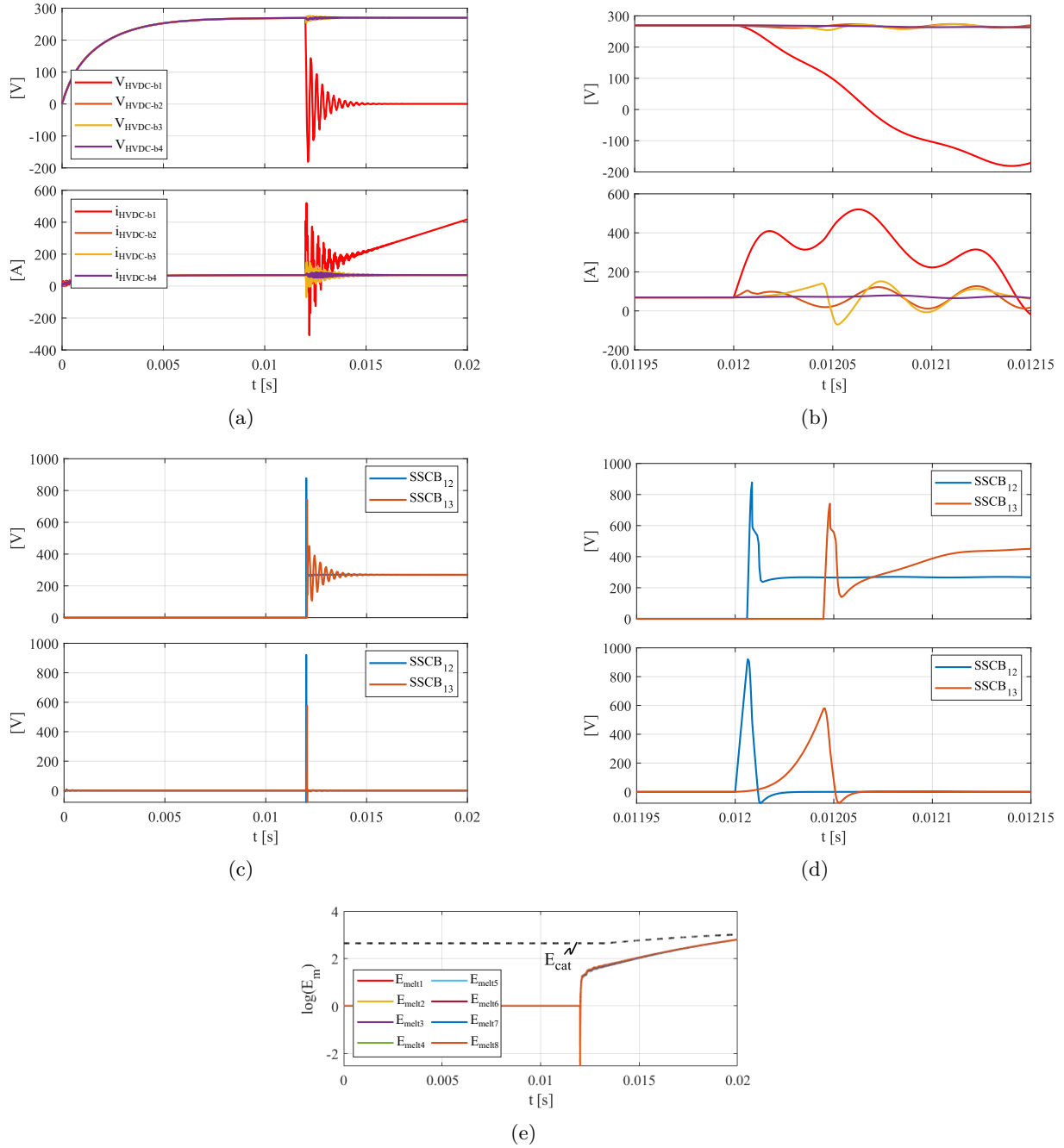**Figure 4.51** Multi-bus EPS simulation when a HVDC busbar fault occurs. (a) voltage and current of the HVDC buses and (b) a zoomed view. (c) $SSCB_{12}$ and $SSCB_{13}$ voltage and current waveforms and (d) a zoomed view. (e) Melting energy of the $2L_{st}$ architecture fuses.

Finally, in order to verify the suitability of the protection scheme for large impedance loads
($\approx 10 \, \mu H$), WIPS$_2$ load, located at $25 \, m$ from HVDC$_{b2}$, is short-circuited. The results of the
simulation are presented in Figure 4.52. Particularly, Figure 4.52(a) and 4.52(a) illustrate the
unsuccessful fault protection against the large inductance fault.

Figure 4.52 Multi-bus EPS simulation results when WIPS$_2$ load is short-circuited (with no additional capacitance). (a) voltage and current of the HVDC buses and (b) a voltage and current at WIPS$_2$ load terminals. (c) SSCB$_{12}$ and SSCB$_{24}$ voltage and current waveforms and (d) a zoomed view.

Due to the larger fault inductance with respect to the previous cases, the current increase
occurs at a lower di/dt. This is reflected in the required time for the SSCBs to isolate the faulty
section of the EPS. As presented in Figure 4.52(c) the SSCBs interrupt the fault current and
maintain their voltage at $270 \, V$ until the fault current is extinguished. Note that, if these current
and voltage waveforms are zoomed as in Figure 4.52(d), it is observed that the time required to
isolate the fault is $\approx 120 \, \mu s$.

This time delay with respect to the previous cases, however, could not be an issue if the
bus voltage was maintained above zero. However, as Figure 4.52(a) show, there is not enough
accumulated energy in the system capacitors to blow the fuse while maintaining the bus voltage
above zero.

In this context, a simple solution to avoid the voltage drop issue is to add an additional capacitor to the load as in Figure 4.53. This way, when the fault occurs, the capacitor delivers the required i²t to blow the fuse so that the fault is quickly cleared [145, 151]. A simple way to calculate this capacitor and verify the proposed solution, is to calculate the required charge to blow the fuse according to the fuse t-i curve and define the capacitor for an assumed voltage drop. For example, the minimum t-i value $(100\,\mu s, 8280\,A)$ and a voltage drop of $220\,V$ as the one happening when a rectifier of the $2L_{st}$ architecture is short-circuited. Hence,

$$Q = i \cdot t \tag{4.37}$$

$$C_{\text{additional}} = \frac{Q}{\Delta V} \tag{4.38}$$
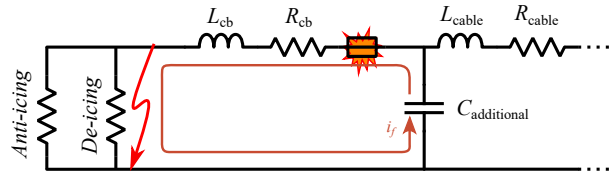
Figure 4.53 Delivered fault current of the additional capacitor added at the terminals of WIPS₂ load.

Thus, with the additional capacitor at the end of the WIPS₂ cable, the resulting protection coordination when a WIPS₂ fault occurs is now successful as demonstrated in Figure 4.54. Particularly, the bus-tie SSCB₁₂ and SSCB₂₄ are opened before the fuse melts so that HVDC_b1 and HVDC_b3 remain unaffected, and the HVDC_b2 voltage does not cross the zero value. Consequently, the protection scheme is considered as successful. It is worth to mention that a larger simulation time is shown in Figure 4.54(a) to show how the HVDC_b1 bus voltage recovers in approximately $20\,ms$.
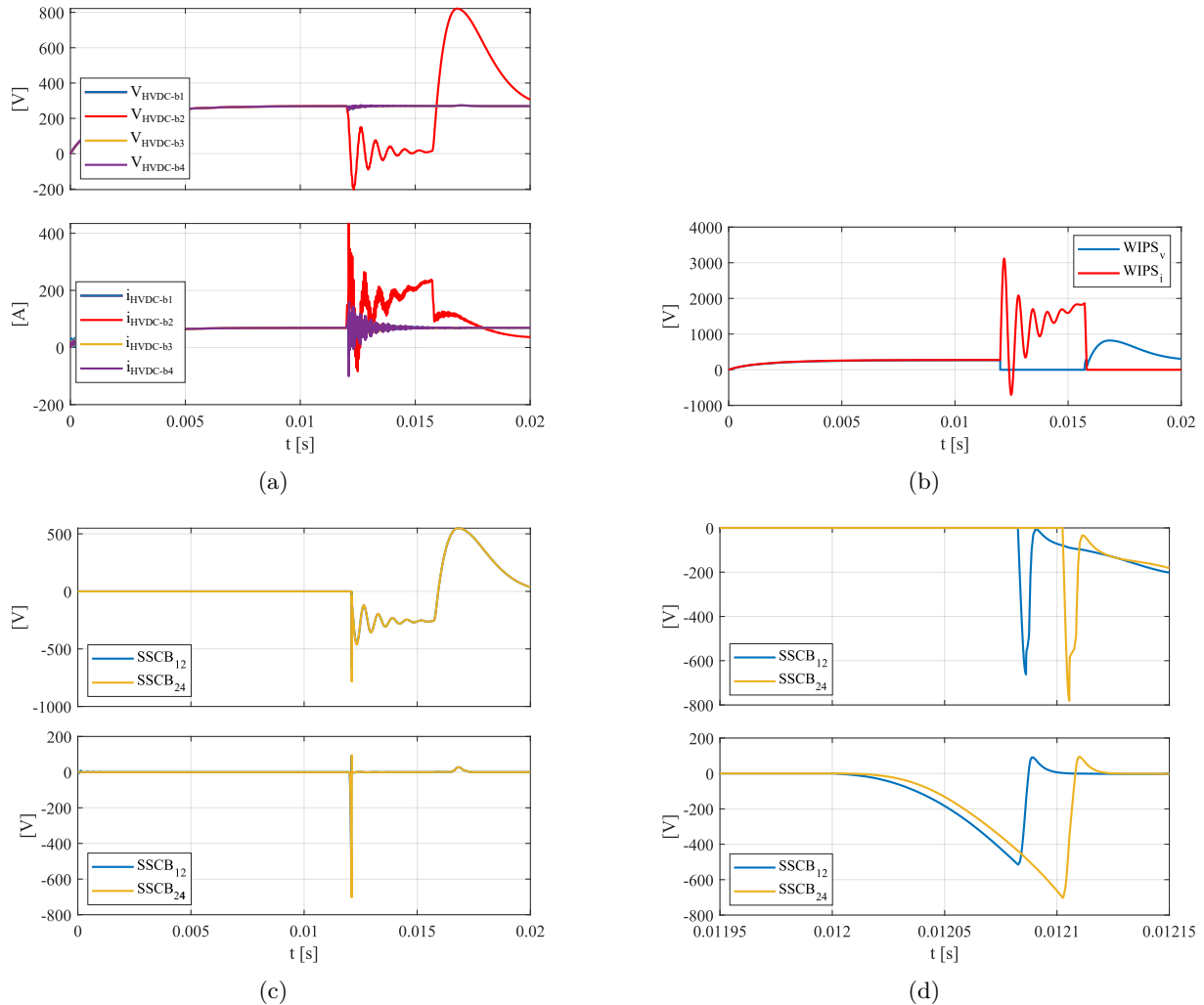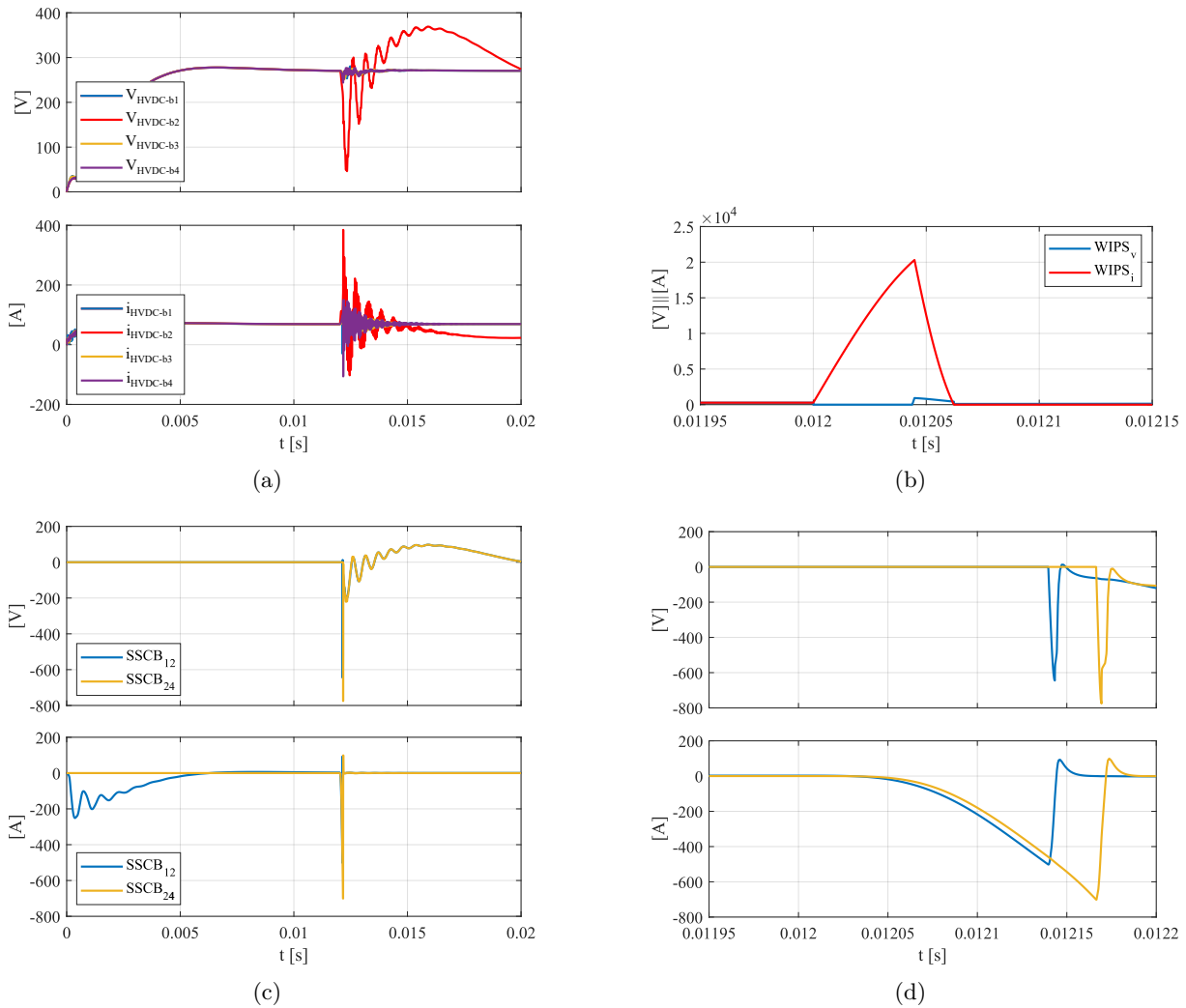
Figure 4.54 Multi-bus EPS simulation when $WIPS_2$ load is short-circuited (considering an additional capacitance). (a) voltage and current of the HVDC buses and (b) a voltage and current at $WIPS_2$ load terminals. (c) $SSCB_{12}$ and $SSCB_{24}$ voltage and current waveforms and (d) a zoomed view.

4.5.2 Ring-Bus Type DC EPS

On the contrary to the Multi-bus EPS which requires from additional "*four path*" cables to increase its reliability, the Ring-Bus EPS topology results an interesting EPS candidate due to its inherent increased reliability and survivability. In fact, as depicted in Figure 4.55(a), this topology not only has a high number of protection devices, but it also presents a distribution ring connecting the four $2L_{st}$ architecture HVDC buses to which all the aircraft loads are connected providing, therefore, the four feeding paths demanded in aircraft application. Considering a symmetrical zonal load distribution approach, it is proposed to discriminate the aircraft loads into the four main zonal loads represented in Figure 4.55(b), being,

Zonal Load 1: The frontside zonal load of the aircraft corresponding to the avionics (Av_1 and Av_2), the consumer loads (CL_1 and CL_2) and the batteries. Thus, a 70 kW rated zonal load is defined which, in case of extreme conditions (2 SG failure) will diminish its consumed power to 20 kW by shedding both CLs.

Zonal Load 2: The left-wing zonal load of the aircraft, which is composed by WIPS$_1$, WIPS$_2$, EHA$_1$, EHA$_2$, EHA$_3$ and EHA$_4$. Note that this zonal load is rated at 230 kW although it consumed power might decrease to 110 kW if the WIPS anti-icings are shed. In other words, in case of 1 SG failure.

Zonal Load 3: The right-wing of the aircraft which is symmetric to the Zonal Load 2.

Zonal Load 4: The backside of the aircraft, which is symmetric to the Zonal Load 1, with the small difference of Av$_1$ and Av$_2$ being replaced by EMA$_1$ and EMA$_2$.
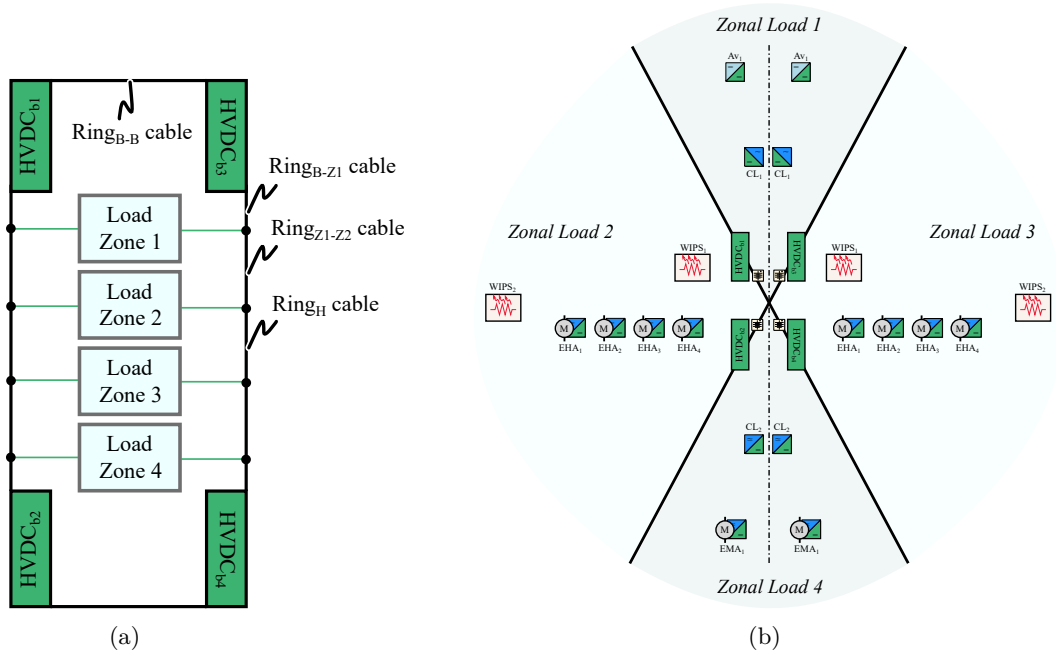

(a)

(b)

Figure 4.55 (a) Simplified Ring-bus schematic and (b) the proposed Zonal Load distribution.

It is worth to mention that, according to the Zonal Load approach explained at the beginning of the chapter, the VLs are connected to both sides of the ring to increase the reliability of supply and maximize the EPS survivability. Therefore, no additional "*four path*" cable is considered in this EPS because it is inherent to the proper EPS topology. Consequently, each Zonal Load is composed by two "small buses" for connecting the loads so that: *(1)* each "small bus" is connected to the ring by means of a cable and a protection device, and *(2)* the VLs are connected to both "small buses" but not the NVLs, which are only connected to one of them.

Based on the previous concepts, the cable connection of the loads of zones 1 and 2 are represented in Figure 4.56. Note that the "small buses" used for load connections are assumed to be inside the ring so that the distance from each load to a "small bus" is identical and so is the distance from a "small bus" to the ring. Hence, the design process of the cables and protection devices simplified. It must be remarked that the VLs of each zone are connected to both "small buses" while, in the Zonal Load 1, the CL are only connected to one of the "small buses".

Considered the proposed zonal loads and cable connections in Figure 4.56, the cable distances and their respective power ratings corresponding to each zonal load are listed in Table 4.13. It must be remarked that, for all the represented cables, considering both positive and negative poles the actual cable length is the double of the distance represented in the table.
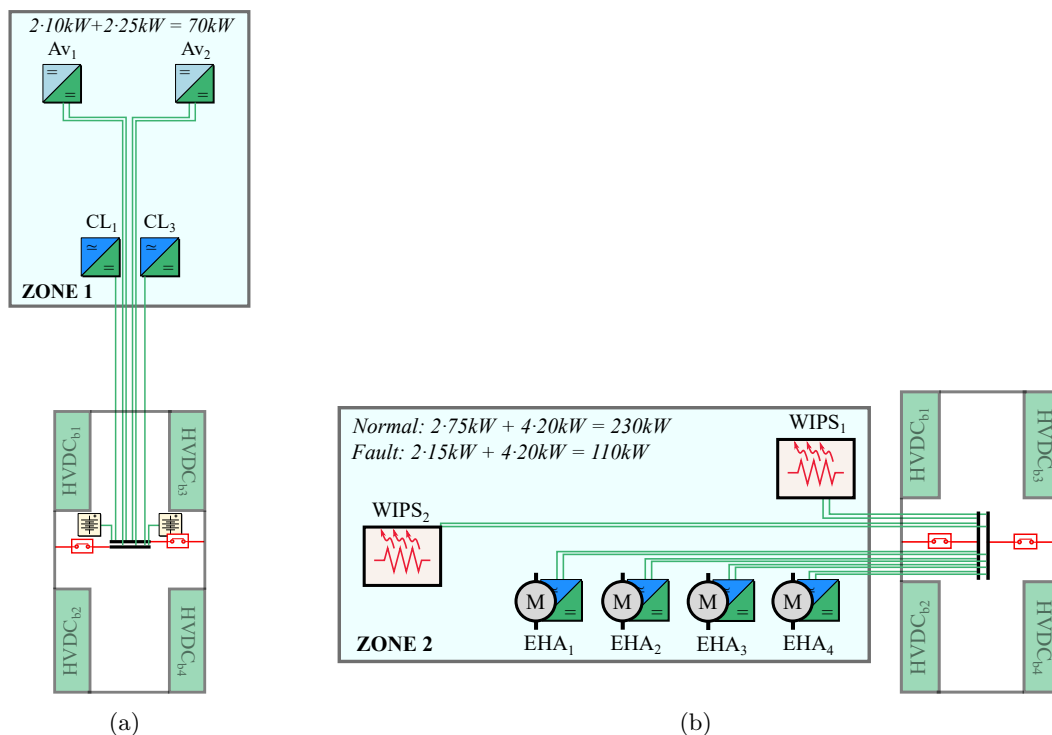
Figure 4.56 Schematics of (a) Zonal Load 1 load cable arrangement corresponding to the front side of the aircraft, and (b) Zonal Load 2 load cable arrangement corresponding to the left wing of the aircraft.

In the case of the bus-tie cable, though, a different power sizing approach has been considered which is linked to the defined load-shedding profile and described in the following. Aiming to size and design the protection devices and the cables that form the ring that interconnects the four HVDC buses, a load-shedding profile-based sizing approach has been employed as in the previous section. In this context, the existing symmetry between the buses and the zonal load cable interconnections is used to identify 4 main ring cable sections pointed in Figure 4.55(a):

- the cable interconnecting two neighboring buses at the front side, named as $Ring_{B-B}$ cable.
- The interconnecting cable between a busbar and the first matched Zonal Load, for example the cable between $HVDC_{b1}$ and Zonal Load 1, named as $Ring_{B-Z1}$ cable.
- The interconnecting ring cable section between the two different power rating zones, that are Zonal Load 1 and Zonal Load 2 or Zonal Load 3 and Zonal Load 4, named as $Ring_{Z1-Z2}$ cable.
- The interconnecting cable that symmetrically divides by half the frontside and the backside of the ring, i.e. Zonal Loads 1 and 3 from Zonal Loads 2 and 4, named as $Ring_H$ cable.

Assuming normal operating conditions (see Figure 4.57(a)), the power generated by a HVDC bus is the same as the power consumed by loads inside the ring, which is $150\,\mathrm{kW}$. Thus, under this operating condition there is no power is flowing through the $Ring_{B-B}$ cable and, due to the proposed load symmetry location inside the ring, either it is flowing through the $Ring_H$ cable.

Table 4.13 Cable distance and power rating required for the different aircraft loads and the summary of the calculated cable parameters for a cable efficiency of 99.1 %.

Cable	Distance [m]	Power [kW]	r_{Al} [mm]	Weight[kg]	R_{cable} [mΩ]	L_{cable} [μH]
Bus-Tie Switch						
$Ring_{B-B}$ cable	6	150	6.2	4.67	4.4	2.4
$Ring_{B-Z1}$ cable	1.2	300	3.9	0.38	2.2	0.49
$Ring_{Z1-Z2}$ cable	1.2	230	3.4	0.3	2.9	0.5
$Ring_H$ cable	1.2	65	1.8	0.09	10.2	0.54
Zonal Load 1						
$Busbar_{Z1}$			Negligible			
$Busbar_{Z1}$ to Ring cable	3	70	2.4	0.38	14.7	1.3
Av cable	25.5	10	3.3	5.87	66.2	10.65
CL cable	15.5	25	4.1	5.33	26.5	6.36
$HVDC_{b2}$						
$Busbar_{Z1}$ to Ring cable	3	230	5.4	1.8	2.9	1.2
EHA_1 cable	23	20	4.4	33.1	18.3	9.38
EHA_2 cable	18	20	3.9	5.77	33.1	7.41
EHA_3 cable	13	20	3.3	3.05	33.1	5.43
EHA_4 cable	8	20	2.6	1.18	33.1	3.42
$WIPS_1$ cable	8	75	5.1	4.2	8.8	3.23
$WIPS_2$ cable	28	75	9.5	75.73	8.8	10.97
EMA_1 cable	20.88	20	5.7	13.7	18.3	8.38

Figure 4.57 Simplified schematic to represent the amount of power transferred by the bus-tie switches (SSCBs) during (a) normal operation, (b) 1 SG failure operation and (c) 2 SG failure operation.

By the time that a SG fails, the HVDC bus connected to the faulty SG stops to deliver active power, and, hence, the VLs have to be fulfilled by the remaining three buses. As described by the load-shedding profile, the anti-icing WIPS loads are shed and, as represented in the example in Figure 4.57(b) and assuming an equal 120 kW power generation per available HVDC bus, 30 kW have to be supplied by the $Ring_H$ cable. An even worse case is given for this cable section when

only two out of four HVDC buses remain available for generating power (see Figure 4.57(c)), and thus, 65 kW have to be supplied through $Ring_H$ cable. Consequently, this power rating is considered as $Ring_H$ cable power rating in Table 4.13.

Note that, up to now, the $Ring_{B-B}$ cable has not been used for power transferring. Since this cable is employed to interconnect HVDC buses, ideally, no power will be flowing through it unless a fault occurs. In this regard, if a fault occurs in one of the $Ring_{Z1-Z2}$ cables as illustrated in Figure 4.58, all the power generated in HVDCb3 should be transferred to the loads through HVDCb1. Note that actually no generating power capability has been lost, and hence, no load-shedding should be applied. This operating scenario, indeed, leads to the worst-case operating condition, i.e. maximum power transferring, of $SSCB_{B-B}$, $SSCBB_{B-Z1}$ and $SSCB_{Z1-Z2}$ which have to conduct 150 kW, 300 kW and 230 kW, respectively.

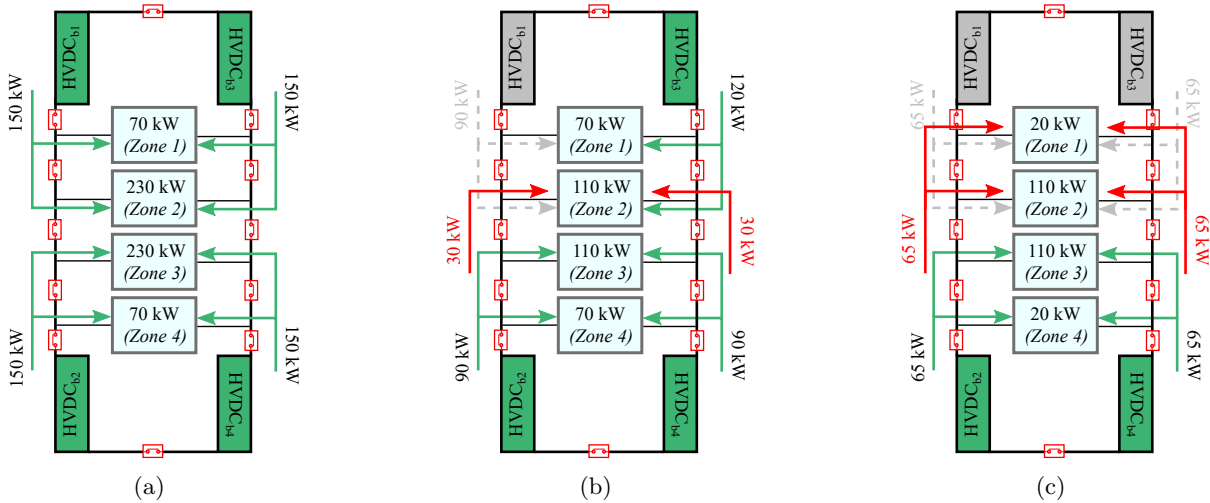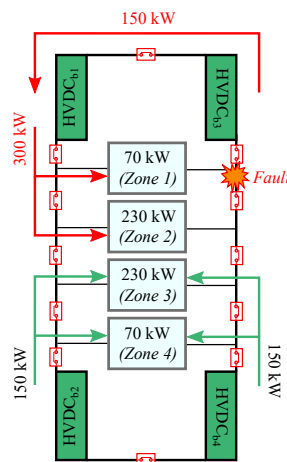**Figure 4.58** Simplified schematic to represent the amount of power transferred by the bus-tie switches (SSCBs) after a fault occurring in the $Ring_{Z1-Z2}$ cable section.

With all the cable lengths and power ratings defined, the weight of the overall DC EPS referred to cable weight is calculated using $(4.30)-(4.33)$ for a range of cable efficiency values between 99 % and 99.8 %. The results of the calculation are graphically presented in Figure 4.59. From the results, it is observed that the knee of the curve is achieved at a ≈ 99.5 % of cable efficiency, which is the same conclusion that has been previously obtained in the Multi-bus EPS design (also added in Figure 4.59 for comparative purpose). This conclusion results logical considering that the same cable design procedure is employed and the same aircraft structure, i.e. HVDC buses and loads locations, is used as baseline for both structures.

Figure 4.59 Results of the overall Ring-bus EPS cable weight calculation and comparison with the proposed Multi-bus derated EPS.

In terms of weight, though, $\approx 80\,\%$ of more weight is expected for the Ring-bus type topology (686 kg) compared to the derated Multi-bus approach when a 99.5 % cable efficiency is targeted. This fact makes Ring-bus topology not competitive in terms of weight and its consequent extra costs unless: *(1)* the proposed zonal load distribution and ca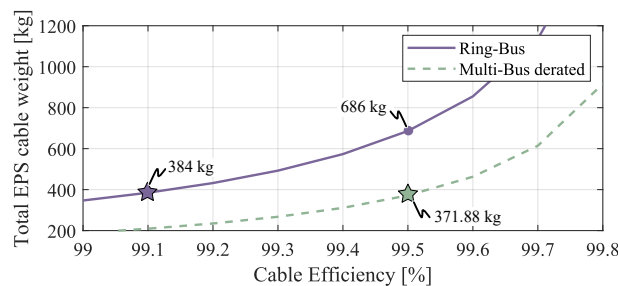ble connections are modified to reduce the overall cable weight, or *(2)* the targeted cable efficiency value is reduced so that the overall weight of the EPS results competitive, such as the point (91 %, 384 kg) in the curve.

Regarding the former potential weight reduction option, a slightly different ring-bus topology approach is presented in Figure 4.60(a) which is based in a six-zonal-load approach. Thus, aiming to reduce the amount of cable, the consumer loads are removed from Zonal Load 1 so that a Zonal Load 3 is established and is connected to the outside of the ring. This way, the cable distance is reduced by 5.5 m, which corresponds to the HVDC bus length. The main reason of this connection is that the NVLs do not require from four feeding paths as VLs do and, hence, this Zonal Load 3 can be connected only to one point of the ring.
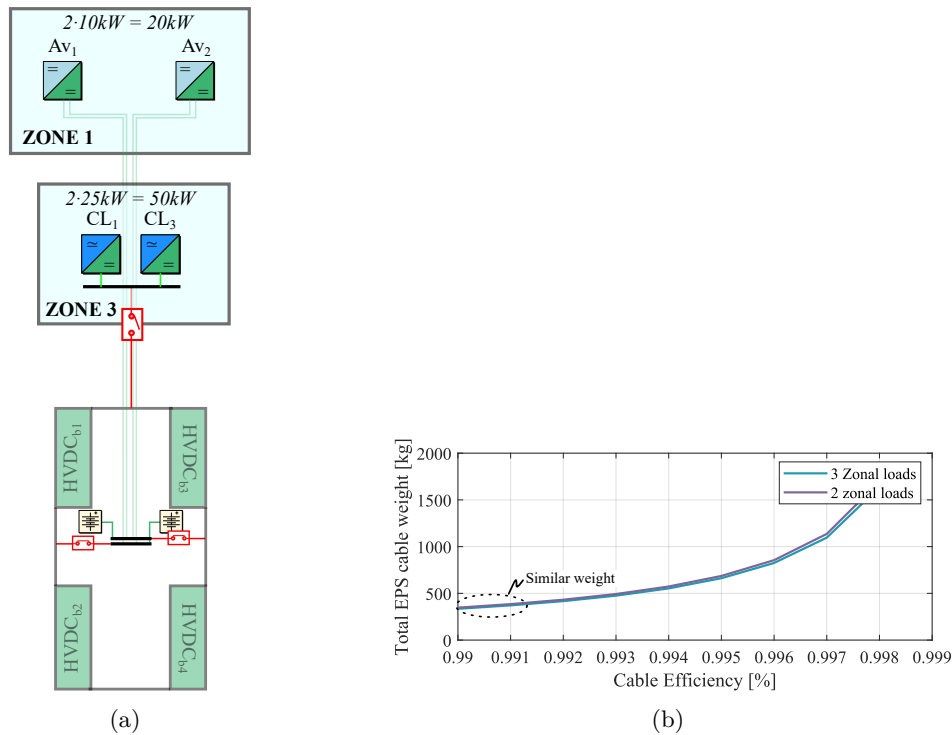
Figure 4.60 (a) Schematic of the alternative 6-zonal-load approach of the Ring-bus type topology and (b) its overall cable weight depending on the specified cable efficiency.

This six-zonal-load Ring-bus topology approach, however, has some drawbacks that should be considered. On the one hand, the fact of increasing the number of connections to the ring is translated into a higher number of protection devices required across the ring so that fail-safety and reconfigurability can be provided. As presented in Figure 4.60(a), an additional SSCB is required in the $Ring_{B\text{-}B}$ cable section so that $HVDC_{b1}$ and $HVDC_{b3}$ can be separated from the Zonal Load 3 in case of failure. This additional SSCB implementation, indeed, not only implies a higher complexity in terms of number of devices and its additional electronics required, but also in terms of their coordination as previously demonstrated in the $2L_{st}$ architecture protection analysis in Chapter 4.3.4. Furthermore, the $SSCB_{B\text{-}B}$ of the four-zonal-load original approach

does not conduct current during normal operation (see Figure 4.57(a)). With this six-zonal-load
approach, not only one but two SSCBs are conducting current during normal operation so that
the CL of the Zonal Load 3 are fed (see Figure 4.60(a)). On the other hand, if the overall
EPS cable weight is calculated (graphically depicted in Figure 4.60(b)), it can be observed that
no significant weight reduction is achieved with respect to the four-zonal-load approach for the
considered aircraft structure.

As a result, targeting a low cable efficiency is preferred in so that the four-zonal-load approach
results competitive in terms of weight with the Multi-bus EPS. Consequently, based on a targeted
cable efficiency of 99.1 %, the corresponding cable parameters calculations are done, i.e. R_{cable}
using (4.23), L_{cable} using (4.36) and the cable weight and diameter, and are summarized in
Table 4.13.

It must be taken into account that, when calculating the EPS overall efficiency for distribut-
ing power, not only the cable losses have to be considered, but also the ones of the protection
devices in the current path. In this sense, the presented ring-bus type topology, which is shown
in Figure 4.61(a) considering all the protection devices as SSCBs (typical in literature), not only
results to be harmed for having a high number of SSCBs in the distribution ring but also the ones
in the zonal load feeders. Thus, a low efficiency can be expected from this approach which addi-
tionally might require a complex coordination effort to achieve a high selectivity degree without
false tripping. In this regard, reducing the amount of SSCBs is proposed in Figure 4.61(b).
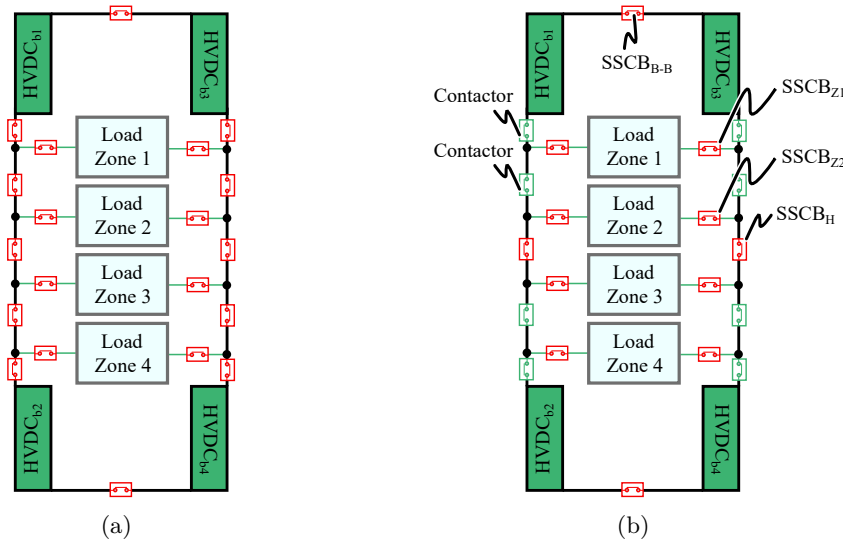
Figure 4.61 (a) Original EPS ring-bus type topology typical in literature and (b) proposed reduced SSCB-based
Ring-bus type topology.

On the one hand, the SSCBs in Ring$_{\mathrm{B\text{-}Z1}}$ cable and Ring$_{\mathrm{Z1\text{-}Z2}}$ sections are replaced by simple
contactors. This way, the related issue to the oversizing of the SSCBs in those sections is avoided
and a similar connection approach to the one of the Multi-bus EPS topology among the buses
is achieved. Note that, unlike in the Multi-bus topology, the cables to the loads are equipped
with SSCBs to avoid the fast fault propagation from one side of the ring to the other, i.e. from
the left side of the aircraft to the right side.

On the other hand, taking into account that during normal operation no current flows through the Ring$_\text{H}$ and Ring$_\text{B-B}$ cable sections, the protection devices to be employed are defined to be SSCBs. Particularly, the SSCB$_\text{H}$ is designed for a 65 kW nominal power as it is the Bus-Tie SSCB used in the Multi-bus EPS. Thus, the previously designed SSCB in Table 4.12 is employed and, consequently, the same SiC MOSFET module is selected for efficiency purposes. It has to be mentioned that in this case the line inductance corresponds to a higher value since, even if the same cable distance is found between HVDC buses (6 m) in the Ring-bus topology 5 cable sections are used. Thus, the connections among the cables have to be considered which, considering 500 nH per connected cable, leads to a line inductance increase of 5 μH. Note that each cable section is assumed to be divided into two real cables due to the SSCB connection in the middle of them. Accordingly, $R_\text{sn} > 3.85\,\Omega$ is required and, thus, a 8 Ω value is selected. The simulation results are presented in Figure 4.62 below.

Figure 4.62 SSCB$_\text{H}$ design results (a) when considering the overall inductance between two HVDC buses (7.41 μH), and (b)when considering the half of the inductance between two buses (7.41 μH /2).

Regarding the SSCB$_\text{B-B}$, the following parameters are calculated:

Table 4.14 150 kW SSCB design characteristics.

Parameter	Value
P_nom	150 kW
i_nom	555.55 A
i_rated	1111.11 A
R_cable	$4.4\,\text{m}\Omega + 2 \cdot 30\mu\Omega$
L_cable	$2.41\mu\text{H} + 2 \cdot 0.5\mu\text{H}$
i_trip	1330.4 A
$R_\text{cable-min}$	$4.46\,m\Omega$ /2
$L_\text{cable-min}$	$3.41\mu\text{H}$ /2
$i_\text{trip-max}$	1549.8 A
Device Rating	1200 V
MOV Model	*SMOV43-SV181*
R_sn	3 Ω
C_sn	6 μF

Considering that the SSCB rated power is 150 kW and the Ring$_\text{B-B}$ cable inductance is 3.41 μH, the approximated voltage clamping required for a defined text is defined in Fig. 4-60 for both the overall cable inductance and the half cable inductance. Aiming to extinguish the

fault current in a lower time than the $2L_{st}$ converter fuse melting ($\approx 25\,\mu s$), it is concluded from
the figure that:

- Power devices rated at $900\,V$ (or below) do not seem suitable for this concrete SSCB.
  Note that for these voltage rating devices, the active clamping voltage should typically be
  fixed around $700\,V \pm 10\,\%$. Thus, a maximum V_{MOV} clamping voltage of $500\,V \pm 10\,\%$ is
  expected so that enough voltage margin is considered. As a result, in the case of large
  impedance loads ($\geq 5\,\mu H$) it might be possible that the fuses melt before the SSCB trips.
  In fact, at $500\,V$ of V_{MOV} a current extinction time of $26\,\mu s$ is estimated to which the
  $2.77\,\mu s$ of fault detection and tripping time should be added. Therefore, the fault might
  be propagated throughout the other healthy sections of the EPS.

- Employing $1200\,V$ rated power devices is considered as a suitable option since, considering
  an active clamping voltage of $1000\,V \pm 10\,\%$, a relatively high V_{MOV} like $700\,V \pm 10\,\%$ can
  be assumed, which permits the fault current extinction time below $15\,\mu s$.
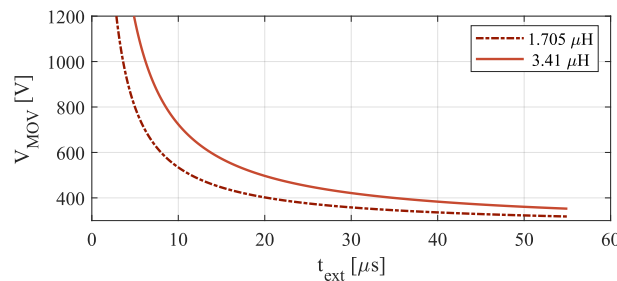
Figure 4.63 MOV clamping voltage depending on the fault current extinction time.

Therefore, the *SMOV43S-V181* MOV model is selected for the SSCB$_{B-B}$ too due to its
tripping current and voltage correlation. Based on this MOV V-I characteristic and the assumed
stray inductance of $400\,nH$, C_{sn} is defined as $6\,\mu F$ by iteration simulation method so that the
peak voltage caused by the stray capacitance does not achieve the minimum active clamping
voltage level of $900\,V$. The R_{sn}, on its behalf, is expected to be $R_{sn} > 1.5\,\Omega$ according to (4.16),
and hence, a $3\,\Omega$ value is selected. The graphical results of the SSCB$_{B-B}$ fault interruption
considering the cable inductance ($3.41\,\mu H$) and the half of it are presented in Figure 4.64.
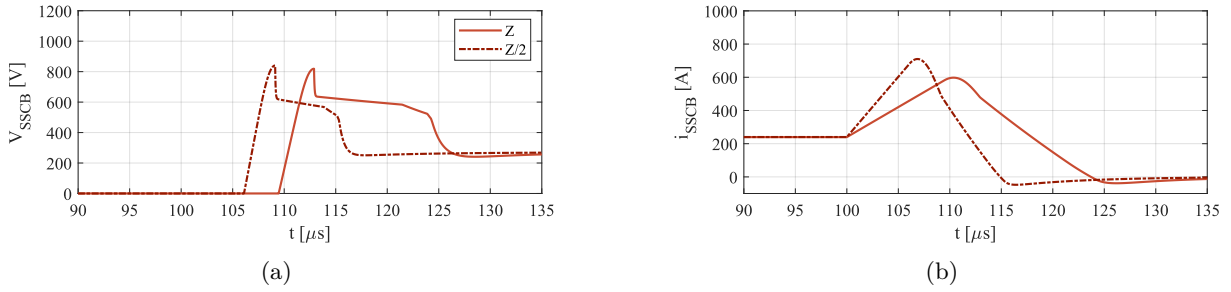

(a)

(b)
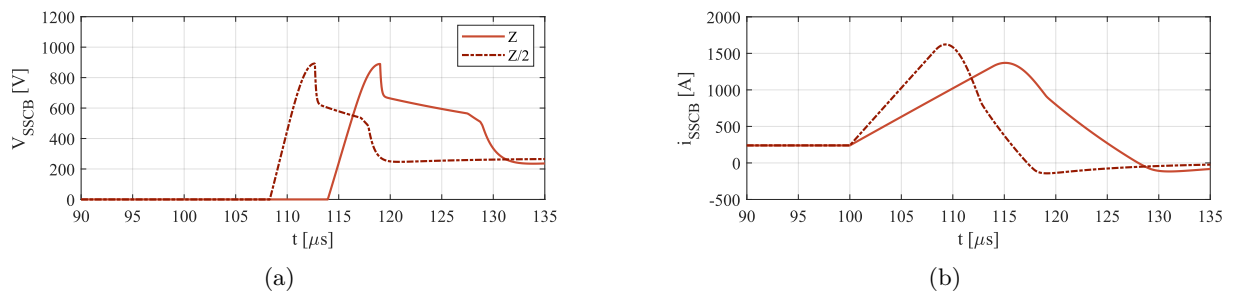
Figure 4.64 SSCB$_H$ design results (a) when considering the overall inductance between two HVDC buses
($7.41\,\mu H$), and (b)when considering the half of the inductance between two buses ($7.41\,\mu H$ /2).

Bearing in mind that for $99\,\%$ the targeted efficiency of the SSCBs in nominal conditions a
$2.73\,V$ voltage drop is calculated in (4.22) across the SSCB during nominal operation ($555.55\,A$),
the *CAB760M12HM3R* SiC MOSFET power module is selected as the employed power device

for the SSCB$_\text{H}$. Note that IGBTs are not contemplated since, as previously mentioned, a larger weight in terms of power module and heatsink is expected from an IGBT-based SSCB than from a SiC MOSFET-based one.

The main datasheet characteristics of the SiC power module are represented in Table 4.15, as well as the estimated heatsink thermal resistance required. This last parameter is calculated using (4.27) and based on the estimated V-I curve in Figure 4.65(a) at the worst-case temperature operating conditions, i.e. 175 °C, the corresponding power losses calculated as in (4.27) at the nominal operating conditions (2.73 V, 555.55 A). Based on the estimated worst-case V-I curve, the efficiency curve of the power device is calculated where a 98.95 % ($\approx$ 99 %) efficiency is calculated at nominal conditions.

Table 4.15 Relevant data of the proposed power device for the design of the 150 kW power device.

Parameter	SiC MOSFET
Model	Wolfspeed - *CAB760M12HM3R*
Rating	1200 V - 760 A
$T_{\text{j,max}}$	175 °C
Weight	175 g
Cost	2858.7 €
$R_{\text{th,h−amb}}$	0.016 °C/W

(a)

(b)
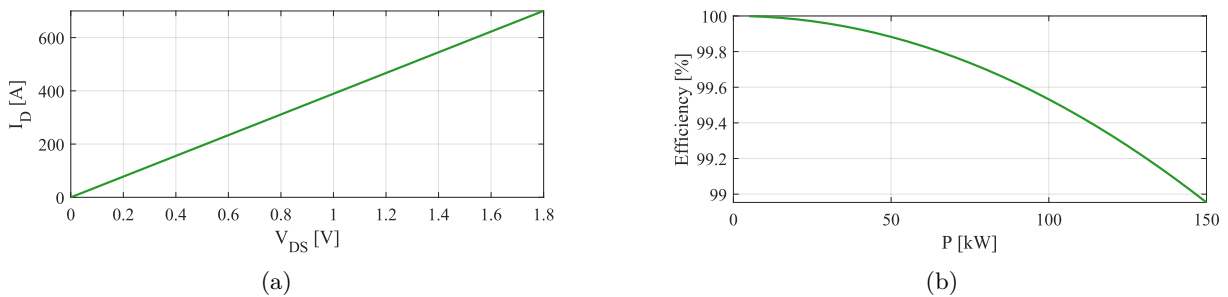
Figure 4.65 (a) output V-I characteristic of *CAB760M12HM3R* SiC MOSFET and (b) efficiency results.

Overall, based on the cable parameters and the calculated device data and, according to the defined load-shedding profile, the overall EPS efficiency results are presented in Figure 4.66 below. It is worth to mention that, even if the power devices related to the load-to-ring cables have not been selected, a similar efficiency approach to the selected devices is assumed. Hence, a 99 % efficiency is expected at nominal power and around a 99.7 % at half power (according to the curves of the SiC MOSFETs in Figure 4.48(b) and Figure 4.65(b).). The related SSCB$_\text{Z1}$ and SSCB$_\text{Z2}$ design data for the fault behavior analysis is presented in Table 4.16 and Table 4.17, respectively. Note that, in this case the tripping current is assumed to be a 25 % higher than the worst-case steady-state condition, i.e. when the DC voltage decays to 240 V according to the aviation standards.

Figure 4.66 Ring-bus EPS efficiency results according to the load-shedding profile scenarios.

Table 4.16 Zonal Load 1 SSCB (SSCB$_{Z1}$) design data.   **Table 4.17** Zonal Load 2 SSCB (SSCB$_{Z2}$) design data.

Parameter	Value
P_{nom}	70 kW
i_{nom}	259.26 A
i_{rated}	364.58 A
R_{cable}	14.7 mΩ + 30$\mu\Omega$
L_{cable}	1.3μH + 0.5μH
MOV Model	*SMOV43-SV251*
R_{sn}	5 Ω
C_{sn}	3 μF

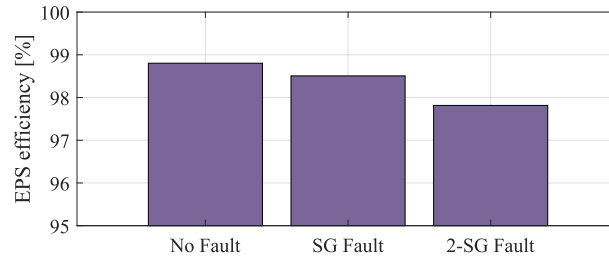| Parameter	Value
P_{nom}	230 kW
i_{nom}	851.85 A
i_{rated}	1197.9 A
R_{cable}	2.9 mΩ + 30$\mu\Omega$
L_{cable}	1.2μH + 0.5μH
MOV Model	*SMOV43-SV251*
R_{sn}	5 Ω
C_{sn}	5 μF

Fault Behavior Analysis

Finally, with all the four-zonal-load ring-bus EPS approach components designed, the operation of the protection scheme against several fault occurrences is tested, being Figure 4.67 the results for a 2L$_{st}$ converter fault, Figure 4.68 the results for a busbar fault, and Figure 4.69 the results for a WIPS$_2$ fault. It is worth to mention that the following simulation results, as in the previous case, do contain the "additional bus capacitor" so that the WIPS$_2$ load fuse is blown in case a fault occurs. Note that due to the inherent structure of the ring-bus EPS, this capacitor will influence in the faster speed of SSCBs operation. Especially the SSCBs located in the load-to-ring cables of zones 2 and 3.

Figure 4.67(a), 4.67(c) and 4.67(e) show the behavior of the system against a 2L$_{st}$ converter fault at HVDC$_{b1}$ occurring at $t = 0.012$ s from which the system is recovered approximately at $t = 0.02$ ms. As a top level-view it can be seen that the EPS survives to the fault, although the voltage drop in the HVDCb1 makes the bus voltage achieve a negative value.

As depicted in the zoomed view of Figure 4.67(b), right after fault occurs, the C_{link} voltage of the faulty converter is decreased to zero and the output current starts to quickly increase. Thus, due to the proposed Ring-bus EPS and the employed protection scheme, the SSCBs which isolate the faulty bus, being SSCB$_H$ and SSCB$_{B-B}$, operate faster than the fuse (see Figure 4.67(d) and 4.67(f)). Similarly, the results of SSCB$_{Z1}$ in Figure 4.67(c) and 4.67(d) show that this SSCB operates almost as fast as the bus-isolating SSCBs. This Zonal Load indeed takes the advantage of the connected batteries which provide an additional capacitance to the small buses of zone 1.

Due to the larger cable impedances in the zone 2, though, the SSCB$_{Z2}$ operates slower than the previous devices. However, the EPS system has been verified ensuring that no significant

voltage drop occurs in the other HVDC buses. Note that, since this SSCB is the one to operate last, it can be said that this device is the one extinguishing the fault propagation in $110\,\mu$s, which indeed is slower than the fuse (see Figure 4.67(d) and 4.67(f).
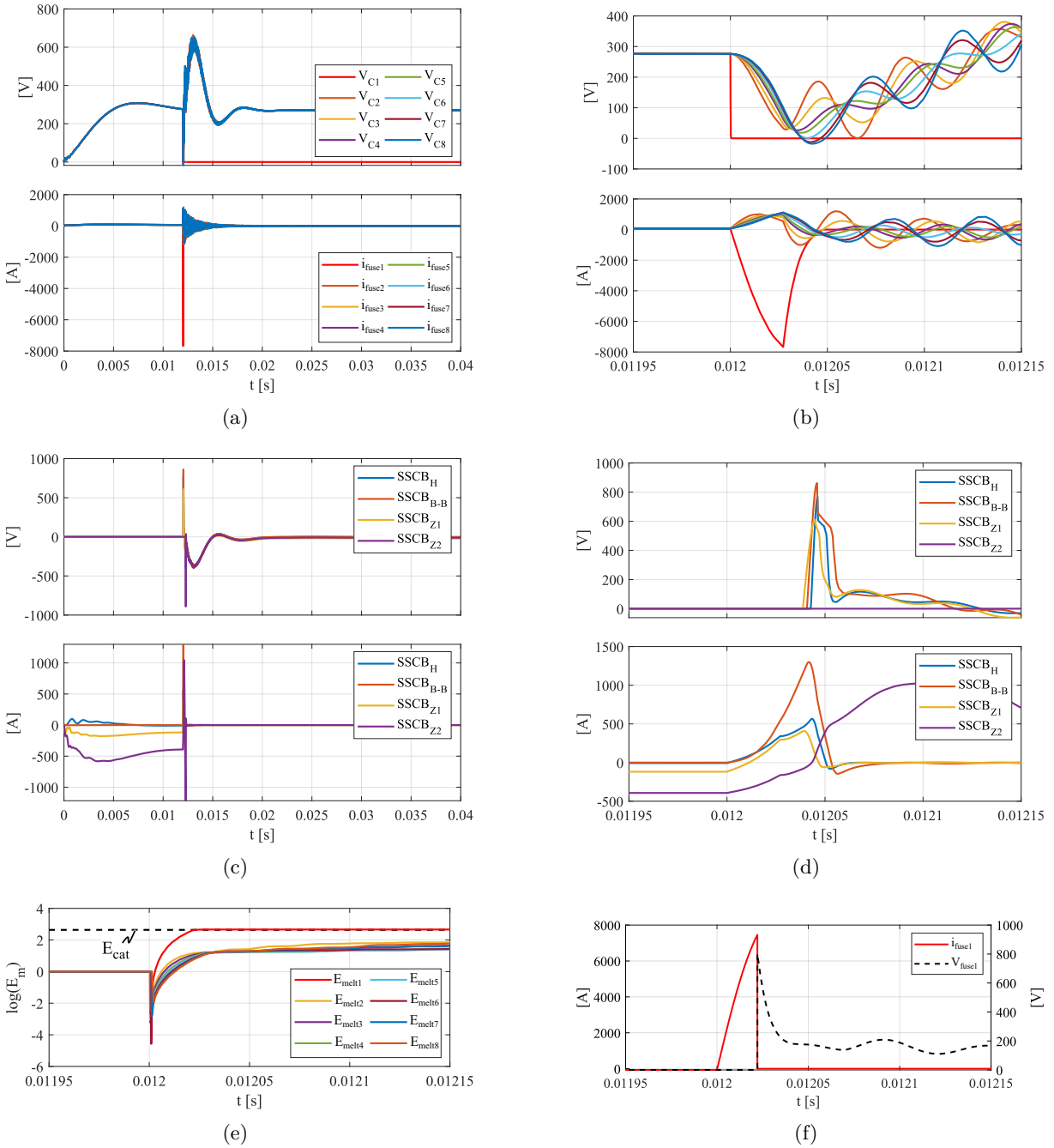
Figure 4.67 Ring-bus EPS simulation when a 2L$_{st}$ converter fault occurs. (a) voltage and current of the HVDC buses and (b) a zoomed view. (c) SSCB$_H$, SSCB$_{B-B}$, SSCB$_{Z1}$ and SSCB$_{Z2}$ voltage and current waveforms and (d) a zoomed view. (e) Melting energy of the 2L$_{st}$ architecture fuses and (f) fuse current.

Finally, it must be remarked that even if the HVDC$_{b1}$ reestablishes the bus voltage value to $270\,V_{DC}$ in 8 ms and that no sympathetic tripping occurs among the fuses in Figure 4.67(e), when the converter fault occurs the HVDC$_{b1}$ voltage decays to a value below zero. Consequently, no successful fault-clearing operation is achieved. On the positive side, this issue could be solve by increasing the HVDC$_{b1}$ capacitance. However, it will also suppose an additional volume and

cost to the EPS.

Aiming to analyze the EPS behavior when a bus fault occurs, a fault has been simulated in $HVDC_{b1}$ terminals. The results of the simulation are illustrated in Figure 4.68.
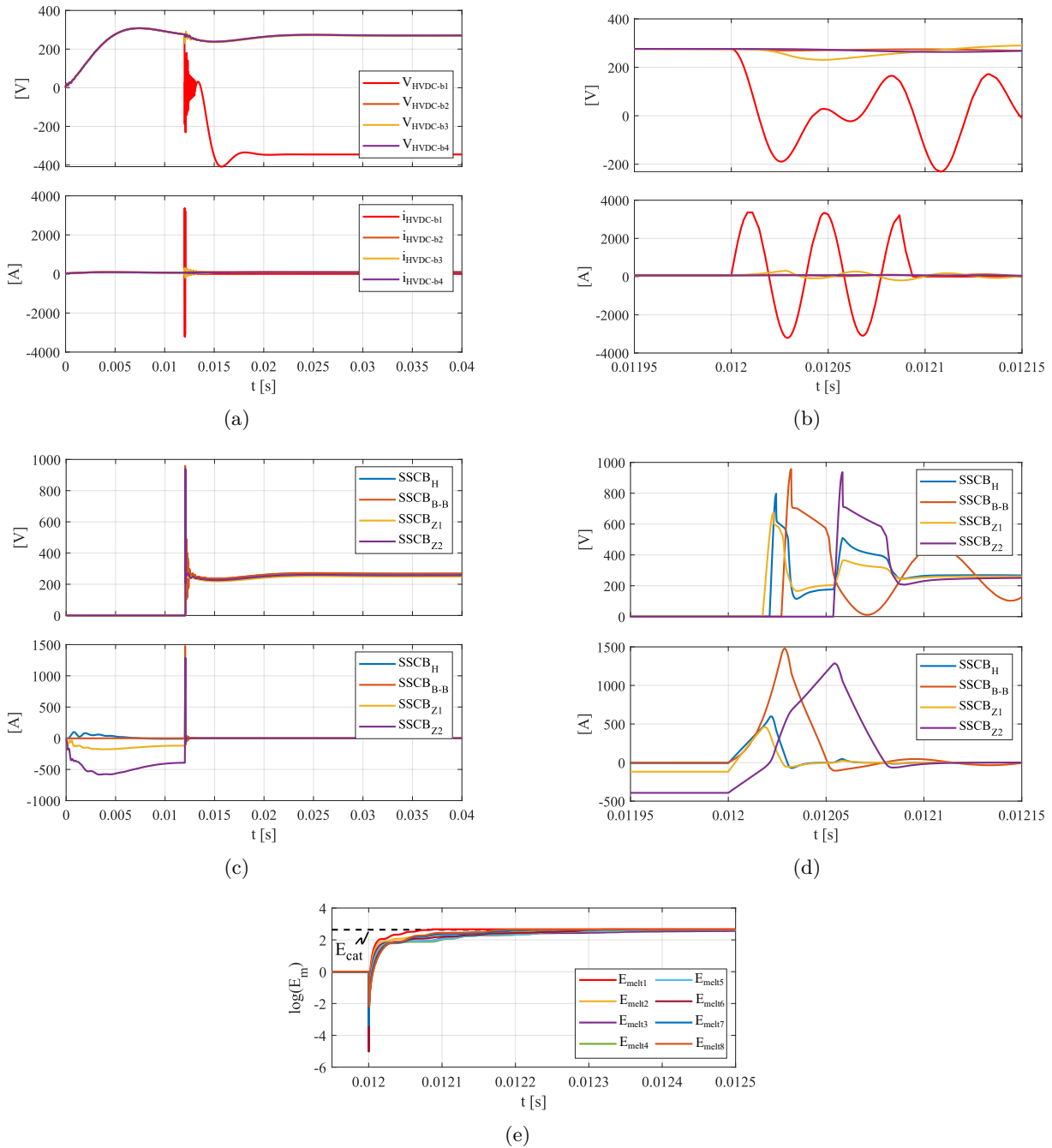
Figure 4.68 Ring-bus EPS simulation when a HVDC fault occurs. (a) voltage and current of the HVDC buses and (b) a zoomed view. (c) $SSCB_H$, $SSCB_{B-B}$, $SSCB_{Z1}$ and $SSCB_{Z2}$ voltage and current waveforms and (d) a zoomed view. (e) Melting energy of the $2L_{st}$ architecture fuses

The top-level view of the proposed Ring-bus EPS behavior against a busbar fault is presented in Figure 4.68(a), 4.68(c) and 4.68(e). As soon as the busbar fault occurs, the bus voltage level decays and oscillates around zero volts. Since the fault occurs at the terminals connecting $HVDC_{b1}$, the fault interrupting devices result to be $SSCB_H$, $SSCB_{B-B}$, $SSCB_{Z1}$ and $SSCB_{Z2}$,

as in the previous case. Particularly, in this case the interruption times result faster due to the lower fault impedance. In fact, SSCB$_H$, SSCB$_{B-B}$ and SSCB$_{Z1}$ stop the fault propagation in approximately $30\,\mu$s (see Figure 4.68(d)). Note that even if this interruption time doubles the operating time achieved in the Multi-bus approach no significantly harmful voltage drop occurs.

In the case of SSCB$_{Z2}$, a larger time is required to extinguish the fault ($\approx 70\,\mu$s). However, since no fault propagation occurs to the other buses or loads, the Ring-bus EPS behavior against bus faults is considered successful.

It must be considered, though, that for the simulated busbar fault, all the fuses of the architecture are blown (see Figure 4.68(e)). Note that the time required for the fuse blowing is extremely low, which makes difficult to switch-off the power devices of the converters when the overcurrent is detected, unlike in the Multi-bus busbar fault case.

Finally, in order to verify the suitability of the protection scheme for larger impedance loads, WIPS$_2$ load is short-circuited. The results of the simulation are presented in Figure 4.69. Particularly, Figure 4.69(a), 4.69(c) and 4.69(e) represent the top-level view of the EPS behavior where it is shown how the EPS is capable of surviving to a large impedance fault, although without considering the Zone 2 reconfiguration.

As presented in Figure 4.69(a), the HVDC buses survive to the fault with a slight overvoltage produced by the sudden disconnection of Zone 2 loads. Particularly, the fast isolation of the fault is achieved thanks to the additional capacitors added to the WIPS$_2$, which achieve a fault clearing time of $62\,\mu$s.

In this context, the larger fault inductance from the ring to the WIPS$_2$ load make the SSCBs to react in a larger time to isolate the faulty section of the EPS. Concretely, Figure 4.69(c) shows how the bus isolating SSCBs remain on, meaning that the fault has not been completely propagated to their section, while Figure 4.69(e) and 4.69(f) present the tripping of the Zone 2-to-ring SSCBs, i.e. SSCB$_{Z2-1}$ and SSCB$_{Z2-2}$. At this point, the fault propagation is completely stopped, being around $217\,\mu$s required.

The main issue here relies on the fact that even if the WIPS$_2$ fuses are blown, the zone 2 is isolated and remains isolated with a voltage level of $30\,$V (see Figure 4.70). Note that this voltage level is the one hold by the input capacitors of the loads. Consequently, the assumed large voltage drop makes complex the system reconfiguration due to the emerging large currents flowing from the HVDC buses, through the SSCBs and finally to the discharged converters of the loads. The main reason is that the appearing large reconfiguration currents might make the SSCBs of the zone 2 to trip again if no smooth capacitor charging is performed.

A simple idea to solve this issue is to add a start-up circuit in series with the ring-to-zoneSSCBs so that a smooth capacitor charging can be performed. The main drawback of this idea is that supposes additional components, weight and costs for the EPS which should also be contemplated in the analysis. Another possibility could be to employ SSCBs to protect the system from a load fault. However, this could significantly affect the EPS efficiency and the overall EPS complexity. An interesting approach, though, could result to change the connecting location of the batteries, so that in case of zonal load isolation, the battery connected to the

zonal load could operate to increase the system voltage and ease the reconfiguration. In addition, this possibility supposes no additional weight to the system.
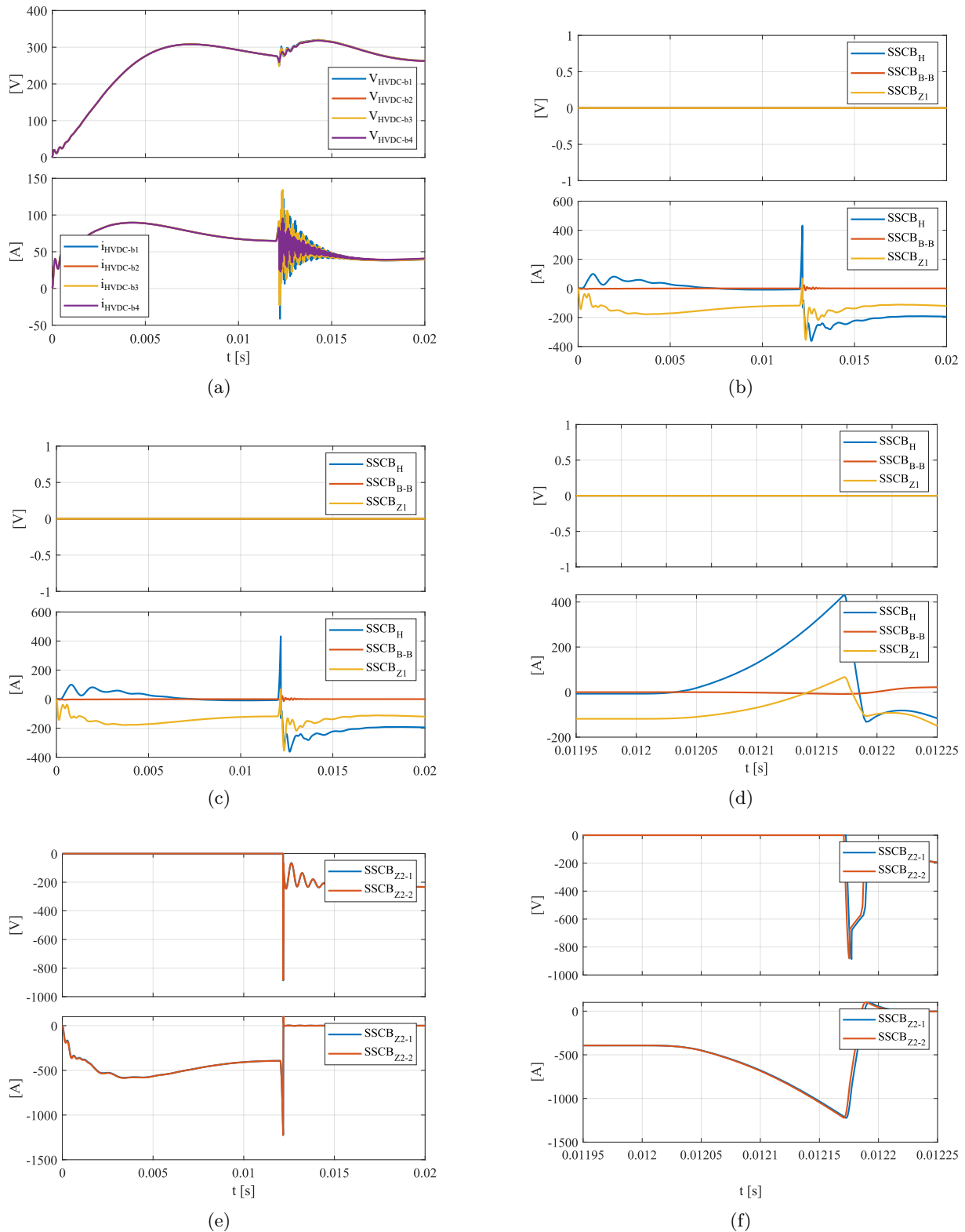

Figure 4.69 Ring-bus EPS simulation when WIPS$_2$ load is short-circuited (with no additional capacitance). (a) voltage and current of the HVDC buses and (b) a voltage and current at WIPS$_2$ load. (c) SSCB$_H$, SSCB$_{B-B}$ and SSCB$_{Z1}$ voltage and current waveforms and (d) a zoomed view. (e) SSCB$_{Z2-1}$ and SSCB$_{Z2-2}$ voltage and current waveforms and (f) a zoomed view.
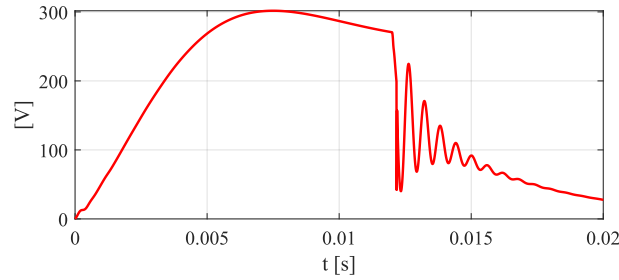
Figure 4.70 Zonal Load 2 voltage result.

4.6 Comparative Analysis of Aircraft EPSs

Based on the proposed comparison methodology a Multi-bus EPS and a Ring-bus EPS topology have been designed. In the following, the two proposed designs are compared considering two main analysis: *(1)* the "*steady-state*" behavior based on analytical results described in Table 4.18, and *(2)* the fault-analysis behavior based on simulation results and described in Table 4-17.

Table 4.18 Steady-state analytical results according to the established load-shedding profile.

Parameter	Multi-bus Topology	Ring-Bus Topology
Efficiency - Normal	99.5 %	98.8 %
Efficiency - 1 SG Fault	98.75 %	98.5 %
Efficiency - 2 SG Fault	98.11 %	97.81 %
Overall EPS Weight	$371.87 + 8.67 = 380.54\,\mathrm{kg}$	$384.87 + 54.37 = 4.39.2\,\mathrm{kg}$
Number of SSCBs	4	20
Survivavility - Normal	28/28	28/28
Survivavility - 1 SG Fault	24/28	24/28
Survivavility - 1 Busbar Fault	22/28	24/28
Survivavility - 2 SG Fault	20/28	20/28

The steady-state analysis is mainly focused in the efficiency, weight, complexity and survivability of the EPS according to the different load-shedding scenarios. According to the results in Table 4.18, the Multi-bus approach achieves a higher efficiency in the three scenarios, although a relatively low difference is estimated between both designs ($< 1\,\%$). The fact that the cables of the Multi-bus approach where targeted for a higher efficiency ($99.5\,\%$) make this topology take advantage in the efficiency scenario. Moreover, the ring-bus topology assumes 16 additional SSCBs which are in the main source-to-load paths and, hence, the efficiency parameter is also harmed. Note that, the additional SSCBs not only suppose additional electronics and system complexity, but also additional weight.

As previously stated, a lower efficiency of the ring-bus EPS has been assumed so that, in terms of weight, both topologies could be competitive. This objective, indeed, has been achieved in terms of cable weight, being $371.87\,\mathrm{kg}$ in the Multi-bus approach against $384.87\,\mathrm{kg}$ in the ring-bus approach. Here, again, the increased number of SSCBs results harmful. Concretely, the Multi-bus approach possesses a total SSCB power rating of $260\,\mathrm{kW}$, that is based on four bus-tie SSCBs of $65\,\mathrm{kW}$ rated power, supposing 8.67 additional kilograms. Contrarily, the Ring-

bus approach possesses a total of 20 SSCBs which suppose a total power rating of $1630\,\mathrm{kW}$ and, consequently, 54.33 additional kilograms according to the expected $30\,\mathrm{kW/kg}$ power density of the SSCBs. As a result, a $15\,\%$ ($59\,\mathrm{kg}$) difference is estimated for the designed EPS, being advantageous the Multi-bus topology.

In terms of survivability similar results are expected from both topologies, which partly, is an expected feature considering that the proposed designs have considered a maximization of survivability. Particularly, the Multi-bus topology results less reliable in this aspect, since a NVL is only connected to one bus and, thus, if a busbar fails the NVLs of that busbar have to be considered as lost during the flight.

Regarding the fault behavior of the proposed EPSs, even if a more reliable operation is expected from the ring-bus topology, a simpler, faster and more robust behavior is found for the Multi-bus approach. On the one hand, when a $2L_{st}$ converter occurs, both topologies result survivable and reconfigurable. Ring-bus topology achieves a faster fault clearing time, although it requires for a longer time to achieve reconfiguration. Moreover, for the considered busbar impedances and DC-link capacitors, the zero voltage is crossed when a $2L_{st}$ converter fault occurs due to the complete HVDC bus isolation and lack of additional fault energy supplying capacitors to blow the fuse of the faulty converter. Thus, a higher value DC-link capacitors should be assumed to fulfill the no-zero-crossing aviation standard, which supposes additional weight to the EPS.

Table 4.19 Fault behavior simulation results according to the established $2L_{st}$ converter fault, HVDC busbar fault and $WIPS_2$ load fault.

Parameter	Multi-bus Topology	Ring-Bus Topology
$2L_{st}$ rectifier fault		
Fault Clearing Time	$65\,\mu s$	$55\,\mu s$
Time to Recovery	$5\,\mathrm{ms}$	$8\,\mathrm{ms}$
Nº of operating devices	3 ($SSCB_{12}$, $SSCB_{13}$, fuse)	5 ($SSCB_{BB}$, $SSCB_H$, $SSCB_{Z1}$, $SSCB_{Z2}$, fuse)
Minimum DC bus voltage	$45\,\mathrm{V}$ ($HVDC_{b1}$)	$-5\,\mathrm{V}$ ($HVDC_{b1}$)
Survivable to fault?	Yes	Yes but $V_{DC} = 0$ crossed
$HVDC_{b1}$ fault		
Fault Clearing Time	$50\,\mu s$	$70\,\mu s$
Time to Recovery	Negligible	Negligible
Nº of operating devices	2 ($SSCB_{12}$, $SSCB_{13}$)	4 ($SSCB_{BB}$, $SSCB_H$, $SSCB_{Z1}$, $SSCB_{Z2}$)
Minimum DC bus voltage	$265\,\mathrm{V}$ ($HVDC_{b2}$)	$240\,\mathrm{V}$ (remaining buses)
Survivable to fault?	Yes	Yes
$WIPS_2$ load fault		
Fault Clearing Time	$55\,\mu s$	$62\,\mu s$
Time to Recovery	$20\,\mathrm{ms}$	$20\,\mathrm{ms}$ (without considering reconfiguration)
Nº of operating devices	3 ($SSCB_{12}$, $SSCB_{13}$, fuse)	3 ($SSCB_{Z2-1}$, $SSCB_{Z2-2}$, fuse)
Minimum DC bus voltage	$45\,\mathrm{V}$ ($HVDC_{b1}$)	$30\,\mathrm{V}$ (Zonal Load 2)
Survivable to fault?	Yes	Yes with additional start-up circuitry

On the other hand, when a bus fault occurs a similar behavior is expected between both EPS

topologies. In fact, the time to recover is negligible, since almost no voltage drop occurs when the bus-tie SSCBs trip, and the fault is cleared at relatively low times. The main difference relies on the number of operating devices required, being two SSCBs for the Multi-bus approach and four for the ring-bus topology.

Finally, the $WIPS_2$ fault, or large impedance fault results distinguishing. Particularly, the fault clearing and recovering times are very similar in both topologies since, actually, the fault clearing process is performed by the load fuse and the additional capacitor attached to deliver the fuse blowing energy. However, it is the proper EPS topology the one that makes them distinguishable. In the case of the Multi-bus approach, when the $WIPS_2$ fault occurs, the HVDC bus and its attached loads are isolated from the rest of the aircraft. Then, the fault is cleared, and the active modular architecture delivers the required energy to recover the system voltage in around 20 ms. In the case of the ring-bus topology, though, it is the zonal load 2 the EPS section that is isolated. Thus, once the $SSCB_{Z2-1}$ and $SSCB_{Z2-2}$ operate and isolate the Zonal Load 2 section, no power feeding is permitted into the section and, hence, after the fault clearing, the Zonal Load voltage stays at a relatively low voltage level, being 30 V in this case. Consequently, the existing voltage difference with respect to the rest of the EPS results in a reconfiguration complexity and even false SSCB tripping if no additional measures are considered. Among the proposed solutions, changing the location of the batteries results interesting so that each zonal load has a battery to, in the case the Zonal Load has been isolated, increase the voltage level to the 270 V system voltage and ease the reconfiguration while avoiding false SSCB tripping.

To sum up, the Multi-bus approach result advantageous for the defined aircraft application and $2L_{st}$ architecture integration not only due to the increased efficiency and reduced weight, but also because of the fast operating speed against faults, simplicity and easy reconfiguration possibilities. It is worth to mention, though, that the ring-bus topology presents an interesting potential which could be increased with a higher distribution voltage and, hence, an expected lower cable weight.

4.7   Summary

The implementation of a HVDC distribution-based MEA EPS provides certain advantages like high power density, due to a reduced number of cables or high efficiency, related to the low-impedance nature of the compact DC EPSs. Establishing a low impedance DC network, though, brings complex challenges along, especially in terms of DC short-circuit protection. Concretely, the lack of zero-crossing of the DC short-circuit current and its fierce initial transient due to the discharge of the DC-link capacitors make the DC fault management, i.e. fault detection, fault isolation and EPS reconfiguration, a high complexity task. Since the reliability of supply is considered as a crucial feature of the aircraft EPS, analyzing the proposed $2L_{st}$ architecture behavior against DC faults and its protection becomes a research focus.

In this regard, a literature review on DC protection devices has been done to identify the pros and cons of each protecting system alternative and implement them for $2L_{st}$ architecture protection. After a discussion and DC converter fault simulation analysis, it is concluded that

a fused-based protection results a suitable option which provides high efficiency and simplicity. The SSCB, though, becomes an interesting alternative for bus-tie applications.

Thus, it is aimed to integrate the $2L_{st}$ active modular architecture into the MEA EPS and analyze the system behavior against DC short-circuit faults. Since few literature is found about the DC EPS to be used in MEA applications, a comparative analysis has been performed among the Multi-bus DC EPS approach and a four-zonal-load base ring-bus topology approach. The design criteria according to the load-shedding profile has been presented, and a comparative methodology has been suggested which, based on a defined EPS structure and a load-shedding profile, evaluates an EPS in terms of efficiency, weight, survivability and operating speed.

From the results, the Multi-bus approach results preferrable to for the defined application and for integrating integrate the $2L_{st}$ architecture due to its inherent simplicity, higher efficiency and lower weight, which indeed, is translated into lower costs. Moreover, the fault behavior, i.e. fault clearing time, reconfigurability and survivability after fault, results similar in both Multi-bus and ring-bus topologies, although for the considered aircraft structure, reconfigurability might be harder for the ring-bus type topology in case of a zonal load results isolated.

CHAPTER **5**

Conclusions and Future Work

Summary:

This final chapter summarizes the research work done in this PhD thesis. The most relevant conclusions of the work are described along with its main contributions. Future work research lines related to the presented work are also presented aiming to continue with the research.

5.1   Conclusions

Aiming to reduce the pollution caused by the traditional aircraft, strong research efforts are done towards the aircraft electrification to reduce the fuel usage. Thus, high efficiency, high power density and high reliability are some of the main characteristics expected from the future MEA, among others. The higher the electrification of the aircraft loads, on its behalf, demands for a higher electric power generation capability and efficient conversion and distribution across the aircraft EPS. In this context, the development of a HVDC-based aircraft distribution grid with bidirectional power flow capability results an interesting alternative to increase the distribution efficiency, reduce cable weight and provide bidirectional power-flow capability. Conversely, the currently employed AC/DC rectifiers, i.e. ATRUs, are composed of bulky passive elements and cannot provide bidirectional power-flow.

In this regard, this PhD thesis focuses on replacing the conventional AC/DC converters for a high-efficient, high-power-dense, fault-tolerant and bidirectional active modular rectifier architecture which enhances the implementation of a HVDC primary distribution-based MEA EPS. For that purpose, the potential active AC/DC topologies for the defined application have been reviewed and their suitability in MEA applications has been studied. Since the input/output voltage operating requirements of the current aviation standards are based on the passive ATRU, that are $115\,\mathrm{V_{AC}}$ and $270\,\mathrm{V_{DC}}$, controllability limitations are found when pretending to implement an active AC/DC operating at unity PF. Particularly, the output DC voltage to be controlled by active rectifier is required to be higher than the one imposed by aviation standards in unity PF operation is desired.

To solve this issue, two alternatives have been proposed: *(1)* employing a two-stage power converter which operates at unity PF, being an AC/DC converter followed by a downstream DC/DC buck converter, and *(2)* employing a single-stage AC/DC converter which worsens its PF to a value lower than unity. Considering these two scenarios and taking into account different semiconductor technologies, an analytical performance evaluation has been done among the identified potential active AC/DC topologies which, afterwards, are benchmarked against a traditional ATRU. The aim of this comparative analysis is to identify the most suitable topology and configuration according to the MEA operating requirements. From the results, two-level boost topology configurations emerge as the most promising candidates. Especially, when relatively high switching frequencies ($80 - 100\,\mathrm{kHz}$) can be reached, which is achieved by implementing SiC MOSFET semiconductors.

Once the topology identified, a study regarding the integration both single-stage and two-stage configurations into an active modular architecture which complies with the aviation standards is performed. Thus, aiming to achieve unity PF on the AC-side (SG), three different converter configurations are proposed for developing the active modular architecture: a two-stage configuration ($2\mathrm{L_2}$), a single-stage configuration with an input capacitor bank for PF compensation ($2\mathrm{L_C}$), and a single-stage configuration with an additional STATCOM for PF compensation ($2\mathrm{L_{st}}$). Based on each proposed converter configuration, the respective $2\mathrm{L_2}$, $2\mathrm{L_C}$ and $2\mathrm{L_{st}}$ active modular architectures are designed for complying with DO-160G standard in

terms of operating requirements, power quality and HF harmonics in differential mode.

Afterwards, a highly detailed comparison framework is suggested aiming to compare the three proposed modular architectures and identify the most suitable architecture to be implemented in MEA applications. Thus, the comparison framework is based on efficiency (targeting a $> 97\%$), power density (referred to the volume of the passive elements and cooling system), reliability (considering wear-out and cosmic radiation-produced failures) and simplicity and costs (expressed as the number of semiconductors required per architecture). From the comparative analysis, it is concluded that the $2L_{st}$ architecture presents a high potential in terms of efficiency, simplicity and volume. Besides, when three redundancies are considered, the large volume related to the stored energy in $2L_C$ architecture, and the relatively large number of power devices required for the $2L_2$ architecture (almost doubled with respect to the $2L_{st}$ architecture) make these architectures inadequate. Consequently, the $2L_{st}$ architecture has been selected as the preferred option not only because lower complexity and costs are expected, but because a relatively low volume is achieved while providing high efficiency, high power quality, and a high redundancy degree.

Finally, the implementation of the $2L_{st}$ architecture into the MEA EPS and its behavior against DC faults has been studied. Since the reliability of supply is considered a crucial feature of the EPS, the fact that the proposed $2L_{st}$ architecture provides a fault-tolerant capability is identified as interesting. Due to the low-impedance nature of the DC EPS, a literature review of the employed DC protection systems has been performed from which, because of their fast-operating speed, fuse and SSCB protection devices are considered the potential protection devices to be employed. The simplified modeling procedure of both protection devices has been presented and, by simulating a rectifier fault, it is observed that the relatively fast fault current increase makes the fuse preferable because no sympathetic tripping occurs as with SSCBs.

However, when implementing the $2L_{st}$ architecture into a MEA EPS, the overall EPS fault behavior as well as the one of the $2L_{st}$ architecture against external faults should be analyzed. In this context, few literature is identified about the suitable MEA DC EPS topologies. Thus, a comparison methodology is proposed which, based on a defined EPS structure and load-shedding profile, pretends to evaluate an EPS in terms of efficiency, weight, simplicity, survivability and fault clearing operating speed. Based on the suggested methodology, the multi-bus radial type and the ring-bus type DC EPS topologies are designed and compared.

As a result of the performed comparative analysis, the Multi-bus approach results preferable in terms of simplicity, efficiency and weight. Furthermore, similar fault clearing and recovery times are achieved in both EPS topologies. Nevertheless, for the considered aircraft structure, reconfigurability and post-fault survivability might be harder for the Ring-bus type topology in case of a zonal load results isolated.

5.2 Contributions

The main research contributions of this PhD thesis are summarized in the following:

- **Suitability analysis of active AC/DC rectifier topologies operating according to the aviation input/output operating requirements.**

  Based on a mathematical approach, the operating limitations of active rectifiers have been analyzed so that the up-to-date aviation standard requirements can be fulfilled, i.e. $115\,V_{AC}$ input voltage and $270\,V_{DC}$ output voltage. As a result, two main solutions are proposed: *(1)* to employ a two-stage converter if unity PF operation is desired, i.e. an AC/DC and a downstream DC/DC, and *(2)* to reduce the operating PF of the converter to a value lower than unity (such as the 0.85 lagging in DO-160G) if a single-stage converter is desired. Based on a technical approach and considering both converter configurations, several active rectifier topologies are benchmarked against the ATRU demonstrating that active rectifier are suitable to replace the ATRU. Further, it is demonstrated that the single-stage configuration presents a high simplicity and efficiency potential.

  $\longrightarrow$ *Refer to publication A.*

- **Design and comparison of the three proposed active modular rectifier architectures complying with aviation standards.**

  Based on the two-level boost topology and considering the proposed two-stage and single-stage converter concepts, three main converter configurations are proposed to establish an active modular architecture which operates at unity PF: the two-stage configuration $2L_2$, the single-stage configuration with capacitor bank $2L_C$ and the single-stage configuration with STATCOM $2L_{st}$. The design criteria of the three proposed active modular architectures have been presented as well as the DM filter design criteria for LF and HF harmonics fulfillment. In this context, a minimum volume DM filter design criterion is proposed for the $2L_2$ converters and a study on the limitations related to different single-stage rectifiers is suggested, being the study of PF and minimum volume design criteria for the $2L_C$, and the reduction of the number of STATCOMs for the $2L_{st}$ architecture. Finally, a comparative analysis has been suggested focusing on efficiency, power density (referred to volume) and reliability, which are crucial in aircraft applications.

  $\longrightarrow$ *Refer to publication B.*

- **Proposed comparison methodology for compact DC EPS based on a defined EPS structure and a load-shedding profile.**

  Multi-bus and ring-bus type DC EPSs are studied in this work. Due to the different expected characteristics in terms of power distribution efficiency, weight, survivability to a fault and fault clearing speed, a comparison methodology is proposed in this work to find the most suitable DC EPS approach for aircraft application. The proposed methodology combines analytical and simulation studies, and is based on a predefined EPS structure (i.e. loads and power sources location) and a load-shedding profile which describes the operating behavior of the EPS in order to avoid a power generation and consumption mismatch in case of loosing a power source.

In addition to the main contributions, another contribution to the State-of-Art has been done based on the research methodologies described throughout the document:

- **Comparative evaluation of active TRU topologies operating according to the aviation input/output operating requirements.**

  Based on an analytical and simulation approach, a comparative analysis among active TRU topologies has been performed using the comparison framework described in this PhD work. In this case, though, the compared topologies have to fulfill different operating requirements due to the naturalness of the TRU application, i.e. $115\,\text{V}_{\text{AC}}$ input voltage and $28\,\text{V}_{\text{DC}}$ output voltage and the requirement of isolation. First, a qualitative analysis is suggested among literature topologies, resulting in phase-modular Flyback and Dual-Active Bridge (DAB) as preselected suitable topologies for Regulated TRU operation. Thus, both topologies are compared in terms of reliability, efficiency, semiconductor stress and converter volume. As result, a high-power isolated AC/DC Flyback topology based on phase-modular single-stage structure for MEA is presented.

  $\longrightarrow$ *Refer to publication C.*

List of Publications

In the following, the technical papers which have been published in international conferences and journals during the course of this research work are presented:

A. **U. Atutxa**, I. Baraia-Etxaburu, V.M. Lopez, A. Rujas, "Suitability and Performance Evaluation of Active Rectifier Topologies for More Electric Aircraft", in *2021 IEEE Vehicle Power and Propulsion Conference (VPPC)*. IEEE, Gijón (Spain), oct. 2021, p.p. 25–28.

B. **U. Atutxa**, I. Baraia-Etxaburu, V.M. Lopez, F. Gonzalez-Hernando, A. Rujas, "Multi-Objective Comparative Analysis of Active Modular Rectifier Architectures for a More Electric Aircraft", *Aerospace*, vol. 9, no. 98, p. 22, feb. 2022.

C. **U. Atutxa**, A. García, A. Rujas, D. Izquierdo, J. Meneses, "Comparison of Active Transformer Rectifier Unit Topologies for More Electric Aircraft", in *The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)*, IET, Online, dec. 2020, p.p. 15-17.

5.3 Future Work

Along this research work, the suitability of active AC/DC rectifiers has been evaluated with the aim of designing and validating by simulation methods the implementation of a bidirectional active modular rectifier architecture in MEA applications which provides high efficiency, high power density and high reliability characteristics. However, aiming to enhance the integration of this architecture into the MEA EPS and establish a HVDC-based distribution network, there are some issues and research lines that have been identified for future research:

- **Analysis on the motoring mode of the $2L_{\text{st}}$ active modular architecture and the SG.** Since the performed analysis focuses mainly in the rectifier operation of the $2L_{\text{st}}$ active modular architecture, researching on the inverter operation is considered as

a future research task. Thus, the architecture control, protection and analysis during inverter operation and SG starting transients becomes interesting.

- **Experimental validation of protection scheme.** Since the performed research analysis on the protection of the $2L_{st}$ architecture as well as on the protection of the EPS is based on a theoretical analysis, the real implementation becomes an interesting focus. This research line could be used to experimentally verify the protection systems modeling as well as their operating behavior against faults. In addition, even if the single-stage operation of a single converter prototype was verified, the larger implementation of the complete architecture results a research challenge in therms of validating the complete architecture operation and analyze its operating behavior against internal and external faults.

- **Fault detection techniques and algorithms.** As described in Chapter 4, the DC fault management comprehends fault detection, fault isolation, and post-fault reconfiguration. In this regard, the employment of SSCBs for protecting the $2L_{st}$ modular architecture has been studied. It has been described how the time delay that occurs since the fault should be detected up to the time that the SSCB operates could be around $2.77\,\mu$s. Thus, during this time delay the fault current might increase significantly so that an increasingly overrated power device must be employed to ensure the safe tripping operation of the SSCB. Therefore, innovative fault detection algorithms and developing faster measuring devices result interesting so that the time delay is diminished and a fast and safe SSCB operation can be employed without excessive device overrating.

- **Electromagnetic Compatibility (EMC) Analysis.** Currently, a strong trend around reducing the power converters volume exist. In this context, increasing the switching frequency, as demonstrated during this work, results key for decreasing the filtering passive elements that a converter has. However, increasing the switching frequency does also mean to increase the switching frequency related harmonics. In this work, concretely, a $80\,$kHz switching frequency has been defined for the $2L_{st}$ architecture converters. Thus, the switching frequency harmonic multiples emerge in a frequency range ($> 150\,$kHz) in which the common impedance might result to be lower than the differential model impedance. Consequently, the study and characterization of the $2L_{st}$ architecture impedance as well as the common mode filter design becomes of special interest.

APPENDICES

APPENDIX A

Simulation Models and Multi-Level Modeling Approach

A.1   Definition of Model, Modeling and Simulation

This appendix pretends to make the reader familiarize with the concepts of modeling and simulation in MEA EPS applications as described in [2, 9, 160]. Initially, the concepts of model, modeling, and simulation are defined aiming to describe later the idea of multi-level modeling and its relation to the MEA EPS.

- **Model:** it refers to a conceptual representation of a concrete phenomena or to some precise aspect(s) of it. Thus, depending on the phenomena under study a system or a component can be described by different models.

- **Modeling:** it represents the process of generating the model. For example, the fact of getting a power converter model by means of experimental modeling or software modeling. In the case of software modeling, several software packages can be found such as *Matlab-Simulink*, *PLECS* or *PSIM*. Note that software modeling is the process employed in this research work.

- **Simulation:** describes the process of the model implementation. Thus, the simulation is used to answer the behavior of the modeled phenomena. In the case of MEA EPS and its subsystems, for example, the simulation is used to set an operational mode and extract the relevant measures to understand the phenomena under research.

A.2   Multi-Level Modeling

Due to the large size and increasing complexity of the MEA EPS, modeling the complete EPS becomes a challenge in terms of computational time requirement. Specially, if complex models are required. Therefore, a good balance is required between the system (or subsystem) simulation time and the model accuracy for any model-based research. Aiming to define a flexible and versatile approach to simulate the MEA EPS, in this research work a four-level modeling approach has been considered [2, 9, 160]. Thus, depending on the accuracy required a different modeling level can be used. Additionally, if higher detailed analysis in specific research topics is required, different modeling-levels can be complemented or even mixed. The four-level approach to be used is depicted in Figure A.1 as a pyramid, being the top of the pyramid a top-level modeling approach and the bottom of the pyramid an ultra-high detail modeling approach. The different modeling layers are described in the following.

- **Architectural level:** This top-level modeling layer aims to ease and simplify the global EPS studies and simulation. Typically, the architectural level modeling is used for steady-state simulations of the EPS. In addition, depending on the tasks to be fulfilled, the architectural level modeling is also separated into two sublevels: the *logical sublevel* and the *requirements sublevel*.

  In the *logical sublevel*, the functional integrity of the aircraft EPS is analyzed. The models typically consist of Boolean states and/or control logic laws permitting the different studies such as the impact of a fault, component (dis)connection and the distribution bus reconfiguration.

In the *requirements sublevel*, on its behalf, typically pre-sizing models of the EPS components are carried out for a set of given specifications. Thus, it typically studies the steady-state operating conditions aiming to ease and provide a first component sizing approach of the generators, converters and cables, among others, in terms of power rating, weight and costs.

- **Functional level:** The functional level modeling is the one below the architectural level and addresses the low-frequency transient behavior. Thus, the EPS components are modeled to manage dynamic frequencies up to the MEA EPS grid frequency value, typically between 360 Hz and 800 Hz. Therefore, the main aim of this modeling approach focuses on achieving simulation-based studies of the EPS dynamics, stability, the reaction to the (dis)connection of loads, load shedding and low-frequency power quality. Typically, in this modeling level non-switching or average converter models are employed which permit to model the entire EPS with a lower time simulation effort while getting a complete generator-to-load dynamic analysis.

  It is worth to mention that the functional level modeling could be extended by including additional effects such as the voltage and current ripple and the dominating harmonics or other domains like thermal or a detailed control structure. Anyway, aiming to avoid long simulating times related to the switching events, the ripples, harmonic effects and even the switching frequencies are introduced by means of advanced baseband transformation techniques.

- **Behavioral level:** This modeling level copes with the EPS and component dynamics on the order of kilohertz. In this context, the behavioral level-based models aim to generate signals which represent the real hardware waveforms. Consequently, these models can be used to execute relatively high detailed tasks such as harmonic analysis, the design of filters or analyze the conducted Electromagnetic Compliance (EMC). Thus, the behavioral models consider the power electronic converters switching, either idealized or device-physics-based, which typically are required to study the repercussion of HF harmonics and conducted EMC. In line with the increased complexity of this modeling layer, the EPS size that can be addressed is considered as limited due to the high computational effort required. Therefore, only the EPS subsystems are typically modeled. In case that the complete EPS is aimed to be modeled, some of the subsystems are often simplified as current or voltage sources and lumped parameters as representative impedances so that a time-effective simulation is achieved. It is worth to mention, that the behavioral level is typically used as the most detailed level for the EPS overall modeling.

- **Component (Device-Physics) level:** The bottom of the pyramid, representative of the lowest modeling layer, is formed by the component or device-physics modeling layer. Thus, this modeling level targets to produce the most detailed characteristics of the EPS components and, hence, it is considered as the most complex and time-consuming modeling level. In fact, it may also include multiple highly detailed physical domains like power quality, thermal stressing or EMC behavior. Hence, small time steps are required so that a highly detailed component simulation can be performed. This high detail level of modeling is not typically employed for designs beyond a specific component or equipment

within the system and, consequently, it is barely used for the simulation of an EPS.
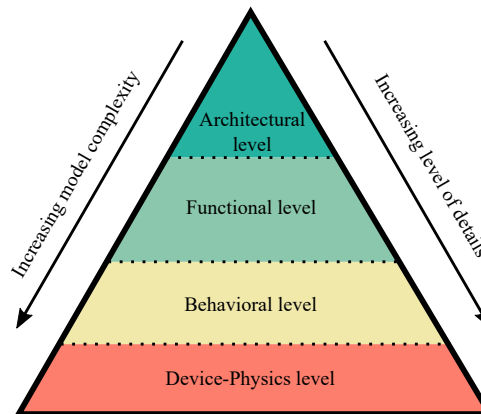

Figure A.1 Multi-level modeling.

Aiming to summarize the most important characteristics of each modeling layer, Table A.1 presents the typical models employed and some example studies in relation to each modeling layer. It is worth to mention that in this research work, not only the behavioral model has been employed for the comparison and filter design of the active rectifier topologies, but also the functional modeling for simulating the whole active modular rectifier architecture in Chapter 3.5 and the fault analysis and protection coordination simulation in Chapter 4.5. To this end, average-value models of the different subsystems have been employed aiming to obtain a relatively low computational effort.

Table A.1 Modeling levels and their fundamental features, and case study examples [2].

Model-level	Model Type	Example studies
Architectural	Boolean States Failure probability contants Control logic Steady-state solution Idealized control loops	▶ EPS architecture functional integrity ▶ Logic control law verification ▶ Preliminary EPS sizing (weight, cost, etc.) ▶ EPS events and reconfiguration modeling
Functional	State-average models Non-switching models Detailed control structure	▶ Fine EPS sizing ▶ Basic EPS dynamics: turn-on/off transients, fault development and clearance, EPS stability ▶ LF power quality ▶ Generator-to-load dynamic overview
Behavioral	Idealized switches No high-level contorl loops	▶ Harmonic analysis and EMC ▶ Active and passive filtering ▶ Fault protection studies
Device-Physics	Physics-based switches Device-scale parasitic effects Multi-physics coupling	▶ Detailed component design (including thermal behavior) ▶ Conducted and rediated EMC ▶ Verification and in-depth analysis

A.3   Average-Value Modeling of Power Converters

Typical simulation software like *Matlab-Simulink*, *PLECS* or *PSIM* include power electronic converter models. Accordingly, these simulation software do also include the full or idealized switching effects of the power converters in their models and, hence, are considered as representative of the behavioral layer. Consequently, a relatively high computational demand can be expected when a study at the overall-EPS-level is aimed [2, 9, 160].

In this regard, the Average-Value Modeling (AVM) of power converters arises as a potential functional-level modeling solution to considerably reduce the simulation time while achieving accurate representations of the power converters in terms of LF dynamics and the steady-state performance [2]. Concretely, the AVM removes the effects of the switching behavior and uses dynamic average values of different variables of represent the converters. Since the power converter switching frequency is considerably higher than the EPS dynamics, the converter-level study can be performed by means of dynamic average values which are defined for the length of a switching interval. As a result, the voltage and current ripples formed by the converter switching are neglected. The dynamic average value, $\bar{x}$, of a variable $x(t)$ referred to the time-domain is described as [2],

$$\bar{x} = \frac{1}{T_{\text{sw}} \int_{t-T_{\text{sw}}}^{t}} x(t) \cdot dt \tag{A.1}$$

where T_{sw} refers to the power converter switching period and $x(t)$ represents the voltage $v(t)$ or current $i(t)$.

A simplified schematic example of the power converter behavioral level and the AVM functional level is presented in Figure A.2 below. Note that the complete control loops are not presented but the difference between the gate signals for the behavioral model for the voltage generation and the simplified method for the AVM model.

(a) (b)
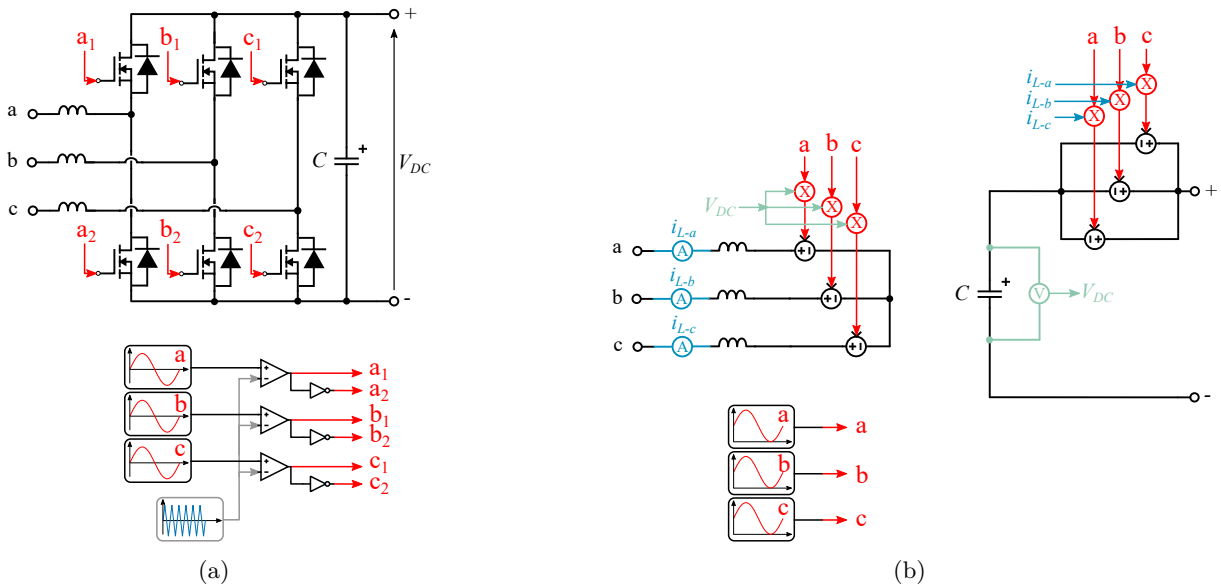
Figure A.2 Schematic models of (a) a switching converter and (b) a non-switching AVM converter.

APPENDIX B

Construction Drawings of the A380

B.1 Construction Drawings

This appendix pretends to summarize the construction drawings of the Airbus A380 MEA model used in this research work [161]. The drawings are presented in Figure B.1 below.
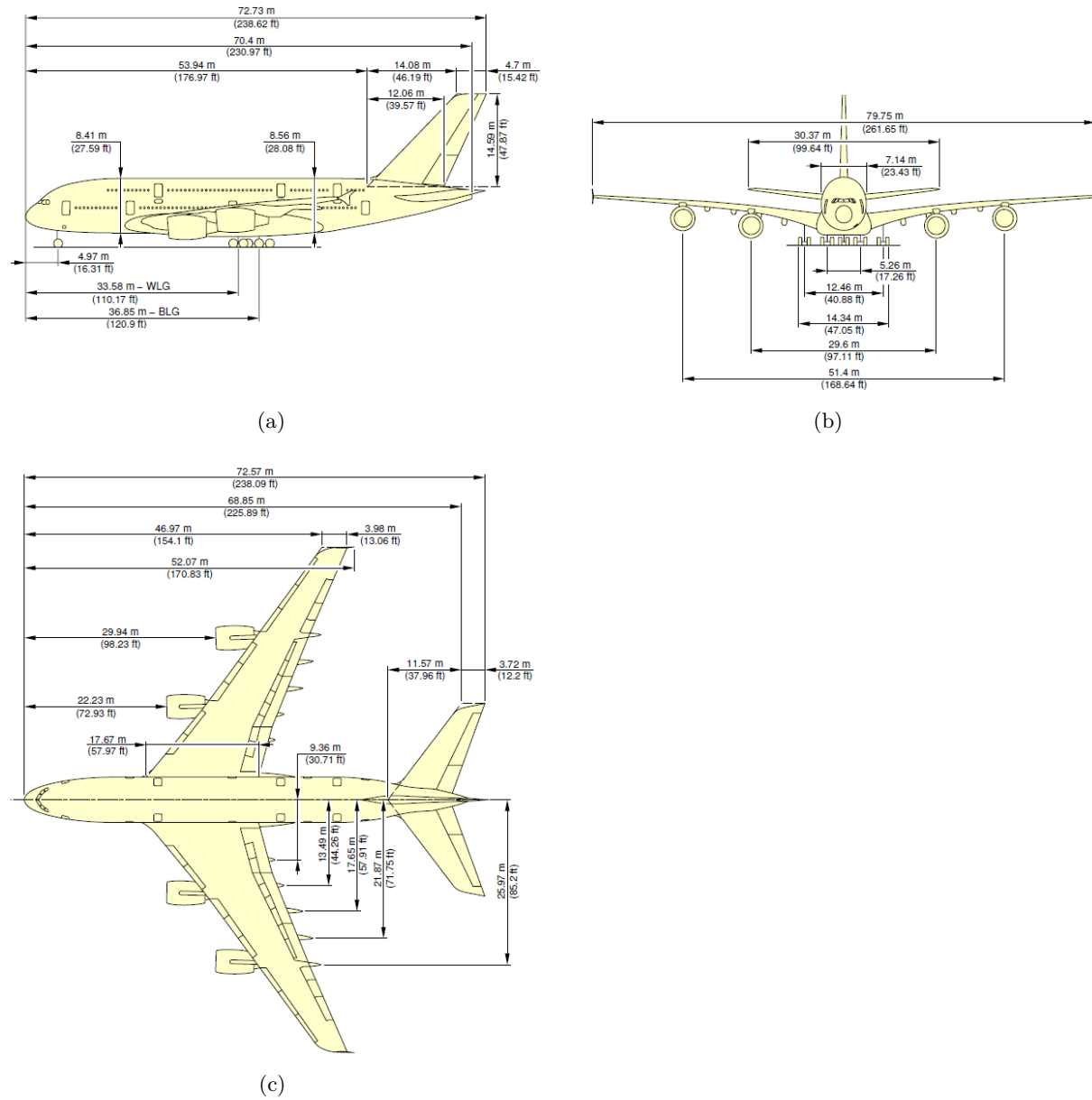

(a)

(b)

(c)

Figure B.1 Construction drawings of the Airbus A380 MEA model.

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