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# DC-link Voltage Balancing Strategy Based on SVM and Reactive Power Exchange for a 5L-MPC Back-to-Back Converter for Medium Voltage Drives

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**Abstract**—The reduced capability of multilevel converters with more than one intermediate node to balance the DC-link capacitors voltage, as well as the lack of standard modulation methods to improve their balancing performance, make these converter topologies unattractive for real power applications. This is especially true when the load demands active power. One of these topologies is the 5L-MPC (Five Level-Multi Point Clamped) converter. The Back-to-Back (B2B) configuration of two 5L-MPC converters and the use of a Space Vector Modulation (SVM) that exploits the voltage balancing capability of the redundant switching vectors extend the operation conditions range in which a proper voltage balance can be achieved. However, if practical modulation restrictions are considered (limitation of voltage steps, dead times, switching losses, etc.) the voltage balance cannot be achieved for all operation conditions. In this paper, a SVM which takes into account practical restrictions is proposed. In order to guarantee the voltage balance at any operation condition, the grid side rectifier exchanges reactive power with the grid side LCL filter. Thus, the voltage balance of the DC-link is guaranteed while a unity grid side power factor is achieved. The proposed modulation scheme and voltage balancing strategy is experimentally validated in a 6.6 kV-1.5 MW 5L-MPC B2B converter.

**Index Terms**—AC Drives, Back-to-Back (B2B), LCL Filter, Medium Voltage (MV), Multilevel converter, Multi Point Clamped (MPC), Neutral Point Clamped (NPC), Space Vector Modulation (SVM), Voltage Source Converter (VSC).

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## I. INTRODUCTION

POWER electronic converters play an important role in Medium Voltage (MV) drive applications [1-9]. The development of power semiconductors [1-2] along with the advent of new multilevel converter topologies and modulation techniques [3-9] have contributed to extend the voltage and current capability of Voltage Source Converters (VSC) on those applications.

Although several new converter topologies have been presented in the last three decades, the Three Level-Neutral Point Clamped converter (3L-NPC) [4] is still one of the most popular converter topologies for MV drive applications. This converter requires the series connection of semiconductors or a step-up transformer in order to operate at voltage levels above 4.16 kV. The use of topologies with more voltage levels improves the output voltage quality and makes possible the transformerless operation at Medium Voltage levels (up to 6.6 kV) using standard semiconductors [3-8].

In this way, the Five Level-Neutral Point Clamped (5L-NPC) converter [10-16], provides real benefits compared with the 3L-NPC converter. The series connection of three clamping diodes and the DC-link voltage balance are the main drawbacks of this topology. The number of required semiconductors and the number of series connected devices can be reduced if a Five Level-Multi Point Clamped (5L-MPC) converter is used instead [17], Fig. 1.

The DC-link of the Five Level-Multi Point Clamped (5L-MPC) converter comprises four series-connected capacitors. The five different output voltage levels ( $V_{Dc}/2$ ,  $V_{Dc}/4$ ,  $0$  V,  $-V_{Dc}/4$ ,  $-V_{Dc}/2$ ) are synthesized connecting the output terminal to the different nodes (P,  $\rho$ , O,  $\eta$ , N) of the DC-link. If a Diode Front End (DFE) is used with a 5L-MPC inverter, the voltage balance of the DC-link capacitors can only be guaranteed at certain operation conditions. Generally speaking, if the inverter operates with a unity power factor, the average node currents are non-zero, Fig. 2(a). This leads to a voltage unbalance of the DC-link capacitors if the modulation index is higher than 0.55 [10-12, 18]. On the contrary, the average node currents tend to be zero if the inverter operates with low power factors, Fig. 2(b). Thus the balanced operation

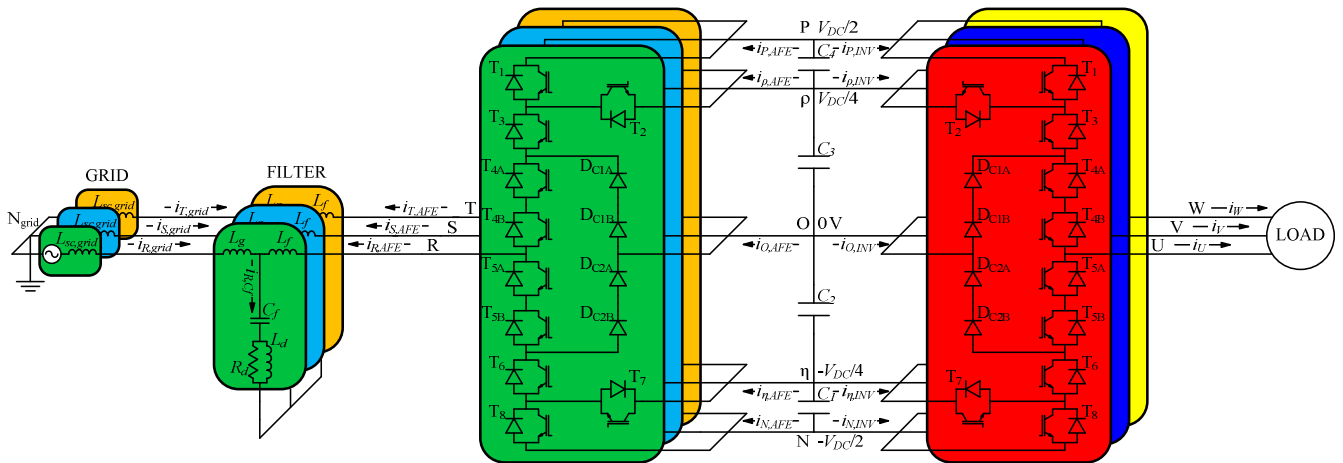


Fig. 1. 5L-MPC B2B Scheme with LCL filter (with RL damping circuit).

is possible for any modulation index if only reactive power is managed by the inverter.

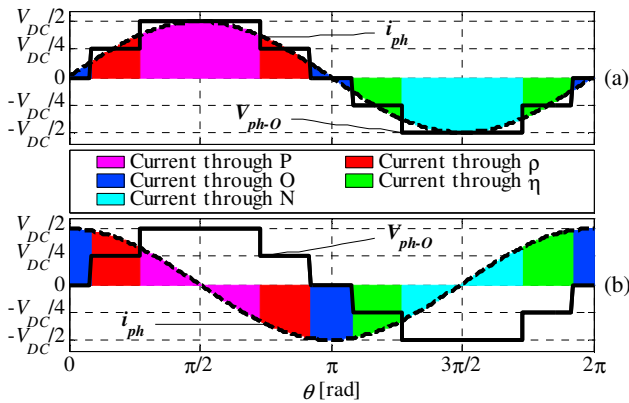


Fig. 2. Current flowing through DC-link nodes depending on the instantaneous phase voltage ( $V_{ph-o}$ ) and current ( $i_{ph}$ ). (a) Pure active power operation ( $\phi = 0^\circ$ ). (b) Pure reactive power operation ( $\phi = -90^\circ$ ).

The capacitors voltage unbalance problem has been widely analyzed for DFE-connected  $n$ -Level MPC inverters ( $n > 3$ ), [10-12, 18]. An ideal balanced operation area can be defined in terms of modulation index ( $m_a$  [0...1]) and load voltage-to-current phase shift ( $\phi$ ) for infinite level MPC converter connected to a DFE rectifier, Fig. 3.

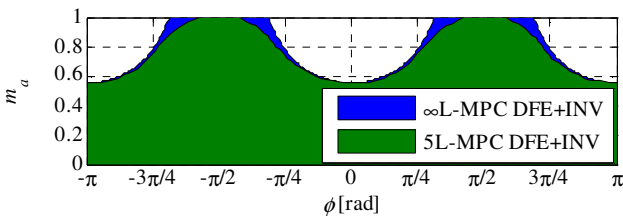


Fig. 3. Theoretical balanced operation area for  $\infty$ -L-MPC and 5L-MPC.

The Back-to-Back (B2B) operation of two 5L-MPC converters with a Space Vector Modulation (SVM) that exploits the balancing effect of the redundant switching vectors results in a notable improvement of the voltage balancing capability of the converter, [12-13]. However, if the active rectifier and the inverter operate with power factors and modulation indices

close to unity, the voltage balance of the DC-link capacitors cannot be guaranteed, [13].

Several voltage balancing methods have been proposed to extend the voltage balancing capability of the converter [10-16]. In [12], an SVM that coordinates the modulation of the Active Front End (AFE) and the inverter of a B2B is proposed. Nevertheless, the coordinated modulation implies a dramatic increase of the computational cost, highly unlikely to be assumable in real application. [14-15] present similar novel modulation schemes that guarantee the voltage balance at any operation condition. However, both methods allow multiple voltage steps per phase, which result in high voltage-derivatives at the output terminals and lead to the series operation of the power devices. In [16] additional power circuitry is used to achieve a proper voltage balance. Despite of the promising results, the use of additional components reduces the reliability and increases the cost and volume of the converter.

In consequence, it can be said that the lack of standard solutions for the DC-link voltage balancing problem makes difficult the use of this converter in real power applications.

This paper proposes a SVM modulation for the 5L-MPC converter which considers real restrictions such as computational cost, dead times, power losses, number of simultaneous voltage level steps per arm, minimum conduction times for semiconductors, etc. The voltage balancing capability of the proposed modulation scheme is analyzed, which guarantees a wide balanced operation range in B2B configuration, however, there are some operation conditions in which the voltage balance is not achieved. In order to guarantee the voltage balance at any operation condition, a voltage balancing strategy is proposed in which reactive power is exchanged between the AFE and the grid side LCL filter. Thus, the voltage balance of the DC-link is guaranteed while a unity grid side power factor is achieved.

The proposed voltage balancing strategy has been experimentally tested in a real scale prototype (6.6 kV-1.5 MW).

## II. PROPOSED SPACE VECTOR MODULATION

### A. Switching States of the 5L-MPC Converter

As shown in Fig. 1, the DC-link of the 5L-MPC converter consists in four series-connected capacitors charged to  $V_{DC}/4$ . Each phase of the 5L-MPC converter can connect its output terminals to any node of the DC-link (P, ρ, O, η, N) and in consequence, five different voltage levels per phase can be synthesized ( $V_{DC}/2$ ,  $V_{DC}/4$ , 0 V,  $-V_{DC}/4$ ,  $-V_{DC}/2$ ). Table I summarizes the different switching states and the synthesized output voltages.

TABLE I  
SWITCHING STATES OF 5L-MPC CONVERTER

$V_{ph-o}$	T <sub>1</sub>	T <sub>2</sub>	T <sub>3</sub>	T <sub>4</sub>	T <sub>5</sub>	T <sub>6</sub>	T <sub>7</sub>	T <sub>8</sub>
$V_{DC}/2$	1	0	1	1	0	0	1	0
$V_{DC}/4$	0	1	1	1	0	0	1	0
0 V	0	1	0	1	1	0	1	0
$-V_{DC}/4$	0	1	0	0	1	1	1	0
$-V_{DC}/2$	0	1	0	0	1	1	0	1

### B. Description of the Proposed SVM

The proposed modulation scheme respects the constraints imposed by the semiconductors (dead times, power losses, minimum conduction times) and by the converter (number of simultaneous voltage levels steps per arm, computational cost). In consequence, this modulation scheme can be applied in real power applications.

A 5L-MPC converter can synthesize  $5^3 = 125$  different voltage vectors, Fig. 4, which are geometrically distributed in 61 positions. The vectors located in a same position synthesize the same line-to-line voltage but have different effect on the node currents. Those vectors are redundant vectors and their proper selection allows the voltage balance of the DC-link capacitors in a wide operation range.

The reference output voltage vector can be represented by

$$\vec{V}_{REF} = \vec{V}_{a-O,REF} \vec{a}^0 + \vec{V}_{b-O,REF} \vec{a}^1 + \vec{V}_{c-O,REF} \vec{a}^2, \quad (1)$$

where  $\vec{a} = e^{j2\pi/3}$  and  $\{abc\} \equiv \{RST, UVW\}$ , [12, 19].

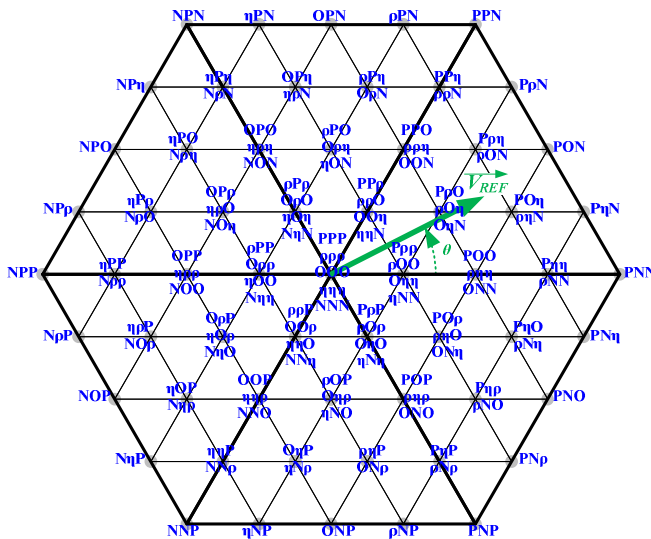


Fig. 4. Five level Space Vector (SV) map.

At a given time interval, the reference voltage vector is placed in a given region, i.e., each triangular area in which is divided the Space Vector (SV) map. This voltage is synthesized combining the nearest switching vectors during a modulation period ( $T_{mod}$ ), that is, vectors from the three vertices of that region [12, 19], by

$$\vec{V}_{REF} = \vec{v}_X \cdot d_X + \vec{v}_Y \cdot d_Y + \vec{v}_O \cdot d_O, \quad (2a)$$

$$d_X + d_Y + d_O = 1. \quad (2b)$$

The duty cycles ( $d_X, d_Y, d_O$ ) of the applied switching vectors ( $\vec{v}_X, \vec{v}_Y, \vec{v}_O$ ) depend on the projection of the reference voltage vector to each axe of the region, Fig. 5(a).

Each modulation period, a four vector sequence is applied to synthesize the reference voltage vector [12, 19],

$$\vec{V}_{REF} = \vec{v}_1 \cdot d_{v_1} + \vec{v}_2 \cdot d_{v_2} + \vec{v}_3 \cdot d_{v_3} + \vec{v}_4 \cdot d_{v_4}, \quad (3a)$$

$$d_{v_1} + d_{v_2} + d_{v_3} + d_{v_4} = 1, \quad (3b)$$

where the first ( $\vec{v}_1$ ) and the fourth ( $\vec{v}_4$ ) vectors are redundant vectors (located in the same vertex of the region) and the other two vectors ( $\vec{v}_2, \vec{v}_3$ ) are located in the other two vertices of the region, Fig. 5(b). The only considered vector sequences are the ones that change just one voltage level from an applied switching vector to its consecutive switching vector, Fig. 5(b), in order to reduce the commutations and therefore to minimize the switching losses. In addition, the IGBT should not be switched off before it is fully saturated, in order to avoid too high switch off speeds and in consequence too high overvoltages [20]. Hence, only sequences that apply their vectors for a minimum time interval are considered. Only the vector sequences in which the duty-cycles of the first ( $d_{v_1}$ ) and fourth ( $d_{v_4}$ ) vectors satisfy

$$d_{v_k} \Big|_{k=\{1,4\}} \geq d_{v_{1,4},min} = \frac{t_{DT} + t_{on,min}}{T_{mod}} \quad (4)$$

guarantee the minimum conduction ( $t_{on,min}$ ) and dead times ( $t_{DT}$ ) of the semiconductors.

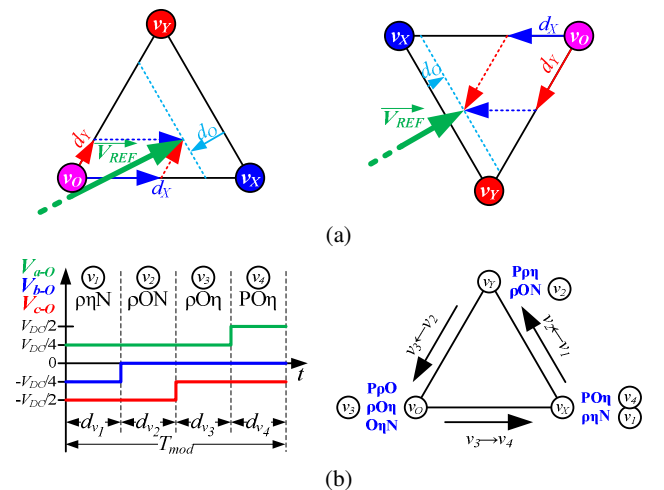


Fig. 5. Four vector sequence construction. (a) Nearest Three Vectors duty-cycle distribution. (b) Four vector sequence.

Furthermore, in order to limit the switching losses, the transitions between applied switching sequences are limited. Depending on the last applied vector sequence, the considered sequences are the ones that cause less switching and consequently less losses.

### C. DC-link Voltage Balancing Strategy

Once the applicable vector sequences have been identified, the applied vector sequence is the one that improves the most the voltage balance of the DC-link capacitors. Depending on the time distribution ( $\delta$ ) between the first and fourth redundant voltage vectors

$$\begin{cases} d_{v_1} = \frac{(1+\delta)}{2} \cdot (d_{v_1} + d_{v_4}) \\ d_{v_4} = \frac{(1-\delta)}{2} \cdot (d_{v_1} + d_{v_4}) \end{cases}, \quad (5)$$

the influence of a vector sequence on the average intermediate node current can be controlled,

$$i_{\gamma,ave}(\delta) = \sum i_{v_j} \cdot d_{v_j}. \quad (6)$$

Note:  $i_{v_j}$  refers to the effect of the  $j^{\text{th}}$  vector in the  $\gamma$  node current ( $\gamma \in \{\rho, O, \eta\}$ ) and  $d_{v_j}$  refers to the duty cycle of  $j^{\text{th}}$  vector of the vector sequence.

A nonzero average node current during a modulation period ( $T_{mod}$ ) contributes to change the voltage difference between its two adjacent capacitors, that is, the node voltage error,

$$\varepsilon_{\gamma} = V_{C_{\gamma}} - V_{C_{\gamma+1}}. \quad (7)$$

The voltage error of the  $\gamma$ -node depends on the currents through all the intermediate nodes and the DC-link capacitors,

$$\begin{bmatrix} \varepsilon_{\rho,end}(\delta) \\ \varepsilon_{O,end}(\delta) \\ \varepsilon_{\eta,end}(\delta) \end{bmatrix} = \begin{bmatrix} \varepsilon_{\rho,ini}(\delta) \\ \varepsilon_{O,ini}(\delta) \\ \varepsilon_{\eta,ini}(\delta) \end{bmatrix} + T_{mod} \cdot [MC] \cdot \begin{bmatrix} i_{\rho,ave}(\delta) \\ i_{O,ave}(\delta) \\ i_{\eta,ave}(\delta) \end{bmatrix}, \quad (8)$$

Note:  $\varepsilon_{\gamma,ini}$  and  $\varepsilon_{\gamma,end}$  refer to the voltage error of the  $\gamma$  node at the beginning and at the end of the modulation period respectively.

where

$$[MC] = \frac{1}{C_{1234}} \begin{bmatrix} C_4 & -C_{123} & C_{12} & -C_{12} & C_1 & -C_1 \\ C_3 & C_4 & C_3 & C_4 & C_3 & C_4 \\ C_4 & C_4 & -C_{34} & -C_{12} & C_1 & -C_1 \\ -C_2 & C_3 & C_2 & -C_3 & C_2 & -C_3 \\ -C_4 & C_4 & -C_{34} & C_{34} & -C_{234} & -C_1 \\ C_1 & C_2 & -C_1 & C_2 & -C_1 & C_2 \end{bmatrix}. \quad (9)$$

Note:  $C_{1234} = C_1 + C_2 + C_3 + C_4$ ;  $C_{123} = C_1 + C_2 + C_3$ ;  $C_{234} = C_2 + C_3 + C_4$ ;  $C_{12} = C_1 + C_2$ ;  $C_{34} = C_3 + C_4$

If the DC-link capacitors are equal ( $C_1 = C_2 = C_3 = C_4$ ), the voltage error of each node depends only on its node current.

The optimum time distribution ( $\delta_{opt}$ ) for the redundant vectors is calculated to minimize the total quadratic error of the three DC-link capacitor nodes from

$$\varepsilon_{total}(\delta) = [\varepsilon_{\rho,end}(\delta)]^2 + [\varepsilon_{O,end}(\delta)]^2 + [\varepsilon_{\eta,end}(\delta)]^2. \quad (10)$$

If the optimum time distribution ( $\delta_{opt}$ ) cannot guarantee minimum conduction times, a minimum duty cycle must be applied to achieve the proper operation of the semiconductors,

$$\delta_{real} = \begin{cases} -\delta_{lim} & \delta_{opt} \leq -\delta_{lim} \\ \delta_{opt} & -\delta_{lim} < \delta_{opt} < \delta_{lim} \\ \delta_{lim} & \delta_{opt} \geq \delta_{lim} \end{cases}, \quad (11a)$$

$$\delta_{lim} = 1 - \frac{2 \cdot d_{v_{j4},min}}{d_{v_1} + d_{v_4}} = 1 - \frac{2}{d_{v_1} + d_{v_4}} \cdot \frac{t_{DT} + t_{on,min}}{T_{mod}}. \quad (11b)$$

Once the time distribution ( $\delta_{real}$ ) is calculated for each applicable four vector sequence, the vector sequence that minimizes the total quadratic error ( $\varepsilon_{total}$ ) is applied.

This modulation strategy is applied independently in the inverter and the AFE of the 5L-MPC B2B converter. The coordinate optimum vector sequence selection [12] results in a poor benefit in terms of voltage balancing capability while it increases dramatically the computational cost.

### III. ANALYSIS OF THE VOLTAGE BALANCING CAPABILITY

The behavior of the 5L-MPC B2B converter (Fig. 1) with the proposed SVM has been analyzed in simulation. The AFE is connected to an ideal 6.6 kV grid by means of an inductive filter (the grid side LCL filter has not been considered in this first analysis). The inverter is connected to a controlled current source which models the behavior of the load.

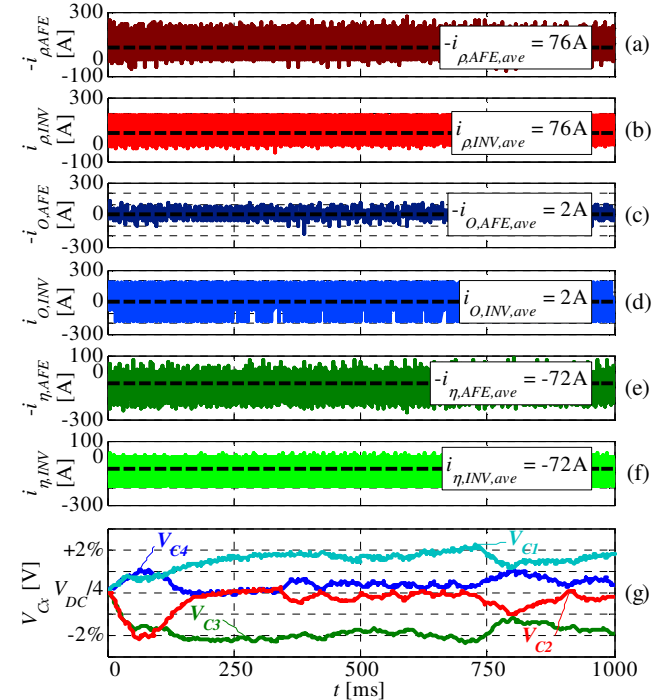


Fig. 6. Currents through DC-link intermediate nodes and DC-link capacitors voltage for  $m_{a1,AFE} = 0.85$ ,  $\cos\phi_{1,AFE} = 1$ ,  $m_{a1,INV} = 0.80$ ,  $\cos\phi_{1,INV} = 1$ ,  $i_{INV,rms,1} = 133$  A,  $V_{DC} = 11$  kV. (a)  $-i_{\rho,AFE}$ . (b)  $i_{\rho,INV}$ . (c)  $-i_{O,AFE}$ . (d)  $i_{O,INV}$ . (e)  $-i_{\eta,AFE}$ . (f)  $i_{\eta,INV}$ . (g) DC-link capacitors voltage:  $V_{C1}$ ,  $V_{C2}$ ,  $V_{C3}$ ,  $V_{C4}$ .

Fig. 6 shows the intermediate node currents synthesized by the AFE and the inverter operating with  $m_{a1,AFE} = 0.85$  and



$m_{a1,INV} = 0.80$  respectively at unity power factor in both converters. According to the Fig. 2(a), in these conditions, the standalone operation of the AFE or the inverter leads to voltage unbalance. The current synthesizable by the inverter in the  $\rho$  node is always positive (Fig. 6(b)), while the current synthesizable in the  $\eta$  node is always negative (Fig. 6(f)). However, in the B2B configuration, the proposed SVM equalizes the average node currents synthesized by the AFE and the inverter making possible to keep the voltage balance of the DC-link capacitors.

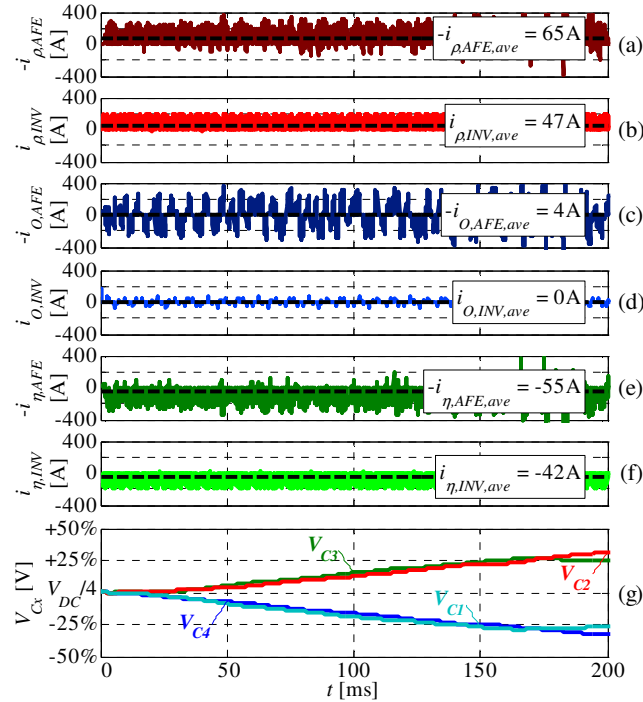


Fig. 7. Currents through DC-link intermediate nodes and DC-link capacitors voltage for  $m_{a2,AFE} = 0.75$ ,  $\cos\phi_{2,AFE} = 1$   $m_{a2,INV} = 0.95$ ,  $\cos\phi_{2,INV} = 1$ ,  $i_{INV,rms,1} = 133\text{A}$ ,  $V_{DC} = 11\text{kV}$ . (a)  $-i_{\rho,AFE}$ . (b)  $i_{\rho,INV}$ . (c)  $-i_{O,AFE}$ . (d)  $i_{O,INV}$ . (e)  $-i_{\eta,AFE}$ . (f)  $i_{\eta,INV}$ . (g) DC-link capacitors voltage:  $V_{C1}$ ,  $V_{C2}$ ,  $V_{C3}$ ,  $V_{C4}$ .

In contrast, as the difference between modulation indices of both converters becomes larger ( $m_{a2,AFE} = 0.75$ ,  $m_{a2,INV} = 0.95$ ) the synthesizable intermediate node currents by each converter become notoriously different. In this case, the average node currents synthesized by the inverter cannot be compensated by the average node currents synthesized by the AFE, Fig. 7. Thus, the DC-link voltage balance is not possible.

The voltage balancing capability of the proposed modulation has been analyzed in simulation in a wide range of operation conditions, Fig. 8. The green shaded area represents the balanced operation conditions and the red shaded area represents the unbalanced operation conditions. The results show that the voltage balance of the DC-link capacitors cannot be achieved if the inverter operates at high modulation indices and power factors. It can also be concluded that higher modulation indices for the AFE lead to wider unbalanced operation areas. This is especially true as the modulation indices of both converters differ more.

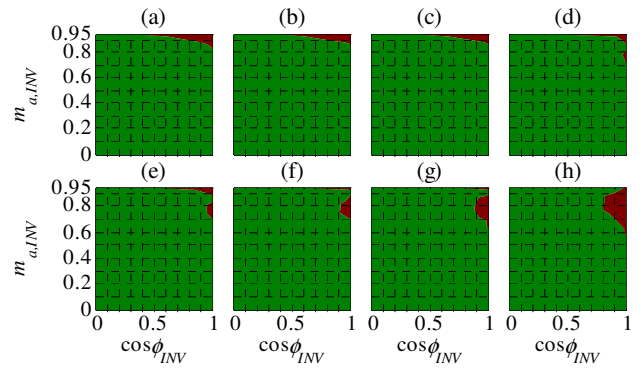


Fig. 8. Voltage balancing capability with the proposed SVM scheme for 5L-MPC B2B converter with  $\cos\phi_{AFE} = 1$ . (a)  $m_{a,AFE} = 0.76$ . (b)  $m_{a,AFE} = 0.80$ . (c)  $m_{a,AFE} = 0.82$ . (d)  $m_{a,AFE} = 0.84$ . (e)  $m_{a,AFE} = 0.86$ . (f)  $m_{a,AFE} = 0.88$ . (g)  $m_{a,AFE} = 0.90$ . (h)  $m_{a,AFE} = 0.935$ .

#### IV. REACTIVE POWER EXCHANGE-BASED VOLTAGE BALANCING CAPABILITY IMPROVEMENT

##### A. Effect of the Reactive Power Managed by the AFE on the Voltage Balance

As demonstrated in previous sections, the power factors of the AFE and the inverter have a big influence on the voltage balancing capability.

When the AFE and the inverter operate with different modulation indices and unity power factors, the voltage balance cannot be achieved, as demonstrated in Fig. 7 ( $m_{a2,AFE} = 0.75$ ,  $\cos\phi_{2,AFE} = 1$  and  $m_{a2,INV} = 0.95$ ,  $\cos\phi_{2,INV} = 1$ ).

In general, the modulation index and the power factor of the inverter are imposed by the load. So, these parameters cannot be freely controlled.

The modulation index and the power factor of the AFE depend on the grid voltage, the used filter and the desired grid side power factor. Generally, a unity grid side power factor is desired. During the design process of the filter, the amount of capacitive reactive power managed by the filter can be defined. In consequence, the AFE must manage inductive reactive power in order to guarantee a unity grid side power factor. Thus, the voltage balancing capability of the AFE is improved.

In order to demonstrate this idea, Fig. 9 shows the operation of the AFE and the inverter with different modulation indices ( $m_{a3,AFE(ini)} = m_{a2,AFE} = 0.75$  and  $m_{a3,INV} = m_{a2,INV} = 0.95$ ). While the inverter operates at unity power factor, the AFE converges to a non-unity power factor ( $\cos\phi_{3,AFE(end)} = 0.8$ ). As it can be observed, under this operation condition, the voltage balance can be achieved.

As shown by Fig. 9(g), the operation of the AFE with reactive power leads also to a reduction of the modulation index of the AFE (from  $m_{a,AFE(ini)} = 0.75$  to  $m_{a,AFE(end)} = 0.67$ ). According to Fig. 8, the reduction of the modulation index contributes to an improvement of the voltage balancing capability of the converter.

The colored areas shown in Fig. 10 depict the reactive power required by the AFE to achieve a proper voltage balance at different operation conditions.

It can be observed that as far as the modulation indices and the power factor of the inverter increase, the reactive power

required by the AFE becomes larger. This is especially true when the inverter operates at unity power factor.

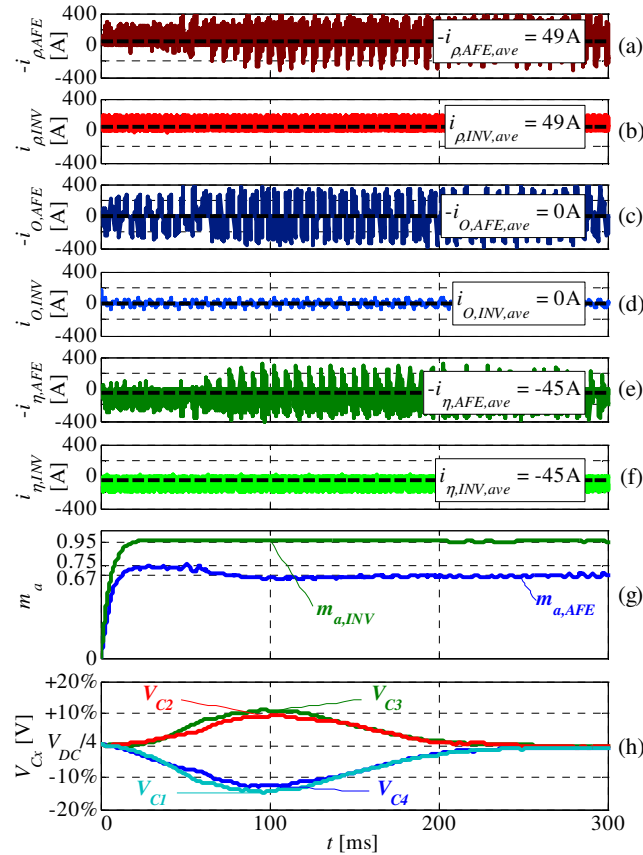


Fig. 9. Currents through DC-link intermediate nodes, modulation indices evolution and DC-link capacitors voltage for  $m_{a3,AFE} = 0.75$ ,  $\cos\phi_{3,AFE} = 0.8$ ,  $m_{a3,INV} = 0.95$ ,  $\cos\phi_{3,INV} = 1$ ,  $i_{INV,rms,1} = 133$  A,  $V_{DC} = 11$  kV. (a)  $-i_{\rho,AFE}$ . (b)  $i_{\rho,INV}$ . (c)  $-i_{O,AFE}$ . (d)  $i_{O,INV}$ . (e)  $-i_{\eta,AFE}$ . (f)  $i_{\eta,INV}$ . (g) Modulation indices:  $m_{a,AFE}$ ,  $m_{a,INV}$ . (h) DC-link capacitors voltage:  $V_{C1}$ ,  $V_{C2}$ ,  $V_{C3}$ ,  $V_{C4}$ .

As the required amount of reactive power has been estimated, the grid side LCL filter can be designed to provide the reactive power required by the AFE in the worst-case scenario. Thus, the grid side power factor can be kept close to the unity.

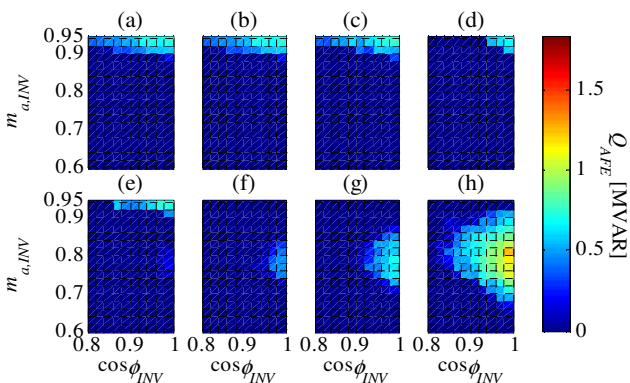


Fig. 10. Required minimum reactive power for guaranteeing voltage balance of the DC-link capacitors considering  $i_{INV,rms,1} = 133$  A and  $V_{DC} = 11$  kV. (a)  $m_{a,AFE} = 0.76$ . (b)  $m_{a,AFE} = 0.80$ . (c)  $m_{a,AFE} = 0.82$ . (d)  $m_{a,AFE} = 0.84$ . (e)  $m_{a,AFE} = 0.86$ . (f)  $m_{a,AFE} = 0.88$ . (g)  $m_{a,AFE} = 0.90$ . (h)  $m_{a,AFE} = 0.935$ .

Due to the current and thermal limits of the power semiconductors, the operation with high amount of reactive power may limit the active power transferred to the DC-link. In order to avoid these operation conditions, the permitted operation range of the inverter is delimited below  $m_{a,INV} \leq 0.88$  modulation index and  $\cos\phi_{INV} \leq 0.90$  power factor. Thus, the AFE can operate with the required amount of reactive power without reducing the power transfer capability.

### B. Description of the LCL Filter and IEEE519 Standard

In order to satisfy the current harmonic content limits defined by the IEEE519 standard [21], a LCL filter is connected to the grid side AFE converter, Fig. 1, since it provides a good attenuation at frequencies above its resonance frequency ( $f_{res}$ ). In addition, the filter includes a RL damping circuit, in which the damping resistor  $R_d$  attenuates the filter gain at resonance frequency whereas the damping inductance  $L_d$  reduces the power losses in the damping resistor, [22-24].

Moreover, as concluded in the previous chapter, in this work the filter is also designed to provide reactive power to the AFE in order to guarantee the proper DC-link voltage balance at a unity grid power factor.

As the AFE is controlled by means of the proposed SVM, its output voltage contains harmonics (whose first-carrier-band appears around semiconductors switching frequency,  $f_{sw}$ ) that accordingly generates current harmonics.

TABLE II  
CURRENT DISTORTION LIMITS FOR GENERAL DISTRIBUTION SYSTEMS (120 V THROUGH 69000 V), [21]

Maximum Harmonic Current Distortion In Percent of $I_L$						
Individual Harmonic Order (Odd Harmonics)						
$r_s = I_{sc}/I_L$	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	TDD
<b>&lt;20*</b>	4.0	2.0	1.5	0.6	0.3	5.0
<b>20&lt;50</b>	7.0	3.5	2.5	1.0	0.5	8.0
<b>50&lt;100</b>	10.0	4.5	4.0	1.5	0.7	12.0
<b>100&lt;1000</b>	12.0	5.5	5.0	2.0	1.0	15.0
<b>&gt;1000</b>	15.0	7.0	6.0	2.5	1.4	20.0

Even harmonics are limited to 25% of the odd harmonic limits above.

Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.

\*All power generation equipment is limited to these values of current distortion, regardless of actual  $I_{sc}/I_L$ .

where	
$I_{sc}$	= maximum short-circuit current at PCC
$I_L$	= maximum demand load current (fundamental frequency component) at PCC
TDD	= total root-sum-square harmonic current distortion, in percent of the maximum demand load current (15 or 30 min demand)
PCC	= Point of common coupling

The IEEE519 standard defines the maximum allowable grid current harmonic content and harmonic distortion for different grid types. Different grid types are defined by their short-circuit strength ( $r_s$ ), i.e., the ratio between the grid short-circuit power ( $S_{sc}$ ) and the rated power of the system that is being connected to it ( $S_L$ ),

$$r_s = \frac{S_{sc}}{S_L} \equiv \frac{I_{sc}}{I_L}. \quad (12)$$

Basically, the stronger the grid is (higher  $r_s$  ratio), the more difficult is to disturb it, and therefore, the more harmonic content is allowed in the common connection point (PCC), Table II.

As shown in Fig. 1, the grid model comprises an ideal voltage source and an equivalent grid inductance ( $L_{sc,grid}$ ). The smaller this inductance is, the stronger the grid is; therefore, it is more difficult to disturb it. The equivalent  $L_{sc,grid}$  inductance is connected in series with the grid side inductance  $L_g$  of the LCL filter. The addition of both inductances can be renamed as  $L_{G,eq}$ ,

$$L_{G,eq} = L_{sc,grid}(r_s) + L_g \quad (13)$$

### C. LCL Filter Design for Reactive Power Exchange

The converter side inductance ( $L_f = 15$  mH) is dimensioned to limit the ripple of the converter side current (typically set below 15-20% of the rated current [22-24]) by

$$\Delta i_{AFE,pp,max} \approx \frac{1}{24} \cdot \frac{V_{DC}}{L_f \cdot f_{sw}} \quad (14)$$

According to the literature, the capacitor of the LCL filter ( $C_f$ ) is typically designed to manage an amount of reactive power about 2-5% of the rated power of the converter, [24]. This design criterion is not enough to satisfy the reactive power requirement of the converter, Fig. 10. In consequence, the voltages of the DC-link capacitors cannot be balanced operating with a unity grid side power factor. For this reason, in this application the filter capacitor has been dimensioned to provide the reactive power ( $Q_{AFE}$ ) required by the AFE, Fig. 10. Thus, the filter capacitor can be calculated as

$$C_f \approx \max \left[ \frac{Q_{AFE}(m_{a,AFE}, m_{a,INV}, \cos \phi_{INV})}{(V_{grid,ll,rms,1})^2 \cdot 2\pi \cdot f_{o,grid}} \right] \quad (15)$$

If the filter capacitor provides a large amount of reactive power in order to guarantee the voltage balance at any operation condition, the capability of the AFE to transfer active power to the DC-link is reduced due to the thermal limitation of the semiconductors.

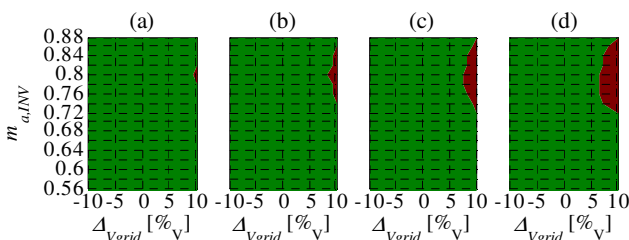


Fig. 11. Balanced DC-link operation area at unity grid power factor (green shaded) with the proposed LCL filter depending on the grid voltage deviation considering  $V_{grid,ll,rms,1,nom} = 6.6$  kV. (a)  $\cos \phi_{INV} = 0.84$ . (b)  $\cos \phi_{INV} = 0.86$ . (c)  $\cos \phi_{INV} = 0.88$ . (d)  $\cos \phi_{INV} = 0.90$ .

In consequence, the filter capacitor has been dimensioned to provide the maximum required reactive power up to  $m_{a,INV} \leq 0.88$  and  $\cos \phi_{INV} \leq 0.88$  and grid voltages ( $V_{grid,ll,rms,1} \leq 6930$  V) up to 5% over the rated grid voltage (6.6 kV). The chosen  $C_f = 25$   $\mu$ F capacitor provides a reactive

power about 23% of the rated power of the converter. Under these conditions, the voltage balance of the DC-link capacitors at unity grid power factor is guaranteed, as depicts the green shaded area in Fig. 11. At operation conditions beyond those limits, the AFE will require more reactive power and the grid side power factor will be less than unity.

The equivalent grid side inductance ( $L_{G,eq}$ ) altogether with the filter capacitor ( $C_f$ ) and the converter side inductance ( $L_f$ ) set the filter cut-off ( $f_{LC}$ ) and resonance ( $f_{res}$ ) frequencies,

$$f_{LC} = \frac{1}{2\pi} \cdot \frac{1}{\sqrt{L_{G,eq} \cdot C_f}} \quad (16a)$$

$$f_{res} = \frac{1}{2\pi} \cdot \sqrt{\frac{L_f + L_{G,eq}}{L_f \cdot L_{G,eq} \cdot C_f}} \quad (16b)$$

The cut-off frequency must be set in order to achieve the required current harmonic attenuation at the switching frequency ( $f_{sw} = 1$  kHz), Fig. 13. In addition, the resonance frequency must be set far below the switching frequency, in order to avoid undesired harmonic amplifications.

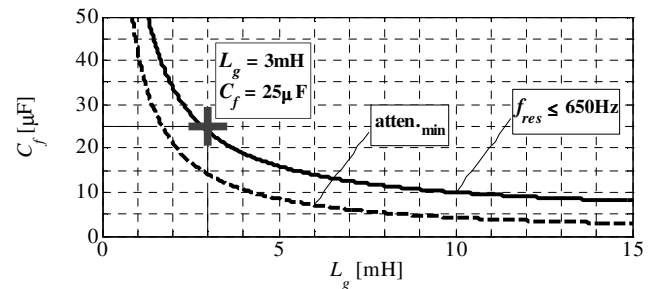


Fig. 12. Minimum  $L_g$ - $C_f$  pair curve for guaranteeing minimum attenuation (dashed) and maximum  $f_{res} \leq 650$  Hz (continuous) in the worst scenario.

The dashed line in Fig. 12 shows the  $L_g$ - $C_f$  pairs that provide the minimum required harmonic attenuation (-30 dB) at the switching frequency in the worst scenario ( $r_s > 1000$ ). However, choosing  $L_g$ - $C_f$  pairs from this curve could lead to set the resonance frequency close to the switching frequency depending on the grid short-circuit inductance ( $L_{sc,grid}$ ). The  $L_g$ - $C_f$  pairs represented by the continuous line in Fig. 12 provide a higher harmonic attenuation at the switching frequency while they guarantee a resonance frequency below  $f_{res} \leq 650$  Hz in the worst scenario ( $r_s > 1000$ ).

Therefore, as the filter capacitor ( $C_f$ ) has been previously set, a grid side inductance of  $L_g = 3$  mH must be chosen, Fig. 12.

Once the main components of the LCL filter have been designed, a damping resistor ( $R_d$ ) must be included to reduce the harmonic amplification around the resonance frequency. In addition, a parallel connected inductor ( $L_d$ ) is used to reduce the power losses generated by the line frequency current components. Different  $R_d$ - $L_d$  pairs have been evaluated by means of analytical estimation and simulation in order to set a damping circuit ( $R_d = 2$   $\Omega$ ,  $L_d = 2$  mH) which guarantees a proper damping behavior and the fulfilment of the IEEE519 standard. Fig. 13 shows the filter response for different grid types. As it can be observed, -40 dB attenuation is guaranteed around the switching frequency ( $f_{sw} = 1$  kHz) for any grid type.



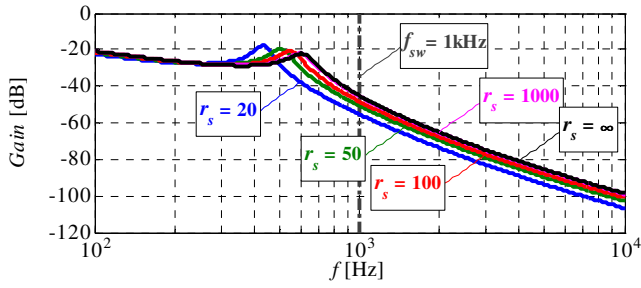


Fig. 13. Frequency response of  $I_{GRID}/V_{AFE}(f)$  transfer function for different grid types ( $r_s = S_{sc}/S_L$ ).

Analytical calculations and simulation results demonstrate that the dimensioned filter guarantees the proper attenuation at different grid types, Fig. 14. Only in the remote scenario in which the 5L-MPC B2B converter is connected to the weakest grid type ( $r_s < 20$ ), the IEEE519 standard fulfillment cannot be guaranteed, Fig. 14(a).

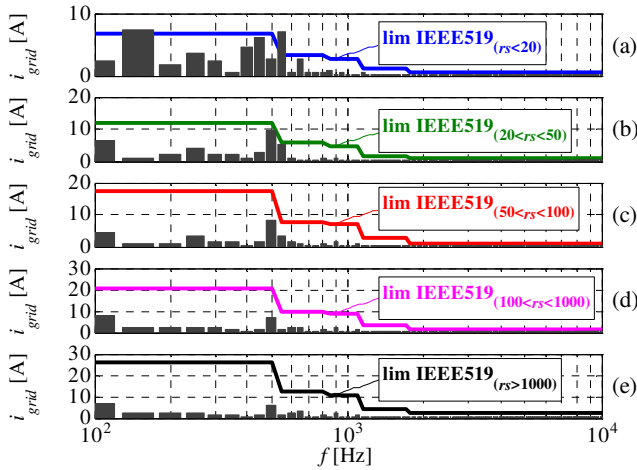


Fig. 14. Grid current harmonics distribution versus IEEE519 standard limits for different grid types ( $r_s = S_{sc}/S_L$ ). a)  $r_s < 20$ . b)  $20 < r_s < 50$ . c)  $50 < r_s < 100$ . d)  $100 < r_s < 1000$ . e)  $r_s > 1000$ .



Fig. 15. 5L-MPC B2B converter based 6.6 kV-1.5 MW prototype.

## V. EXPERIMENTAL RESULTS

The effect of the proposed SVM and designed filter on the DC-link voltage balance has been experimentally tested in a 6.6 kV-1.5 MW 5L-MPC B2B converter prototype, Fig. 1. The converter, Fig. 15, has been built by Ingeteam Power Technology S.A. (Zamudio, Spain).

Table III summarizes the parameters of the experimental setup. In order to obtain similar voltage ripples in the four DC-link capacitors, it has been observed that the required capacitance of the outer capacitors ( $C_1 = C_4 = 4$  mF) is higher than the capacitance of the inner capacitors ( $C_2 = C_3 = 2$  mF). The load used for these experimental tests is a 6 kV asynchronous machine ( $\cos\phi_{load,nom} = 0.864$ ).

TABLE III  
EXPERIMENTAL TEST BENCH PARAMETERS

	Parameter	Value
GRID	Grid rated voltage ( $V_{grid,ll,rms,I,nom}$ )	6.6 kV
	Grid frequency ( $f_{o,grid}$ )	50 Hz
FILTER	Filter grid side inductance ( $L_g$ )	3 mH
	Filter capacitor ( $C_f$ )	25 $\mu$ F
	Filter damping resistor ( $R_d$ )	2 $\Omega$
	Filter damping inductance ( $L_d$ )	2 mH
	Filter converter side inductance ( $L_f$ )	15 mH
B2B CONVERTER	DC-link rated voltage ( $V_{DC,nom}$ )	11.2 kV
	Inner DC-link capacitors capacitance ( $C_2, C_3$ )	2 mF
	Outer DC-link capacitors capacitance ( $C_1, C_4$ )	4 mF
	Semiconductors switching frequency ( $f_{sw}$ )	1 kHz
	IGBTs minimum conduction time ( $t_{on,min}$ )	8 $\mu$ s
	IGBTs dead time ( $t_{DT}$ )	5 $\mu$ s
	Rectifier rated current ( $I_{AFE,rms,I,nom}$ )	133 A
Inverter rated current ( $I_{INV,rms,I,nom}$ )	133 A	
LOAD	Load rated voltage ( $V_{load,ll,rms,I,nom}$ )	6 kV
	Load rated power factor ( $\cos\phi_{load,nom}$ )	0.864
	Output rated frequency ( $f_{o,INV}$ )	50 Hz

### D. Diode Front End Configuration

In the first experimental test, the voltage balancing capability of the inverter fed by a DFE is evaluated. For this purpose, the IGBTs of the AFE are forced to stay switched-off, so the AFE operates as a diode rectifier.

Several operation conditions have been evaluated experimentally (for  $\phi_{INV} = 0^\circ \dots 90^\circ$ ) and compared with simulation results and theoretical limits [10-12], as depicts Fig. 16. As it can be observed, the voltage balancing capability limits deduced from experimental measurements are slightly more restrictive than simulation and theoretical results.

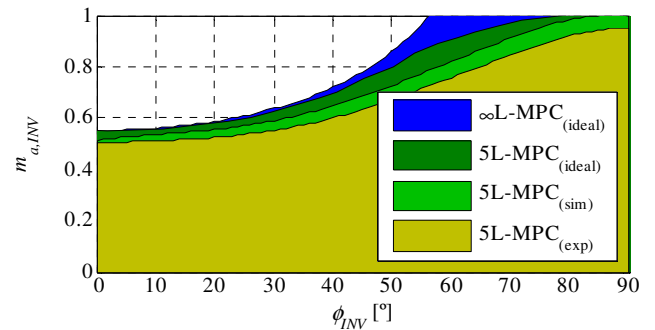


Fig. 16. Comparison of theoretical, simulation and experimental balanced operation areas of 5L-MPC in DFE-INV configuration.

Fig. 17 shows current and voltage measurements at  $m_{a,INV} = 0.86$  and  $\cos\phi_{INV} = 0.25$  ( $\phi_{INV} = 75.5^\circ$ ). Balanced DC-link operation permits the proper synthesis of the phase and line voltages and output current.

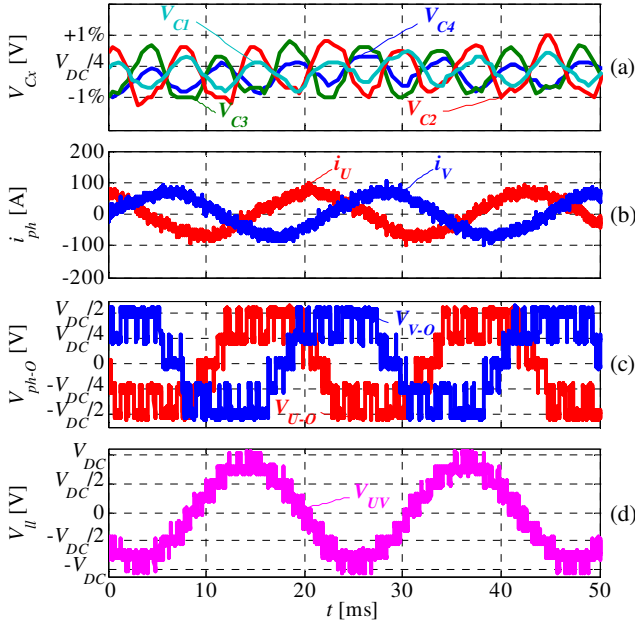


Fig. 17. Experimentally measured waveforms at  $m_{a,INV} = 0.86$ ,  $\cos\phi_{INV} = 0.25$ ,  $i_{INV,rms,1} = 47.6$  A,  $V_{DC} = 7.73$  kV in DFE-INV configuration. (a) DC-link capacitors voltage:  $V_{C1}$ ,  $V_{C2}$ ,  $V_{C3}$ ,  $V_{C4}$ . (b) Inverter phase currents:  $i_u$ ,  $i_v$ . (c) Inverter phase voltages:  $V_{U-O}$ ,  $V_{V-O}$ . (d) Inverter line-to-line voltage:  $V_{UV}$ .

### E. Back-to-Back Configuration with Pure Inductive Filter

In a second test, the B2B operation of the AFE and the inverter has been evaluated. In this test, a pure inductive grid side filter ( $L_g + L_f$ ) has been configured. Therefore, neglecting the voltage drop in the filter, similar power factor in the grid and the AFE can be considered. In order to evaluate the voltage balancing capability limits of the SVM, both the AFE and the inverter operate at high modulation indices. In addition, the power factor of the AFE is kept close to unity.

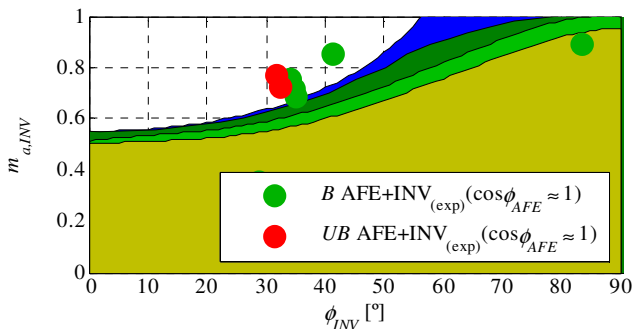


Fig. 18. Comparison of balanced operation areas of 5L-MPC in DFE-INV configuration and experimentally analyzed balanced (B)/unbalanced (UB) operation points in AFE-INV configuration.

Fig. 18 compares the operation limits of the DFE-INV configuration and the AFE-INV configuration. Green dots represent the balanced operation points, whereas the red dots represent the unbalanced operation points. Results demonstrate

that the B2B configuration extends the voltage balancing capability of the DFE-INV configuration. However, if a unity grid power factor is kept and the inverter operates at high modulation indices and power factors the DC-link voltage balance cannot be guaranteed (red dots in Fig. 18).

### F. Back-to-Back Configuration with the LCL Filter

Finally, in order to evaluate the effect of the reactive power managed by the AFE on the DC-link voltage balance, the LCL filter has been connected.

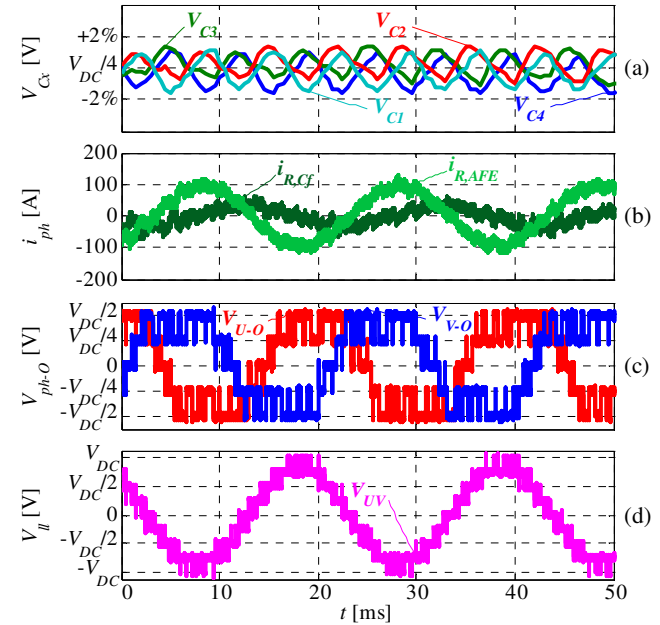


Fig. 19. Experimentally measured waveforms at  $m_{a,AFE} = 0.91$ ,  $\cos\phi_{AFE} = 0.97$ ,  $m_{a,INV} = 0.875$ ,  $\cos\phi_{INV} = 0.79$ ,  $i_{INV,rms,1} = 90.5$  A,  $V_{DC} = 8.75$  kV,  $V_{grid,ll,rms,1} = 5.84$  kV in LCL-AFE-INV configuration. (a) DC-link capacitors voltage:  $V_{C1}$ ,  $V_{C2}$ ,  $V_{C3}$ ,  $V_{C4}$ . (b) Grid side phase currents:  $i_{R,AFE}$ ,  $i_{R,CF}$ . (c) Inverter phase voltages:  $V_{U-O}$ ,  $V_{V-O}$ . (d) Inverter line-to-line voltage:  $V_{UV}$ .

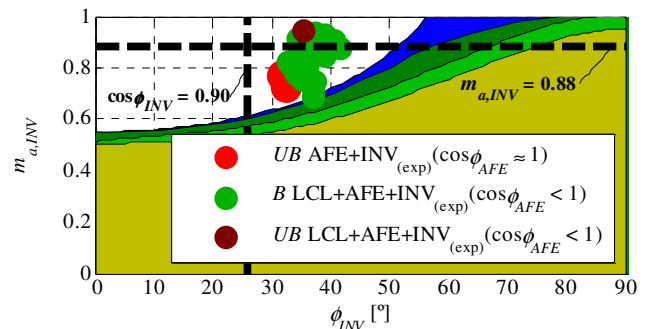


Fig. 20. Comparison of balanced (B)/unbalanced (UB) operation points in AFE-INV configuration and operation points in LCL-AFE-INV configuration.

This third test has been carried out around the same operation conditions of the second test in which the AFE-INV configuration without LCL filter cannot guarantee the DC-link voltage balance (red dots in Fig. 18, also depicted in Fig. 20). Experimental results show clearly that reactive power provided by the filter makes possible to balance the DC-link voltage with a unity grid power factor. Fig. 19 shows current and voltage

measurements at high modulation indices in the AFE and the inverter.

The converter has been tested under many other operation conditions, Fig. 20. Results demonstrate that this configuration makes possible the proper voltage balance of the DC-link capacitors in the defined operation area ( $m_{a,INV} < 0.88$ ). If the grid side power factor remains at unity, some unbalanced operation points appear beyond the defined operation limits ( $m_{a,INV} > 0.88$ ).

When the reactive power provided by the LCL filter is not enough to achieve a proper voltage balance, the AFE increases the consumed reactive power from the grid, reducing its power factor ( $\cos\phi_{AFE}$ ) and modulation index ( $m_{a,AFE}$ ), as depicts Fig. 21. In consequence, if the converter operates beyond the defined limits, the unity grid side power factor is not guaranteed.

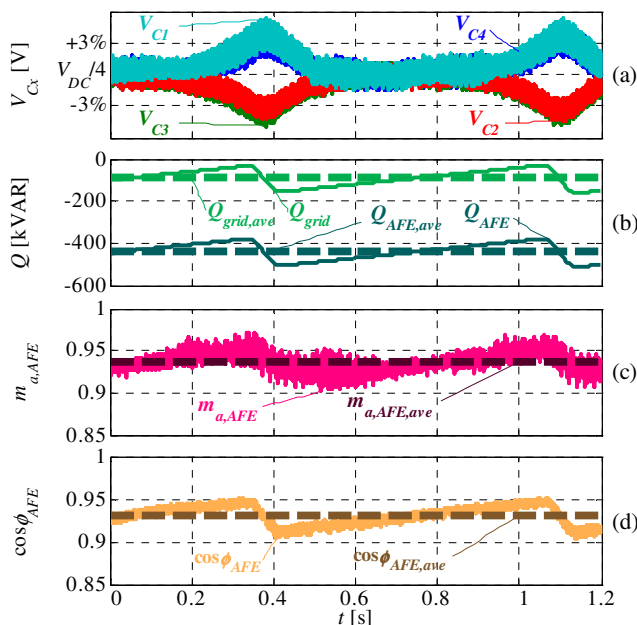


Fig. 21. Experimentally measured waveforms at  $m_{a,AFE,ave} = 0.937$ ,  $\cos\phi_{AFE,ave} = 0.931$ ,  $m_{a,INV} = 0.88$ ,  $\cos\phi_{INV} = 0.85$ ,  $i_{INV,rms,1} = 126.9$  A,  $V_{DC} = 9.5$  kV,  $V_{grid,ll,rms,1} = 6.6$  kV in LCL-AFE-INV configuration. (a) DC-link capacitors voltage:  $V_{C1}$ ,  $V_{C2}$ ,  $V_{C3}$ ,  $V_{C4}$ . (b) Reactive power:  $Q_{grid}$ ,  $Q_{AFE}$ . (c) Modulation index:  $m_{a,AFE}$ . (d) Power factor:  $\cos\phi_{AFE}$ .

Generally speaking, experimental results demonstrate that there is a close correlation between the operation conditions estimated in simulation and the experimentally measured conditions.

## VI. CONCLUSION

This paper describes and proposes a solution to the DC-link voltage balance problem of the 5L-MPC B2B converter. Basically, the AFE and the inverter are modulated by a SVM that considers practical restrictions, such as computational cost, dead times, power losses, etc. It can be observed that the operation at unity power factor of both converters leads to several unbalanced operation conditions. Thus, the power factor of the grid side AFE converter is reduced in order to improve the voltage balance capability of the B2B converter.

In order to keep a unity grid side power factor, LCL filter is designed to compensate the reactive power demanded by the AFE up to certain operation conditions (below  $m_{a,INV} \leq 0.88$ ,  $\cos\phi_{INV} \leq 0.90$  and  $V_{grid,ll,rms,1} \leq 6930$  V).

The operation under these operation limits guarantees the voltage balance of the DC-link capacitors with a unity grid power factor. Beyond these limits, the AFE increases the required reactive power to guarantee the DC-link voltage balance, however, the grid power factor is reduced.

Experimental results obtained in a 6.6 kV-1.5 MW converter prototype demonstrate the suitability of this solution for real power applications.

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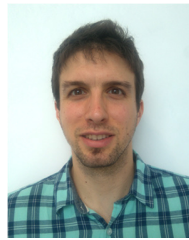
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