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Ph. D Thesis

Modular Multilevel Converter based HVDC Transmission System for Offshore Wind Farms

ESTÍBALIZ SOLAS MARTÍNEZ

Thesis supervisors:

GONZALO ABAD BIAIN

JON ANDONI BARRENA BRUÑA

MONDRAGÓN

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Abstract

This doctoral thesis falls within the scope of electronic power converters oriented to high voltage transmission applications, in particular the power generated in remote offshore wind farms by means of HVDC subsea cables.

This research is focused on the Modular Multilevel Converter (MMC) with two level submodules but also with multilevel topology submodules such as 3L-FC (three level flying capacitors) and 3L-NPC (three level neutral point capacitors). The main contribution of this thesis is the developed PWM based modulation strategy which allows the balancing of the total amount of submodules capacitors. It is applicable to the aforementioned submodule topologies under different working conditions as evidenced by experimental results.

Contents

List of abreviations

AC	Alternative Current
APO	Alternative Phase Opposition
CTL	Cascaded Two Level
DC	Direct Current
HVDC	High Voltage Direct Current
FC	Flying Capacitor
FRT	Fault Ride Through
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
LCC	Line Commutated Converters
LSPWM	Level Shifted Pulse Width Modulation
LV	Low Voltage
LVRT	Low Voltage Ride Through
MMC	Modular Multilevel Converter
MPC	Multi Point Clamped
MV	Medium Voltage
HVAC	High Voltage AC Transmission
MTDC	Multi-terminal DC
MVAC	Medium Voltage AC Transmission
NPC	Neutral Point Clamped
NPP	Neutral Point Piloted
PC	Collector Point
PCC	Point of Common Coupling
PEBB	Power Electronics Building Block
PF	Power Factor
PH	Phase
PO	Phase Opposition
PSPWM	Phase Shifted Pulse Width Modulation
PWM	Pulse Width Modulation
SF^6	Sulfurhexaflouride
SHE	Selective Harmonic Elimination
STATCOM	Static Synchronous Compensator
SVM	Space Vector Modulation
THD	Total harmonic Distortion
VSC	Voltage Source Converter
WPP	Wind Power Plant
XLPE	Cross Linked Polyethylene
ZnO	Zinc Oxide

Chapter 1

Introduction

In recent years, the continuously increasing demand for electric power is becoming our society more involved in saving energy. Climate change concerns together with high oil prices and increasing government support, have drived the use of renewable energy with the aim of dramatically reducing the emissions of greenhouse gases that harm the environment.

The naturally replenished wind energy resource has undergone a spectacular growth over the last years. Due to this fast increase, the most suitable sites to build an onshore wind farm are already in use, so offshore wind power is destined to have an important role. The evolution of the wind farms from onshore to offshore has led to some technological challenges, such as the energy transmission system or energy integration in the main grid. The economic access to remote renewable energy sources requires an electric energy transmission system that bridges very long distances with low losses. This is why the interest in High Voltage Direct Current (HVDC) technology has been revived.

The main advantage the HVDC offers versus High Voltage Alternative Current (HVAC) for bulky and long-distance electrical underwater power transmission is that HVDC avoids the heavy currents required by the cable capacitance improving the capacity of transmitting active power. For shorter distances, the higher cost of DC conversion equipment compared to an AC system may still be warranted, due to other benefits of direct current links.

1.1 Wind energy generation overview

1.1.1 Wind power installations

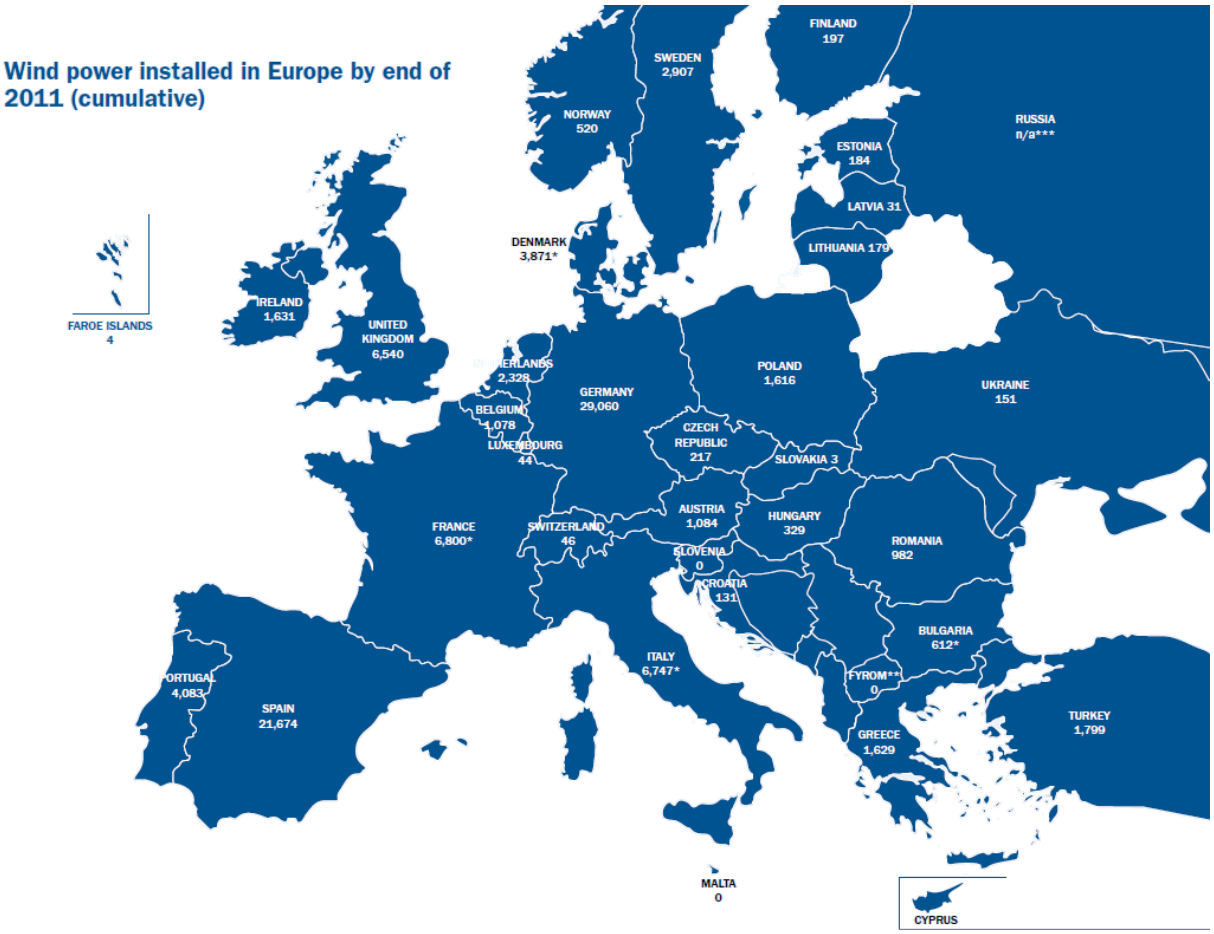


Fig. 1-1. Cumulative wind power installed in Europe by the end of 2011. Source: EWEA [1].

As described in [1], since 1995 wind energy has played an increasing and accelerating role in the evolution of the power sector. Despite the fact that most of the 94 GW of wind energy installed in the EU by the end of 2011 were added in the last 10 years, annual wind power installations in the EU have increased steadily over the past 17 years from 814 MW in 1996 to 9616 MW in 2011, an average annual growth rate of 15.6% (the progression is exposed in Fig. 1-2a). From those 9616 MW installed throughout 2011, 866 MW are offshore wind's share which represents a 9% of total installations, a little less than in 2010 (9.2%) as shown in Fig. 1-2b. Germany remains the EU country with the largest installed capacity (29 GW), followed by Spain (21.7 GW), Italy (6.7 GW), France (6.8 GW) and the UK (6.5 GW). Nine other countries have over 1 GW of installed capacity: Portugal, Denmark, the Netherlands, Sweden, Ireland, Greece, Poland, Austria and Belgium.

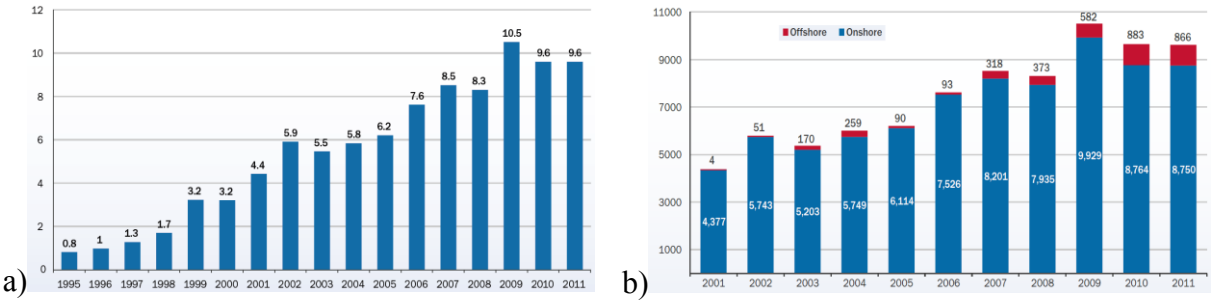


Fig. 1-2. a) Annual wind power installations in EU in GW. b) Annual onshore and offshore installations in MW. Source: EWEA [1].

This significant deployment of wind energy has been instrumental in reducing greenhouse gas emissions from the power sector, with more wind power capacity being installed in the EU than any other power generating technology in the last 10 years, except for gas. The 21st century sees the EU power sector moving away from fuel oil, coal and nuclear while continuing to increase its total installed capacity with gas, wind and solar PV to meet increasing demand.

1.1.2 Offshore wind power generation

Based on information available at [2], the average size of offshore turbines grid connected during 2011 was 3.6 MW. Since 2000, when the first 2 MW turbines were introduced, the average size of offshore turbines has been increasing, albeit not linearly, and in the middle of the last decade turbines in the 3+ MW range were being deployed. The first 5 MW turbines were used in 2007 at Beatrice in the UK and 2008 at Hooksiel in Germany. This size turbine became more common and, by 2011 the average size of offshore turbines was 3.6 MW, 20% more than in 2010 (3 MW) and over 6 times more than the turbines used in the early nineties (Fig. 1-3a). Moreover, in 2011 REpower installed the first turbines with a rated capacity above 5 MW at Ormonde in the UK. Looking at the under construction offshore wind farm pipeline (4,583 MW), the Siemens 3.6 MW turbine will continue to be used extensively. However, roll-out of 5 – 6 MW turbines means that the under construction pipeline averages 3.9 MW.

Owing to the incessant development of wind turbines, the average size of offshore wind farms has been increasing steadily (Fig. 1-3b). A total of 1371 offshore turbines are now installed and grid connected in European waters totalling 3812.6 MW spread across 53 wind farms in 10 countries. In 2011, the average size of the projects, once fully completed, is just under 200 MW, 45 MW (+29%) more than in 2010 when Thanet, a 300 MW project in the UK, was the largest offshore wind farm completed and fully grid connected in the world.

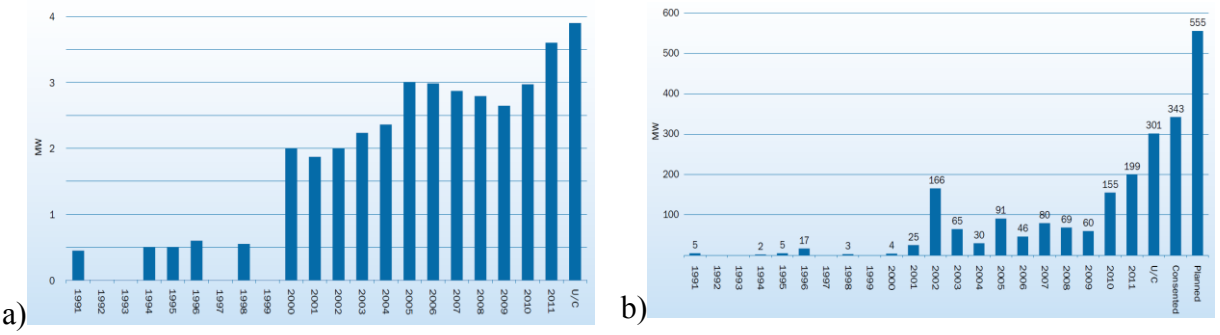


Fig. 1-3. a) Average annual size of offshore wind turbines in MW. b) Average wind farm size in MW. Source: EWEA [2].

This trend is expected to continue and, indeed, accelerate as the average size of offshore wind farms currently under construction is almost 300 MW, thanks to the construction that has already started on the first phase of the London Array project which will be 630 MW (the progression of the last years appears in Fig. 1-4a). As the technology matures and it is expected that wind farms will continue to grow in size, the average size of projects being planned by developers increases to 555 MW.

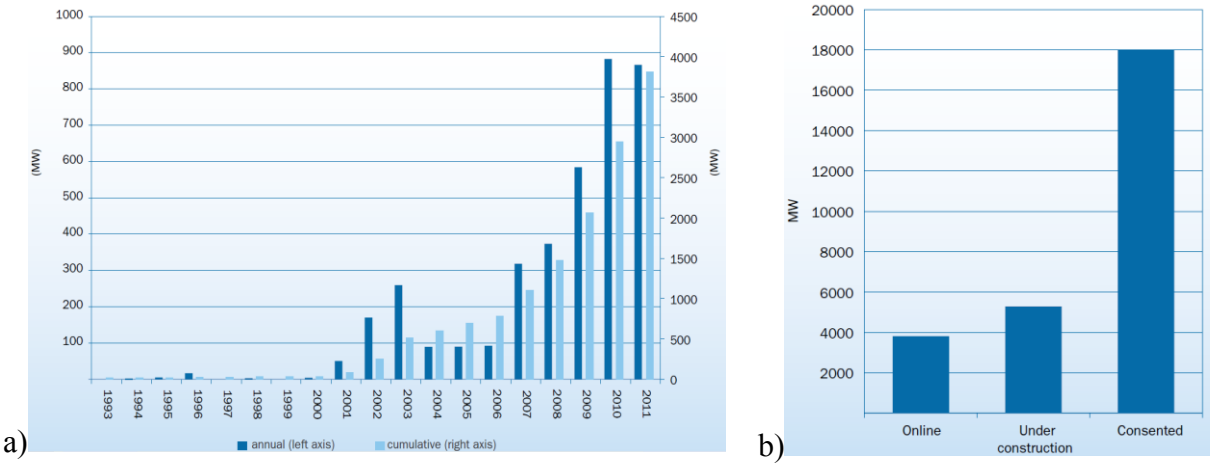


Fig. 1-4. a) Cumulative and annual offshore wind installations in MW. b) Offshore wind farms online, under construction and consented in MW. Source: EWEA [2].

The 9 offshore projects under construction in 2011, will bring online a further 2375 MW of capacity. These projects alone will bring total installed capacity in Europe to 6188 MW, a 62% increase. Furthermore, preparatory work on nine other projects started in 2011. These projects have a cumulative capacity of 2910 MW, 2272 in Germany and 638 in the UK. Therefore, when these 18 projects are completed, total installed offshore wind capacity in Europe would reach 9 GW. Furthermore, EWEA has identified 18 GW of fully consented projects in 12 European countries (information represented in Fig. 1-4b).

The UK is by far the largest market with 2094 MW installed, representing over half of all installed offshore wind capacity in Europe. Denmark follows with 857 MW (23%), then the Netherlands (247 MW, 6%), Germany (200 MW, 5%), Belgium (195, 5%), Sweden (164, 4%), Finland (26 MW in near-shore projects) and Ireland 25 MW. Norway and Portugal both have a full-scale floating turbine (2.3 MW and 2 MW respectively).

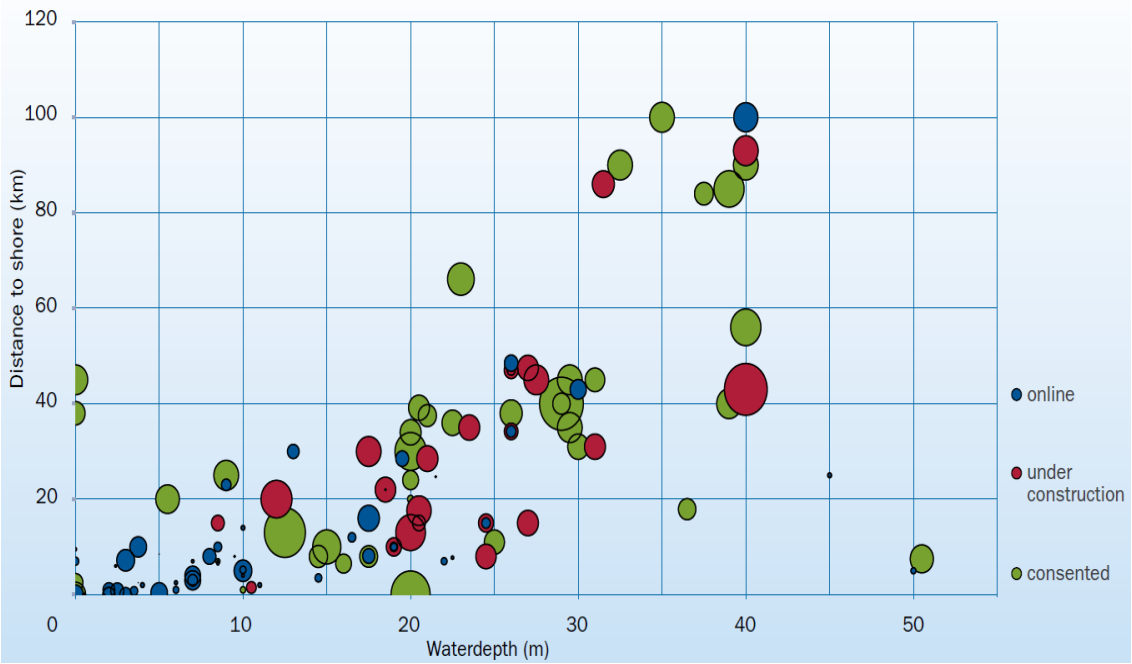


Fig. 1-5. Average size, distance to shore and water depth. Source: EWEA [2].

As far as the location of offshore wind farms is concerned, they are increasingly being built further from the coast and in deeper waters. Analysis of the planned projects pipeline shows that this trend will continue. In 2011 average water depth of wind farms was 22.8 m and average distance to shore 23.4 km. In Fig. 1-5 can be observed that there is already online a wind farm 100 km far away from the coast where the water depth is 40 meters, and similar distances as well as depth are chosen for future constructions. This is why for projects under construction, average depth is 25.3 m and distance to shore 33.2 km.

1.1.3 General wind farm layout

An evaluation of various large-scale wind farms layout are investigated in [3] but mainly three of them can be found all over the world as represented in Fig. 1-6: onshore, offshore with AC transmission and offshore with HVDC transmission to shore.

Onshore turbine installations are placed in hilly or mountainous regions. The exact position of the turbines is carefully chosen: these tend to be on ridgelines generally at least three kilometres inland from the nearest shoreline to exploit the topographic acceleration as the

wind accelerates over a ridge. The additional wind speeds gained in this way can increase energy produced because more wind goes through the turbines. Many of the largest operational onshore wind farms are located in the USA but as listed in Table 1-1 they are installed all over the world

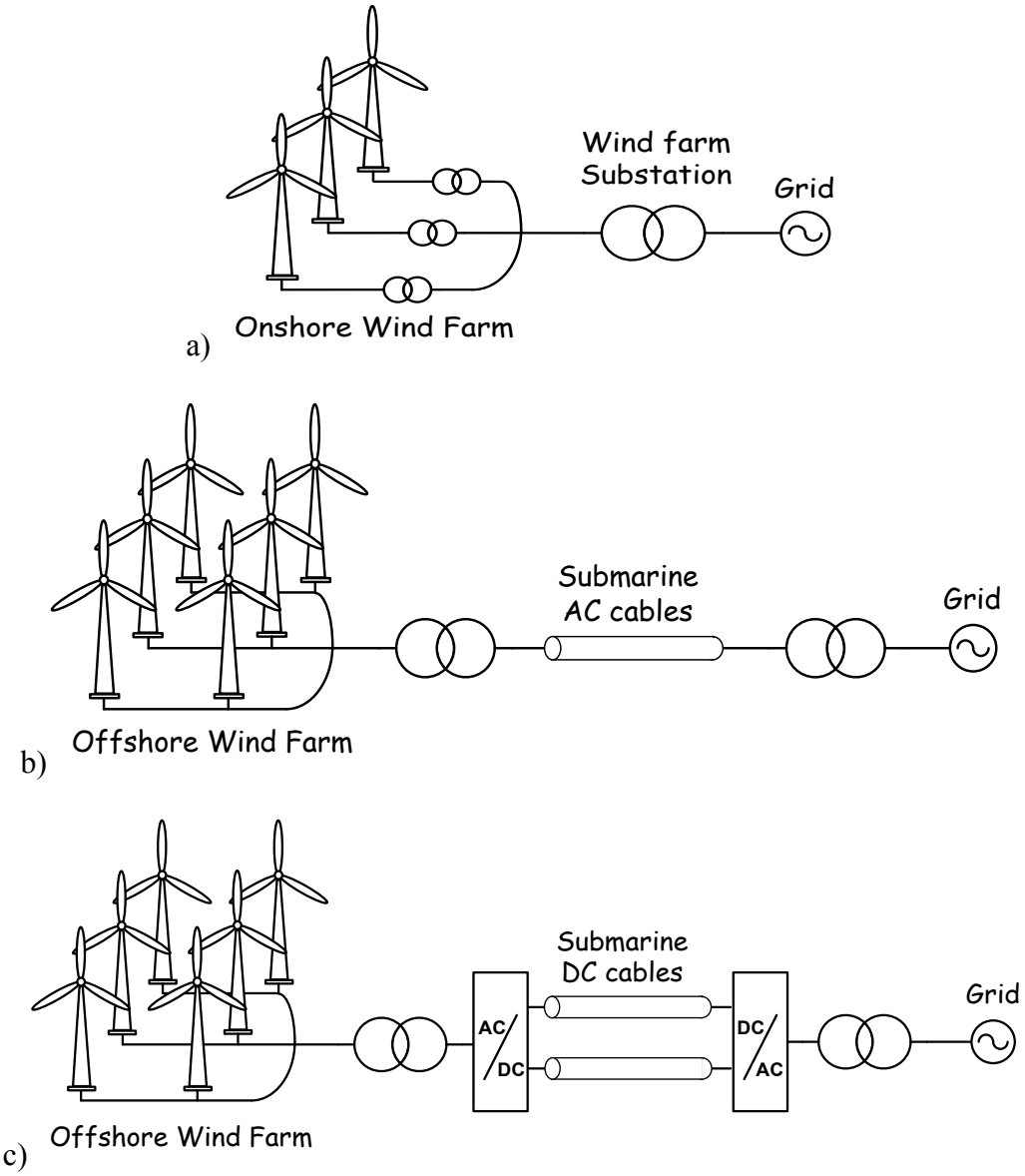


Fig. 1-6. General layouts of wind farms: a) Onshore. b) Offshore with AC transmission. c) Offshore with HVDC transmission.

The electricity generated in the wind turbines is typically low voltage. As the inter-turbine grid is usually medium voltage, a transformer is required at the output of each turbine to step up its voltage level. All the energy collected on the wind farm is again transformed at the substation to high voltage for the bulk transfer of the electrical energy, from the collecting point to electrical substations located near demand centres. The main function of the transformer is, besides voltage level conditioning, galvanic insulation of the two connected circuits.

Wind farm	Current Capacity	Country	No. of turbines	Production date
Roscoe	781.5 MW	USA	627	2009
Horse Hollow	735.5 MW	USA	421	2006
Dabancheng	500 MW	China	300	2009
Fântânele-Cogealac	387.5 MW	Romania	240	2011
Whitelee	322 MW	Scotland	140	2009
Lake Bonney	279 MW	Australia	99	2008

Table 1-1. Some operational onshore wind farms.

Unlike onshore wind farms, offshore ones refer to the construction of extensive wind farms in open bodies of water. Better wind speeds are available off the coast compared to on land, because it is typically more consistent and stronger over the sea, due to the absence of topographic features that disrupt wind flow. So its contribution in terms of electricity supplied is higher. Furthermore, offshore wind turbines are less obtrusive than turbines on land, as their apparent size and noise is mitigated by distance.

There are nonetheless trade-offs. The operation and maintenance are more complicated than in land, the environment is more corrosive owing the salinity and humidity, the construction of the foundations on the seabed difficulties and increases the installation costs. However, the main differentiating feature is the energy transmission system to the shore.

Two transmission options are used to transport the energy generated on the offshore wind farms to the grid connection point on the shore: HVAC or HVDC. Both the generation and the distribution grid are AC, so by using HVAC submarine cables only some transformers to step up and accommodate the voltage are required at both transmission ends in order to reduce the resistive line losses. On the other hand, if DC is the transmission choice, besides the transformers an apparatus to convert from AC to DC and vice versa is imperative as represented in Fig. 1-6c. The latter requirement is an important drawback which can be countered with the power savings related to reactive currents. Due to the short distance between the conductor and the shield, subsea power cables exhibit a much higher shunt capacitance, in the order of 100-200 nF/km meanwhile in overhead lines it is around 9-13 nF/km. Accordingly, a large charging current flows through the cable as soon as it is energized. This current is proportional to the length of the cable an even at moderate lengths (50-150 km) its magnitude can approach the cable's rated current reducing the power transfer capability of the cable [4]. AC power transmission suffers from these reactive losses meanwhile the only losses in a DC (zero frequency) transmission line are the resistive ones, which are present in AC lines as well.

On the last years several studies ([5], [6], [7] for instance) have been conducted in this field trying to determine the most cost-effective alternative. Although the optimum layout

depending on rated power and distance to shore is not clear, all the analysis concur in stating that HVDC is the most attractive for high power and long distances. An example is shown in Fig. 1-7 in which HVDC is recommended for power higher than 300 MW or a submarine transmission longer than 250 km.

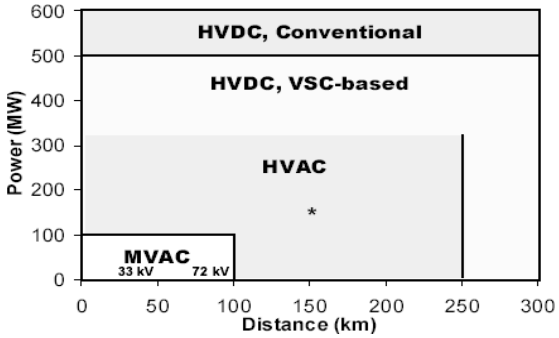


Fig. 1-7. Approximate ranges for voltage options as a function of power and distance [7].

All the currently operational offshore wind farms have HVAC transmission system some of which are listed in Table 1-2 rated by the latest commissioning date. However, BorWin1 is a 400 megawatt (MW) offshore wind farm with HVDC transmission that is presently under construction and is expected to be fully operational by the end of 2012. It will be an 80-turbine wind farm, located 100 kilometres northwest of the isle Borkum (Germany), in water which is 40 metres deep.

Wind farm	Total Capacity	Country	No. of turbines	Commissioning date
Longyuan Rudong Intertidal	131.3 MW	China	37	2012
Ormonde	150 MW	UK	30	2012
Walney (phases 1&2)	367.2 MW	UK	102	2012
Baltic 1	48 MW	Germany	21	2011
Thanet	300 MW	UK	100	2010
Bligh Bank (Belwind)	165 MW	Belgium	55	2010
Gunfleet Sands	172 MW	UK	48	2010
Donghai Bridge	102 MW	China	34	2010
Robin Rigg (Solway Firth)	180 MW	UK	60	2010
Rødsand II	207 MW	Denmark	90	2010
Horns Rev II	209 MW	Denmark	91	2009
Alpha Ventus	90 MW	Germany	12	2009
Rhyl Flats	60 MW	UK	25	2009
Princess Amalia	120 MW	Netherlands	60	2008
Lynn and Inner Dowsing	194 MW	UK	54	2008

Table 1-2. Latest operational offshore wind farms.

Onshore wind farms as well as offshore wind farms with AC transmission system are a mature technology. Therefore, from the three aforementioned wind farm layouts this study will be focused in the last one, offshore wind farms with HVDC transmission system.

Fig. 1-8. Photographs of Horns Rev II offshore wind farm taken from. Source: [8].

1.2 Description of a HVDC transmission based offshore wind farm

This section gives an overview of how the energy transmission from offshore wind farms to shore is accomplished. The complete layout of the system is illustrated in Fig. 1-9 and then a brief description of its main parts is presented.

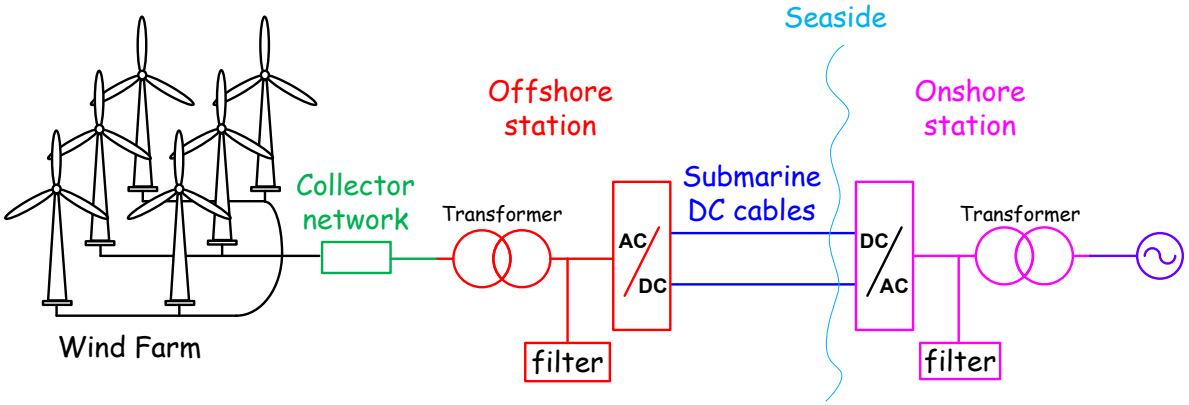


Fig. 1-9. General layout of an offshore wind farm transmission system.

The electricity generated in the wind turbines, which are placed further away from the shoreline, is collected in the medium voltage inter-turbines network. In order to reduce transmission losses, at the offshore station it is transformed to high voltage, then filtered to eliminate undesirable harmonics and finally converted to DC by a power converter. Afterward it is ready for transferring by submarine cables towards the onshore station where the reverse action takes place. Once it is again converted to AC and filtered on such a way that it fulfils the grid codes, the electricity is adapted to the voltage levels of the grid on the onshore connection point.

1.2.1 Wind farm

The offshore wind power plant (WPP) is considered to be a large size and capacity wind farm located at more than 100 kilometres off the coast where noise and visual impact cannot be perceived from the inhabited areas. Assuming that the wind power has a non-controllable stochastic character since it depends on the weather conditions, better wind speeds (stronger and less roughness) are available offshore than on land.

It consists of a large number of wind turbines which can be classified by three parameters according to most of the authors [9], [10]: the direction of the rotor axis (vertical or horizontal), the number of rotor blades and the rotor position (upwind or downwind). They are comprised of rotor blades, a gearbox, an electrical AC generator, the associated power electronics and measuring devices (anemometer and wind vane primarily).

Due to the large size of the wind farm, the average distance between wind turbines and the collecting point can be of some kilometres. This is why each turbine has its own transformer to step-up the output voltage level to the medium voltage of inter-turbines line with the aim of reducing losses along the mentioned distance.

1.2.2 Wind turbines

Up to 2005 all turbines installed offshore had been 2 or 3 MW. Since 2006, 3.6 and 5 MW wind turbines have been introduced [11]. But the situation is changing. Experts state that we stand on the threshold of a revolution in the wind power and with the right equipment besides strategy, huge returns on investment are achievable. That is why nowadays, a new generation of turbines 100 per cent dedicated to offshore environments are being developed [12].

As a progression from the G10X 4.5-MW turbine, Gamesa has developed the G11X, a 5 MW permanent magnet generator with full-scale converter [13]. Regarding Repower Systems, after the great success in REpower 5M, the new REpower 6M offshore wind turbine represents the further development of its predecessor with a 6 MW asynchronous doubly-fed generator [14]. That same rated output power has achieved Siemens Wind Power in their SWT-6.0-120 prototype in which several trials to assess its performance and availability are now being conducted. This wind turbine is fitted with an innovative direct drive and therefore does not require a gearbox. If everything proceeds according to schedule, the SWT-6.0-120 wind turbine should enter series production in 2014 [15].

In the same way, Alstom has built up a new generation, high yield offshore wind turbine prototype: Haliade 150 – 6 MW, with a direct drive permanent magnet generator plus a full conversion converter [16].

With the launch of the V164-7.0 MW Vestas introduces almost the largest wind turbine: a 7 MW permanent magnet generator provided with a full scale converter which has been designed with challenging offshore conditions in mind [12]. There is still a bigger one: Enercon E-126 which is able to generate up to 7.5 MW with a direct-drive annular generator [17].

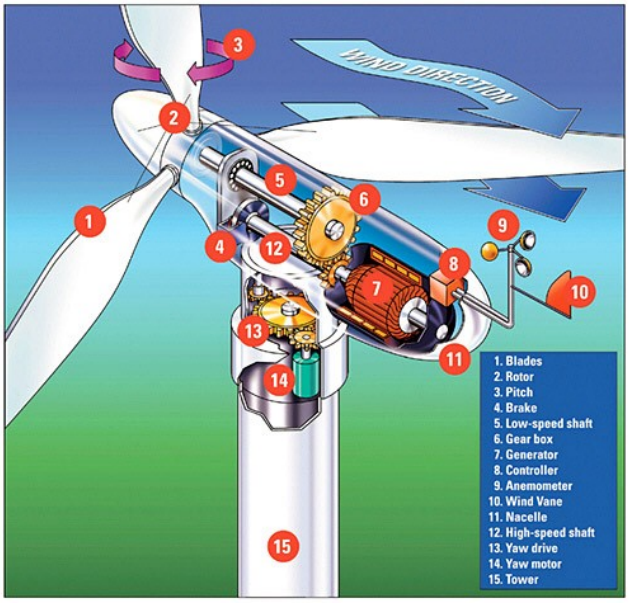


Fig. 1-10. Wind turbine components. Source: NREL.

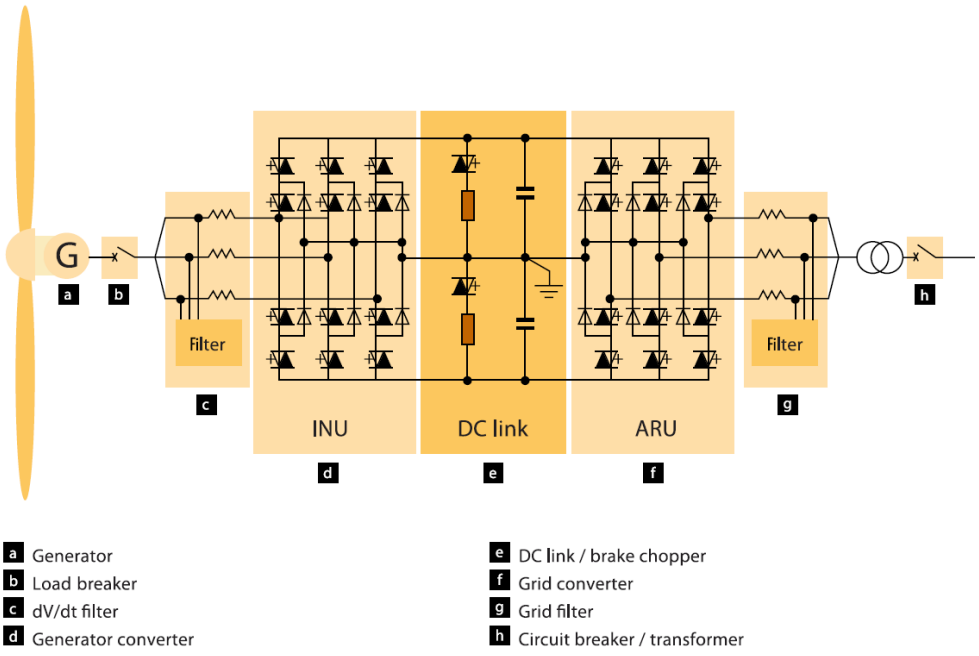


Fig. 1-11. A wind turbine general system design in which all its components are specified. Source: [18].

Each wind turbine has on a single platform inside the tower a compact full scale converter installed. As the power ratings of the wind turbines increases, medium voltage converters have become more competitive. The technology of the converter is in general a 3L neutral-point-clamped (see Fig. 1-11). This converter, which uses PEBB technology IGCT as semiconductor, acts as a drive and can operate in all 4 quadrants, providing bidirectional power flow and full reactive power control. Moreover, during grid disturbances, the brake chopper dissipates the generated power in a shunt resistor. As soon as the fault has cleared, the turbine is taken back smoothly onto the grid in compliance with grid codes.

1.2.3 Local inter-turbine grid

The local inter-turbine grid can be AC or DC (this feature does not determinate the transmission systems technology), but the installed majority is an AC collector grid. Regarding the voltage level, the usage of above 36kV for the inter-turbine grid becomes uneconomic due to the impossibility to accommodate switchgear and transformers in each turbine tower. So, a medium voltage such as 33kV is widely used for collection schemes [19].

The cable length to the offshore collector point depends on the number of wind turbines, their disposition and the space among them which must be enough to avoid turbulences generated at the surrounding turbines, usually from 500 to 1000 m between two of them [20]. There are various standard arrangements for wind farm collector systems but these four designs are the most employed in existing offshore wind farms:

- Radial design
- Single side ring design
- Double-side ring design
- Star design

The layouts of the four listed designs are illustrated in Fig. 1-12 from the simplest one to the most reliable [21]. The differences are related to the length and sizing of the cable, redundancy, energy saving thanks to extra paths, etc.

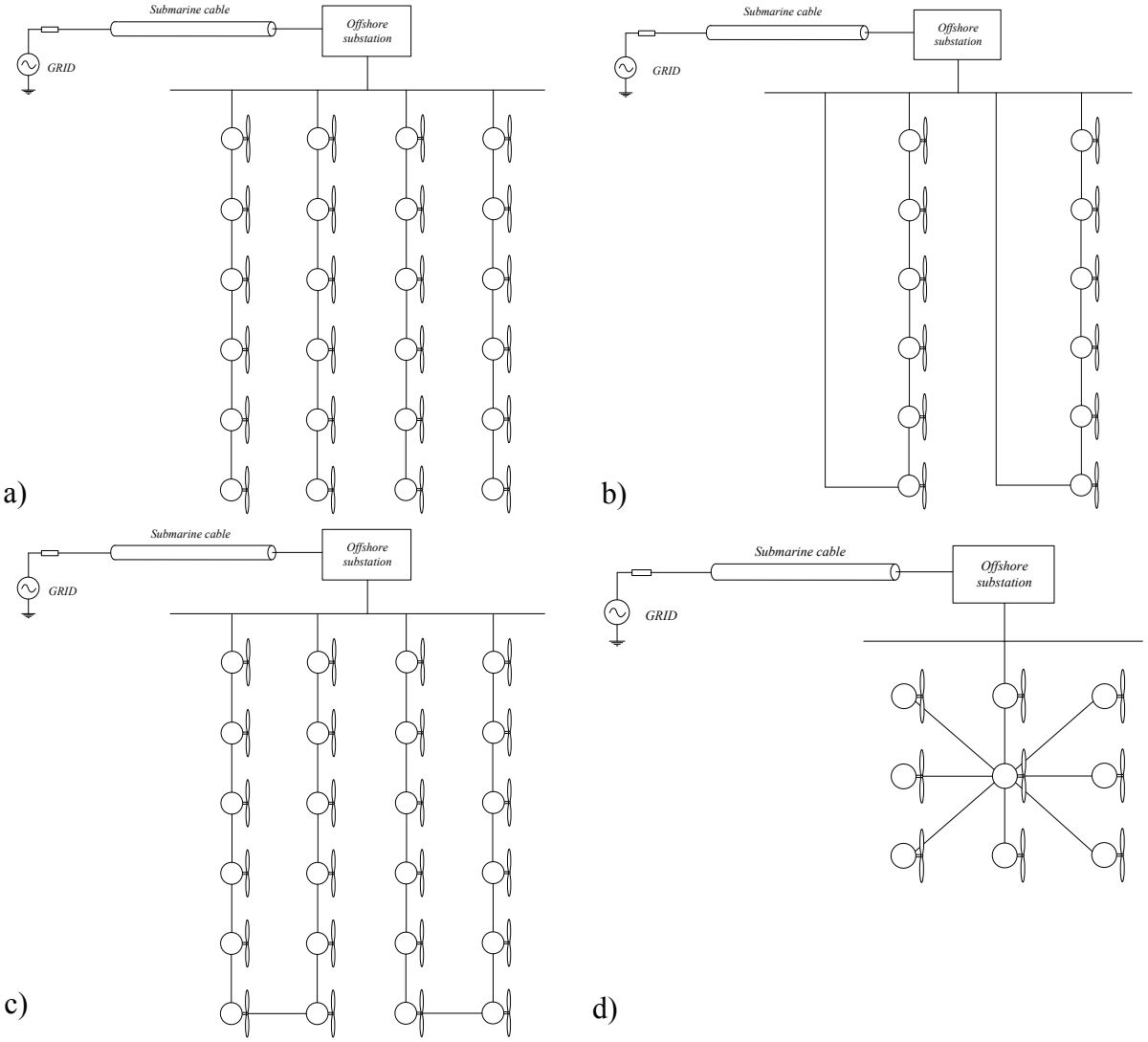


Fig. 1-12. Layout of the local inter-turbine grid. a) Radial design. b) Single side ring design. c) Double side ring design. d) Star design.

1.2.4 Offshore platform transformer

On the offshore transformer platform step-up transformation takes place to interconnect the VSC with the AC network. The main function of the transformers is to adapt the voltage level of the AC network to a voltage level suitable to the converter and galvanic insulation of the two connected circuits. This voltage level can be controlled using a tap changer, which will maximize the reactive power flow.

Dry type transformers are preferred in offshore applications rather than oil-filled transformer basically because they require less maintenance services as well as space. Oil-filled transformers are capable of working at higher voltages and powers thanks to its better cooling characteristics. However, this liquid needs a regular maintenance which is a handicap in

station on the sea. Moreover this type of transformers needs greater installation space owing to the fire safety measures which must be taken to avoid oil combustion.

The transformer is modelled using the equivalent circuit designated in [22] as the classical approach and depicted in Fig. 1-13. Power loss in the windings is current-dependent and is represented as in-series resistances R_p and R_s. Flux leakage results in a fraction of the applied voltage dropped without contributing to the mutual coupling, and thus can be modelled as reactances of each leakage inductance X_p and X_s in series with the perfectly coupled region. Iron losses are caused mostly by hysteresis and eddy current effects in the core and are represented by a resistance R_c in parallel with the ideal transformer. A core with finite permeability requires a magnetizing current I_m to maintain the mutual flux in the core. It is modelled as a magnetizing reactance X_m in parallel with the core loss component R_c. If the secondary winding is made open-circuit, the current i_0 taken by the magnetizing branch represents the transformer's no-load current.

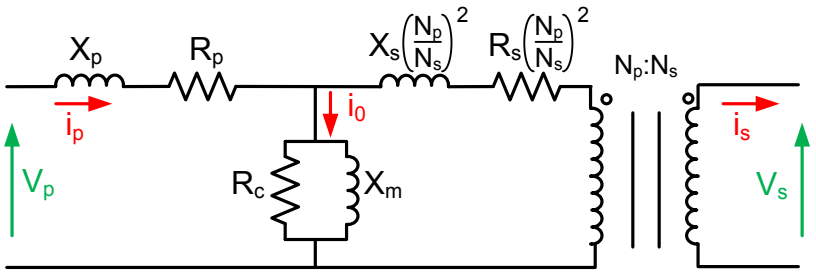


Fig. 1-13. Transformer electrical equivalent circuit per phase with secondary impedances referred to primary side.

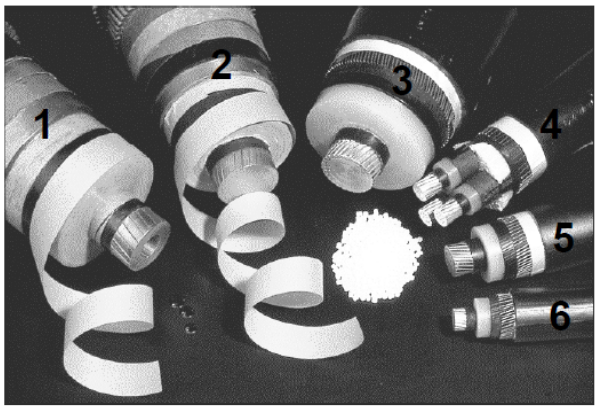
1.2.5 Converters

The converter is the distinct and essential element of this transmission system. In total two of these are needed in the system, one at each HVDC end. An AC/DC is placed on the offshore station and the DC/AC is a part of the onshore converter station. As will be later detailed, two principal technologies exist for this purpose: LCC (Line Commutated Converter) using the classical thyristors and VSC (Voltage Source Converter) using IGBTs or IGCTs.

1.2.6 HVDC transmission cables

They are the physical medium to transfer the energy from the offshore station to the onshore PCC (Point of Common Coupling). For long distance transmission of bulk electrical power generated at the wind farm to the grid, high voltage direct current cables are installed undersea. HVDC systems may be less expensive and suffer lower electrical losses in contrast

with the more common alternating current systems because it avoids the heavy currents required by the cable capacitance.



1. LPOF for a.c. or d.c.
2. MIND for d.c.
3. Single core XLPE for a.c.
4. Three core XLPE for a.c.
5. Extruded sea cable for VSC
6. Extruded land cable for VSC

Fig. 1-14. High voltage cables. Source: ABB [23].

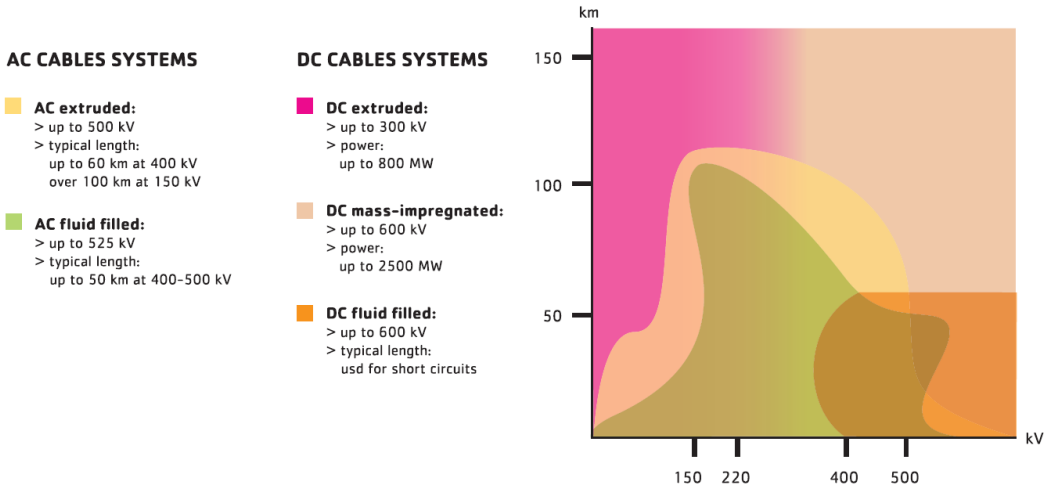


Fig. 1-15. Power transmission cable systems. Source: [24].

Some of the basic requirements of a submarine cable are: Long-life design, low environmental impact as well as maintenance, mechanical resistance capable of withstanding undersea installation, high reliability and long manufacturing lengths to minimize cable joints. There are different available type of cables depending on the insulation and the transmission parameters such as power and voltage. Mass Impregnated cables (high-density paper tapes impregnated with a high-viscosity compound) have proven suitable for voltage ratings up to 600kV DC and current rating up to 1600A and without requiring fluid pressure feeding, thus allowing these cables to be installed in HVDC links in very long lengths, up to several hundreds of kilometres. However, due to the remarkable applicability of VSC for HVDC transmissions, which allow the power to be transmitted in both directions without requiring polarity reversal, has allowed re-introducing the use of extruded cables (called XLPE) in DC

power transmission. With the polarity reversal being no longer required, the problem of space charges that can arise with an extruded insulation and create excessive dielectric stress within the cable in the case of sudden polarity reversal is avoided. Extruded insulation offers several remarkable advantages and makes for lighter and easier-to-handle cables, which can operate at high temperatures and at high electrical stresses up to 300kV. The graph in Fig. 1-15 shows the variety of cable systems which could fit best according to the transmission length and voltage.

From the broad range of types described, polymeric cables are usually the preferred choice for HVDC mainly because of their mechanical strength, flexibility and low weight [25].

Based on the electric representation of the cables and depending on the cable model requirements, it is possible to perform more or less simplifications, in order to maintain the accuracy of the model and reduce its complexity. There are two basic transmission line or cable modelling techniques [26]:

a) Models based on constant parameters: Π models or Bergeron model.

b) Models based on frequency dependent parameters: modal domain or phase domain.

A single π model is used more commonly for normal design and control study in order to model the transients in easy way. If the objective is the analysis of a wide frequency spectrum accurately, a more precise model of a line can be developed considering the distributed parameters and frequency dependent. An example of the simple π model is represented in Fig. 1-16. The parameters for a 100 km line are taken from [26] where the whole analysis regarding the way to obtain them in PSCAD is explained.

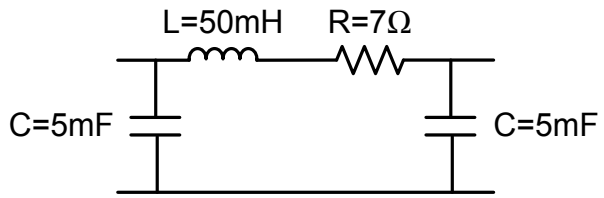


Fig. 1-16. Standard Π model using the parameters validated in [26] for a 100km line.

1.2.7 Resonant passive filters

An HVDC converter station usually requires ac filters, the purpose of which is to mitigate voltage distortion. On the AC side of a 12-pulse LCC-HVDC converter, current harmonics of the order of 11, 13, 23, 25 and higher are generated. Filters are installed in order to limit the amount of harmonics to the level required by the network apart from compensating to a

certain extent the reactive power. However, with VSC converters there is no need to compensate any reactive power consumed by the converter itself and the current harmonics on the AC side are related directly to the PWM frequency. Therefore the amount of filters in this type of converters is reduced dramatically compared with natural commutated converters.

The passive filters are connected near the transformer to lessen some specific harmonics. The resonant passive filters are constituted by a series connection of a capacitor, an inductor and a resistor, this is, a RLC branch (see Fig. 1-17). The main property of this kind of branch is the delay of 180º between the voltage drop in the inductive impedance and the voltage drop in the capacitive impedance. As a consequence of this characteristic, at the resonance frequency, inductive and capacitive impedances counteract (becoming zero the reactive part of the circuit impedance) and as a result the electric branch only presents the resistive impedance.

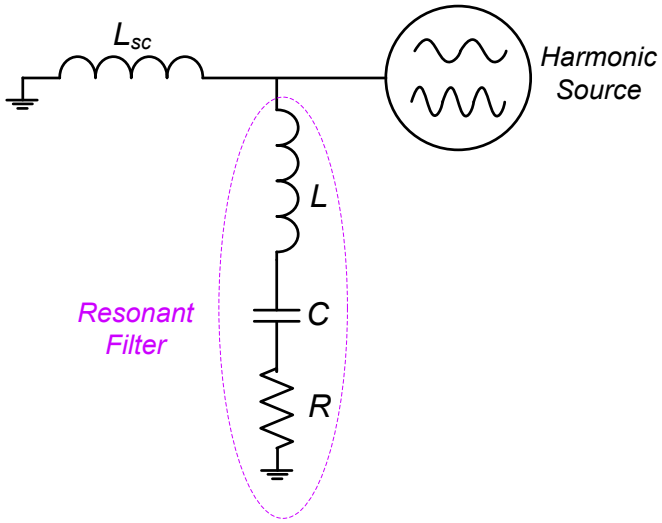


Fig. 1-17. RLC resonant filter in parallel with the system.

The RLC branch is tuned to present only the resistive part at the frequency where the harmonic, which is wished to be eliminated, is located. That is achievable by means of infinite combinations of the two independent *L* and *C* parameters of the RLC circuit as deduced from (1-1).

$$Z = R + j \cdot \left(2 \cdot \Pi \cdot f \cdot L - \frac{1}{2 \cdot \Pi \cdot f \cdot C} \right) \qquad (1\text{-}1)$$

It should be highlighted that to attain a reduction higher than a 50% of any harmonic current with this kind of filters (a RLC branch in parallel with the circuit), the impedance of the filter at the selected frequency has to be less than the impedance presented by the system *(L_{sc})* at that frequency. In this way, part of the generated harmonic current is deviated (according to

Kirchoff's law) to the filter instead to flow to the distribution grid or power source as represented in Fig. 1-18.

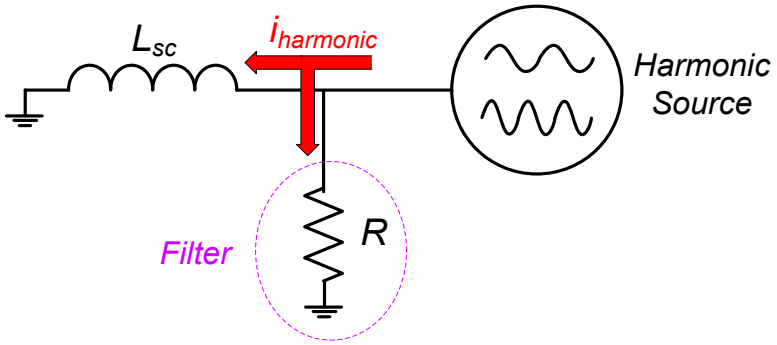


Fig. 1-18. Simplified RLC filter at the resonance frequency in parallel with the system.

It will be shown later in this report that filters will be dispensable when MMC with high number of submodules is used because the obtained output voltage waveform is of very good quality being its harmonics placed at quite high frequencies.

1.2.8 Electrical grid

It is the main electrical distribution grid to which the energy coming from the wind farm is integrated. It is fundamental to bear in mind that not every world countries have got the same legislation in force what means that the transmission system has to meet the current regulations at the PCC. For that, the onshore substation adapts the voltage, frequency and the reactive power of the transmission system to the voltage level, frequency and reactive power required by the main grid.

1.2.9 Coordinated control system

In the case of VSC-based HVDC transmission systems the transfer of power is controlled in the same way as in the case of a classical HVDC transmission [27], the inverter side controls the active power, while the rectifier side controls the DC voltage [28]. One of the advantages of VSC-HVDC is that it makes possible to independently control the active power and the reactive one. Unlike the power transmission between two AC grids in which the power flow can be bidirectional, the VSC-based HVDC system that is used to deliver power from an offshore wind power plant, the active power flow is unidirectional (the offshore side is delivering active power to the onshore side and not vice-versa).

As represented in Fig. 1-9, in a VSC-based HVDC transmission between an offshore WPP and an AC network, two converters are needed: one offshore and another one onshore. Despite not existing direct communication between the two VSC controllers, the objective of

the coordinated system lies in guaranteeing the stability of the whole system. It has to ensure that the energy produced by the wind farm is injected first into the DC link and then transferred into the grid at the onshore side. This entire task has to be accomplished carefully to damp out troublesome oscillations which could disrupt the normal operation of the large interconnected power system.

The offshore HVDC station has the rectifier task which means that all the AC energy delivered by the wind farm is transformed in DC and sent to the land through the DC cables. As shown in Fig. 1-19 the offshore VSC controller maintains the offshore AC inter-turbine grid voltage and frequency. The AC voltage is controlled by the means of the reactive power reference while the frequency is controlled according to the active power which has to be delivered.

The onshore VSC controller regulates the HVDC bus voltage and the reactive power or AC grid voltage for grid codes compliance [29]. In this case the reference values for the fast inner current controllers are obtained as represented in Fig. 1-19: the DC voltage controller provides the reference value for the active current and the reactive power controller or the AC voltage controller for the reactive current [30].

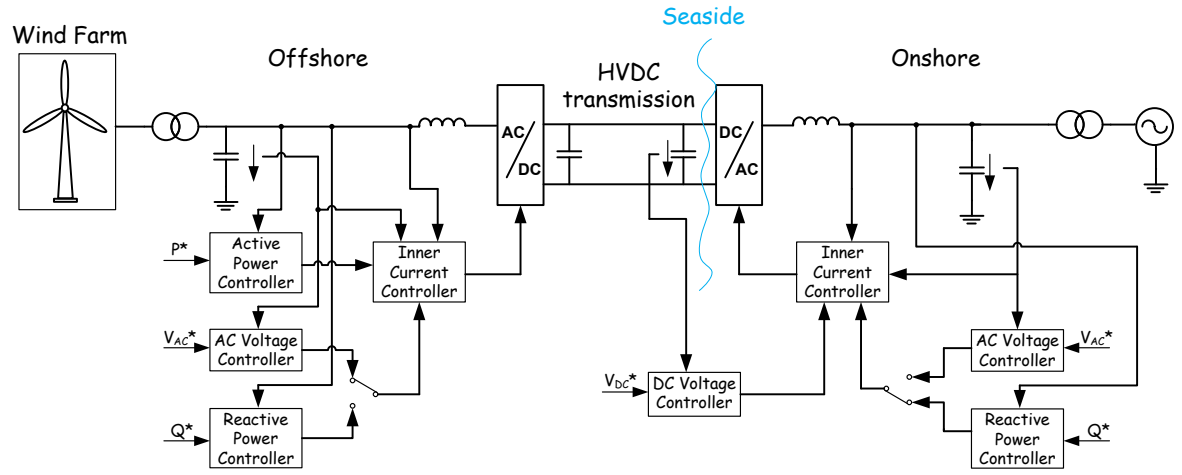


Fig. 1-19. Overall control structure of the VSC-HVDC transmission system [31].

Most of the existing HVDC connection systems in the world are point to point. It means that only one sending-end and one receiving-end stations are available. This kind of connection does not allow the expansion of physical interconnection capacity and improvements of the possibility of power exchange. Nowadays, multiterminal connection (see the diagram represented in Fig. 1-20) is the solution for this lack and it is a suitable solution that can provide the offshore wind farm connection and also that can facilitate the transnational exchange with high cost efficiency [32].

However, when more than one receiving-end station is considered, the control of DC voltages and the power sharing which guarantees the power exchange between the inverter stations can bring some complications. Due to the random behaviour of the wind energy, at any moment is not possible to precisely determine the power which can be delivered. Power converters play an essential role in the safe operation of the system. In order to guarantee the DC voltage balance and power sharing, in [33] three control strategies are compared: scheduled power control, DC voltage droop control and central DC voltage control.

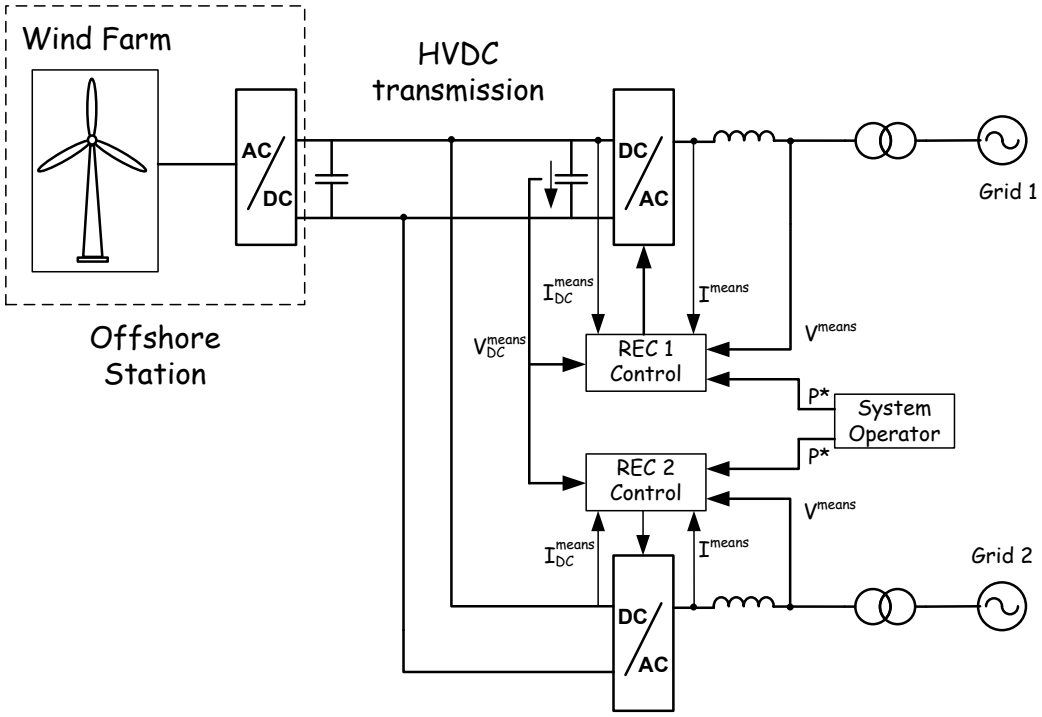


Fig. 1-20. Overall control structure of the MTDC system [34].

1.3 Converter technologies

Along with the development of the power devices, the AC drive system has improved. Fig. 1-21 shows the progress of the power devices and the drive systems development. The diode and thyristor were developed at first. The thyristor was able to turn on the power but the thyristor cannot turn off by itself, so it must be turned off with the help of outside conditions. Then GTO appeared with a function of turn on and turn off capability. Then the GCT/IGCT was developed as fast switching device. Now, the GCT/IGCT is used for large ac drives. And IGBT and IEGT were also developed and now used widely for large ac drives.

Based on the development of the power device and main circuit design, the multilevel inverters are developed and applied in wide range of industries.

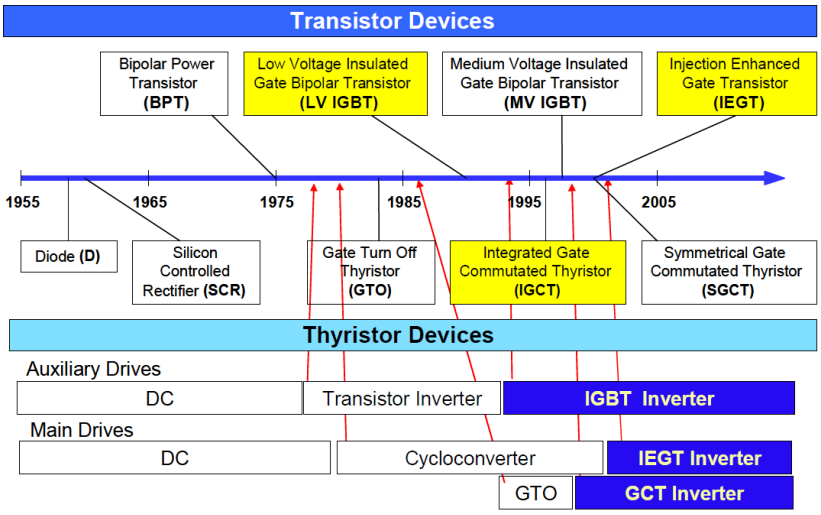


Fig. 1-21. Progress of the power devices and the drive systems. Source: [5].

HVDC technologies are often categorised by the power electronic switching device used within the AC to DC converter. **Line commutated current source converters (LCC-CSC)** use thyristor based converters and are capable of achieving high power ratings. Traditionally, it has been the technology for transmitting vast amounts of energy from point to point within an HVDC system (see Fig. 1-22). This tried and tested technology is primarily chosen because of the reliability and robustness inherent within the thyristor valves at the heart of the converter. Over the last decades, progress within the rating and dependability of the thyristor valve has allowed this technique to become more practical and cost effective. It has become the primary technique for medium to long distance electrical transmission with a total of more than 80GW worldwide [35]. However they require a synchronous voltage source to operate due to the limited flexibility inherited within the thyristor valve.

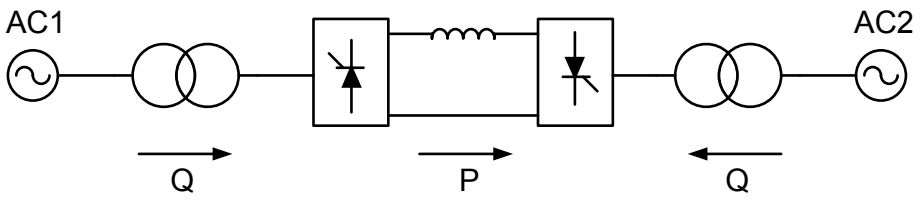


Fig. 1-22. HVDC system based on LCC technology.

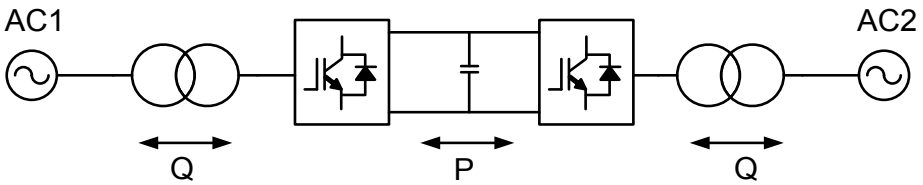


Fig. 1-23. HVDC system based on VSC technology.

Recent developments within power electronics have engendered the rise of a contending technology parallel to CSC-LCC. Previously, **self commutated voltage source converters**

(VSC-SCC) had lacked the robustness, plus the high voltage and current rating to be considered for high power transmission. This changed following the development of, amongst others, the Insulated Gate Bipolar Transistor, a device which marries the controllability of the MOSFET with the reliability and power rating of the BJT. The increasing penetration of the power electronics technologies into the power systems is mainly due to the continuous progress of the high voltage high power fully controlled semi conductors. The full controllability and switching symmetry through both turn-on and turn-off operation allows the device to reverse power flow much more quickly than its predecessor. Meanwhile the thyristor can only commute once per cycle, IGBTs can do it several times. This property enables the voltage and current modulation of the converter in order to outage better quality waveforms. Current flowing in the opposite direction is conducted by a reversed diode in parallel to the IGBT. However, this additional component brings a weakness to the system when a fault occurs on the DC side by creating a path for the resulting fault current.

a)  b) 

Fig. 1-24. a) First HVDC thyristor valve (1967). b) The world's first 12-pulse converter (1976). Source: ABB [23].

It is useful to consider some of the advantages the VSC transmission system offers [36]:

- The ability to control reactive and active power independently.
- The link is operational with weak AC systems.
- No commutation failures within the converter.
- Black-start capability.

- No polarity reversal required to reverse the power flow direction which has a positive effect on the isolation of the conductors.
- The modularity of the converter reduces manufacturing costs, facilitates maintenance and permits provisions for spare parts.
- With the use of intercycle PWM switching, or multi-level configurations in the VSC schemes, the filter requirements are drastically reduced or even eliminated altogether.

Project Name	Commissioning year	Power rating	No. of circuits	AC voltage	DC voltage	Length of DC cable	Reasons for choosing HVDC	topology
Hällsjön, Sweden	1997	3 MW ±3MVAR	1	10 kV (both ends)	± 10 kV	10 km Overhead lines	Test transmission. Synchronous AC grid	2L
Gotland HVDC light, Sweden	1999	50 MW -50 to +55MVAR	1	80 kV (both ends)	± 80 kV	2×70 km Submarine cables	Wind power (voltage support). Easy to get permission for underground cables.	2L
Eagle Pass, USA	2000	36 MW ±36MVAR	1	138 kV (both sides)	± 15.9 kV	Back to back HVDC light station	Controlled asynchronous connection for trading. Voltage control. Power exchange	3L-NPC
Tjaereborg, Denmark	2000	8 MVA 7.2 MW -3 to +4 MVAR	1	10.5 kV (both sides)	± 9 kV	4×4.3 km Submarine cables	Wind power. Demonstration project.	2L
DirectLink, Australia	2000	180 MW -165 to +90 MVAR	3	110 kV (Bungalora) 132 kV (Mullumbimby)	± 80 kV	6×59 km Underground cable	Controlled asynchronous connection for trading. Easy to get permission for underground cables.	2L
MurrayLink, Australia	2002	220 MW -150 to 140 MVAR	1	132 kV (Berri) 220 kV (Red Cliffs)	± 150 kV	2×180 km Underground cable	Controlled asynchronous connection for trading. Easy to get permission for underground cables.	3L-ANPC
CrossSound, USA	2002	330 MW ±150MVAR	1	345 kV (New Heaven) 138 kV (Shoreham)	± 150 kV	2×40 km Submarine cables	Controlled connections for power enhance. Submarine cables.	3L-ANPC
Troll offshore, Norway	2005	84 MW -20 to +24 MVAR	2	132 kV (Kollsnes) 56kV (Troll)	± 60 kV	4×70 km Submarine cables	Environment, long submarine cable distance, compactness of converter on platform electrification.	2L
Estlink, Estonia-Finland	2006	350 MW ±125MVAR	1	330kV (Estonia) 400kV (Finland)	± 150 kV	2×31 km Underground 2×74 km Submarine	Length of land cable, sea crossing and non-synchronous AC systems.	2L
Caprivi Link, Namibia	2009	300 MW	1	330kV Zambezi 400kV Gerus	350 kV	970 Overhead lines	Synchronous AC grid, long distance, weak networks	-
Valhall offshore, Norway	2009	78 MW	1	300 kV (Lista) 11kV (Valhall)	150 kV	292 km Submarine cables	Reduce cost and improve operation efficiency of the field. Minimize emission of green house gases.	2L
BorWin1, Germany	2012	400 MW	1	380 kV Diele 170kV Borkum 2	± 150 kV	2×75 km Underground 2×128 km Submarine	Offshore wind farm, length of land and sea cables, asynchronous system	-

Table 1-3. Summary of worldwide VSC-HVDC projects and their basic parameters.

The recommended converter technology varies depending on the application. Although there is not a well-defined range, the previous Fig. 1-7 represents an approach of the optimum technology according to the application power and transmission distance. So, as indicated in the figure, from 500 MW on conventional HVDC is more favourable than VSC based HVDC. In Table 1-3 some of the worldwide HVDC-VSC projects are collected.

1.4 HVDC-VSC topologies

The VSC HVDC technology using IGBTs recently has gained growing interest due to its simplified modularity and flexibility due to the four-quadrant operation of the converter. One of the main advantages of VSC-based transmission is its ability to control reactive power in both directions, independently of the real power flow. Except for the maximal rating power (which is limited in VSC HVDC to around 500 MW while single LCC HVDC link can possibly transmit more than one GW power [37]), this second topology has superior advantages. That is why from the two converter technologies explained before, this study will be focused on the second one, VSC.

This section deals with a number of VSC topologies suitable for HVDC transmissions. In addition to those topologies and control philosophies already developed by major manufacturers, along this document some variations will be introduced.

1.4.1 Two level converter

HVDC Light conversion system [38] was first introduced by ABB in 1997. It is based on a two level topology meaning that the output voltage is switched between two voltage levels. As can be seen in Fig. 1-25, each phase has two valves, one between the positive potential and the phase terminal and the other between the phase terminal and negative potential. Thus, a three phase converter has got six valves, three phase reactors and a set of DC capacitors. To be able to switch voltages higher than the rated voltage of one IGBT, several positions are connected in series in each valve. A complete IGBT position consists of a StakPak IGBT, a reversing diode, a gate unit, a voltage divider and a water-cooled heat sink [39].

HVDC Light uses a sinusoidal based PWM control philosophy to control the IGBT's gate switching frequency producing a two level AC waveform. This is then improved to a sinusoidal form by the phase reactors. To eliminate harmonics, they are concentrated into a narrow band where small filters can be used. The series connected IGBT's need to switch at exactly the same moment, to do this the voltage over each individual IGBT is measured and a

boost signal is provided to the gate of the transistor depending on the measured voltage. The monitoring system for the IGBT states is managed by a patented ABB control technology.

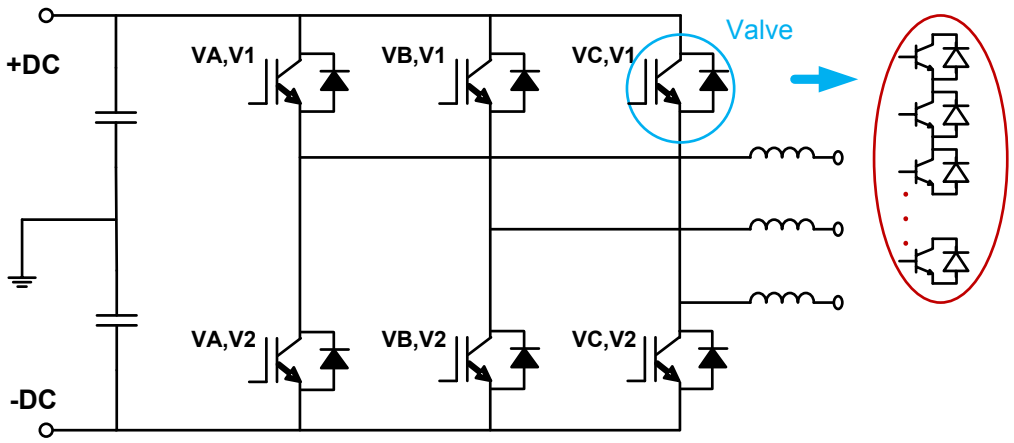


Fig. 1-25. Schematic of a three phase 2 level HVDC-Light converter with series connected positions in each valve.

The latest example of a HVDC Light application is the Borkum 2 (Germany) offshore wind farm transmission which is in operation since 2009. The transmission capacity is 400 MW at ± 150kV DC voltage by 128 km of extruded polymer insulated submarine cables. The receiving station on land is located at Diele, 75 km from the coast, where the power will be injected into the German 380kV grid [38].

1.4.2 Modular Multilevel Converter (MMC)

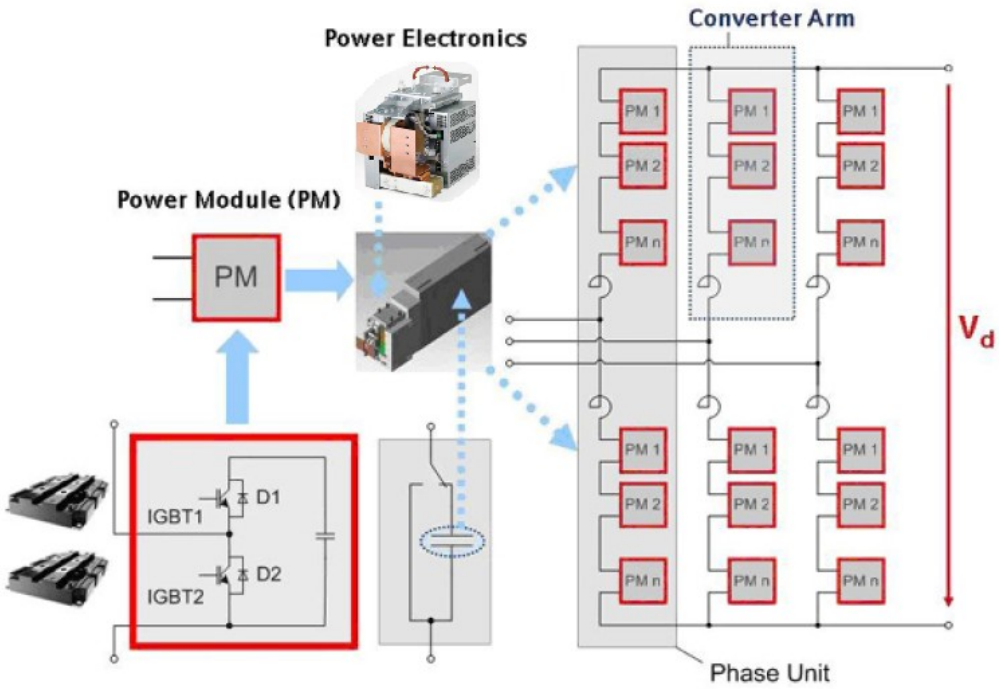


Fig. 1-26. SIEMENS' Modular Multilevel Converter main circuit. Source: [40].

An alternative approach is Siemens' last technology and control system referred to as HVDC Plus [41] which uses multilevel converters (see the three phase schematic in Fig. 1-26). It consists of six converter legs, whereas the individual converter leg consists of a series connection of power modules (PM) connected in series with one converter reactor. Each of the submodules contains an IGBT half bridge as switching element and a DC storage capacitor. The two converter legs of each phase module represent a controllable voltage source because it is possible to separately and selectively control each of the individual submodules. The total voltage of the two converter legs in one phase unit equals the DC voltage, and by adjusting the ratio of the converter leg voltages in one phase module, the desired sinusoidal voltage at the AC terminal can easily be achieved. The AC waveform is built using small voltage steps formed by controlling the modules which are turned off or turned on at any given instant. Therefore there is very small need for AC voltage filtering to achieve a sinusoidal waveform in comparison to a two level circuit. This approach of using modules maximises the output voltage of the converter as many modules can be used in series [42]. The first project to use HVDC Plus came online in November of 2010 and is called the Trans Bay Cable in California.

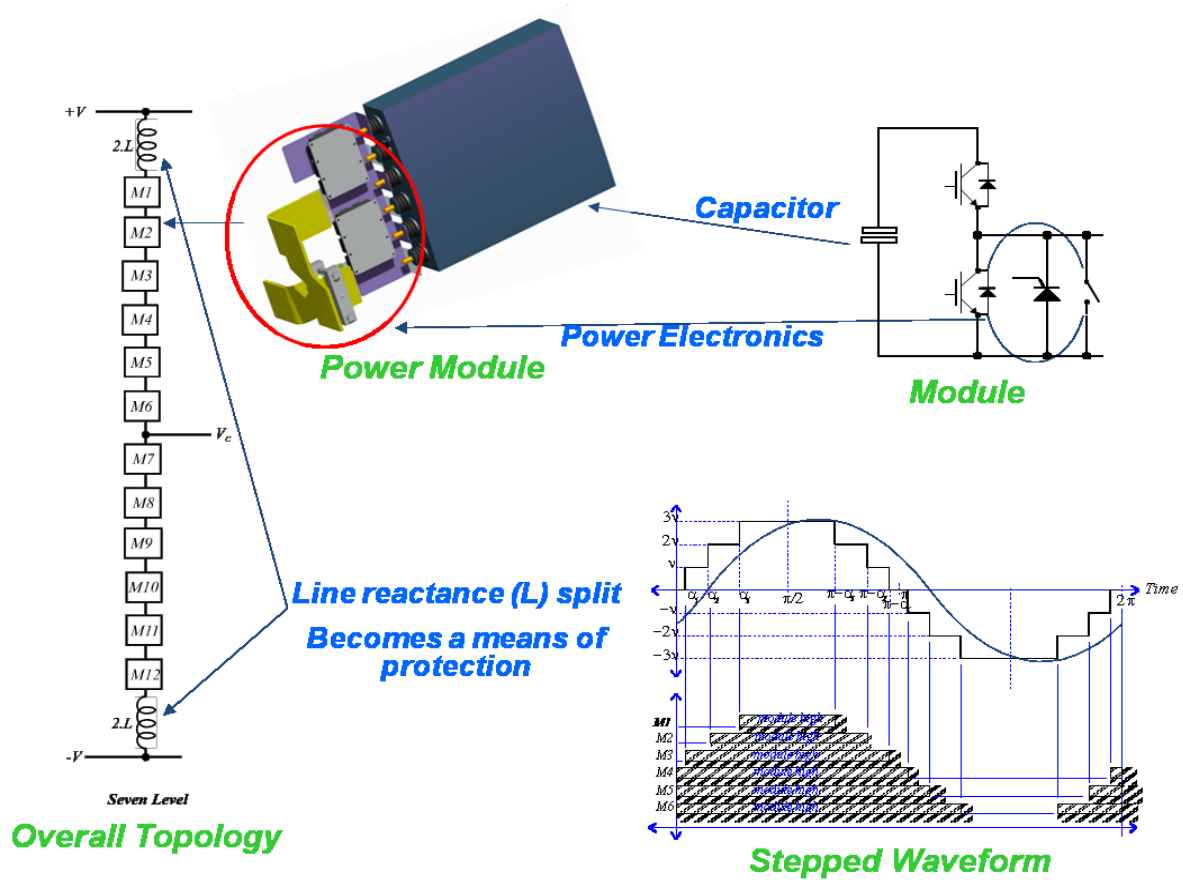


Fig. 1-27. Alstom Grid's Chain-link converter based VSC-HVDC main equipment. Source: [40].

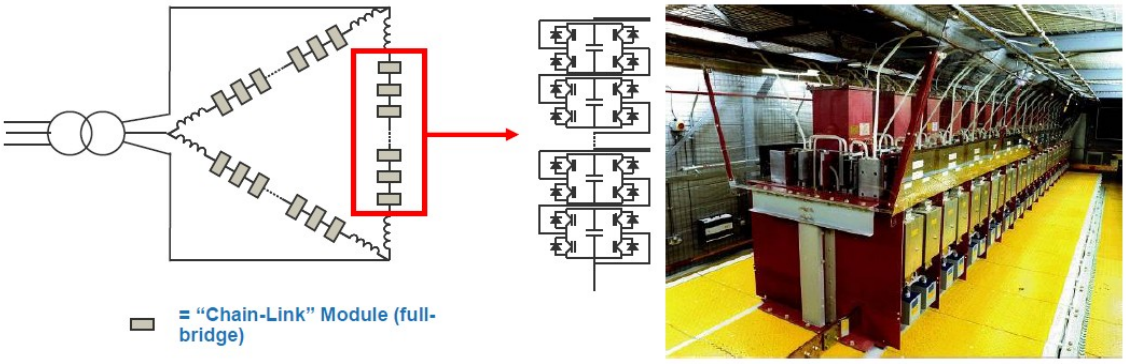


Fig. 1-28. Alstom Grid's STATCOM based on the MMC or "chain circuit": circuit arrangement (left) and one phase of a ±75MVAr STATCOM supplied for National Grid's East Claydon substation. Source: [43].

Two other prominent manufacturers, Alstom Grid and ABB, have developed very similar Modular Multilevel Converters (MMC) known by the commercial trade names Chain-Link and Cascaded Two Level converter (CTL) [44] respectively. This fact is evidenced by Fig. 1-27 and Fig. 1-29 where little differences in the arrangement can be found. However, it has to be highlighted the fact that in CTL series-connected press-pack IGBTs are used in the valves, thus extending a technology which successfully has been used for high voltage two-level VSCs to multilevel VSCs through cascade connection.

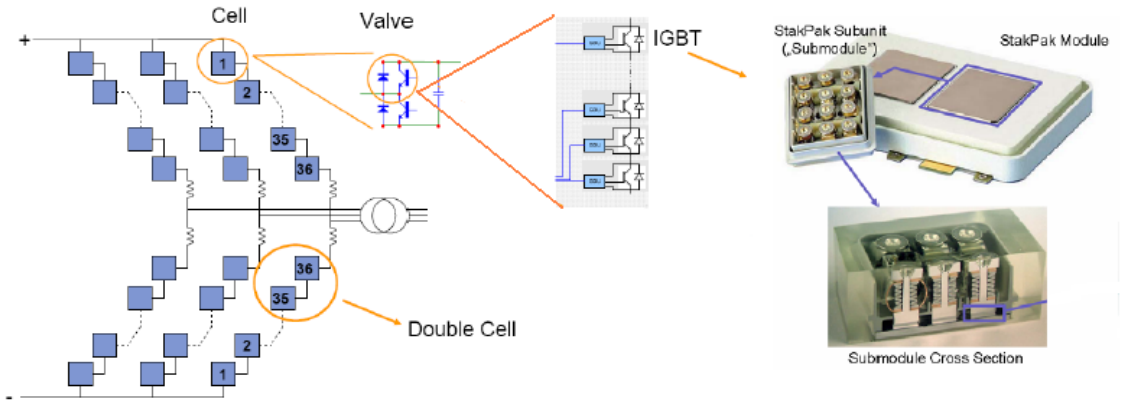


Fig. 1-29. Outline of ABB's Cascaded Two-Level (CTL) converter. Source: [45].

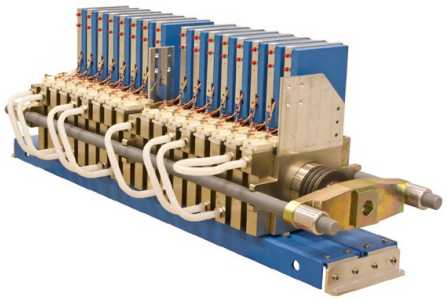


Fig. 1-30. Cell module with two valves, each comprising eight series-connected press-pack. Source: [45].

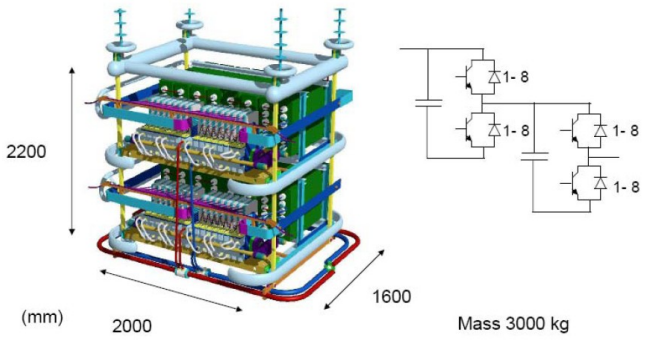


Fig. 1-31. Mechanical outline of ABB's CTL double submodule. Source: [45].

Apart from these two converter topologies, another possible option is the series-parallel connection of converters using transformers. This topology lies in assembling conventional VSC in series or parallel connection using transformers with the aim of reaching the required voltage and current values avoiding the necessity of designing an exclusive converter to fulfill the application requirements. Some configurations appear in patents such as [46] or [47]. However, there is not any known HVDC application in which it has been applied despite being an alternative for the two previous explained topologies.

1.5 Purpose of the thesis

As has been introduced, this thesis was within the framework of the study of electronic power converter topologies oriented to the HVDC transmission of the power generated in offshore wind farms, focusing the research on the Modular Multilevel Converter (MMC) topology. There have been two general objectives pursued in this thesis:

- To study, analyse, compare and evaluate the MMC comprised of different submodule topologies.
- To propose a capacitors voltage balancing algorithm, which can be applied to the MMC with different submodule topologies.

To accomplish these objectives it is necessary to model the converter, to simulate it in Matlab software and then to built a downscaled real test bench in the laboratory to contrast the simulation results with the experimental ones.

1.6 Description of the chapters

This thesis is divided into seven chapters, appendixes and bibliography. The content of these chapters is summarized below:

Chapter 1: the opening chapter reviews the current situation and trends of the wind energy as well as wind farms. Then a HVDC transmission from an offshore wind farm to the onshore substation is thoroughly described. From all the elements which make that energy transmission possible, this thesis is focused on the converter, that is why a brief state of the art of power converter technologies and topologies is exposed. Finally the objectives pursued by this thesis are presented.

Chapter 2: this chapter studies deeply the Modular Multilevel Converter with three different submodule concepts: 2L half bridge, 3L-FC and 3L-NPC. The converter is modelled by means of differential equations, the way of implementing the modulation technique is explained and some simulation results are shown. In addition, a methodology to size the converter capacitors and inductances is presented. Although the total voltage of the submodules is controlled, at the end of the chapter the individual capacitors unbalancing problem is raised.

Chapter 3: Despite the fact that any modulation technique applicable to multilevel converters is also valid for MMC, along this chapter a modulation algorithm based on phase shifted PWM which copes with the capacitors unbalances is introduced. Firstly the general modulation philosophy is explained applied to the 2L submodule concept and then it is extended to 3L-FC, and 3L-NPC submodule topologies. Its effectiveness is confirmed by simulation results at different modulation indexes, $cos(\varphi)$, number of submodules per phase and switching frequency.

Chapter 4: in the fourth part of the report, the validation of the previously developed modulation strategy is carried out by means of successful experimental results obtained in a downscaled laboratory setup. The capacitors balancing at any operation condition are corroborated with submodules 2L and 3L-FC topologies.

Chapter 5: A comparative assessment based on thermal analysis and sizing of the converter elements is made, revealing the benefits and drawbacks of using the studied different submodule concepts (including the 2L half bridge submodules with series connection of several controlled switches) and the conclusions drawn therefrom.

Chapter 6: On the one hand, this chapter deals with technical difficulties associated to the implementation and the structure of the converter. On the other hand, breakdown and failure protections for the system are proposed. Especially an analysis concerning the consequences of malfunctions in submodules is carried out.

Chapter 7: General conclusions and main contributions of the thesis as well as future work are summarized.

Chapter 2

Modular Multilevel Converter (MMC)

From the three converter topologies explained before, the decision as to continue studying in depth the MMC topology has been made. This converter topology has arisen as the leader and most competitive solution for VSC applications operating in the range of high power and high voltage levels [48]-[52]. Transmission of energy by means of HVDC seems to be an application area with an attractive future for this kind of converter topology [44], [53]-[54]. The main characteristics and most important features of this converter are summarized and discussed in publications such as [56]-[61], being its scalability or modular structure and its transformerless nature, probably its major advantages [61]-[62]. Due to these reasons, the MMC provides a suitable and flexible converter design that can be adapted to different ranges of voltages and powers.

Although the majority of the published papers have been focused on MMC designs with two level half bridge submodules [48]-[64], it is also possible to arrange MMC topologies using multilevel submodule concepts, as reported for instance in [65]. Note that under this situation, we can find many possible submodule concepts, just combining the multilevel topology chosen, for example Flying Capacitor (FC), Neutral Point Clamped (NPC), Multi Point Clamped (MPC), Neutral Point Piloted (NPP), etc… and the number of levels used: 3, 4, 5, etc…[59]. This innovative solution, can be interesting for example from a manufacturer perspective, in order to bring already existing and well proven multilevel submodule designs to novel MMC arrangements, or simply to achieve a better usage of the trade components such as the semiconductors. In addition, it can help solving protecting actions taken by different manufacturers related to patents. On the other hand, from a construction point of view, using multilevel

modules is advantageous in reducing the dimensions of the whole converter at expenses of complicating the technology of the submodule.

Therefore, in this thesis besides studying the MMC with 2L submodules, the same converter with unconventional submodules will be researched. Obviously not all the topologies will be considered, only two of the multilevel: the well known 3 Level NPC and the 3 Level FC based submodule concepts.

Along this chapter, first the basic operation of the converter as well as the mathematical behavioural modelling of the MMC with 2L submodules is described. The modelling of the MMC has been carried out through differential equations because it is essential to learn in depth the behaviour of the converter but it is also useful for developing the control of the system and choosing the most suitable modulation technique. Secondly how the modulator generates the switching pulses for the semiconductors using PWM is explained. Then some simulation results are exposed to clarify the previous concepts. The same steps have been followed for the MMC with 3L-FC and 3L-NPC submodules.

A sizing methodology for the passive components of the converter (the inductances and capacitors) is also included. After that, the way of controlling the voltage of all the submodules of the converter is presented. Despite employing this control method, the balancing problems which appear in the submodules capacitors will be discussed. To end up, the obtained conclusions of the chapter are provided.

2.1 MMC with 2L submodules

2.1.1 Modelling

The aim of modelling the converter by means of differential equations is first to describe its behaviour taking into consideration that all the switches are ideal. This helps develop a deeper understanding of the performance of the system. Moreover, thanks to the mathematical model the converter can be simulated, the different control loops designed and the suitable modulation technique chosen.

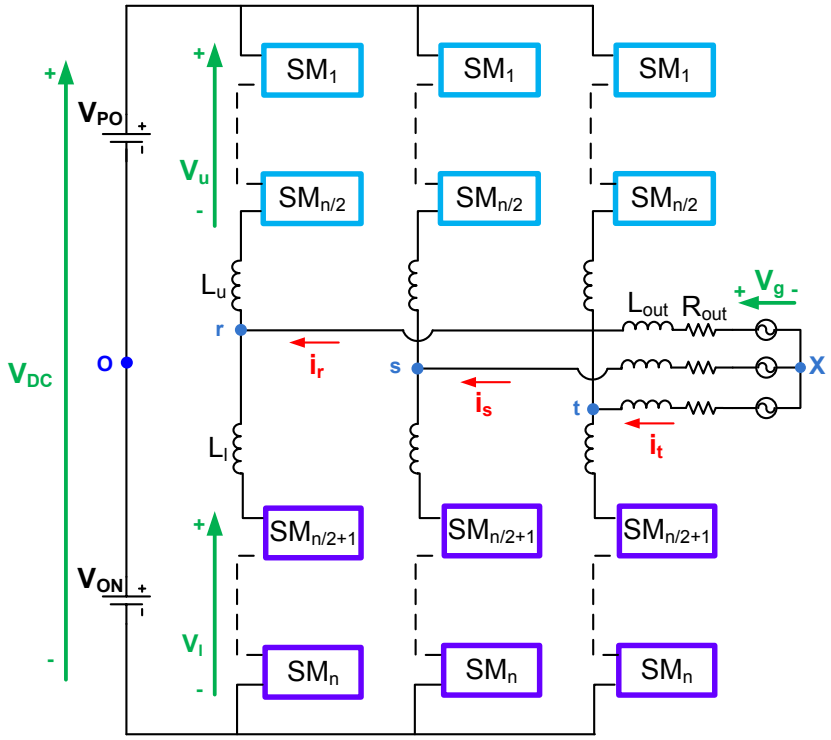


Fig. 2-1. Layout of the three phase MMC.

The layout of the three phase Modular Multilevel Converter is shown in Fig. 2-1. The converter consists of three identical phase units, each with upper and lower multivalves. However, for the following developments, the simplest structure will be considered, this is, the single phase converter with *n* submodules shown in Fig. 2-2. It consists of two arms of converter, each one formed by a *n/2* series connected power submodules plus an inductor or filter that can adopt several configurations [53]. Each submodule contains two insulated-gate bipolar transistors (IGBT), two reversing diodes and a DC energy storage capacitor. The DC side is modelled by two DC voltage sources (considered as constants in this study $V_{PO}=V_{ON}=V_{DC}/2$), while the AC side between terminals *M* and *O* is modelled by an AC voltage source (V_g), a resistor (R_{out}) and an inductor (L_{out}). Both arm inductors and the output one are taken to be linear and without internal resistance.

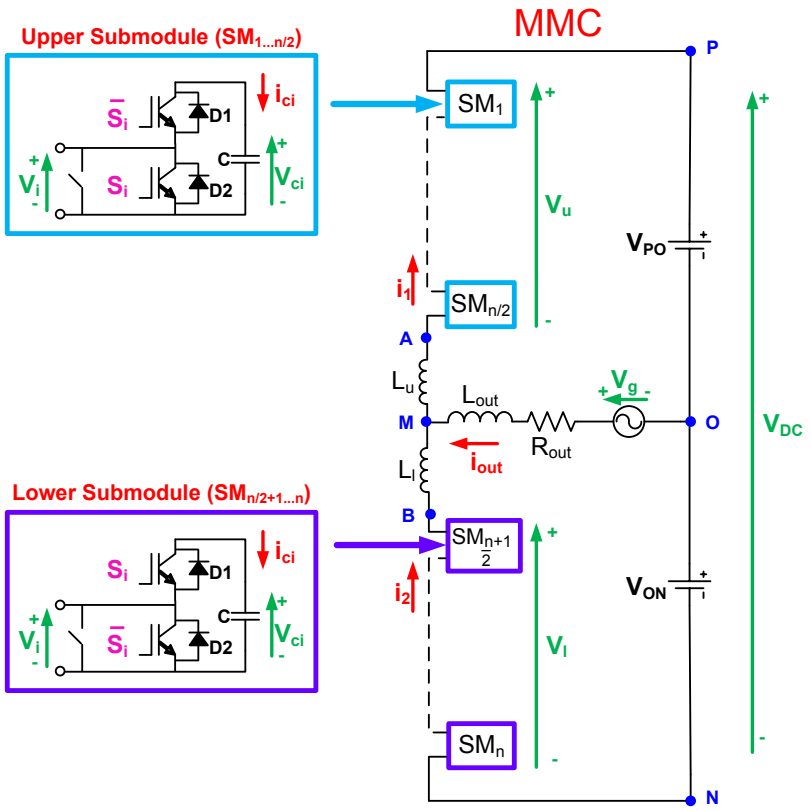


Fig. 2-2. Layout of the single phase MMC.

Once the layout of the converter is shown, the purpose of the following analysis is to work out the differential equations which describe the dynamic of the different variables of the converter: the voltage of every capacitor *(V_{ci})*, the two arms currents (i_1 and i_2) and the output current *(i_{out})*. These four variables will be a function of the steady ones or the conduction state of all the switches. Being the configuration of the upper and lower arm submodules identical, note that along the next discussion, their firing commands are considered opposite between them (see Fig. 2-2). The reason of this choice will be later explained but it should be taken into account on the whole system.

In normal operation, only one of the two semiconductors is on at a given time instant, that is why each submodule toggles between two states. In the upper arm submodules, on state *(S_i=1)* represents that the lower semiconductor is conducting but not the upper one, whereas off state *(S_i=0)* means that the upper semiconductor is conducting but not the lower one. Assuming that the capacitor voltage is V_{ci}, the output voltage V_i of each power submodule can take one of the two different voltage levels. When the submodule state is on, the voltage within submodule terminals is zero but when it is off the submodule is outputting V_{ci}. In order to make everything clear, in Table 2-1 the voltage at submodules terminals is exposed, as well as the current that circulates along the capacitor for both upper and lower arms and switching states.

Upper arm				
S_i	V_i	i_{ci}	$i_1>0$	$i_1<0$
0	V_{ci}	$-i_1$	$V_{ci}\downarrow$	$V_{ci}\uparrow$
1	0	0	$V_{ci}\approx$	$V_{ci}\approx$

Lower arm				
S_i	V_i	i_{ci}	$i_2>0$	$i_2<0$
0	0	0	$V_{ci}\approx$	$V_{ci}\approx$
1	V_{ci}	$-i_2$	$V_{ci}\downarrow$	$V_{ci}\uparrow$

Table 2-1. Switching states, voltage and currents of 2L submodules.

Therefore, it is possible to selectively and separately control each of the individual submodules in the converter to provide a voltage which is either V_{ci} or zero. Remembering that each converter arm is formed by a series connection of several submodules, the voltage obtained in the *n/2* upper submodules of the phase is the result of adding up the individual voltages and is called V_u (2-1). Likewise the voltage obtained in the *n/2* lower submodules of the phase is V_l (2-2). Notice that these two equations depend on the switching state of every submodule and thus their value will be varying continuously according to those switching states. This is the reason why in the simplified diagram of Fig. 2-3 upper and lower submodules have been replaced by some alternative voltage sources.

$$V_u = \sum_{i=1}^{n/2} V_{ci} \cdot (1 - S_i) \tag{2-1}$$

$$V_l = \sum_{i=n/2+1}^{n} V_{ci} \cdot S_i \tag{2-2}$$

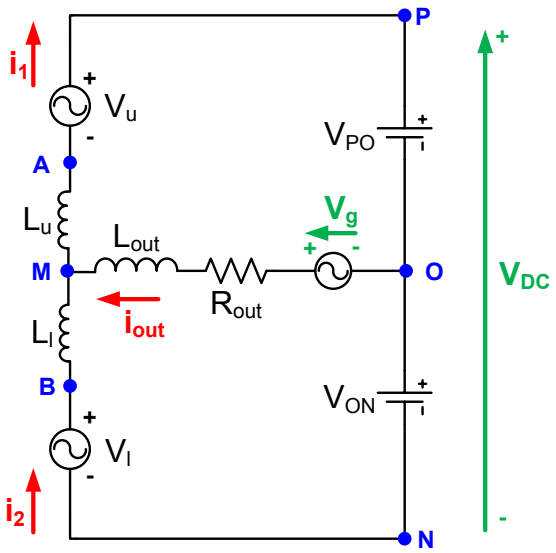


Fig. 2-3. Simplified diagram of the single phase MMC.

Looking at Fig. 2-3, the voltage between different points of the circuit which depends on the state of all submodules is calculated, where *n* refers to the total number of submodules per phase:

$$V_{AO} = V_{PO} - V_u = V_{PO} - \sum_{i=1}^{n/2} V_{ci} \cdot (1 - S_i) \tag{2-3}$$

$$V_{BO} = -V_{ON} + V_l = -V_{ON} + \sum_{i=n/2}^{n} V_{ci} \cdot S_i \tag{2-4}$$

Subtracting the previous equations the voltage V_{AB} is achieved:

$$V_{AB} = V_{AO} - V_{BO} = V_{PO} + V_{ON} - \sum_{i=1}^{n/2} V_{ci} \cdot (1 - S_i) - \sum_{i=n/2+1}^{n} V_{ci} \cdot S_i \tag{2-5}$$

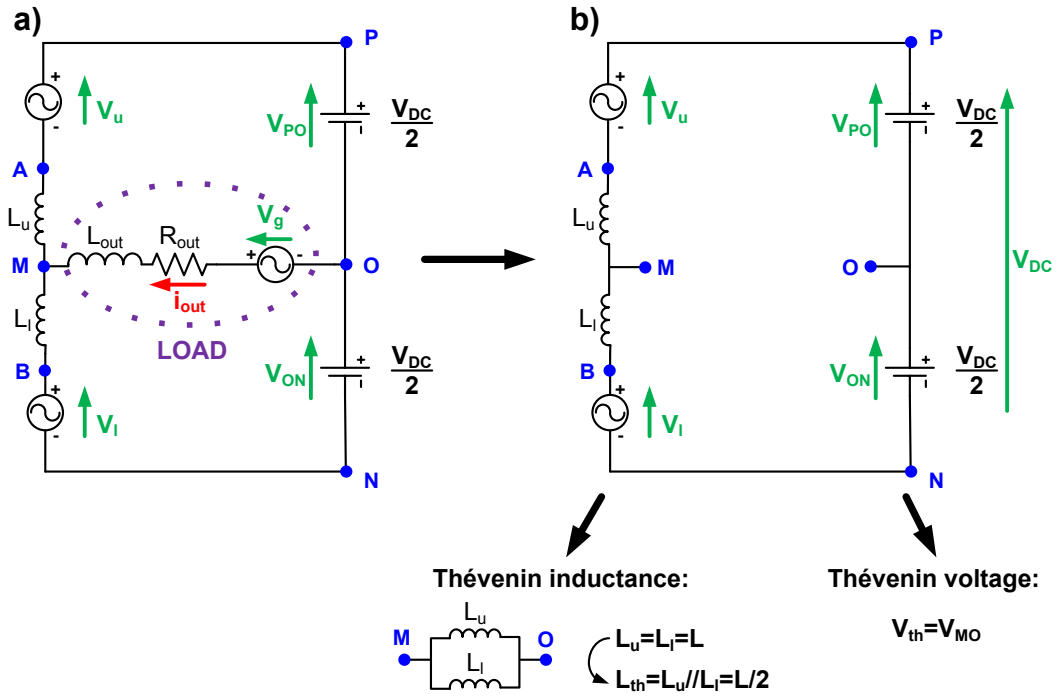


Fig. 2-4. a) Diagram of the simplified single phase MMC. b) Diagram of the simplified single phase MMC without the load.

A further simplification of the MMC circuit is necessary in order to continue with the modelling of the converter. For that, Thévenin's theorem is applied to the circuit of Fig. 2-3. As the theorem states, Thévenin's voltage V_{th} is the voltage between *M* and *O* which has to be calculated in open circuit condition (meaning infinite resistance) that is why the load is disconnected in Fig. 2-4a. So when $i_{out}=0$ and taking into account that the two arm inductors have the same value $(L_u = L_l = L)$, the voltage drop is equal in both components as expressed in equation (2-6):

$$V_{MA} = V_{BM} = -\frac{V_{AB}}{2} \tag{2-6}$$

Including this last equality in (2-7) besides the preceding three equations, Thévenin's voltage can be determined. After substituting several already known terms and reordering them, the expression (2-10) is obtained. Paying attention to (2-10) it can be deduced that if all the capacitors are well balanced, the first term of the equation should be approximately zero, the second one $-V_{DC}/2$ and the third one provides the $n+1$ voltage levels of the output signal being each level of $V_{ci}/2$ volts.

$$V_{th} = V_{MO} = V_{MA} + V_{AO} = -V_{BM} + V_{BO} = \frac{-V_{AB}}{2} + V_{AO} = \frac{V_{AB}}{2} + V_{BO} \tag{2-7}$$

$$V_{th} = \frac{V_{PO} - V_{ON}}{2} - \frac{V_u}{2} + \frac{V_l}{2} \tag{2-8}$$

$$V_{th} = \frac{V_{PO} - V_{ON}}{2} - \sum_{i=1}^{n/2} \frac{(V_{ci} \cdot (1 - S_i))}{2} + \sum_{i=n/2+1}^{n} \frac{(V_{ci} \cdot S_i)}{2} \tag{2-9}$$

$$V_{th} = \frac{V_{PO} - V_{ON}}{2} - \sum_{i=1}^{n/2} \frac{V_{ci}}{2} + \sum_{i=1}^{n} \frac{(V_{ci} \cdot S_i)}{2} \tag{2-10}$$

At the beginning of this chapter it has been pointed out that the firing commands of the upper and lower submodules are considered opposite between them (see Fig. 2-2). The explanation of this choice comes from (2-10). Notice that when all the firing commands of the phase are off *(Si=0)*, $V_{th} \approx -V_{DC}/2$. By contrast when all of them are on *(Si=1)*, $V_{th} \approx V_{DC}/2$. In addition, when half of them are on and the rest are off, $V_{th} \approx 0$ (see Fig. 2-5). Therefore this means that activating any of the firing commands (regardless the arm it belongs to) implies increasing a voltage level of V_{th}, meanwhile deactivating one implies decreasing a voltage level. This idea facilitates reasonably the implementation of the modulation besides resulting V_{th} a zero centred stepped signal.

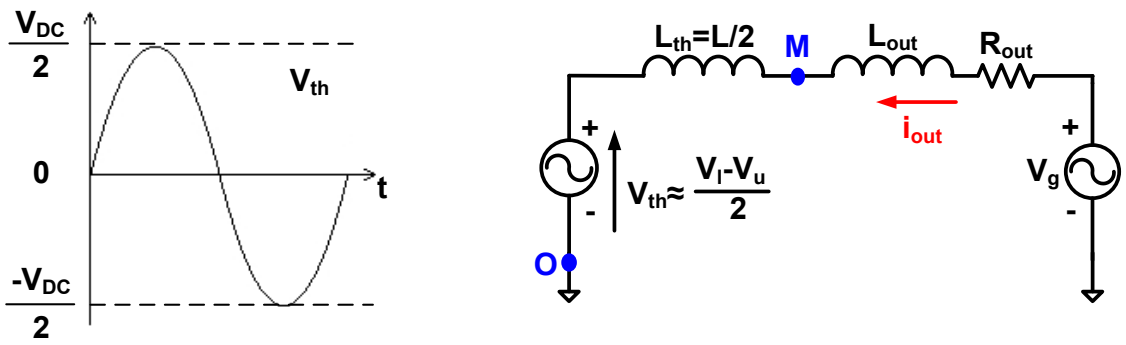


Fig. 2-5. Simplified MMC circuit applying Thévenin theorem.

On the other hand, Thévenin's equivalent inductance L_{th} is the one measured between points *M* and *O* considering the voltage sources as short circuits. In this case it is the parallel between the two arms inductances as depicted in Fig. 2-4b. Once both V_{th} and L_{th} are calculated, the whole converter's circuit can be substituted by a single voltage source and an inductance as appears in Fig. 2-5.

Then, by means of Kirchhoff's laws applied to the simplified circuit of Fig. 2-5 equations (2-11) and (2-12) are deduced.

$$V_{MO} = V_{th} + \frac{L}{2} \cdot \frac{di_{out}}{dt} \tag{2-11}$$

$$V_g - R_{out} \cdot i_{out} - L_{out} \cdot \frac{di_{out}}{dt} - \frac{L}{2} \cdot \frac{di_{out}}{dt} - V_{th} = 0 \tag{2-12}$$

Putting in order the expression (2-12), the differential equation which defines the dynamic of the output current is obtained:

$$\frac{di_{out}}{dt} = \left(\frac{1}{0.5 \cdot L + L_{out}} \right) \cdot \left(V_g - R_{out} \cdot i_{out} - V_{th} \right) \tag{2-13}$$

The expression which models the current circulating along the upper arm i_1 depends on the voltage at L_u inductor's terminals. It is achieved substituting (2-11) and (2-3) in (2-14). In the same way, the current along the lower arm i_2 is obtained, this time substituting (2-11) and (2-4) in (2-16).

$$\frac{di_1}{dt} = \frac{V_{MA}}{L_u} = \frac{V_{MO} - V_{AO}}{L_u} \tag{2-14}$$

$$\frac{di_1}{dt} = \frac{1}{L_u} \cdot \left(V_{th} + \frac{L}{2} \cdot \frac{di_{out}}{dt} - V_{PO} + \sum_{i=1}^{n/2} V_{ci} \cdot (1 - S_i) \right) \tag{2-15}$$

$$\frac{di_2}{dt} = \frac{V_{BM}}{L_l} = \frac{V_{BO} - V_{MO}}{L_l} \tag{2-16}$$

$$\frac{di_2}{dt} = \frac{1}{L_l} \cdot \left(-V_{th} - \frac{L}{2} \cdot \frac{di_{out}}{dt} - V_{ON} + \sum_{i=n/2}^{n} V_{ci} \cdot S_i \right) \tag{2-17}$$

Finally, the differential equations which define the voltage in the submodules capacitors are worked out. Owing to the opposite definition of the firing pulses for upper and

lower submodules, the obtained equations are different: (2-18) for the capacitors of the upper submodules and (2-19) for the lower ones.

$$\text{Upper:}\ \frac{dV_{ci}}{dt} = \frac{1}{C_i} \cdot i_1 \cdot (S_i - 1) \tag{2-18}$$

$$\text{Lower:}\ \frac{dV_{ci}}{dt} = \frac{1}{C_i} \cdot (-i_2 \cdot S_i) \tag{2-19}$$

Hence, from (2-13) to (2-19) the differential equations which define de dynamic of the Modular Multilevel Converter are achieved. In the following figure (Fig. 2-27), a summary of how these variables are accomplished is revealed, being all the submodules firing orders the inputs.

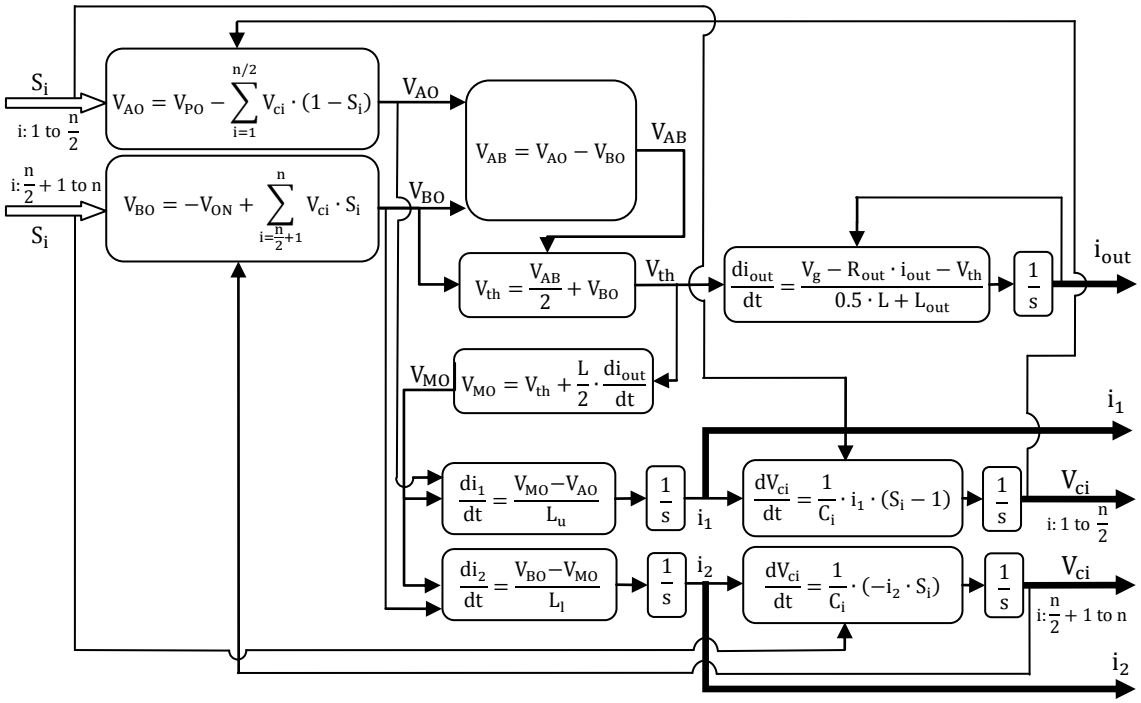


Fig. 2-6. Diagram of equations which defines the dynamic behaviour of the MMC.

2.1.2 Modulation

Any modulation technique which is employed in multilevel converters can be adapted to the MMC. In [66] modulation techniques for multilevel converters are grouped into three headings:

- Multilevel SHE (Selective Harmonic Elimination)
- Multilevel Carrier-Based PWM (Pulse Width Modulation)

- Multilevel SVM (Space Vector Modulation)

Several examples of these techniques applied to different multilevel inverters are exposed in [67]-[68]. Multilevel carrier-based PWM uses several triangular carrier signals, which can be modified in phase and/or vertical position in order to reduce the output voltage harmonic content. According to [69], the most commonly used modulation technique for cascaded multilevel inverters is the PSPWM (Phase Shifted Pulse Width Modulation) because it offers an evenly power distribution among cells and it is very easy to implement independently of the number of inverters. Fundamental concepts as well as variations of PWM appear in [70]. This modulation shifts the phase of each carrier in a proper angle to reduce the harmonic content of the output voltage. Therefore, this technique is the chosen one for the MMC modelled before.

The fundamental task of the firing control system is to generate the switching pulses for every n submodules of the converter phase by means of the chosen modulation technique and the two input references V_u* and V_l*. The fact of having modelled the two arms of the phase as two independent voltage sources is the reason why two reference signals have to be generated. In the simplified model of Fig. 2-3 can be seen that each arm is simplified as an alternative voltage source plus an inductor and both arms are in parallel connection. Then, in order to find out which is the desired voltage at both upper and lower submodules, a voltage reference per each arm is needed. This way, the external control system generates V_u* and V_l* and thanks to the applied modulation a voltage similar to the references is tried to be achieved by means of switching the submodules. Moreover, according to the operating of the MMC described in 2.1.1 these two references should be similar in amplitude but with a phase shift of 180º.

For the MMC with 2L submodules, in particular, a carrier signal per submodule is necessary, evenly interleaved with a phase shift of $360º/n$ between two consecutive carriers. As each arm is modelled separately, half of the carriers belong to the upper phase arm and the other half to the lower one being those carriers which belong to the same arm evenly shifted $(2 \cdot 360º)/n$. From the comparison between upper reference signal (V_u^*) and upper triangular carrier signals $(T_1..T_{n/2})$, the firing pulses for upper submodules are generated. On the other hand, lower submodules commutation orders are generated from the comparison between lower reference signal (V_l^*) and lower triangular carrier signals $(T_{n/2+1}..T_n)$.

Every time a reference signal crosses with a carrier signal which belongs to its same arm, its respective submodule must switch. In order to distinguish between a switching on and switching off, the value of those two signals is compared. In this point it has to be taken into account that switching orders for upper and lower submodules are taken oppositely. Thus, regarding the upper arm, the semiconductor is on meanwhile the reference is lower than the triangular and off when it is greater. However, as far as the lower arm is concerned, the contrary becomes the case as detailed in Table 2-2.

Upper arm (i=1..n/2)		Lower arm (i=n/2+1..n)	
S_i=1	V_u*<T_i	S_i=1	V_u*>T_i
S_i=0	V_u*>T_i	S_i=0	V_u*<T_i

Table 2-2. Switching states depending on the comparison between reference and carrier signals.

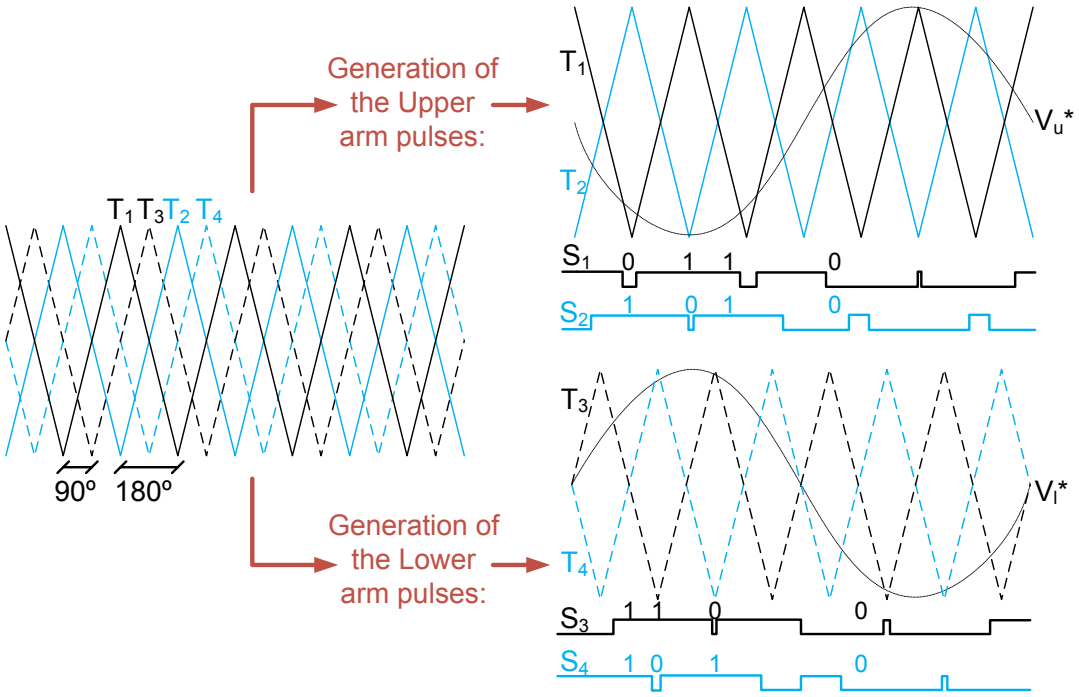


Fig. 2-7. Triangular and reference signals of a single phase 2L submodule MMC where *n=4*.

An example of the generation of commutation orders for a MMC with four submodules in the phase is drawn in Fig. 2-7 to clarify these theoretical explanations. In this case *n=4*, which implies the requirement of four triangular carriers. T_1 and T_2 are those which belong to the upper two submodules while T_3 and T_4 belong to the lower ones. It can be seen in Fig. 2-7 how between T_1 and T_2 there is a phase shift of 180º *((2·360º)/n)* as well as between T_3 and T_4. However, if two carriers from different arms are taken, T_1 and T_3 for instance, they are shifted 90º *(360º/n)*. Later, these signals are compared with V_u* and V_l* references to generate the firing pulses *(S_1..S_4)* in accordance with Table 2-2.

2.1.3 Simulation results

Next, some simulation figures which demonstrate what has been previously explained will be shown. All the graphics from Fig. 2-8, Fig. 2-10 and Fig. 2-12 have been taken from a single phase MMC simulation model whose DC voltage is fixed to 2 volts. The only two parameters which change are the number of submodules on the converter and the frequency of the triangular carriers. First the two references and the triangular signals are depicted. Then both upper and lower arms output voltage, V_u and V_l, are shown. Each one consists of *(n/2+1)* levels of V_i volts as expressed in (2-20). The last graphic represents the Thévenin voltage of one phase of the converter defined in (2-10). V_{th} is a staircase voltage waveform synthesized by combining the voltages of all the submodules of the phase and it is characterized by its *(n+1)* voltage levels of $V_i/2$ volts.

$$V_i = \frac{V_{DC}}{n/2} \tag{2-20}$$

Being f_{sw} the frequency of every triangular carrier signal, the frequency of the first harmonic band of the arm output voltage f_{1hb_arm} depends on the number of submodules per arm (2-21). The same happens with the f_{1hb} of V_{th} which is pushed to n times the carrier frequency as expressed in (2-22). This property can be checked in Fig. 2-9, Fig. 2-11 and Fig. 2-13 where the spectrum of the example in the left is shown. Choosing the waveforms from Fig. 2-8 as an example, multiplying $n=4$ by $f_{sw}=500\ Hz$ outcomes $f_{1hb}=2\ kHz$, exactly the frequency of the first harmonic band in Fig. 2-9. Moreover, the following harmonic bands appear every f_{1hb}.

$$f_{1hb\_arm} = \frac{n}{2} \cdot f_{sw} \tag{2-21}$$

$$f_{1hb} = n \cdot f_{sw} \tag{2-22}$$

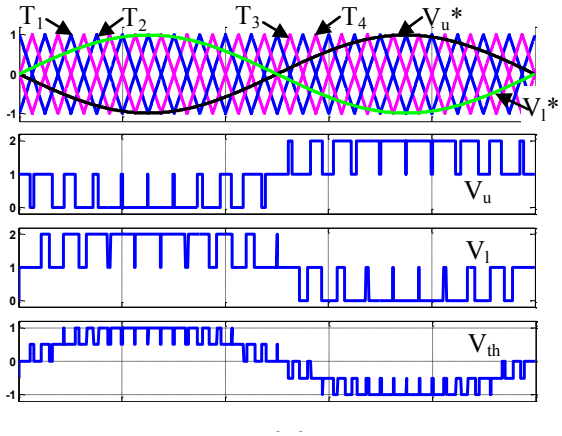


Fig. 2-8. Triangular and reference signals, V_u, V_l and V_{th} of a single phase 2L submodule MMC where $n=4$, $V_{DC}=2$ volts and $f_{sw}=500$ Hz.

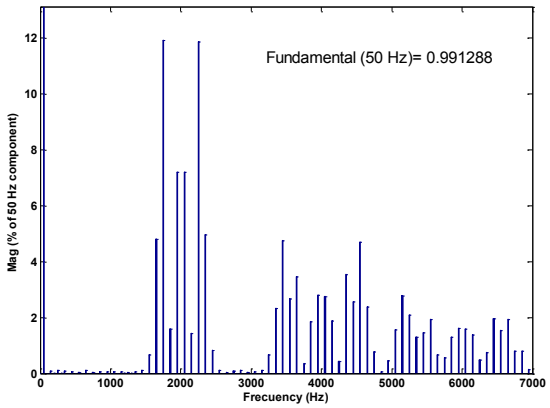


Fig. 2-9. Spectrum of V_{th} from a 2L submodule MMC where $n=4$ and $f_{sw}=500$ Hz.

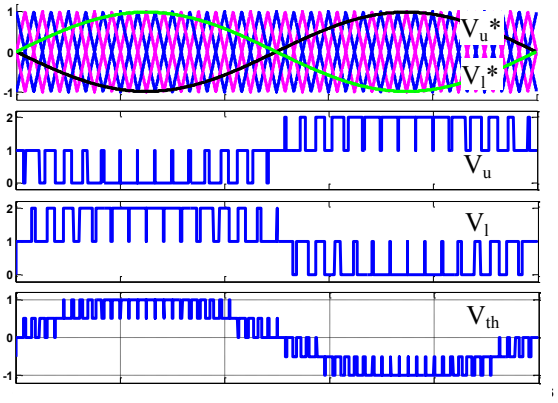


Fig. 2-10. Triangular and reference signals, V_u, V_l and V_{th} of a single phase 2L submodule MMC where $n=4$, $V_{DC}=2$ volts and $f_{sw}=750$ Hz.

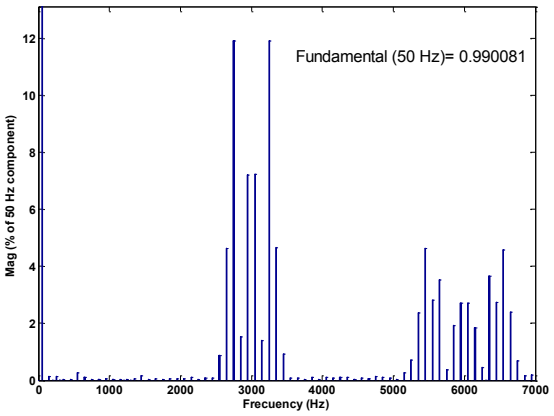


Fig. 2-11. Spectrum of V_{th} from a 2L submodule MMC where $n=4$ and $f_{sw}=750$ Hz.

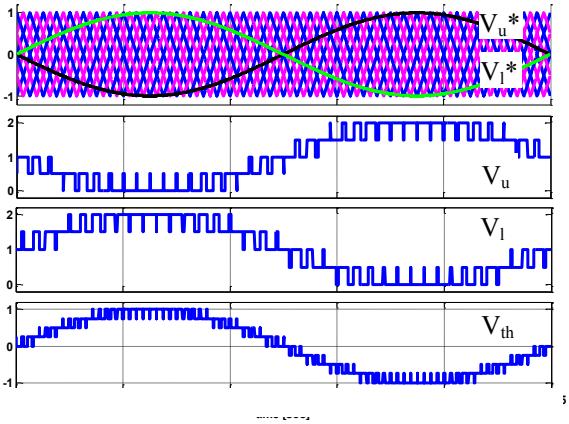


Fig. 2-12. Triangular and reference signals, V_u, V_l and V_{th} of a single phase 2L submodule MMC where $n=8$, $V_{DC}=2$ volts and $f_{sw}=500$ Hz.

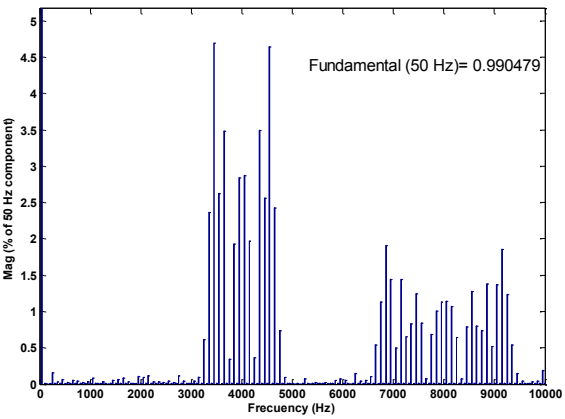


Fig. 2-13. Spectrum of V_{th} from a 2L submodule MMC where $n=8$ and $f_{sw}=500$ Hz.

2.2 MMC with 3L-FC submodules

2.2.1 Modelling

The Modular Multilevel Converter with 3L-FC submodules (Fig. 2-14) keeps the same converter modular concept than the MMC with 2L submodules but what does change is the topology of every submodule. In this case, each submodule comprises a classical 3L-FC converter structure formed by four controlled semiconductors, four reversing diodes and two capacitors. Regarding the electronic devices, one of these submodules is equivalent to two 2L submodules. However, as an advantage of the 3L-FC configuration, the capacity of the two capacitors is not the same, being one of them smaller $C_{1i}=2\cdot C_{2i}$.

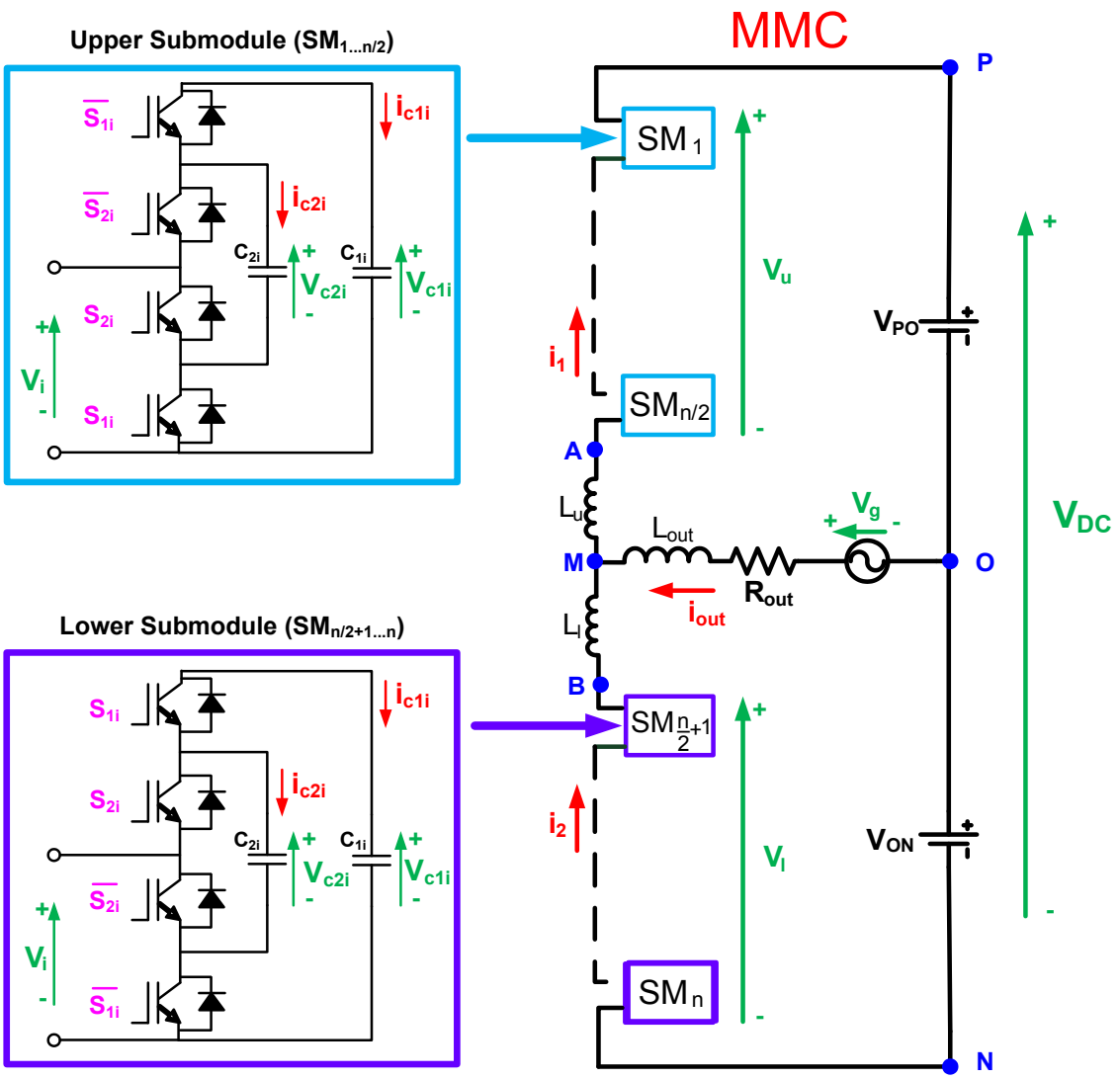


Fig. 2-14. Structure of the single phase MMC with 3L-FC submodules.

Upper arm						
S_{1i}	S_{2i}	V_i	i_{c1i}	i_{c2i}	$i_1>0$	$i_1<0$
0	0	V_{c1i}	$-i_1$	0	$V_{c1i}\downarrow, V_{c2i}\approx$	$V_{c1i}\uparrow, V_{c2i}\approx$
0	1	V_{c1i}-V_{c2i}	$-i_1$	i_1	$V_{c1i}\downarrow, V_{c2i}\uparrow$	$V_{c1i}\uparrow, V_{c2i}\downarrow$
1	0	V_{c2i}	0	$-i_1$	$V_{c1i}\approx, V_{c2i}\downarrow$	$V_{c1i}\approx, V_{c2i}\uparrow$
1	1	0	0	0	$V_{c1i}\approx, V_{c2i}\approx$	$V_{c1i}\approx, V_{c2i}\approx$
Lower arm						
S_{1i}	S_{2i}	V_i	i_{c1i}	i_{c2i}	$i_2>0$	$i_2<0$
0	0	0	0	0	$V_{c1i}\approx, V_{c2i}\approx$	$V_{c1i}\approx, V_{c2i}\approx$
0	1	V_{c2i}	0	$-i_2$	$V_{c1i}\approx, V_{c2i}\downarrow$	$V_{c1i}\approx, V_{c2i}\uparrow$
1	0	V_{c1i}-V_{c2i}	$-i_2$	i_2	$V_{c1i}\downarrow, V_{c2i}\uparrow$	$V_{c1i}\uparrow, V_{c2i}\downarrow$
1	1	V_{c1i}	$-i_2$	0	$V_{c1i}\downarrow, V_{c2i}\approx$	$V_{c1i}\uparrow, V_{c2i}\approx$

Table 2-3. Switching states, voltage and currents of 3L-FC submodules.

Again, upper and lower arm submodules are absolutely identical except for their firing commands which are considered opposite between them. Unlike the 2L submodules in which only two commutation combinations could occur, in this configuration there can be four switching states per submodule as detailed in Table 2-3. As a result, three voltage levels (see V_i column of Table 2-3) are achieved at its terminals as the submodule topology name suggests. Not only do the voltage levels differ from the former configuration but also the currents which flow through capacitors. So the next step is to obtain the equations which model this alternative converter. It should be taken into account that only those equations which have to do with the submodules voltages are modified because the converter structure remains unaltered.

First of all, the voltage between different points of the circuit of Fig. 2-14 which depends on the state of all submodules is calculated ((2-23), (2-24) and (2-25)) where n refers to the total number of submodules per phase.

$$V_{AO} = V_{PO} - V_u = V_{PO} - \sum_{i=1}^{n/2} V_{c1i} \cdot \overline{S_{1i}} + V_{c2i} \cdot \left(S_{1i} \cdot \overline{S_{2i}} - \overline{S_{1i}} \cdot S_{2i} \right) \tag{2-23}$$

$$V_{BO} = -V_{ON} + V_l = -V_{ON} + \sum_{i=n/2+1}^{n} V_{c1i} \cdot S_{1i} + V_{c2i} \cdot \left(\overline{S_{1i}} \cdot S_{2i} - S_{1i} \cdot \overline{S_{2i}} \right) \tag{2-24}$$

$$\begin{aligned} V_{AB} &= V_{AO} + V_{BO} = \\ &= V_{PO} + V_{ON} - \sum_{i=1}^{n/2} V_{c1i} \cdot \overline{S_{1i}} + V_{c2i} \cdot \left(S_{1i} \cdot \overline{S_{2i}} - \overline{S_{1i}} \cdot S_{2i} \right) - \sum_{i=n/2+1}^{n} V_{c1i} \cdot S_{1i} + V_{c2i} \cdot \left(\overline{S_{1i}} \cdot S_{2i} - S_{1i} \cdot \overline{S_{2i}} \right) \end{aligned} \tag{2-25}$$

Remember from the simplified diagram of Fig. 2-4 that Thévenin's voltage *(V_{th})* is the voltage between *M* and *O*. Then, it is given by the equation (2-26) which can be expanded on (2-27).

$$V_{th} = \frac{V_{PO} - V_{ON}}{2} - \frac{V_u}{2} + \frac{V_l}{2} \tag{2-26}$$

$$V_{th} = \frac{V_{PO} - V_{ON}}{2} - \sum_{i=1}^{n/2} \frac{V_{c1i} \cdot \overline{S_{1i}} + V_{c2i} \cdot \left(S_{1i} \cdot \overline{S_{2i}} - \overline{S_{1i}} \cdot S_{2i}\right)}{2} + \sum_{i=n/2+1}^{n} \frac{V_{c1i} \cdot S_{1i} + V_{c2i} \cdot \left(\overline{S_{1i}} \cdot S_{2i} - S_{1i} \cdot \overline{S_{2i}}\right)}{2} \tag{2-27}$$

Once V_{th} is calculated and keeping in mind that $L_{th}=L/2$, the whole converter circuit can be reduced to the one in Fig. 2-5. Applying Kirchhoff's laws to this circuit, the differential equation which defines the dynamic of i_{out} current is conformed (2-30). Note that the output current of the converter is a function of V_{th} calculated in (2-27).

$$V_{MO} = V_{th} + \frac{L}{2} \cdot \frac{di_{out}}{dt} \tag{2-28}$$

$$V_g - R_{out} \cdot i_{out} - L_{out} \cdot \frac{di_{out}}{dt} - \frac{L}{2} \cdot \frac{di_{out}}{dt} - V_{th} = 0 \tag{2-29}$$

$$\frac{di_{out}}{dt} = \left(\frac{1}{0.5 \cdot L + L_{out}}\right) \cdot \left(V_g - R_{out} \cdot i_{out} - V_{th}\right) \tag{2-30}$$

The expression which models the current circulating along the upper arm i_1 depends on the voltage at the inductor terminals. It is achieved substituting (2-28) and (2-23) in (2-31).The same way, the current along the lower arm i_2 is obtained, this time substituting (2-28) and (2-24) in (2-33).

$$\frac{di_1}{dt} = \frac{V_{MA}}{L_u} = \frac{V_{MO} - V_{AO}}{L_u} \tag{2-31}$$

$$\frac{di_1}{dt} = \frac{1}{L_u} \cdot \left(V_{th} + \frac{L}{2} \cdot \frac{di_{out}}{dt} - V_{PO} + \sum_{i=1}^{n/2} V_{c1i} \cdot \overline{S_{1i}} + V_{c2i} \cdot \left(S_{1i} \cdot \overline{S_{2i}} - \overline{S_{1i}} \cdot S_{2i}\right)\right) \tag{2-32}$$

$$\frac{di_2}{dt} = \frac{V_{BM}}{L_l} = \frac{V_{BO} - V_{MO}}{L_l} \tag{2-33}$$

$$\frac{di_2}{dt} = \frac{1}{L_1} \cdot \left(-V_{th} - \frac{L}{2} \cdot \frac{di_{out}}{dt} - V_{ON} + \sum_{i=n/2+1}^{n} V_{c1i} \cdot S_{1i} + V_{c2i} \cdot \left(\overline{S_{1i}} \cdot S_{2i} - S_{1i} \cdot \overline{S_{2i}} \right) \right) \quad (2\text{-}34)$$

In the 3L-FC topology 2 DC energy storage elements are needed, C_{1i} and C_{2i}, but due to their location on the circuit, their behaviour is defined by (2-35) and (2-36) respectively. As the firing pulses for upper and lower submodules are opposite (see Fig. 2-14), the equations which define the voltage in the two arm capacitors is also different, being (2-37) and (2-38) for the lower ones.

$$\text{Upper:} \frac{dV_{c1i}}{dt} = \frac{-1}{C_{1i}} \cdot i_1 \cdot \overline{S_{1i}} \quad (2\text{-}35)$$

$$\text{Upper:} \frac{dV_{c2i}}{dt} = \frac{-1}{C_{2i}} \cdot i_1 \cdot \left(S_{1i} \cdot \overline{S_{2i}} - \overline{S_{1i}} \cdot S_{2i} \right) \quad (2\text{-}36)$$

$$\text{Lower:} \frac{dV_{c1i}}{dt} = \frac{-1}{C_{1i}} \cdot i_2 \cdot S_{1i} \quad (2\text{-}37)$$

$$\text{Lower:} \frac{dV_{c2i}}{dt} = \frac{-1}{C_{2i}} \cdot i_2 \cdot \left(\overline{S_{1i}} \cdot S_{2i} - S_{1i} \cdot \overline{S_{2i}} \right) \quad (2\text{-}38)$$

2.2.2 Modulation

After the modelling equations of the MMC with 3L-FC submodules being explained, how the modulation is carried out will be described. The chosen modulation technique is the phase shifted PWM as in the MMC with 2L submodules. The difference lies in the number of switching states per submodule which has been increased in two. The way to get those four switching states per submodule is by means of two triangular signals as depicted in Fig. 2-15, one per semiconductor. So overall, $2 \cdot n$ triangular signals per phase are required altogether with a constant phase shift among them of $360°/(2 \cdot n)$. As occurred with the 2L configuration, half of the total triangular carrier signals belongs to the phase upper arm $(T_1 \ldots T_n)$ whereas the rest belong to the lower one $(T_n \ldots T_{2n})$. Obviously, there is a phase difference of $360°/n$ between two consecutive triangular signals which belong to the same arm (it is the same concept than the explained in Fig. 2-7).

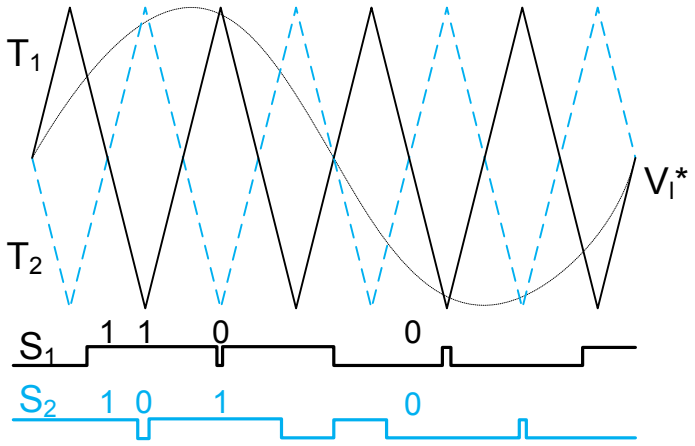


Fig. 2-15. Lower reference, triangular carriers and firing orders of a lower arm 3L-FC submodule.

Once again, two reference signals V_u* and V_l* are needed. These keep unaltered from the previous chapter. From the comparison between V_u* and $T_1..T_n$, the firing pulses for upper submodules are generated. On the other hand, lower submodules commutation orders are generated from the comparison between V_l* and $T_{n+1}..T_{2n}$. On and off switching states depend on the value of both the reference signal and the carriers as specified in Table 2-4.

Upper arm (i=1..n)		Lower arm (i=n+1..2n)	
S_i=1	V_u*<T_i	S_i=1	V_u*>T_i
S_i=0	V_u*>T_i	S_i=0	V_u*<T_i

Table 2-4. Switching states depending on the comparison between reference and carrier signals.

2.2.3 Simulation results

Next, some simulation figures will be shown to demonstrate what has been previously explained and at the same time to analyze the output waveform. The graphics from Fig. 2-16 have been taken from a two submodules single phase MMC normalized model whose DC voltage is fixed to 2 volts. First the two reference and the four triangular signals are depicted. Then both upper and lower arms output voltage, V_u and V_l, are shown. Each one consists of $(n+1)$ levels of V_i volts as expressed in (2-39). The last graphic represents the Thévenin voltage of one phase of the converter defined in (2-27), this is, the voltage between points M and O from Fig. 2-14. V_{th} is a staircase voltage waveform synthesized by combining the voltages of all the submodules of the phase and it is characterized by its $(2 \cdot n+1)$ voltage levels of $V_i/2$ volts (2-40).

$$V_i = \frac{V_{DC}}{n} \tag{2-39}$$

$$\text{Number of } V_{th} \text{ levels} = 2 \cdot n + 1 \tag{2-40}$$

If Fig. 2-8 and Fig. 2-16 are compared, no difference will be found even knowing that the topology of the submodule is not the same neither the number of total submodules of the converter. However, it is the best example to explain that one 3L-FC submodule is equivalent to two 2L submodules. In both cases the amount of total elements to build the converter is identical, the carrier signals are generated in an analogous way so as a consequence the arm voltages as well as the output voltage turns out to be equal.

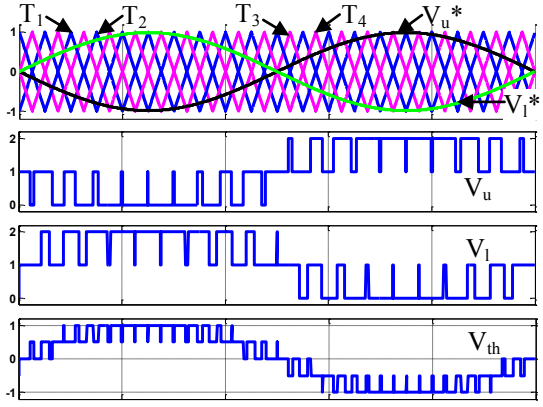


Fig. 2-16. Triangular and reference signals, V_u, V_l and V_{th} of a single phase 3L-FC submodule MMC where $n=2$, $V_{DC}=2$ volts and $f_{sw}=500$ Hz.

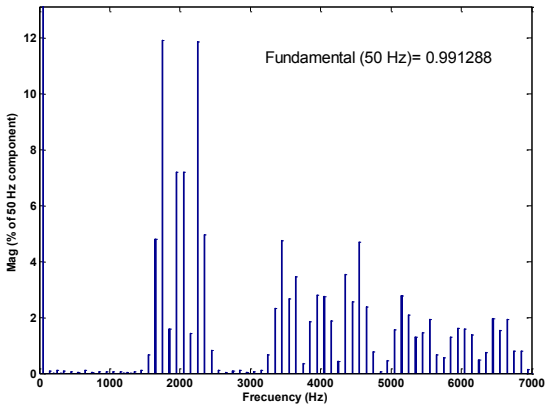


Fig. 2-17. Spectrum of V_{th} from a 3L-FC submodules MMC where $n=2$ and $f_{sw}=500$ Hz.

As far as the spectrum of the output signal is concerned, if V_{th} in both examples are identical, obviously the spectrum will be identical too. Being f_{sw} the frequency of every triangular carrier signal, the frequency of the first harmonic band of the arm output voltage f_{1hb_arm} depends on the number of submodules per arm (2-46). The same happens with the f_{1hb} of V_{th} which is pushed to $2 \cdot n$ times the carrier frequency as expressed in (2-42). This property can be checked in Fig. 2-17 where the spectrum of the example in the left is shown. Moreover, the following harmonic bands appear every f_{1hb}.

$$f_{1hb\_arm} = n \cdot f_{sw} \tag{2-41}$$

$$f_{1hb} = 2 \cdot n \cdot f_{sw} \tag{2-42}$$

2.3 MMC with 3L-NPC submodules

2.3.1 Modelling

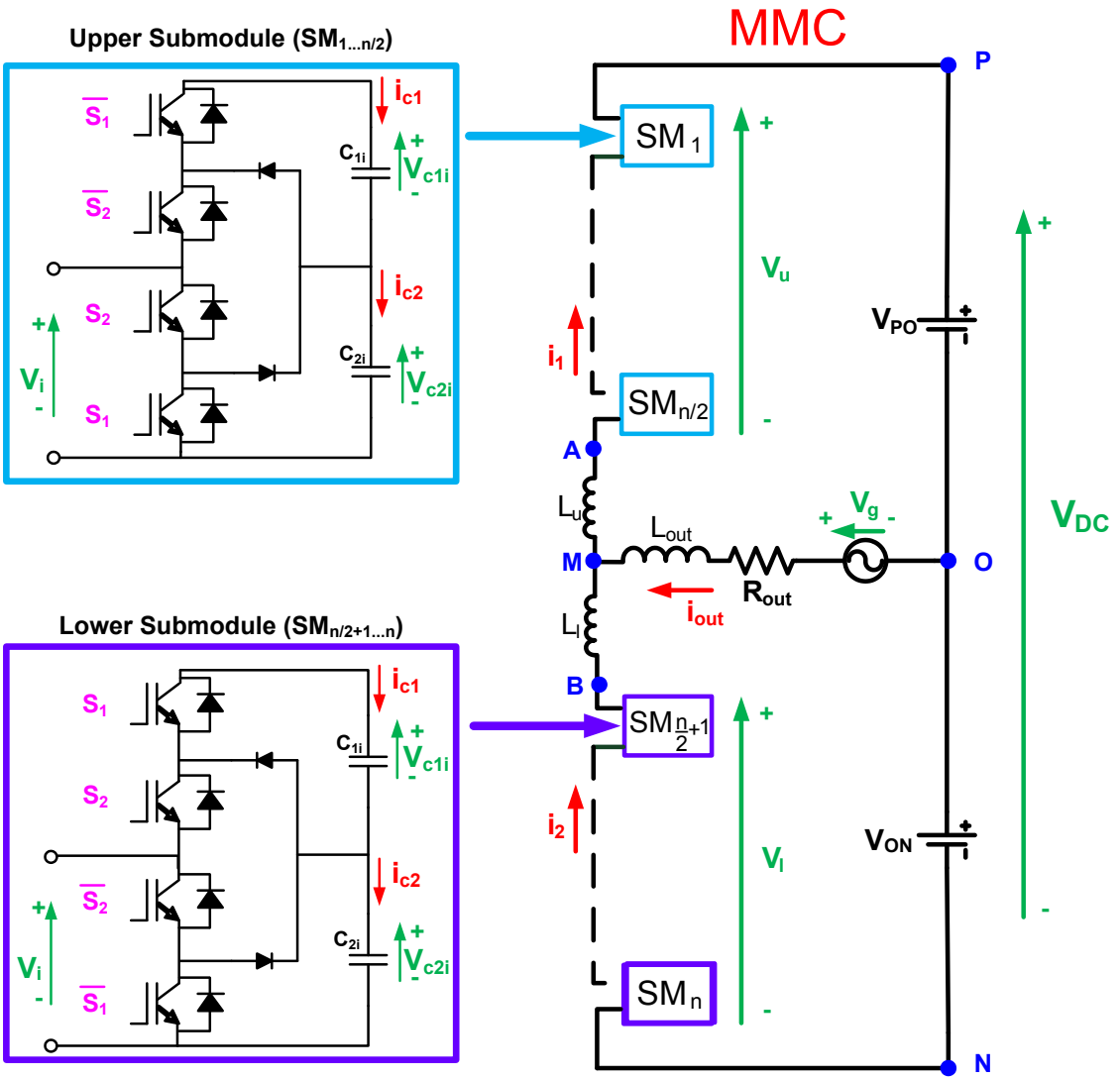


Fig. 2-18. Structure of the single phase MMC with 3L-NPC submodules.

The Modular Multilevel Converter with 3L-NPC submodules (Fig. 2-18) keeps the same converter modular concept than the MMC with 2L and 3L-FC submodules but what does change is the topology of every submodule. In this case, each submodule comprises a classical 3L-NPC converter structure formed by four controlled semiconductors, four reversing diodes, two freewheeling diodes and two capacitors. Unlike the 3L-FC configuration, these two capacitors are identical regarding the capacity and the operating voltage.

Upper arm						
S_{1i}	S_{2i}	V_i	i_{c1i}	i_{c2i}	$i_1>0$	$i_1<0$
0	0	$V_{c2i}+V_{c1i}$	$-i_1$	$-i_1$	$V_{c1i}\downarrow$, $V_{c2i}\downarrow$	$V_{c1i}\uparrow$, $V_{c2i}\uparrow$
0	1	-	-	-	-	-
1	0	V_{c2i}	0	$-i_1$	$V_{c1i}\approx$, $V_{c2i}\downarrow$	$V_{c1i}\approx$, $V_{c2i}\uparrow$
1	1	0	0	0	$V_{c1i}\approx$, $V_{c2i}\approx$	$V_{c1i}\approx$, $V_{c2i}\approx$
Lower arm						
S_{1i}	S_{2i}	V_i	i_{c1i}	i_{c2i}	$i_2>0$	$i_2<0$
0	0	0	0	0	$V_{c1i}\approx$, $V_{c2i}\approx$	$V_{c1i}\approx$, $V_{c2i}\approx$
0	1	V_{c2i}	0	$-i_2$	$V_{c1i}\approx$, $V_{c2i}\downarrow$	$V_{c1i}\approx$, $V_{c2i}\uparrow$
1	0	-	-	-	-	-
1	1	$V_{c2i}+V_{c1i}$	$-i_2$	$-i_2$	$V_{c1i}\downarrow$, $V_{c2i}\downarrow$	$V_{c1i}\uparrow$, $V_{c2i}\uparrow$

Table 2-5. Switching states, voltage and currents of 3L-NPC submodules.

Once more, upper and lower arm submodules are absolutely identical except for their firing commands which are considered opposite between them. Combining semiconductors states, the path followed by the current can be altered and as a consequence 3 voltage levels can be achieved at submodule terminals (0, V_{c1i} and $V_{c1i}+V_{c2i}$) depending on which capacitor passes through. In this case only 3 switching combinations for the semiconductors are allowed as detailed in Table 2-5.

The equations which model this converter are based on the data gathered in Table 2-5 besides the former general equations concerning the whole converter. So first, the voltage between different points of the circuit of Fig. 2-18 which depends on the state of all submodules is calculated ((2-43), (2-44) and (2-45)) where *n* refers to the total number of submodules per phase.

$$V_{AO} = V_{PO} - V_u = V_{PO} - \sum_{i=1}^{n/2} V_{c1i} \cdot \overline{S_{1i}} + V_{c2i} \cdot \overline{S_{2i}} \tag{2-43}$$

$$V_{BO} = -V_{ON} + V_l = -V_{ON} + \sum_{i=n/2+1}^{n} V_{c1i} \cdot S_{1i} + V_{c2i} \cdot S_{2i} \tag{2-44}$$

$$V_{AB} = V_{AO} - V_{BO} = V_{PO} + V_{ON} - \sum_{i=1}^{n/2} V_{c1i} \cdot \overline{S_{1i}} + V_{c2i} \cdot \overline{S_{2i}} - \sum_{i=n/2+1}^{n} V_{c1i} \cdot S_{1i} + V_{c2i} \cdot S_{2i} \tag{2-45}$$

Remember from the simplified diagram of Fig. 2-4 that Thévenin's voltage (V_{th}) is the voltage between *M* and *O*. Then, it is given by equation (2-46) which can be expanded on (2-47).

$$V_{th} = \frac{V_{PO} - V_{ON}}{2} - \frac{V_u}{2} + \frac{V_l}{2} \tag{2-46}$$

$$V_{th} = \frac{V_{PO} - V_{ON}}{2} - \sum_{i=1}^{n/2} \frac{V_{c1i} \cdot \overline{S_{1i}} + V_{c2i} \cdot \overline{S_{2i}}}{2} + \sum_{i=n/2+1}^{n} \frac{V_{c1i} \cdot S_{1i} + V_{c2i} \cdot S_{2i}}{2} \tag{2-47}$$

Once V_{th} is calculated and keeping in mind that $L_{th}=L/2$, the whole converter circuit can be reduced to the one in Fig. 2-5. Applying Kirchhoff's laws to this circuit, the differential equation which defines the dynamic of i_{out} current is conformed (2-50). Note that the output current of the converter is a function of V_{th} calculated in (2-47).

$$V_{MO} = V_{th} + \frac{L}{2} \cdot \frac{di_{out}}{dt} \tag{2-48}$$

$$V_g - R_{out} \cdot i_{out} - L_{out} \cdot \frac{di_{out}}{dt} - \frac{L}{2} \cdot \frac{di_{out}}{dt} - V_{th} = 0 \tag{2-49}$$

$$\frac{di_{out}}{dt} = \left(\frac{1}{0.5 \cdot L + L_{out}} \right) \cdot \left(V_g - R_{out} \cdot i_{out} - V_{th} \right) \tag{2-50}$$

The expression which models the current circulating along the upper arm i_1 depends on the voltage at the inductor terminals. It is achieved substituting (2-48) and (2-43) in (2-51).The same way, the current along the lower arm i_2 is obtained, this time substituting (2-48) and (2-44) in (2-53).

$$\frac{di_1}{dt} = \frac{V_{MA}}{L_u} = \frac{V_{MO} - V_{AO}}{L_u} \tag{2-51}$$

$$\frac{di_1}{dt} = \frac{1}{L_u} \cdot \left(V_{th} + \frac{L}{2} \cdot \frac{di_{out}}{dt} - V_{PO} + \sum_{i=1}^{n/2} V_{c1i} \cdot \overline{S_{1i}} + V_{c2i} \cdot \overline{S_{2i}} \right) \tag{2-52}$$

$$\frac{di_2}{dt} = \frac{V_{BM}}{L_l} = \frac{V_{BO} - V_{MO}}{L_l} \tag{2-53}$$

$$\frac{di_2}{dt} = \frac{1}{L_l} \cdot \left(-V_{th} - \frac{L}{2} \cdot \frac{di_{out}}{dt} - V_{ON} + \sum_{i=n/2+1}^{n} V_{c1i} \cdot S_{1i} + V_{c2i} \cdot S_{2i} \right) \tag{2-54}$$

In the 3L-NPC topology 2 DC energy storage elements are needed, C_{1i} and C_{2i}, but due to their location on the circuit, their behaviour is defined by (2-55) and (2-56) respectively. As the firing pulses for upper and lower submodules are opposite (see Fig.

2-18), the equations which define the voltage in the two arm capacitors is also different, being (2-57) and (2-58) for the lower ones.

$$\text{Upper:}\ \frac{dV_{c1i}}{dt} = \frac{-1}{C_{1i}} \cdot i_1 \cdot \overline{S_{1i}} \tag{2-55}$$

$$\text{Upper:}\ \frac{dV_{c2i}}{dt} = \frac{-1}{C_{2i}} \cdot i_1 \cdot \overline{S_{2i}} \tag{2-56}$$

$$\text{Lower:}\ \frac{dV_{c1i}}{dt} = \frac{-1}{C_{1i}} \cdot i_2 \cdot S_{1i} \tag{2-57}$$

$$\text{Lower:}\ \frac{dV_{c2i}}{dt} = \frac{-1}{C_{2i}} \cdot i_2 \cdot S_{2i} \tag{2-58}$$

2.3.2 Modulation

As far as the modulation is concerned, not any modulation technique can be used for the 3L-NPC topology because as revealed in Table 2-5 there are some forbidden states. Owing to the limitations inherent to this submodule topology the PSPWM applied to the previous submodule concepts is not fully useful in this one. However, a LSPWM (Level Shifted Pulse Width Modulation) technique (which is widely used in NPC inverters [69]) will be used in combination with the PSPWM. Using a LSPWM, the forbidden states in the 3L-NPC topologies can be avoided. An analysis regarding the harmonic content of this modulation technique can be found in [71]. There, it is explained that the phase displacement between two contiguous triangular carriers is free but there are three very simple dispositions that seem the most interesting:

- APO disposition: all the carriers are alternatively in opposition.
- PO disposition: all the carriers above the zero value reference are in phase among them but in opposition with those below.
- PH disposition: all the carriers are in phase.

For a 3L converter only two carriers are needed, that is why from the preceding dispositions, the phase displacement with APO or PO will be the same. Hence, in this analysis PH disposition is chosen because for a single phase model the harmonic content is minimized.

With the aim of avoiding one switching combination per submodule, two triangular signals and the reference are disposed as drawn in Fig. 2-19. According to the semiconductors arrangement of upper submodules, the unacceptable combination is: $S_{1i}=0$, $S_{2i}=1$ which means that the complementary S_{1i} and S_{2i} are conducting but S_{1i} and the complementary S_{2i} are not conducting (see Table 2-5). Then, the triangular signal at the top must be the one related to S_{1i} whereas the triangular signal at the bottom must be the one related to S_{2i}. This way, the crossings between the reference and T_1 or T_2 will never work out the state $S_{1i}=0$ and $S_{2i}=1$. On the other hand, the unacceptable combination for lower submodules is $S_{1i}=1$, $S_{2i}=0$ as can be checked in Fig. 2-19 and Table 2-5.

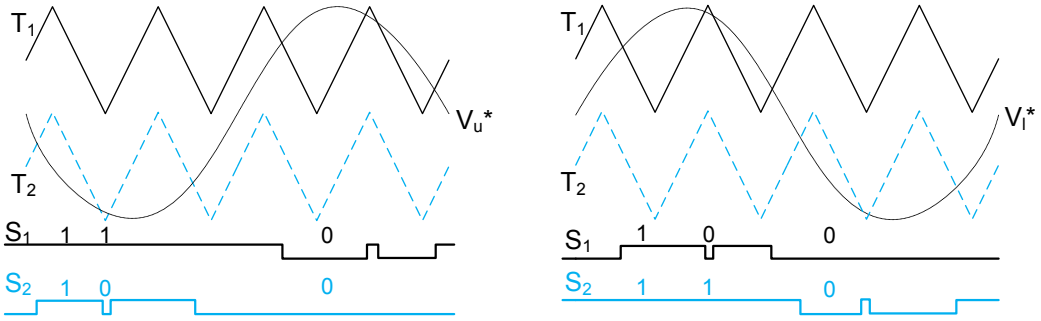


Fig. 2-19. Reference, triangular carriers and firing orders of an upper (drawing in the left) and lower (drawing in the right) arm 3L-NPC submodule.

Regarding the whole MMC with n 3L-NPC submodules per phase, n triangular signals are required altogether because as depicted in Fig. 2-19 the same triangular carriers $T_1 \ldots T_n$ are valid for generating upper and lower submodules firing pulses. In that picture can also be observed that the two triangular signals of the same submodule are in phase. However, phase-shift PWM concept is applied among triangular signals of different submodules. Two consecutive triangular carriers which belong to the same arm are evenly interleaved with a phase shift of $(2 \cdot 360º)/n$ (it is the same concept than the explained in Fig. 2-7).

Finally, from the comparison between V_u* and $T_1..T_n$, the firing pulses for upper submodules are generated. On the other hand, lower submodules commutation orders are generated from the comparison between V_l* and $T_1..T_n$. On and off switching states depend on the value of both the reference signal and the carriers as specified in Table 2-6.

Upper arm (i=1..n)		Lower arm (i=1..n)	
S_i=1	V_u*<T_i	S_i=1	V_l*>T_i
S_i=0	V_u*>T_i	S_i=0	V_l*<T_i

Table 2-6. Switching states depending on the comparison between reference and carrier signals.

2.3.3 Simulation results

Next, some simulation figures will be shown to demonstrate what has been previously explained and at the same time to analyze the output waveform. The graphics from Fig. 2-20 have been taken from a two submodules single phase MMC normalized model whose DC voltage is fixed to 2 volts. First the two references and the two triangular signals are depicted. Then both upper and lower arms output voltage, V_u and V_l, are shown. Each one consists of *(n+1)* levels of V_i volts as expressed in (2-59). The last graphic represents the Thévenin voltage of one phase of the converter defined in (2-47), this is, the voltage between points *M* and *O* from Fig. 2-18. V_{th} is a staircase voltage waveform synthesized by combining the voltages of all the submodules of the phase and it is characterized by its $(2 \cdot n+1)$ voltage levels of $V_i/2$ volts (2-60).

$$V_i = \frac{V_{DC}}{n} \tag{2-59}$$

$$\text{Number of } V_{th} \text{ levels} = 2 \cdot n + 1 \tag{2-60}$$

If Fig. 2-8 and Fig. 2-20 are compared, no difference will be found even knowing that the topology of the submodule is not the same neither the number of total submodules of the converter. The same happens with the 3L-FC submodules: one 3L-NPC submodule is equivalent to two 2L submodules. Regarding the analysis of the waveforms, in the three cases the amount of total elements to build the converter is identical, the carrier signals are generated in an analogous way so as a consequence the arm voltages as well as the output voltage turns out to be equal.

As far as the spectrum of the output signal is concerned, if V_{th} in both examples are identical, obviously the spectrum will be identical too. Being f_{sw} the frequency of every triangular carrier signal, the frequency of the first harmonic band of the arm output voltage f_{1hb_arm} depends on the number of submodules per arm (2-61). The same happens with the f_{1hb} of V_{th} which is pushed to *n* times the carrier frequency as expressed in (2-62). This property can be checked in Fig. 2-21 where the spectrum of the example in the left is shown. Moreover, the following harmonic bands appear every f_{1hb}.

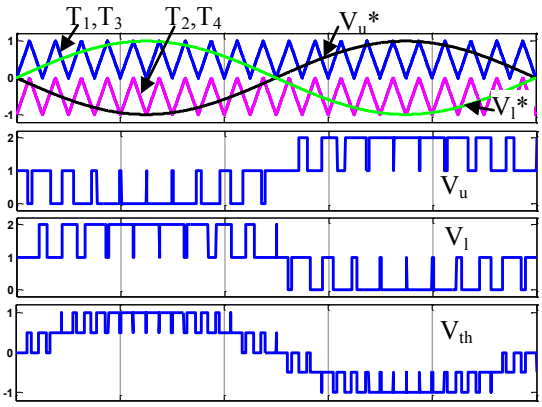


Fig. 2-20. Triangular and reference signals, V_u, V_l and V_{th} of a single phase 3L-NPC submodule MMC where $n=2$, $V_{DC}=2$ volts and $f_{sw}=1000$ Hz.

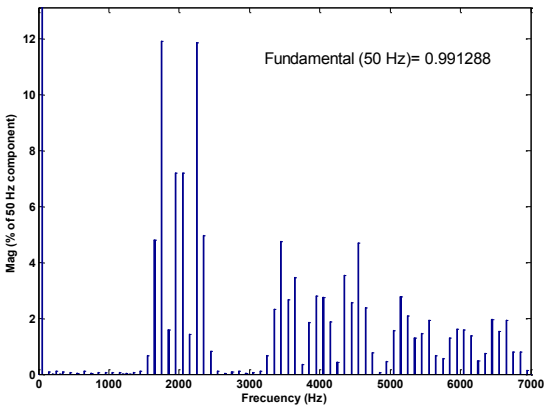


Fig. 2-21. Spectrum of V_{th} from a 3L-NPC submodules MMC where $n=2$ and $f_{sw}=1000$ Hz.

$$f_{1hb\_arm} = \frac{n}{2} \cdot f_{sw} \tag{2-61}$$

$$f_{1hb} = n \cdot f_{sw} \tag{2-62}$$

2.4 Sizing of the passive elements of the MMC

Throughout this chapter the operation of the converter as well as the components needed to comprise it are described. From all those elements, this section is focused on the sizing of the passive elements of the converter. First, how to calculate the capacity of the capacitors of all the submodules is explained. Then, both the arm and output inductances are estimated according to the maximum fixed ripple.

2.4.1 Sizing of the capacitors

2.4.1.1 Capacitors of the 2L submodules

The capacitor is one of the principal elements of each submodule, this is the reason why it should be well sized according to its application. The sizing methodology of the capacitors will be based on the power exchange of the single phase converter. For this analysis, notice that each converter arm has been substituted by an inductor plus an alternative voltage source v_1 or v_2 in the diagram of Fig. 2-22. These, in turn, are formed by an alternative voltage source and a constant value (for instance, in the upper arm $v_1=e_1+E_1$). As the alternative component of each phase arm is approximately the grid

voltage, e_1 is considered to get that same value. Moreover, assuming that both arms have the same average voltage, $E_1 \approx V_{PN}/2$.

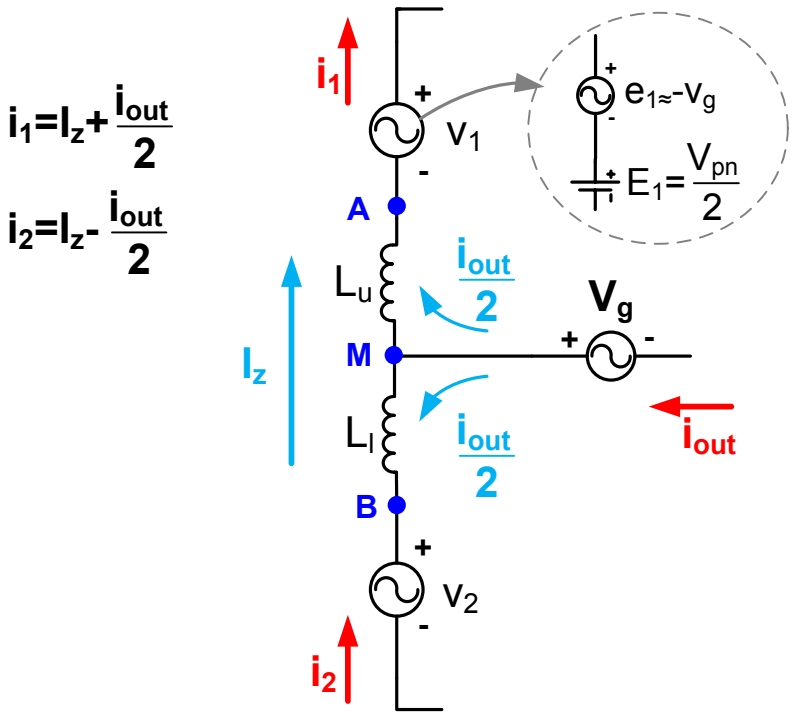


Fig. 2-22. Simplified diagram of the single phase MMC.

Regarding the arm i_1 and i_2 currents, they consist of a continuous current I_z plus the alternative one, $i_{out}/2$ (the output current is distributed equally between the two arms). So it can be deduced that the active power of a single phase MMC is (2-63) being V_g and I_{out} are the rms values of these variables and φ is the phase shift between them.

$$P = V_g \cdot I_{out} \cdot \cos(\varphi) \quad \text{or} \quad P = V_{PN} \cdot I_z \tag{2-63}$$

To get started, the dynamic equation of a capacitor is exposed in (2-64):

$$i_{ci} = C_i \cdot \frac{dv_{ci}}{dt} \tag{2-64}$$

It can also be expressed as a function of the instantaneous power in the capacitor $(p_{ci}(t))$:

$$\frac{p_{ci}(t)}{v_{ci}(t)} = C_i \cdot \frac{dv_{ci}}{dt} \tag{2-65}$$

But the dynamic equation of a submodule capacitor voltage can be also written as a function of the instantaneous power of a MMC phase *($p_{ph}(t)$)* being *n* the total number of submodules on the phase:

$$\frac{dv_{ci}}{dt} = \frac{p_{ci}(t)}{C_i \cdot v_{ci}(t)} = \frac{p_{ph}(t)}{C_i \cdot v_{ci}(t) \cdot n/2} \tag{2-66}$$

In order to obtain the expression of $v_{ci}(t)$ the differential equation shown in (2-66) must be solved. Assuming that the ripple of the capacitor voltage is negligible compared to the average capacitor voltage value *(V_{ci})*, this approximation is made to facilitate the solving of this differential equation: $v_{ci}(t) \approx V_{ci}$.

$$v_{ci}(t) = \frac{\int p_{ci}(t)dt}{C_i \cdot V_{ci}} = \frac{\int p_{ph}(t)dt}{C_i \cdot V_{ci} \cdot n/2} \tag{2-67}$$

To determine $v_{ci}(t)$ from (2-67) it is necessary to calculate the instantaneous power on the phase. Taking into account the voltages and currents on the phase detailed in Fig. 2-22, $p_{ph}(t)$ is:

$$p_{ph}(t) = E_1 \cdot I_z + E_1 \cdot \frac{i_{out}(t)}{2} + e_1(t) \cdot I_z + e_1(t) \cdot \frac{i_{out}(t)}{2} \tag{2-68}$$

Where:

$$E_1 \cdot I_z = \frac{V_{PN}}{2} \cdot \frac{P}{V_{PN}} = \frac{P}{2} \tag{2-69}$$

$$E_1 \cdot \frac{i_{out}(t)}{2} = \frac{V_{PN}}{2} \cdot \sqrt{2} \cdot \frac{I_{out}}{2} \cdot \cos(\omega \cdot t + \varphi) = \frac{V_{PN} \cdot I_{out}}{2 \cdot \sqrt{2}} \cdot \cos(\omega \cdot t + \varphi) \tag{2-70}$$

$$e_1(t) \cdot I_z \approx -\sqrt{2} \cdot V_g \cdot \cos(\omega \cdot t) \cdot \frac{P}{V_{PN}} = \frac{-\sqrt{2} \cdot P \cdot V_g}{V_{PN}} \cdot \cos(\omega \cdot t) \tag{2-71}$$

$$e_1(t) \cdot \frac{i_{out}(t)}{2} \approx -\sqrt{2} \cdot V_g \cdot \cos(\omega \cdot t) \cdot \sqrt{2} \cdot \frac{I_{out}}{2} \cdot \cos(\omega \cdot t + \varphi) = \frac{-V_g \cdot I_{out}}{2} \cdot \left(\cos(2 \cdot \omega \cdot t) + \cos(\varphi)\right) \tag{2-72}$$

Therefore, after integrating the expression of the phase power and substituting it in (2-67) results in the following:

$$v_{ci}(t) \approx \frac{\frac{P}{2}\cdot t + \frac{V_{PN}\cdot I_{out}}{2\cdot\omega\cdot\sqrt{2}}\cdot\sin(\omega\cdot t+\varphi) - \frac{\sqrt{2}\cdot P\cdot V_g}{V_{PN}\cdot\omega}\cdot\sin(\omega\cdot t) - \frac{V_g\cdot I_{out}}{2}\cdot\left(\frac{\sin(2\cdot\omega\cdot t)}{2\cdot\omega} + t\cdot\cos(\varphi)\right)}{C_i\cdot V_{ci}\cdot n/2} \quad (2\text{-}73)$$

In order to check the validity of equation (2-73) worked out with the aim of defining $v_{ci}(t)$, some simulations have been carried out. The converter used as example is a single phase MMC with 8 2L submodules whose most characteristic parameters are: $V_{gmax}=230V$, $I_{outmax}=36.8A$, $V_{PN}=500V$, $V_{ci}=125V$, $L_u=L_l=2mH$, $C_i=0{,}01F$. Fig. 2-23 is the result of substituting these parameters in equation (2-73) meanwhile Fig. 2-24 shows the submodules capacitors voltage taken from the simulation model described before. From the comparison of the two figures can be deduced that the shape of the ripple is very similar and that there is little difference in the amplitude. Therefore, it can be concluded that the equation which defines the dynamic of the capacitors voltage ($v_{ci}(t)$) worked out in this section of the report is acceptable.

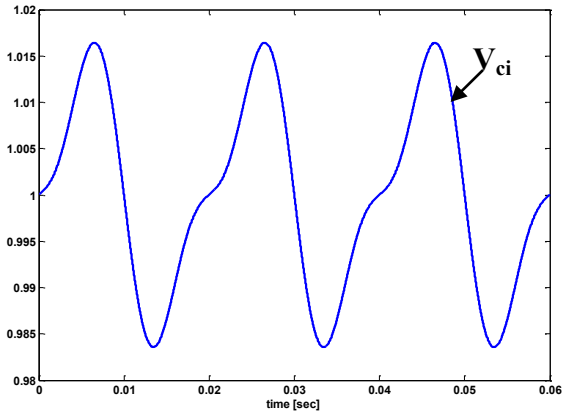


Fig. 2-23. Capacitors voltages (in p.u.) obtained from equation (2-73).

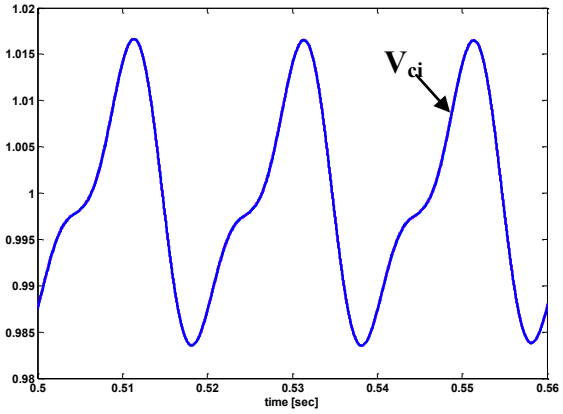


Fig. 2-24. Capacitors voltages (in p.u.) obtained from simulation.

However, this long expression can be greatly simplified. Assuming that the converter is working in a HVDC application in which there is not reactive power exchange with the grid, only active power is being transmitted. In this case, the phase shift between i_{out} and v_g is zero, thus $cos(\varphi)=1$. Moreover, if the converter is considered to be working at a unitary modulation index, $V_g = \frac{V_{PN}}{2\cdot\sqrt{2}}$. So applying this latter equality in (2-68), the expression of the instantaneous power on the phase is:

$$p_{ph}(t) = \frac{P}{2}\cdot\left(\cos(\omega\cdot t) - \cos(2\cdot\omega\cdot t)\right) \quad (2\text{-}74)$$

As done before, integrating $p_{ph}(t)$ and substituting it in (2-67) the obtained $v_{ci}(t)$ expression is considerably reduced if it is compared with (2-73):

$$v_{ci}(t) = \frac{P/2}{C_i \cdot V_{ci} \cdot \omega \cdot n/2} \cdot \left(\sin(\omega \cdot t) - \frac{\sin(2 \cdot \omega \cdot t)}{2} \right) + K \tag{2-75}$$

Once the temporal equation of the voltage in the submodules capacitors is already known, the ripple produced in them can be achieved by calculating the voltage difference between the maximum and minimum $v_{ci}(t)$. Fulfilling that purpose mathematically is as easy as solving the derivative of (2-75) set equal to zero. In this case, as the derivative of $v_{ci}(t)$ is the phase power, (2-76) has to be solved.

$$p_{ph}(t) = \frac{P}{2} \cdot \left(\cos(\omega \cdot t) - \cos(2 \cdot \omega \cdot t) \right) = 0 \tag{2-76}$$

(2-77) trigonometric identity is used to transform (2-76) in (2-78).

$$\cos(2 \cdot \omega \cdot t) = 2 \cdot \cos^2(\omega \cdot t) - 1 \tag{2-77}$$

$$-2 \cdot \cos^2(\omega \cdot t) + \cos(\omega \cdot t) + 1 = 0 \quad \begin{cases} t_1=0 \rightarrow \text{inflection point} \\ t_2=2/300 \rightarrow \max \\ t_3=4/300 \rightarrow \min \end{cases} \tag{2-78}$$

Three different solutions are obtained from the latter equation but t_1 does not match up with any maximum or minimum of the function because it corresponds to an inflection point. Therefore, entering the other two found solutions in (2-75) the ripple under the aforementioned conditions is achieved:

$$\Delta V_{ci} = v_{ci}(t_2) - v_{ci}(t_3) = \frac{3 \cdot \sqrt{3} \cdot P}{C_i \cdot V_{ci} \cdot \omega \cdot n \cdot 2} \tag{2-79}$$

Finally, defining ΔV_{cimax} as the maximum ripple allowed in the submodules capacitors, the capacity of these elements must be higher than:

$$C_i \geq \frac{3 \cdot \sqrt{3} \cdot P}{\Delta V_{cimax} \cdot V_{ci} \cdot \omega \cdot n \cdot 2} \tag{2-80}$$

It has to be remarked that this equation is a quite good approach for the approximations specified before: $ma=1$, $\cos(\varphi)=1$ and $V_g = \frac{V_{PN}}{2 \cdot \sqrt{2}}$. However, as long as these

parameters are further from the specified previous values, the calculated C_i from equation (2-80) is more inaccurate and the ripple will be higher than the one estimated in (2-79). In that case, it can be used to obtain an approximated capacity value but if a more exact value had to be determined, equation (2-73) should be employed instead which is demonstrated to be really precise.

2.4.1.2 Capacitors of the multilevel submodules

The previous methodology for the sizing of the submodules capacitor is based on the instantaneous power exchange. This instantaneous power given or absorbed by each of the submodules is independent of the topology used in these submodules. Regardless of the used topology (2L or multilevel) the equation (2-68) describes the instantaneous power delivered by the submodule. As described in the previous section, based on the equations (2-68) and (2-73) it is possible to correctly size the capacity of the 2L submodules capacitors, but these equations are not entirely valid for multilevel submodule topologies. The reason is that in the multilevel submodules there is more than one capacitor, so instantaneously it is possible to know how much power the submodule delivers, but it is very difficult to know which capacitor (or capacitors) is giving or absorbing this instantaneous power. The individual capacitor ripple depends on many factors such as the submodule topology, the employed modulation, etc.

Therefore, finding out the analytical expression of the individual capacitor ripple in multilevel submodules is a very complex task. So it is necessary to size the capacitors on the basis of their behavioural simulations and keep on adjusting the C_i value until their ripple meets the required specifications in these simulations. This is the procedure which has been followed to get the 3L-FC and 3L-NPC submodules capacitor values in the next chapters of this thesis.

2.4.2 Sizing of the inductances

The objective of this section as in the previous one is to obtain the most suitable value of the system inductances. The criteria adopted for the sizing of these elements is the maximum admissible ripple through the arm and output currents. For the following analysis, the single phase MMC with $n=4$ 2L submodules is taken as example.

As can be deduced in Fig. 2-1, V_{MA} and V_{BM} represent the voltage drop across L_u and L_l inductances respectively. So the general equations that model the current variation along L_u and L_l inductances are (2-81) and (2-82) respectively:

$$\Delta i_1 = \frac{V_{MA}}{L_u} \cdot \Delta t \tag{2-81}$$

$$\Delta i_2 = \frac{V_{BM}}{L_l} \cdot \Delta t \tag{2-82}$$

At the beginning of this chapter, the voltage drop across each inductance is defined in (2-6) being V_{AB} the voltage drop across the two of them expressed in (2-5). From those equations and bearing in mind the example where $n=4$, it can be deduced that in V_{MA} or V_{BM} three voltage levels can be achieved: 0 and $\pm V_{ci}/2$. Under these considerations, 4 triangular signals are needed for the typical PWM as depicted in Fig. 2-25 and described in chapter 2.1.2. It could be shown that the worst case for the current ripple is when the reference crosses two triangular carriers at the same instant as depicted in Fig. 2-25. In this particular case, the voltage applied at each inductance changes from $V_{ci}/2$ to $-V_{ci}/2$ or vice versa resulting a square signal with an amplitude of V_{ci} and a duty cycle of 0.5 as represented in Fig. 2-25. Although this is based on an example where $n=4$, it can be extended to any number of submodules in the converter. Then, the resulting V_{MA} or V_{BM} signal would acquire similar shape but its period would be $T_{pwm}/(n/2)$.

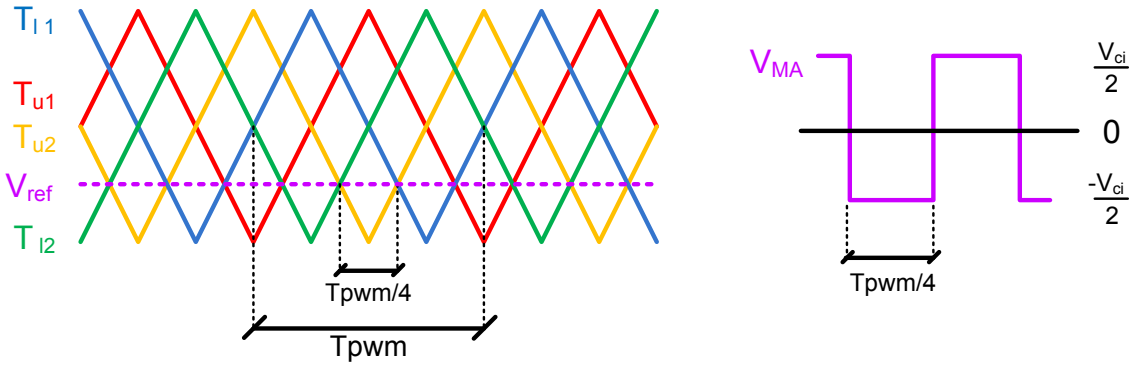


Fig. 2-25. Triangular signals for PWM generation as well as V_{MA} and V_{BM} voltage levels.

Then, the current variation through the phase inductances can be calculated as in (2-83) and (2-84) where n is the total number of the phase submodules.

$$\Delta i_1 = \frac{\frac{V_{ci}}{2} \cdot \frac{T_{pwm}}{n}}{L_u} \tag{2-83}$$

$$\Delta i_2 = \frac{\frac{V_{ci}}{2} \cdot \frac{T_{pwm}}{n}}{L_1} \tag{2-84}$$

Making use of the previous equations the two arm inductances can be dimensioned to fulfil the arm current ripple requirements.

The next step is to do the equivalent for the output current ripple. Going back to the Thévenin circuit (Fig. 2-4) it can be seen that not only is i_{out} current determined by L_{out} but also by L_u and L_l, that is, L_{th}. So as the value of L_u and L_l increases, the ripple in i_{out} also decreases. The general equation that models the output current ripple is (2-85):

$$\Delta i_{out} = \frac{V_{BA} \cdot \Delta t}{L_{th} + L_{out}} \tag{2-85}$$

As mentioned before, V_{BA} is a staircase voltage waveform whose voltage levels are $\pm V_{ci}/2$. It can be demonstrated that in this kind of signals, the maximum current ripple takes place for a duty cycle equal to 0.5. Δt depends on the number of triangular carriers needed for the PWM modulator. Then, the output current variation can be expressed as in (2-86).

$$\Delta i_{out} = \frac{\frac{V_{ci}}{2} \cdot 0.5 \cdot \frac{T_{pwm}}{n}}{L_{th} + L_{out}} \tag{2-86}$$

As the two arm inductances take part in (2-86) ($L_{th}=L_1$ in parallel with L_2), it could happen that only with these inductances calculated previously, the output current ripple requirements are fulfilled. In that case, an output filter L_{out} would be unnecessary.

Regarding the design considerations, it has been previously explained that a direct current is circulating through the two arms inductors. Accordingly, in order to avoid the magnetic core saturation, employing air core inductances would be a suitable solution.

2.4.3 Summary of passive elements

Once compared the voltages and currents from various simulations, it is known that while the value of L_u and L_l increases but decreases L_{out}, the ripple of arm currents as well as capacitors voltages minimizes. On the other hand, the time required for the system to reach the steady state increases considerably. In Table 2-7 the consequences of varying the value of some components is summarized.

Increasing	Consequence
L_u=L_l	The ripple in i_1 and i_2 decreases but also the ripple in i_{out} The transient time increases Higher energy at inductances → Higher price and volume Higher voltage drop between V_g and V_{th}
L_{out}	i_{out} ripple decreases → Smaller AC filter required Higher energy at inductance → Higher price and volume Higher voltage drop between V_g and V_{th}
C_i	V_{ci} ripple decreases Higher energy in the capacitors → Higher price and volume The output AC voltage is improved

Table 2-7: Consequences of increasing the value of inductances or capacitors.

2.5 Control of the voltage of the submodules

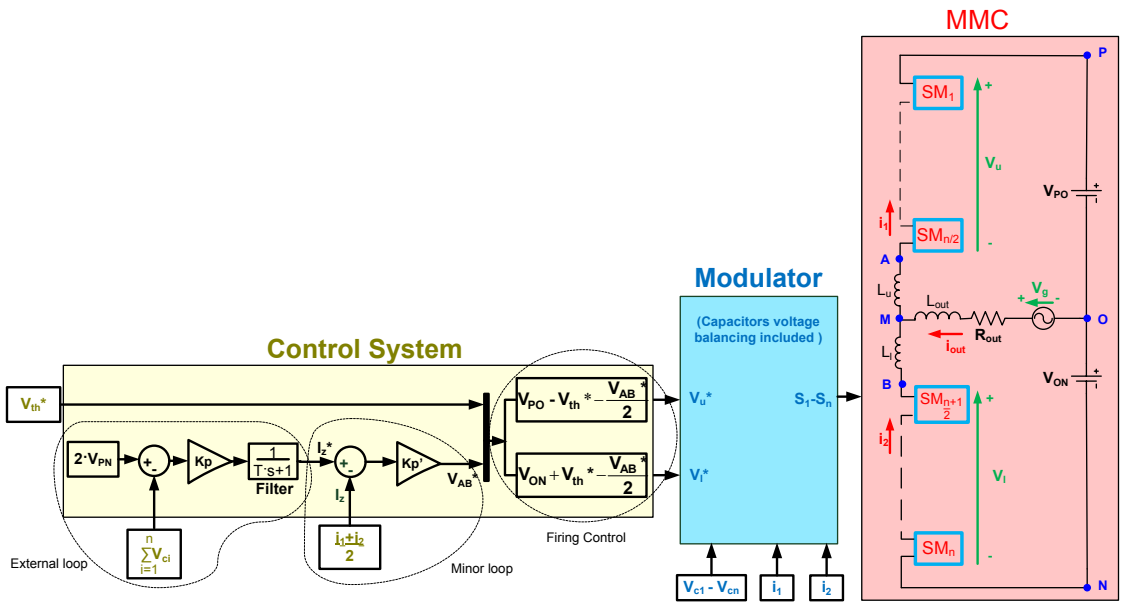


Fig. 2-26. Block diagram of the single phase Modular Multilevel Converter.

The main objective of a DC/AC converter is to obtain from continuous voltage sources a near sinusoidal stepped waveform at its output, in this case V_{th} (referred to the middle point of the DC bus side). In the MMC, to fulfil that purpose the switches of the submodules are operated so that the individual voltages from each submodule add up to form the multilevel waveform. It is crucial that every submodule voltage has the same value with the aim of attaining regular steps in V_{th}. This task is executed by the modulator but in addition to this, the total capacitors voltage has to be controlled to keep the DC bus at a constant value.

In this thesis, no possible control strategies or control dynamics for the converter are analysed. This part of the research is just based on the regulation of the average current through the phase I_z as done in [72] in order to control the total voltage of the capacitors as can be seen in the block diagram of Fig. 2-26.

2.5.1 Capacitors voltage control

V_{th} is a signal formed by so many levels of continuous voltages as the number of phase submodules plus one. So the more submodules there are the better is the output signal, that is, the more it will look like a sinusoidal wave avoiding the AC side filtering requirement.

$$\text{Number of } V_{th} \text{ levels} = n+1 \tag{2-87}$$

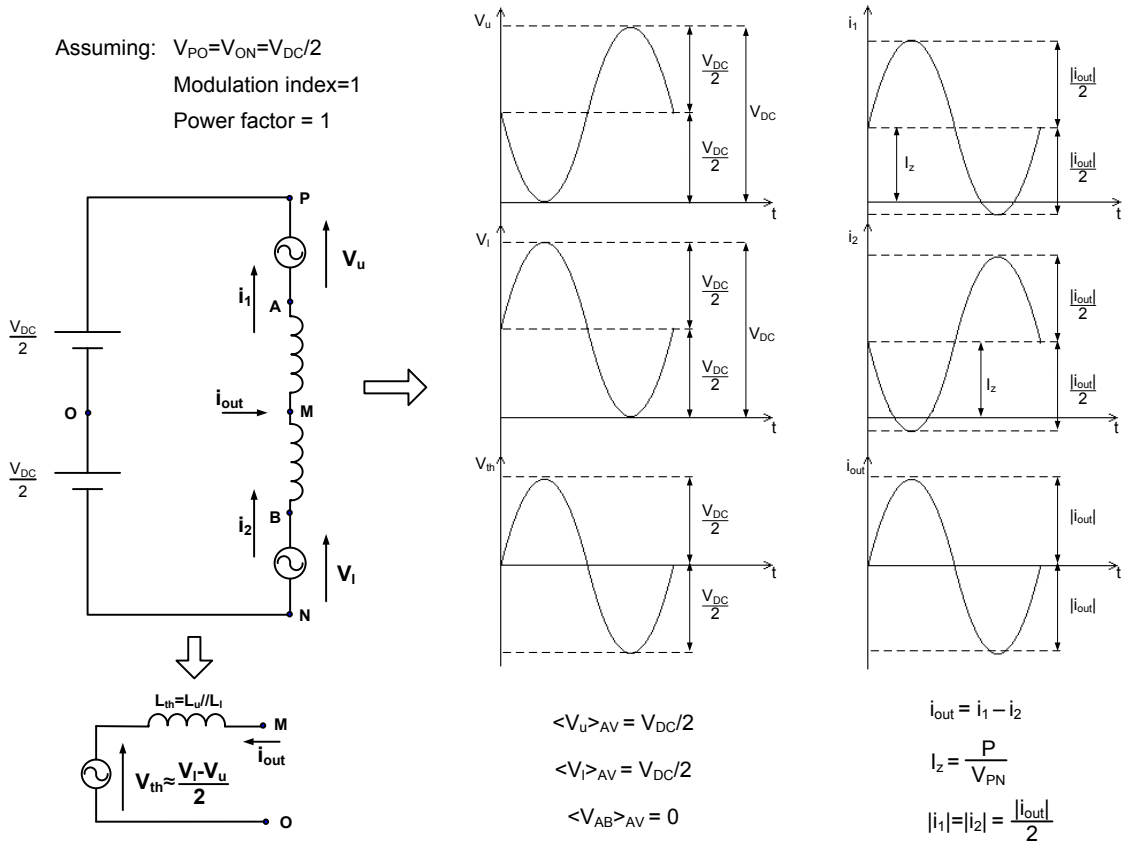


Fig. 2-27. Summary of the most relevant waveforms under ideal conditions.

Going back to equation (2-9) which defines the voltage V_{th}, it is deduced that the total sum of one arm capacitors voltage must be equal to V_{PN} in order to obtain symmetrical

voltages, that is, a sinusoidal wave without offset (see Fig. 2-27). This way, when all the submodules of the phase are off *($S_i=0$)*, $V_{th}= -V_{PN}/2$; in case half of the total submodules are on while the others are off, $V_{th}=0$; and when all the submodules of the phase are on *($S_i=1$)*, $V_{th}= V_{PN}/2$.

Therefore, when the whole system is active, to ensure a symmetrical output voltage it is essential to keep the sum of all the capacitors of the phase to twice the value of the DC voltage. This is the reason why the command of the external loop is $2 \cdot V_{PN}$. From this first control loop the reference of the average current through all the capacitors I_z is resulted.

2.5.2 Average current control

In accordance with the converter general circuit of Fig. 2-26, the currents fulfil the equation (2-88) – (2-90) where the average current through the phase I_z is defined as the half of the two arm currents sum as expressed in (2-91) [72].

$$i_1 = i_2 + i_{out} \tag{2-88}$$

$$i_1 = I_z + \frac{i_{out}}{2} \tag{2-89}$$

$$i_2 = I_z - \frac{i_{out}}{2} \tag{2-90}$$

$$I_z = \frac{i_1 + i_2}{2} \tag{2-91}$$

Fig. 2-26 shows the block diagram of the minor loop. The current command of I_z is the outcome of the external control loop and is given by equation (2-92). Controlling the difference between the current command and the measured average current (2-91) implies setting the voltage at the end of the inductances V_{AB} according to equation (2-93).

$$I_z^* = \left(2 \cdot V_{PN} - \sum_{i=1}^{n} V_{ci}\right) \cdot K_p \cdot \left(\frac{1}{T \cdot s + 1}\right) \tag{2-92}$$

$$\frac{di_z}{dt} = \frac{-V_{AB}}{L_u + L_l} \tag{2-93}$$

Once the command V_{AB}* from de current loop is calculated and the command of the output signal V_{th}* is fixed, it is feasible to get the upper and lower reference signal for the modulator with the purpose of calculating the switching pulses.

2.6 Unbalances of the submodule voltages

Until this point, the whole analysis of the converter has carried out considering ideal submodules in which all the electronic devices behave ideally and above all, the capacitors keep balanced at the same voltage level. However, in practice the features of electronic components are never identical and as a result there are always inequalities which can lead to unbalances in the capacitors. It has been found out that the capacitors voltage control together with the PWM modulation applied to the converter is not effective when disturbances turn up because the switching pattern is always the same.

It has been checked by means of several simulations using Matlab/Simulink that 2L submodules capacitors voltages tend to diverge when slight differences among submodules parameters appear. Proof of this is Fig. 2-28.

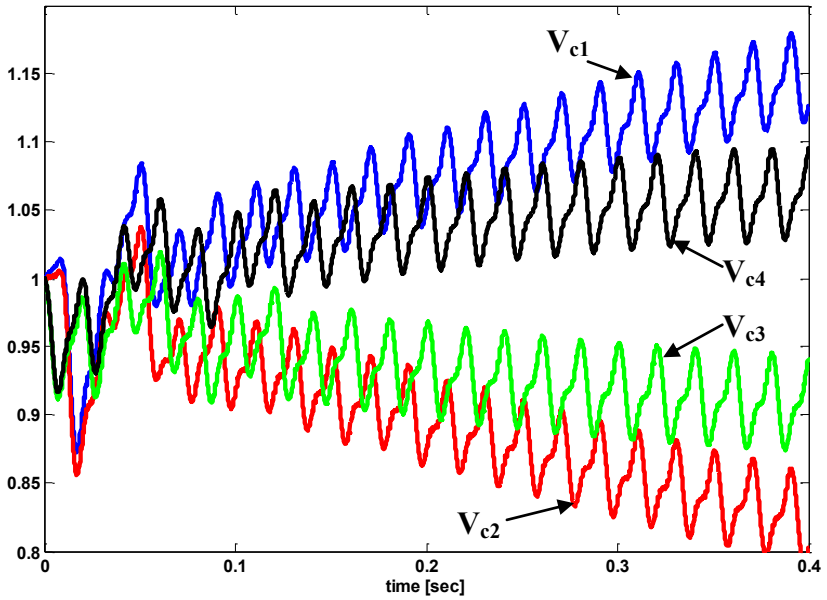


Fig. 2-28. Capacitor voltages of a single phase 2L submodule MMC being *n=4*.

As with the 2L submodules MMC, the 3L submodules does not bring any improvement with respect to the balancing of the submodules capacitors after applying the presented

modulation as is demonstrated in Fig. 2-29 and Fig. 2-30. Unless an adjustment in the modulation is adopted, a well-balanced will not be achieved.

Capacitors voltage balancing is one of the main objectives of the thesis. It is an issue that has to be treated because the consequence is a malfunctioning of the whole converter. It should not be forgotten that the multilevel output signal is formed adding up the DC voltage of these capacitors, so if their voltages are unbalanced the DC levels will be different. Therefore it is essential to cope with this problem in next chapters.

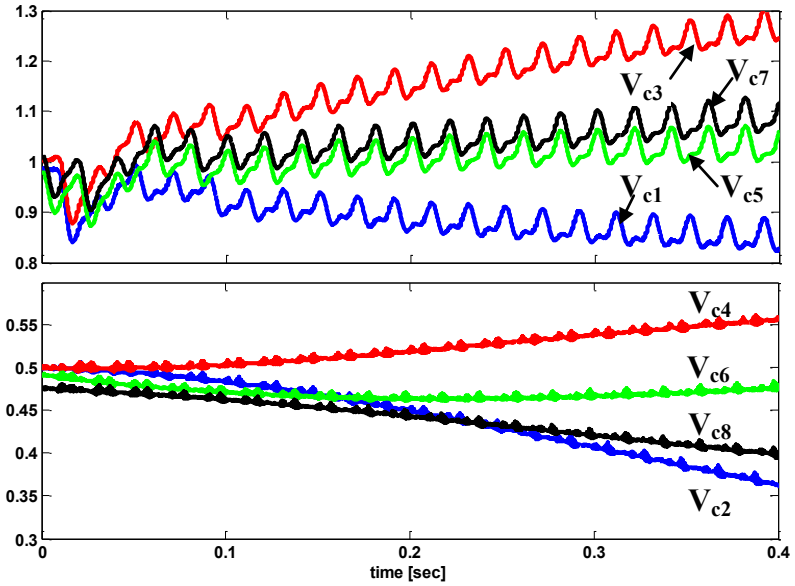


Fig. 2-29. Capacitor voltages of a single phase MMC with 3L-FC submodules being *n=4*.

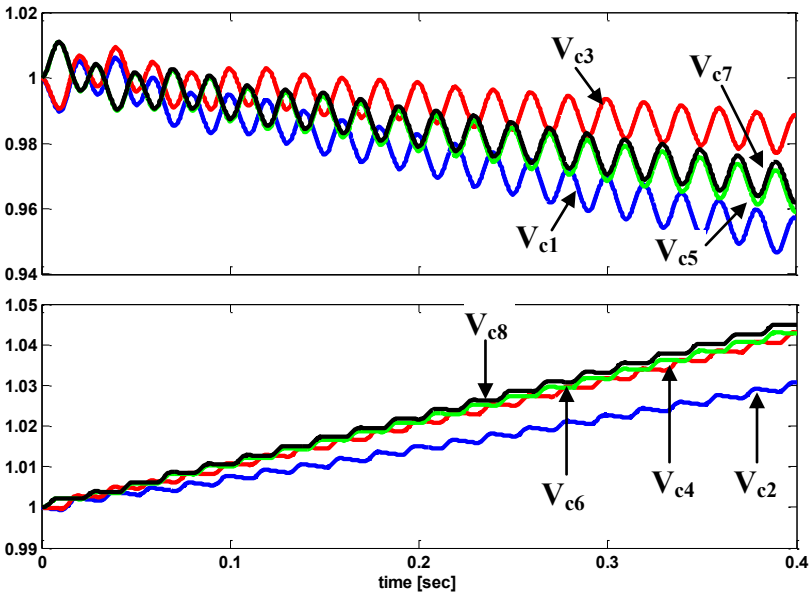


Fig. 2-30. Capacitor voltages of a single phase MMC with 3L-NPC submodules being *n=4*.

2.7 Conclusions

In chapter 2, the *n* submodules single phase Modular Multilevel Converter layout is described and its behaviour is deeply explained by means of differential equations. Apart from two level half bridge submodules, multilevel topology submodules can be also used with the intention of increasing each submodule voltage which is, in the 2L submodules, imposed by the chosen semiconductor.

The modelling of the converter does not have to do with the topology of the submodules. However, there are some differences in the way of obtaining the firing orders for the switches. Therefore, how the modulation should be implemented according to the three selected submodule topologies is explained: 2L, 3L-FC and 3L-NPC. Moreover, some simulation results are displayed by means of which the output signal in the three cases can be analysed.

A sizing methodology for the passive elements of the MMC is expounded. In the case of the capacitors, the expression obtained to size their capacity is valid for the 2L submodules but not for the rest because when there is more than a capacitor per submodule, their individual ripple depends on several factors. Thus, in the coming chapters the C_i estimation for the multilevel submodules will be determined by simulations results.

This thesis does not go into the analysis of feasible control strategies for the converter or any specific control loop optimization, simply the total capacitors voltage is controlled in order to keep the total DC bus constant. Despite implementing the mentioned control, it has been demonstrated that the proposed modulation is not useful for models with little disturbances for the reason that the capacitors are likely to diverge. So once the problem is identified a solution for the balancing of the capacitors will hereinafter be exposed.

Chapter 3

Modulation algorithm with capacitors voltage balancing valid for multilevel submodules

It has been demonstrated in chapter 2 that this converter unavoidably requires a voltage balancing control of all the capacitors of the submodules comprising the converter. In publications such as [49], [73]-[81], several capacitors voltage balancing methods have been treated with a MMC topology with 2L submodule concepts. Most of the mentioned balancing philosophies are based on a PWM modulation, selecting the submodule that must switch at any time, depending on the capacitors voltage and arm currents of the converter. These philosophies lead to an extra computational cost requirement, since all capacitors voltages must be measured, then the one that switches according to a given criteria must be selected, etc...

Hence, in [73]-[74], a specific procedure for generating the voltage references of the two voltage sinusoidal references for each arm is proposed, together with its corresponding balancing method based on PWM. This method is especially suitable for operating in STATCOM application. With a slightly different philosophy, in [58], [75], the balancing and modulation method requires a division of the sinusoidal voltage references in n (number of submodules) levels, ensuring that only one submodule will switch at each level. On the other hand, in [76] for instance, phase disposition levels shifted carriers are used for the modulation method, while the voltage balancing of the capacitors is carried out by choosing the appropriate redundant voltage vector. By contrast, in [72],[77]-[78], two external closed loops are incorporated to ensure the balancing of the capacitors: first an averaging control loop guarantees the appropriate circulating current, while secondly, a balancing control loop actuates on the voltage

sinusoidal references, ensuring the balancing. In a similar philosophy, [79] also includes additional closed control loops to perform the balancing. Finally, [81] compares different modulation and control methods for MMC.

It must be pointed out that for instance in [49], in a different approach compared to previous cases, a space vector modulation based balancing method is employed in a low number of submodules MMC. Thus, in this case, common mode voltages of the MMC are used as degrees of freedom for balancing the capacitors. In an attempt to reduce the complexity of the implementation, [82] explores the possibility of controlling the converter in open loop by estimating the stored energy in the arms and thereby avoiding the necessity of using a large number of measured voltages. Finally, [83] studies the voltage balancing limits in MMCs.

However, no publication has been presented dealing with the voltage balancing problem being the MMC constructed by multilevel submodules concepts, such as the well known NPC, FC or NPP topologies (note that from the capacitors voltage balancing point of view, 3L-NPC and 3L-NPP topologies are equivalent). Thus, this chapter presents an effective and versatile solution for the voltage balancing of the capacitors originally proposed in [80], based solely on the appropriate PWM modulation strategy and now extended to different “classic” and innovative multilevel submodule concepts. It can be easily implemented in standard hardware boards, not being difficult to adapt the implementation program to arrangements with a different number of submodules.

Therefore in this chapter a modulation method to face the encountered problem is proposed. It is firstly described and applied to 2L submodules. After testing its proper performance illustrating the most characteristic variables, it is applied to 3L submodules. As the balancing of the capacitors cannot be assured for all the working conditions in the 3L-NPC submodules, some extra changes are included in the modulation.

Finally, additional simulation results are shown to prove the right operation of the converter at low switching frequencies and high number of submodules.

3.1 Description of the Modulation Algorithm applied to 2L submodules

Meanwhile the voltage control system maintains the total voltage of capacitors constant to twice the DC bus value, a crucial requisite of the modulator is to uphold all the submodules capacitors at the same voltage level. Despite being their total amount correct, in case the capacitors are unbalanced, the result is a distorted output voltage. It has been verified in chapter 2 that a PWM technique is not enough to fulfil both tasks: generate the right semiconductors firing pulses to achieve a multilevel output signal meanwhile the capacitors are getting charged and discharged in a balanced manner. However, it has been deduced that just modifying the semiconductors switching sequence those duties could be completed. This is briefly the clue of the following modulation. So it has to be remarked that in this thesis none modulation technique is developed, but anyone valid for multilevel converters can be chosen and then slightly modified to achieve the balancing of the capacitors. To sum up, instead of following an even switching pattern, the modulator algorithm chooses which submodule has to be activated or deactivated according to the capacitors voltages when the modulation technique detects that a submodule state has to be toggled.

The modulation method proposed in this chapter consists on a multilevel carrier PWM based on [85]. In a standard PWM technique, each triangular carrier signal is linked to a specific semiconductor in such a way that, the firing pulses of each semiconductor are generated when both reference and its correlated triangular signal intersect. This means that all the semiconductors toggle according to a regular repetitive sequence. So the main difference of the modulation algorithm developed here is that none of the triangular carrier signals are directly linked with any semiconductor. They are just grouped by phase arms, so the principle lies in deciding which of the arm semiconductor should toggle when a voltage reference signal and a triangular intersect, according to the submodule capacitor voltage. Consequently, apart from obtaining a multilevel signal in the output voltage of the converter, it is possible to achieve the balance of the capacitor voltages.

Despite there being no interaction among the generation of the switching pulses for the 2 arms of the phase, the procedure followed is almost the same as can be seen in the summary of Fig. 3-1. Every time a reference signal crosses with any of the triangular signal which belong to its same arm, any of the arm submodules must switch. The first

task the modulator does is to put in order from the lowest to the highest all the arm submodules capacitors according to their voltages. Then, in order to distinguish between a switching on and switching off, it compares the value of the carrier signal with the reference. As can be observed in the diagram of Fig. 3-1 and also in the Table 2-2, if the upper reference value is larger than the triangular carrier, a submodule must be switched off. In case it is smaller, a submodule must be switched on. The contrary should occur with the lower arm.

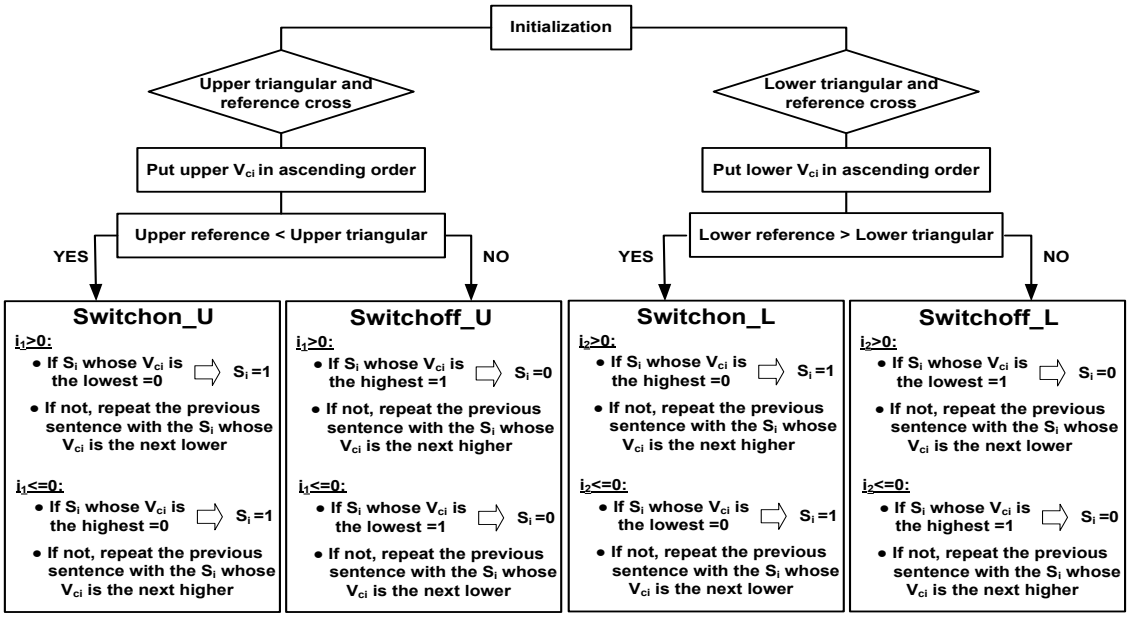


Fig. 3-1. Diagram of the modulation algorithm.

Whenever the arm current i_1 or i_2 is positive (see the current direction chosen in Fig. 5-1), the voltage level of the capacitor through which that current is flowing decreases, but it increases when the current is negative (see Table 2-1). So with positive current, its circulation must be forced through the capacitor whose voltage level is the highest with the aim of discharging it, meanwhile with negative current it must be forced through the one whose voltage level is the lowest to charge the capacitor. It can be seen in Fig. 3-1 that the algorithm carries out different commands depending on the current direction and the switching states. This is the main philosophy of the voltage balancing algorithm.

This algorithm will be well understood looking at Fig. 3-2 which depicts an example of the lower arm switching states of a MMC formed by 8 submodules in total, 4 in each arm. Every time the lower reference signal crosses with one of the triangular signals $(T_5 \ldots T_8)$, the control algorithm decides which submodule of the arm toggles depending on the $V_{ci(5\text{-}8)}$. The first commutation that appears in the figure happens as a result of the intersection between T_5 and V_l*. In this case one switch must be deactivated because the

triangular is becoming greater than the reference. The current is negative so following the steps of the diagram of Fig. 3-1, the switch which should change is that whose capacitor voltage is the highest, S_5. As its state is on, it is possible to switch it off. Paying attention to the next commutation where a switch on takes place being $i_2<0$, it should be noticed that instead of activating S_7 (as the intersection occurs with T_7), the switch that toggles is S_8. This is because V_{c8} is the lowest capacitor voltage and its previous state is $S_8=0$. If in that moment S_8 was already on, that is, $S_8=1$, it will be the turn of the next submodule with less capacitor voltage to switch on, in this example S_7. In case this one was also activated, the algorithm would continue checking the next states in increasing order of capacitors voltage until it found one whose state was off.

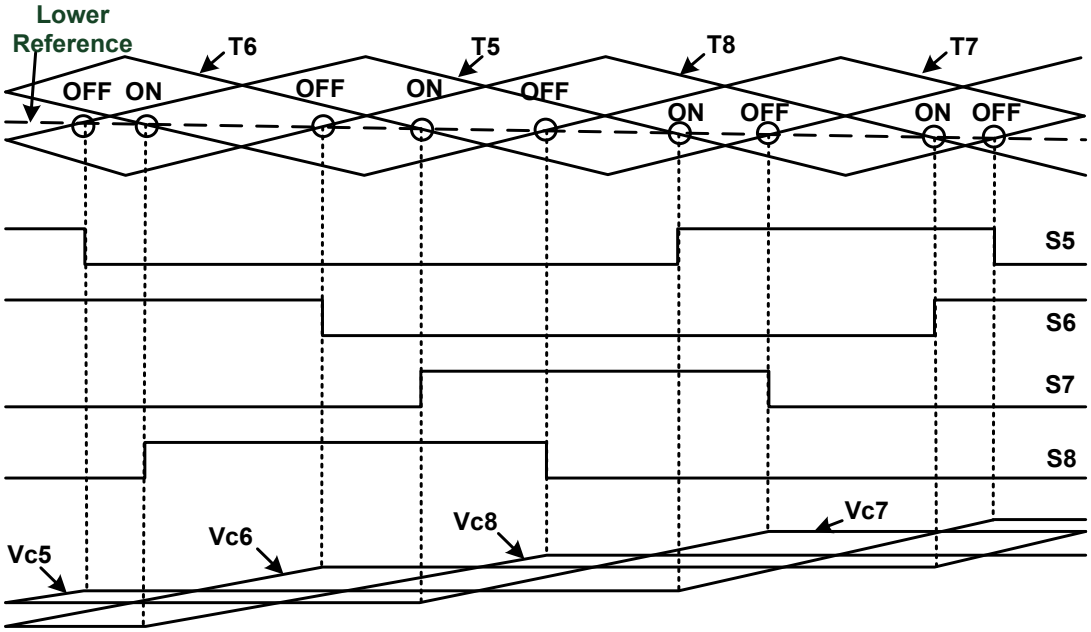


Fig. 3-2. Detailed lower arm switching behaviour of a single phase with 8 submodules Modular Multilevel Converter when i2<0.

To recapitulate and validate all the previous concepts, this modulation has been applied to the simplest model of the Modular Multilevel Converter: a single phase MMC with four 2L submodules at all, two in each arm. The most significant parameters of this converter are: $V_{DC}=500V$, $C_i=4.1mF$, $L_1=L_2=2mH$. It is connected to an L filter ($L_{out}=2mH$, $R_{out}=0.1\Omega$) and to the grid $(V_{g\_rms}=163V)$.

Fig. 3-3 is focused on the lower arm of the converter. Two triangular carriers are needed $(T_{2\text{-}3})$ and a reference V_l* to achieve the switching pulses for the two submodules of that arm. As a consequence of their IGBTs commutations, the voltage of capacitors V_{c3} and V_{c4} are reflected at submodules terminals as V_{l1} and V_{l2} respectively. The sum of these two voltages works out V_l while V_{th} represents the two arms output voltage. Note that

the steps of these signals have got a regular value which means that capacitors are pretty well balanced due to sinusoidal currents as can be seen in Fig. 3-4.

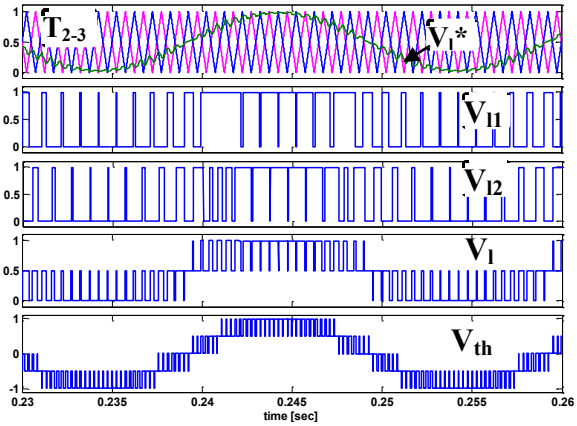


Fig. 3-3. Single phase 4 2L submodules MMC. Triangular and reference signals of the lower arm, voltages at the output of the two lower submodules, voltage of the lower arm and output voltage being *cos(φ)=1*, f_{sw}*=1 kHz* (all in p.u.).

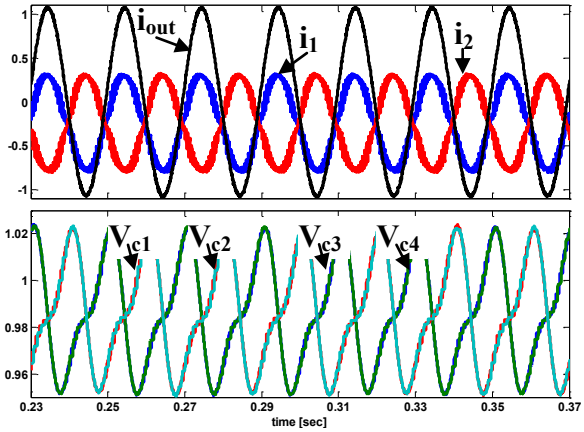


Fig. 3-4. 4 Single phase 2L submodules MMC. Converter currents and capacitors voltages being *cos(φ)=1*, f_{sw}*=1 kHz* (all in p.u.).

It has been verified that the balancing works correctly for any operation mode of *ma*, *cos(φ)*, etc. It is evidenced in Fig. 3-5-Fig. 3-6 where the working point has changed to *cos(φ)=0.76*. The modification of the shape in the capacitors voltage is what stands out most. The ripple of these signals has got a 50 Hz plus a 100 Hz component (as explained in 2.4.1.1) which gets altered according to the power exchange. That is what exactly happens in this example, *P* and *Q* values have been changed to obtain another working point and consequently the capacitors ripple and the arm currents have also undergone that change.

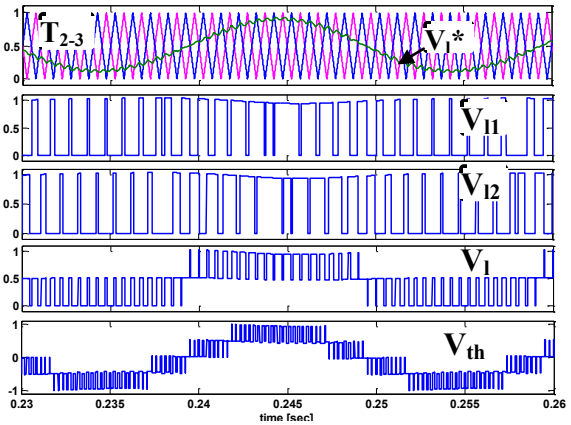


Fig. 3-5. Single phase 4 2L submodules MMC. Triangular and reference signals of the lower arm, voltages at the output of the two lower submodules, voltage of the lower arm and output voltage being *cos(φ)=0.76*, f_{sw}*=1 kHz* (all in p.u.).

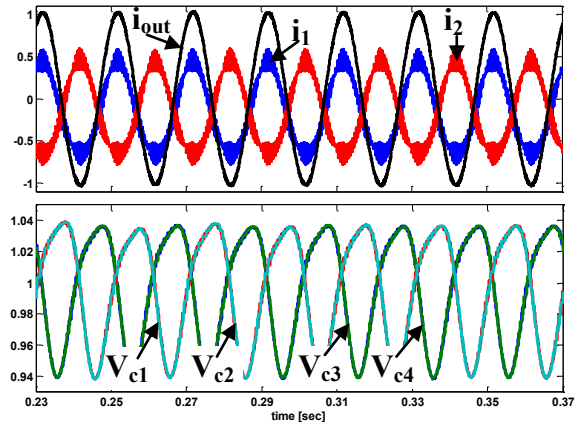


Fig. 3-6. 4 Single phase 2L submodules MMC. Converter currents and capacitors voltages being *cos(φ)=0.76*, f_{sw}*=1 kHz* (all in p.u.).

3.2 Modulation applied to 3L-FC submodules

Not only is the developed modulation well suited to any number of submodules per phase but also to different submodule configurations. The algorithm has been described for 2L submodules but it is also valid for multilevel submodules adding minor amendments.

In chapter 2.2.2 how to create all the triangular carriers and the reference signals to get the semiconductor firing pulses for the MMC with 3L-FC submodules is explained. Even though the previous modulation technique was a PWM, carriers as well as reference signals keep unaltered for this modulation technique. Meanwhile in the standard PWM has been revealed that the carrier signals are linked with a determined semiconductor, in this modulation what must be correlated are capacitors with semiconductors. The reason is that in this case semiconductors will commute disorderly depending on capacitors voltages and the arms current direction, with the aim of balancing all these capacitors.

Thus, the modulation algorithm explained before (Fig. 3-1) can be applied to this submodule topology assuming that capacitor C_{1i} is related to S_{1i} and C_{2i} to S_{2i}. In the FC configuration, as half of the capacitors have got twice the capacity than the rest, their voltage is also supposed to be always the double $(V_{c1i}=2\cdot V_{c2i})$.Then, in order to get comparable voltages in the modulator block, great capacitors measured voltages are divided by two. Afterwards the algorithm puts in order these voltages before deciding which submodule should commute following the steps of Fig. 3-1.

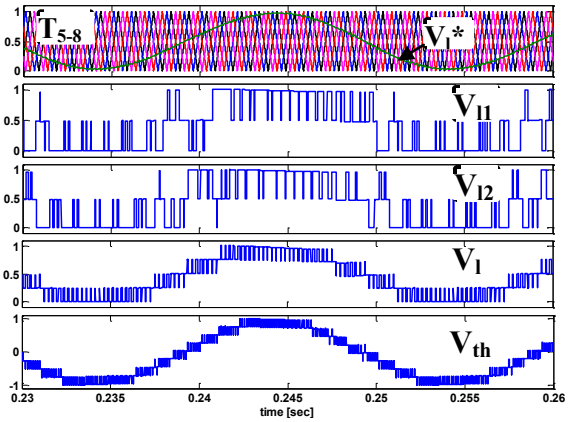


Fig. 3-7. Single phase 4 3L-FC submodules MMC. Triangular and reference signals of the lower arm, voltages at the output of the two lower submodules, voltage of the lower arm and output voltage being *cos(φ)=1*, f_{sw}*=1 kHz* (all in p.u.).

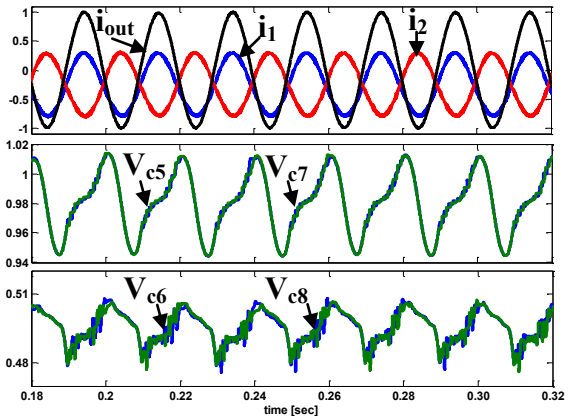


Fig. 3-8. Single phase 4 3L-FC submodules MMC. Converter currents and lower arm capacitors voltages being *cos(φ)=1*, f_{sw}*=1 kHz* (all in p.u.).

After these explanations, it is rather clear that the operating mode as well as the output signals of the converter with 3L-FC submodules configuration are very similar to the 2L submodules configuration.

Once having explained how to apply the aforementioned modulation algorithm to the 3L-FC submodules, the simulation results will be shown. The converter model is again a single phase MMC with $n=4$ and the same parameters as the one described for the 2L submodules simulation obtaining as a result Fig. 3-7 and Fig. 3-8.

Being the switching frequency of the carriers 1 kHz as in the 2L submodules model, in Fig. 3-7 it is clearly observed that the apparent frequency of the output signal (V_{th}) is twice that frequency because in this topology the double amount of triangular signals per phase are required [59]. Moreover, although $n=4$ in both converters, in this case 3 voltage levels are obtained per submodule (see V_{l1} and V_{l2}) and as a consequence, V_{th} is formed by 9 voltage levels. As far as the balancing is concerned, lower arm capacitors voltages are plotted in Fig. 3-8. Note that $V_{c5}=2\cdot V_{c6}$ or $V_{c7}=2\cdot V_{c8}$ relationship is satisfied and at the same time their value is totally balanced as a clear evidence of the smooth operation of the modulation block.

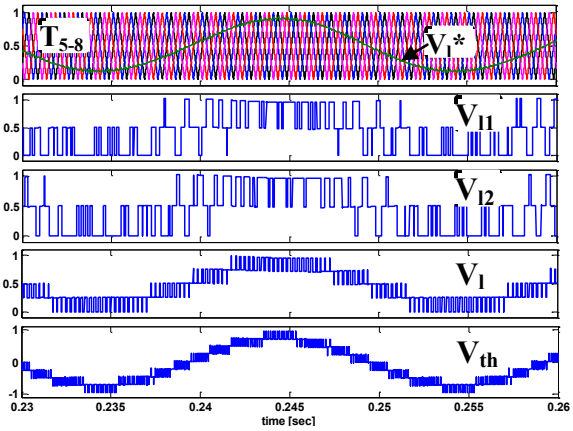


Fig. 3-9. Single phase 4 3L-FC submodules MMC. Triangular and reference signals of the lower arm, voltages at the output of the two lower submodules, voltage of the lower arm and output voltage being $cos(\varphi)=0.76$, $f_{sw}=1$ kHz (all in p.u.).

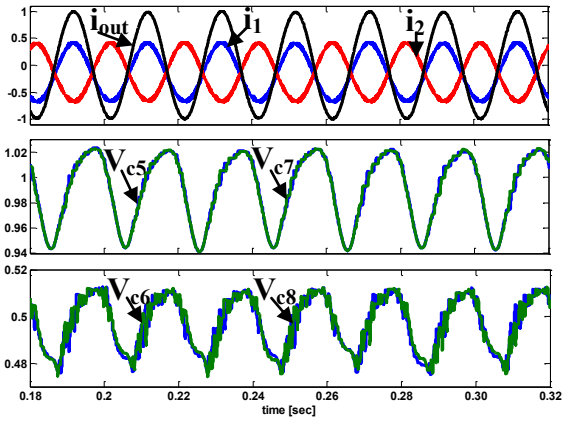


Fig. 3-10. Single phase 4 3L-FC submodules MMC. Converter currents and lower arm capacitors voltages being $cos(\varphi)=0.76$, $f_{sw}=1$ kHz (all in p.u.).

Apart from the results taken when $ma=1$ and $cos(\varphi)=1$, it has been verified that the balancing is working correctly at different operating conditions. For example, Fig. 3-9 and Fig. 3-10 are obtained when $cos(\varphi)=0.76$, but the resulting signals are similar to the previous ones except for capacitors ripple appearance.

3.3 Modulation applied to 3L-NPC submodules

As with the 3L-FC submodules, the explanation of creating the modulator input signals to get the semiconductor firing pulses for the converter is included in chapter 2.3.2. Once these are correctly generated, the aforesaid modulation algorithm (Fig. 3-1) can be applied assuming that capacitor C_{1i} is correlated to S_{1i} and C_{2i} to S_{2i}.

Next, the simulation results of the 3L-NPC submodules will be exposed. In Fig. 3-11 some representative voltages of the converter are depicted. Despite using the same number of carrier signals as in the 3L-FC submodules topology, the apparent frequency of V_{th} of this figure is half that of the one in Fig. 3-7. It is owing to the LSPWM technique used in combination with the PSPWM to generate the carrier signals.

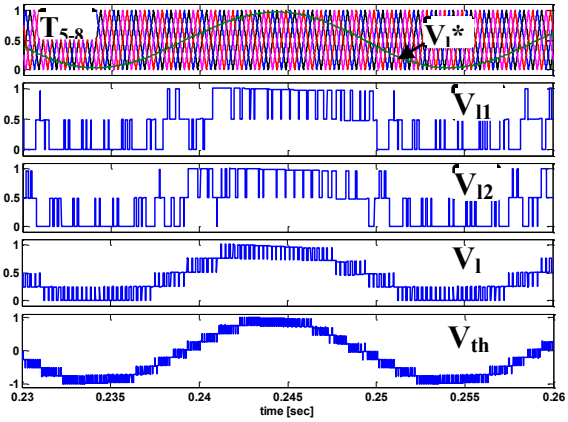


Fig. 3-11. Single phase 4 3L-NPC submodules MMC. Triangular and reference signals of the lower arm, voltages at the output of the two lower submodules, voltage of the lower arm and output voltage being *cos(φ)=1*, f_{sw}*=1 kHz* (all in p.u.).

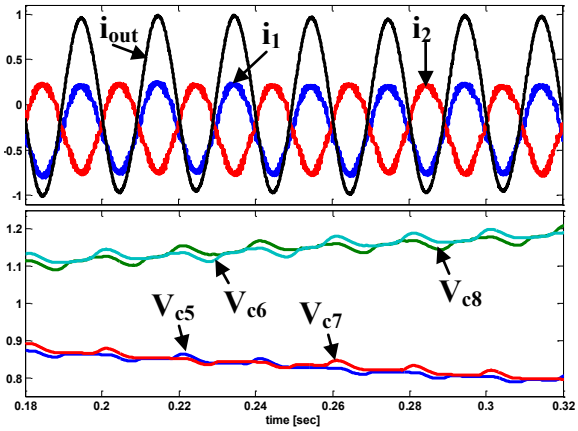


Fig. 3-12. Single phase 4 3L-NPC submodules MMC. Converter currents and lower arm capacitors voltages being *cos(φ)=1*, f_{sw}*=1 kHz* (all in p.u.).

The converter model has not changed from the previous simulations but the result of Fig. 3-12 reveal that even applying the new modulation, using 3L-NPC submodules capacitors voltages tend again to diverge. Looking at this picture, it is obvious that the modulation tries to get the required output voltage V_{th}. However, the balancing of the capacitors cannot be achieved reaching an unstable operating point. Consequently, although the shape of V_{th} is apparently acceptable, taking a close look to that signal (or to V_{l1} and V_{l2}) it can be noted that its levels are unequal because they depend on the actual capacitors voltages. Paying attention to Table 2-5, it can be observed that for each voltage level provided at the terminals of the submodule, the switching states of semiconductors do not matter that until the arm current direction changes, it is unworkable to alter the tendency of the capacitors. This means that if a capacitor is

getting charged, it can never be forced to start discharging (or conversely). At most its value can be kept constant.

Modifying P and Q power exchange in order to provoke a variation in the phase shift between output current and voltage, unlike the previous simulation, it is demonstrated by means of Fig. 3-13 and Fig. 3-14 that for example, when $cos(\varphi)=0.5$ the balancing of the capacitors voltages is achievable.

After carrying out a thorough analysis on this converter topology, the boundaries which define its stability are collected in the graph of Fig. 3-15. As it is done in [86], a $cos(\varphi)$ sweep is made by means of successive simulations in which a modulation index is imposed, the amplitude of the current remains constant but the phase shift between i_{out} and V_{th} is modified from 0º to ±180º. In this way, whether or not the modulation is able to balance the bus capacitors in each case is checked.

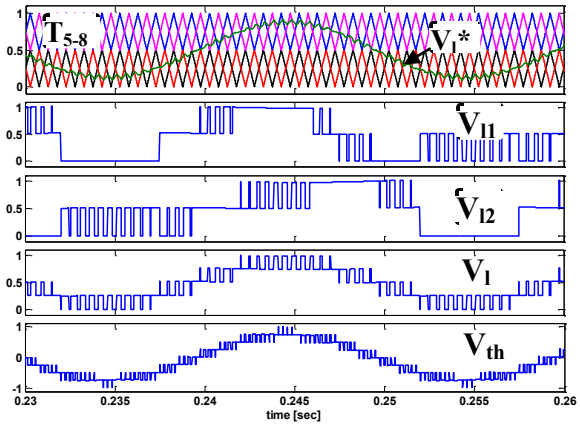


Fig. 3-13. Single phase 4 3L-NPC submodules MMC. Triangular and reference signals of the lower arm, voltages at the output of the two lower submodules, voltage of the lower arm and output voltage being $cos(\varphi)=0.5$, $f_{sw}=1$ kHz (all in p.u.).

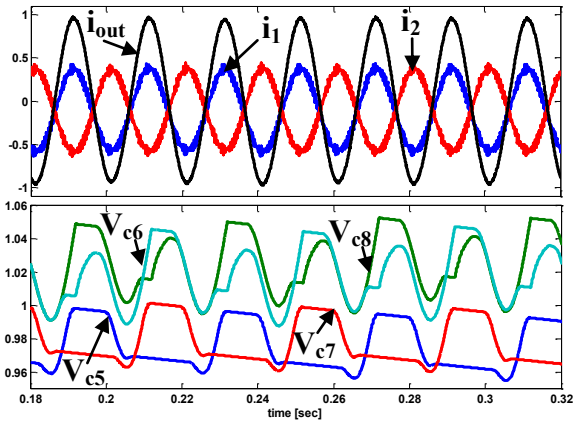


Fig. 3-14. Single phase 4 3L-NPC submodules MMC. Converter currents and lower arm capacitors voltages being $cos(\varphi)=0.5$, $f_{sw}=1$ kHz (all in p.u.).

Summarizing, when the modulation index of the output voltage is under 0.4, the converter is able to balance all the capacitors without any restriction, which is reasonable because V_{th} signal is formed of few voltage levels and in that situation more switching combinations are possible. But unfortunately as modulation index increases, the $cos(\varphi)$ limit which allows an acceptable balancing is reduced as detailed in Fig. 3-15.

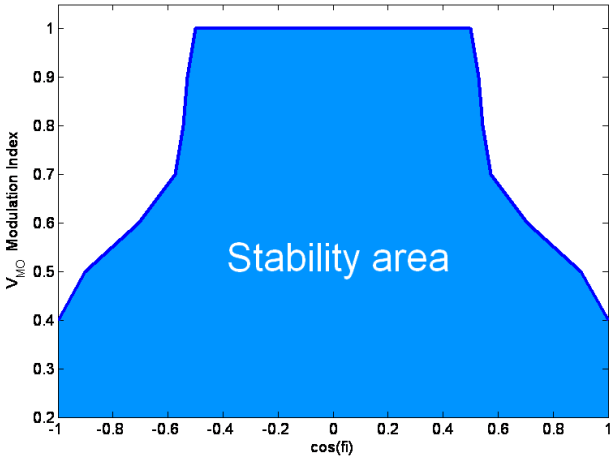


Fig. 3-15. Stability graph of the 3L-NPC submodules MMC.

3.3.1 Modification in the modulation of the MMC with 3L-NPC Submodules

A successful variation has been included in the modulation algorithm by means of which is possible to get the balancing of the capacitors for the whole *cos(φ)* range. It lies in altering triangular amplitudes so that the t_{on}-t_{off} ratio (duty cycle) of IGBTs is modified. By doing so, the medium current along capacitors could be the desired one so as to increase or decrease their voltage depending on their instantaneous value.

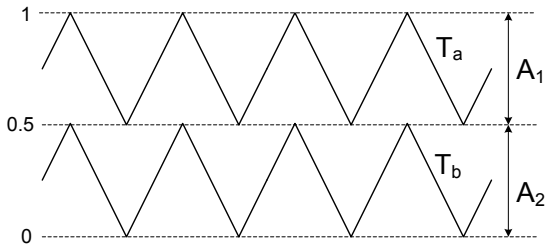


Fig. 3-16. Amplitude of the two triangular signals of a 3L-NPC submodule.

As stated before, two triangular signals are needed per 3L-NPC submodule, the amplitude of each one being 0.5 p.u. and disposed as in Fig. 3-16. Not only should the voltage of these capacitors fulfil equation (3-1) but also keep them balanced. In case of a deviation in both capacitor voltages the amplitude of the carrier signals should change in relation to the produced variation as expressed in equation (3-2). Therefore, every calculation step, the modulus of all the triangular signals is determined being the one of triangular T_a the calculated in equation (3-3) while the modulus of T_b the one estimated from (3-4). Note that if the deviation is positive ($V_{1i} > V_{2i}$ according to (3-2)), A_2 will result larger than A_1 and vice versa. It has to be remarked that any frequency of triangular signals changes, only the gradient. Otherwise the switching frequency of IGBTs would also change which is not desirable.

$$V_{c1i} + V_{c2i} = V_{ci} = 1\,p.u \tag{3-1}$$

$$V_{c1i} - V_{c2i} = \frac{\Delta V_{ci}}{V_{c1i} + V_{c2i}} \tag{3-2}$$

$$|A_1| = 0.5 - \frac{\Delta V_{ci}}{V_{c1i} + V_{c2i}} \tag{3-3}$$

$$|A_2| = 0.5 + \frac{\Delta V_{ci}}{V_{c1i} + V_{c2i}} \tag{3-4}$$

Simulation results with the described modulation implemented are shown in Fig. 3-17 and Fig. 3-18. The most unfavourable case is represented *(Q=0)* in order to test the modulation algorithm. In the first plot of Fig. 3-17 the four triangular signals of the lower arm are depicted. As the image is not clear enough, it has been magnified to be able to distinguish the variation in the amplitude of $T_{5\text{-}8}$. Thanks to this alteration, V_{th} is properly formed and capacitors voltages keep constant all the time around the fixed value. However, a remarkably drawback appears at arm currents. Changing the amplitude of carrier signals with the intention of altering the voltage on capacitors, implies at the same time a modification of the output signal besides a variation on both arms consumption.

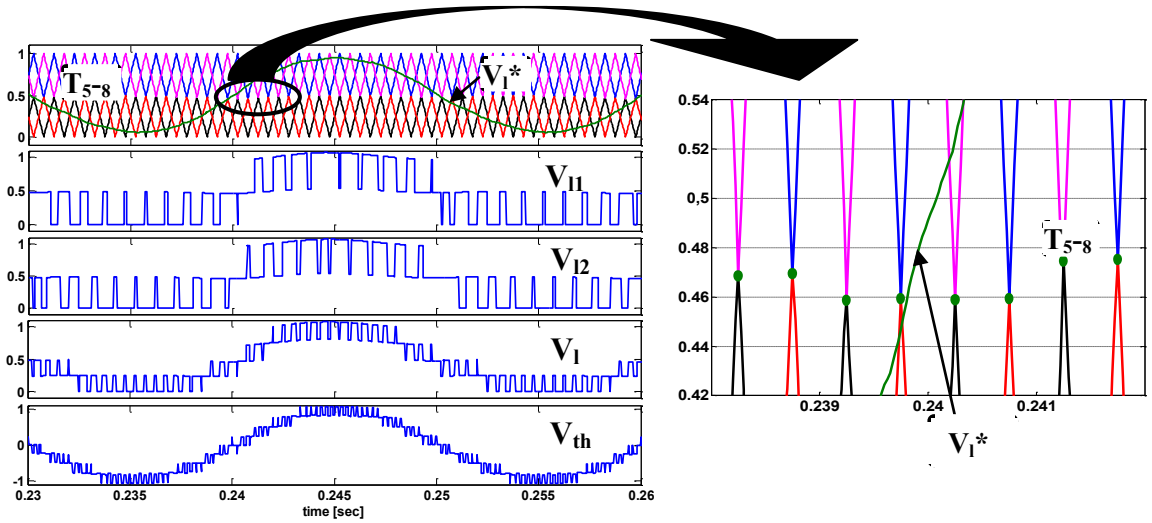


Fig. 3-17. Single phase 4 3L-NPC submodules MMC including a modification in the modulation. Triangular and reference signals of the lower arm, voltages at the output of the two lower submodules, voltage of the lower arm and output voltage being *cos(φ)=1*, f_{sw}*=1 kHz* (all in p.u.).

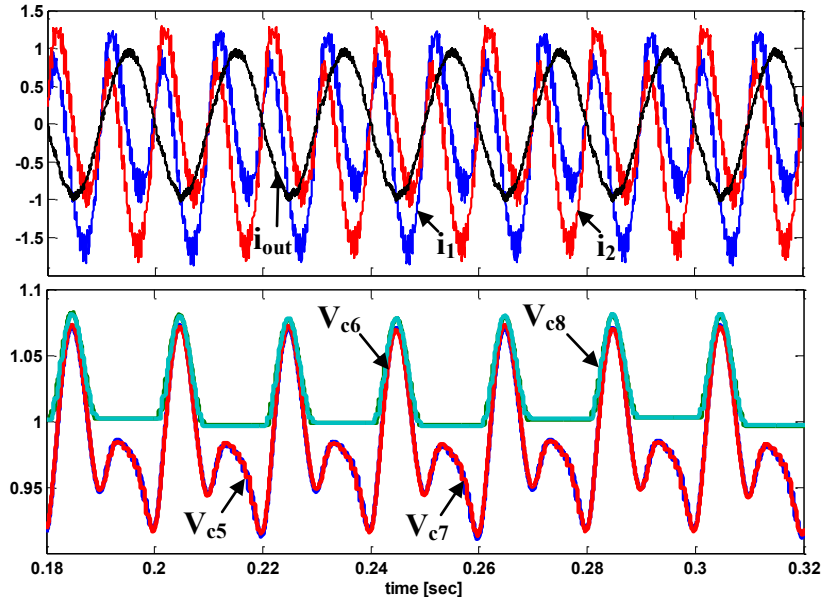


Fig. 3-18. Single phase 4 3L-NPC submodules MMC including a modification in the modulation. Converter currents and lower arm capacitors voltages being *cos(φ)=0.5*, f_{sw}*=1 kHz* (all in p.u.).

The perturbation generated in the two arms can be compensated by adding a zero sequence component control in the three phase system which will modify V_u* and V_l* references. As a result, a second order harmonic turns up in i_1 and i_2 as can be seen in Fig. 3-18. Although this harmonic does not appear in the output signals such as V_{th} or i_{out} and does contribute to the balancing, it disrupts the operation of the converter. For example, the amplitude of arm currents is much higher than i_{out} meanwhile in previous cases it was always half the amount of it. Due to this degraded performance its potential application in real systems is reduced.

3.4 Validation of the modulation for a HVDC application

All the previous simulation results have been obtained for a 1 kHz triangular frequency which may well be quite high in case of a HVDC transmission application. To test the developed modulation validity at lower switching frequencies, first a simulation of a 4 3L-FC submodules MMC has been conducted at 250 Hz. Its results are illustrated in Fig. 3-19-Fig. 3-20. Despite the encountered difficulties owing to the low f_{sw} and low number of submodules, the obtained voltages are the right ones and the modulator is capable of balancing the eight capacitors voltages although their shapes as well as the currents are slightly degraded.

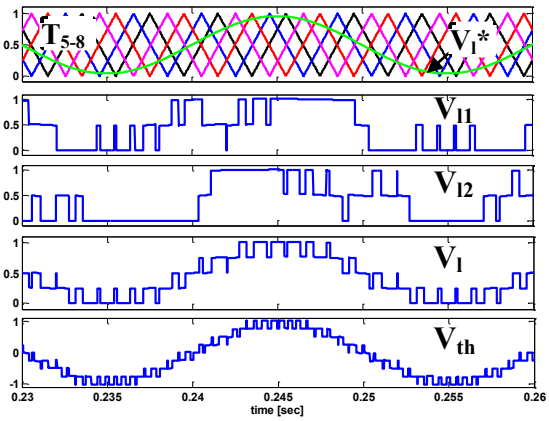


Fig. 3-19. Single phase 4 3L-FC submodules MMC. Triangular and reference signals of the lower arm, voltages at the output of the two lower submodules, voltage of the lower arm and output voltage being *cos(φ)=1*, f_{sw}*=250 Hz* (all in p.u.).

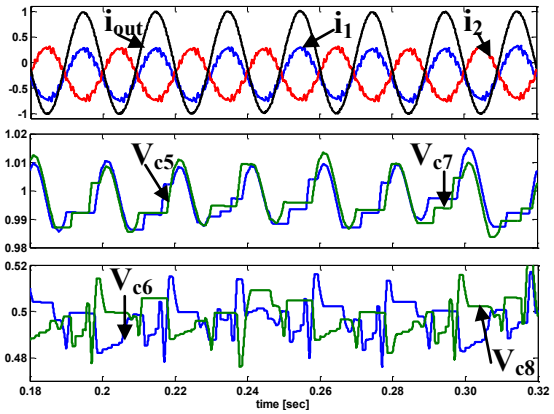


Fig. 3-20. Single phase 4 3L-FC submodules MMC. Converter currents and lower arm capacitors voltages being *cos(φ)=1*, f_{sw}*=250 Hz* (all in p.u.).

Besides corroborating the proper operation of the modulation at low triangular frequencies, Fig. 3-21-Fig. 3-22 give evidence of its effectiveness when the application requires a high number of submodules. The proposed simulation scenario consists of a 140kV DC transmission being the converter a single phase 2L submodule MMC. A medium voltage semiconductor has been selected as the switching device whose $V_{CE@100FIT}$*=2800V* and which withstands a maximum current of I_c*=1200A*. This information is enough to calculate in (3-5) the number of submodules per phase of the converter, *n=100* in this case (actually in a real converter extra submodules would be installed to assure the redundancy).

$$n = \frac{V_{DC}}{V_{CE@100FIT}/2} = \frac{140kV}{2.8kV/2} = 100 \text{ (2L submodules)} \tag{3-5}$$

Following the sizing methodology described in the chapter 2.4, the capacitor and inductances are going to be calculated. For that, the ripple of the capacitors voltage and converter currents is considered to be a 10% of the value at most. Moreover, only active power is assumed to be transmitted at an unitary modulation index.

$$C_i \geq \frac{3\cdot\sqrt{3}\cdot P}{\Delta V_{cimax}\cdot V_{ci}\cdot\omega\cdot n\cdot 2} = \frac{3\cdot\sqrt{3}\cdot\frac{140kV}{2\cdot\sqrt{2}}\cdot\frac{1200}{\sqrt{2}}}{280\cdot 2800\cdot 2\cdot\pi\cdot 50\cdot 100\cdot 2} \approx 4.4mF \tag{3-6}$$

$$L_u \geq \frac{\frac{V_{ci}}{2}\cdot\frac{T_{pwm}}{n}}{\Delta i_l} = \frac{\frac{2800}{2}\cdot\frac{1/100}{100}}{\frac{1200}{2\cdot\sqrt{2}}\cdot 0.1} \approx 3.29mH \tag{3-7}$$

$$L_{th} \geq \frac{\frac{V_{ci}}{2} \cdot 0.5 \cdot \frac{T_{pwm}}{n}}{\Delta i_{out}} = \frac{\frac{2800}{2} \cdot 0.5 \cdot \frac{1/100}{100}}{\frac{1200}{\sqrt{2}} \cdot 0.1} \approx 0.82mH \qquad (3\text{-}8)$$

Along the modelling of the converter it has been commented that the two arm inductors have the same value *(L_u=L_l=L)* and therefore the Thévenin inductance results L_{th}=L_{out}+$L/2$. In (3-12) L_{th} turns out to be smaller than L_u meaning that there is no need of using an output filter L_{out} in order to fulfil the requirements of the current ripple. The reason is that the two arms inductances have got influence over the dynamic of i_{out}. The ripple on arms currents is much bigger than the ripple on output currents. Thus, if the inductances L_u and L_l are sized to get less than a 10% ripple in their currents, it implies a decreasement on i_{out}'s ripple being it less than a 10% too.

To sum up, the simulation model in which this modulation has been applied this time is a single phase MMC with 100 2L submodules whose most significant parameters are according to equations (3-6), (3-7): C_i=*4.5mF*, L_u=L_l=*4mH*. Despite not being necessary, it is connected to an *L* filter *(L_{out}=2mH, R_{out}=0.2Ω)* to make it easier to control the system and to the grid *(V_{g_rms}=50kV)*. Although the switching frequency is 100 Hz, as the number of submodules is so high, the resulting signals are of very good quality.

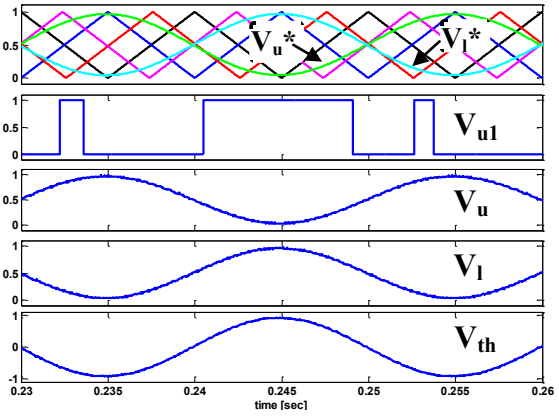


Fig. 3-21. Single phase 100 2L submodules MMC. Few triangular and the reference signals, voltage of the first upper submodule, voltage of the upper and lower arm and output voltage being *cos(φ)=1*, *f_{sw}=100 Hz* (all in p.u.).

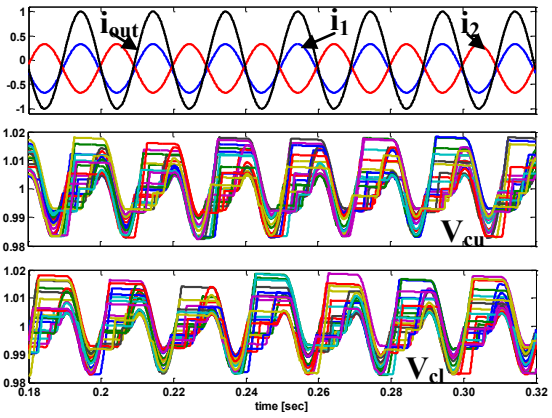


Fig. 3-22. Single phase 100 2L submodules MMC. Converter currents and both upper and lower arm capacitors voltages (only some of them) being *cos(φ)=1*, *f_{sw}=100 Hz* (all in p.u.).

This modulation is already demonstrated to be suitable for any number of submodules in the arm or switching frequencies but it is also quite simple to extrapolate it to a three phase MMC model (see Fig. 2-1 or Fig. 3-23). On the single phase model the output AC

signal of the converter is considered V_{th}. However, on the three phase model, the three output signals are considered those between terminals *r*, *s* or *t* and the neutral point called *X* in Fig. 3-23. In order to obtain those voltages, the converter is supposed to be a balanced system where (3-9) and (3-10) expressions are fulfilled:

$$i_r + i_s + i_t = 0 \tag{3-9}$$

$$V_{rX} + V_{sX} + V_{tX} = 0 \tag{3-10}$$

To get the equations referred to *X* instead to *O,* the following equalities are applied (3-11)-(3-13):

$$V_{rO} = V_{rX} + V_{XO} \tag{3-11}$$

$$V_{sO} = V_{sX} + V_{XO} \tag{3-12}$$

$$V_{tO} = V_{tX} + V_{XO} \tag{3-13}$$

Adding these last equations and bearing (3-10) in mind, some terms are removed. This way, the unknown factor V_{XO} could be easily worked out as written in (3-14). Once the value of V_{XO} managed, it is simple to get V_{Kn} where *k=r, s or t*.

$$V_{XO} = \frac{1}{3} \cdot \left(V_{rX} + V_{sX} + V_{tX} \right) \tag{3-14}$$

The most representative signals of the three phase converter are exposed from Fig. 3-24 to Fig. 3-26. First, the currents and the output voltage referred to *O* of one phase are depicted in Fig. 3-24. Notice that there is almost no difference in comparison with the single phase converter's signals. Again, it is hard to appreciate the 101 levels which form the output signal as it has more or less the same shape of it reference. Then, in the top chart of Fig. 3-25, the voltages of all the capacitors of a phase are shown meanwhile in the bottom chart the sum of the one hundred capacitor's voltage and it reference are shown. It can be seen that all the capacitors are properly balanced and that each capacitor presents less than 10% of voltage oscillation which becomes in only a 3%

oscillation in the total voltage above its reference due to the opposite shape between the upper and lower capacitors ripple.

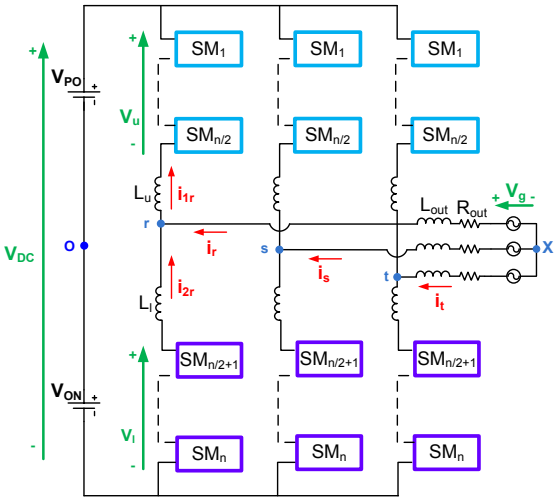


Fig. 3-23. Layout of the three phase MMC.

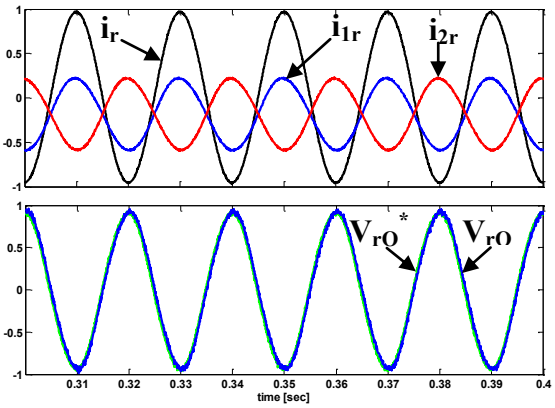


Fig. 3-24. 3 phase100 2L submodules MMC. Currents of the *r* phase and voltage and reference of *r* phase referred to *O* being *cos(φ)=1*, f_{sw}*=500 Hz* (all in p.u.).

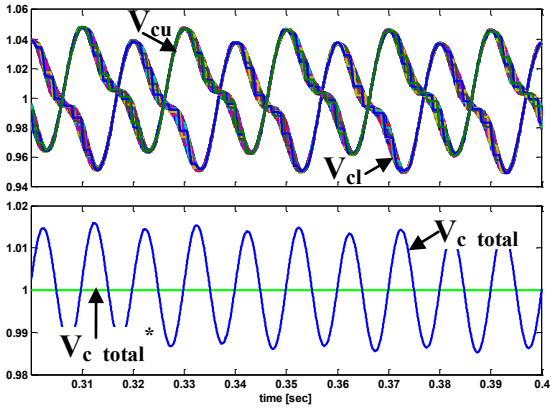


Fig. 3-25. 3 phase 100 2L submodules MMC. Upper – lower arm capacitors voltages of one phase and the sum of all them with the reference being *cos(φ)=1*, f_{sw}*=500 Hz* (all in p.u.).

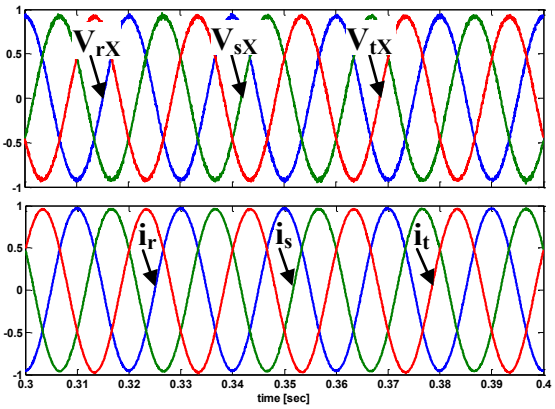


Fig. 3-26. 3 phase 100 2L submodules MMC. Three phases voltages and currents being *cos(φ)=1*, f_{sw}*=500 Hz* (all in p.u.).

Finally, the graphic on the top of Fig. 3-26 illustrates the three phases' output voltages between *r*, *s*, *t* points and the common neutral point *X* meanwhile the bottom graphic represents the three phases' output currents of Fig. 3-23. Note that there is 120º phase shift among converter phases which means that the system is balanced thanks to the correct operating modulation. Sinusoidal shape at the output AC terminals is the main advantage of this multilevel converter because big filters are avoided.

The oscillatory behaviour of the capacitors voltage differs from Fig. 3-22 to Fig. 3-25. It is mainly owing to the extremely low triangular frequency. This parameter (f_{sw}) is

deduced, as will be described in chapter 5, from a compromise among: power losses (converter's efficiency), thermal stress (working life of the semiconductor), quality of the output waveform, capacitors voltage ripple, etc.

3.5 Conclusions

In this chapter the developed modulation algorithm based on the PWM for MMCs is detailed. It has to be highlighted that in this thesis none modulation technique is developed, in fact, anyone employed for multilevel converters can be applied. What essentially has been done here is to modify slightly the chosen modulation technique to achieve the balancing of the capacitors. Instead of following an even switching pattern, the modulator algorithm chooses which submodule has to be activated or deactivated according to the capacitors voltages when the modulation technique detects that a submodule state has to be toggled. The most important features compared to the previously mentioned balancing methods can be summarized as follows:

•It has been designed in such a way that, a prior analysis of the specific converter arrangement is not necessary to identify redundant voltage combinations. Thus, the adaptation of the algorithm to arrangements of MMC with a different number of submodules is straightforward.

•For this reason as well, it is easily adaptable to arrangements of MMC with different multilevel submodule concepts.

It is clear that this modulation algorithm is suitable for any topology of submodule employed in the MMC arrangement, which allows the voltage balancing of the capacitors comprising the converter to be obtained. Thus, by means of simulation results carried out in Simulink software tool, the successful performance of capacitors balancing at any operating condition ($cos(\varphi)$, f_{sw}, n) is validated, with submodules 2L (even in the three phases converter) and 3L-FC topologies. In this way, this topologies operating with the proposed modulation method, could be useful for grid connected high power and high voltage applications such as HVDC power transmission or STATCOM applications.

On the other hand, the results obtained with 3L-NPC submoudules with the proposed modulation are not as successful as with 2L or 3L-FC submodules, since the voltage balancing cannot be guaranteed when the active power exchange is predominant to the

reactive power (*cos(φ)* near 1). Nevertheless, this 3L-NPC based topology could be useful for instance, in STATCOM applications. Trying to solve the problem with 3L-NPC submodules, the proposed modulation algorithm is modified, imposing a second harmonic current circulation through the arm currents, allowing the successful capacitors voltage balancing to be obtained. However, these arm currents are significantly increased, reducing the effectiveness of the solution for practical applications. Finally, it can be concluded and highlighted that the proposed modulation technique could also be extended to different multilevel topologies such as NPP, SMC, etc and combined with higher number of multilevel levels too.

Chapter 4

Experimental validation of the modulation strategy

In previous chapters the MMC is modelled by means of the differential equations which define the dynamic of the converter. That modelling has been helpful to simulate it in Simulink software and to develop a special modulation algorithm whose goal is to balance all the capacitors voltages besides obtaining the proper output signal. Although the simulation results confirm its effectiveness mainly in the MMC model with 2L and 3L-FC submodules, it is of big interest to corroborate it on a real implementation. So the aim of this chapter is to check if the results of the modelled converter and those of the real one match.

First of all, the used laboratory test bench is roughly described providing the most significant data and showing the main arrangement layout. Subsequently, how the control system and the modulation are implemented on a dSPACE and a FPGA boards respectively is detailed, besides explaining the interaction among all the elements of the system.

From the three submodule topologies previously analysed, only 2L and 3L-FC topologies are experimentally evaluated because it has been deduced that the MMC with 3L-NPC submodules presents some balancing restrictions. Thus the last part of the chapter focuses on the experimental results taken under different situations and the conclusions drawn therefrom.

4.1 Description of the laboratory test bench

The diagram of this laboratory setup is illustrated in Fig. 4-1 meanwhile the pictures of the real test bench appear in Fig. 4-3. It consists of a single phase Modular Multilevel Converter with 6 submodules at all, three in each arm. First, the configuration of the submodules was 2L topology (Fig. 4-1a), but after obtaining the experimental results, it was replaced by 3L-FC topology (Fig. 4-1b). Although the 3L-NPC topology has also been evaluated, it is not experimentally tested due above all to the balancing caused problems.

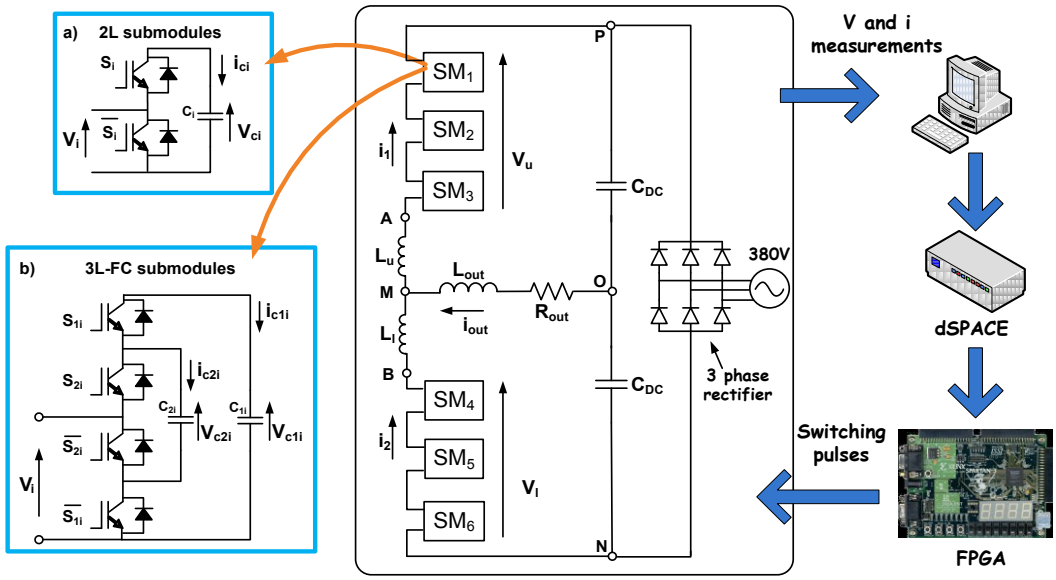


Fig. 4-1. Layout of the laboratory test bench.

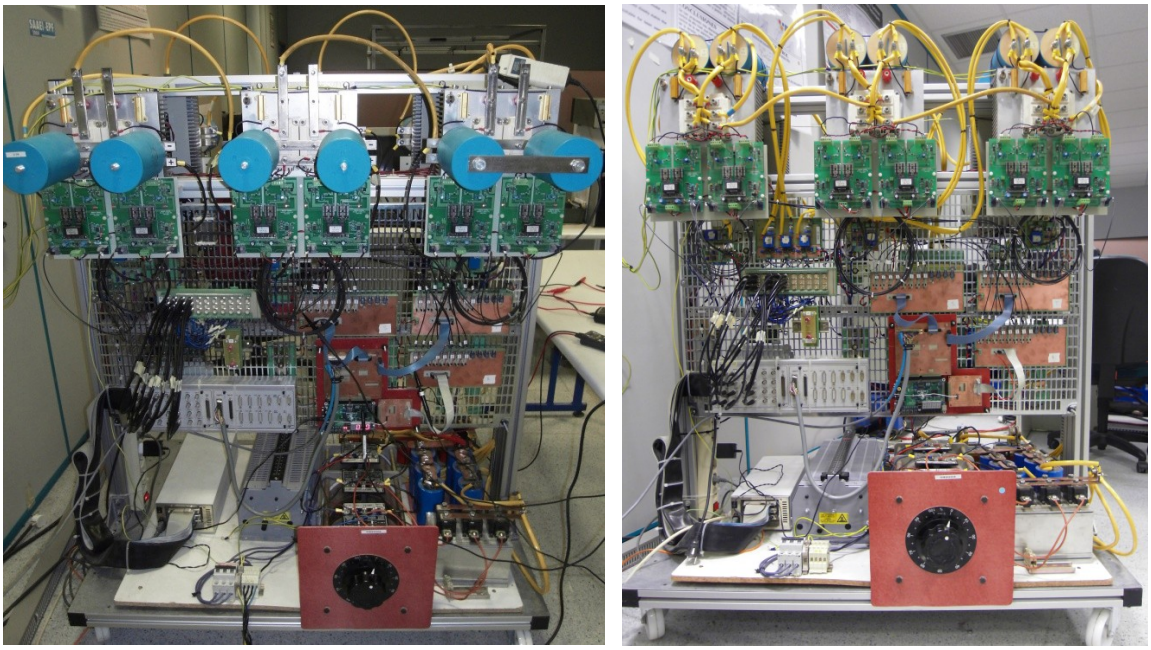


Fig. 4-2. Laboratory test bench being the configuration of its submodules: 2L topology (left) and 3L-FC topology (right).

Eupec's IGBT modules [87] are the semiconductors used in the submodules. Each module is formed by a series connection of two IGBTs with their freewheeling diode. The DC side is obtained rectifying the 3 phase's grid voltages and adding a bank of 6 capacitors in series connection. Only for simplicity, an *R-L* load is connected at the output terminals of the converter, between the two arms and the middle point of the DC side. The converter parameters are specified in Table 4-1.

IGBT module (Eupec BSM100GB170DLC)			
V_{CE}	1700 V	$I_{c,nom}$	100 A
Converter parameters			
$L_u=L_l=L_{out}$	2 mH	V_{DC}	537 V
R_{out}	47 Ω	$V_{AC\ rms}$	380 V
C_i	350mF,1100V	C_{DC}	8000mF, 400V

Table 4-1. Parameters of the single phase MMC with 6 submodules test bench.

All the connection cables are electrically isolated and a hand-operated inhibition for the IGBTs has been designed besides the rest of the protective elements included in the test bench. The control system is programmed in a dSPACE controller board meanwhile the modulation is implemented on a field-programmable gate array (FPGA). A computer is employed to visualize in a real time all the measured values as well as to modify the desired control parameters.

4.2 Implementation of the control system on a dSPACE

The control system detailed in chapter 2.5 has been designed and simulated in MATLAB/Simulink. Then it has been implemented in a rapid prototyping platform called dSPACE controller board by means of its Real-Time Interface (RTI) which is the link between dSPACE hardware and the development software MATLAB/Simulink. To connect the simulation model previously executed in Simulink to a dSPACE input/output (I/O) board, it is just necessary to drag and drop the I/O module from the RTI block library and then connect it to the Simulink blocks without the user having to write a single line of code. When the building button is pressed, the real-time model is compiled, downloaded, and started automatically on the hardware.

By means of several voltage and current sensors assembled over electronic boards placed on the converter, all capacitors voltages (V_{c_u} (upper capacitor voltages), V_{c_l} (lower capacitor voltages)), two arm currents (i_1, i_2) and the output current (i_{out}) are continuously measured. These captured signals are analogically adapted to the ADC inputs of the dSPACE Expansion Box. The first task the dSPACE controller board does

is to digitalize the received signals and send the computer the read values to display them on the Control Desk experiment software. This software which is provided with the controller board allows the user to visualize and interact with the control application in real time. It is possible to configure all I/O graphically, watch in situ the temporary evolution of any desired system variable even change any control system parameter of the model implemented in Simulink. For instance, in the picture of Fig. 4-3, some control buttons are displayed on the top in order to control the system references or to inhibit the semiconductors firing orders in case of emergency. In the remaining displays some real measures taken from the test bench are shown such as the capacitors voltages, the arms and output currents or the output voltage.

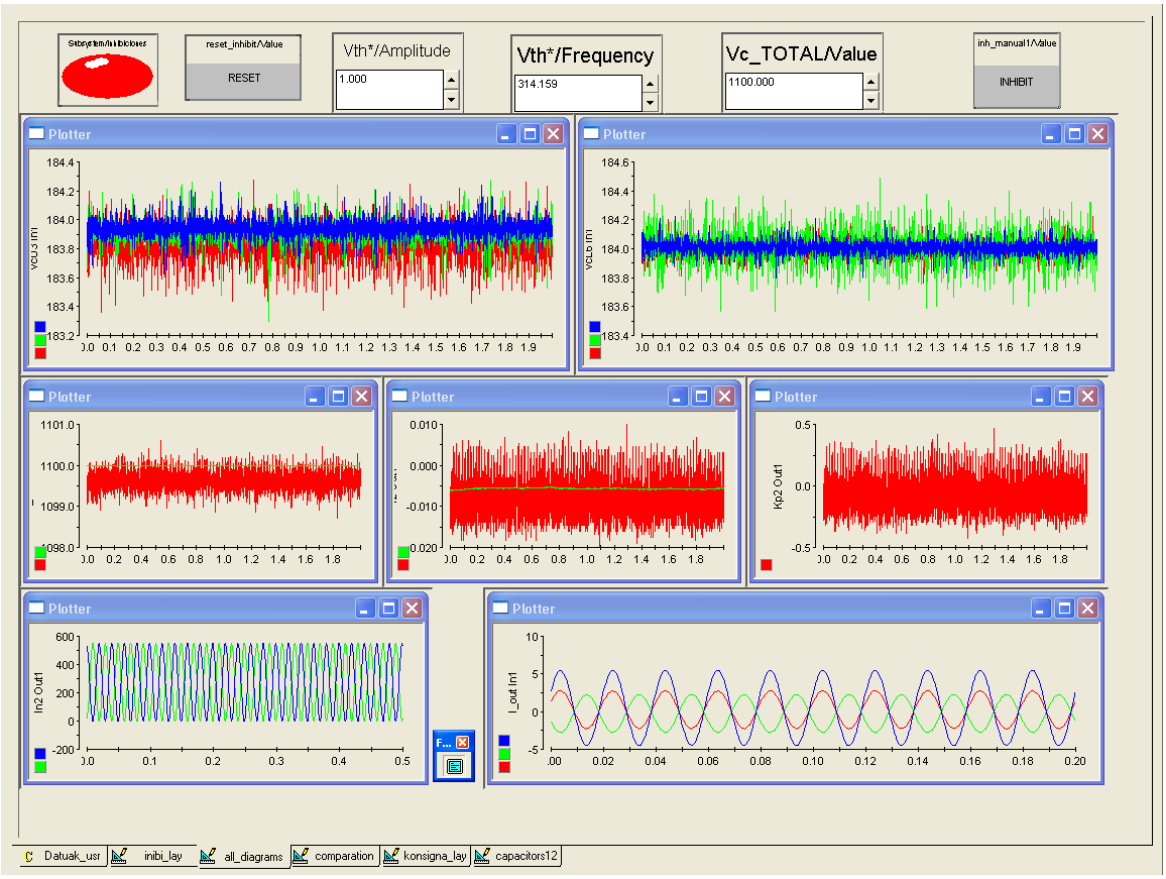


Fig. 4-3. Picture taken from the Control Desk experiment software.

Another duty carried out by this board lies in comparing the measured variables with the maximum allowable voltage and current values, so in case they exceed these limits, an inhibition signal is generated for all the semiconductors as a protection system for the converter. And the last task is to process that digital data and execute the control system with the aim of generating the two references (V_u*, V_l*) for the modulator.

Afterwards, the generated references, the inhibition and the measured variables except i_{out} are converted again to analogue signals before sending them to the modulator block which is implemented on a FPGA (see Fig. 4-4).

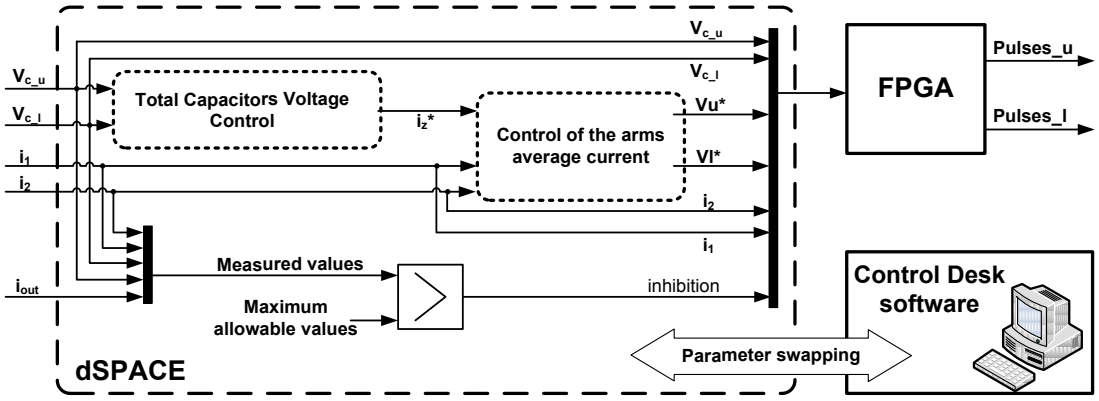


Fig. 4-4. Diagram of the control implemented on a dSPACE.

4.3 Implementation of the modulation on a FPGA

Even though the dSPACE has a PWM generation unit, the decision of incorporating a FPGA has been taken. The reason is that the dSPACE has a single PWM generation unit whereas for the aforementioned modulation several triangular carriers have to be generated. The complexity of creating these carrier signals analogically with a phase shift sufficiently precise between them has been a relevant argument for opting for the digital programmable systems.

In particular Xilinx's Starter Kit has been used which is comprised of a board with a Spartan-3 as well as other components such as seven-segment displays, leds, I/O connectors, etc. So the modulation algorithm for the converter is implemented on a FPGA which is integrated on a Spartan-3 family device of Xilinx. It is an integrated circuit which contains programmable logic components and a hierarchy of reconfigurable interconnectors that allows the blocks to be inter-wired in many different configurations [88]. This device has been programmed in VHDL language using the provided ISE Design Suite software.

Next, the way the modulation has been implemented on the FPGA will be described. During the entire document has been mentioned that both arms behaviour is similar but they just differ on the opposite switching orders. This is why in Fig. 4-5 only the schematic block of the upper arm modulation is broken down. As the converter was targeted towards high voltage applications, an important requirement was that both the

modelling and the implementation had to be easily adaptable to arrangements of high number of submodules. Note that the implementation of the modulation has been specially designed, keeping in mind this purpose.

All the data coming in different byte streams from the dSPACE (see Fig. 4-4) is stored in the memory component of the FPGA. That data is distributed to the corresponding variables when the clock signal is activated. Besides the memory and clock, there are other two identical modulation components: one for the upper arm pulses and another for the lower. They carry out the same tasks, but the input and output variables are different. Inside each modulation component, the events generator compares the triangular signals with the reference and in case there is a crossing between them, it decides whether there should be a change in the switching pulses according to the previous states. If it detects by means of the XOR logic gates that two opposite changes have been occurred at the same time (ON and OFF), it rules out the action. Otherwise, it finds out if a switch-on or switch-off should be fulfilled. Depending on the activated order, one of the next two blocks is running.

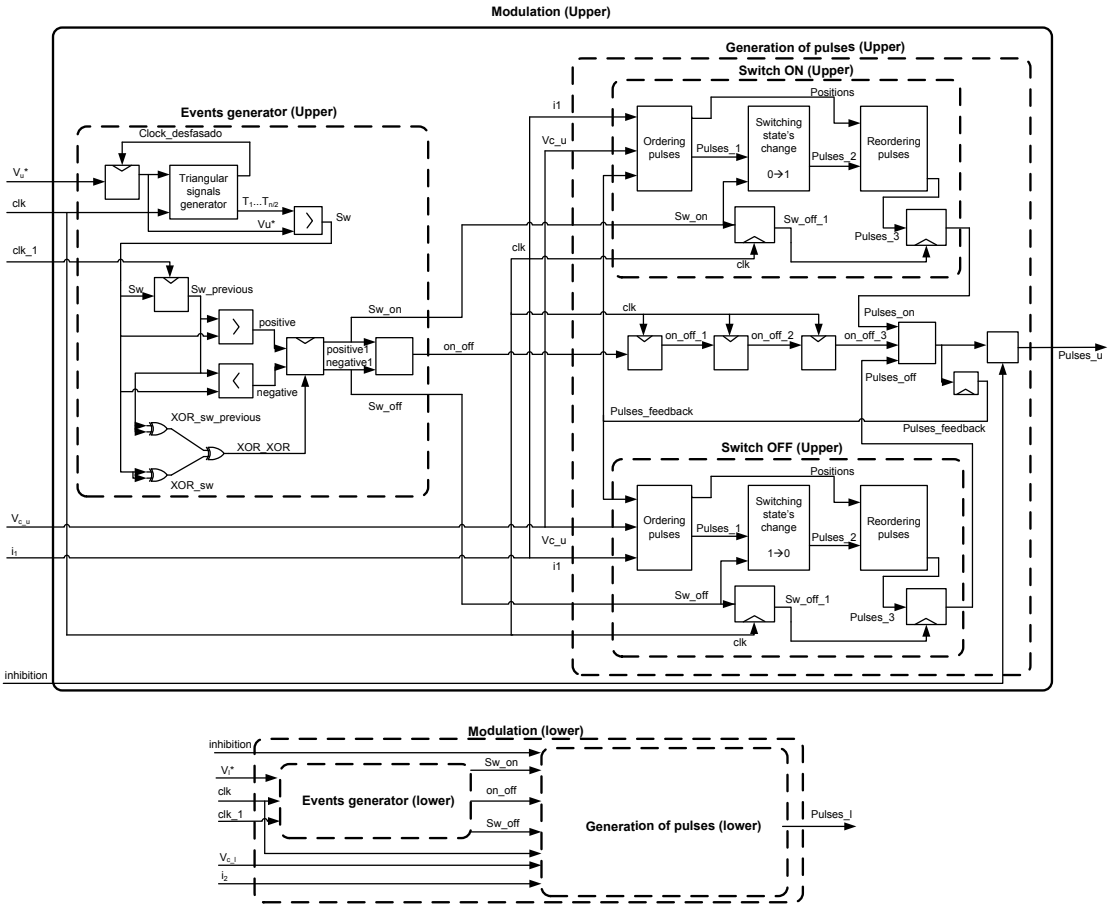


Fig. 4-5. Diagram of the modulation implemented on a FPGA.

As can be observed in Fig. 4-5, both Switch ON and Switch OFF blocks are very similar: first pulses are ordered depending on capacitors voltage, then the appropriate switching state is changed and finally the pulses are prepared to be sent to the semiconductors. From these three, the second task is the different one: on the Switch ON the corresponding switching state changes from 0 to 1 meanwhile in Switch OFF it changes from 1 to 0. Note that all these actions are synchronized by a clock signal. Thus, every clock signal the firing pulses for all the IGBTs will be updated at the output of the FPGA.

Optical fibres are used to provide isolation and fast flow of the control signals from Spartan-3 device to the semiconductors drivers of the converter. It is interesting to mention that the driver is the responsible for generating not only pulses for principal IGBTs but also those for complementary IGBTs.

4.4 Experimental Results

Once the laboratory downscaled model as well as the implementation of the control system and the modulation is described, the experimental results will be shown. The main idea is to plot the same variables than those shown in the simulation results to be able to contrast them. In the simulation results V_{th} stepped waveform was considered the output voltage of the converter. Nevertheless, this is a variable which cannot be physically measured so in the real converter the voltage in the load (voltage between *M* and *O* of Fig. 4-1) is captured in the oscilloscope instead. In the simplified diagram of Fig. 4-6 can be observed that V_{MO} and V_{th} are not exactly the same voltages because Thévenin inductance appears between them. However, taking into account the parameters of Table 4-1, as the load impedance is far larger than L_{th} the voltage drop in the latter element is negligible and therefore considering V_{MO} equal to V_{th} is an accurate approximation.

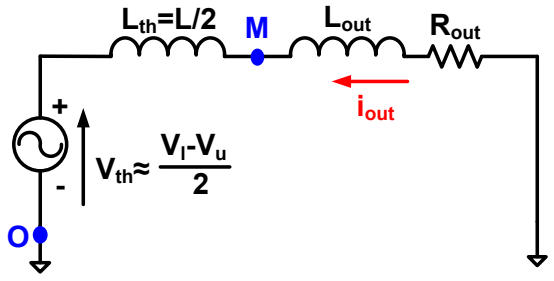


Fig. 4-6. Simplified MMC circuit applying Thévenin theorem.

4.4.1 Results with 2L submodules

In this subsection the most relevant experimental results obtained from the first laboratory model will be shown. Remember that initially the topology of the submodules was the 2L illustrated in Fig. 4-1a and Fig. 4-2 (left picture).

According to Table 4-1, the DC voltage attained in the test bench is around 540 volts, which means that during the steady state the voltage at the output of any of the six submodules should be 180 volts (capacitors balancing voltage, V_{ci}). A proper switching sequence of the submodules turns out a four levels waveform at each arm terminals as depicted in Fig. 4-7a. As expected, the steps of V_u and V_l are approximately of 180 V, totalling a maximum of V_{DC} and having an average value of $V_{DC}/2$ as anticipated in Fig. 2-27. This picture also shows the upper and lower references generated in the dSPACE board to check how closely they are tracked by their respective signals. When subtracting them as expressed in (2-8) the converter output voltage is obtained, that is, the voltage between the terminals *M* and *O* (see Fig. 4-7b). From two stepped waveforms of four levels each, another one of seven levels is achieved, V_{MO}. So, the output voltage of a converter with 6 2L submodules results in a 7 levels signal (2-87) with $V_{DC}/2$ volts of peak voltage and centred on zero. If the modulation index is reduced to i.e. $ma=0.5$ (Fig. 4-7c and Fig. 4-7d), the voltages are also reduced according to that factor and the voltage levels are the required to get the $ma \cdot V_{DC}$ and $ma \cdot V_{DC}/2$ values respectively.

Apart from the output voltage, in Fig. 4-7e the three currents which circulate through the converter are depicted. The output current i_{out} and arm currents i_1 and i_2 are determined by the load and the commanded modulation index. Although arm currents appear a bit distorted due to the submodules commutations, notice that a 5 amps perfect sinusoidal output current is achieved when $ma=1$. Moreover looking thoroughly, it can be perceived that i_1 and i_2 have got an average value which coincides with I_z (the average current along the phase from Fig. 4-7f.

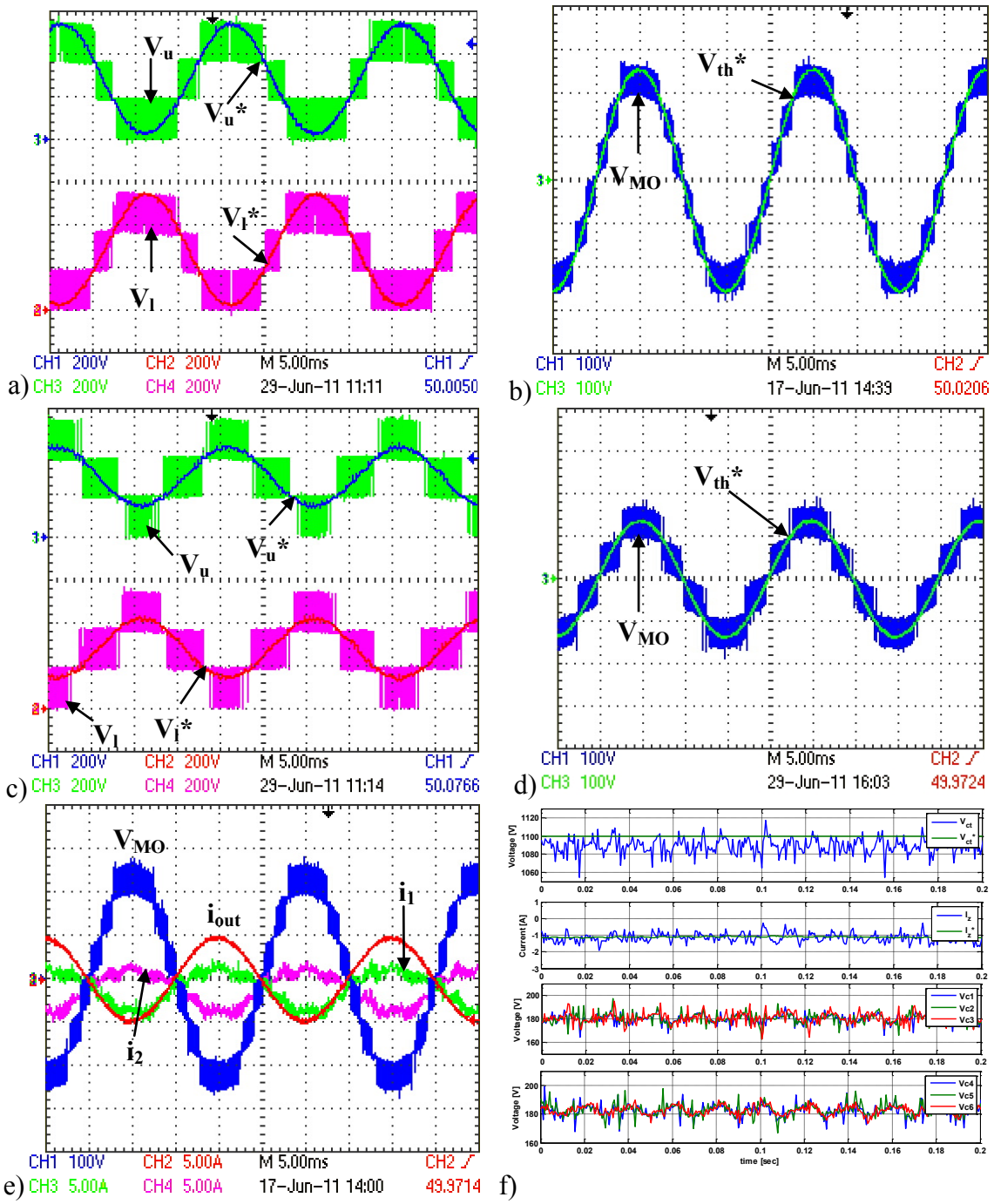


Fig. 4-7. Experimental results of a single phase Modular Multilevel Converter with 6 2L submodules. a) Upper and lower arms voltages and references. b) Output voltage and its reference being *ma=1*. c) Upper and lower arms voltages and references being *ma=0.5*. d) Output voltage and its reference being *ma=0.5*. e) Output voltage and currents. f) Control variables and capacitors measurements taken from the Control Desk software.

In Fig. 4-7f, some of the variables displayed in real time on the computer are depicted. The first graph is the sum of the six capacitor voltages illustrated in the two graphs on the bottom. Look how V_{ci} keeps more or less constant to 180 V and as a result V_{ct} is a rippled signal around 1080 volts. Despite having fixed the reference to 1100 V, the real voltage cannot attain it because remember that the DC side of the converter is obtained rectifying 380 volts from the AC grid.

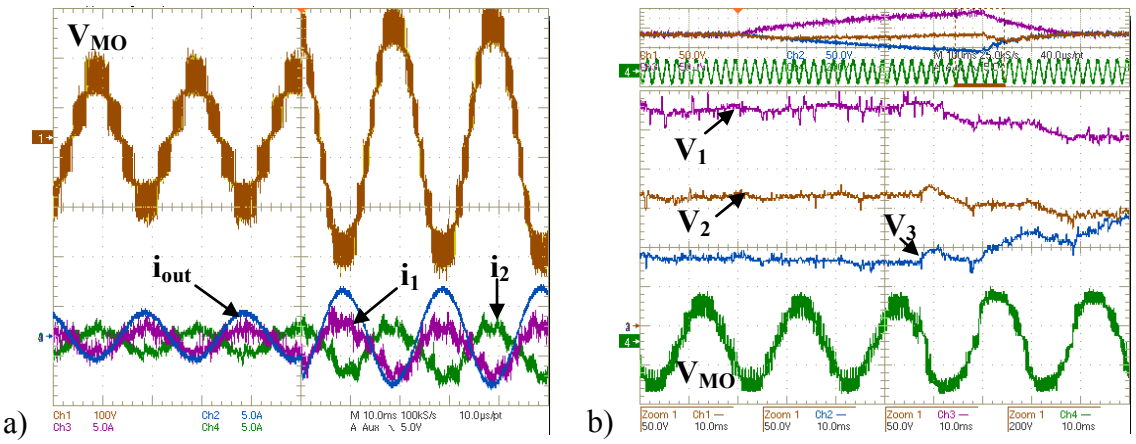


Fig. 4-8. Experimental results of a single phase Modular Multilevel Converter with 6 2L submodules. a) Transient *ma=0.5* to *ma=1*. b) Balancing of the upper arm capacitors.

After ensuring an acceptable steady state operation of the converter, the next stage is to test its behaviour during transients. For that, the modulation index is changed from 0.5 to 1 but as can be seen in Fig. 4-8a, the transient is properly performed.

To prove the proper operation of the modulation, the balancing algorithm is disabled during a short period of time. It can be observed at the top of Fig. 4-8b that initially all voltages have got the same value and after 70 ms of imbalance situation the system is able to get recovered from it. Only upper arm capacitors voltages are displayed due to the lack of input channels on the oscilloscope. However, the behaviour of the lower capacitors is exactly the same. The picture has been enlarged in the moment when capacitors voltage differs the most to point out how the output signal gets distorted.

4.4.1.1 Results with 2L submodules. A different working point

The aim of this section is to demonstrate that not only can this converter work exchanging active power but also in other working points. For this purpose, the load parameters have been changed a little bit, increasing L_{out} until 48 mH and decreasing R_{out} to 40 Ω as specified in Table 4-2. This way the load turns more inductive.

Converter parameters			
$L_u=L_l$	2 mH	V_{DC}	537 V
L_{out}	48 mH	$V_{AC\ rms}$	380 V
R_{out}	40 Ω	C_{DC}	8000 mF, 400V

Table 4-2. Parameters of the single phase MMC with 6 submodules test bench.

The effect produced by the new load in the currents is noticeable in the first four graphs of Fig. 4-9. In this case currents are some degrees ahead comparing with the former working point. Instead of being 180º phase shift between i_{out} and V_{MO}, now there is about 165º. Apart from that, the behaviour of the converter is identical. The individual

voltages from each submodule add up to form four level arm voltages (Fig. 4-9c) and at the same time V_u and V_l add up to form the seven level output voltage. The consequence of reducing the modulation index can be noticed in Fig. 4-9d where the four depicted signals are reduced to the half according to the modulation index. It is obvious that the modulation is working properly, otherwise voltage levels would be irregular. However, to verify it, the measured values are displayed in Fig. 4-9b.

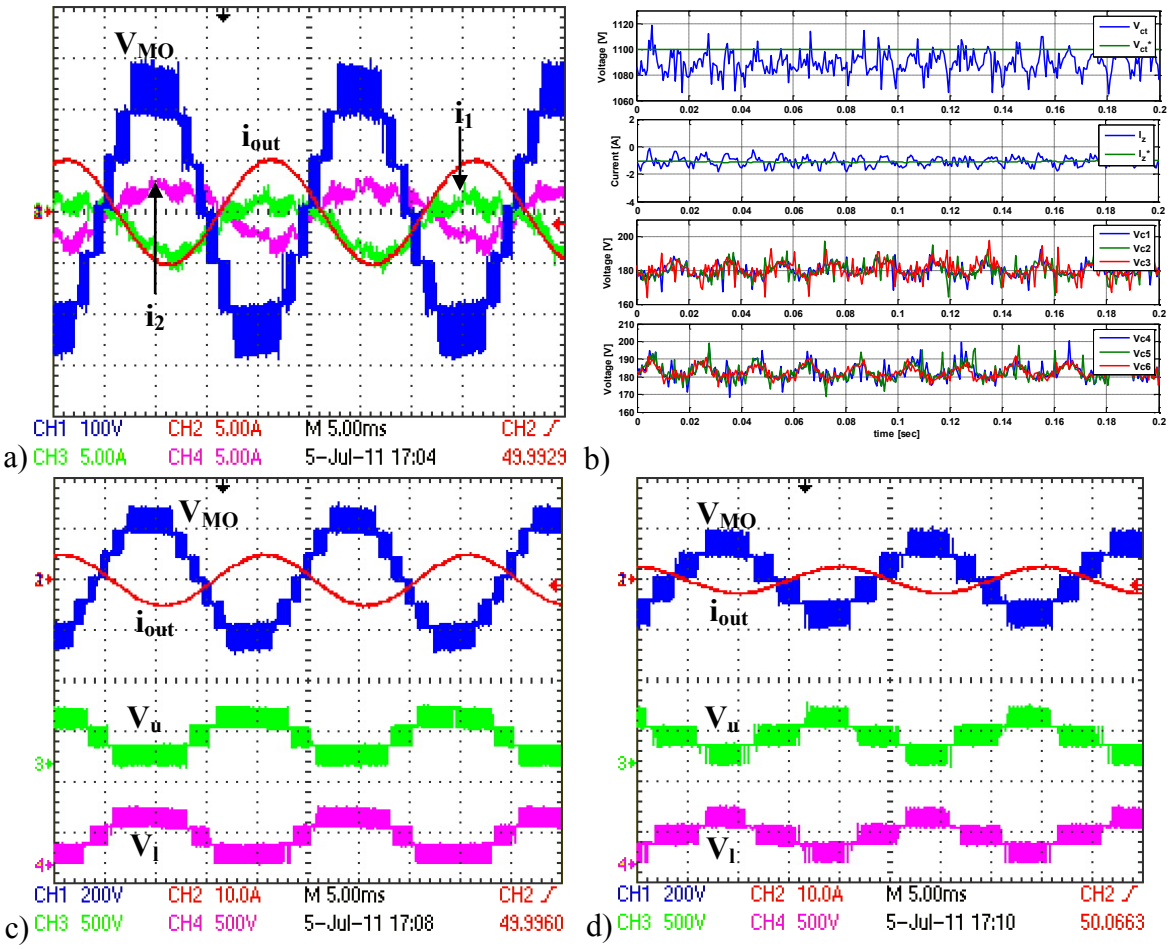


Fig. 4-9. Experimental results of a single phase Modular Multilevel Converter with 6 2L submodules being R_{out} 40 Ω and L_{out} 48 mH. a) Output voltage and currents being *ma=1*. b) Control variables and capacitors measurements taken from the Control Desk software. c) Output voltage, upper and lower arms voltages and output current being *ma=1*. d) Output voltage, upper and lower arms voltages and output current being *ma=0.5*.

4.4.2 Results with 3L-FC submodules

Once the experimental results obtained from the test bench with 2L submodules are shown, those obtained from the test bench with 3L-FC submodules (Fig. 4-1b) will be exposed.

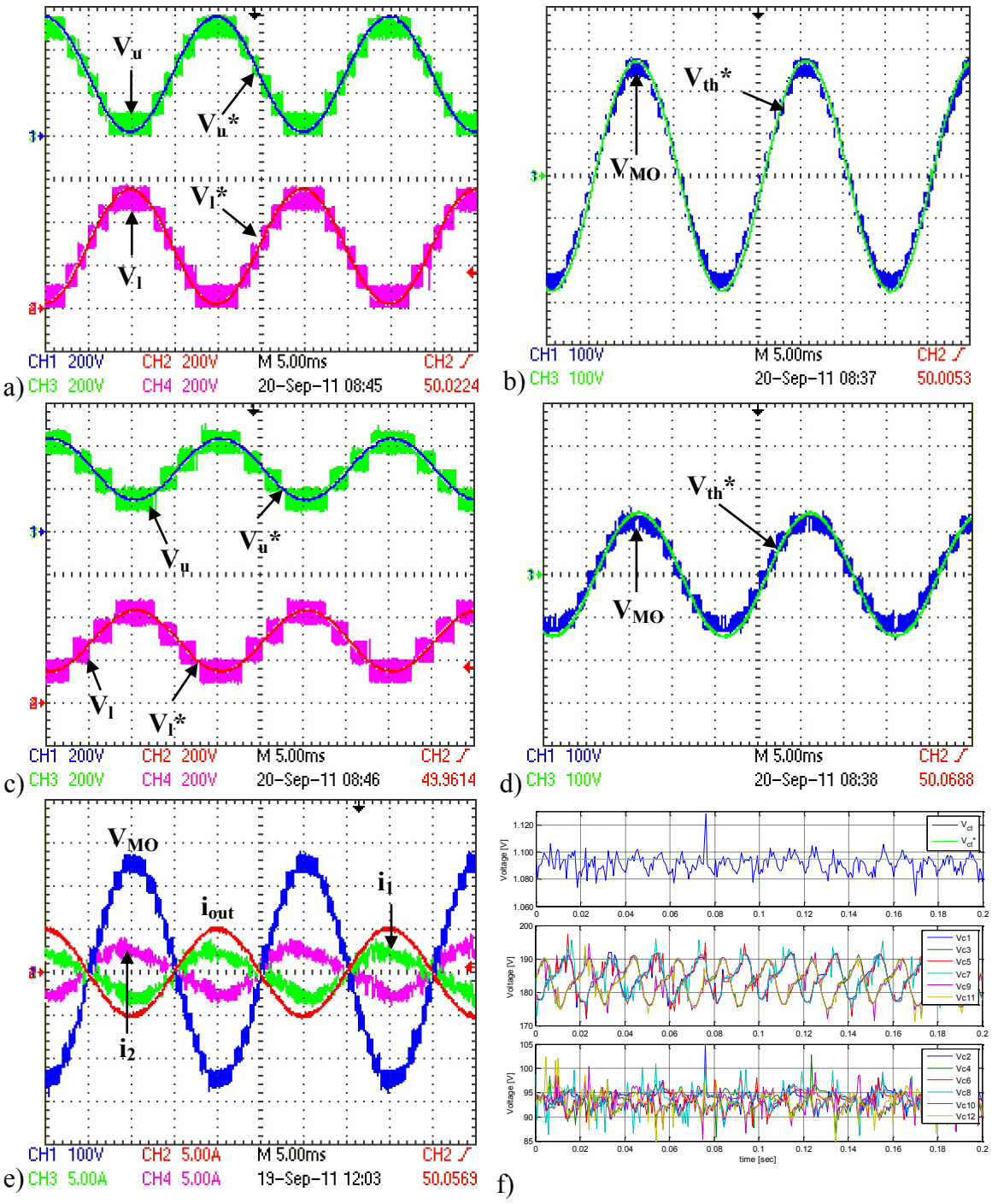


Fig. 4-10. Experimental results of a single phase Modular Multilevel Converter with 6 3L-FC submodules. a) Upper and lower arms voltages and references. b) Output voltage and its reference being *ma=1*. c) Upper and lower arms voltages and references being *ma=0.5*. d) Output voltage and its reference being *ma=0.5*. e) Output voltage and currents. f) Control variables and capacitors measurements taken from the Control Desk software.

The number of submodules of the converter remains constant but to reconfigure the submodule, the elements have been doubled and the connections have been changed. Unlike the 2L configuration, the arm voltages are formed by 7 levels (see Fig. 4-10a) instead of 3. Consequently, the individual voltages from each submodule add up to form a multilevel, now near sinusoidal 13 stepped waveform (V_{MO}), this is, $2 \cdot n+1$ as shown in

Fig. 4-10b. These two pictures are repeated in Fig. 4-10c and Fig. 4-10d but in this case the references are fixed to half of its maximum value being the modulation index 0.5 instead of 1.

Regarding the currents, in Fig. 4-10e it can be observed how the output current is a sinusoidal signal while i_1 and i_2 contain a lot of noise because of the submodules commutations. As far as capacitors voltage is concern, the last picture of Fig. 4-10 shows their measured values. It should not be forgotten that as a characteristic of this submodule topology, one of the two capacitors per submodule is charged to the half of the other's voltage. In this test bench, $V_{c1i}=2\cdot V_{c2i}$ being $V_{c1i}\approx 180V$ and $V_{c2i}\approx 90V$. However, as explained in the modelling chapter, to adjust the external control loop (the one related to the total capacitors voltage) the twelve capacitors of the converter are supposed to be charged to the same level. For this reason, just for carrying out some calculations, the greatest capacitors voltages are divided by two. Thus, the reference signal V_{ct}* is fixed to 1080 volts, this is $12\cdot V_{c2i}=12\cdot 90V$.

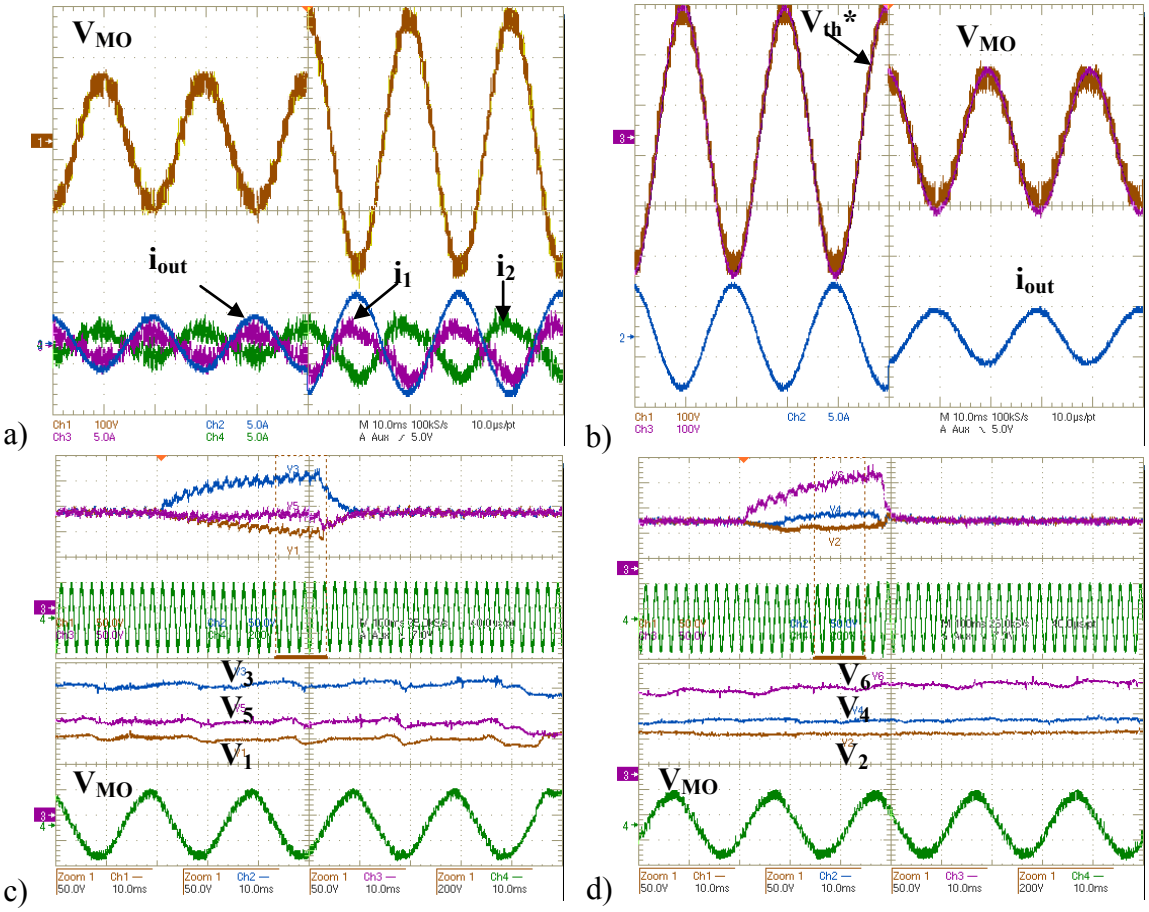


Fig. 4-11. Experimental results of a single phase Modular Multilevel Converter with 6 3L-FC submodules. a) Transient *ma=0.5* to *ma=1*. b) Transient *ma=1* to *ma=0.5*. c) Balancing of the greater upper arm capacitors. d) Balancing of the smaller upper arm capacitors.

After ensuring a satisfactory steady state operation of the converter, similar transient than in the previous configuration has been caused. First, in Fig. 4-11a the modulation index is changed from 0.5 to 1 and in Fig. 4-11b the opposite is done, *ma* is changed from 1 to 0.5. In both experiments the transient is properly performed, currents and voltages acquire an acceptable shape as well as value.

To prove the proper operation of the modulation, the balancing algorithm is disabled during 30-40 ms. It can be observed at the top of Fig. 4-11c and Fig. 4-11d that initially all voltages have got the same value, then capacitors start getting unbalanced and after the modulation being reactivated the system is able to recover rapidly from the instabilities, it takes only 10 ms to go back to the steady state. Only upper arm capacitors voltages are displayed but the behaviour of the lower capacitors is similar. In this case two figures have been plotted because the two capacitors of the same submodule acquire different values, so to clearly perceive them, those with equal V_{ci}*s* are grouped in the same picture. As can be noticed, capacitors voltages of Fig. 4-11c are two times the voltages of capacitors in Fig. 4-11d. These two pictures have been enlarged in the moment when capacitors voltage differs the most to point out how the output signal gets distorted.

4.5 Conclusions

In this chapter, the modulation strategy described in chapter 3 is implemented in a downscaled laboratory setup. This implementation has been specially designed keeping in mind that for a high voltage application, it will be necessary to control a high number of submodules.

By means of experimental results shown here, the successful simulation results of the capacitors balancing at any operation condition are corroborated with submodules 2L and 3L-FC topologies. In this way, this topologies operating with the proposed modulation method, could be useful for grid connected high power and high voltage applications such as HVDC power transmission or reactive compensator applications.

Chapter 5

Comparison of MMC with different submodules

It has been demonstrated that not only the MMC can be comprised of 2L half bridge submodules but also of multilevel submodules, without impairing the operating of the converter or hindering its implementation. So in this chapter primarily the advantages and disadvantages of using different suitable submodules concepts for the MMC topology to be used in HVDC applications will be discussed.

The submodule topologies under comparison are, apart from the three considered so far (2L, 3L-FC, 3L-NPC), the 2L half bridge with series connection of several controlled switches. The analysis includes guidelines to choose the most suitable semiconductor, accompanied with an illustrative example that compares the performances obtained with two different natures of IGTBs, one of low voltage (LV) and the other one of medium voltage (MV). Thus, the analysis will evaluate the four aforementioned submodule concepts built up with different nature of semiconductors, applying a comparison procedure that is mainly focused on a thermal analysis of the resulting converter. From that procedure, the maximum achievable output AC currents and powers under different operating conditions, such as number of submodules employed, switching frequency, modulation index, power factor, etc are deduced. In addition to this, the comparison also takes into account other aspects such as the quality of the generated waveforms and implementation complexity.

To summarize, the findings of more interest from each section are collected in a large table in order to find out easily the positive and negative aspects of each submodule topology.

5.1 Output voltage analysis of MMC topology

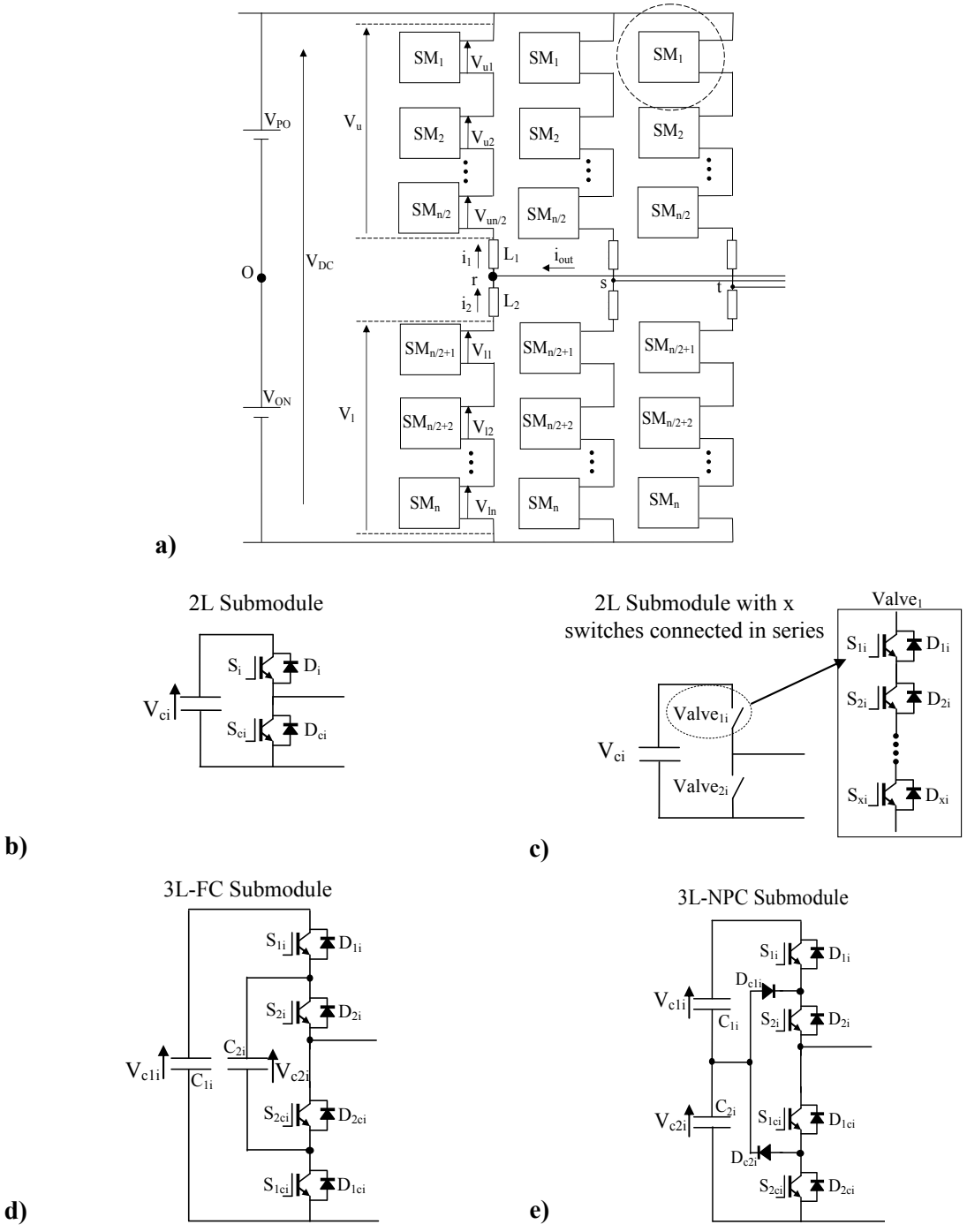


Fig. 5-1. Diagram of the three phase Modular Multilevel Converter (MMC) with an undefined number of submodules and types. a) MMC converter, b) 2L submodule concept, c) 2L submodule with series connection of IGBTs concept, d) 3L-FC submodule concept, e) 3L-NPC submodule concept.

This section compares the submodule topologies under study presented in Fig. 5-1 in terms of output AC voltage quality. Note that apart from the three submodule topologies that have been analysed in the previous chapters, from now on the 2L submodule topology with several switches connected in series will be as well considered.

Taking into account that in HVDC applications, the operating voltages are relatively high, for instance from 100kV (could be ±50kV) up to even 640kV (could be ±320kV) at DC side, the required number of semiconductors in the arrangement of the converter will also be high. This situation from an optimistic perspective can be understood as advantageous in MMC topologies, for the reason that although a high number of submodules are required to reach these high voltages, multilevel AC waveforms of good quality or low distortion ratios are achieved. Therefore, this study is focused on the quality of the V_{th} waveform according to two main parameters: the switching frequency and the number of submodules used. The analysis is carried out under an idealized scenario [89], with classical PWM modulation methods, not considering the balancing algorithm of the DC bus voltage capacitors explained in chapter 3. Note that this scenario, simplifies the evaluation and easies the understanding, without loss of generality or representativeness.

5.1.1 MMC topology with different submodule concepts

As the Modular Multilevel Converter with different submodule concepts has already been described, the outing voltage characteristics have been detailed. But in this section all that information is gathered and deeply analysed.

Initially, 2L submodule topology represented in Fig. 5-1b and 2L with series connection of switches submodule topology illustrated in Fig. 5-1c will be analyzed. All the graphics in Fig. 5-2a and Fig. 5-2b have been taken from a single phase MMC simulation with 4 submodules in total (2 in the upper arm and 2 more in the lower arm). It is supposed that the same type of semiconductors is utilized but not the number of them. In the second topology (Fig. 5-2b), two semiconductors (IGBTs and diodes) are considered in series connection per valve which makes up in total 8 of each meanwhile in the 2L topology only four.

$$V_i = \frac{V_{DC}}{n/2} \tag{5-1}$$

In those figures, first the two references (V_u^* and V_l^*) and the corresponding triangular carrier signals to generate the firing orders are depicted. Then both upper and lower arms output voltage, V_u and V_l are shown. Each one consists of *(n/2+1)* levels of V_i volts as expressed in (5-1) in which *n* is the number of submodules per phase. The last

graphic of Fig. 5-2, represents the output voltage of one phase of the converter V_{th}. This voltage is characterized by its *(n+1)* voltage levels of $V_i/2$ volts.

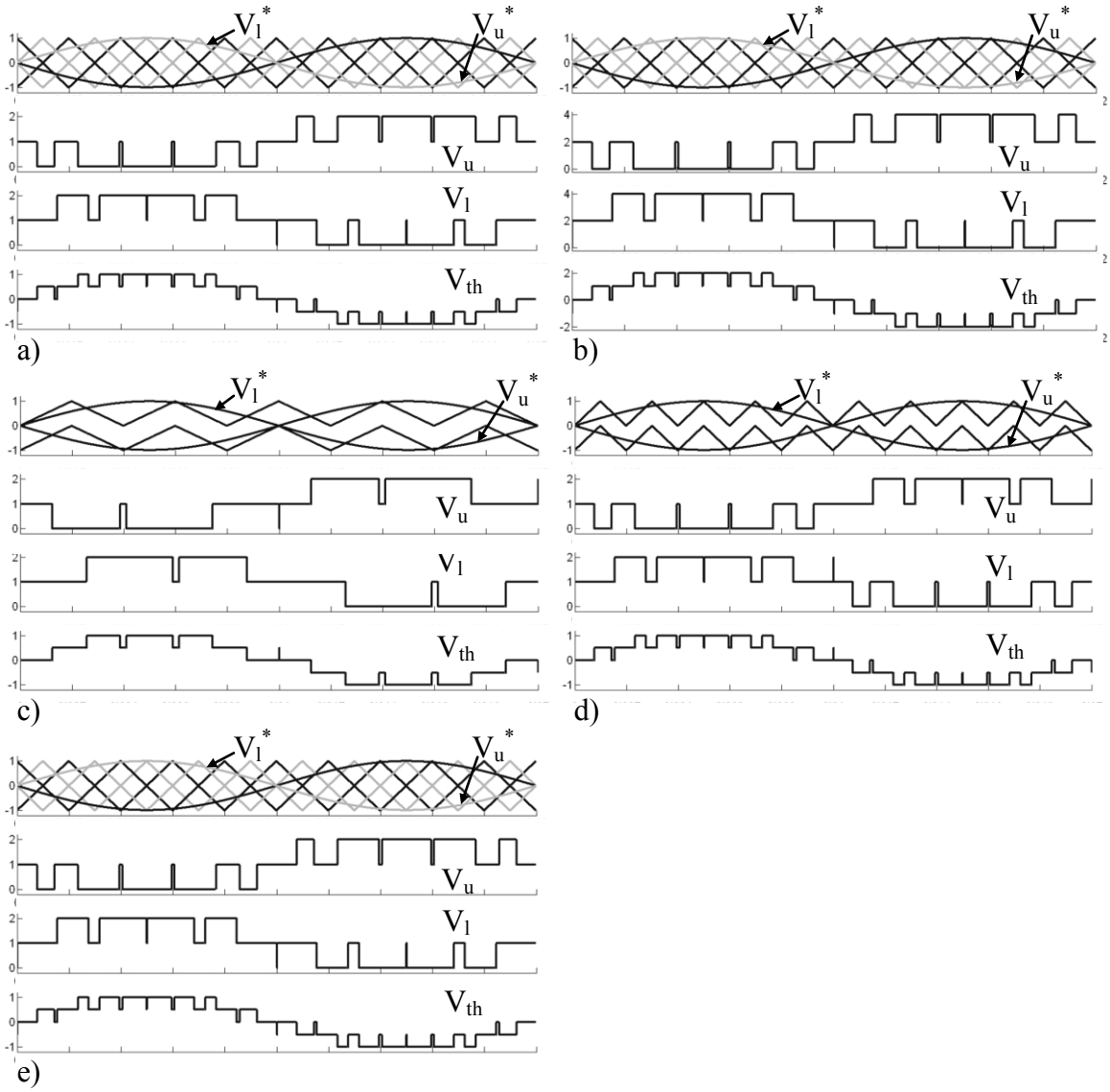


Fig. 5-2. Normalized triangular and reference signals, V_u, V_l and V_{th} of different MMC configurations (all with same semiconductor). a) 4 2L concept submodules at f_{sw}=250 Hz. b) 2 2L concept submodules with series connection of 2 switches at f_{sw}=250 Hz. c) 2 3L-NPC concept submodules at f_{sw}=250 Hz. d) 2 3L-NPC concept submodules at f_{sw}=500 Hz. e) 2 3L-FC concept submodules at f_{sw}=500 Hz.

The fact of serializing 2 semiconductors in each valve lead us to chose the voltage of the capacitor double for the configuration of Fig. 5-2 b, in order to set equal voltage at each semiconductor allowing to operate them at the collector-emitter 100 FIT (Failure In Time rate) voltage *($V_{ce@100FIT}$)*. Consequently, the relation of amplitude voltages for V_u, V_l and V_{th} are double in Fig. 5-2b than in Fig. 5-2a, but the appearance of the obtained waveforms is equal. To sum up, for a determined number of submodules in the converter, with the series connection of semiconductors submodule topology voltage

amplitude is gained at the expense of increasing the number of elements while the wave shape keeps unaltered.

On the other hand, Fig. 5-2c and Fig. 5-2d are the corresponding waveforms, for a 3L-NPC submodule concept. In this case, they represent a single phase MMC simulation with 2 submodules in total (1 in the upper arm and 1 more in the lower arm). Once again, it is supposed that the same type of semiconductor as in the previous two configurations is utilized. Consequently, equal V_{DC} voltage is needed for configurations of Fig. 5-2a, Fig. 5-2c and Fig. 5-2d. The same number of controlled switches is also necessary (except for the clamping diodes) for these configurations. Due to the nature of a 3L-NPC submodule, in Fig. 5-2c, the triangular signals needed are level shifted and their frequency (f_{sw}) is fixed to equal value as in Fig. 5-2a. As a result, unlike the previous cases, its output waveform differs from the one in Fig. 5-2a. However, by doing two times greater the triangular frequency of the MMC with 3L-NPC submodule concept, a curious effect shown in Fig. 5-2d is appeared: the same output voltages V_u, V_l and V_{th} as in configuration of Fig. 5-2a are achieved.

Finally, if MMC converter with submodules based on 3L-FC topology is utilized with equivalent philosophy than the 3L-NPC submodules, the obtained output voltage results are exactly equivalent to the MMC converter with 2L submodule concept. Naturally, to obtain the output waveforms of Fig. 5-2a for instance by using 3L-FC submodules, only 2 submodules in total (1 in the upper arm and 1 more in the lower arm) should be used and their corresponding triangular signals (and frequencies) should be equal as shown in Fig. 5-2a. Note that in this particular case, the number of semiconductors of both configurations would be also equal (2L and 3L-FC).

5.1.2 Output voltage quality analysis

Keeping in mind that V_{th} is a multilevel waveform whose number of levels depends on the number of submodules per phase, and f_{1hb} depends on the switching frequency, it is predictable that the quality of the signal will improve as these two parameters increase. Thus, next the evolution of the quality of MMC waveforms is going to be analyzed according to the chosen n and f_{sw}. For that, the total harmonic distortion (THD) of V_{th} (5-2) and the weighted total harmonic distortion (WTHD) (5-3) will be calculated (without the injection of the third harmonic) for a 2L submodule based MMC. After that, the results are extrapolated to the studied submodule concepts.

$$THD_v[\%] = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^{\,2}}}{V_1} \cdot 100 \tag{5-2}$$

$$WTHD_v[\%] = \frac{\sqrt{\sum_{h=2}^{\infty} \left(\frac{V_h}{h}\right)^2}}{V_1} \cdot 100 \tag{5-3}$$

Observing Fig. 5-3 it can be noticed that both THD and WTHD decrease exponentially as n increases, meanwhile the fundamental value of the analyzed signal remains constant in all the cases with a little ripple lower than 0.2%. Furthermore while f_{sw} rises, WTHD presents a downward trend. It does not happen the same in the case of THD which keeps more or less stable regardless of the frequency.

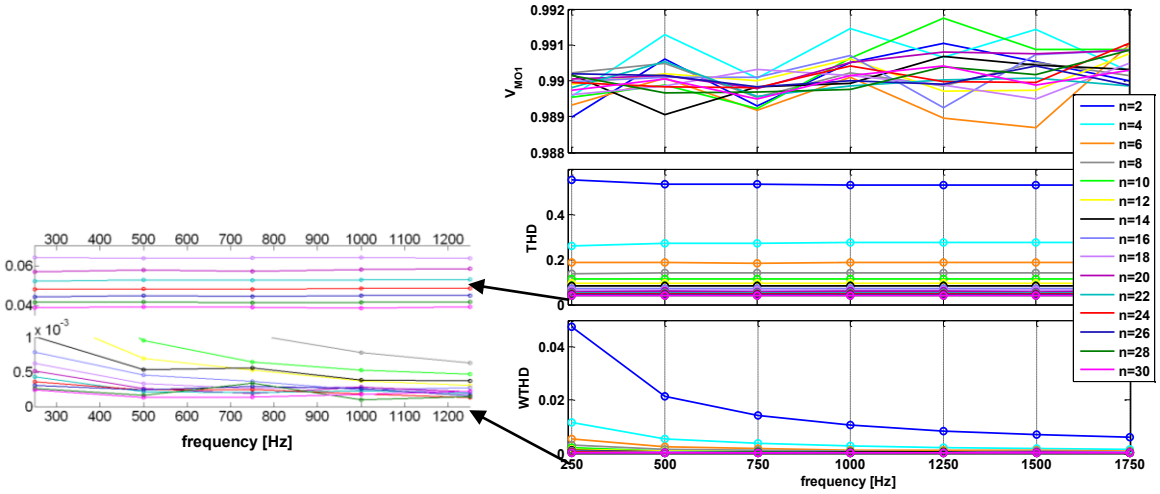


Fig. 5-3. Fundamental voltage, THD and WTHD of V_{th}, in a 2L submodule MMC converter according to the number of submodules and the switching frequency.

It could be natural to think that the THD has to change due to the switching frequency, enhancing with higher f_{sw}. However, looking at the spectrum of the same converter but at two different switching frequencies (Fig. 5-4, Fig. 5-5) it can be seen how the amplitude of the harmonic bands hardly change one another. The reason is that in the THD rate calculation the frequency is not taken into account (5-2).

On the other hand, the switching frequency does have influence on the WTHD rate. Although the amplitude of the harmonic bands in Fig. 5-4 and Fig. 5-5 are almost the same, the frequency where those harmonic bands appear is different, 12.5 kHz and 17.5 kHz respectively. WTHD is a weight calculation of THD which means that the lower harmonics have got more importance. Therefore, in a particular MMC with n submodules, the converter whose f_{sw} is the lowest will obtain the lowest WTHD rate.

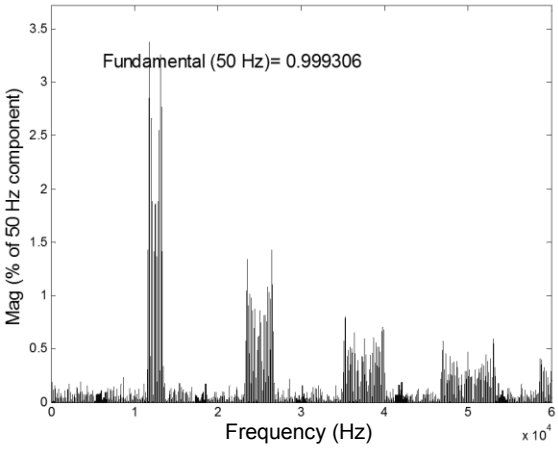


Fig. 5-4. Spectrum of a 2L submodule MMC where *n=10* and f_{sw}*=1250 Hz.*

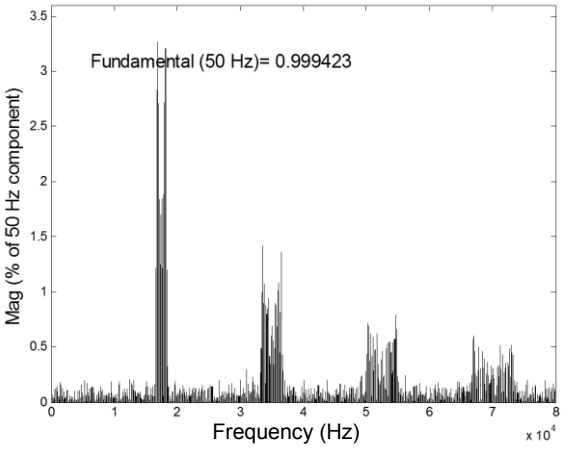


Fig. 5-5. Spectrum of a 2L submodule MMC where *n=10* and f_{sw}*=1750 Hz.*

To have a quick overview of the obtained voltage waveforms with such high number of submodules as required in HVDC applications, when Fig. 5-6 is compared with Fig. 5-7, the quality difference is not so remarkable (30 total submodules against 60), both can be accepted as very good quality signals (note that the output current quality would be improved due to the effect of the inductances of the MMC converter).

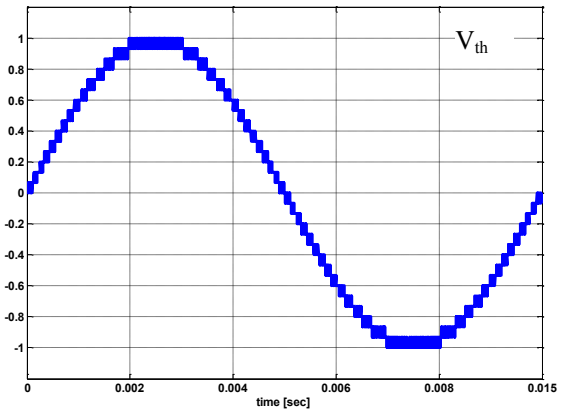


Fig. 5-6. V_{th} in a 2L submodule MMC where *n=30*, V_{DC}*=2* volts and f_{sw}*=500 Hz.*

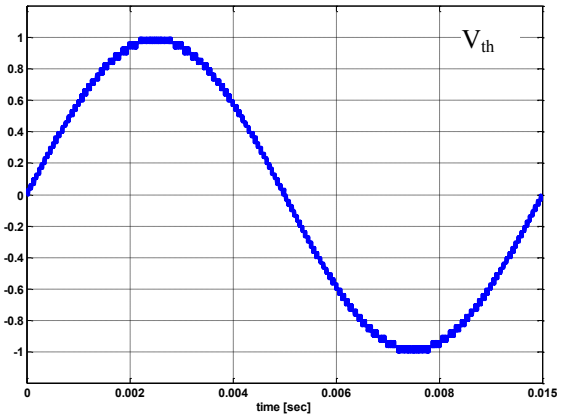


Fig. 5-7. V_{th} in a 2L submodule MMC where *n=60*, V_{DC}*=2* volts and f_{sw}*=500 Hz.*

Therefore, Table 5-1 gathers some representative numerical examples. THD, WTHD and achievable total DC bus voltage *(V_{DC})* of the MMC, with 2L, 3L-NPC and 3L-FC submodule concepts, according to *n* at fixed switching frequencies. It should be remarked, that the three submodule concepts obtain exactly the same voltage waveform at the conditions covered in the table. Thus, if for instance a MMC to a fixed DC voltage of 112kV is needed, it would be necessary to use 80 submodules of 2L concept, achieving a WTHD of 0.0873e-3 being f_{sw}*=500 Hz*. Equivalently, with 40 submodules

of 3L-NPC (at f_{sw}=*1000 Hz*) or 3L-FC (at f_{sw}=*500 Hz*), exactly the same results in terms of output AC voltage V_{th} would be obtained.

	2L SUBMODULE CONCEPT, AT F_{SW}=500 HZ							
	SUBMODULES PER ARM OF MMC							
	16	**32**	**48**	**64**	**80**	**96**	**112**	**128**
THD	0.071857	0.036475	0.024405	0.018421	0.014533	0.012054	0.010428	0.009094
WTHD	0.4587e-3	0.1908e-3	0.1889e-3	0.1157e-3	0.0873e-3	0.1251e-3	0.0359e-3	0.0880e-3
TOTAL V_{DC} (KV)	22.4	44.8	67.2	89.6	112	134.4	156.8	179.2
	8	**16**	**24**	**32**	**40**	**48**	**56**	**64**
	SUBMODULES PER ARM OF MMC							
	3L-NPC SUBMODULE CONCEPT, AT F_{SW}=1000 HZ AND 3L-FC SUBMODULE CONCEPT, AT F_{SW}=500 HZ							

Table 5-1. Output voltage quality *(V_{th})* comparison of different submodule concepts at *modulation index=1* (all topologies use the same semiconductor being its $V_{CE@100FIT}$=2.8kV).

On the other hand, Table 5-2 shows that with 2L submodule concept with series connection of 8 semiconductors, if the same DC voltages as in Table 5-1 are needed, obviously less number of submodules are required but achieving poorer quality of the output voltages. Thus, in order to achieve 112kV of total DC bus voltage for instance, there are only 10 submodules needed, obtaining a WTHD of 0.000958 with f_{sw}=*500 Hz*. However, a later analysis of this document shows that with still higher required DC bus voltages, this last configuration can be very useful, since the achieved output voltage quality can be reasonably accepted as very good, reducing the number of submodules needed.

	2L SUBMODULE CONCEPT WITH SERIES CONNECTION OF 8 SWITCHES, AT F_{SW}=500 HZ							
	SUBMODULES PER ARM OF MMC							
	2	**4**	**6**	**8**	**10**	**12**	**14**	**16**
THD	0.533203	0.269346	0.187230	0.140897	0.114450	0.094864	0.081400	0.071857
WTHD	0.021375	0.005544	0.002525	0.001480	0.000958	0.000695	0.000533	0.000458
TOTAL V_{BUS} (KV)	22.4	44.8	67.2	89.6	112	134.4	156.8	179.2

Table 5-2. Output voltage quality *(V_{th})* of 2L submodule concept with series connection of 8 switches per valve, at f_{sw}=*500 Hz* (being $V_{CE@100FIT}$=*2.8kV* of all semiconductors).

For the beyond analysis, it is established *WTHD=0.1908e-3*, corresponding to 32 submodules of 2L concept (approximately the waveform of Fig. 5-6), as the quality of waveform that provides very good converter currents quality exchange.

5.2 Output current capacity analysis of MMC topology

The following step implies the maximum output current capacity deduction. This maximum achievable output current, depends on the semiconductor nature itself, the

topology of the converter (the way and conditions where the semiconductors are arranged) and the manner in which the semiconductors are switched during the operation of the converter. Therefore, in this section the maximum achievable output current (i_{out} of Fig. 5-1, from now on $I_{ph,rms,1}$) evolution versus the switching frequency (f_{sw}) based on the procedure explained in [89] is analyzed. It is carried out for various working conditions of the MMC, two different semiconductors and also the different submodules configurations presented in Fig. 5-1. This maximum output current characteristic versus switching frequency is going to be evaluated considering these two limits:

1. The semiconductor current thermal limit ($I_{ph,rms,1}$), which is imposed by the maximum admissible semiconductor junction temperature ($T_{j,max}$). The T_j of all the semiconductors of the converter must be evaluated in order to find out which component settles the thermal limit under the considered operating conditions.
2. The maximum semiconductor current is restricted by its Safe Operating Area, which is influenced by the semiconductor switching conditions (DC voltage, driving characteristics, parasitic elements, etc.). This limit is a constant value (I_{max_SOA}) not influenced by the f_{sw}. This I_{max_SOA} limits the whole converter output maximum current, henceforth, called (5-4):

$$I_{ph,rms,1.max} = I_{max\_SOA} / \sqrt{2} \tag{5-4}$$

In order to obtain the thermal output limit, the use of five ($f_{sw,max}$,$I_{ph,rms,1}$) simulations points provides a good computation versus error, trade off when obtaining $I_{ph,rms,1}=f(f_{sw})$. As simulating three f_{sw} points per $I_{ph,rms,1}$ is more than enough to obtain the T_j evolution, this implies the need of only 15 simulations for the same procedure input conditions. The chosen frequency and current values are:

- f_{sw}= 500 Hz, 1000 Hz, 1450 Hz.
- $I_{ph,rms,1}$= 121.3 A, 414.2 A, 707.1 A, 1000 A, 1292.9 A, 1585.8 A. (note that the semiconductor temperature is evaluated even at higher currents than the I_{max_SOA}).

5.2.1 Semiconductors

Two commercial IGBT modules are selected for the analysis, SEMIC. A: Infineon DBFS450R17KE3 [90] used in low voltage (LV) applications and SEMIC. B: ABB 5SNA1200G450300 [91] usually used in medium voltage (MV). However, the maximum collector current of both of them is the same, 1.2 kA.

The first one (SEMIC. A), consists of a series connected two IGBT-Diode pair. Therefore by means of this module a half bridge converter topology can be formed (one 2L submodule). At the same time, each equivalent semiconductor is composed of 3 components in parallel. Thanks to this configuration the current through the module is shared out among the three internal components, so that it can reach up to 1.2kA. This module's $V_{CE@100FIT}$ voltage is assumed to be 900V. Nonetheless, [92] has already checked that it can work at 1100V without putting at risk its integrity. This is why from now on this voltage will be considered 1100 volts. The second one (SEMIC. B), withstands 1.2kA too but regarding the semiconductor collector-emitter voltage, it nearly resists 3 times Infineon's being its $V_{CE@100FIT}=2800$ volts.

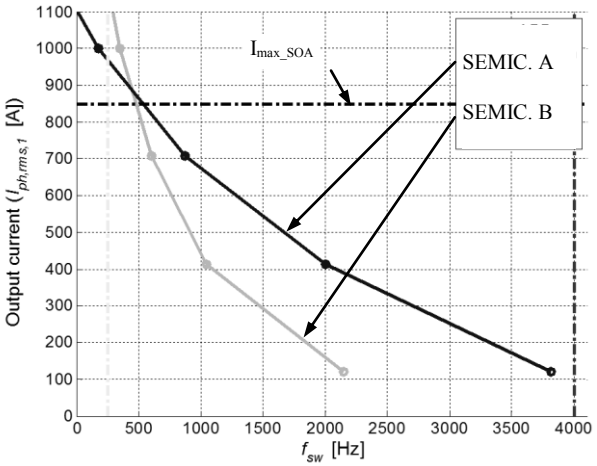
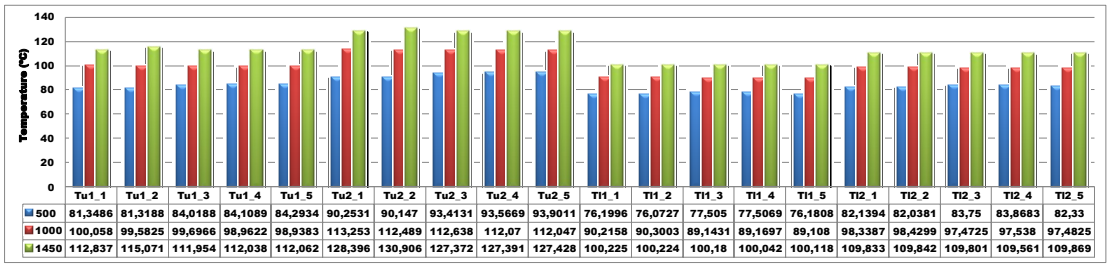


Fig. 5-8. $I_{ph,rms,1}=f(f_{sw})$ characteristics in a MMC with different semiconductors, $n=16$, $ma=1$, $cos(\varphi)=1$ and submodule concept of Fig. 5-1b.

The nature and switching characteristics of both semiconductors are quite different, yielding to two maximum achievable output current characteristics quite different too, as depicted in Fig. 5-8 [89], it is seen that SEMIC. B is more restraining when the switching frequency is higher than roughly 500 Hz, what means that this semiconductor is designed to preferably work at low frequencies. Apart from the curves that define the output current characteristic versus switching frequency, in Fig. 5-8 three limits are included. The horizontal black line represents SOA current whose value in this case is

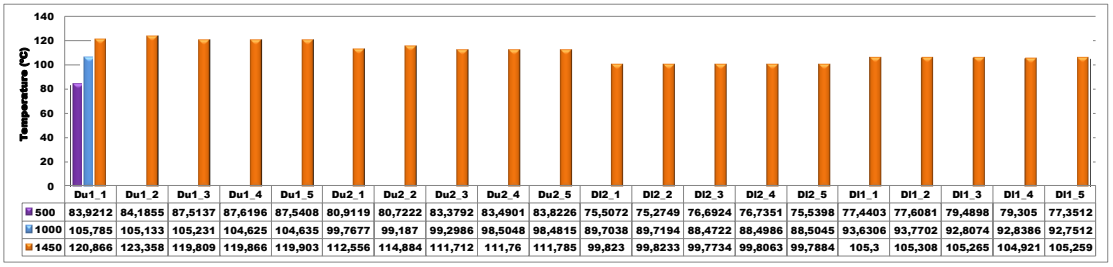
1200/√2 = 848.5A. On the other hand, the limits on the frequency axes are imposed by the minimum switching frequency (250 Hz defined according to the output voltage quality) and the maximum (4 kHz defined ideally according to the minimum microprocessor sampling time). Despite at switching frequencies lower than 500 Hz, the thermal limit allows operating at higher currents than the maximum SOA current, it is preferable not to overtake this limit. Thus, the point where the current capacity is maximized for both semiconductors is similar: around 600 Hz for SEMIC. A and around 500 Hz for SEMIC. B.

a)



	Tu1_1	Tu1_2	Tu1_3	Tu1_4	Tu1_5	Tu2_1	Tu2_2	Tu2_3	Tu2_4	Tu2_5	Tl1_1	Tl1_2	Tl1_3	Tl1_4	Tl1_5	Tl2_1	Tl2_2	Tl2_3	Tl2_4	Tl2_5
500	81,3486	81,3188	84,0188	84,1089	84,2934	90,2531	90,147	93,4131	93,5669	93,9011	76,1996	76,0727	77,505	77,5069	76,1808	82,1394	82,0381	83,75	83,8683	82,33
1000	100,058	99,5825	99,6966	98,9622	98,9383	113,253	112,489	112,638	112,07	112,047	90,2158	90,3003	89,1431	89,1697	89,108	98,3387	98,4299	97,4725	97,538	97,4825
1450	112,837	115,071	111,954	112,038	112,062	128,396	130,906	127,372	127,391	127,428	100,225	100,224	100,18	100,042	100,118	109,833	109,842	109,801	109,561	109,869

b)



	Du1_1	Du1_2	Du1_3	Du1_4	Du1_5	Du2_1	Du2_2	Du2_3	Du2_4	Du2_5	Dl2_1	Dl2_2	Dl2_3	Dl2_4	Dl2_5	Dl1_1	Dl1_2	Dl1_3	Dl1_4	Dl1_5
500	83,9212	84,1855	87,5137	87,6196	87,5408	80,9119	80,7222	83,3792	83,4901	83,8226	75,5072	75,2749	76,6924	76,7351	75,5398	77,4403	77,6081	79,4898	79,305	77,3512
1000	105,785	105,133	105,231	104,625	104,635	99,7677	99,187	99,2986	98,5048	98,4815	89,7038	89,7194	88,4722	88,4986	88,5045	93,6306	93,7702	92,8074	92,8386	92,7512
1450	120,866	123,358	119,809	119,866	119,903	112,556	114,884	111,712	111,76	111,785	99,823	99,8233	99,7734	99,8063	99,7884	105,3	105,308	105,265	104,921	105,259

Fig. 5-9. Temperatures of all the semiconductors (SEMIC. A) of one arm, for a MMC with *n*=10, m_a=*1*, *cos(φ)=1*, with 2L submodule concept at equal current and at 3 different switching frequencies. A) IGBTs, b) Diodes.-

Note that the corresponding DC bus voltages and the output AC fundamental voltages are different for each configuration. In each configuration, the DC voltage of each submodules capacitor is ideally fixed to 1100V and 2800V respectively, while the number of submodules is equally fixed to 16. Consequently, the maximum achievable output power is also different for both converter configurations. However, the switching frequency at which the semiconductor reaches the maximum current is found. In both cases, T_{u2} is the most restrictive semiconductor (see Fig. 5-1b, with *u* denoting upper arm), achieving the highest temperature in all the cases. It must be pointed out that the MMC topology presents a strong symmetry between submodules. Thus, as noticed in the evaluation of temperatures summarized in Fig. 5-9, within the upper arm for instance, semiconductor T_{u1} of all the submodules reaches very similar temperature (the only difference is due to non-linear effects such as dead times, or minimum conduction times of semiconductors). Equal behaviour is also obtained, with the rest of the semiconductors T_{u2}, D_{u1} and D_{u2}, reaching very similar temperature at every submodule of the upper arm. Finally, in an equivalent way, this symmetry is also present at the

lower arm (see Fig. 5-1b, with *l* denoting lower arm), being the temperatures of each semiconductor (T_{l1}, T_{l2}, D_{l1} and D_{l2}) very similar at each submodule.

Finally, it must be remarked that in order to perform a uniform comparison, the arm currents i_1 and i_2 are maintained of sinusoidal shape (plus an offset when active power is transmitted and the high frequency ripple), as simplified illustrated in Fig. 2-27 by the appropriate control strategy [80], [93], [84].

5.2.2 Output current analysis at different modulation indexes

The objective of this subsection is to find out which the modulation index that cause higher temperature on the semiconductors is, in short, which the most restrictive modulation index in terms of temperature is. The curves of Fig. 5-10 and Fig. 5-11 are obtained applying the aforementioned procedure to a single phase MMC with SEMIC.A and SEMIC. B respectively. These models were simulated with three different modulation indexes: 1, 0.8 and 0.6. It must be specified that *ma=1* is assumed to be as in (5-5) where V_{DC} is the total DC bus:

$$\mathrm{ma} = \frac{2\cdot\sqrt{2}}{1.15\cdot\sqrt{3}}\cdot\frac{\mathrm{V_{LL,rms,1}}}{\mathrm{V_{DC}}} \tag{5-5}$$

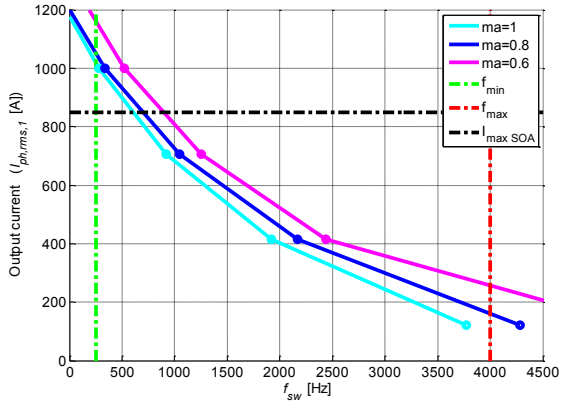


Fig. 5-10. $I_{ph,rms,1}=f(f_{sw})$ characteristics with different modulation indexes, *n=20*, *cos(φ)=1* and submodule concept of Fig. 5-1b (SEMIC. A).

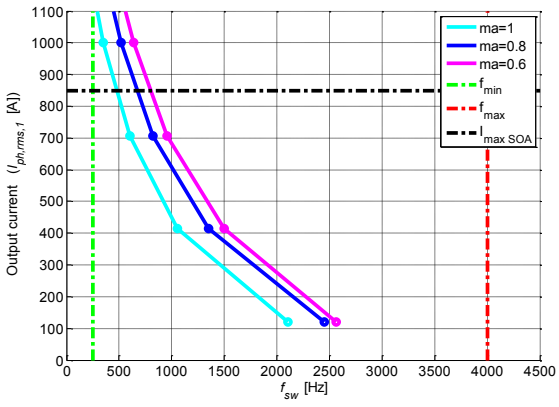


Fig. 5-11. $I_{ph,rms,1}=f(f_{sw})$ characteristics with different modulation indexes, *n=12*, *cos(φ)=1* and submodule concept of Fig. 5-1b (SEMIC. B).

It can be noticed that in both cases the most restrictive characteristic belongs to the simulation with highest modulation index, while the less restrictive belongs to that whose modulation index is the lowest, *ma=0.6*. This effect is related to the influence of the conduction time of the semiconductors. Thus, from a design point of view, if the

converter must operate in all the range of modulation indexes, the switching frequency must be fixed no higher than 500 Hz - 600 Hz (depending on the semiconductor), enabling to reach the maximum output current of 848.5A. It must be pointed out that in all the cases, the most restrictive semiconductor is T_{u2}, since all the submodules of each arm presents equivalent behaviour. Note that this converter topology presents a very symmetric behaviour, since at given operating conditions, T_{u1}, T_{u2}, D_{u1} and D_{u2} of all submodules present equivalent power losses and consequently, equivalent thermal behaviour.

5.2.3 Output current analysis at different *cos(φ)*

In this subsection, the same procedure is applied to a MMC converter where the phase shift between output current and voltage is changed, in order to find out the influence of *cos(φ)* on the maximum achievable output current of the converter. In the previous subsection, $m_a=1$ has been found to be the most restricting modulation index. Therefore, from now on simulations will be always performed considering the worst case, $m_a=1$.

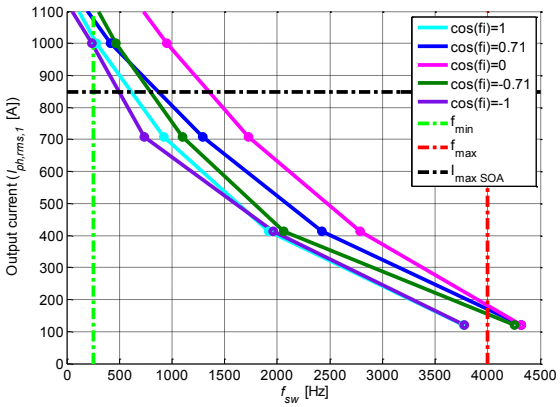


Fig. 5-12. $I_{ph,rms,1}=f(f_{sw})$ characteristics with *n=20*, *ma=1* at different *cos(φ)* with SEMIC. A and submodule concept of Fig. 5-1b.

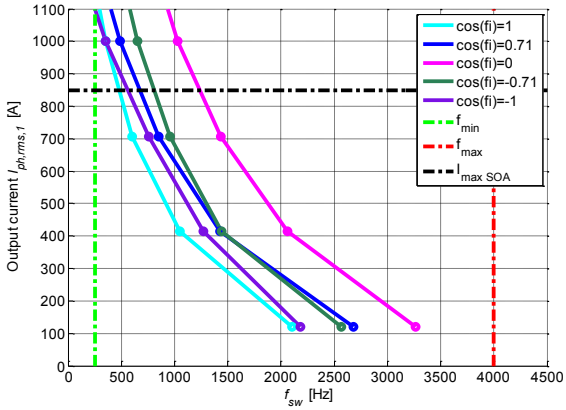


Fig. 5-13. $I_{ph,rms,1}=f(f_{sw})$ characteristics with *n=12*, *ma=1* at different *cos(φ)* with SEMIC. B and submodule concept of Fig. 5-1b.

Five angles have been assigned to *φ*: 0º, 45º, 90º, 135º and 180º. Fig. 5-12 and Fig. 5-13 show the obtained maximum output current characteristic for each phase shift. Notice that for each case, the active and reactive power exchange through the converter is different. Remember that at the highest active power exchange, in i_1 and i_2 currents an offset value (i_z) appears. The higher the active power exchange is, the higher is this offset current value, provoking a greater overall current seen by the submodules. This fact mainly determines the average temperature differences of semiconductors at different *cos(φ)*. Thus, the switching frequency at which the converter reaches the

maximum SOA limit in function of *cos(φ)* is summarized in Table 5-3 for the used two semiconductors. If all the range of phase shifts at maximum current exchange wants to be guaranteed, the selected switching frequency of the converter should be fixed around 500 Hz.

Cos(φ)	$f_{sw\ max}$ (SEMIC. A)	Most restrictive semiconductor
1	612 Hz	T_{u2}
0.7	868 Hz	T_{u2}
0	1353 Hz	D_{u2}, D_{l1} (slight ΔT^a between semiconductors)
-0.7	793 Hz	D_{u2}
-1	495 Hz	D_{u2}
cos(φ)	**$f_{sw\ max}$ (SEMIC. B)**	**Most restrictive semiconductor**
1	480 Hz	T_{u2}
0.7	677 Hz	T_{u2}
0	1236 Hz	T_{u2}, T_{l1} (slight ΔT^a between semiconductors)
-0.7	812 Hz	D_{u2}
-1	560 Hz	D_{u2}

Table 5-3. Summary of obtained results at different *cos(φ)* and semiconductor.

5.2.4 Output current analysis with different number of submodules

The aim of this analysis lies in investigating whether the switching frequency which makes better usage of the semiconductors is altered by the number of submodules arranged in the MMC converter. The abovementioned procedure is used again to obtain $I_{ph,rms,1}=f(f_{sw})$ curves according to the number of submodules in the converter but this time being $m_a=1$ and $cos(\varphi)=1$. The submodules capacitor voltage is left constant, so that, what changes with the number of submodules is the fundamental AC output voltage of the converter.

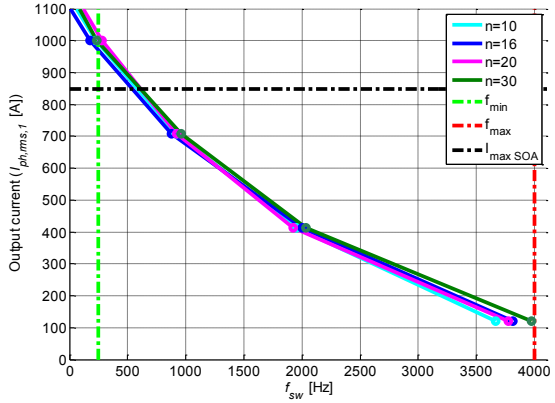


Fig. 5-14. $I_{ph,rms,1}=f(f_{sw})$ characteristics in a MMC with *n=10, 16, 20 and 30* using SEMIC. A, $m_a=1$ and $cos(\varphi)=1$.

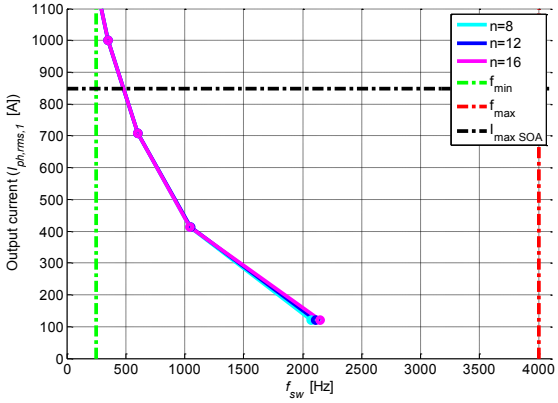


Fig. 5-15. $I_{ph,rms,1}=f(f_{sw})$ characteristics in a MMC with *n=8, 12 and 16* submodules per arm using SEMIC. B, $m_a=1$ and $cos(\varphi)=1$.

In Fig. 5-14 the output current versus the switching frequency characteristics in a single phase MMC with 10, 16, 20 and 30 submodules are depicted. It can be noticed that due

to the strong symmetry of this converter topology there is hardly any deviation among the four characteristics. Equivalent results are obtained using SEMIC. B as can be seen in Fig. 5-15. Therefore it can be stated that the number of submodules in the MMC does not affect the thermal limit of the MMC converter. However, be aware that the higher the number of submodules is, greater is the number of semiconductors switching, what means that the power losses of the converter becomes greater, although the maximum achievable output current is obtained at equal switching frequency.

It should not be forgotten that this study is oriented to HVDC transmission application where *n* is likely a high number. So that, the previous conclusion is quite useful in case it is essential to extrapolate it to a big dimensions model. Once known that $I_{ph,rms,1}=f(f_{sw})$ characteristic is independent of *n*, it is quite easy to estimate the achievable power of the converter regarding the semiconductors switching frequency.

SEMIC. A					
n	**V_{DC}**	**P_{outmax}**	**$f_{sw\ max}$**	**Most restrictive semiconductor**	**WTHD**
8	5.5 kV	5.6 MW	582 Hz	T_{u2}	9.37e-4
12	11 kV	11.2 MW	611 Hz	T_{u2}	3.1e-4
16	16.5 kV	16.8 MW	612 Hz	T_{u2}	1.98e-4
Extrapolating:					
72	200 kV	203 MW	612 Hz	T_{u2}	<1.98e-4
228	640 kV	650 MW	612 Hz	T_{u2}	<1.98e-4
SEMIC. B					
n	**V_{DC}**	**P_{outmax}**	**$f_{sw\ max}$**	**Most restrictive semiconductor**	**WTHD**
8	11.2 kV	11.4 MW	480 Hz	T_{u2}	14.5e-4
12	16.8 kV	17 MW	480 Hz	T_{u2}	6.59e-4
16	22.4 kV	22.7 MW	480 Hz	T_{u2}	4.28e-4
Extrapolating:					
72	200 kV	203 MW	480 Hz	T_{u2}	<1.98e-4
228	640 kV	650 MW	480 Hz	T_{u2}	<1.98e-4

Table 5-4. Summary of obtained results at different *cos(φ)* with the two semiconductors.

In Table 5-4, the most representative parameters of the MMCs illustrated in the previous pictures are detailed. The selected switching frequency is the one which makes better use of semiconductors, this is, the frequency which allows flowing the maximum SOA current through these elements being its temperature under 110ºC. In this table two extrapolation examples are included with similar parameters than a HVDC application. Voltage or power is fixed (for example 200kV DC) and due to the converter's symmetries deduced in this section, the rest of the values are calculated. The output AC voltage considers a 20% voltage drop from the maximum available, due to

effects such as the output inductances, margin for control, etc...In addition, third harmonic injection is also commanded in the modulation.

5.2.5 Output current analysis with serialized submodule concept

In the context where a high number of submodules are required to reach the high voltages of HVDC applications, it can be interesting to be able to reduce the number of submodules. This objective can be achieved, for instance by increasing the DC voltage of each submodule arranging serialized semiconductors (for each valve) and maintaining the two level arm concept of each submodule. This option is presented for instance in [44], where each submodule valve is configured by 8 press-pack IGBTs in series connection as shown in Fig. 5-1c. Therefore, for instance by using valves arranging SEMIC. B in series, under idealized conditions, the DC bus voltage of each submodule would be 22.4kV, being the voltage seen by each semiconductor still 2.8kV. Thus, although the number of needed semiconductors is exactly the same to reach a given voltage level, the submodules are decreased 8 times, reducing the complexity of the modulation implemented and its corresponding control hardware.

When decreasing the amount of submodules with the serialized concept, the quality of the signal is worsen due to the fact that the number of levels in the output signal is directly related to n. It may well be crucial in low and medium voltage applications but it is not so relevant in high voltage applications like the one detailed in this analysis (section 5.1). Referring to the thermal study, considering an ideal serialization that means a uniform voltage distribution through all the IGBTs of the valve, the temperature reached by each of them does not depend on the number of serialized semiconductors because in fact these are independent chips. On the other hand, going back to the previous subsection, it is deduced that the temperature of the semiconductors is not related to the amount of submodules needed to reach a required total converter DC bus voltage. Consequently, it can be declared that there is no difference between $I_{ph,rms,1}=f(f_{sw})$ characteristics of a MMC with serialized submodule concept or the 'classic' one, if the total number of semiconductors used in each configuration is the same. Consequently, in order not to repeat figures, no characteristic of this configuration is shown in this section. However, as an example, from Table 5-1 and Table 5-2, if we pay attention for instance to the two configurations that based on 2L submodule concepts reach 179.2kV of total DC bus voltage, 128 'classic' submodules and 16 of serialized submodules are needed, but it can be said that both

solutions present the same $I_{ph,rms,1}=f(f_{sw})$ characteristic. Note that this is an idealized approach that does not consider auxiliary circuits which support the commutations [94], especially for the serialized case. However, it is expected that this fact does not affect significantly the conclusions.

5.2.6 Output current analysis with 3L-FC submodule concept

This analysis dedicated to the MMC is focused on the 3L-FC submodule concept. Following equivalent philosophy as in the previous subsection, the MMC converter is constructed with submodules as illustrated in Fig. 5-1d. This MMC converter concept is totally equivalent to the MMC based on the classic 2L submodules, with equal number of IGBTs and diodes which operate in exactly equal conditions at both philosophies despite being the number of submodules *(n)* the half. The AC output voltage of one 3L-FC submodule concept, is equivalent to the output voltage provided by two 2L submodules (Table 5-1 and Fig. 5-2). The main difference recalls in one of the capacitors of the 3L-FC submodule that must be of two times higher voltage than the capacitors of the 2L submodules. Therefore, with regards to the maximum achievable output current capacity of the MMC converter by using 3L-FC submodules, it can be concluded that provides equal results as obtained in subsections 5.2.2, 5.2.3 and 5.2.4. So for instance, to reach 179.2kV of total DC voltage with SEMIC. B, it would be necessary 128 submodules of 2L concept, or 64 submodules of 3L-FC concept, however, the same maximum output current characteristic $I_{ph,rms,1} = f(f_{sw})$, would be achieved, reaching also the same output power of the converter.

5.2.7 Output current analysis with 3L-NPC submodule concept

The way pulses are created for the 3L-NPC submodules of Fig. 5-1e is quite dissimilar to the previous topologies and thus thermal losses too. Hence finally the last objective is to compare 3L-NPC submodules with the others. For that, equal AC output voltage has been defined (or equivalently, same voltage of the total DC Bus) in order to avoid mistakes among results and $cos(\varphi)$ has been changed from 1 to 0 to keep away from its balancing problems. This is why the simulation of the MMC with 2L submodules consists of 6 submodules per arm while that of the 3L-NPC consists only of 3. In both cases the SEMIC. B is used and regarding the number of IGBTs needed, in both configurations is the same. Nevertheless, a higher number of diodes are required with 3L-NPC submodules, due to the usage of clamping diodes. On the other hand, this new

configuration needs extra balancing method of the capacitors of each submodule. This fact does not add extra complexity to the entire modulation schema of the MMC converter, as shown in [95].

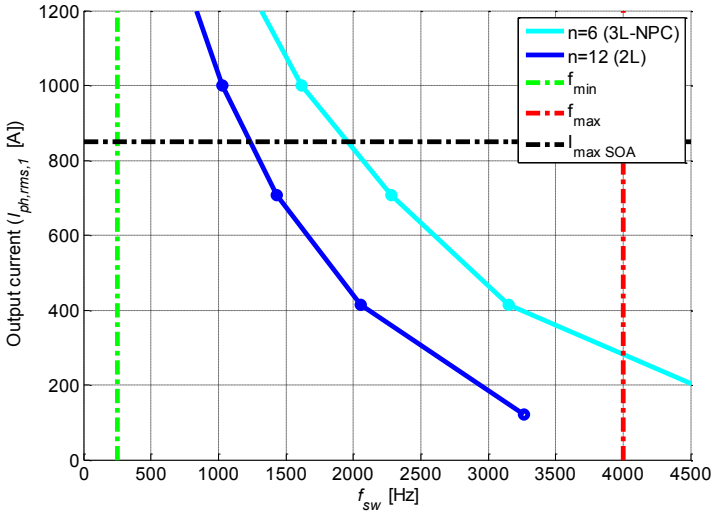


Fig. 5-16. $I_{ph,rms,1}=f(f_{sw})$ characteristics in a MMC(2L-VSC) with 12 submodules per phase and MMC(3L-NPC) with 6 submodules per phase using SEMIC. B, *ma=1* and *cos(φ)=0*.

$I_{ph,rms,1} = f(f_{sw})$ characteristics of Fig. 5-16 reveal that 2L submodules are more restrictive in all the frequency range. Meanwhile at the maximum SOA current this topology can work to 1250 Hz of triangular frequency, the 3L-NPC can do it to 2000 Hz. Nevertheless, it is important to remark that the output apparent frequency of the 2L submodules converter is twice.

Submodule configuration	n	V_{DC}	P_{outmax}	$f_{sw\ max}$	Most restrictive semiconductor	Number of elements	WTHD
2L	12	8.4 kV	8.5 MW	480 Hz	T_{u2}, T_{l1}	24 Diodes 24 IGBTs 12 Capacitors	6.59e-4
3L-NPC	6	8.4 kV	8.5 MW	573 Hz	T_{u1c}	24 Diodes 24 IGBTs 12 Capacitors 12 clamp diodes	6.59e-4

Table 5-5. Summary of obtained results with SEMIC. B.

From the 4 semiconductors which form a submodule in a MMC (2L-VSC), T_{u2}, T_{l1} are those with higher losses if the working conditions are: *ma=1* and *cos(φ)=0*. With the 3L-NPC submodule concept, T_{2c} is the most restrictive semiconductor. This fact is summarized in Table 5-5, concluding that the converter can be operated at higher triangular frequency, with 3L-NPC submodules. The main reason for that is because in 3L-NPC philosophy, during half of the period, there is always one semiconductor that is ON all the time, but not commutating, reducing therefore the average switching losses.

However, in 2L philosophy, there is always one semiconductor commutating at every switching period, increasing then the switching losses, compared to the 3L-NPC concept.

5.2.8 Extrapolation of the power losses

Having calculated the power losses generated in a MMC with 8, 12 and 16 2L submodules (keep in mind that serialized 2L and 3L-FC topologies behave equally in terms of thermal losses and consequently in power losses) when *cos(φ)=0* and *cos(φ)=1*, in Fig. 5-17 the resulting lines are derived by extrapolation for comparability purposes. In the same vein, the losses generated in a MMC with 3L-NPC submodules when *cos(φ)=0* are represented. So by means of this graph, it can be noticed that under equal working conditions (same converter power) the 3L-NPC submodule topology is a bit more efficient than the others.

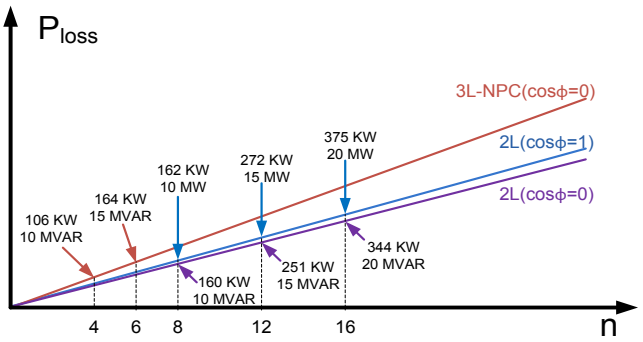


Fig. 5-17. Measured and extrapolated power losses regarding the converter output active or reactive power depending on its *cos(φ)* and *n*.

5.2.9 Analysis of the submodules capacitors

It is already well known that a 3L-(FC or NPC) submodule is equivalent to two 2L submodules in terms of number of elements (but for the clamp diodes in the NPC) as well as voltage output in their terminals. However, regarding the capacitors few differences appear:

- One of the two capacitors of the 3L-FC submodules has to be balanced at double voltage than the rest.
- In the 2L submodules with series connection of semiconductors, the balancing voltage of the capacitor depends on the amount of IGBTs serialized per valve.

- Due to the balancing algorithm besides the charge and discharge process of each topology, the obtained ripple over capacitor voltages changes in amplitude but also in shape.

Several simulations have been conducted in order to find out the capacity of each topology capacitor which leads to a determined ripple. For that, it has been chosen a single phase MMC with eight 2L submodules, other with four 3L-FC submodules and another one formed by four 3L-NPC submodules, thereby totalling 16 IGBTs in each arrangement. Due to the balancing problem of the 3L-NPC submodules topology when transmitting active power, both *cos(φ)=1* and *cos(φ)=0* have been considered. Pretty high f_{sw} has been chosen in order to disregard imperfections due to the commutations.

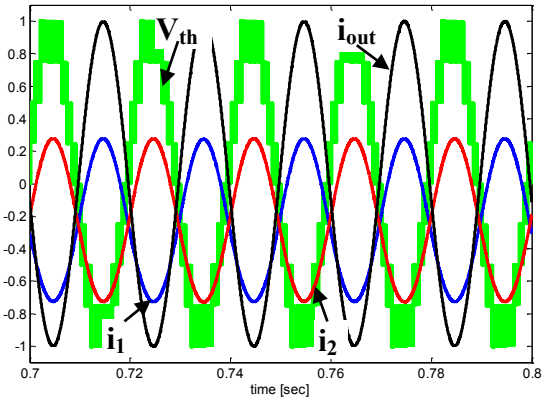


Fig. 5-18. 8 2L submodules MMC. Converter currents and output voltage being *cos(φ)=1*, f_{sw}*=10 kHz* (all in p.u.).

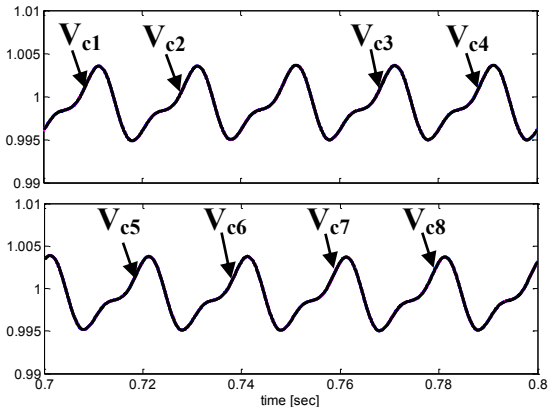


Fig. 5-19. 8 2L submodules MMC. Capacitors voltage being *cos(φ)=1*, f_{sw}*=10 kHz* (all in p.u.).

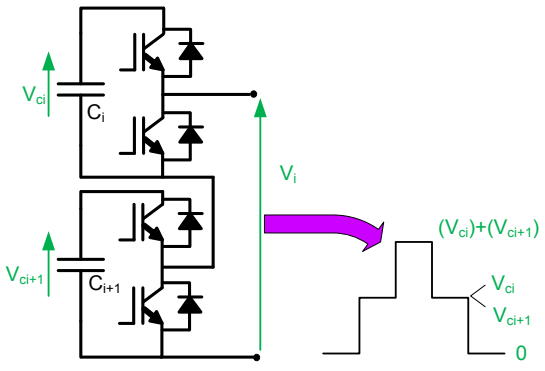


Fig. 5-20. An arrangement of a MMC two 2L submodules in series connection and its three possible voltage levels.

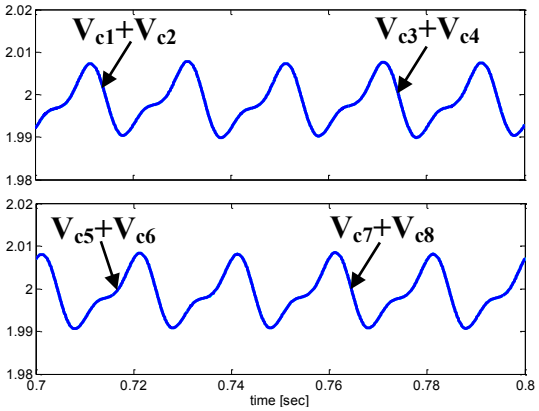


Fig. 5-21. 8 2L submodules MMC. Capacitors voltage being *cos(φ)=1*, f_{sw}*=10 kHz* (all in p.u.).

First, the results when *cos(φ)=1* are depicted. Fig. 5-18 and Fig. 5-22 demonstrate that both converters are working under the same conditions. In the 2L submodule configuration, the eight capacitors are balanced at the same voltage level but it is also

deduced from Fig. 5-19 that the ripple in the four capacitors of the each arm has got the same shape. Keeping in mind that two 2L submodules are needed to be equivalent to a 3L-FC one, the output voltage of two 2L submodules has to be added in order to contrast with the voltage at the 3L-FC terminals. As the ripple in the capacitors of the same arm has got identical shape, when their voltages are added to obtain the maximum level in V_x (see Fig. 5-20), the ripple is multiplied by two as can be observed in Fig. 5-23. Talking in percentage it reaches at around 1%.

Regarding the maximum level which is obtained in V_s of Fig. 5-20, similar results are achieved in the greater capacitors of the 3L-FC submodules as can be compared with Fig. 5-23. In this submodule topology, the value of the maximum level corresponds with V_{ci} as specified in Fig. 5-24 and thus the maximum ripple at the output terminals (being again of around 1%).

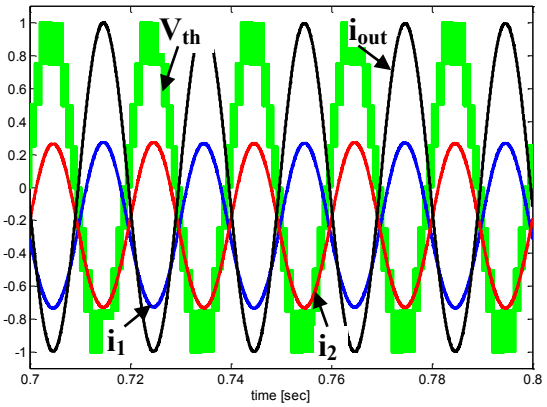


Fig. 5-22. 4 3L-FC submodules MMC. Converter currents and output voltage being *cos(φ)=1, f_{sw}=10 kHz* (all in p.u.).

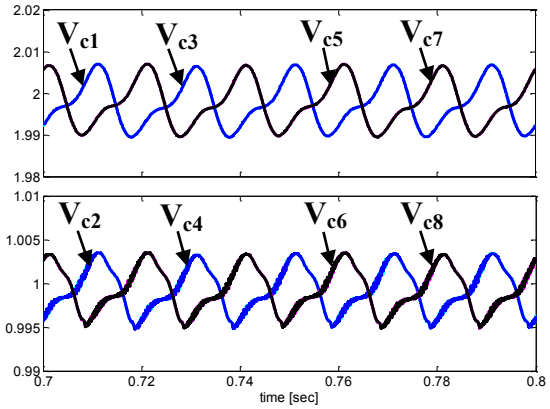


Fig. 5-23. 4 3L-FC submodules MMC. Capacitors voltage being *cos(φ)=1, f_{sw}=10 kHz* (all in p.u.).

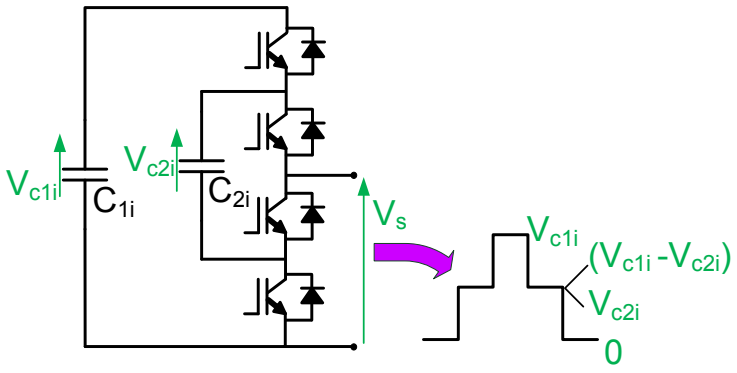


Fig. 5-24. A MMC 3L-FC submodule and its three possible output voltage levels.

It is verified that under the shown working conditions a 1% ripple has been obtained in both submodule topologies. However, to get that percentage, the capacity assigned to

capacitors is different. Meanwhile in the 3L-FC submodule $C_{1i}=C$ and $C_{2i}=0.4 \cdot C$, in the 2L submodule $C_i=C_{i+1}=2.2 \cdot C$. So in respect of the capacity, the 2L submodule is adversely affected. Nevertheless, in terms of stored energy in these elements, the outcome is the same in both cases. The reason is the double voltage of C_i in the 3L-FC submodule which increases the energy a lot because in the equation (5-6) the capacitor voltage is squared.

$$E_c = \frac{1}{2} \cdot C \cdot V_c^2 \tag{5-6}$$

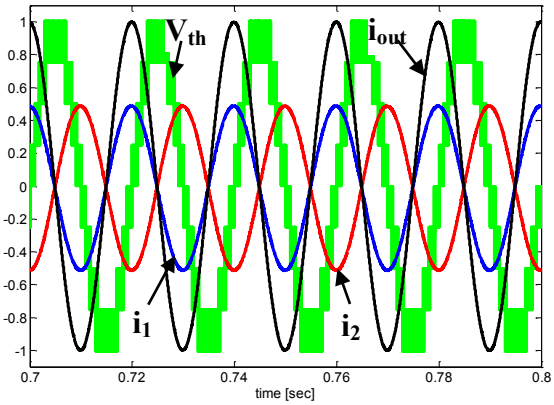


Fig. 5-25. 8 2L submodules MMC. Converter currents and output voltage being *cos(φ)=0*, f_{sw}*=10 kHz* (all in p.u.).

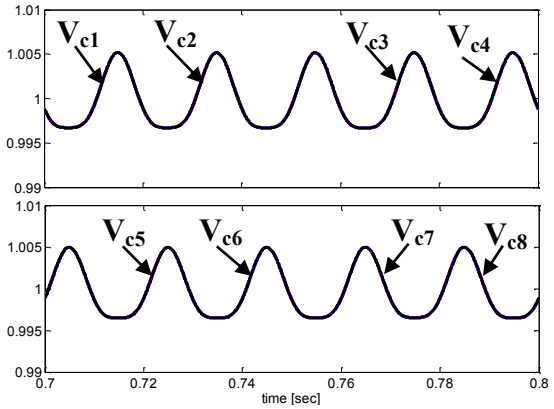


Fig. 5-26. 8 2L submodules MMC. Capacitors voltage being *cos(φ)=0*, f_{sw}*=10 kHz* (all in p.u.).

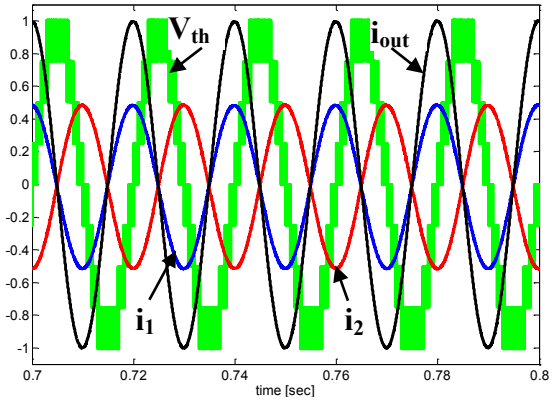


Fig. 5-27. 4 3L-FC submodules MMC. Converter currents and output voltage being *cos(φ)=0*, f_{sw}*=10 kHz* (all in p.u.).

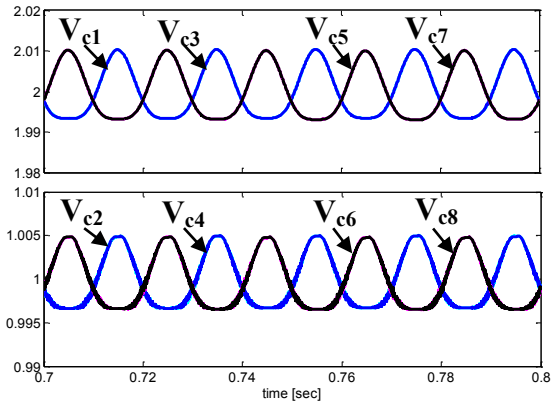


Fig. 5-28. 4 3L-FC submodules MMC. Capacitors voltage being *cos(φ)=0*, f_{sw}*=10 kHz* (all in p.u.).

The previous simulations are repeated but changing the working point from *cos(φ)=1* to *cos(φ)=0*. In this case, not only the former submodule topologies are analysed but also the 3L-NPC one. As can be checked in Fig. 5-25 and Fig. 5-27 there is a phase shift of 90º between the output current and voltage but their amplitudes have not change from the preceding pictures. Looking at the obtained capacitors voltages in Fig. 5-26 and Fig.

5-28 it can be noticed that although the ripple shape has been modified a little bit, its amplitude is again of around 1% in both topologies. To achieve this ripple percentage the capacity of the capacitors have had to be increased and therefore their stored energy too:

- 3L-FC submodule: $C_{1i}=C$, $C_{2i}=0.4 \cdot C$.
- 2L submodule: $C_i=C_{i+1}=2.2 \cdot C$.

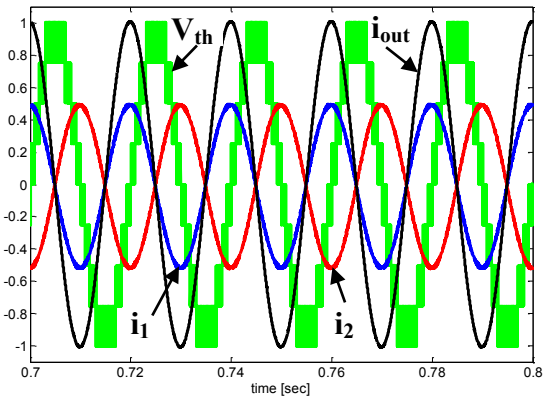


Fig. 5-29. 4 3L-NPC submodules MMC. Converter currents and output voltage being *cos(φ)=0, f_{sw}=10 kHz* (all in p.u.).

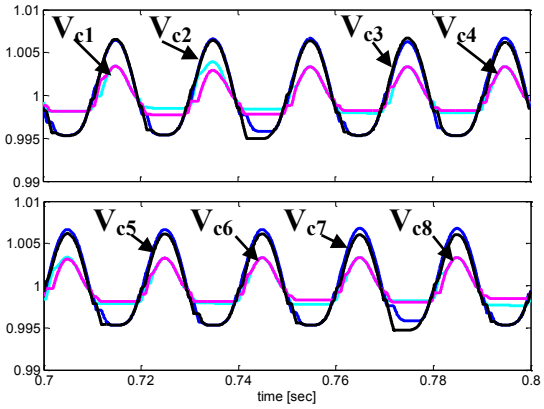


Fig. 5-30. 4 3L-NPC submodules MMC. Capacitors voltage being *cos(φ)=0, f_{sw}=10 kHz* (all in p.u.).

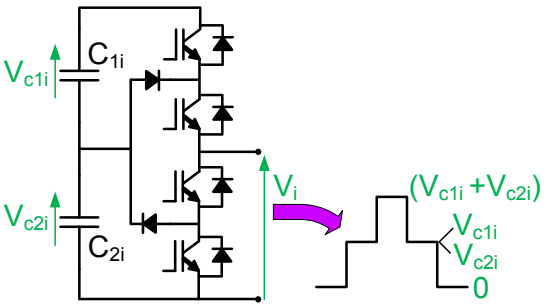


Fig. 5-31. A MMC 3L-NPC submodule and its three possible output voltage levels.

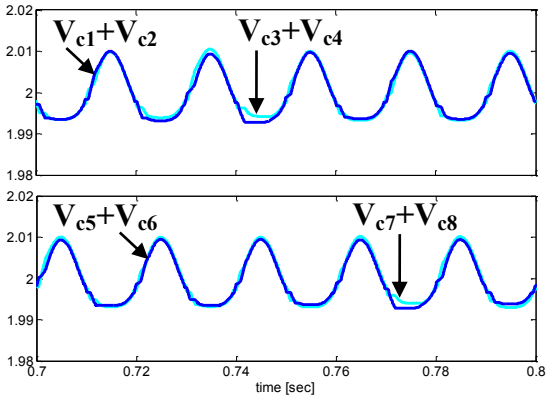


Fig. 5-32. 4 3L-NPC submodules MMC. Capacitors voltage being *cos(φ)=0, f_{sw}=10 kHz* (all in p.u.).

With regard to the 3L-NPC submodule topology, in Fig. 5-29 can be seen that the working point is *cos(φ)=0* because in this case the balancing of the capacitors is achieved. The objective of getting a ripple of 1% at the terminals of the submodule is obtained being $C_{1i}=2.3C$, $C_{2i}=3 \cdot C$. The voltage of all the capacitors of the simulated converter is illustrated in Fig. 5-30. Due to the modulation, the charge and discharge process of the two capacitors of the same submodule is not identical, resulting different amplitudes in their voltage ripple. However, as represented in Fig. 5-31, the maximum

voltage level of the submodule is got adding the two capacitors voltages as it is illustrated in Fig. 5-32. By means of that picture is corroborated that the proposed objective is satisfied.

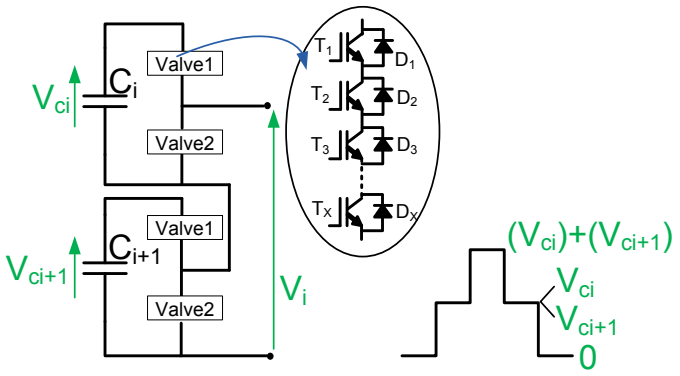


Fig. 5-33. A MMC serialized 2L submodule and its three possible output voltage levels.

Finally the serialized 2L submodule of Fig. 5-33 will be considered. Generally it works like a standard 2L submodule because the serialized semiconductors per valve behave like a single one, they all commute at the same time. However, the voltage of each submodule capacitor gets multiplied by *X* (number of serialized semiconductors). On the contrary, to fulfil the imposed 1% ripple at the terminals of the submodules, capacitors capacity is reduced in *X*. As a consequence, the stored energy per capacitor results equal to the 2L one, but it should be kept in mind that the number of elements is decreased.

		Submodules type			
		2L	**Serialized 2L (X IGBTs in series connection per valve)**	**3L-NPC**	**3L-FC**
Cos(φ)=1	**Capacity**	$C_i = 2.2 \cdot C$	$C_i = 2.2 \cdot C/X$	-	$C_{1i} = C$, $C_{2i} = 0.4 \cdot C$
	Voltage	$V_{ci} = V_c$	$V_{ci} = X \cdot V_c$		$V_{c1i} = 2 \cdot V_c$, $V_{c2i} = V_c$
	Current (rms)	$I_{ci} = I_c$	$I_{ci} = \cdot I_c$		$I_{c1} = \cdot I_{c2} = I_c$
	Energy	$E = 2.2 \cdot C \cdot V_c^2$	$E = 2.2 \cdot C \cdot V_c^2$		$E = 2.2 \cdot C \cdot V_c^2$
Cos(φ)=0	**Capacity**	$C_i = 2.2 \cdot C$	$C_i = 2.2 \cdot C/X$	$C_{1i} = 2.3$, $C_{2i} = 3 \cdot C$	$C_{1i} = C$, $C_{2i} = 0.4 \cdot C$
	Voltage	$V_{ci} = V_c$	$V_{ci} = X \cdot V_c$	$V_{c1i} = V_{c2i} = V_c$	$V_{c1i} = 2 \cdot V_c$, $V_{c2i} = V_c$
	Current (rms)	$I_{ci} = \cdot I_c$	$I_{ci} = \cdot I_c$	$I_{c1} = 0.8 \cdot I_c$, $I_{c2} = 1.2 \cdot I_c$	$I_{c1} = \cdot I_{c2} = I_c$
	Energy	$E = 2.2 \cdot C \cdot V_c^2$	$E = 2.2 \cdot C \cdot V_c^2$	$E = 2.65 \cdot C \cdot V_c^2$	$E = 2.2 \cdot C \cdot V_c^2$

Table 5-6. Summary of capacitors features at different *cos(φ)* and submodule type.

The results obtained along this section are collected in Table 5-6. To sum up, it can be said that regardless the operation point, the 3L-FC submodule is advantageous in the capacity as well as rms current through capacitors but conversely, the voltage of one of

them is double. Including these two terms in equation (5-6), the energy comes out to be the same than in the others except in the 3L-NPC which is penalized in the analysed terms.

5.2.10 Extrapolating to a HVDC application

Once different configuration of MMC converters are studied considering output voltage quality and maximum achievable output current capacity, the next task consists of extrapolating these results to the voltage characteristics required by a HVDC application. Two HVDC scenarios have been chosen in terms of total DC connecting voltages to fill in the Table 5-7: 200kV and 640kV (which could be ±100kV and ±320kV respectively). Note that these connection voltages could be catalogued as considerably high, if we compare them with the worldwide VSC-HVDC projects already existing now [96]. Neither simulations nor experimental tests have been performed at these voltage levels, arranging all the required number of submodules. Instead, the conclusions of previous sections deduced with reasonably low number of submodules have been utilized, and then extrapolated to the amount of submodules necessary to reach the specified voltages. In this section only SEMIC. B will be taken into account because it does not have any sense to choose a low voltage semiconductor for this kind of application.

As can be seen, all the configurations let transmit the same amount of power barely differing in the number of submodules needed. By considering the results deduced in the precedent section, it can be assumed that the number of utilized submodules does not affect to the maximum achievable output current of the converter, leading us to the conclusion that the maximum output current *(I_{max_SOA}=848.5A)* would be given at 480 Hz or less, as deduced in Fig. 5-15. Furthermore, the output AC voltage quality is excellent as noticed by the WTHD except in the case of 2L configuration in which only 18 submodules are required and the silicon efficiency is almost similar. Note that this configuration allows reducing considerably the complexity of the modulation and implementation philosophy. However, it must be guaranteed a reliable series connection of semiconductors. This is the reason why alternative submodule concepts such as 3L-FC might well be considered for HVDC applications as described before.

On the other hand, for those sceneries in which working at *cos(φ)=1* is not required, for example reactive power compensators, not only could 3L-NPC submodule topology be useful but also competitive.

Submodule configuration	V_{DC}	n	P_{outmax}	$f_{sw\ max}$	Number of elements per phase	WTHD
2L	200 kV	144	203 MW	480 Hz	288 Diodes 288 IGBTs 144 Capacitors	<1.98e-4
	640 kV	460	650 MW	480 Hz	920 Diodes 920 IGBTs 460 Capacitors	<1.98e-4
2L with 8 IGBTs in series per valve	200 kV	18	203 MW	480 Hz	288 Diodes 288 IGBTs 18 Capacitors	3.18e-4
	640 kV	58	650 MW	480 Hz	928 Diodes 928 IGBTs 58 Capacitors	<1.98e-4
3L-FC	200 kV	77	203 MW	480 Hz	288 Diodes 288 IGBTs 144 Capacitors	<1.98e-4
	640 kV	230	650 MW	480 Hz	920 Diodes 920 IGBTs 460 Capacitors	<1.98e-4

Table 5-7. Summary of obtained results with different submodule concepts, at *cos(φ)=1* and m_a*=1.*

5.2.11 Final comparison

In Table 5-8 the most relevant characteristics of the studied MMC submodules arrangements are collected with the aim of making a comparison among them. For this purpose, although the submodule topologies are different, the chosen semiconductor and number of them keep unaltered in order to reach an equal defined AC output voltage of the converter. Being difference neither in the current nor in the voltage, the power value works out to be the identical (provided that the f_{sw} is low).

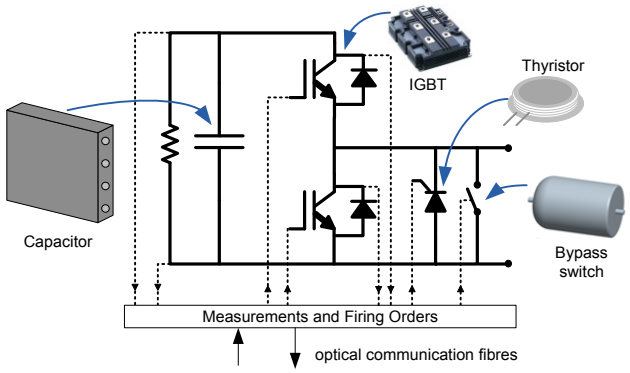


Fig. 5-34. Components of a MMC 2L submodule showing apart from the capacitor and semiconductors, the protection thyristor, bypass switch and all signal exchange between the power module and the management system.

On the one hand, along the chapter it has been mentioned that the total number of semiconductors per phase is exactly the same for all the topologies except for the 3L-NPC one, in which 2 extra clamp diodes per submodule are needed. On the other hand, it should also be remembered that one 3L-NPC or 3L-FC submodule is equivalent to two 2L submodules in terms of power electronic switches, anti-parallel diodes, capacitors and voltage levels at their terminals. Therefore those components such as

cold-plates, bus-bars, protective switches, connections, etc. which are required per submodule will be double in 2L topology (see in Fig. 5-34 the elements needed per submodule). On the contrary, one of the 2L with series connection topology's benefit is that the amount of submodules is reduced according to *X* and in turn fewer associated components are necessary. As a drawback of this last arrangement, the serialization of semiconductors entails the usage of passive elements to share the voltage accurately which provoke higher losses. In addition, the driver for these valves gets more complex and thus probably more expensive.

		Submodules type			
		2L	**Serialized 2L (X IGBTs in series connection per valve)**	**3L-NPC**	**3L-FC**
Achievable power (output current)		=	= [1]	=	=
Semiconductors in normal operation:		=	=	**Unfavourable**	=
No. of IGBTs		=	=	=	=
No. of anti-parallel diodes		=	=	clamp diodes required	=
Elements of the Submodule:		**Unfavourable**	**best**	=	=
No. of submodules		Double	X times less	=	=
No. of cooling plates		=	X times less	Unfavourable (clamp diodes)	=
No. of bus-bars		Double	X times less	=	=
No. of high speed Bypass switch		Double (but half voltage)	X times less	=	=
No. of protective thyristor		Double (but half voltage)	X times less	=	=
No. of thyristor control circuits		Double	X times less	=	=
No. of thyristor clamp		Double	X times less	=	=
Bypass switch and thyristor trigger		Double	X times less	=	=
No. of capacitors voltage sensors		=	X times less (of higher voltage)	=	=
No. of connections between submodules		Double	X times less	=	=
No. of optical communication fibres		Double	X times less	=	=
THD		=	**Unfavourable (when less than 14 submodules are required)**	=	=
Driver and switching assistance:		=	**Unfavourable**	=	=
Complexity of the driver for the IGBTs		=	Unfavourable	=	=
Passive elements for serializing semiconductors		No	Yes	No	No
Modulation:		=	**best**	**Unfavourable**	=
No. of triangular carrier signals		=	N times less	=	=
Capacitors balancing problem		No	No	Yes (at some cosφ)	No
Complexity considering the balancing principle [2]		=	=	=	=
Computational cost of the hardware where it is implemented		=	best	=	=
Bus capacities:		=	=	**Unfavourable**	=
Voltage sensors for the modulation		=	=	=	=
No. of capacitors		=	=	=	=
Capacitors characteristics (of one submodule):		=	=	Unfavourable	=
Cos(φ)=1:	Capacity	$C_i = 2.2 \cdot C$	$C_i = 2.2 \cdot C/N$	-	$C_{1i} = C$, $C_{2i} = 0.4 \cdot C$
	Voltage	$V_{ci} = V_c$	$V_{ci} = N \cdot V_c$		$V_{c1i} = 2 \cdot V_c$, $V_{c2i} = V_c$
	Current (rms)	$I_{ci} = I_c$	$I_{ci} = I_c$		$I_{c1} = I_{c2} = I_c$
	Energy	$E = 2.2 \cdot C \cdot V_c^2$	$E = 2.2 \cdot C \cdot V_c^2$		$E = 2.2 \cdot C \cdot V_c^2$
Cos(φ)=0:	Capacity	$C_i = 2.2 \cdot C$	$C_i = 2.2 \cdot C/N$	$C_{1i} = 2.3 \cdot C$, $C_{2i} = 3 \cdot C$	$C_{1i} = C$, $C_{2i} = 0.4 \cdot C$
	Voltage	$V_{ci} = V_c$	$V_{ci} = N \cdot V_c$	$V_{c1i} = V_{c2i} = V_c$	$V_{c1i} = 2 \cdot V_c$, $V_{c2i} = V_c$
	Current (rms)	$I_{ci} = I_c$	$I_{ci} = I_c$	$I_{c1} = I_c \cdot 0.8$, $I_{c2} = I_c \cdot 1.2$	$I_{c1} = I_{c2} = I_c$
	Energy	$E = 2.2 \cdot C \cdot V_c^2$	$E = 2.2 \cdot C \cdot V_c^2$	$E = 2.65 \cdot C \cdot V_c^2$	$E = 2.2 \cdot C \cdot V_c^2$
Switching and conducting losses		=	=	**Favourable** [3]	=
Passive elements losses (assistance to the switching)		=	**Unfavourable**	=	=

[1] If the number of submodules is high enough to avoid an output filter.
[2] Regarding the balancing method explained in this article.
[3] At the same triangular frequency.

Table 5-8. Summary of the most relevant characteristics of a MMC with different submodule concepts using the same IGBT and diode in all the cases (same total output AC voltage of the converter).

The principal advantage of the MMC is that for high voltage applications which demands great number of submodules to form the converter, a multilevel signal is obtained adding their voltages in a well-organized way. From 15 steps on, the output signal is considered good enough because the acquired THD is really low. However, this particularity could be lost with the serialized 2L topology since the total number of submodules is reduced affecting the quality of the output signal. In STATCOM applications [97], [73] where the MMC is becoming more interesting, the AC voltage is about 30kV (unlike the HVDC which can reach ±300kV). In these cases, since no very large number of submodules is needed, deteriorating the wave quality by using valves with serialized IGBTs cannot be profitable because greater output passive filter may be used as compensation.

Regarding the modulation, it is worth mentioning that the most disadvantageous topology is the 3L-NPC due to the fact that it is impossible to get the balancing of the capacitors for a wide operating range as has been detailed before. Conversely, the most favourable is the serialized 2L due to the number of submodules once again. The fewer submodules there are, the fewer triangular carrier signals have to be implemented and as a consequence the capacity of the control hardware will not be so demanding. As far as the capacitors are concerned, all the capacities specified in de table have been calculated to attain the same percentage ripple rate.

No great differences are detected between 2L and serialized 2L topologies. On the last one, capacitors capacity and voltage depend on the number of series connected semiconductors but in the end, the stored energy result identical. The negative point of the 3L-FC submodules is that the voltage of one of its two capacitors is established to $2 \cdot V_c$. Nevertheless, it has been discovered that comparing to the previous two topologies, the capacity required to achieve a determined relative ripple is lower. Despite the differences in capacity and voltage parameters, not only does the total energy in the 3L-FC topology outcome as in both 2L arrangements but the rms current which circulate through them is also the same. Regardless the balancing problem of the 3L-NPC when $cos(\varphi)=1$, the results gathered in the table reveal that it is also disadvantageous when it is working for example as a STATCOM (being $cos(\varphi)=0$).

Finally, concerning the efficiency, it has been demonstrated by means of several experiments that the 3L-NPC topology generates higher switching and conducting losses than the rest, although the serialized 2L topology is the only one which adds significant passive elements power losses.

Once all the characteristics have been explained, it can be concluded that there is not a clear topology which stands out from the rest, each of them has got its beneficial and disruptive points. This means that depending on the hot issue and interest of each company, any of these topologies could well be chosen. Nonetheless, to sum up, it can be stated that the 3L-FC submodule topology is the most favourable one overall because taking into account the whole table it does not show up to be the worst in none of the detailed aspects. Moreover, comparing it with the 2L submodule, the fact of needing half submodules greatly facilitates the assembling process and reduces to a great extent the number of elements of the converter.

5.3 Conclusions

This analysis and evaluation of different submodule concepts for Modular Multilevel Converter, has concluded on several interesting and useful aspects. First of all, from the achieved output quality point of view, it has been seen that all the submodule concepts can provide a very good quality waveforms when they operate in the range of the high voltage levels of HVDC applications. This fact is mainly due to the necessity of a high number of submodules to reach this high voltage levels, together with the intrinsic multilevel nature of the MMC converter. This can be understood as an advantageous characteristic, reducing the necessity of bulky and costly filter requirements. It must be pointed out that the ingenuous 2L submodule concept with series connection of IGBTs, can effectively reduce the number of submodules resulting an interesting solution that can significantly improve important issues of HVDC applications such as: firing orders, implementation complexity, modulation complexity, etc… mainly associated to the high number of modules involved in the converter. However, this solution is accompanied with an unavoidable reduction of the quality of the generated waveforms, compared with the rest of the submodule concepts studied. Actually, this is not a real drawback, since the quality of signals achieved is still considered as very good, allowing to eliminate the costly filter requirements if the connecting voltage range must be of very high range (640kV for instance).

Secondly, from the thermal analysis, several conclusions can be remarked. First of all, it must be highlighted that the procedure itself, allows calculating the maximum achievable output power and currents of the MMC converter, without the necessity of performing the simulation with the high number of submodules (even several hundreds)

required by the HVDC application. From the obtained results, it has been seen that it is enough to perform some few 'easier' simulations with low number of submodules and then extrapolate by simple analytical calculus (can be done by hand), to the required connection voltage level, with the corresponding 'high' submodule number, but avoiding the necessity of performing such complicated simulations. Thus, this simple evaluation procedure permits to study the appropriateness of several semiconductor options available in the market for one specific HVDC application.

In addition, this evaluation procedure is able to calculate the switching frequency limit at which the semiconductor utilized can operate at its maximum current limit (SOA current limit) for every submodule studied in MMC topology and at different operating conditions. This value is useful first to know which switching frequency permits to reach the maximum current of the semiconductor, and secondly to know the quality of the waveforms achieved under this condition. Therefore, the study that has been carried out reveals that all the submodule concepts considered with the two utilized semiconductors can operate at around 500 Hz switching frequency limit. Under these circumstances, all of them can make operate the converter with around 200MW (at 200kV of DC voltage) or 650MW (at 640kV of DC voltage), which is a useful range of powers for HVDC applications. However, in a HVDC application where the number of submodules will be really high, it is more convenient to decrease the f_{sw} obtaining a good quality waveform but with the aim of reducing the converter power losses and therefore enhancing its efficiency. Generally frequencies around 100 – 250 Hz are employed, that is why the 500 Hz one would not be very realistic. On the other hand, if the converter is going to work as a STATCOM where the voltage is lower and consequently the number of submodules too, a proper f_{sw} should be evaluated in a compromise among power losses, output filter requirement, number of submodules, etc.

Going into more detail, it can be said that SEMIC. A permits to switch faster (around 600 Hz) than SEMIC. B. However, this does not almost produce benefits from the quality of the generated waveforms point of view, and is penalizing the fact that it needs much higher number of submodules (due to its smaller $V_{ce@100FIT}$ voltage), increasing the implementation complexity and potential reliability of the converter. It can be thought that it is better to use a semiconductor with a higher $V_{ce@100FIT}$ voltage ratio, for instance SEMIC. B, allowing using the least number of submodules that is possible, even if the switching frequency limit achieved is slightly lower. On the other hand, it is

remarkable that the 3L-NPC submodule concept also permits to obtain higher switching frequency limits, due to its intrinsic modulation philosophy.

From a practical point of view, it can be said that the best advantage of the multilevel submodule concept, compared to the classic 2L submodule, is that the number of submodules can be reduced, leading, in turn, to a significant reduction of elements associated to the submodule (thyristors, bypass switches, optical fibres, etc..), potentially reduction in the volume and assembling process of the converter. Moreover, from a manufacturer point of view, the multilevel submodule concepts (3L-NPC and 3L-FC in this case), can be attractive in order to avoid problematic situations related with patents.

Regarding the final comparison provided in this chapter, it is not intended to defend any of the studied topologies as the best. Instead, the only intention is to show in a rigorous way the advantages and disadvantages among them, providing to the reader a wider and realistic perspective of the factors that can influence a manufacturer of converters, to take the decision of choosing one topology from other.

Finally, it can be concluded saying that perhaps a good option for a HVDC application, could be to use a submodule concept together with a semiconductor that permits to operate with a considerably high voltage level at each submodule (for instance, 2L with series connection of 6 to 12 IGBTs), in order to achieve good balance between implementation complexity and quality of the waveforms generated. The semiconductor should be in the range of kAmperes, in order to reach considerably high power levels and suitable to perform an efficient series connection, to finally build up reliable valves. All of this, of course should be also well coordinated with constructive, control, dimensions, cost, etc… aspects, which are out of the scope of this analysis.

Chapter 6

Problems associated with disturbances and feasible solutions

As described in the previous chapter, many equipments take part in the power transmission from the generators to the onshore connection point. Obviously in such a large and important system, all of them have to be studied in detail and perfectly adapted to the particular case because any of them can entail a source of malfunctions.

This chapter deals with some issues which have not been deeply analysed but are believed to be fundamental for the smooth running of the system. The first section is about the hardnesses that this kind of converter presents regarding the voltage supply of some devices, isolation among them, complicated management system and assembling of the structure.

The second section concerns the failures in general. Some of them are provoked by external causes, for instance, the breakage of a submarine cable or a lightning strike. The most used protections against these failures are proposed. However, there are others which can occur in the same converter like the breakdown of a semiconductor. For this case, the consequences are discussed and some possible solutions are suggested.

6.1 Specific characteristics of the MMC working as HVDC

6.1.1 Precharge of the capacitors

A not very cited drawback of the MMC (regardless the topology of its submodules) is the precharge of all the capacitors before becoming the converter operational. In practice, difficulties occur when a common network intertie has to start without power from the de-energized condition into operating condition ("black start").

A possible process of charge per inverter arm for 2L submodules is described in [98]. In order to accomplish this procedure, only one auxiliary voltage source with a relatively low output voltage ($V_{Load} \approx V_C$) is necessary. The output terminals of the supply are connected to the DC bus of the multilevel converter. Per inverter arm a number of *(2n-1)* IGBTs T_2 (Fig. 6-1a) are turned on. The remaining IGBT T_2 and all remaining IGBTs T_1 in the inverter leg are kept off. When one capacitor per phase leg has reached the operation voltage, the next ones are selected by appropriate gating. In that way all capacitors in the arms are gradually charged to the operation voltage (Fig. 6-1b). Finally, the voltage source has to be disconnected by series diodes or mechanical switching.

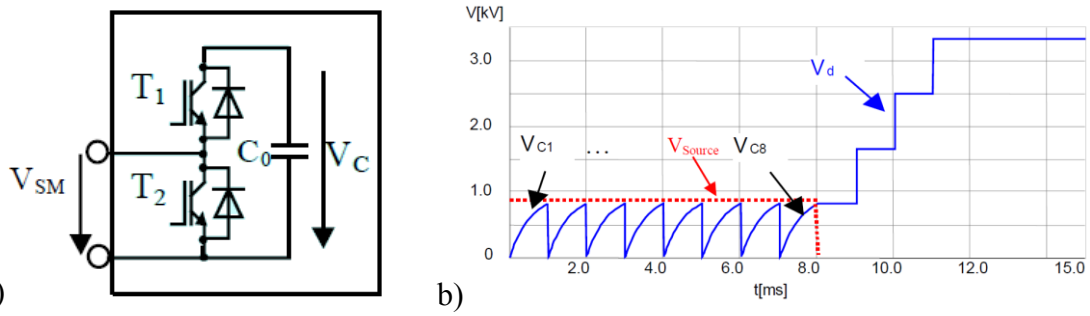


Fig. 6-1. Process of charge per inverter arm. Source: [98].

However, this precharge presents some drawbacks related to the duration of the process and charging level. A solution to overcome these problems is proposed in [99]. It consists of a new precharge topology of MMC based on submodules in parallel and attached to external DC bus bars to precharge synchronously in order to accelerate the "black start" process (Fig. 6-2). Triggering the four included antiparallel thyristors with pulses synchronously will start the precharge process until all the capacitors are simultaneously charged to U_{C0}. Then the thyristors will automatically turn off so that the submodules' terminals have the same electric potential and the maintenance current

fall to zero. Then all the capacitors will be connected to the submodules and operated in normal mode. The waveform of the new MMC precharge topology is shown in Fig. 6-3.

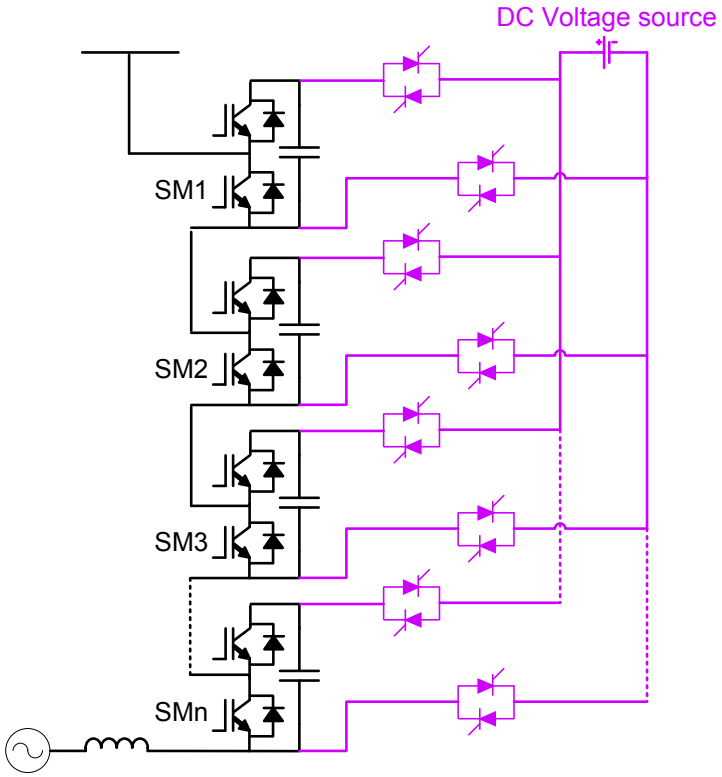


Fig. 6-2. New 2L submodules MMC precharge topology [99].

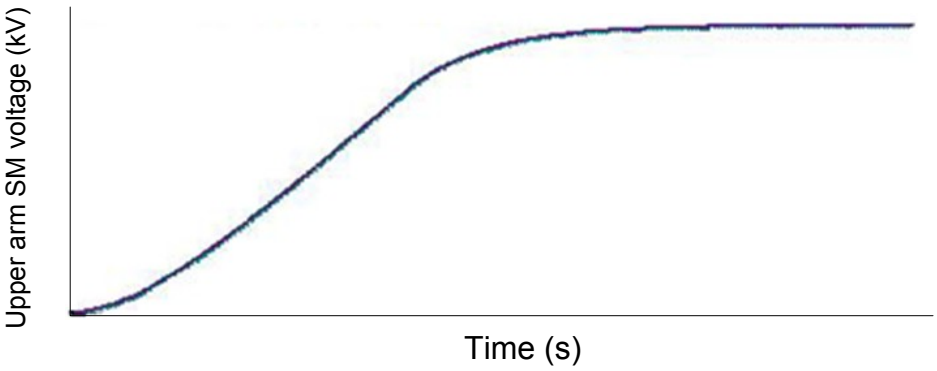


Fig. 6-3. Process of charge per inverter arm [99].

This last precharging process is expressly designed for 2L submodules but it could be used for the multilevel submodules studied in this report implementing some changes to overcome the different disposition of the capacitors. Beginning with 3L-FC submodules, where there are 2 capacitors with different balancing voltage and based on the previous idea, the solution consists of using 2 DC voltage sources to accomplish that

task (see Fig. 6-4a). The process would be identical but one of the submodules capacitor would be charged to half voltage in comparison with the other one.

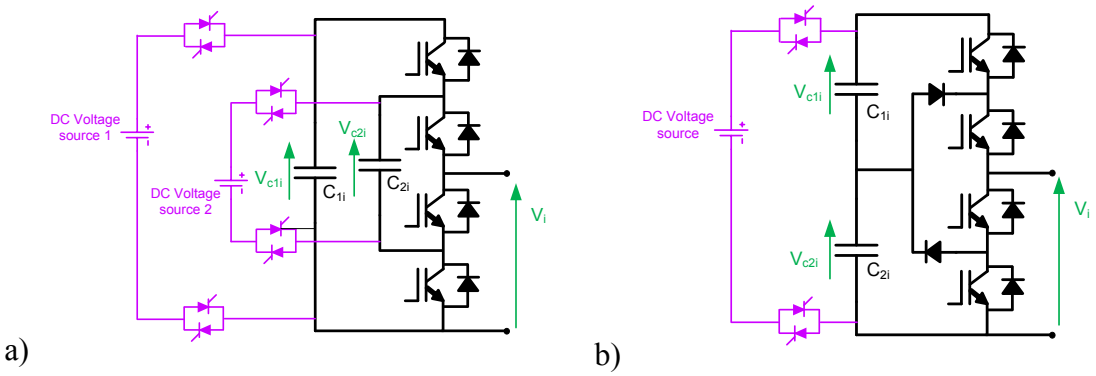


Fig. 6-4. a) 3L-FC submodules MMC precharge topology. b) 3L-NPC submodules MMC precharge topology.

On the other hand, regarding the 3L-NPC submodules, the topology would only differ in the connection points as depicted in Fig. 6-4b. Ideally, in this way the two capacitors would be charged simultaneously and acquire the same voltage level although in practice their charge should be controlled.

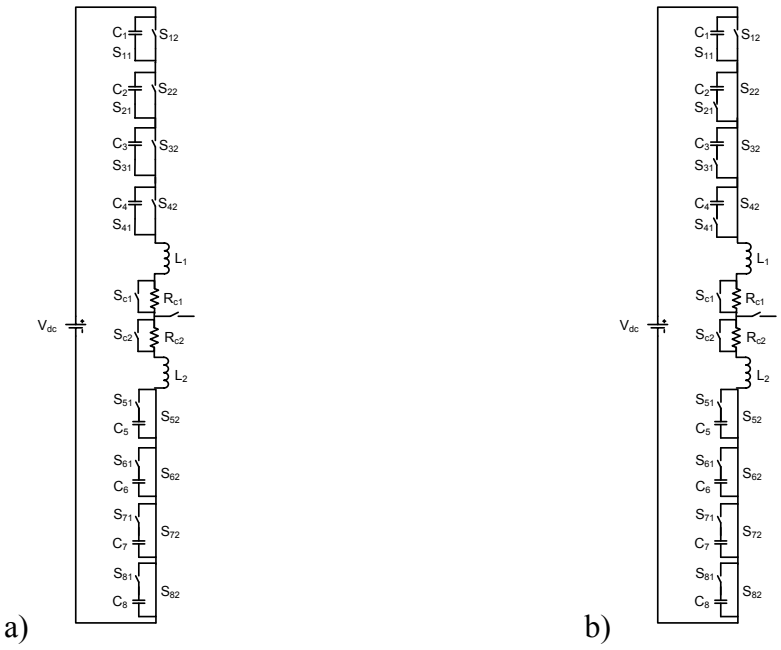


Fig. 6-5. a) Simultaneous charging of upper capacitors in one phase. b) Individually charging of capacitors in each submodule.

Some other methods for charging the series capacitors proposed in the literature also rely on an external voltage source to do so [100], [101]. However, according to [102] the charging and discharging of the capacitors can be done from the main voltage source. For this, an additional resistance controlled by a mechanical or electronic switch

is connected in series to the arms, see Fig. 6-5. At steady state operation, the resistance is bypassed from the circuit. Conversely, by appropriately inserting it, the capacitors in the submodules can be charged or discharged, for instance during the removal of a submodule from the circuit. All those capacitors of one arm can be charged simultaneously and then those of the other arm as in Fig. 6-5a, or one by one as shown in Fig. 6-5b.

6.1.2 Control hardware

In a MMC oriented to the HVDC application in which hundred submodules per phase are needed, the management system becomes really complex. In previous chapters has been explained that as many triangular signals have to be generated as number of submodules with a particular phase shift among them. Apart from these carriers, it is crucial to measure the voltage of every submodules capacitor in order to generate the proper firing order for each submodule with the aim of balancing the whole phase capacitors. In addition, it is important to measure the voltage at the semiconductors terminals to identify failures. This means that the converter's overall management system has to deal with a great amount of data transmitted to it by two optical fibres from the power module of each submodule. Therefore a really powerful hardware is required to coordinate the received information, manage the power exchange, generate the firing orders, activate the protection systems, etc.

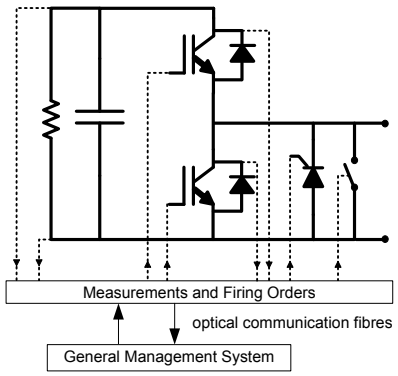


Fig. 6-6. Signal exchange between the power module of a 2L MMC and the management system.

6.1.3 Voltage supply for the drive of the submodule

When using many power semiconductor devices connected in series in a high voltage converter circuit such as the MMC, there is a problem in supplying the individual drive units. Utilizing individual transformers (one for each drive unit) is a very expensive solution, especially in high voltage converter circuits in which the potential differences between ground and the different drive units are high, tens of kV or more. Therefore a

much simpler, reliable, well isolated and considerably less expensive power supply for the drive units has to be designed.

A possible solution is to provide the different drive units with energy taken from the capacitor of its same submodule. To obtain the desired input voltage level for the drive, various circuits are patented in [103]. For example: a static voltage divider connected in parallel with the power semiconductor device plus a shunt regulator (shown in Fig. 6-7a), a regulator connected in series with the capacitor or a DC/DC converter if positive but also negative voltage has to be applied to the gate of the semiconductor. A similar proposal is explained in [104] whose main layout is depicted in Fig. 6-7b. The advantage of this type of power supply is that there is no need for utilizing high voltage insulated transformers which results in saving costs and a smaller size of the apparatus.

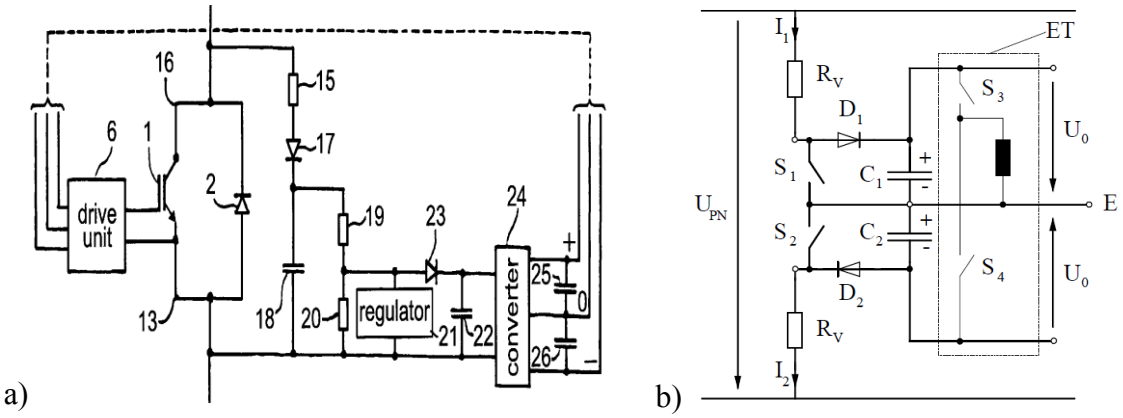


Fig. 6-7. Voltage supply for the drive taking energy from the submodule capacitor a) Source: [103]. b) Source: [104].

6.1.4 Submodules and converter arrangements

The aim of the pictures above (Fig. 6-23) is to give a physical view of the VSC-HVDC submodules and the whole converter. Fig. 6-23a is the image of a submodule where the capacitor is as bigger as the rest of the components. In Fig. 6-23b the typical 400 MW converter arrangement is represented. It consists of six arms of more than 200 submodules per each one. Finally, in Fig. 6-23c a real installation of Siemens converter is shown to give an idea of its size as well as how the submodules are disposed. Here it can be appreciated that each arm structure is formed by three submodules floors separated by means of isolators and reinforced with protections against seismic movements.

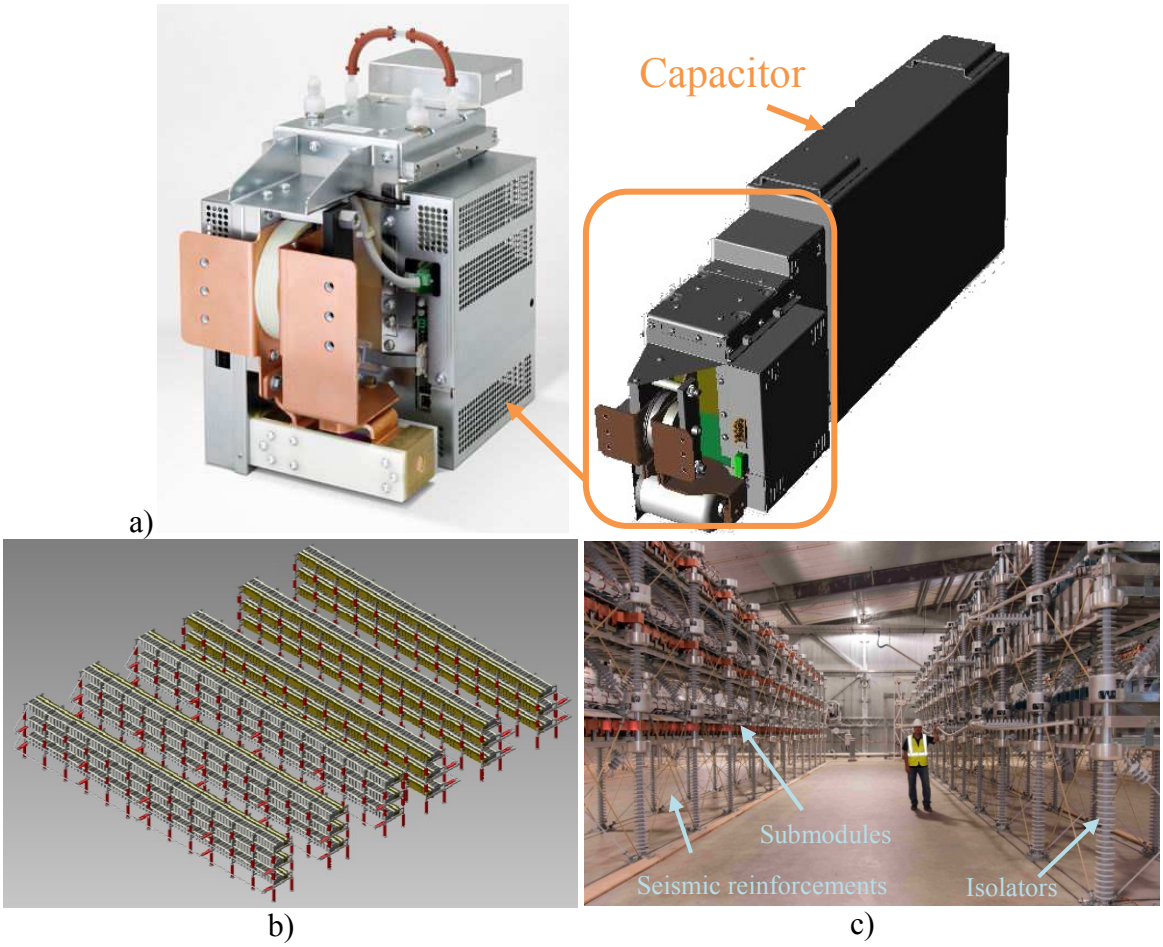


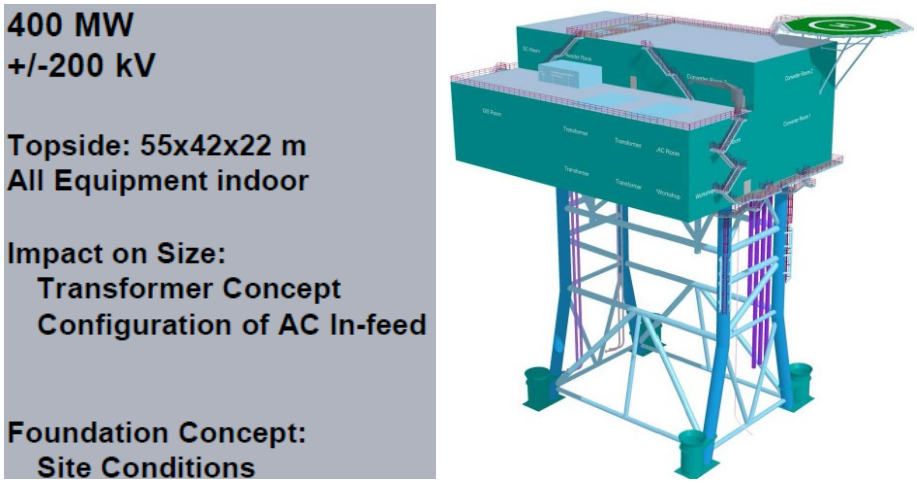
Fig. 6-8. a) Power module. b) Typical converter arrangement for 400 MW. c) On site installation. Source: [105].

6.1.5 Onshore and offshore substations

Once seen the structure and the space required for the converter thereof, the onshore and offshore substation will be shown. Meanwhile all the components size is minimized on the offshore platform and a special foundation (depending on the water depth and seabed) is needed for its emplacement, these requirements are not so critical on the onshore substation. Comparing both Fig. 6-9 pictures which represent the same 400 MW converter, the surface occupied by the offshore substation is 55x42 meters while the onshore one is around 130x90 meters.

As can be seen in Fig. 6-9a, a landing area is built on the topside of the platform because it is only accessible by air (helicopter for maintenance works or simple standardised repairs) or by sea (requiring the use of a service vessel for routine access, and a jackup rig for heavy and big piece replacements). Unlike the offshore substation with indoor equipment, on the onshore one there are some elements such as the transformers or switchyards (Fig. 6-9b) that can be placed outdoor.

a)



b)

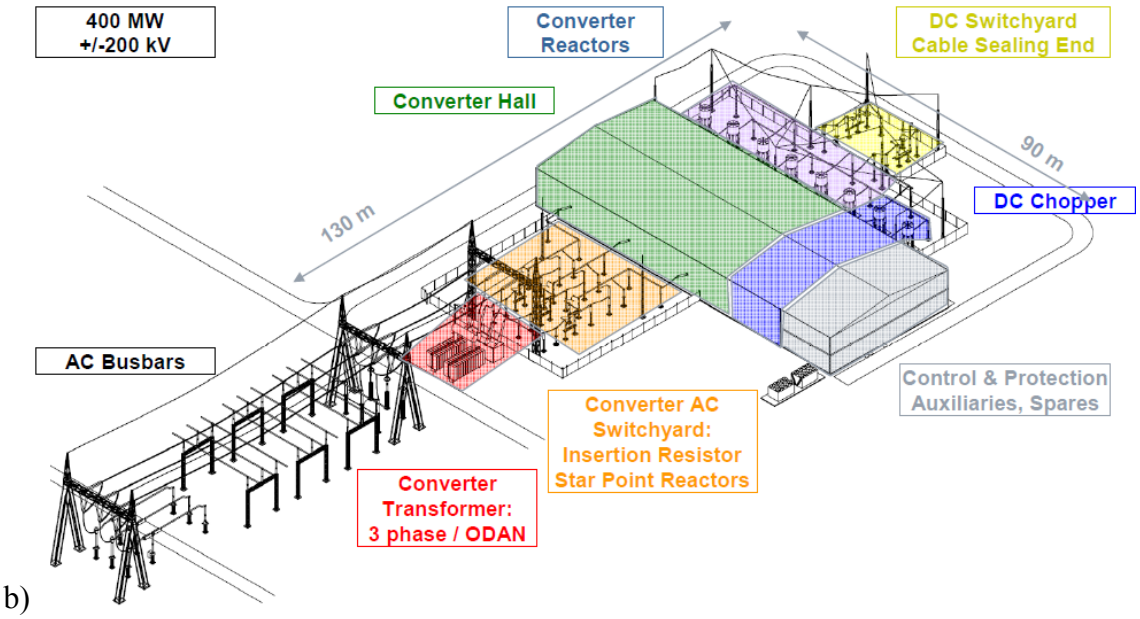


Fig. 6-9. a) Offshore platform design. b) Onshore station layout. Source: [105].

6.2 Problems associated with failures

6.2.1 AC current interrupter

AC circuit breaker (Fig. 6-10b) is a switching device which can open or close circuit in a small fraction of second. This is achieved thanks to its separable contacts. The closing and opening of the circuit allows to establish or to interrupt the circulation of current through the circuit under usual or unusual working conditions such as short circuits.

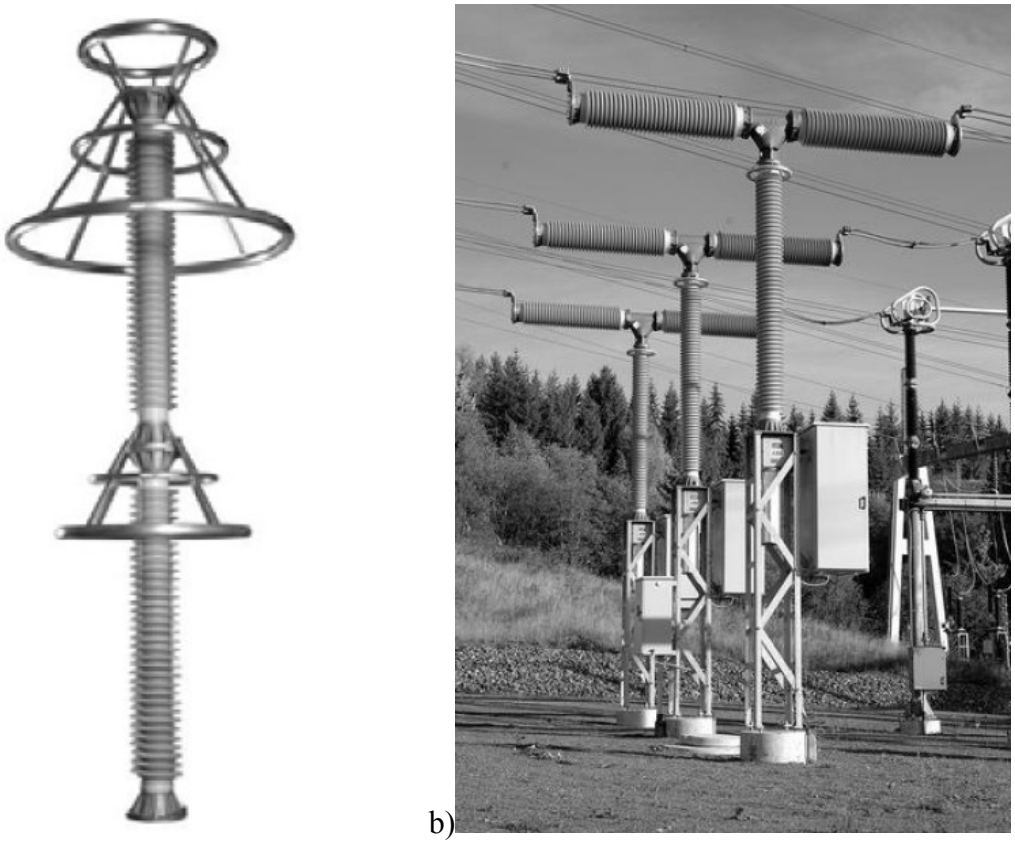
SF^6 (sulfurhexaflouride) circuit breaker is undoubtedly the most common one used nowadays for high voltage applications [106]. It has replaced air and oil circuit breakers as most SF^6 properties are superior to other interrupting mediums, such as its high dielectric strength or higher thermal conductivity.

In this kind of circuit breakers the current continues flowing after contact separation through a plasma arc of ionized SF^6. It is designed to direct a constant gas flow to the arc that extracts heat from the arc and so allows achieving its extinction at zero current. The gas flow de-ionizes also the contact gap and restores the required dielectric strength to prevent an arc re-strike.

6.2.2 Overvoltage and overcurrent protections

For the acceptance and reliability of high-voltage networks, the availability of protective elements such as surge arresters or circuit breakers is critical, making them one of the key enabling technologies.

The surge arresters (Fig. 6-10a) are the primary protection against atmospheric and switching overvoltages providing alternative path to ground or bypassing protected object. They are generally connected in parallel with the equipment to be protected to divert the surge current. The active elements (ZnO blocks) of surge arresters are manufactured using a highly non-linear ceramic resistor material, composed primarily of zinc oxide mixed with other metal oxides and sintered together [54].



a) b)

Fig. 6-10. a) Surge arrester. b) Circuit breaker. Source: [54].

There are significant differences between the requirements of ac and dc circuit breakers, mainly due to the absence of a natural current zero crossing in dc systems. DC breakers have to interrupt short-circuit currents very quickly and need to dissipate the large amount of energy which is stored in the inductances in the system.

For HVDC applications, transfer and load current switches are in use. Breakers interrupting HVDC short-circuit currents are not commonly available and have very limited ratings. The numerous presented proposals for breaker designs all comprise different series and parallel connections of classical ac interrupters, resonance circuits with inductors and capacitors, semiconductors, charging units, varistors, or resistors [107].

6.2.3 DC side pole to pole fault

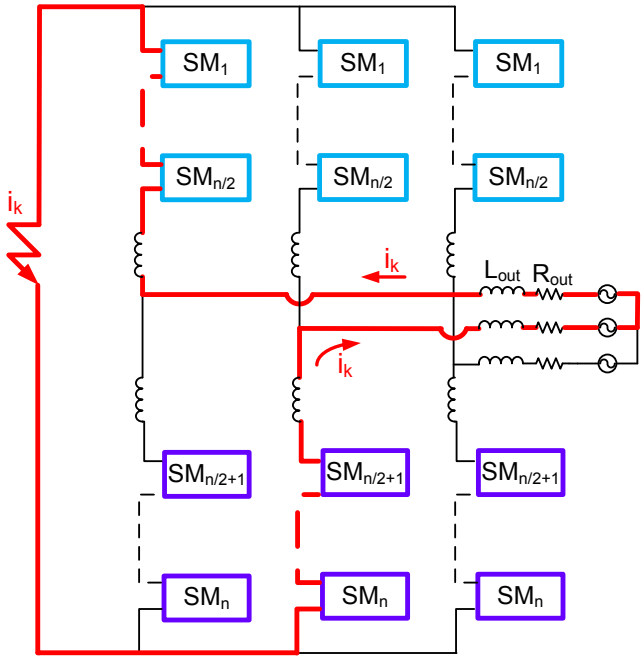


Fig. 6-11. DC side fault handling with MMC [108].

Although pole to pole faults are more frequent when DC overhead lines are used, they still have to be taken into account. The stored energy of the concentrated DC capacitors at the DC bus results in extremely high surge currents and subsequent damage if short circuits at the DC bus cannot be excluded. When a DC failure occurs, power transmission and AC grids are no more feasible. It is very desirable to affect the system as little as possible and to restart power transmission as quickly as possible.

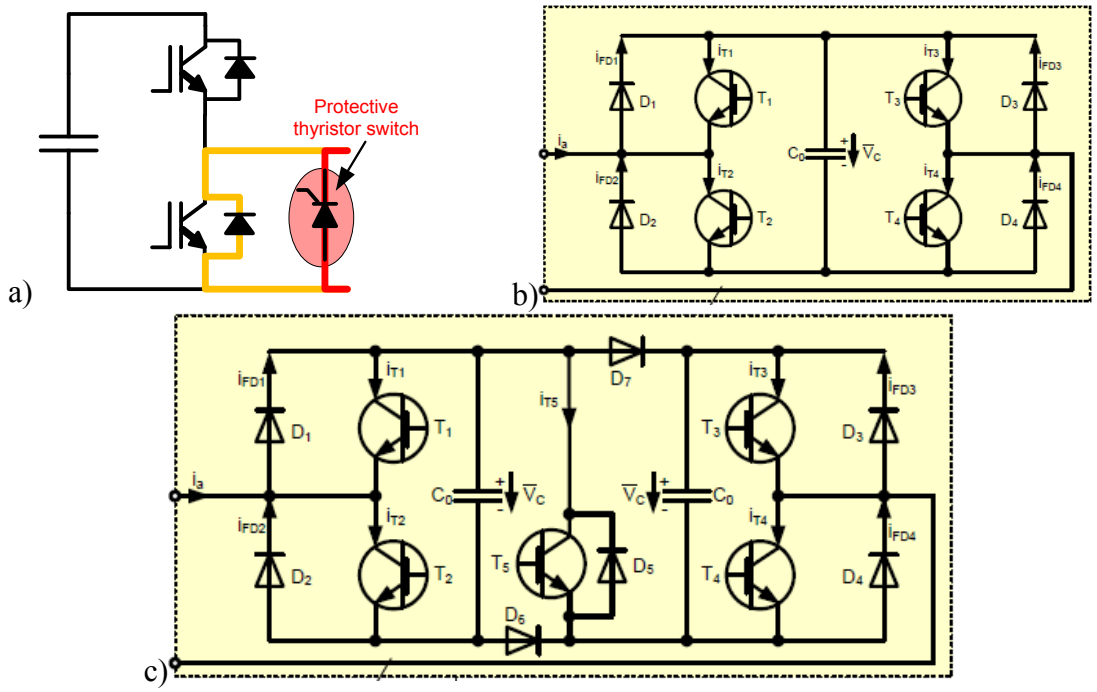


Fig. 6-12. a) Bypass thyristor. b) Full bridge cells. c) Clamp double cell. Source: [109].

Inherent to this converter topology, rated diodes and reactors would have to handle those surge currents. At first glance, limiting the DC fault currents by fast acting DC switches (mechanical or semiconductor switches) could be the best option. However, owing to physical reasons, the DC switches would be very hard to realize because they need forced arc extinction and very high energy absorption. So alternative proposed remedies:

- Bypass thyristor (Fig. 6-12a). Thanks to this solution the short circuit current does not entirely flow through the submodules diode but through the bypass thyristor as well with the aim of protecting the diodes.
- Full bridge cell (Fig. 6-12b). It can cut off arms currents of any direction by impressing appropriate polarity of terminal voltages in the arm. This can be assured in a simple manner by turning off all the IGBTs. However, comparing with the half bridge submodules, its additional switching states are not useful in normal operation because a reverse voltage polarity at the DC bus is not required for HVDC applications. Therefore, using double number of semiconductors and doubling the semiconductor losses represents a severe drawback.

Hybrid clamp double cell (Fig. 6-12c). This topology enables the desired cut off and voltage clamping functionality. In normal operation it represents an equivalent of two half bridge submodules. The total expense for the semiconductors and the resulting

losses are only slightly increased, owing to the addition of T_5, which is normally on. In case of fault currents it is turned off, resulting in voltage clamping and energy absorption. During voltage clamping, both capacitors are in parallel, ensuring minimized overvoltage.

6.2.4 Grid faults

When the voltage in the grid side is temporarily reduced due to a fault or load change in it, the voltage dip has to be faced according to the legislation in force of the country where the wind farm is installed. In electricity supply and generation, low voltage ride through (LVRT), or fault ride through (FRT), is what the electric device might be required to be capable of. The voltage may be reduced in one, two or all the three phases of the AC grid. The severity of the voltage dip is defined by the voltage level during the dip (it can even go down to zero) and its duration. For generating units such as wind turbines, the required LVRT behaviour is defined in grid codes issued by the grid operator. Taking as example the German E.On grid code, it establishes that wind farms and their equipments must keep connected if the dip characteristics match the dotted area of the voltage/time curve depicted in Fig. 6-13. In addition, they have to support the grid with a reactive power dependant on the voltage drop pertecentage.

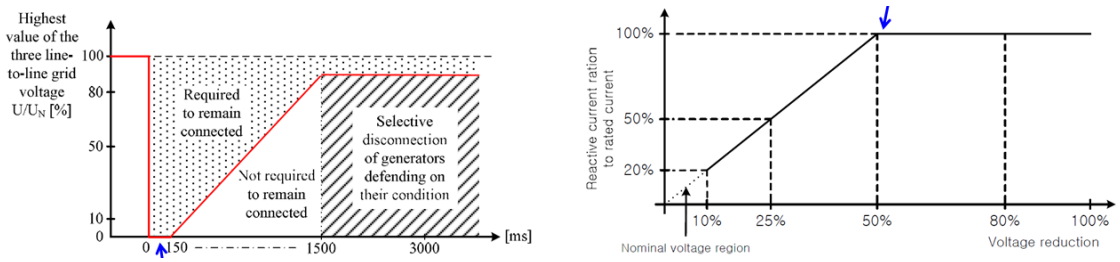


Fig. 6-13. Voltage/time curve and power factor requirement of the EON's LVRT grid code.

Wind turbines have only 100 ... 200ms fault ride through capability meanwhile onshore grid codes require interruption capability higher than 1s. Under this circumstance, the main goal is to maintain the wind farm operational, preventing at all costs the wind turbines shutdown. The difficulty then lies in what to do with the wind farm output power (as represented in Fig. 6-14) which has to be kept up during this period because there are no feasible means of storage for the excess power.

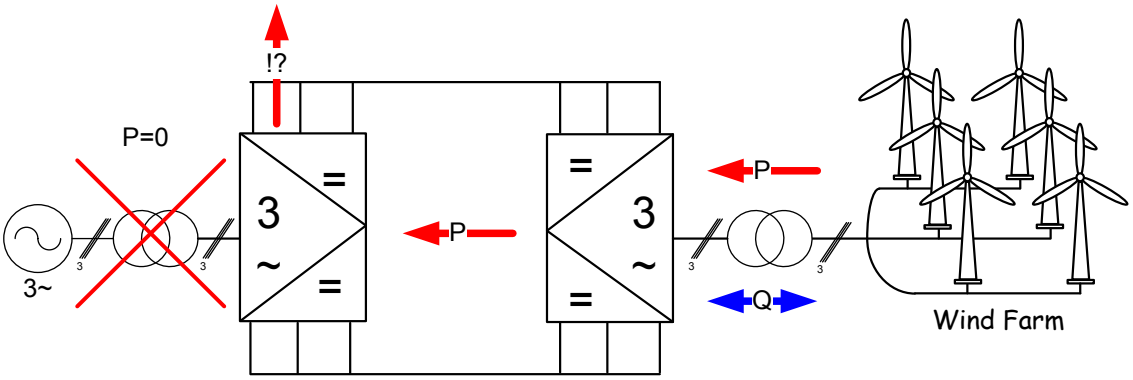


Fig. 6-14. Encountered problem when an AC grid fault occurs [108].

A possible solution is adding a DC side braking chopper unit formed by a series connection of several braking chopper modules such as the one illustrated in Fig. 6-15 and used by Siemens in its HVDC PLUS system. It consists of an IGBT, reversing diodes, a resistor to dissipate the surplus energy and a capacitor to uphold the same voltage level at the terminals of all the IGBTs. This DC chopper module topology is designed for 2L MMC but it might well be altered for alternative MMC submodules.

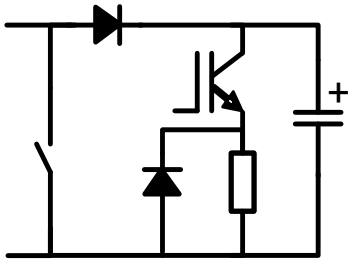


Fig. 6-15. Braking chopper module [108].

The braking chopper unit is arranged in parallel with the converter phases as depicted in Fig. 6-16. Its function is to absorb the dynamic excess power generated by the wind farm during onshore grid interruptions. However, for enduring grid faults, the wind farm may be throttled down in usual order via wind farm power control but it keeps away from the emergency shutdown. As the chopper is installed at the onshore converter station, the offshore station's footprint is not enlarged.

The features and benefits of this component are the following:

- Smooth DC voltage and current→Save fault ride through of offshore wind farm.
- Redundant design→High reliability.
- Use of well-proven standard components→High availability of state of the art components.
- Design & control scheme derived from HVDC PLUS→Power Module Synergy with Power Module in development and production.

- Easy scalability → Low engineering efforts
- Low number of primary components → Low maintenance requirements

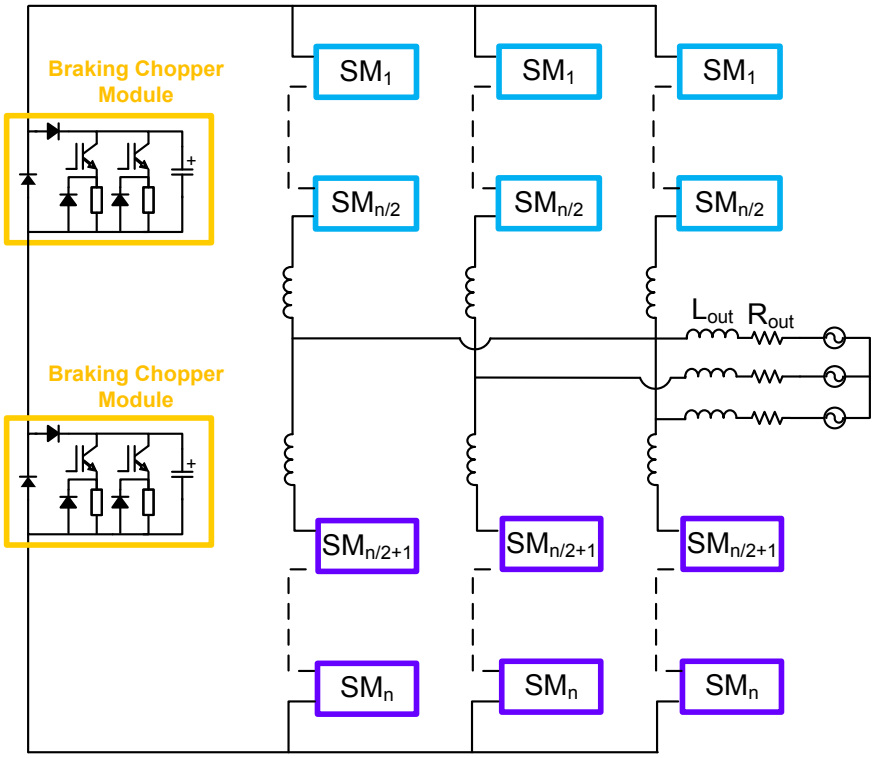


Fig. 6-16. Converter layout incorporating the breaking chopper module [108].

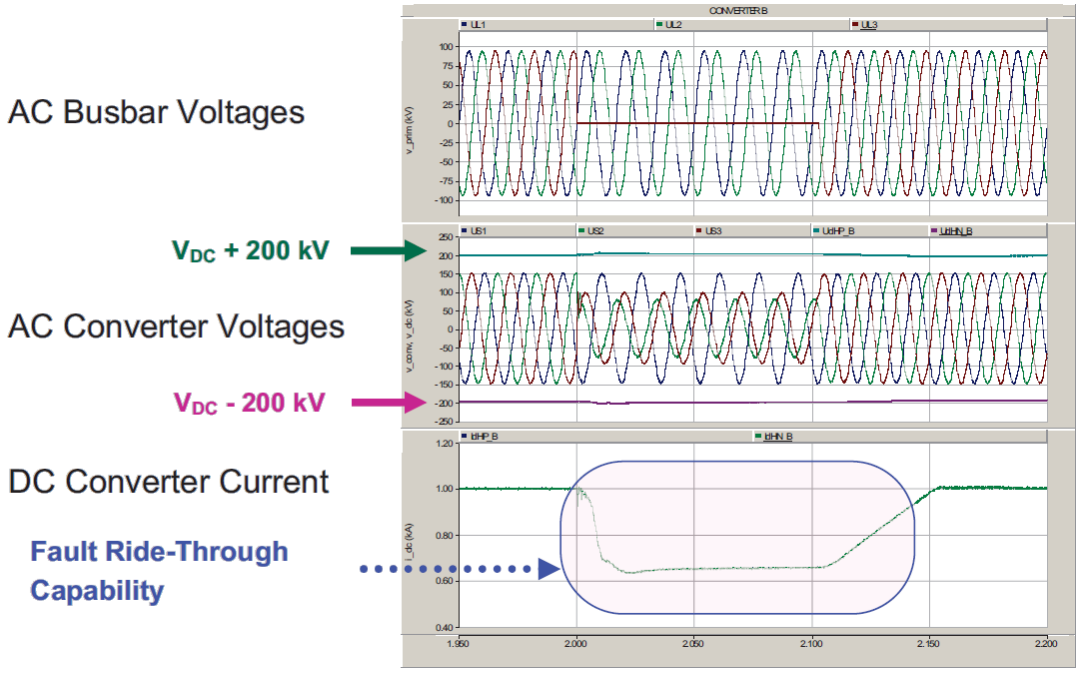


Fig. 6-17. Close AC line to ground fault in the inverter side. Source: [108].

A demonstration of an AC line to ground fault and the recovery of the system are represented in Fig. 6-17. In the first graph how the voltage of line 3 drops to zero for a short time interval can be observed. When it occurs, the converter changes its operating

mode (look at the AC converter voltages) in order to accomplish the imposed requirements for that situation without disconnecting the wind farm. In the bottom graph the FRT behaviour is appreciated thank to which after the dip clearance the system is able to return to the normal state.

6.2.5 Failure management in submodules

Failures in electronic devices are quite usual, sometimes because of its end of life but others unexpectedly. The malfunction of a little device can bring the whole apparatus to a standstill or provoke damages to the rest of the components. Such event is always undesirable but the consequences are aggravated in equipments located on offshore stations. The main reason is that maintenance staff has to move by boat to the station where not only the working conditions and accessibility are harder but costs are also driven up. So the fewer trips required to the station the better. That is why it is interesting to analyze which penalties could be caused by a submodule's fault in the MMC.

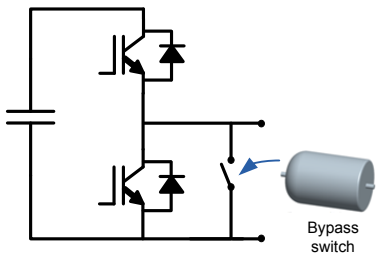


Fig. 6-18. 2L submodule including a bypass switch.

Regardless the submodule topology, when any of the elements which constitute it breaks down, it is assumed that it drops to failure mode without damaging anything else. Moreover the whole submodule must be short-circuited to let the rest of the converter continue working (a high speed bypass switch like in Fig. 6-18 is typically used for such purpose). Although some redundant submodules are installed in the converter to avoid unscheduled repair service, it is not possible to install many of them due to the space requirements and costs above all. Therefore, it is interesting to find out what would happen in the worst case when there are no more spare submodules left until it gets repaired or replaced by a new one.

From the moment that a submodule remains short-circuited, its output voltage will be always zero. For this reason the arm signal instead of having *(n/2+1)* levels, it will be formed by a level less per submodule broken down. Such case is represented in Fig. 6-19 (simulation in per unit of a MMC with 2L submodules being *n=10*) where one of the five upper submodules is not operating. As can be observed, V_l is a 1V amplitude signal formed by six levels meanwhile V_u is a signal formed only by 5 levels and whose amplitude cannot reach the one volt. Obviously, the converter output voltage V_{th} gets

affected. Not only is the amplitude reduced due to the lack of voltage levels but the shape of the signal is also altered.

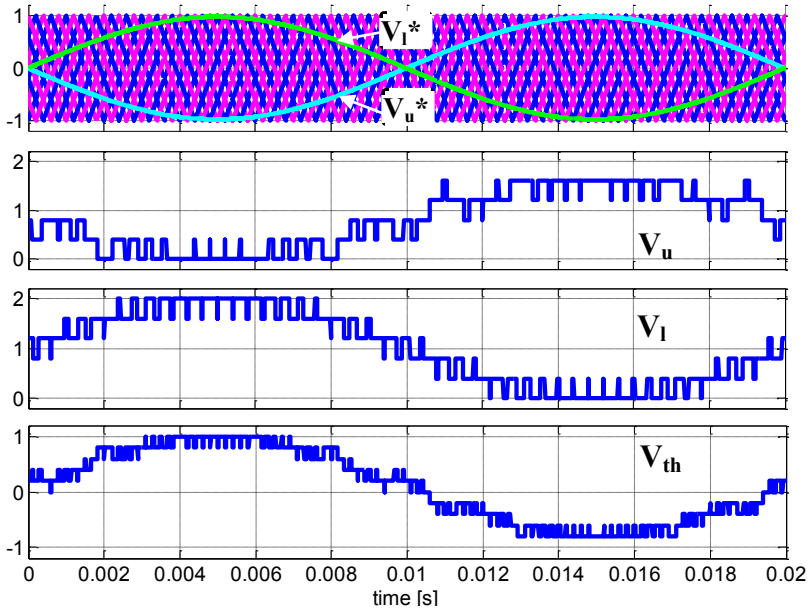


Fig. 6-19. Modulator references and carriers, voltages of upper and lower submodules and output voltage of a single phase MMC with 5 submodules per arm with failure in the first upper submodule, *ma=1*, V_{DC}*=2* volts and f_{sw}*=500 Hz.*

The spectrum of the V_{th} signal of a single phase MMC with 5 submodules per arm with failure in an upper submodule is depicted in Fig. 6-20 (with zoom at low frequencies). As explained in chapter 2 its first harmonic band come into view at *n* times the switching frequency (f_{1hb}*=12.5 kHz* in this example) fulfilling the equation (2-22). However, if the spectrum of Fig. 6-20 is compared with the one of Fig. 5-4 which is taken from the same MMC without failures in the submodules, it can be noticed that there is a new family of harmonics at low frequencies which belongs to the switching frequency, 1250 Hz in this example. It is obvious that this fact deteriorates the output voltage, but what really cannot be acceptable for the proper operation of the converter is the continuous voltage of this signal.

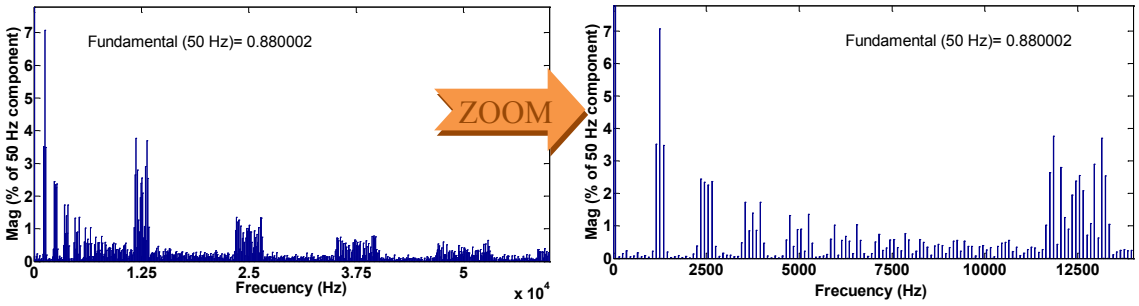


Fig. 6-20. Spectrum of V_{th} of a single phase MMC with 5 submodules per arm with failure in the first upper submodule, f_{sw}*=1250 Hz* and V_{DC}*=2 volts*.

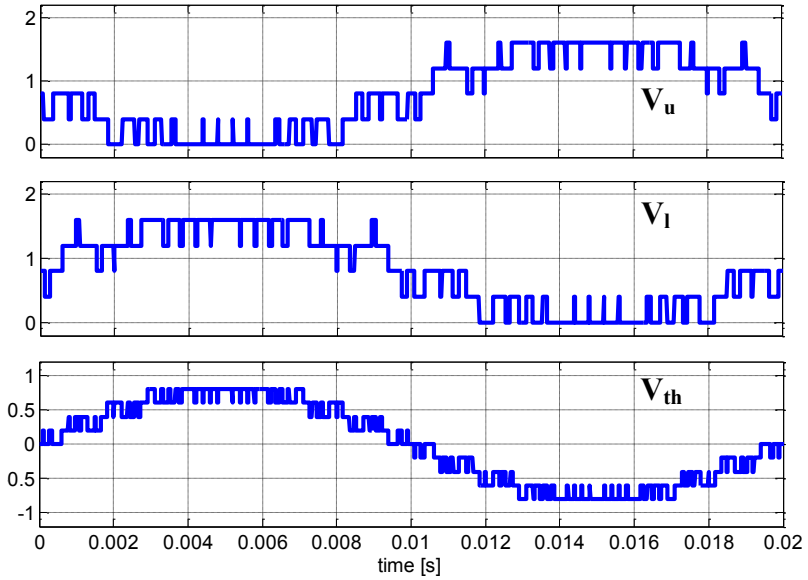
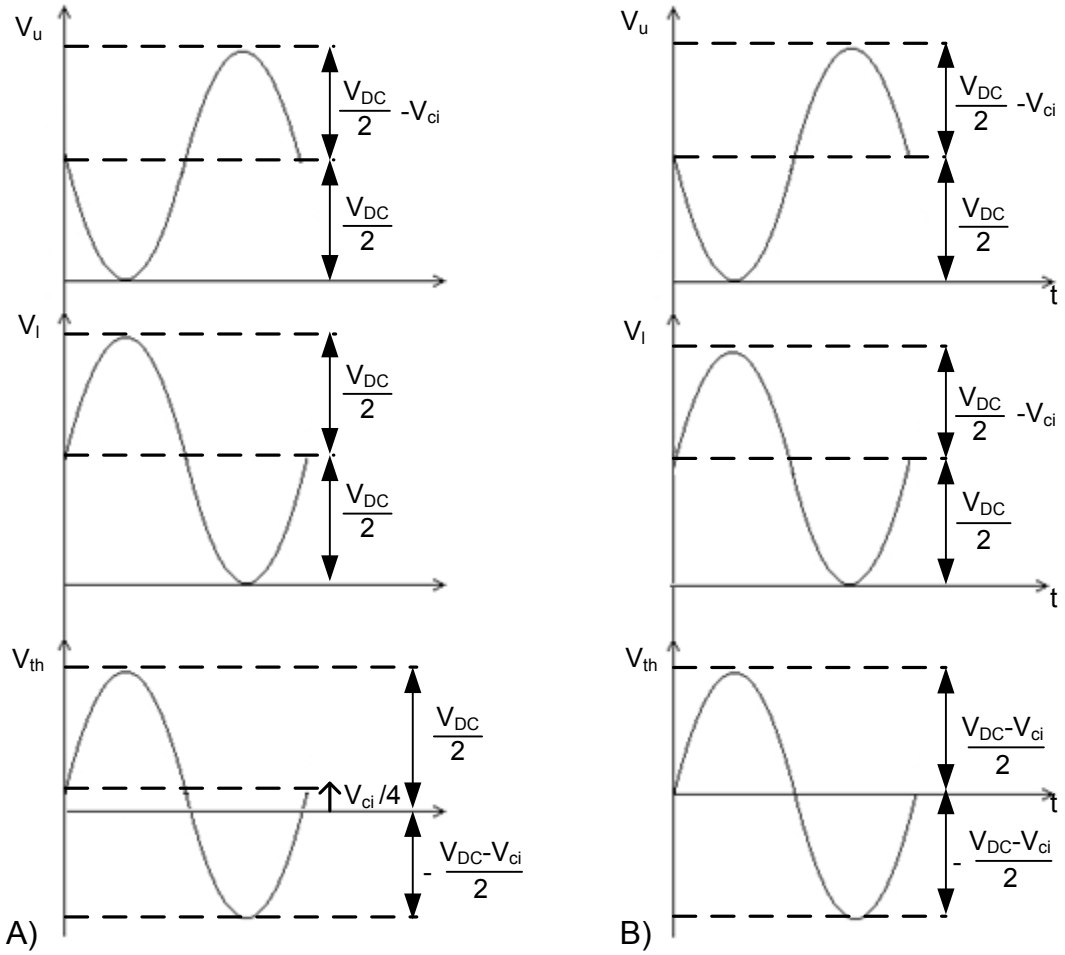


Fig. 6-21. Voltage of upper and lower submodules and output voltage of a single phase MMC with 5 submodules per arm with failure in the first upper and first lower submodule, *ma=1*, V_{DC}*=2V* and f_{sw}*=500 Hz.*



6-22. a) Output voltage and upper and lower submodules voltages in a MMC with failure in an upper submodule. b) Output voltage and upper and lower submodules voltages in a MMC with failure in one upper submodule as well as in one lower submodule.

Whenever a submodule breaks down, the simplest way of getting rid of the continuous voltage at the output of the converter is short-circuiting another submodule of the opposite arm. Therefore the same number of submodules in each arm will be missing and V_{th} will not present any offset as demonstrated in Fig. 6-21. The main disadvantage is that the total output voltage amplitude is reduced in another V_{ci} level. With the aim of making the comprehension of failure modes easier, these two cases are depicted in the general diagrams of 6-22.

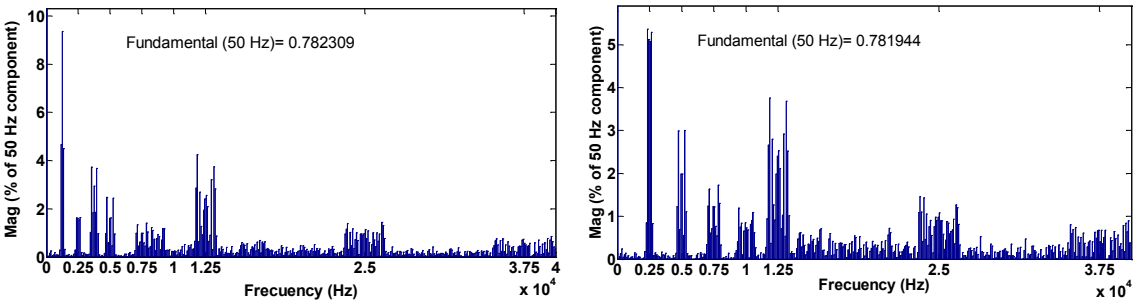
		Position of the short-circuited submodule in the lower arm				
		1	2	3	4	5
f_{sw}	250 Hz	**0,009678**	0,019616	0,033372	0,032150	0,021130
	500 Hz	**0,004468**	0,009513	0,015249	0,015249	0,009513
	750 Hz	**0,002897**	0,006218	0,010013	0,010059	0,006288
	1000 Hz	**0,002171**	0,004686	0,007504	0,007504	0,004686
	1250 Hz	**0,001795**	0,003773	0,006012	0,006001	0,003748
	1500 Hz	**0,001440**	0,003123	0,004989	0,004989	0,003123
	1750 Hz	**0,001288**	0,002652	0,004266	0,004280	0,002695

Table 6-1. WTHD of V_{th} according to f_{sw} and the position of the short-circuited submodule in a MMC being *n=10* with failure in the first upper submodule.

		Position of the short-circuited submodule in the upper arm				
		1	2	3	4	5
f_{sw}	250 Hz	0,021130	0,030819	0,031204	0,020796	**0,009097**
	500 Hz	0,009513	0,015239	0,015227	0,009479	**0,004319**
	750 Hz	0,006288	0,010065	0,010063	0,006267	**0,002884**
	1000 Hz	0,004686	0,007506	0,007499	0,004677	**0,002176**
	1250 Hz	0,003748	0,005993	0,005998	0,003749	**0,001758**
	1500 Hz	0,003123	0,005006	0,004990	0,003115	**0,001466**
	1750 Hz	0,002695	0,004321	0,004298	0,002677	**0,001261**

Table 6-2. WTHD of V_{th} according to f_{sw} and the position of the short-circuited submodule in a MMC being *n=10* with failure in the fifth lower submodule.

Once known that it is necessary to have the same number of submodules operating in both upper and lower arm, what has to be determined now is which of the opposite arm's submodule is more convenient to short-circuit. For that, the values of the WTHD of a MMC with five submodules per arm have been compared. First, a failure in the first upper submodule has been set and the WTHD values of the converter's output voltage have been gathered in Table 6-1depending on which lower submodule is short-circuited. Then (see Table 6-2), the failure has been set in the fifth lower submodule and the WTHD values have been calculated varying the upper submodule in which the short-circuit is forced. After having evaluated all the possibilities, it is deduced that the best option is to disregard the same submodule of the opposite arm than the one broken down because the weighted total harmonic distortion in that case is the minimum in the two tables.



a) b)

Fig. 6-23. Spectrum of V_{th} of a single phase MMC with 10 submodules, f_{sw}=1250 Hz and V_{DC}=2V. a) With failure in the first upper and fifth lower submodule. b) With failure in the first upper and first lower submodule.

Comparing the two spectrum obtained in Fig. 6-23, which both refer to the same converter with failure in the first upper submodule but different short-circuited one in the lower arm, it can be noticed why the calculated WTHD values are different. Paying attention to frequencies lower than 10 kHz, if the damaged submodule is not in the same arm position than the short-circuited one, the first significant harmonic appears at switching frequency and repeats every f_{sw} (see Fig. 6-23a). Nevertheless, if their position matches up, the quality of the signal improves a little because low frequency harmonics appear every $2{\cdot}f_{sw}$ instead of every f_{sw} as can be checked in Fig. 6-23b.

Taking up the HVDC application again, in Table 6-3 the signal quality parameters calculated for a submodule failure of four different MMC examples are added. In case a great number of submodules are needed to comply the converter requirements, it is evident that under normal conditions the quality of the output signal will almost be affected because of a failure in one submodule since that quality was already good enough (remember than in chapter 5.1.2 from $n=32$ 2L topology ($WTHD=0.1908e\text{-}4$ at $f_{sw}=500$ Hz), the obtained signal was considered top-quality). Nonetheless, considering the MMC configuration where 8 IGBTs per valve are serialized, the total number of submodules in the converter decreases considerably and any change on the signal levels can be important. For instance, in the first example of Table 6-3 in which the number of submodules per phase is 36, if the converter is working properly its WTHD is lower than 0.1908e-3 (the one considered good enough). Otherwise, if a submodule fails and consequently another one of the opposite arm has to be short-circuited, the WTHD value rises roughly ten times exceeding the optimum value.

Submodules topology	Voltages (kV)	n	Normal conditions		1 submodule less/arm	
			WTHD	THD	WTHD	THD
2L-VSC MV with 8 IGBTs serialized per valve	V_{DC}=400 $V_{AC(LL\text{-}rms)}$=276	36	1.08e-4	3.25e-2	1.25e-3	4.29e-2
	V_{DC}=640 $V_{AC(LL\text{-}rms)}$=444	58	6.81e-5	2.02e-2	7.43e-4	2.69e-2
2L-VSC MV without serialization	V_{DC}=400 $V_{AC(LL\text{-}rms)}$=276	288	6.34e-5	4e-3	1.6e-4	5.42e-3
	V_{DC}=640 $V_{AC(LL\text{-}rms)}$=444	458	4.25e-5	2.5e-3	1.11e-4	3.54e-3

Table 6-3. THD and WTHD under normal conditions and with a damaged submodule evaluated in two converters with different submodules topology.

The defects which appear in the voltages are caused by the modulation algorithm. It is prepared for a specific number of submodules but not for failure cases. Therefore when any of the submodules is under failure mode there is an extra triangular carrier in the modulator. The intersection of that triangular signal and the reference involves a commutation of the submodule out of work which consequently provokes some inadequate switching actions as can be observed in Fig. 6-19 or Fig. 6-21. Not only do these imperfections occur with the typical PWM but also with the modulation explained in this document. In order to avoid these imperfections that worsen considerably the output signal's quality, in those applications with low number of submodules where the quality has great importance, it is worth reconfiguring the modulator despite losing amplitude in the AC signal.

Apart from the solution aforementioned, instead of forcing a short-circuit in the opposite arm's submodule, the offset can be removed by means of the control system. In Fig. 6-24 what happens in the control system when a submodule of the upper arm fails can be seen. There is a semi period where the V_u voltage cannot reach the total amplitude of its reference due to the lack of voltage contribution of the submodule which is broken down. As said before, this fact causes an offset in the output voltage due to the decrease in its amplitude.

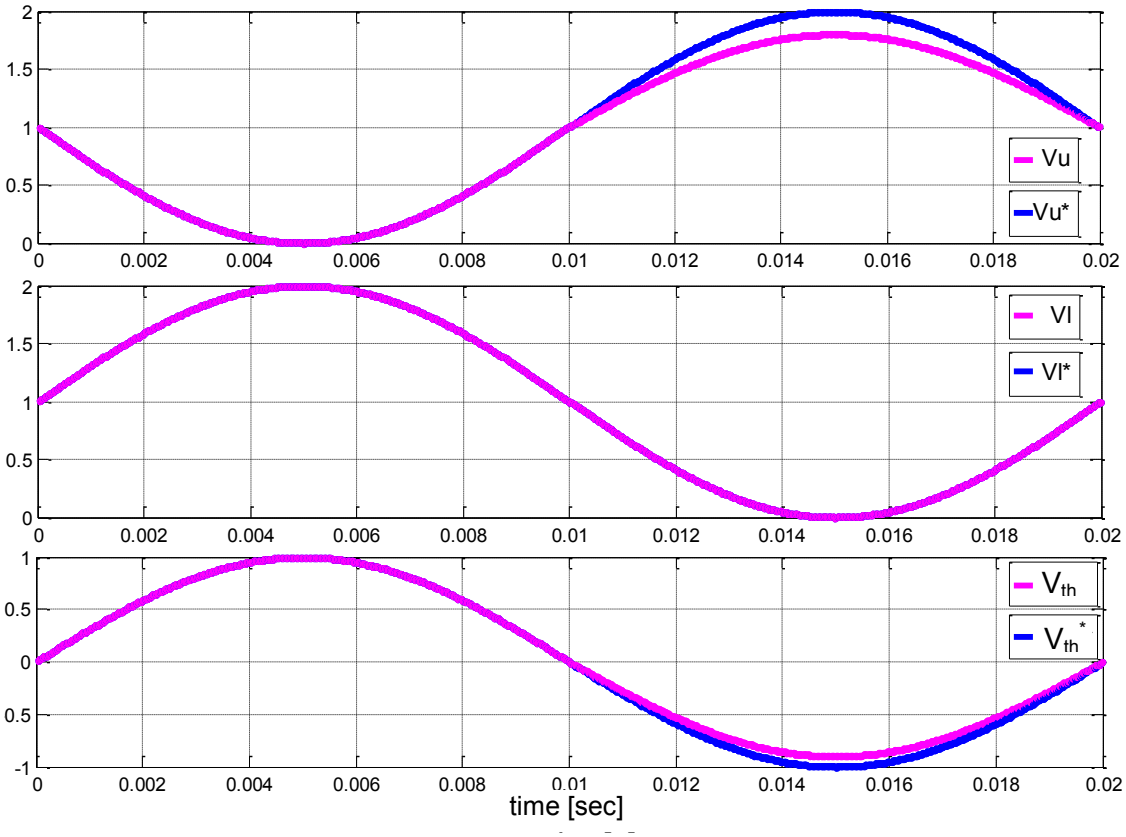


Fig. 6-24. Voltage of upper and lower submodules, output voltage as well as its references of a generic single phase MMC with failure in an upper submodule, *ma=1* and V_{DC}=2V.

If the reference V_u* is adjusted to the maximum amplitude reachable with the number of operative submodules in the arm as shown in Fig. 6-25, the result is a sinusoidal output voltage V_{th} without offset. This way the references can be followed by its voltages during all the period without any problem. However, according to the signal's quality, whenever the modulation algorithm is not modified to make the number of triangular signals equal to the number of active submodules, the solution of short-circuiting an opposite arm's submodule is better than adjusting the control loop. The reason is that when the same submodules are left in both arms, the irregularities caused by wrong commutations due to the extra triangular are compensated. On the other hand, when adjusting the control loop, the imperfections of one of the arms affect the output signal worsening its quality.

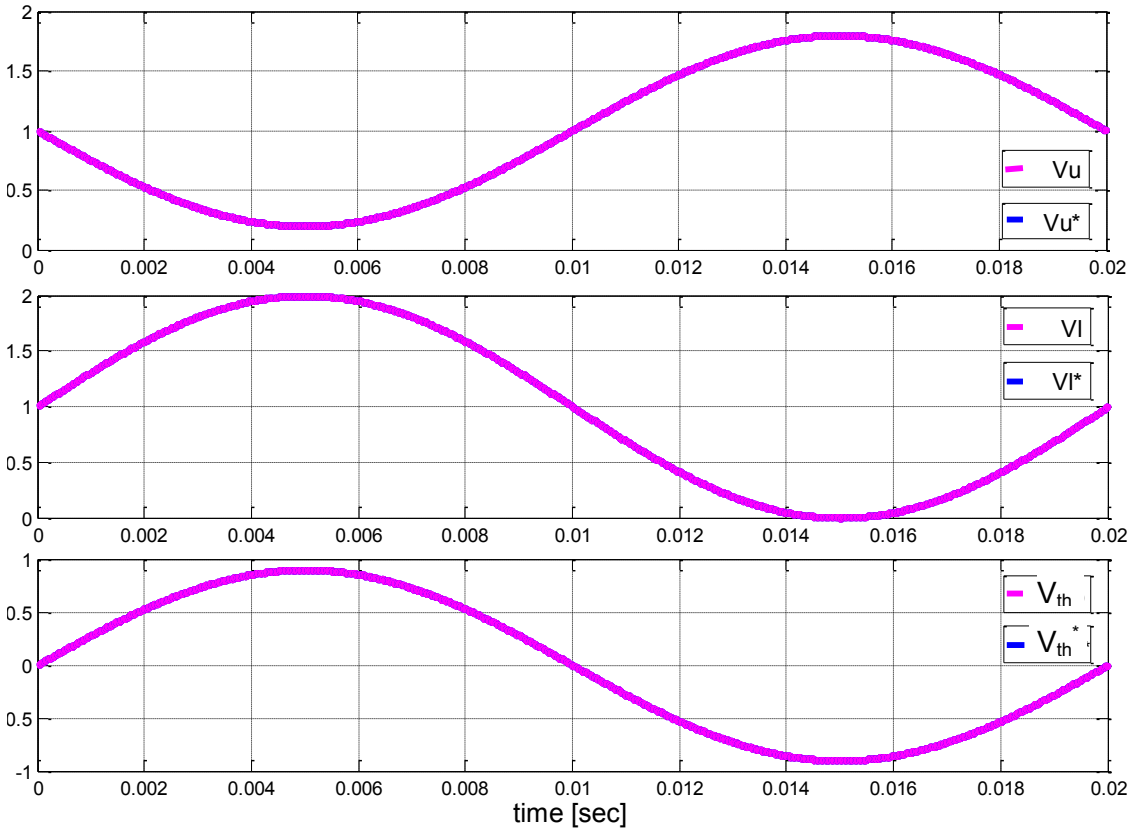


Fig. 6-25. Voltage of upper and lower submodules, output voltage as well as its references of a generic single phase MMC with failure in an upper submodule, *ma=1* and $V_{DC}=2V$. The control system is adjusted to the number of active submodules.

6.3 Conclusions

Regarding the precharge of the submodules capacitors, all the found choices agree that an external voltage source is needed for that purpose. The first most viable option consists of connecting each submodule by means of some thyristors to a DC voltage source and triggering these semiconductors precharge the capacitors synchronously. The second one instead, suggests charging them from the main voltage source just connecting in series to the arms some resistances controlled by a switch. Although the second one seems to be simpler, it is protected by a patent and it is not useful for any submodule concept.

It has been deduced that the arrangement of the components is of vital importance in this kind of converters. On the one hand, particularly the converter placed at the offshore substation has to occupy as little space as possible. However, on the other hand, isolation distances among elements with high potential differences must be respected. Moreover, not only should it incorporate protective elements against electrical faults (overvoltages, overcurrents, AC or DC side failures) but also

mechanical reinforcements to prevent any collapse of the structure, for instance due to seismic movements.

Continuing with protective measures, MMC manufacturers taking for granted unexpected damages in electronic devices, incorporate several redundant submodules to avoid unplanned shutdowns. Nevertheless, it could well happen that there may be more destroyed than redundant submodules. The research conducted about this topic determines that unequal number of submodules in the arms of the same phase provokes an undesirable DC voltage at the output waveform. The simplest remedy lies in identifying the position of the broken device and short-circuiting the counterpart submodule in the opposite arm. Instead of that, if the control parameters could be modified, another solution would be adjusting the arm references (V_u*, V_l*) to the maximum amplitude reachable with the number of operative submodules in the arm. However, it would be even better reconfiguring carriers generation in the modulator to avoid undesired commutations.

Chapter 7

Conclusions and future work

7.1 Conclusions

With increasing attention to sustainable development and environmental protection, the application of renewable energy is the proposal to reduce the dependence on fossil fuels. The integration of the energy generated by large scaled offshore wind farms more effectively than with existing AC networks, is a new challenge. Many investigations concur in stating that VSC-HVDC is the most attractive option for high power and long distances. It is concluded that this thesis is focused on the MMC for the benefits that it presents over the two level converter.

The principal weakness of this converter topology is the unbalance that appears among the submodules capacitors causing disruptions in the proper operating of the converter. One of the general objectives of this thesis was to find a solution to this trouble. It is effectively solved with the implementation of a PSPWM based balancing strategy, which detects when a commutation has to be completed but toggles the submodule whose capacitor voltage is furthest from the balancing value. Successful simulations as well as experimental results confirm the latter statement.

Typically, the MMC is comprised of 2L half bridge submodules. However, thinking about high voltage applications in which high number of submodules per phase is required, it could be interesting to use multilevel submodules instead. Therefore, the implementability and effectiveness of the developed modulation algorithm is also verified in the MMC with 3L-FC and 3L-NPC multilevel submodule concepts so as to fulfil the second objective established in this research work. In addition, a comparison revealing the benefits and drawbacks of using the proposed different submodule

concepts is carried out. It concludes that the best advantage of the multilevel submodule concept compared to the classic 2L submodule, is that the number of submodules can be reduced, leading in turn to a significant reduction of elements associated to the submodule (thyristors, bypass switches, optical fibres, etc..), potentially reduction in the volume and assembling process of the converter. It can also significantly improve important issues of HVDC applications such as: firing orders, implementation complexity, modulation complexity, etc…

7.2 Contributions

The main contributions of this thesis have been:

- The modelling of the MMC by means of differential equations which describe the dynamic of its most relevant variables. This provides to develop good understanding about the behaviour of the system but also to design the appropriate control system and the suitable modulation technique. Not only is the modelling valid for 2L submodules but it can easily be extended to 3L-FC and 3L-NPC submodule concepts.
- The development of a modulation algorithm which solves the submodules capacitors unbalancing problem. In this case, it is based on the PSPWM modulation technique but actually it is applicable to anyone employed for multilevel converters. It has been designed in such a way that, a prior analysis of the specific converter arrangement is not necessary to identify redundant voltage combinations. Thus, the adaptation of the algorithm to arrangements of MMC with a different number of submodules is straightforward. In addition, it is easily adaptable to arrangements of MMC with different multilevel submodule concepts.
- Experimental validation of the capacitors balancing strategy in the laboratory downscaled MMC test bench, first with 2L submodules and then with 3L-FC.
- Comparison and evaluation of different submodule concepts for MMC applying a procedure that is mainly focused on a thermal analysis and sizing of the converter elements, showing the advantages and disadvantages among them.
- To find solutions to some problems associated with disturbances, either for specific characteristics of the converter or simply because failures. As the

submodule is a vital element of the MMC, the consequences for the converter operability resulting from submodule breakages and some remedies are explained in detail.

7.3 Future work

In this section several future lines of research are proposed as a continuation of the work developed in this report:

- A detailed 3 phase MMC design for a specific application in which every single component should be defined. Besides selecting the semiconductors, capacitors and inductances many other important elements have to be configured: the cooling system, voltage sources for the capacitors precharge, connection plates and cables, measurement boards, etc. Moreover the arrangement of all these components is crucial in order to minimize the overall size, but at the same time the minimum distances among elements have to be observed with the aim of guaranteeing the isolation.
- Analysis of the converter internal control loops strategies to regulate the total capacitors voltage by means of the average current through the phase or the transmitted active power. Dynamics, stability, advantages, disadvantages of different control strategies should be examined.
- Simulation of a complete wind farm with HVDC transmission comprising the model of several wind turbines, cables, transformers and converters at both ends. Then, the most suitable coordinated control for the whole system should be determined.
- After implementing a coordinated control technique and the modulation algorithm proposed in this thesis, it would be interesting to analyse the behavioural of the whole system under different operation conditions such as variable wind speed, voltage dips at the connection point, breakage of transmission cables...Obviously grid code requirements should be fulfilled in all these cases.
- Study of the data communication between converter's measurement boards and the overall management system regarding a three phase MMC with hundred submodules per arm. A research on the viability of different powerful hardwares

which can collect, process and manage all the received information as well as the implemented modulation algorithm must be done.

- Study of alternative applications that this converter topology can have in which just reactive power is exchanged, for instance FACTS such as STATCOMs, grid balancers, active filters, etc.

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Appendix

Power flow

An analysis about power flow in the Modular Multilevel Converter has been carried out. Thus, the converter is simplified as done before by means of Thévenin's theorem, so that, the circuit that will be analysed consists only of two voltage sources and an inductance connected in series (the resistor is omitted in this case) as represented on Fig. A-1.

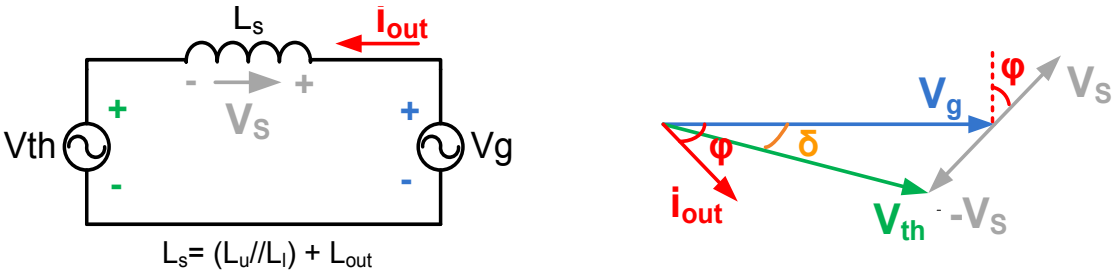


Fig. A-1: Simplified circuit and vector diagram of the MMC.

First of all, the sign convention used along this section will be explained because it is essential to avoid confusion:

- The output current i_{out} is considered positive from the grid toward the converter as drawn in Fig. A-1. This means that the converter absorbs active power when $P>0$ but it gives when $P<0$.
- The reactive power is positive when the current i_{out} is behind the grid voltage V_g, this is, when φ angle is negative.
- δ is defined as the angle between both V_{th} and V_g voltages. It is measured from V_{th} to V_g.

Next three equations about voltages (A-1), active (A-2) and reactive power (A-3) are deduced from the circuit and diagram of Fig. A-1.

$$V_{th} = V_g - V_S \tag{A-1}$$

$$P = V_g \cdot I_{out} \cdot \cos\varphi \tag{A-2}$$

$$Q = -V_g \cdot I_{out} \cdot \sin\varphi \tag{A-3}$$

Using the sine theorem and other trigonometric identities, the equations of active and reactive powers on the grid can be achieved, (A-4) and (A-5) respectively. These depend on voltages V_{th} and V_g of the circuit, as well as the phase shift between them.

$$P = \frac{V_g \cdot V_{th}}{X_L} \cdot \text{sen}\delta \tag{A-4}$$

$$Q = \frac{-V_g \cdot \left(V_{th} \cdot \cos\delta - V_g\right)}{X_L} \tag{A-5}$$

$$\text{Where: } X_L = 2 \cdot \pi \cdot L_s = 2 \cdot \pi \cdot \left(L_{th} + L_{out}\right) \tag{A-6}$$

Variation of the active power when *Q=0*

This section deals with modifying the active power delivered or absorbed from the grid without reactive power flow. The reactive power will be zero according to (A-5) when the expression (A-7) is fulfilled. This fact happens every time i_{out} and V_g have got the same or the opposite phase (see Fig. A-2), which means that the angle $\varphi=0^o$ or 180º because the projection of V_{th} on x axis has got the same value than grid voltage.

$$V_{th} \cdot \cos\delta - V_g = 0 \tag{A-7}$$

As X_L is fixed by the inductances of the circuit, more or less current flow must be forced along the circuit in order to achieve different active powers. Hence the angle between the two voltages varies with the module of V_s causing changes in the active power. If

$\delta=0$, there is not voltage drop in the inductance because there is not any current circulation and consequently the active power will be null.

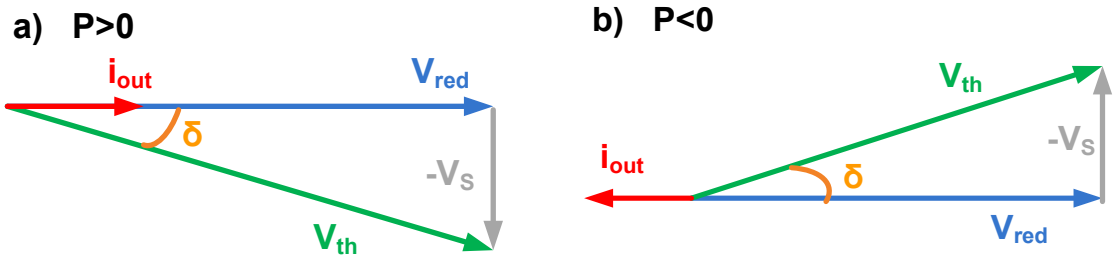


Fig. A-2: a) Vector diagram for *P>0*. b) Vector diagram for *P<0*.

Variation of the active power when *P=0*

It deals with modifying the reactive power delivered or absorbed from the grid without active power flow. The reactive power will be zero according to (A-4) when the δ angle (the angle between V_g and V_{th}) is zero, that is, whenever both voltages are in phase as shown in Fig. A-3. Therefore the value of Q depends on the subtraction of these two voltages as can be deduced from equation (A-5). The result of this subtraction is the voltage V_s that changes according to the current which circulates along the converter.

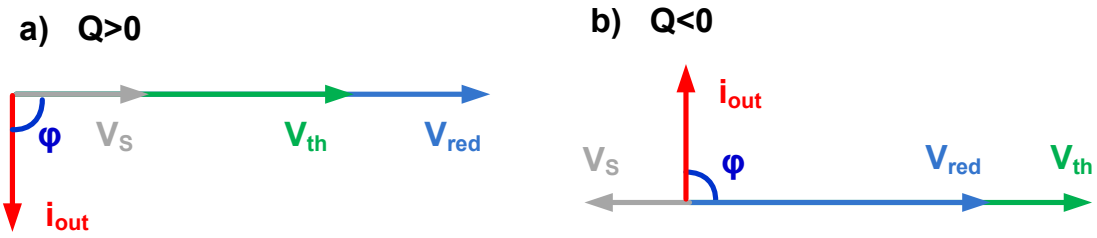


Fig. A-3: a) Vector diagram for *Q>0*. b) Vector diagram for *Q<0*.

Variation of the active and reactive power

In the previous sections, two special features about the power flow are detailed, specifically how to vary the active or reactive power separately, keeping one of them to zero. However, in this section the four power possible working cases depicted in Fig. A-4 will be verified by means of some numeric examples.

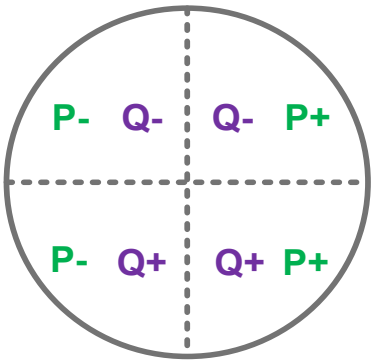


Fig. A-4: The four quadrants of power.

Setting one of those two powers to zero makes

the unknown parameters calculation easier. However, for the remaining cases the calculation of these unknown parameters is a bit more complex, it depends on the variables known. Next, the steps which have been followed to obtain V_{th} and δ knowing the value of V_g, i_{out} and φ are detailed.

From equations (51) and (52), *sin(δ)* and *cos(δ)* are worked out respectively. Then, Pythagorean's identity (A-10) is applied so that the value of V_{th} is obtained (A-11). Finally, V_{th} is substituted in (A-8) to get δ.

$$\sin\delta = \frac{P \cdot X_L}{V_g \cdot V_{th}} \tag{A-8}$$

$$\cos\delta = \frac{-Q \cdot X_L + V_g{}^2}{V_g \cdot V_{th}} \tag{A-9}$$

$$\sin^2\delta + \cos^2\delta = 1 \tag{A-10}$$

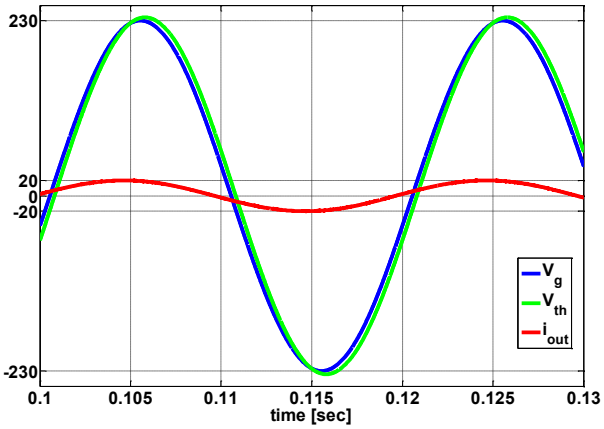
$$V_{th} = \frac{\sqrt{\left(P^2 + Q^2\right) \cdot X_L{}^2 + V_g{}^4 - 2 \cdot Q \cdot X_L \cdot V_g{}^2}}{V_g} \tag{A-11}$$

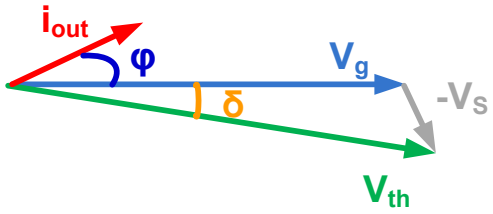
All these equations have been checked by means of some simulations in Matlab-Simulink software. These simulations have been conducted in a single phase MMC with 8 submodules in which all submodules capacitors have been substituted by ideal voltage sources, with the aim of avoiding disturbances and the results could match up.

In Fig. A-5 simulations as well as numerical results are illustrated. Starting from V_g=*230V*, I_{out}=*20A* and φ angle data, all the other variables (active and reactive power, V_{th} and δ) are calculated with the equations presented before. Four different φ angles have been considered to validate it on the four quadrants of power.

It is hard to appreciate exactly the voltage difference between V_g and V_{th} signals and also the phase shift in the figures, but it can be seen whether V_{th} is greater than those 230 volts of grid voltage and which is some degrees behind the other. As settled, the maximum value of I_{out} is always 20 amperes and the phase shift matches up with numerical results.

a) φ=10º





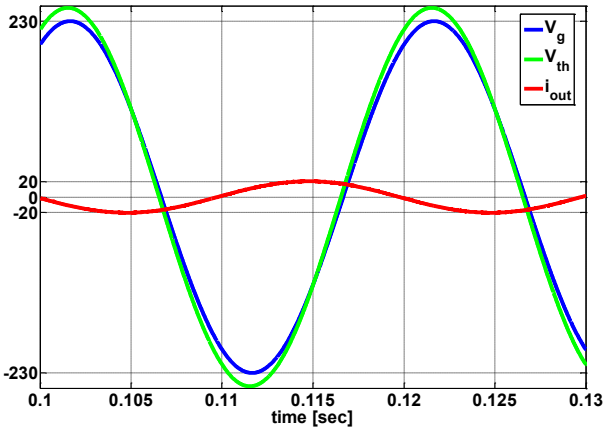
P = 2.265 KW

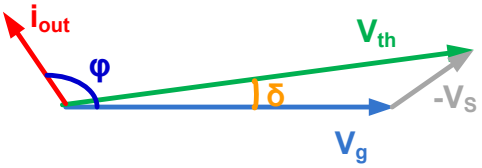
Q = −399.4 VAR

V_{th} = 234.2 V

δ = 0.079 rad = 4.5º

b) φ=120º





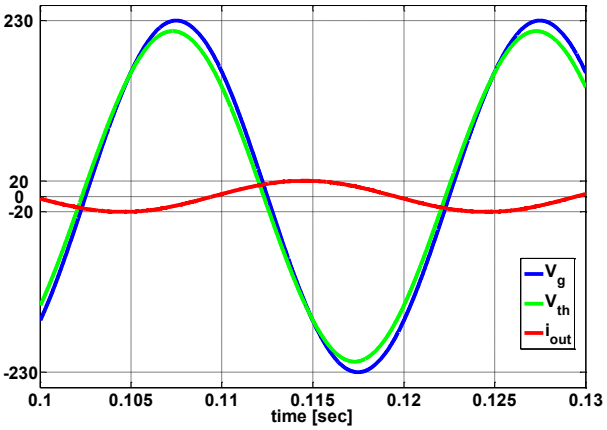
P = −1.15 KW

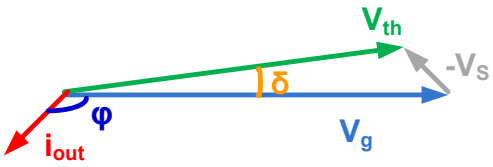
Q = −1.99 KVAR

V_{th} = 247.43 voltios

δ= −0.038 rad = −2.18º

c) φ=225º





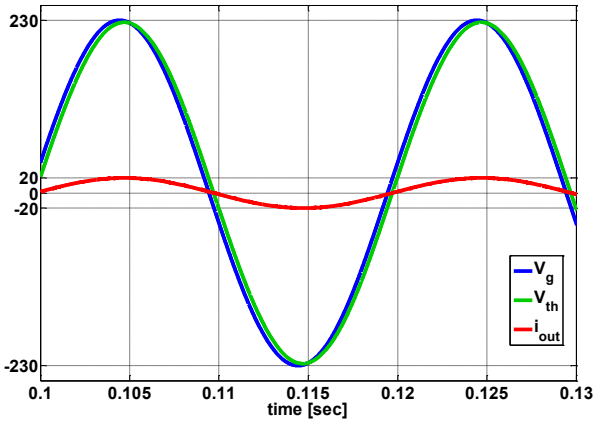
P = −1.63 KW

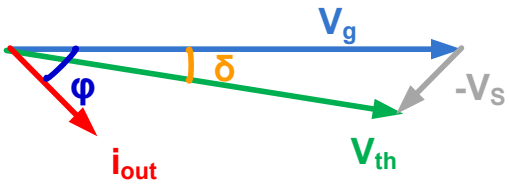
Q = 1.63 KVAR

V_{th} = 216.22 voltios

δ = −0.062 rad = −3.53º

d) φ=350º





P = 2.265 KW

Q = 399.39 VAR

V_{th} = 227.28 voltios

δ = 0.082 rad = 4.68º

Fig. A-5. a) Output current, grid and Thévenin voltages, vector diagram and parameters for *φ=10º*. b) Output current, grid and Thévenin voltages, vector diagram and parameters for *φ=120º*. c) Output current, grid and Thévenin voltages, vector diagram and parameters for *φ=225º*. d) Output current, grid and Thévenin voltages, vector diagram and parameters for *φ=350º*.