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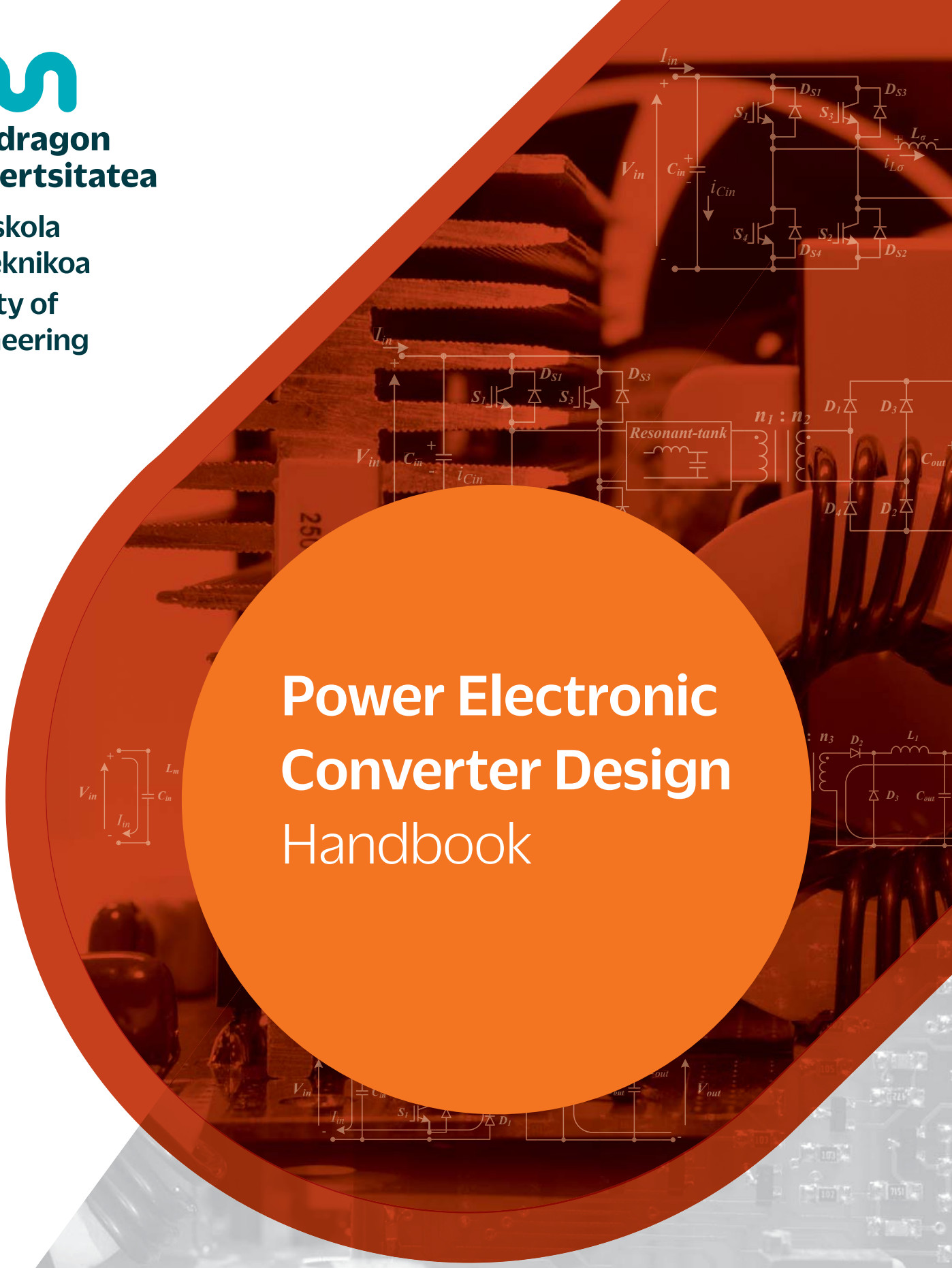

Power Electronic Converter Design

Handbook

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POWER ELECTRONIC CONVERTER DESIGN HANDBOOK

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Abstract

Nowadays, power electronic converters play an essential role in the majority of consumer electronic devices and are widely used in industrial applications. Since most of these applications are supplied through the AC grid, the use of rectifiers and DC-DC conveters are mandatory to adapt the grid voltage to the application requirements.

In this book, most used AC-DC rectifier topologies and DC-DC converter topologies are thoroughly discussed. Basics of each converter, equations for the power losses evaluation and passive elements design are described. Moreover, the medium frequency transformer required by several of the studied DC-DC converters is analysed in depth.

Therefore, this book pretends to be a handbook with a wide scope, which could be used for academic purposes or even by engineers.

Abbreviations

2L-VSC	Two-level voltage source converter
3L-NPC	Three-level neutral point clamped
AC	Alternating-current
AFE	Active front end
CCM	Continuous current mode
CHB	Cascaded H-bridge
DC	Direct-current
DCM	Discontinuous current mode
DFE	Diode front end
EMI	Electromagnetic interference
HB	H-bridge
IGSE	Improved generalized Steinmetz equation
LCC	Line commutated converter
MFT	Medium frequency transformer
NRF	Notch resonance frequency
PRF	Parallel resonance frequency
PWL	Piecewise linear
PWM	Pulse width modulation
SHE	Selective harmonic elimination
SRF	Series resonance frequency
SVM	Space vector modulation
THD	Total harmonic distortion
VSC	Voltage source converter

Contents

Chapter 1

AC-DC Rectifiers

In this chapter, the main characteristics of various active and passive converter topologies for AC to DC rectifying purposes are discussed. For each converter, analytical expressions of semiconductor power losses are described and DC bus capacitor design criteria are shown.

1.1 Introduction

The electrical devices used to convert an alternating-current (AC) to a direct-current (DC) are known as rectifiers. So, the AC to DC conversion process is known as rectification.

Depending on the rectifier type and the input AC voltage, the output DC voltage can be variable or not. Diode rectifiers make the output DC voltage to be input AC voltage dependent, while active rectifiers maintain the output DC voltage constant.

In order to have a wide pool of choices to select the most suitable rectifier for a given application, different converters that could be used as rectifiers must be analyzed. In this chapter, the main characteristics of four different converters are detailed, their operation is described and DC link capacitor design criterion is discussed. In addition, given that the efficiency evaluation is mandatory in energy conversion applications, analytical power loss models for each converter are presented.

1.2 Three-phase diode front end

Fig 2.1 shows a three-phase diode front end (DFE) rectifier composed of a DC bus capacitor (C_{bus}) and three legs with two diodes in each leg. As it is composed of diodes, the power flow is unidirectional (from AC source to DC bus) and the bus voltage cannot be controlled (it depends on the AC supply and the load). This rectifier is widely used in industry due to its low manufacturing cost and high efficiency and reliability [1]. However, they generate current harmonics in the AC side, which are detrimental for electrical generators.

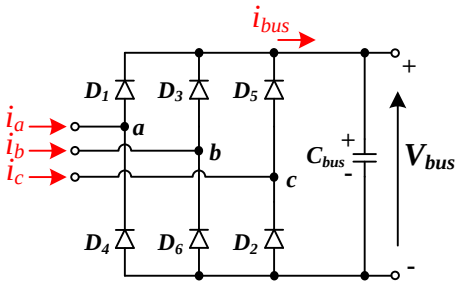


Fig 2.1. Three-phase diode front end rectifier.

Under the assumption of a highly inductive AC side, the rectifier operates in a continuous current mode (CCM) [2], [3] and the DC bus current (i_{bus}) can be considered constant.

As shown in Fig 2.2, each diode conducts when it is forward-biased and two diodes are always current conducting in the bridge. Assuming a highly inductive AC side, the current ripple in the DC side can be neglected (cf. Fig 2.2). Thus, the current conducted by all the diodes is considered equal to the DC side current I_{bus}. This DC side current varies depending on the transferred power, i.e. the higher the power the higher is the circulating current. Being conservative, the maximum DC bus voltage (v_{bus}) is equal to the line to line voltage and hence, the maximum reverse voltage of the diodes is given by the peak line to line voltage (V_{bus}). The conducted current and reverse voltage of all diodes are same and in consequence, it can be assumed that all diodes have same power losses and thermal stress.

1.2.1 Power losses estimation

Assuming an ideal DC bus capacitor with no losses, the converter power losses are equal to the diode power losses, which are given by average conduction power losses (P_{cond}) and average switching power losses (P_{sw}), Eq. (2.1).

$$P_{losses} = P_{cond} + P_{sw} \tag{2.1}$$

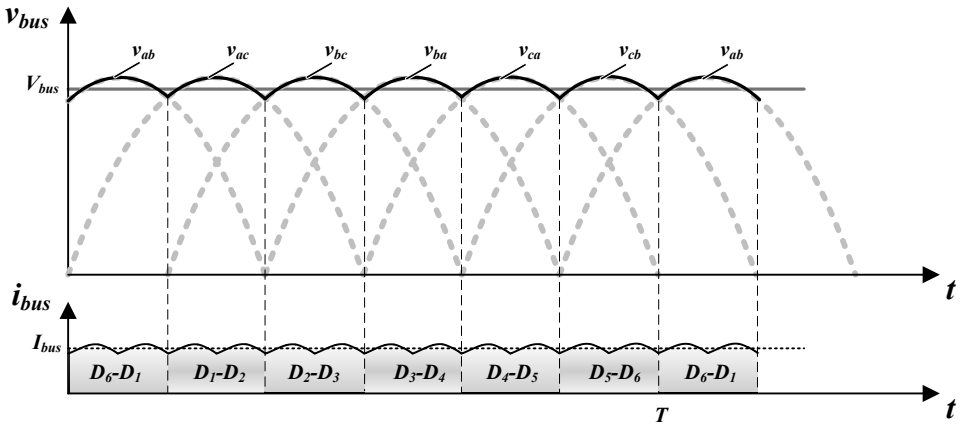


Fig 2.2. Voltage and current waveforms in a three-phase diode rectifier.

Average conduction power losses are estimated from the diode forward characteristics provided by the manufacturer (cf. Fig 2.3a). In order to simplify the final expression, the real voltage-vs-current curve (grey line) is approximated to a first order equation (black line) as shown by Fig 2.3a. Thus, the voltage drop over the diode can be expressed by the threshold voltage (V_{th}) and the characteristic on-state resistance (r_d), see Eq. (2.2). Therefore, the instantaneous power dissipated in the diode is given by Eq. (2.3) and in consequence, if the instantaneous power losses are averaged in a fundamental period (T), average conduction power losses are obtained as in Eq. (2.4).

$$v_F(t) = V_{th} + i_F(t) \cdot r_d \tag{2.2}$$

$$p_{cond}(t) = i_F(t) \cdot v_F(t) = i_F(t) \cdot V_{th} + {i_F}^2(t) \cdot r_d \tag{2.3}$$

$$P_{cond} = \frac{1}{T} \cdot \int_0^{T_{cond}} p_{cond}(t)\, dt = r_d \cdot {I_{rms}}^2 + V_{th} \cdot I_{ave} \tag{2.4}$$

where i_F, I_{rms} and I_{ave} are respectively forward, root-mean-square (*rms*) and average currents through the diode, v_F is the forward voltage drop over the diode, and, T_{cond} is the diode conduction time interval.

From Fig 2.2, the *rms* current and the average current can be derived:

$$I_{rms} = \sqrt{\frac{1}{T} \cdot \int_0^{T/3} {I_{bus}}^2 dt} = \frac{I_{bus}}{\sqrt{3}} \tag{2.5}$$

$$I_{ave} = \frac{1}{T} \cdot \int_0^{T/3} I_{bus}\, dt = \frac{I_{bus}}{3} \tag{2.6}$$

When a diode is suddenly reverse biased (with high *di/dt*), the carriers must be recovered before it starts acting as a blocking device. Average switching power losses (P_{sw}) are due to this phenomenon. In order to estimate these losses (E_{rec}), the manufacturer provides the dissipated energy (cf. Fig 2.3b) at the 100FIT test voltage (V_{100FIT}). This curve can be modelled with a second order equation as Eq. (2.7). The dissipated energy must be

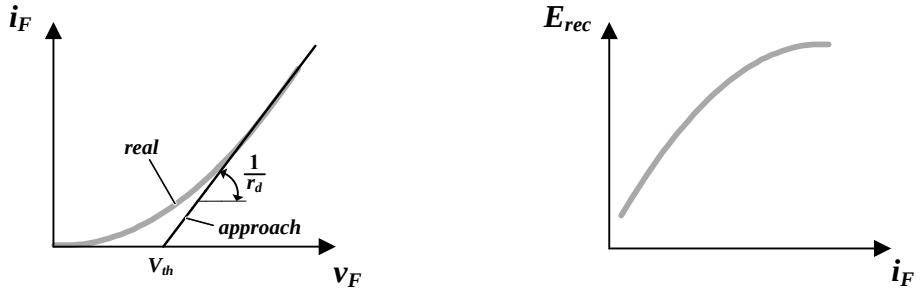
normalized to the switched voltage (v_{sw}), Eq. (2.8). Average switching power losses are equal to the summation of the switching energy losses over a fundamental period (T), Eq. (2.9).

$$E_{rec} = A_{off} \cdot {i_F}^2 + B_{off} \cdot i_F + C_{off} \tag{2.7}$$

$$E_{rec} = \frac{v_{sw}}{V_{100FIT}} \cdot \left(A_{off} \cdot {i_F}^2 + B_{off} \cdot i_F + C_{off} \right) \tag{2.8}$$

$$P_{sw} = \frac{1}{N \cdot T} \cdot \sum_{n=1}^{N} \frac{v_{sw}(n)}{V_{100FIT}} \cdot \left(A_{off} \cdot i_F(n)^2 + B_{off} \cdot i_F(n) + C_{off} \right) \tag{2.9}$$

where A_{off}, B_{off} and C_{off} are the energy loss characteristic coefficients.



a) b)

Fig 2.3. Typical diode characteristics. a) Diode forward characteristic. b) Dissipated energy vs forward current.

However, as a highly inductive AC side has been assumed, the *di/dt* of the current through the diodes is small. Thus, the carriers to be recovered are few and in consequence, average switching power losses can be neglected. Therefore, Eq. (2.10) gives the efficiency of the three-phase diode rectifier.

$$\eta = 1 - \frac{2 \cdot \left(V_{th} \cdot I_{bus} + r_d \cdot {I_{bus}}^2 \right)}{P_{in}} \tag{2.10}$$

1.2.2 DC bus capacitor design

When the AC side voltage is lower than the capacitor voltage, the DC bus capacitor must supply the load power guaranteeing a given voltage ripple. To do so, C_{bus} must store a certain amount of energy.

The maximum DC bus voltage is provided by the line to line voltage ($V_{LL,rms}$):

$$V_{bus,\max} = \sqrt{2} \cdot V_{LL,rms} \tag{2.11}$$

The energies stored by the capacitor when it is charged with the maximum bus voltage and with the minimum bus voltage are given respectively by:

$$E_{C\max} = \frac{1}{2} \cdot C_{bus} \cdot \left(V_{bus} + \frac{\Delta v}{2} \right)^2 \tag{2.12}$$

$$E_{C\min} = \frac{1}{2} \cdot C_{bus} \cdot \left(V_{bus} - \frac{\Delta v}{2} \right)^2 \tag{2.13}$$

where Δv is the voltage ripple.

Considering a ΔT time interval in which the C_{bus} capacitor is being discharged, the power provided by the capacitor can be expressed as:

$$P = \frac{E_{C\max} - E_{C\min}}{\Delta T} \tag{2.14}$$

If the transient power variation (P) is limited to the 10% of the rated power, the required DC bus capacitance is calculated introducing Eq. (2.12) and Eq. (2.13) into Eq. (2.14).

$$C_{bus} = \frac{2 \cdot P \cdot \Delta T}{\left(V_{bus} + \frac{\Delta v}{2} \right)^2 - \left(V_{bus} - \frac{\Delta v}{2} \right)^2} = \frac{3 \cdot V_{\max} \cdot I_{\max} \cdot \Delta T}{20 \cdot V_{bus} \cdot \Delta v} \tag{2.15}$$

where V_{max} and I_{max} are the peak phase voltage and current.

1.3 Two-level voltage source converter

The two-level voltage source converter (2L-VSC) is composed of a DC bus capacitor (C_{bus}) and three legs with two transistors and their respective freewheel diodes in each leg (cf. Fig 2.4). All the semiconductors have to withstand the DC bus voltage during the off-state. The low component number makes this converter simple, cost effective and reliable [4]. In consequence, it is one of the most popular converters in conventional wind turbines [1], [4]. Space vector modulation (SVM) and pulse width modulation (PWM) are two of the most used modulation techniques in this converter [5]. In this book, the analytical expressions for power losses estimation are obtained under the assumption that a PWM technique is used. The accuracy of obtained analytical expressions is pretty acceptable [6-7].

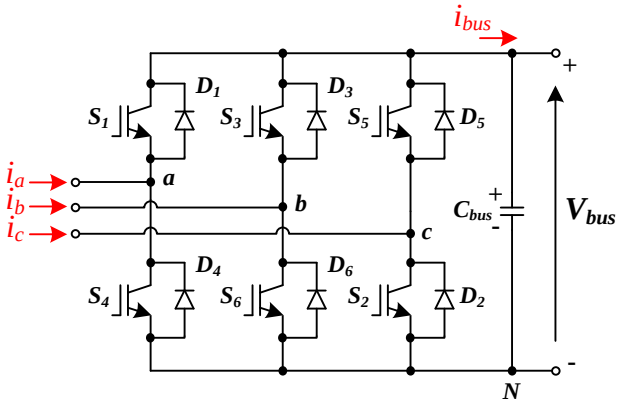


Fig 2.4. Two-level voltage source converter.

In Fig 2.5, typical voltage waveforms of a 2L-VSC operated with PWM are shown. v_{cr} is the triangular carrier and v_a*, v_b* and v_c* are the reference phase voltages to be synthesized. The reference voltages are 120 degrees phase shifted each other. When the reference voltage is higher than the triangular carrier, the upper transistor of that leg is turned-on while the lower transistor is turned-off. Conversely, when the reference voltage is lower than the triangular carrier, the upper transistor of that leg is turned-off and the lower transistor is turned-on. Thus, two different voltage levels can be synthesized in each phase [0, V_{bus}]. Line to line voltage is obtained by subtracting two-phase voltages as shown in Fig 2.5. This resulting line to line voltage has three voltage levels.

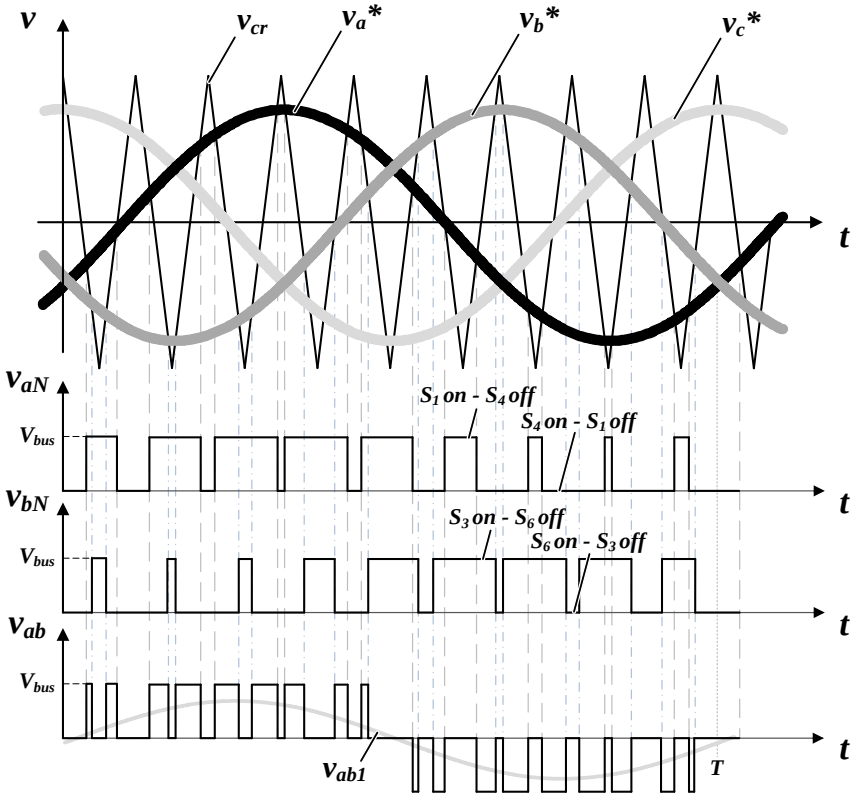


Fig 2.5. Typical voltage waveforms of a two-level voltage source converter with a PWM modulation strategy.

1.3.1 Power losses estimation

Generally speaking, main converter power losses come from conduction and switching power losses of the semiconductors. In order to obtain simple analytical expressions for power losses, the following is assumed:

- The phase current is a purely sinusoidal current.
- The converter operates under a PWM modulation strategy in the linear region (overmodulation is not considered).
- The switching frequency is very high.

- The output characteristics and the switching energy losses characteristics provided by the manufacturer are used to estimate conduction and switching power losses.

1.3.1.1 Conduction power losses

Conduction power losses depend on the semiconductor output characteristic and the average and *rms* values of the current flowing through it, see Eq. (2.4). Due to the symmetrical structure of the converter, the circulating current expressions are equal for all the transistors as well as for all the diodes. As it can be observed in Fig 2.6, a pulsating current circulates through the transistor S_1. Furthermore, considering a very high switching frequency, this current can be considered constant (I_a).

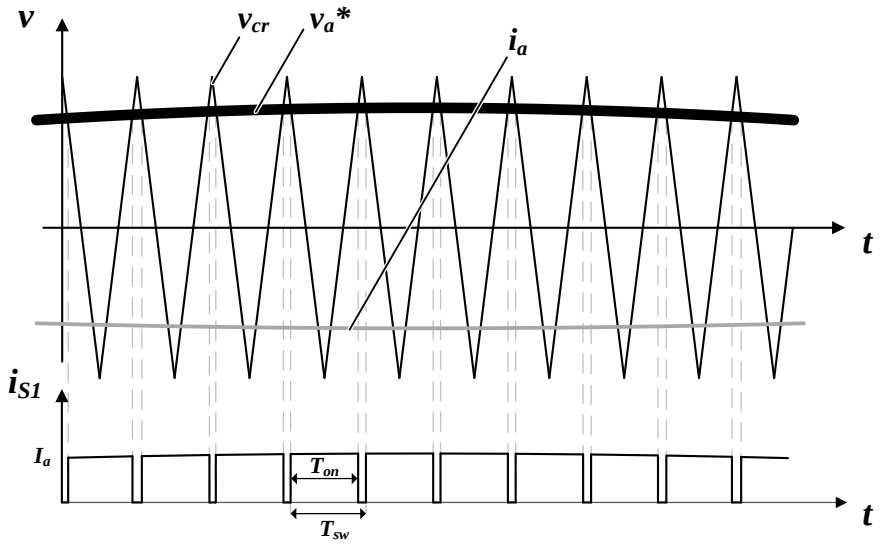


Fig 2.6. Current circulating through the transistor S_1 assuming a very high switching frequency.

Therefore, the average and *rms* current expressions in a switching period T_{sw} are given by:

$$I_{ave} = I_a \cdot \frac{T_{on}}{T_{sw}} \tag{2.16}$$

$$I_{rms}^{\ 2} = I_a^{\ 2} \cdot \frac{T_{on}}{T_{sw}} \tag{2.17}$$

where T_{on} is the conduction time interval.

The current circulating through the semiconductor during the conduction time interval is the same as the phase current. As the amplitude of this sinusoidal current varies along the fundamental period, the conduction power losses in a fundamental period can be estimated by the summation of conduction power losses in each switching period:

$$P_{cond} = \frac{1}{N} \cdot \sum_{n=1}^{N} r_d \cdot I_{rms}(n)^2 + V_{th} \cdot I_{ave}(n) = \\ = \frac{1}{N} \cdot \sum_{n=1}^{N} r_d \cdot I_a(n)^2 \cdot \frac{T_{on}}{T_{sw}}(n) + V_{th} \cdot I_a(n) \cdot \frac{T_{on}}{T_{sw}}(n) \tag{2.18}$$

$$N = \frac{T}{T_{sw}} \tag{2.19}$$

where V_{th} is the threshold voltage in the semiconductor and r_d is the characteristic on-state resistance.

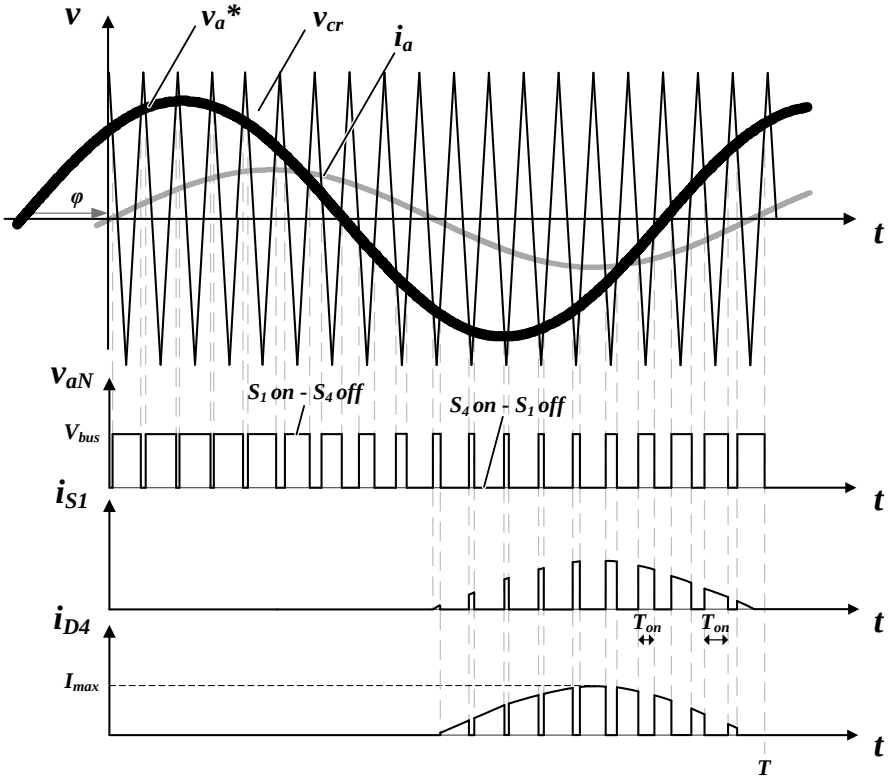


Fig 2.7. Current and voltage waveforms of a two-level voltage source converter with a PWM modulation strategy.

In Eq. (2.18) the output characteristics of the semiconductors (r_d, V_{th}) are constant. So, in order to obtain an analytical conduction losses expression, the pulsating current waveform is converted into a continuous current with similar average and *rms* current values.

At each T_{on} conduction interval, the I_a current value of Eq. (2.16) and Eq. (2.17) has the same amplitude as the phase current i_a:

$$I_a(n) = i_a(t) = I_{\max} \cdot \sin(\omega t) \tag{2.20}$$

where I_{max} is the maximum amplitude of the phase current.

If conduction time intervals are observed in Fig 2.7, it can be seen how T_{on} varies proportionally to the reference voltage v_a* of Eq. (2.21). Thus, the lower v_a* the narrower

the T_{on} period. Therefore, T_{on}/T_{sw} can be expressed in function of the reference voltage. As T_{on}/T_{sw} must be positive and its value contained within 0 and 1, the modulation function can be defined by Eq. (2.22).

$$v_a^*(t) = m \cdot \sin(\omega t + \varphi) \tag{2.21}$$

$$\frac{T_{on}}{T_{sw}}(t) = \frac{1}{2} \cdot (1 - m \cdot \sin(\omega t + \varphi)) \tag{2.22}$$

where m is the modulation index and φ is the phase shift between v_a^* and the phase current i_a.

Taking into account that the transistor S_1 conducts only when the phase current is negative (cf. Fig 2.4 and Fig 2.7), the average and *rms* currents through it in a fundamental period can be approached to:

$$I_{ave} = \frac{1}{T} \cdot \int_{T/2}^{T} I_{\max} \cdot \sin(\omega t) \cdot \frac{1}{2} \cdot (1 - m \cdot \sin(\omega t + \varphi)) dt \tag{2.23}$$

$$I_{rms}{}^2 = \frac{1}{T} \cdot \int_{T/2}^{T} I_{\max}{}^2 \cdot \sin^2(\omega t) \cdot \frac{1}{2} \cdot (1 - m \cdot \sin(\omega t + \varphi)) dt \tag{2.24}$$

As a consequence, average conduction power losses are obtained substituting Eq. (2.23) and Eq. (2.24) in Eq. (2.18):

$$\begin{aligned} P_{cond\_S1} &= \frac{1}{T} \cdot \int_{T/2}^{T} (r_d \cdot I_{\max} \cdot \sin(\omega t) + \cdot V_{th}) \cdot I_{\max} \cdot \sin(\omega t) \cdot \frac{1}{2} \cdot (1 - m \cdot \sin(\omega t + \varphi)) dt = \\ &= \frac{1}{2} \cdot (V_{th} \cdot \frac{I_{\max}}{\pi} + r_d \cdot \frac{I_{\max}{}^2}{4}) - m \cdot \cos(\varphi) \cdot (V_{th} \cdot \frac{I_{\max}}{8} + r_d \cdot \frac{I_{\max}{}^2}{3 \cdot \pi}) \end{aligned} \tag{2.25}$$

Average conduction power losses of the diode D_4 are calculated similarly. The only difference is that it conducts when S_1 is turned-off. Thus, its modulation function is given by:

$$\frac{T_{off}(t)}{T_{sw}} = 1 - \frac{T_{on}(t)}{T_{sw}} = \frac{1}{2} \cdot (1 + m \cdot \sin(\omega t + \varphi)) \tag{2.26}$$

Therefore, its conduction power losses are given as:

$$P_{cond\_D4} = \frac{1}{2} \cdot (V_{th} \cdot \frac{I_{\max}}{\pi} + r_d \cdot \frac{I_{\max}{}^2}{4}) + m \cdot \cos(\varphi) \cdot (V_{th} \cdot \frac{I_{\max}}{8} + r_d \cdot \frac{I_{\max}{}^2}{3 \cdot \pi}) \tag{2.27}$$

As it can be noticed in Eq. (2.25) and Eq. (2.27), the operation with a low phase-shift ($\varphi \approx 0$) leads to larger power losses in the diodes than in the transistors. Conversely, if the converter operates with a high phase-shift of $\varphi \approx \pi$, the losses in the transistors are larger than in the diodes.

1.3.1.2 Switching power losses

Average switching losses in a fundamental period can be calculated by the summation of all turn-on and turn-off losses:

$$P_{sw} = \frac{1}{N \cdot T} \cdot \sum_{n=1}^{N} \left[\begin{array}{l} \frac{v_{on}(n)}{V_{100FIT}} \cdot \left(A_{on} \cdot i_{on}(n)^2 + B_{on} \cdot i_{on}(n) + C_{on} \right) + \\ + \frac{v_{off}(n)}{V_{100FIT}} \cdot \left(A_{off} \cdot i_{off}(n)^2 + B_{off} \cdot i_{off}(n) + C_{off} \right) \end{array} \right] \tag{2.28}$$

where v_{on} and v_{off} are respectively the voltages commutated during turn-on and turn-off, i_{on} and i_{off} are respectively the currents commutated during turn-on and turn-off, V_{100FIT} is the 100FIT test voltage and A_{on}, B_{on}, C_{on} and A_{off}, B_{off}, C_{off} are respectively the turn-on and the turn-off energy loss characteristic coefficients.

As a high switching frequency has been assumed, the currents and voltages commutated in the turn-on and the turn-off of the semiconductors are assumed to be the same (cf. Fig 2.6). Thus, Eq. (2.28) can be simplified to:

$$P_{sw} = \frac{1}{N \cdot T} \cdot \sum_{n=1}^{N} \frac{v_{sw}(n)}{V_{100FIT}} \cdot \left(A \cdot i_{sw}(n)^2 + B \cdot i_{sw}(n) + C \right) \tag{2.29}$$

$$i_{sw} = i_{on} = i_{off} \tag{2.30}$$

$$v_{sw} = v_{on} = v_{off} \tag{2.31}$$

$$A = A_{on} + A_{off} \tag{2.32}$$

$$B = B_{on} + B_{off} \tag{2.33}$$

$$C = C_{on} + C_{off} \tag{2.34}$$

Given that the commutated voltage is assumed to be the mean DC bus voltage (V_{bus}) and the switched current is the phase current, the previous expression can be approached as:

$$\begin{aligned} P_{sw\_S1} &= \frac{V_{bus}}{V_{100FIT} \cdot T \cdot T_{sw}} \cdot \int_{T/2}^{T} \left(I_{\max} \cdot \sin(\omega t) \cdot \left(A \cdot I_{\max} \cdot \sin(\omega t) + \cdot B \right) + C \right) dt = \\ &= \frac{V_{bus}}{V_{100FIT} \cdot T_{sw}} \cdot \left(\frac{A \cdot {I_{\max}}^2}{4} + \frac{B \cdot I_{\max}}{\pi} + \frac{C}{2} \right) \end{aligned} \tag{2.35}$$

The switching losses of the D_4 freewheel diode are also calculated with Eq. (2.35). However, the turn-on energy loss coefficients (A_{on}, B_{on} and C_{on}) of Eq. (2.32), Eq. (2.33) and Eq. (2.34) are equal to zero due to the negligible turn-on losses of diodes.

1.3.1.3 Total power losses

Because of the symmetrical structure of the 2L-VSC, all transistors as well as all diodes have the same power losses. Therefore, once the losses of S_1 and D_4 are calculated, the estimation of the total converter power losses is straightforward:

$$P_{cond} = 6 \cdot \left(P_{cond\_S1} + P_{cond\_D4}\right) \tag{2.36}$$

$$P_{sw} = 6 \cdot \left(P_{sw\_S1} + P_{sw\_D4}\right) \tag{2.37}$$

$$P_{losses} = P_{cond} + P_{sw} \tag{2.38}$$

1.3.2 DC bus capacitor design

For the DC bus capacitance calculation, the next assumptions are made:

- The converter has an AC side filter with negligible energy storage.
- The DC bus voltage is constant and smooth.
- The switching frequency is very high.
- The power factor of the converter is unitary.

Under these considerations, the DC side current (i_{bus} in Fig 2.4) can be expressed as:

$$i_{bus} = \frac{3 \cdot V_{\max} \cdot I_{\max}}{2 \cdot V_{bus}} \tag{2.39}$$

where V_{max} and I_{max} are the peak phase voltage and current respectively.

Eq. (2.39) shows the DC side current i_{bus} is constant [8]. In reality, this current is chopped and hence, it has high frequency components. Nonetheless, the effect of these high frequency components over the DC bus voltage ripple are negligible and in consequence, the required C_{bus} value is small. Therefore, the energy stored by it is small too.

As discussed for the three-phase DFE rectifier, when the AC side voltage is lower than the DC bus voltage, the DC bus capacitor must provide the load power guaranteeing a minimum DC bus voltage. To do so, C_{bus} must store a certain amount of energy. If the transient power variation (P) is limited to the 10% of the rated power the bus capacitance is expressed as:

$$C_{bus} = \frac{2 \cdot P \cdot \Delta T}{\left(V_{bus} + \frac{\Delta v}{2}\right)^2 - \left(V_{bus} - \frac{\Delta v}{2}\right)^2} = \frac{3 \cdot V_{\max} \cdot I_{\max} \cdot \Delta T}{20 \cdot V_{bus} \cdot \Delta v} \tag{2.40}$$

where Δv is the desired voltage ripple and ΔT is the time interval in which the capacitor C_{bus} is being discharged.

1.4 Three-level neutral point clamped converter

Multilevel converters apply more than two levels at their output phase terminals thereby reducing the *dv/dt* and the total harmonic distortion (THD) in comparison to the 2L-VSC [5]. Furthermore, the use of multilevel converters reduces the series connection requirements of power semiconductors and therefore, auxiliary circuits for voltage

balancing are avoided, or at least, minimized. Amog the different multilevel converters, the three-level neutral point clamped converter (3L-NPC) [9] illustrated in Fig 2.8 is a widely used topology in medium-voltage applications, e.g. in wind power, where it is one of the most popular multilevel converter for medium-voltage variable speed wind turbines [10].

The DC bus of the 3L-NPC is composed of two series connected capacitors (C_{bus1} and C_{bus2}) and each converter leg has four controlled switches with their antiparallel diodes. The neutral point N of the DC bus is connected to the phase terminal through the clamp diodes. Thus, three different voltage levels are applied at phase terminals ($V_{bus}/2$, 0 and $-V_{bus}/2$).

The differences between the extracted and the injected charges from/to the neutral point terminal lead to voltage unbalances in the DC bus capacitors. Thus, modulation or control level considerations must be taken into account to achieve a proper voltage balance [5]. In addition, the power loss distribution among the power switches is not symmetrical. Therefore, the thermal stress in some semiconductors is higher than in others. In consequence, the junction temperature of the most stressed power devices limits the output power of the converter (might lead to derated power capacity in practical cases).

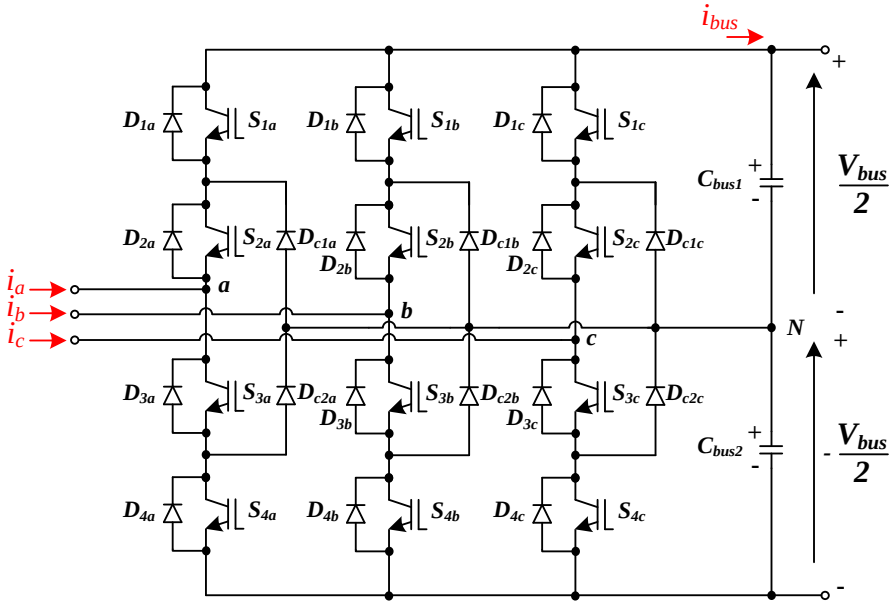


Fig 2.8. Three-level neutral point clamped converter.

Fig 2.9 shows the allowed switching states of one leg of the converter that, independently of the phase current polarity, define the output voltage. When transistors S_1 and S_2 are turned-on, the converter applies a voltage of $V_{bus}/2$ at phase terminals (cf. Fig 2.9a). When the transistors are S_2 and S_3 transistors are turned-on, see Fig 2.9b, the current circulates through the clamp diodes and zero voltage is applied at phase terminals. Finally, when S_3 and S_4 are turned-on, a $-V_{bus}/2$ voltage is applied at phase terminals as shown by Fig 2.9c. At each switching state, the phase current sense determines the switches that are

conducting that current, transistors or freewheel diodes. Additionally, all the semiconductors have to withstand a voltage of $V_{bus}/2$. Compared with the 2L-VSC, if same voltage rated switching devices are used, the DC bus voltage can be doubled and therefore, higher power is transferred.

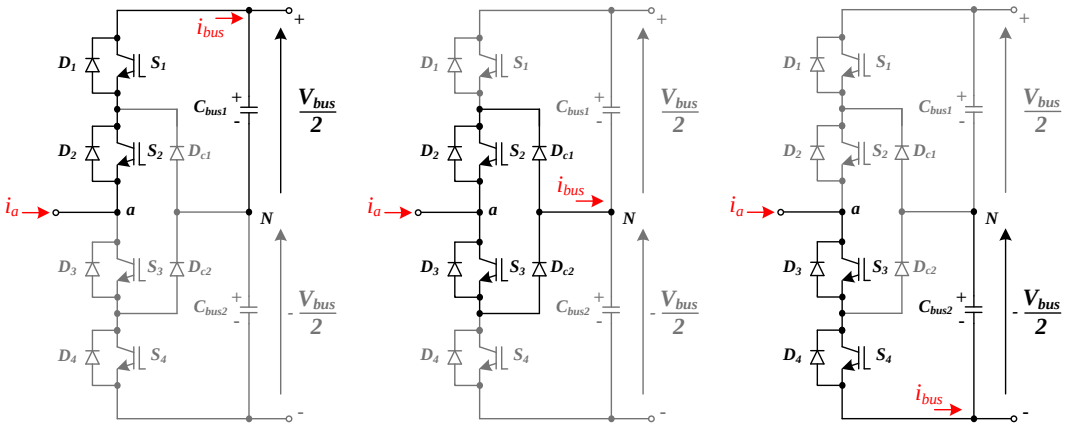


Fig 2.9. Switching states of the single-phase NPC. a) Positive voltage applied at the output. b) Zero voltage applied at the output. c) Negative voltage applied at the output.

In Table 2.1, afore described switching states are summarized. It can be noticed that S_1-S_3 and S_2-S_4 switches are complementary. This way, phase short circuits are avoided. Furthermore, an additional switching state where S_1-S_4 are turned-on and S_2-S_3 are turned-off is shown. This operational state is known as the forbidden state since the output voltage applied at this state is uncontrollable (depends on the current sense). Additionally, the voltage blocked by S_2-D_2 or S_3-D_3 is V_{bus}, which is two times the voltage stress they withstand with allowed switching states. All in all, this switching state must be avoided.

TABLE 2.1

SWITCHING STATES OF THE SINGLE-PHASE NPC

Voltage applied at phase terminal	S_1	S_2	S_3	S_4
$V_{bus}/2$	1	1	0	0
0	0	1	1	0
$-V_{bus}/2$	0	0	1	1
$V_{bus}/2$ or $-V_{bus}/2$	1	0	0	1

The 3L-NPC can be modulated with level-shifted PWM, SVM or selective harmonic elimination (SHE) techniques [9, 11]. Fig 2.10 shows the typical waveforms of a single-phase NPC operating with a level-shifted PWM modulation technique. As it can be noticed, this modulation technique requires two level-shifted carriers (one per each pair of complementary semiconductors). When the reference phase voltage v_a* is higher than the carrier v_{cr1}, S_1 is turned-on and S_3 is turned-off. Conversely, when the reference voltage

v_a* is lower than the carrier v_{cr1}, S_1 is turned-off and S_3 is turned-on. Similarly, transistors S_2 and S_4 are commanded the carrier v_{cr2}.

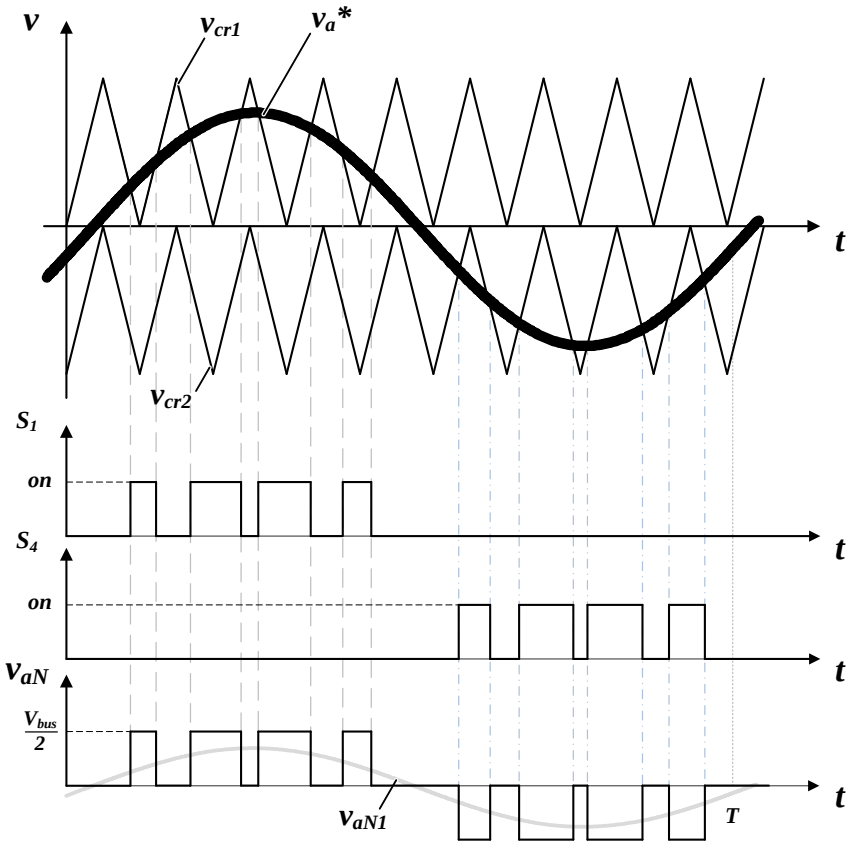


Fig 2.10. Typical voltage waveforms of a single-phase NPC with a level-shifted PWM modulation strategy.

As it has been mentioned, the phase voltage has three voltage levels (cf. Fig 2.10). The line to line voltage is obtained subtracting the phase voltages. This way, five voltage levels are achieved.

1.4.1 Power losses estimation

Assuming an ideal DC bus capacitor with no losses, the converter power losses are given by the conduction and switching power losses of the semiconductors. These power losses can be modeled with analytical expressions, obtained assuming the converter operates with a high frequency PWM modulation [12] (similarly to that discussed in section 2.3.1). Furthermore, assuming an ideal AC supply grid without unbalances, the current circulating through each leg has the same amplitude and frequency. Therefore, the power losses in each leg are the same.

In Fig 2.11, the currents circulating through the first leg of the 3L-NPC are shown. The outer transistors S_1 and S_4 conduct the same current value with a 180 degree phase displacement. Thus, average power losses in both transistors are equal. As it can be noticed, this is applicable to inner transistors S_2-S_3, freewheel diodes D_1-D_2-D_3-D_4 and

clamp diodes D_{c1}-D_{c2}. Thus, power losses expressions are calculated just for one semiconductor in each group.

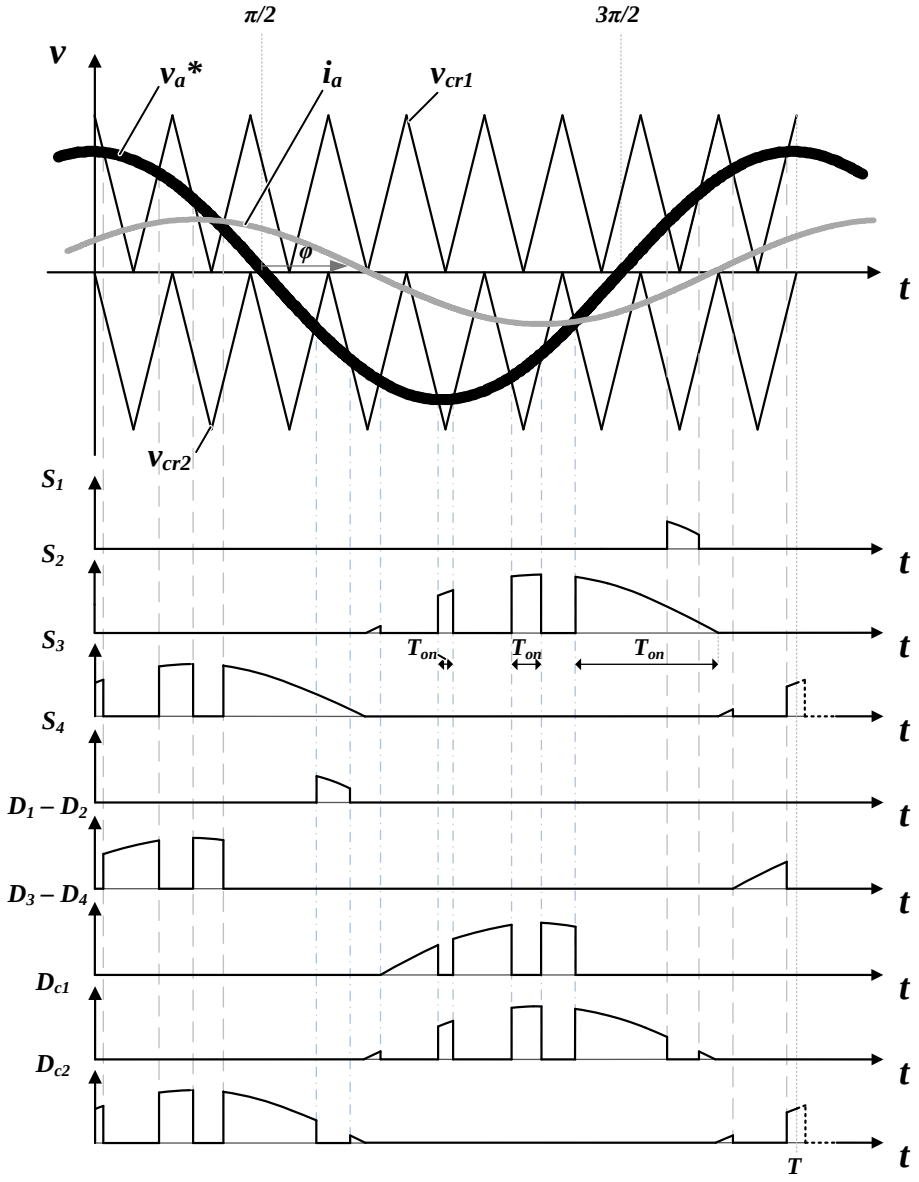


Fig 2.11. Typical current waveforms of a single-phase NPC with a level-shifted PWM modulation strategy.

1.4.1.1 Conduction power losses

Conduction power losses in a fundamental period (T) can be estimated by the summation of conduction power losses in each switching period (T_{sw}). So, in order to obtain an analytical conduction losses expression, the pulsating current waveform is converted into a continuous current with similar average and *rms* current values:

$$P_{cond} = \frac{1}{N} \cdot \sum_{n=1}^{N} r_d \cdot I_{rms}(n)^2 + V_{th} \cdot I_{ave}(n) = \\ = \frac{1}{N} \cdot \sum_{n=1}^{N} r_d \cdot i_a(n)^2 \cdot \frac{T_{on}}{T_{sw}}(n) + V_{th} \cdot i_a(n) \cdot \frac{T_{on}}{T_{sw}}(n) \tag{2.41}$$

$$N = \frac{T}{T_{sw}} \tag{2.42}$$

where V_{th} is the threshold voltage in the semiconductor, r_d is the characteristic on-state resistance and T_{on} is the conduction time interval of the semiconductor.

When the semiconductors are on, the current through the semiconductors is equal to the phase current:

$$i_a(t) = I_{\max} \cdot \cos(\omega t - \varphi) \tag{2.43}$$

where I_{max} is the maximum amplitude of the phase current and φ is the phase-shift between the reference voltage v_a* and the phase current i_a.

As depicted in Fig 2.11, this current flows through semiconductors when the latter have a turn-on command and the current circulates in the natural conduction sense of the semiconductors. This last depends on the the phase-shift φ. Thus, each semiconductor is current conducting during a given interval of the phase output voltage. These conduction intervals are summarized in Table 2.2.

The total conduction time of the semiconductors within a fundamental period (T) is given by the summation of the different T_{on} conduction times of the semiconductors. This summation is modelled with a modulation function. Within a switching period, the T_{on} conduction time of each semiconductor is proportional to the reference voltage v_a*. Thus, the modulation function of each semiconductor is derived from of Eq. (2.44) and Fig 2.11. For transistor S_1, the T_{on} conduction time is directly proportional to the reference voltage (the lower v_a*, the narrower T_{on}). Therefore, the modulation function of this transistor is equal to Eq. (2.44). Conversely, in the first conduction period comprehended from ($\pi/2+\varphi$) to $3\pi/2$, the T_{on} conduction interval of the transistor S_2 is inversely proportional to the reference voltage. After $3\pi/2$, S_2 is always conducting. Therefore, the modulation function of this second conduction period is equal to one (the modulation function must be within 0 and 1). The modulation functions of the rest of the semiconductors are derived in a similar way and summarized in Table 2.2.

$$v_a^*(t) = m \cdot \cos(\omega t) \tag{2.44}$$

where m is the modulation index.

TABLE 2.2

CONDUCTION TIMES AND MODULATION FUNCTIONS OF SINGLE-PHASE NPC'S SEMICONDUCTORS

S_1	**Conducting**	From $\frac{3\cdot\pi}{2}$ to $\frac{3\cdot\pi}{2}+\varphi$	
	Modulation function	$\frac{T_{on}}{T_{sw}}(t)=m\cdot\cos(\omega t)$	
D_1	**Conducting**	From $\frac{3\cdot\pi}{2}+\varphi$ to $\frac{5\cdot\pi}{2}$	
	Modulation function	$\frac{T_{on}}{T_{sw}}(t)=m\cdot\cos(\omega t)$	
S_2	**Conducting**	From $\frac{\pi}{2}+\varphi$ to $\frac{3\cdot\pi}{2}$	From $\frac{3\cdot\pi}{2}$ to $\frac{3\cdot\pi}{2}+\varphi$
	Modulation function	$\frac{T_{on}}{T_{sw}}(t)=1+m\cdot\cos(\omega t)$	$\frac{T_{on}}{T_{sw}}(t)=1$
D_{c1}	**Conducting**	From $\frac{\pi}{2}+\varphi$ to $\frac{3\cdot\pi}{2}$	From $\frac{3\cdot\pi}{2}$ to $\frac{3\cdot\pi}{2}+\varphi$
	Modulation function	$\frac{T_{on}}{T_{sw}}(t)=1+m\cdot\cos(\omega t)$	$\frac{T_{on}}{T_{sw}}(t)=1-m\cdot\cos(\omega t)$

From Eq. (2.43) and Table 2.2 the average and *rms* current expressions are obtained and thereby, conduction power losses given by Eq. (2.41) can be calculated:

- Outer transistor S_1:

$$I_{ave}=\frac{1}{2\cdot\pi}\cdot\int_{\frac{3\cdot\pi}{2}}^{\frac{3\cdot\pi}{2}+\varphi}\left(-I_{\max}\cdot\cos(\omega t-\varphi)\right)\cdot m\cdot\cos(\omega t)d\omega t=\frac{m\cdot I_{\max}}{4\cdot\pi}\cdot\left(\sin(\varphi)-\varphi\cdot\cos(\varphi)\right) \tag{2.45}$$

$$I_{rms}{}^2=\frac{1}{2\cdot\pi}\cdot\int_{\frac{3\cdot\pi}{2}}^{\frac{3\cdot\pi}{2}+\varphi}I_{\max}{}^2\cdot\cos^2(\omega t-\varphi)\cdot m\cdot\cos(\omega t)d\omega t=\frac{m\cdot I_{\max}{}^2}{6\cdot\pi}\cdot\left(1-2\cdot\cos(\varphi)+\cos^2(\varphi)\right) \tag{2.46}$$

$$P_{cond\_S1}=V_{th}\cdot\frac{m\cdot I_{\max}}{4\cdot\pi}\cdot\left(\sin(\varphi)-\varphi\cdot\cos(\varphi)\right)+r_d\cdot\frac{m\cdot I_{\max}{}^2}{6\cdot\pi}\cdot\left(1-2\cdot\cos(\varphi)+\cos^2(\varphi)\right) \tag{2.47}$$

where r_d and V_{th} are the output characteristics of the semiconductor.

- Freewheel diode D_1:

$$I_{ave}=\frac{1}{2\cdot\pi}\cdot\int_{\frac{3\cdot\pi}{2}+\varphi}^{\frac{5\cdot\pi}{2}}I_{\max}\cdot\cos(\omega t-\varphi)\cdot m\cdot\cos(\omega t)d\omega t= \tag{2.48}$$

$$=\frac{m\cdot I_{\max}}{4\cdot\pi}\cdot\left(\pi\cdot\cos(\varphi)+\sin(\varphi)-\varphi\cdot\cos(\varphi)\right)$$

$$I_{rms}{}^2 = \frac{1}{2\cdot\pi}\cdot\int_{\frac{3\cdot\pi}{2}+\varphi}^{\frac{5\cdot\pi}{2}} I_{\max}{}^2\cdot\cos^2(\omega t-\varphi)\cdot m\cdot\cos(\omega t)d\omega t = \frac{m\cdot I_{\max}{}^2}{6\cdot\pi}\cdot\left(1+2\cdot\cos(\varphi)+\cos^2(\varphi)\right) \tag{2.49}$$

$$P_{cond\_D1} = V_{th}\cdot\frac{m\cdot I_{\max}}{4\cdot\pi}\cdot\left(\pi\cdot\cos(\varphi)+\sin(\varphi)-\varphi\cdot\cos(\varphi)\right)+ + r_d\cdot\frac{m\cdot I_{\max}{}^2}{6\cdot\pi}\cdot\left(1+2\cdot\cos(\varphi)+\cos^2(\varphi)\right) \tag{2.50}$$

- First conduction period (from $\pi/2+\varphi$ to $3\pi/2$) of inner transistor S_2 and clamp diode D_{c1}:

$$I_{ave} = \frac{1}{2\cdot\pi}\cdot\int_{\frac{\pi}{2}+\varphi}^{\frac{3\cdot\pi}{2}}\left(-I_{\max}\cdot\cos(\omega t-\varphi)\right)\cdot\left(1+m\cdot\cos(\omega t)\right)d\omega t = = \frac{m\cdot I_{\max}}{4\cdot\pi}\cdot\left(\frac{2+2\cdot\cos(\varphi)}{m}+\varphi\cdot\cos(\varphi)-\sin(\varphi)-\pi\cdot\cos(\varphi)\right) \tag{2.51}$$

$$I_{rms}{}^2 = \frac{1}{2\cdot\pi}\cdot\int_{\frac{\pi}{2}+\varphi}^{\frac{3\cdot\pi}{2}} I_{\max}{}^2\cdot\cos^2(\omega t-\varphi)\cdot\left(1+m\cdot\cos(\omega t)\right)d\omega t = = \frac{m\cdot I_{\max}{}^2}{6\cdot\pi}\cdot\left(\frac{3\cdot(\pi-\varphi)+3\cdot\sin(\varphi)\cdot\cos(\varphi)}{2\cdot m}-1-2\cdot\cos(\varphi)-\cos^2(\varphi)\right) \tag{2.52}$$

$$P_{cond\_S2/1} = P_{cond\_Dc1/1} = V_{th}\cdot\frac{m\cdot I_{\max}}{4\cdot\pi}\cdot\left(\frac{2+2\cdot\cos(\varphi)}{m}+\varphi\cdot\cos(\varphi)-\sin(\varphi)-\pi\cdot\cos(\varphi)\right)+ + r_d\cdot\frac{m\cdot I_{\max}{}^2}{6\cdot\pi}\cdot\left(\frac{3\cdot(\pi-\varphi)+3\cdot\sin(\varphi)\cdot\cos(\varphi)}{2\cdot m}-1-2\cdot\cos(\varphi)-\cos^2(\varphi)\right) \tag{2.53}$$

- Second conduction period (from $3\pi/2$ to $3\pi/2+\varphi$) of inner transistor S_2:

$$I_{ave} = \frac{1}{2\cdot\pi}\cdot\int_{\frac{3\cdot\pi}{2}}^{\frac{3\cdot\pi}{2}+\varphi}\left(-I_{\max}\cdot\cos(\omega t-\varphi)\right)d\omega t = \frac{I_{\max}}{2\cdot\pi}\cdot\left(1-\cos(\varphi)\right) \tag{2.54}$$

$$I_{rms}{}^2 = \frac{1}{2\cdot\pi}\cdot\int_{\frac{3\cdot\pi}{2}}^{\frac{3\cdot\pi}{2}+\varphi} I_{\max}{}^2\cdot\cos^2(\omega t-\varphi)d\omega t = \frac{I_{\max}{}^2}{4\cdot\pi}\cdot\left(\varphi-\cos(\varphi)\cdot\sin(\varphi)\right) \tag{2.55}$$

$$P_{cond\_S2/2} = V_{th}\cdot\frac{I_{\max}}{2\cdot\pi}\cdot\left(1-\cos(\varphi)\right)+r_d\cdot\frac{I_{\max}{}^2}{4\cdot\pi}\cdot\left(\varphi-\cos(\varphi)\cdot\sin(\varphi)\right) \tag{2.56}$$

- Second conduction period (from $3\pi/2$ to $3\pi/2+\varphi$) of clamp diode D_{c1}:

$$I_{ave} = \frac{1}{2\cdot\pi}\cdot\int_{\frac{3\cdot\pi}{2}}^{\frac{3\cdot\pi}{2}+\varphi}\left(-I_{\max}\cdot\cos(\omega t-\varphi)\right)\cdot\left(1-m\cdot\cos(\omega t)\right)d\omega t = \\ = \frac{m\cdot I_{\max}}{4\cdot\pi}\cdot\left(\frac{2-2\cdot\cos(\varphi)}{m}+\varphi\cdot\cos(\varphi)-\sin(\varphi)\right) \tag{2.57}$$

$$I_{rms}{}^2 = \frac{1}{2\cdot\pi}\cdot\int_{\frac{3\cdot\pi}{2}}^{\frac{3\cdot\pi}{2}+\varphi} I_{\max}{}^2\cdot\cos^2(\omega t-\varphi)\cdot\left(1-m\cdot\cos(\omega t)\right)d\omega t = \\ = \frac{m\cdot I_{\max}{}^2}{6\cdot\pi}\cdot\left(\frac{3\cdot\varphi-3\cdot\sin(\varphi)\cdot\cos(\varphi)}{2\cdot m}-1+2\cdot\cos(\varphi)-\cos^2(\varphi)\right) \tag{2.58}$$

$$P_{cond\_Dc1/2} = V_{th}\cdot\frac{m\cdot I_{\max}}{4\cdot\pi}\cdot\left(\frac{2-2\cdot\cos(\varphi)}{m}+\varphi\cdot\cos(\varphi)-\sin(\varphi)\right)+ \\ + r_d\cdot\frac{m\cdot I_{\max}{}^2}{6\cdot\pi}\cdot\left(\frac{3\cdot\varphi-3\cdot\sin(\varphi)\cdot\cos(\varphi)}{2\cdot m}-1+2\cdot\cos(\varphi)-\cos^2(\varphi)\right) \tag{2.59}$$

1.4.1.2 Switching power losses

Average switching losses in a fundamental period can be calculated by the summation of all turn-on and turn-off losses:

$$P_{sw} = \frac{1}{N\cdot T}\cdot\sum_{n=1}^{N}\left[\begin{array}{l}\frac{v_{on}(n)}{V_{100FIT}}\cdot\left(A_{on}\cdot i_{on}(n)^2+B_{on}\cdot i_{on}(n)+C_{on}\right)+\\ +\frac{v_{off}(n)}{V_{100FIT}}\cdot\left(A_{off}\cdot i_{off}(n)^2+B_{off}\cdot i_{off}(n)+C_{off}\right)\end{array}\right] \tag{2.60}$$

where v_{on} and v_{off} are respectively the voltages commutated during turn-on and turn-off, i_{on} and i_{off} are respectively the currents commutated during turn-on and turn-off, V_{100FIT} is the 100FIT test voltage and A_{on}, B_{on}, C_{on} and A_{off}, B_{off}, C_{off} are respectively the turn-on and the turn-off energy loss characteristic coefficients.

Under the assumption of a high switching frequency, the currents and voltages commutated in the turn-on and the turn-off of the semiconductors are assumed to be the same. Moreover, considering a sufficiently large DC bus capacitor, the DC bus voltage ripple can be neglected and the switched voltage is assumed to be the average DC bus voltage V_{bus}.

Thus, the overall expression of the average switching power losses of S_1, D_1, S_2 and D_{c1} are given respectively by:

$$P_{sw\_S1} = \frac{V_{bus} \cdot f_{sw}}{V_{100FIT} \cdot 2 \cdot \pi} \int_{\frac{3 \cdot \pi}{2}}^{\frac{3 \cdot \pi}{2}+\varphi} \left(\left(-I_{\max} \cdot \cos(\omega t - \varphi)\right) \cdot \left(A \cdot \left(-I_{\max} \cdot \cos(\omega t - \varphi)\right) + \cdot B\right) + C\right) dt = \tag{2.61}$$

$$= \frac{V_{bus} \cdot f_{sw}}{4 \cdot \pi \cdot V_{100FIT}} \cdot \left(A \cdot {I_{\max}}^2 \cdot \left(\varphi - \sin(\varphi) \cdot \cos(\varphi)\right) + 2 \cdot B \cdot I_{\max} \cdot \left(1 - \cos(\varphi)\right) + 2 \cdot C \cdot \varphi\right)$$

$$P_{sw\_D1} = \frac{V_{bus} \cdot f_{sw}}{V_{100FIT} \cdot 2 \cdot \pi} \int_{\frac{3 \cdot \pi}{2}+\varphi}^{\frac{5 \cdot \pi}{2}} \left(I_{\max} \cdot \cos(\omega t - \varphi) \cdot \left(A_{off} \cdot I_{\max} \cdot \cos(\omega t - \varphi) + \cdot B_{off}\right) + C_{off}\right) dt = \tag{2.62}$$

$$= \frac{V_{bus} \cdot f_{sw}}{4 \cdot \pi \cdot V_{100FIT}} \cdot \left(A \cdot {I_{\max}}^2 \cdot \left(\pi - \varphi + \sin(\varphi) \cdot \cos(\varphi)\right) + 2 \cdot B \cdot I_{\max} \cdot \left(1 + \cos(\varphi)\right) + 2 \cdot C \cdot \left(\pi - \varphi\right)\right)$$

$$P_{sw\_S2} = \frac{V_{bus} \cdot f_{sw}}{V_{100FIT} \cdot 2 \cdot \pi} \int_{\frac{\pi}{2}+\varphi}^{\frac{3 \cdot \pi}{2}} \left(\left(-I_{\max} \cdot \cos(\omega t - \varphi)\right) \cdot \left(A \cdot \left(-I_{\max} \cdot \cos(\omega t - \varphi)\right) + \cdot B\right) + C\right) dt = \tag{2.63}$$

$$= \frac{V_{bus} \cdot f_{sw}}{4 \cdot \pi \cdot V_{100FIT}} \cdot \left(A \cdot {I_{\max}}^2 \cdot \left(\pi - \varphi + \sin(\varphi) \cdot \cos(\varphi)\right) + 2 \cdot B \cdot I_{\max} \cdot \left(1 + \cos(\varphi)\right) + 2 \cdot C \cdot \left(\pi - \varphi\right)\right)$$

$$P_{sw\_Dc1} = \frac{V_{bus} \cdot f_{sw}}{V_{100FIT} \cdot 2 \cdot \pi} \int_{\frac{\pi}{2}+\varphi}^{\frac{3 \cdot \pi}{2}+\varphi} \left(\left(-I_{\max} \cdot \cos(\omega t - \varphi)\right) \cdot \left(A_{off} \cdot \left(-I_{\max} \cdot \cos(\omega t - \varphi)\right) + \cdot B_{off}\right) + C_{off}\right) dt = \tag{2.64}$$

$$= \frac{V_{bus} \cdot f_{sw}}{4 \cdot \pi \cdot V_{100FIT}} \cdot \left(\pi \cdot A \cdot {I_{\max}}^2 + 4 \cdot B \cdot I_{\max} + 2 \cdot C \cdot \pi\right)$$

$$A = A_{on} + A_{off} \tag{2.65}$$

$$B = B_{on} + B_{off} \tag{2.66}$$

$$C = C_{on} + C_{off} \tag{2.67}$$

where f_{sw} is the semiconductor switching frequency.

1.4.1.3 Total power losses

Once the switching power losses of selected switching devices are calculated, the total conduction and switching losses can be described as:

$$P_{cond} = 6 \cdot \left(P_{cond\_S1} + P_{cond\_D1} + P_{cond\_S2/1} + P_{cond\_S2/2}\right) + 6 \cdot \left(P_{cond\_D1c/1} + P_{cond\_D1c/2}\right) \tag{2.68}$$

$$P_{sw} = 6 \cdot \left(P_{sw\_S1} + P_{sw\_D1} + P_{sw\_S2} + P_{sw\_Dc1}\right) \tag{2.69}$$

$$P_{losses} = P_{cond} + P_{sw} \tag{2.70}$$

1.4.2 DC bus capacitor design

The DC bus of the 3L-NPC is composed of two series connected capacitors. Ideally, both absorb the same amount of charges and therefore, their capacitance is same. Thus, for the sake of simplicity, the following analysis is focused on the upper capacitor C_{bus1}.

Assuming a constant DC bus voltage with no ripple (V_{bus}), the current circulating through the positive bus terminal (i_{bus} of Fig 2.8) depends on the instantaneous power *p(t)* and the voltage of the upper capacitor ($V_{bus}/2$):

$$i_{bus} = \frac{2 \cdot p(t)}{V_{bus}} \tag{2.71}$$

If one leg is applying a positive voltage to the phase terminal, the phase current circulates through the positive bus terminal.

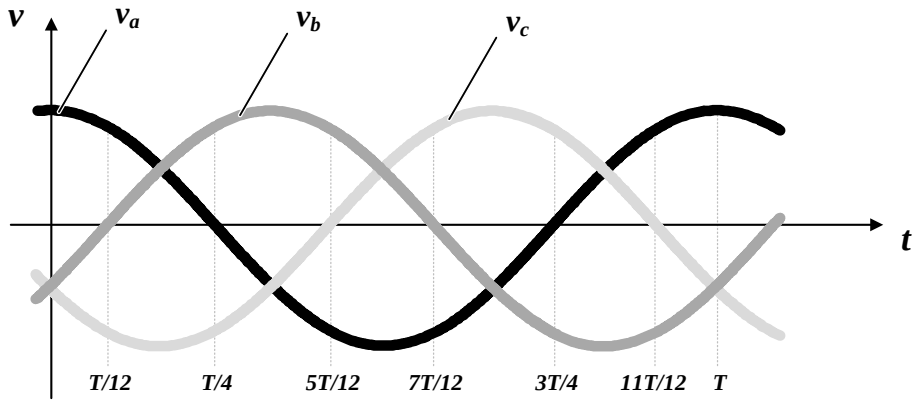


Fig 2.12. AC side voltage waveforms of the 3L-NPC.

Assuming a unitary power factor, Fig 2.12 shows the different time intervals to calculate the i_{bus} current circulating through the positive bus terminal. Phase *a* current circulates from 0 to *T/4* and from *3T/4* to *T*. Similarly, phase *b* current circulates through the positive bus terminal from *T/12* to *7T/12*, while phase *c* current does it from *5T/12* to *11T/12*. Thus, the instantaneous i_{bus} current circulating through the positive bus terminal are calculated as follows:

- From 0 to *T/12*:

$$\begin{aligned} i_{bus} &= \frac{2 \cdot p(t)}{V_{bus}} = \frac{2}{V_{bus}} \cdot \left(v_a(t) \cdot i_a(t) + 0 \cdot i_b(t) + 0 \cdot i_c(t)\right) = \\ &= \frac{2}{V_{bus}} \cdot V_{\max} \cdot \cos(\omega t) \cdot I_{\max} \cdot \cos(\omega t) = \frac{V_{\max} \cdot I_{\max}}{V_{bus}} \cdot \left(1 + \cos(2\omega t)\right) \end{aligned} \tag{2.72}$$

where V_{max} and I_{max} are the peak phase voltage and current respectively.

- From *T/12* to *T/4*:

$$i_{bus} = \frac{2 \cdot p(t)}{V_{bus}} = \frac{2}{V_{bus}} \cdot \left(v_a(t) \cdot i_a(t) + v_b(t) \cdot i_b(t) + 0 \cdot i_c(t)\right) =$$

$$= \frac{2}{V_{bus}} \cdot \left(V_{\max} \cdot \cos(\omega t) \cdot I_{\max} \cdot \cos(\omega t) + V_{\max} \cdot \cos\left(\omega t - \frac{2 \cdot \pi}{3}\right) \cdot I_{\max} \cdot \cos\left(\omega t - \frac{2 \cdot \pi}{3}\right)\right) = \tag{2.73}$$

$$= \frac{V_{\max} \cdot I_{\max}}{V_{bus}} \cdot \left(2 - \cos\left(2\omega t - \frac{2 \cdot \pi}{3}\right)\right)$$

- From *T/4* to *5T/12*:

$$i_{bus} = \frac{2 \cdot p(t)}{V_{bus}} = \frac{2}{V_{bus}} \cdot \left(0 \cdot i_a(t) + v_b(t) \cdot i_b(t) + 0 \cdot i_c(t)\right) =$$

$$= \frac{2}{V_{bus}} \cdot V_{\max} \cdot \cos\left(\omega t - \frac{2 \cdot \pi}{3}\right) \cdot I_{\max} \cdot \cos\left(\omega t - \frac{2 \cdot \pi}{3}\right) = \frac{V_{\max} \cdot I_{\max}}{V_{bus}} \cdot \left(1 + \cos\left(2\omega t - \frac{4 \cdot \pi}{3}\right)\right) \tag{2.74}$$

- From *5T/12* to *7T/12*:

$$i_{bus} = \frac{2 \cdot p(t)}{V_{bus}} = \frac{2}{V_{bus}} \cdot \left(0 \cdot i_a(t) + v_b(t) \cdot i_b(t) + v_c(t) \cdot i_c(t)\right) =$$

$$= \frac{2}{V_{bus}} \cdot V_{\max} \cdot \cos\left(\omega t - \frac{2 \cdot \pi}{3}\right) \cdot I_{\max} \cdot \cos\left(\omega t - \frac{2 \cdot \pi}{3}\right) +$$

$$+ \frac{2}{V_{bus}} \cdot V_{\max} \cdot \cos\left(\omega t + \frac{2 \cdot \pi}{3}\right) \cdot I_{\max} \cdot \cos\left(\omega t + \frac{2 \cdot \pi}{3}\right) = \tag{2.75}$$

$$= \frac{V_{\max} \cdot I_{\max}}{V_{bus}} \cdot \left(2 - \cos(2\omega t)\right)$$

- From *7T/12* to *3T/4*:

$$i_{bus} = \frac{2 \cdot p(t)}{V_{bus}} = \frac{2}{V_{bus}} \cdot \left(0 \cdot i_a(t) + 0 \cdot i_b(t) + v_c(t) \cdot i_c(t)\right) =$$

$$= \frac{2}{V_{bus}} \cdot V_{\max} \cdot \cos\left(\omega t + \frac{2 \cdot \pi}{3}\right) \cdot I_{\max} \cdot \cos\left(\omega t + \frac{2 \cdot \pi}{3}\right) = \frac{V_{\max} \cdot I_{\max}}{V_{bus}} \cdot \left(1 + \cos\left(2\omega t + \frac{4 \cdot \pi}{3}\right)\right) \tag{2.76}$$

- From *3T/4* to *11T/12*:

$$i_{bus} = \frac{2 \cdot p(t)}{V_{bus}} = \frac{2}{V_{bus}} \cdot \left(v_a(t) \cdot i_a(t) + 0 \cdot i_b(t) + v_c(t) \cdot i_c(t)\right) =$$

$$= \frac{2}{V_{bus}} \cdot \left(V_{\max} \cdot \cos(\omega t) \cdot I_{\max} \cdot \cos(\omega t) + V_{\max} \cdot \cos\left(\omega t + \frac{2 \cdot \pi}{3}\right) \cdot I_{\max} \cdot \cos\left(\omega t + \frac{2 \cdot \pi}{3}\right)\right) = \quad (2.77)$$

$$= \frac{V_{\max} \cdot I_{\max}}{V_{bus}} \cdot \left(2 - \cos\left(2\omega t + \frac{2 \cdot \pi}{3}\right)\right)$$

- From *11T/12* to *T*:

$$i_{bus} = \frac{2 \cdot p(t)}{V_{bus}} = \frac{2}{V_{bus}} \cdot \left(v_a(t) \cdot i_a(t) + 0 \cdot i_b(t) + 0 \cdot i_c(t)\right) =$$

$$= \frac{2}{V_{bus}} \cdot V_{\max} \cdot \cos(\omega t) \cdot I_{\max} \cdot \cos(\omega t) = \frac{V_{\max} \cdot I_{\max}}{V_{bus}} \cdot \left(1 + \cos(2\omega t)\right) \quad (2.78)$$

The estimated current through positive bus terminal is shown in Fig 2.13. As it is noticed, the current oscillates over a mean value, which is the average power provided by the AC supply.

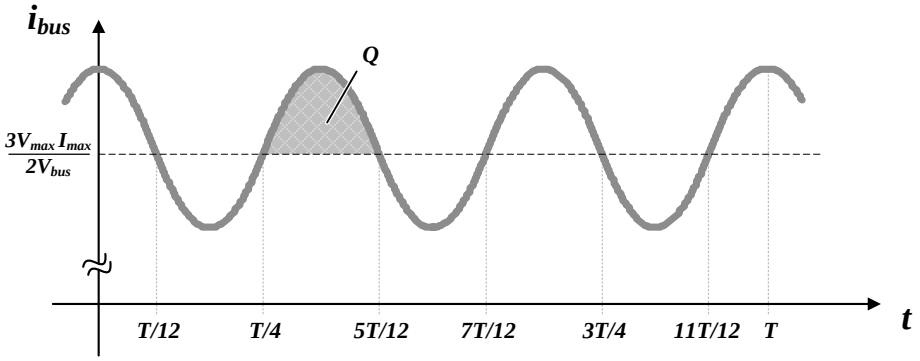


Fig 2.13. Current circulating through the positive bus terminal of the 3L-NPC.

Assuming the mean current is drawn by the load connected to the DC bus, the current circulating through the capacitor will be the oscillating term of i_{bus}, which is given by the third harmonic of the fundamental period (T). Thus, the Q charges illustrated in Fig 2.13 and circulating through C_{bus1} can be expressed as:

$$Q = \int_{\frac{T}{4}}^{\frac{5 \cdot T}{12}} i_{Cbus}(t)dt = \int_{\frac{T}{4}}^{\frac{5 \cdot T}{12}} \frac{V_{\max} \cdot I_{\max}}{V_{bus}} \cdot \left(1 + \cos\left(2\omega t - \frac{4 \cdot \pi}{3}\right) - \frac{3}{2}\right)dt =$$

$$= \frac{V_{\max} \cdot I_{\max} \cdot T}{4 \cdot V_{bus}} \cdot \left(\frac{\sqrt{3}}{\pi} - \frac{1}{3}\right) \approx \frac{V_{\max} \cdot I_{\max} \cdot T}{6 \cdot \pi \cdot V_{bus}} \quad (2.79)$$

Hence, the capacitance of C_{bus1} is provided by Eq. (2.79) and the desired voltage ripple (Δv):

$$C_{bus1} = \frac{V_{\max} \cdot I_{\max} \cdot T}{4 \cdot V_{bus} \cdot \Delta v} \cdot \left(\frac{\sqrt{3}}{\pi} - \frac{1}{3} \right) \approx \frac{V_{\max} \cdot I_{\max} \cdot T}{6 \cdot \pi \cdot V_{bus} \cdot \Delta v} \tag{2.80}$$

As it has been assumed that capacitor C_{bus2} absorb the same amount of charges as capacitor C_{bus1}, it is considered that their capacitance is same.

Since the DC bus capacitors are series connected, the total capacitance required by the DC bus (C_{bus}) can be approximated to:

$$C_{bus} \approx \frac{V_{\max} \cdot I_{\max} \cdot T}{12 \cdot \pi \cdot V_{bus} \cdot \Delta v} \tag{2.81}$$

1.5 Cascaded H-bridge converter

The cascaded H-bridge (CHB) converter [13-14] has been used in real drive applications [5] and static synchronous compensator (STATCOM) applications [15-17]. As illustrated in Fig 2.14, the CHB converter is composed of series connected single-phase H-bridge (HB) converters. Each HB converter comprises one DC bus capacitor and four bidirectional switches. Generally speaking, the number chained HB converters depends on the AC side voltage and the voltage blocking capability of the used switching devices. For a given semiconductor device, a higher AC side voltage leads to a higher number of chained HB converters. Thus, series connection of power semiconductor devices is not required. The increase of HB modules increases the number of voltage levels at the AC output terminals and hence, the output voltage quality is improved (less *dv/dt* and harmonic distortion).

The modularity of this converter makes possible the use of simple and well known HB modules, which brings economical and technical benefits [15]. In addition, redundant HB modules can be included so as to increase the reliability of the converter. Thus, the failure of one HB converter does not jeopardize the energy transmission capability of the converter [18].

The main drawback resides in the need of independent DC power supplies for each HB converter, especially, when active power is transferred. Additionally, the capacitance required by the DC bus is higher than that required by three-phase rectifiers due to the second harmonic current component. This will be discussed later on section 2.5.2.

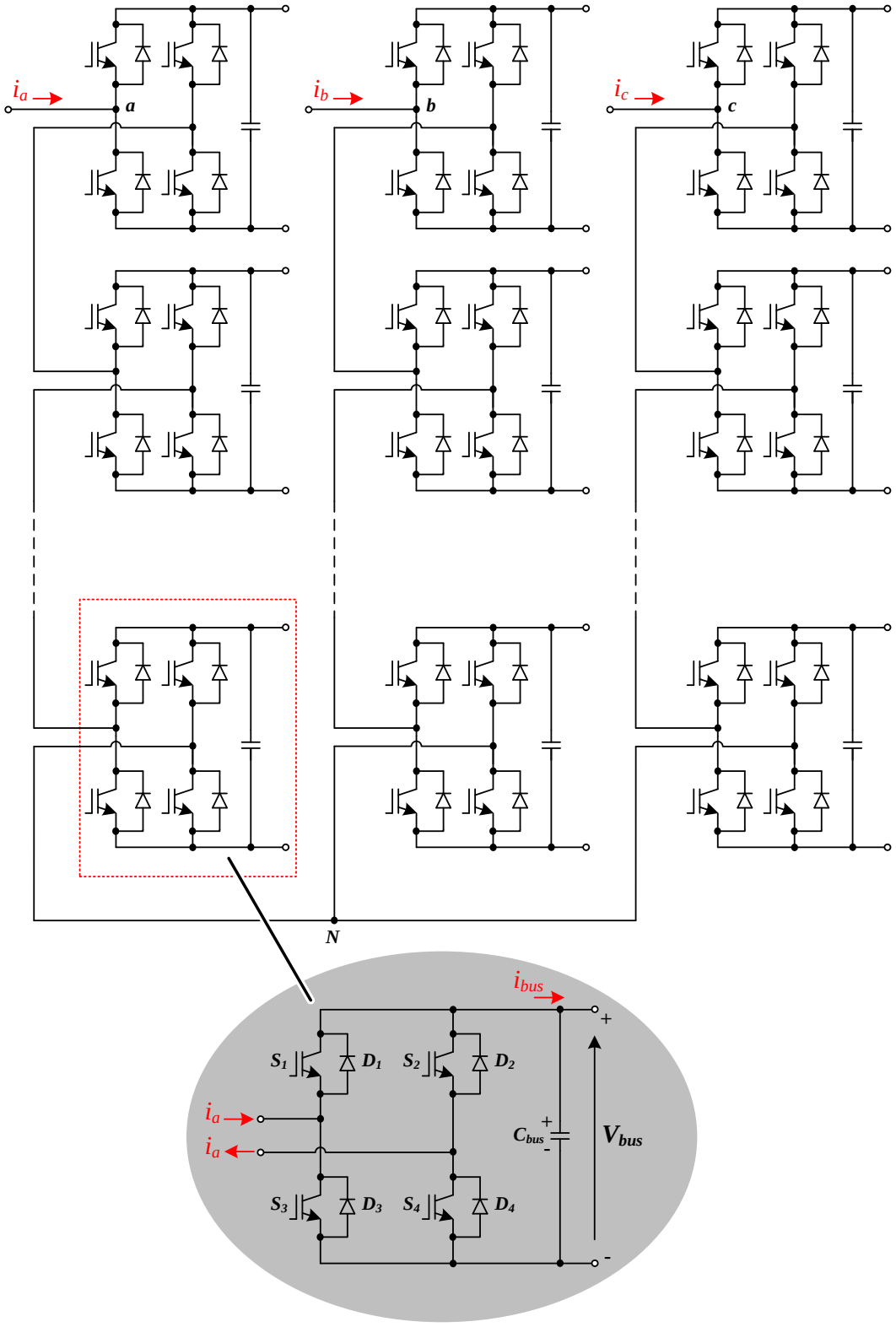


Fig 2.14. Cascaded H-bridge converter.

Table 2.3 shows the allowed switching states and the three different voltages synthesized at the output of each HB (V_{bus}, *0* and $-V_{bus}$). When switches S_1 and S_4 are on, a V_{bus} voltage is applied at the output terminals. Conversely, when switches S_2 and S_3 are on, a $-V_{bus}$

voltage is applied at the output terminals. Finally, two operational states can be used to apply 0 volts at the phase terminals, S_1=S_2=1 or S_3=S_4=1. From Table 2.3 and Fig 2.14, it can be deduced that switches S_1 and S_3 are complementary since their simultaneous conduction leads to a DC bus short circuit. This is applied also to switches S_2 and S_4. The used switching devices must withstand the DC bus voltage of the HB converter (V_{bus}).

TABLE 2.3
OPERATIONAL STATES OF THE SINGLE-PHASE HB CONVERTER

Voltage applied at phase terminal	S_1	S_2	S_3	S_4
V_{bus}	1	0	0	1
0	1	1	0	0
0	0	0	1	1
-V_{bus}	0	1	1	0

Since switches S_1 and S_3 as well as S_2 and S_4 are complementary, the output voltage of a HB converter can be expressed as a function of the switching states of S_1 and S_2:

$$V_{out,HB} = V_{bus} \cdot (S_1 + S_2 - 1) \tag{2.82}$$

Therefore, it can be deduced that the maximum voltage applied by a CHB converter composed of n_{HB} modules with the same DC bus voltage (V_{bus}) is:

$$V_{\max,CHB} = V_{bus} \cdot n_{HB} \tag{2.83}$$

For that number of HB modules, the number of phase voltage levels (k) and the number of line to line voltage levels (h) are:

$$k = 2 \cdot n_{HB} + 1 \tag{2.84}$$

$$h = 2 \cdot k - 1 \tag{2.85}$$

The preferred modulation techniques for the CHB converters are the phase-shifted PWM and the SVM [19].

Fig 2.15 shows the typical voltage and command waveforms of a single-phase HB converter modulated with a phase-shifted PWM technique. As it can be seen, there are two triangular carriers (v_{cr1} and v_{cr2}) phase-shifted 180 degrees each other and a reference voltage (v_{HB}*). The switching orders of S_1 depends on the triangular carrier wave v_{cr1} while the orders of S_4 depends on v_{cr2}.

While the carriers of a HB are 180 degrees phase-shifted in order to synthesize a proper voltage waveforms, the carriers of the different n_{HB} HB modules must be phase-shifted in PS degrees:

$$PS = \frac{180^{\circ}}{n_{HB}} \tag{2.86}$$

Additionally, the modulation index m_{HB} of each HB converter depends on its DC bus voltage (V_{bus}) and the number of chained converters (n_{HB}):

$$m_{HB} = \frac{v^*}{V_{bus} \cdot n_{HB}} \tag{2.87}$$

where v^* is the maximum phase reference voltage.

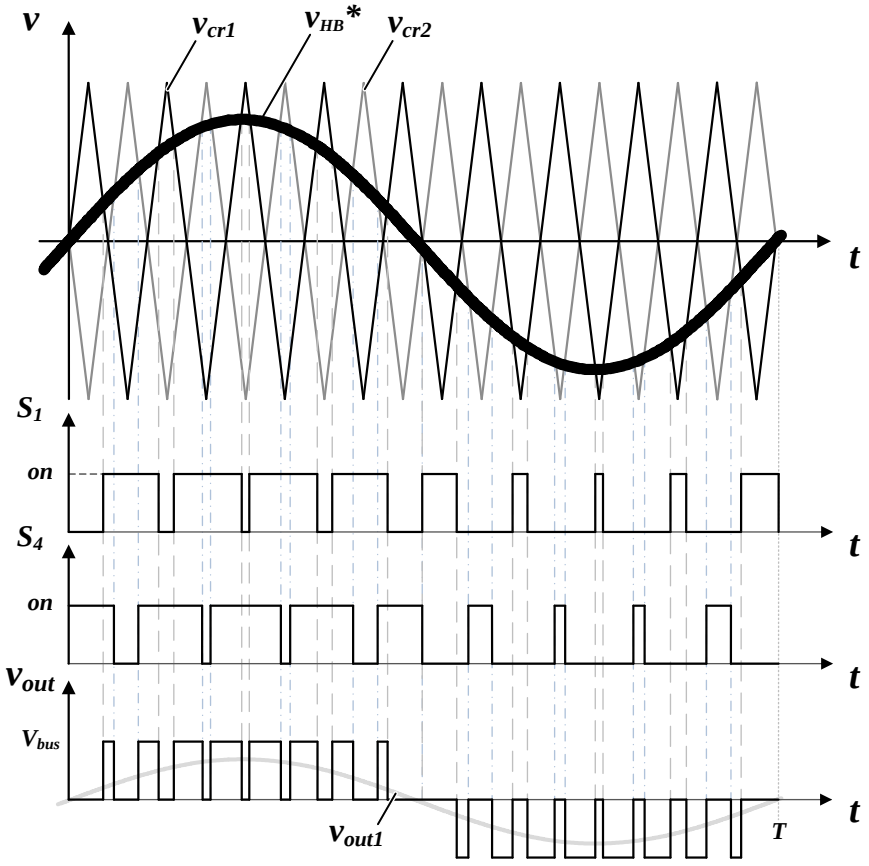


Fig 2.15. Typical command and voltage waveforms of a single-phase HB converter.

1.5.1 Power losses estimation

As shown in Fig 2.15, the behaviour of each leg of the single-phase HB converter is identical to that of each leg of the 2L-VSC (section 2.3). Hence, power losses can be estimated with Eq. (2.25) and Eq. (2.27) for conduction losses and Eq. (2.35) for switching losses. Therefore, total conduction and switching losses are:

$$P_{cond} = 12 \cdot n_{HB} \cdot \left(P_{cond\_S1} + P_{cond\_D4}\right) \tag{2.88}$$

$$P_{sw} = 12 \cdot n_{HB} \cdot \left(P_{sw\_S1} + P_{sw\_D4}\right) \tag{2.89}$$

$$P_{losses} = P_{cond} + P_{sw} \tag{2.90}$$

1.5.2 DC bus capacitor design

As discussed for the 2L-VSC, capacitance C_{bus} is defined by the charges (Q) circulating through the capacitor and the desired voltage ripple (Δv). In turn, the circulating charges are given by the current circulating through the capacitor (i_{Cbus}), which assuming a constant DC bus with no ripple (V_{bus}), is given by the instantaneous DC side power $p(t)$. Assuming that the load will absorve the mean power, the $2\omega t$ oscillating power is continuously stored and transferred by the bus capacitor.

The DC side current (i_{bus} current depicted in Fig 2.14) depends on the DC bus voltage (V_{bus}) and the instantaneous power ($p(t)$):

$$i_{bus} = \frac{p(t)}{V_{bus}} \tag{2.91}$$

In addition, the DC bus voltage of each HB converter is given by the peak phase voltage (V_{max}) and the number of phase modules (n_{HB}):

$$V_{bus} = \frac{V_{\max}}{n_{HB}} \tag{2.92}$$

Assuming a unitary power factor, the instantaneous power absorbed by each HB module is:

$$p(t) = v(t) \cdot i(t) = V_{\max HB} \cdot \sin(\omega t) \cdot I_{\max HB} \cdot \sin(\omega t) = \frac{V_{\max HB} \cdot I_{\max HB}}{2} \cdot (1 - \cos(2\omega t)) \tag{2.93}$$

where V_{maxHB} and I_{maxHB} are respectively the maximum output voltage and the maximum current through each HB module.

As it can be observed in Eq. (2.93), the instantaneous power has two main components: a constant term and an oscillating term. As the constant term is the average power transferred by the converter, the power circulating through the capacitor is equal to the oscillating term:

$$p(t) = -\frac{V_{\max HB} \cdot I_{\max HB}}{2} \cdot \cos(2\omega t) \tag{2.94}$$

Introducing Eq. (2.94) into Eq. (2.91), the current through the capacitor is expressed as:

$$i_{Cbus}(t) = -\frac{V_{\max HB} \cdot I_{\max HB}}{2 \cdot V_{bus}} \cdot \cos(2\omega t) \tag{2.95}$$

As it is noticed in the current circulating through the C_{bus} capacitor illustrated in Fig 2.16, the charges are absorbed between $T/8$ and $3T/8$:

$$Q = \int_{\frac{T}{8}}^{\frac{3 \cdot T}{8}} i_{Cbus}(t)dt = \frac{V_{\max HB} \cdot I_{\max HB} \cdot T}{4 \cdot \pi \cdot V_{bus}} \tag{2.96}$$

where T is the fundamental period of the AC side current.

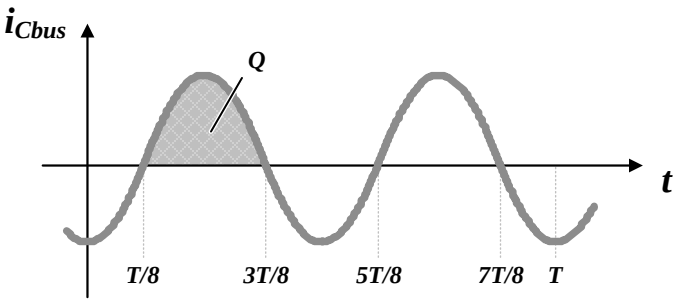


Fig 2.16. Current circulating through the DC bus capacitor of a HB module.

Therefore, the required DC bus capacitance to obtain a given voltage ripple (Δv) can be expressed as:

$$C_{bus} = \frac{V_{\max HB} \cdot I_{\max HB} \cdot T}{4 \cdot \pi \cdot V_{bus} \cdot \Delta v} \tag{2.97}$$

It must be highlighted that single-phase HB converters require larger capacitor values than three-phase converters. This difference comes from the second current harmonic component circulating in the DC bus capacitor of single phase converters shown by Eq. (2.97).

1.6 Summary

Rectifiers convert AC side voltages and currents to DC side voltages and currents. Depending on the rectifier type, the DC side voltage can be constant or AC input voltage dependent. In this chapter, different rectifier topologies have been studied. For each converter, analytical expressions for the estimation of the DC bus capacitor and power losses have been presented.

The main characteristics of the analysed converters can be summarized as:

- The three-phase DFE rectifier is a unidirectional, cheap, simple and reliable converter. As this converter does not provide any control over the output voltage, the DC side voltage is dependent on the AC input voltage. Compared to VSC type rectifiers, the AC side current waveform contains more harmonic components, which provoke heating and torque issues to the generators in the AC side.
- Compared with the DFE rectifier, 2L-VSC requires controlled switching devices that increase its complexity. However, the DC bus voltage controllability and the better AC side waveforms quality have become this converter in one of the most used rectifiers in several industrial applications.
- Multilevel converters overtake the 2L-VSC in terms of switch power losses, harmonic distortion, applied voltage derivatives to the AC side generator and

common mode voltage. The 3L-NPC has become the preferred multilevel converter demonstrating a reliable and efficient performance. As each leg is composed of four series connected switching devices, the total DC bus voltage can be twice the DC bus voltage of the 2L-VSC. In consequence, this converter is better suited for medium voltage than the 2L-VSC.

- The modular structure of the CHB makes possible the operation of the converter at high voltages and the use of redundant modules leads to high reliability. Its main drawback is the high number of capacitors it requires. Furthermore, as the CHB converter is composed of single-phase HB converters, the second current harmonic component circulating through their DC bus capacitors makes the required DC bus capacitor larger than that required by three-phase converters.

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Chapter 2

DC-DC converters

This chapter describes the main features of 17 different switch mode DC-DC converters and 10 different resonant mode DC-DC converter topologies. It also discusses analytical models required for their design and semiconductor power loss estimation.

2.1 Introduction

DC-DC converters are used to convert an input DC voltage level to another output DC voltage level. Generally speaking, the converters that maintain the output voltage higher than the input voltage are known as step-up converters or boost derived converters. Conversely, step-down or buck derived converters maintain the output voltage lower than the input voltage. The converters that allow the output voltage being either higher or lower than the input voltage are known as step-up/down or buck/boost converters.

Depending on the switching conditions of the semiconductors, DC-DC converters can be divided in two main groups: switch mode converters and resonant mode converters. On the one hand, most of the switch mode converters operate under hard switching conditions. In consequence, the semiconductors must withstand high switching stresses making the switching power losses to increase linearly with the switching frequency. In addition, the electromagnetic interferences (EMIs) produced by the high *di/dt* and *dv/dt* are another drawback of this kind of converters. In order to reduce the problems derived from the hard switching conditions, the converters operate with relatively low switching frequencies and thereby, the volume, size and weight of these converters is high (low power density). On the other hand, resonant mode converters provide soft switching conditions to the semiconductors (zero voltage switching or zero current switching) and

therefore, the aforementioned problems can be avoided or, at least, reduced. Thus, operation at higher frequencies is possible. Main drawbacks of resonant converters reside on the volume of the resonant tank and the voltage/current stress of the passive elements of the resonant tank.

When an AC input voltage has a variable amplitude (for example an AC source regulated through an autotransformer) and is rectified through a three-phase DFE rectifier, the input DC bus voltage of the DC-DC converter completely depends on the AC input voltage amplitude. This makes the DC-DC converter to operate with a non-constant input voltage, which makes more challenging its design and control. These issues can be addressed if the input DC voltage of the DC-DC converter is kept constant. To do so, AFE rectifiers must be considered.

In this chapter, 17 different switch mode converters and 10 different resonant mode converters are analysed. Converter design equations and power loss estimation methods are discussed. Although most of the analyzed DC-DC converters require a medium frequency transformer (MFT), its analysis is not discussed along this chapter. The thorough analysis of the MFT will be discussed in Chapter 4.

2.2 Switch mode DC-DC converters

Generally speaking, switch mode DC-DC converter semiconductors are operated under hard switching conditions. However, soft switching operation conditions can also be achieved if specific converter topologies (e.g. single-active-bridge and dual-active-bridge), modulation techniques (e.g. phase-shifting) or additional circuitry (e.g. snubbers) are considered.

In this section, converter design and power loss estimation expressions are presented for different converter topologies. On the one hand, it is assumed that main power losses of the converter come from the power semiconductors. In consequence, power losses in the passive elements are neglected. Therefore, total average power losses of the converters are calculated by the sum of average conduction power losses (Eq. (3.1)) and average switching power losses (Eq. (3.2)) of the semiconductors. Average conduction power losses depend on *rms* and average currents (I_{rms}, I_{ave}) through the semiconductors and the output characteristic of the semiconductor (r_d, V_{th}). In turn, average switching power losses depend on switched voltages (v_{sw}) and currents (i_{sw}) and the switching loss characteristic provided by the manufacturer (A_{sw}, B_{sw} and C_{sw}). Additionally, analytical expressions of the maximum current circulating through the semiconductors (i_{max}) and their maximum reverse blocking voltage (v_{max}) are calculated. These calculations allow selecting semiconductors with appropriate voltage and current ratings for each converter. All the aforementioned expressions have been validated through simulations in Synopsys/SABER platform as it is shown in Appendix A.

$$P_{cond} = r_d \cdot I_{rms}{}^2 + V_{th} \cdot I_{ave} \tag{3.1}$$

$$P_{sw} = \frac{1}{N} \cdot \sum_{n=1}^{N} \frac{v_{sw}(n)}{V_{100FIT}} \cdot \left(A_{sw} \cdot i_{sw}(n)^2 + B_{sw} \cdot i_{sw}(n) + C_{sw} \right) \cdot f_{sw} \tag{3.2}$$

where r_d is the semiconductor switch on-state resistance, V_{th} is the threshold voltage, f_{sw} is the switching frequency and A_{sw}, B_{sw}, C_{sw} are the energy loss characteristic provided by the manufacturer for the 100FIT test voltage (V_{100FIT}).

On the other hand, this section discusses the design expressions required for the sizing of each converter. Moreover, in order to minimize the installed semiconductor power, the semiconductor utilization factor [20] of each converter has been calculated. This factor determines the relation between the installed semiconductor power and the rated power of the converter:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} \tag{3.3}$$

where v_{max} is the maximum reverse blocking voltage of the semiconductors and I_{rms} is the *rms* current circulating through them.

In order to obtain easy to use expressions, the semiconductor utilization factor has been calculated assuming a continuous current mode (CCM) operation of the converters and neglecting the voltage ripple in v_{max} and current ripple in I_{rms}.

In order to reduce the number of equations of the buck/boost type DC-DC converters, only the expressions of the boost operation cases are discussed, i.e. it is assumed that the output voltage is higher than the input voltage. The expressions of the buck operation cases, when the output voltage is lower than the input voltage, could be easily deduced from the waveforms shown in each section.

2.2.1 Boost

The boost converter is a well known unidirectional step-up converter used in applications where no galvanic isolation is required [8]. Depicted in Fig 3.1, the converter has few components, which makes its structure to be simple and reliable.

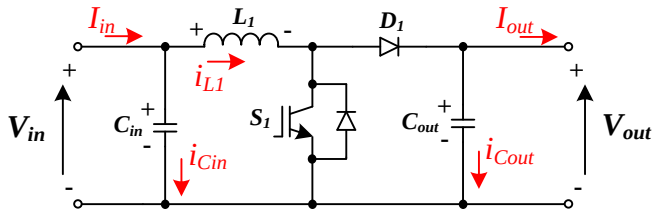


Fig 3.1. Boost converter.

2.2.1.1 Converter design

The converter operates storing the energy coming from the input in L_1 and then transferring it to the output. As shown in Fig 3.2a, when transistor S_1 is on (T_{on} time

interval), the energy coming from the input is stored in the inductor L_1 and the output power is supplied by the capacitor C_{out}. When transistor S_1 is off (T_{off} time interval), the energy coming from the input and the energy stored in L_1 are transferred to C_{out} and the output load (Fig 3.2b). If the current circulating through the inductor L_1 is greater than zero, the converter operates in a continuous current mode (CCM). In contrary, if the inductor current reaches to be zero, the converter operates in a discontinuous current mode (DCM).

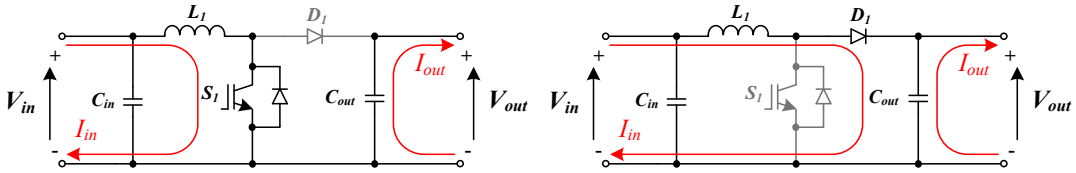


Fig 3.2. Currents circulating through the boost converter a) when S_1 is on and b) when S_1 is off.

Therefore, considering a steady state CCM operation, the voltage and current waveforms of the inductor L_1 and the capacitor C_{out} are illustrated in Fig 3.3a and Fig 3.3b. Notice that the voltage ripple in L_1 and the current ripple in C_{out} have been neglected.

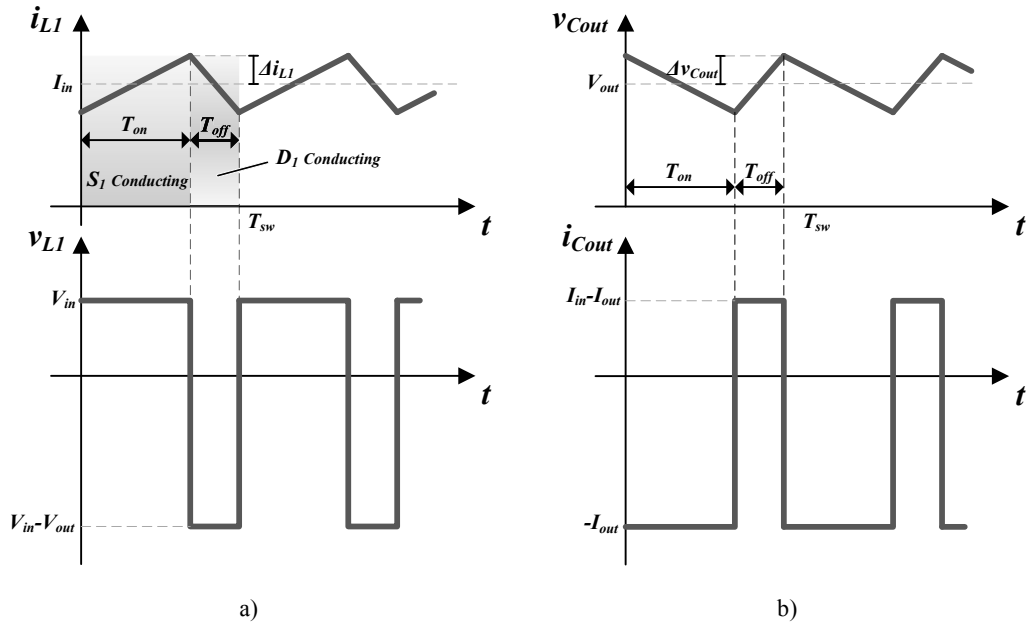


Fig 3.3. Typical voltage and current waveforms in boost converter's a) inductor L_1 and b) capacitor C_{out}.

The relation between the input voltage and the output voltage (DC voltage transfer function) can be obtained from Fig 3.3a. As the average current circulating through L_1 is constant, the mean voltage drop in the inductor ($<v_{L1}>$) during a switching period T_{sw} is equal to zero, Eq. (3.4). Developing Eq. (3.4), the DC voltage transfer function given by Eq. (3.5) is obtained.

$$\langle v_{L1} \rangle = \frac{1}{T_{sw}} \cdot \left(\int_0^{T_{on}} v_{L1}\ dt + \int_{T_{on}}^{T_{sw}} v_{L1}\ dt \right) = 0 \tag{3.4}$$

$$V_{out} = \frac{V_{in}}{1-\delta} \tag{3.5}$$

$$\delta = \frac{T_{on}}{T_{sw}} \tag{3.6}$$

where V_{in} and V_{out} are the average input and output voltages respectively (cf. Fig 3.1), δ is the transistor's duty cycle and T_{sw} is the switching period. Eq. (3.5) shows that the output voltage is higher than the input voltage for any duty cycle. So, the step-up nature of this converter is corroborated.

Similarly, the relation between the input current and the output current (DC current transfer function) is obtained. From Fig 3.3b the average voltage of C_{out} is constant and in consequence, the average current through the capacitor ($<i_{Cout}>$) during a switching period T_{sw} is equal to zero, Eq. (3.7). Solving Eq. (3.7) for the currents in Fig 3.3b, the DC current transfer function given by Eq. (3.8) is obtained.

$$\langle i_{Cout} \rangle = \frac{1}{T_{sw}} \cdot \left(\int_0^{T_{on}} i_{Cout}\ dt + \int_{T_{on}}^{T_{sw}} i_{Cout}\ dt \right) = 0 \tag{3.7}$$

$$I_{out} = I_{in} \cdot (1-\delta) \tag{3.8}$$

where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.1).

As it can be concluded from Eq. (3.5) and Eq. (3.8), the duty cycle of the boost converter must be lower than one. If the duty cycle is equal to one, the input current will theoretically increase up to infinite while the load will discharge the output capacitance. This undesired behaviour can be easily avoided limiting the maximum duty cycle of the converter.

Fixing the desired current ripple Δi_{L1} and voltage ripple Δv_{Cout}, the values of L_1 and C_{out} are calculated from Fig 3.3a and Fig 3.3b respectively:

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L1}} \cdot \delta \cdot T_{sw} \tag{3.9}$$

$$C_{out} = i_{Cout} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{Cout}} \cdot \delta \cdot T_{sw} \tag{3.10}$$

Assuming the input current I_{in} is constant and non-zero, Fig 3.4 shows that the current circulating through the input capacitor (C_{in}) has a zero average value and the same current ripple as that in the inductor (Δi_{L1}).

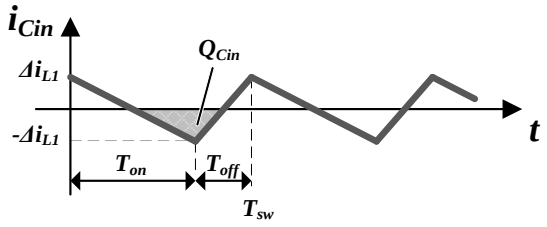


Fig 3.4. Current circulating through the input capacitor of the boost converter.

From Fig 3.4 the charges (Q_{Cin}) circulating through C_{in} can be trigonometrically calculated. Hence, as the capacitance is given by the charges circulating through the capacitor and the desired voltage ripple (Δv_{Cin}), the capacitance of C_{in} is calculated as:

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{\Delta i_{L1}}{8 \cdot \Delta v_{Cin}} \cdot T_{sw} \tag{3.11}$$

Table 3.1 summarizes the expressions of the *rms* current circulating through passive elements (determines the thermal stress), their maximum voltage stress (determines the voltage rating) and the energy they store (it is an image of the volume), which are calculated from Fig 3.3 and Fig 3.4.

Additionally, the semiconductor utilization factor is obtained introducing the I_{rms} current values and the v_{max} voltage values shown in Table 3.2 into Eq. (3.3):

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{1-\delta}{\sqrt{\delta} + \sqrt{1-\delta}} \tag{3.12}$$

TABLE 3.1

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2} \cdot C_{in} \cdot (V_{in} + \Delta v_{Cin})^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$(V_{in} + \Delta v_{Cin})$
L_1	$\frac{1}{2} \cdot L_1 \cdot (I_{in} + \Delta i_{L1})^2$	$\sqrt{I_{in}^2 + \frac{\Delta i_{L1}^2}{3}}$	$\approx V_{in}$ or $\approx (V_{out} - V_{in})$
C_{out}	$\frac{1}{2} \cdot C_{out} \cdot (V_{out} + \Delta v_{Cout})^2$	$\sqrt{I_{out}^2 \cdot \delta + (I_{in} - I_{out})^2 \cdot (1-\delta)}$	$(V_{out} + \Delta v_{Cout})$

The utilization factor for different duty cycle values is plotted in Fig 3.5. As it can be noticed, the utilization factor is maximized operating at low duty cycles. Although the converter should be designed for operating with a low duty cycle and a high utilization

factor, the boost converter is commonly designed for duty cycles close to its maximum value leading to a poor utilization of the semiconductors.

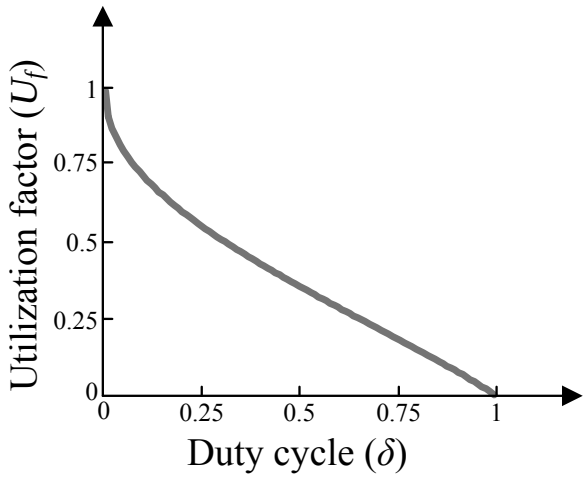


Fig 3.5. Semiconductor utilization factor of the boost converter.

2.2.1.2 Power losses estimation

During the turn-on time interval, the transistor conducts the inductor (L_1) current while during the turn-off time interval, the inductor current circulates through the diode. Therefore, the currents and voltages in the semiconductors are calculated from Fig 3.3a and summarized in Table 3.2.

TABLE 3.2
EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistor S_1**	**Diode D_1**
Average current (I_{ave})	$I_{in} \cdot \delta$	$I_{in} \cdot (1-\delta)$
rms current (I_{rms})	$\sqrt{\delta \cdot \left({I_{in}}^2 + \frac{{\Delta i_{L1}}^2}{3} \right)}$	$\sqrt{(1-\delta) \cdot \left({I_{in}}^2 + \frac{{\Delta i_{L1}}^2}{3} \right)}$
Maximum current (i_{max})	$(I_{in} + \Delta i_{L1})$	$(I_{in} + \Delta i_{L1})$
Turn-on switched current (i_{on})	$(I_{in} - \Delta i_{L1})$	–
Turn-off switched current (i_{off})	$(I_{in} + \Delta i_{L1})$	$(I_{in} - \Delta i_{L1})$
Maximum voltage (v_{max})	$(V_{out} + \Delta v_{Cout})$	$(V_{out} + \Delta v_{Cout})$
Turn-on switched voltage (v_{on})	$(V_{out} + \Delta v_{Cout})$	–
Turn-off switched voltage (v_{off})	$(V_{out} - \Delta v_{Cout})$	$(V_{out} + \Delta v_{Cout})$

As mentioned in the introduction (section 3.2), the semiconductor power losses are given by the average conduction power losses of Eq. (3.1) and the average switching power losses of Eq. (3.2). Therefore, from the currents summarized in Table 3.2, the average conduction power losses of S_1 and D_1 are expressed respectively as:

$$P_{cond\_S1} = V_{th} \cdot I_{in} \cdot \delta + r_d \cdot \delta \cdot \left({I_{in}}^2 + \frac{\Delta {i_{L1}}^2}{3} \right) \tag{3.13}$$

$$P_{cond\_D1} = V_{th} \cdot I_{in} \cdot (1-\delta) + r_d \cdot (1-\delta) \cdot \left({I_{in}}^2 + \frac{\Delta {i_{L1}}^2}{3} \right) \tag{3.14}$$

where r_d is the semiconductor switch on-state resistance and V_{th} is the semiconductor threshold voltage.

Similarly, the average switching power losses of D_1 are given as follows:

$$P_{sw\_D1} = \frac{(V_{out} + \Delta v_{Cout})}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,D1} \cdot (I_{in} - \Delta i_{L1})^2 + B_{off,D1} \cdot (I_{in} - \Delta i_{L1}) + C_{off,D1} \right) \tag{3.15}$$

where $A_{off,D1}$, $B_{off,D1}$ and $C_{off,D1}$ are the turn-off energy loss characteristic provided by the manufacturer for the 100FIT test voltage (V_{100FIT}).

The average switching losses of S_1 are obtained as below:

$$\begin{aligned} P_{sw\_S1} = {} & \frac{(V_{out} - \Delta v_{Cout})}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,S1} \cdot (I_{in} + \Delta i_{L1})^2 + B_{off,S1} \cdot (I_{in} + \Delta i_{L1}) + C_{off,S1} \right) + \\ & + \frac{(V_{out} + \Delta v_{Cout})}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{on,S1} \cdot (I_{in} - \Delta i_{L1})^2 + B_{on,S1} \cdot (I_{in} - \Delta i_{L1}) + C_{on,S1} \right) \end{aligned} \tag{3.16}$$

where $A_{off,S1}$, $B_{off,S1}$ and $C_{off,S1}$ are the turn-off energy loss characteristic provided by the manufacturer for the 100FIT test voltage. Similarly, $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are the turn-on energy loss characteristic provided by the manufacturer.

2.2.2 Zeta

The zeta converter, illustrated in Fig 3.6, is a unidirectional step-up/down converter suitable for applications where no galvanic isolation is required. The converter comprises two semiconductors (a transistor and a diode) and five passive elements including the input and output capacitors.

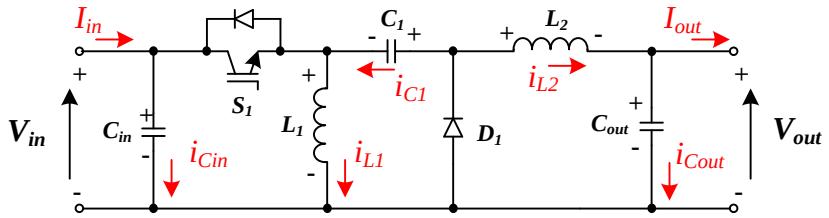


Fig 3.6. Zeta converter.

2.2.2.1 Converter design

The converter operates storing/transferring the energy coming from the input every semiconductor switching period (T_{sw}). Thus, during the on-state of transistor S_1 (T_{on} time interval), the energy coming from the input and the energy stored in C_{in} is transferred to L_1 and the output load, while the energy stored in the capacitor C_1 is transferred to L_2 (Fig 3.7a). Fig 3.7b shows that when S_1 is off (T_{off} time interval), the energy stored in L_1 is transferred to C_1 and the energy stored in L_2 is transferred to the output load. Meanwhile, the energy coming from the input is stored in C_{in}.

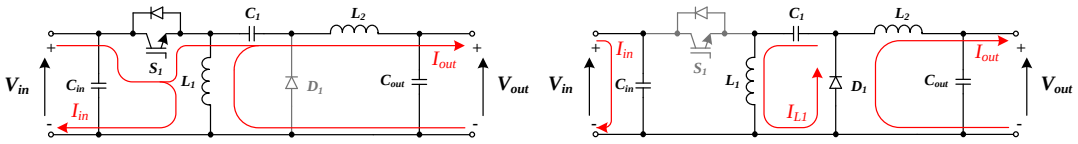


Fig 3.7. Currents circulating through the zeta converter a) when S_1 is on and b) when S_1 is off.

In steady state, assuming a CCM operation, the voltages and currents in L_1, L_2 and C_1 are drawn as in Fig 3.8a, Fig 3.8b and Fig 3.8c respectively. Furthermore, the average voltage of inductor L_1 ($<v_{L1}>$) and inductor L_2 ($<v_{L2}>$) in a switching period (T_{sw}) is zero:

$$\langle v_{L1} \rangle = \frac{1}{T_{sw}} \cdot \left(\int_0^{T_{on}} v_{L1} dt + \int_{T_{on}}^{T_{sw}} v_{L1} dt \right) = 0 \tag{3.17}$$

$$\langle v_{L2} \rangle = \frac{1}{T_{sw}} \cdot \left(\int_0^{T_{on}} v_{L2} dt + \int_{T_{on}}^{T_{sw}} v_{L2} dt \right) = 0 \tag{3.18}$$

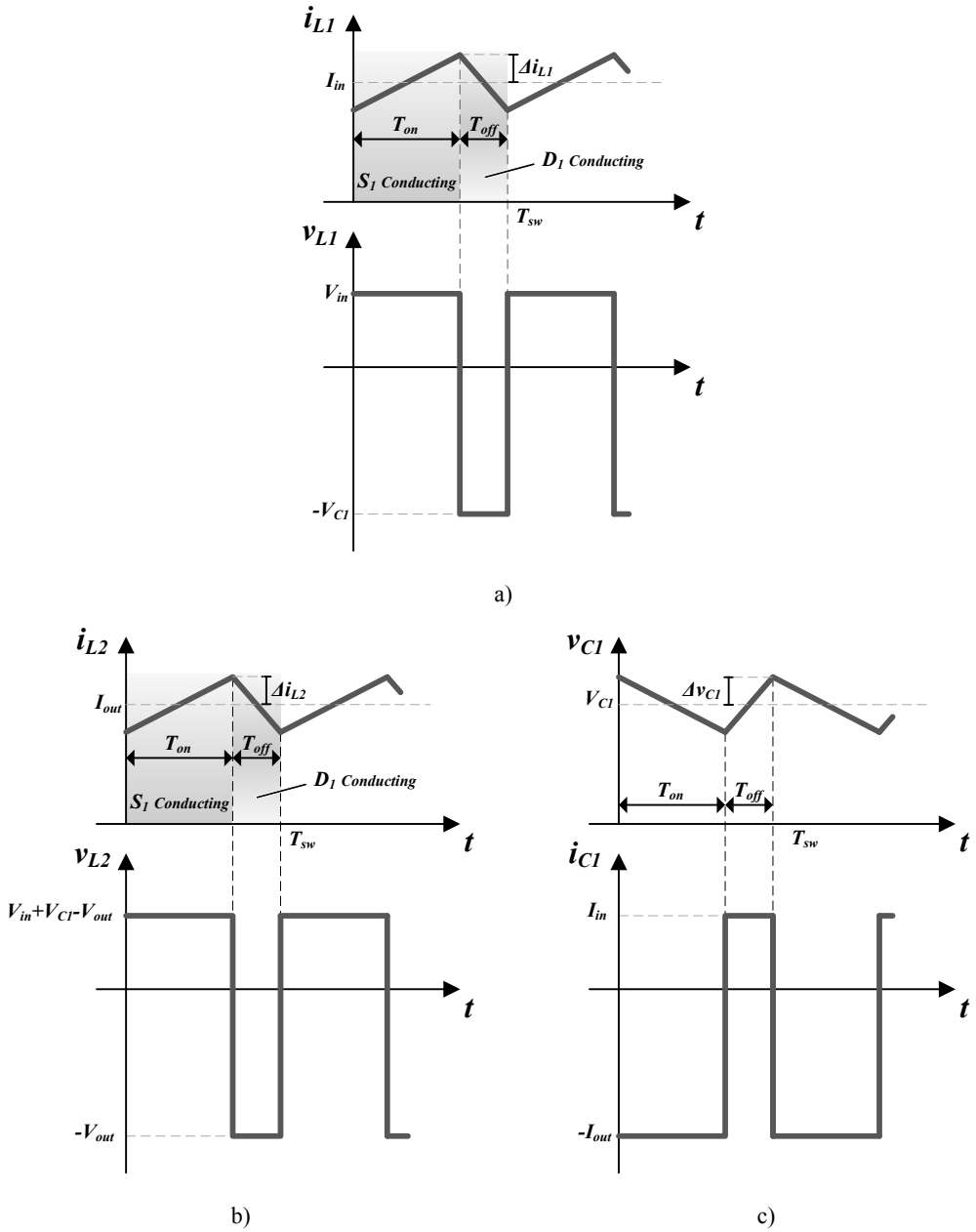


Fig 3.8. Typical voltage and current waveforms in zeta converter's a) inductor L_1, b) inductor L_2 and c) capacitor C_1.

Thus, from Fig 3.8a and Eq. (3.17), Eq. (3.19) is obtained and similarly, from Fig 3.8b and Eq. (3.18), Eq. (3.20) is obtained.

$$V_{in} = V_{C1} \cdot \frac{(1-\delta)}{\delta} \tag{3.19}$$

$$V_{out} = (V_{in} + V_{C1}) \cdot \delta \tag{3.20}$$

where δ is the duty cycle of the converter (T_{on}/T_{sw}), V_{in} and V_{out} are the average input and output voltages respectively (cf. Fig 3.6) and V_{C1} is the average voltage of C_1.

The average voltage of C_1 is obtained introducing Eq. (3.19) into Eq. (3.20):

$$V_{C1} = V_{out} \tag{3.21}$$

And introducing Eq. (3.21) into Eq. (3.19), the DC voltage transfer function is obtained:

$$V_{out} = V_{in} \cdot \frac{\delta}{(1-\delta)} \tag{3.22}$$

From Eq. (3.22), the output voltage of the zeta converter can be either, higher or lower than the input voltage (step-up/down converter).

In steady state, the average current circulating through C_1 ($\langle i_{C1} \rangle$) in a switching period is equal to zero, Eq. (3.23). Hence, the DC current transfer function given by Eq. (3.24) can be obtained from Fig 3.8c and Eq. (3.23).

$$\langle i_{C1} \rangle = \frac{1}{T_{sw}} \cdot \left(\int_0^{T_{on}} i_{C1}\, dt + \int_{T_{on}}^{T_{sw}} i_{C1}\, dt \right) = 0 \tag{3.23}$$

$$I_{out} = I_{in} \cdot \frac{(1-\delta)}{\delta} \tag{3.24}$$

where I_{in} and I_{out} are respectively the average input and output currents (cf. Fig 3.6).

The inductances of L_1 and L_2 are obtained from Fig 3.8a and Fig 3.8b respectively:

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L1}} \cdot \delta \cdot T_{sw} \tag{3.25}$$

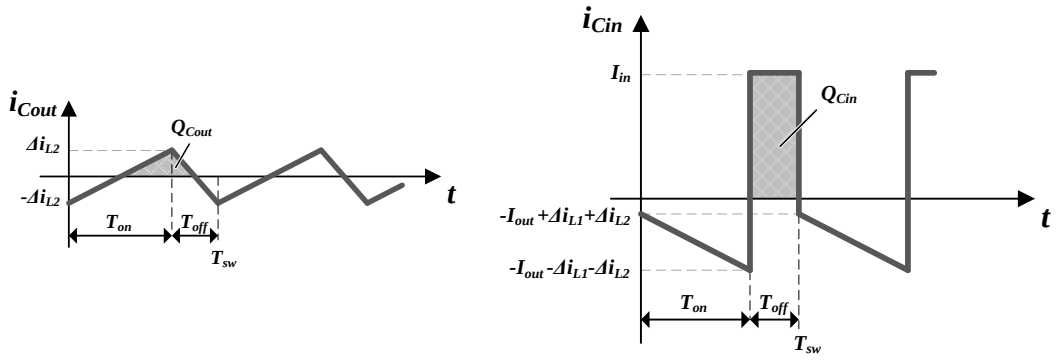
$$L_2 = v_{L2} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L2}} \cdot \delta \cdot T_{sw} \tag{3.26}$$

where Δi_{L1} and Δi_{L2} are the current ripple of L_1 and L_2 inductors respectively.

Similarly, the capacitance of C_1 is obtained from Fig 3.8c:

$$C_1 = i_{C1} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{C1}} \cdot \delta \cdot T_{sw} \tag{3.27}$$

where Δv_{C1} is the desired voltage ripple.



a) b)

Fig 3.9. Current circulating through a) the output capacitor and b) the input capacitor of the zeta converter.

As illustrated in Fig 3.9a, the current ripple of the inductor L_2 (Δi_{L2}) circulates through the output capacitor. Thus, the Q_{Cout} charges circulating through C_{out} can be trigonometrically calculated and therefore, the capacitance of C_{out} is given by :

$$C_{out} = \frac{Q_{Cout}}{\Delta v} = \frac{\Delta i_{L2}}{8 \cdot \Delta v_{Cout}} \cdot T_{sw} \tag{3.28}$$

where Δv_{Cout} is the half of the desired peak to peak output voltage ripple.

The current through the input capacitor (C_{in}) when the transistor S_1 is opened (T_{off} time interval) is equal to the input current (I_{in}). Assuming the input current is constant, the current circulating through the input capacitor can be drawn as in Fig 3.9b. Therefore, the input C_{in} capacitance is calculated from the Q_{Cin} charges depicted in Fig 3.9b and the desired input voltage ripple Δv_{Cin}:

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{I_{in}}{2 \cdot \Delta v_{Cin}} \cdot (1-\delta) \cdot T_{sw} \tag{3.29}$$

From Fig 3.8 and Fig 3.9, the *rms* current circulating through the passive elements (thermal stress), their maximum voltage stress (voltage rating) and the energy they store (image of their volume) are obtained. Table 3.3 summarizes aforementioned expressions.

TABLE 3.3

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2} \cdot C_{in} \cdot (V_{in} + \Delta v_{Cin})^2$	$\sqrt{I_{in}^2 \cdot (1-\delta) + \delta \cdot \left(I_{out}^2 + \frac{(\Delta i_{L1} + \Delta i_{L2})^2}{3} \right)}$	$(V_{in} + \Delta v_{Cin})$
L_1	$\frac{1}{2} \cdot L_1 \cdot (I_{in} + \Delta i_{L1})^2$	$\sqrt{I_{in}^2 + \frac{\Delta i_{L1}^2}{3}}$	$(V_{out} + \Delta v_{C1})$
C_1	$\frac{1}{2} \cdot C_1 \cdot (V_{out} + \Delta v_{C1})^2$	$\sqrt{\delta \cdot I_{out}^2 + (1-\delta) \cdot I_{in}^2}$	$(V_{out} + \Delta v_{C1})$
L_2	$\frac{1}{2} \cdot L_2 \cdot (I_{out} + \Delta i_{L2})^2$	$\sqrt{I_{out}^2 + \frac{\Delta i_{L2}^2}{3}}$	$(V_{out} + \Delta v_{Cout})$
C_{out}	$\frac{1}{2} \cdot C_{out} \cdot (V_{out} + \Delta v_{Cout})^2$	$\frac{\Delta i_{L2}}{\sqrt{3}}$	$(V_{out} + \Delta v_{Cout})$

Finally, from the maximum voltages (v_{max}) and the *rms* currents (I_{rms}) shown in Table 3.4, the semiconductor utilization factor is calculated as follows:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{(1-\delta) \cdot \delta}{\sqrt{\delta} + \sqrt{1-\delta}} \tag{3.30}$$

Fig 3.10 illustrates the Eq. (3.30) for different duty cycle values. As noticed, the maximum utilization factor is obtained when the duty cycle is equal to 0.5. Hence, from the DC voltage transfer function of Eq. (3.22), it is concluded that the converter is optimally designed when it operates with an input voltage equal to the output voltage.

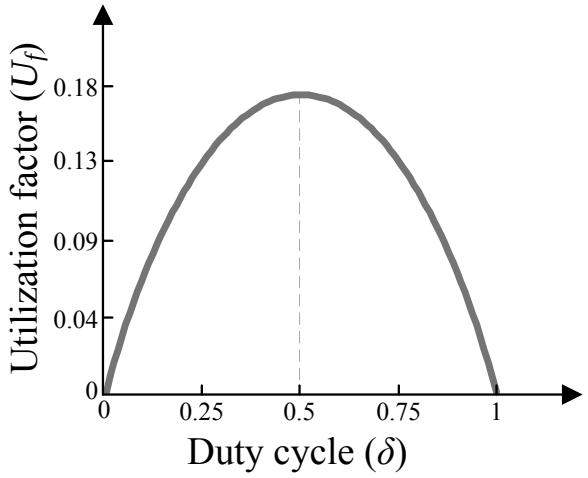


Fig 3.10. Semiconductor utilization factor of the zeta converter.

2.2.2.2 Power losses estimation

The semiconductors of zeta converter conduct the sum of the input current and the output current (greyish areas of Fig 3.8a and Fig 3.8b). Thus, from Fig 3.8a and Fig 3.8b, the currents and voltages in the semiconductors required for the power loss estimation are obtained and summarized in Table 3.4.

Average conduction power losses of S_1 and D_1 are expressed respectively as:

$$P_{cond\_S1} = V_{th} \cdot I_{in} + r_d \cdot \left(\frac{{I_{in}}^2}{\delta} + \delta \cdot \frac{\left(\Delta i_{L1} + \Delta i_{L2}\right)^2}{3} \right) \tag{3.31}$$

$$P_{cond\_D1} = V_{th} \cdot I_{out} + r_d \cdot \left(1-\delta\right) \cdot \left(\left(\frac{I_{in}}{\delta} \right)^2 + \frac{\left(\Delta i_{L1} + \Delta i_{L2}\right)^2}{3} \right) \tag{3.32}$$

where r_d is the semiconductor switch on-state resistance and V_{th} is the semiconductor threshold voltage.

Additionally, the average switching power losses of D_1 are given by:

$$P_{sw\_D1} = \frac{\left(\frac{V_{in}}{\left(1-\delta\right)} + \Delta v_{Cin} + \Delta v_{C1} \right)}{T_{sw} \cdot V_{100FIT}} \cdot \begin{pmatrix} A_{off,D1} \cdot \left(I_{in} + I_{out} - \Delta i_{L1} - \Delta i_{L2}\right)^2 + \\ + B_{off,D1} \cdot \left(I_{in} + I_{out} - \Delta i_{L1} - \Delta i_{L2}\right) + C_{off,D1} \end{pmatrix} \tag{3.33}$$

where $A_{off,D1}$, $B_{off,D1}$ and $C_{off,D1}$ are the turn-off energy loss characteristic provided by the manufacturer for the 100FIT test voltage (V_{100FIT}).

TABLE 3.4
EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistor S_1**	**Diode D_1**
Average current (I_{ave})	I_{in}	I_{out}
rms current (I_{rms})	$\sqrt{\frac{I_{in}^{\,2}}{\delta}+\delta\cdot\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{3}}$	$\sqrt{(1-\delta)\cdot\left(\left(\frac{I_{in}}{\delta}\right)^2+\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{3}\right)}$
Maximum current (i_{max})	$(I_{in}+I_{out}+\Delta i_{L1}+\Delta i_{L2})$	$(I_{in}+I_{out}+\Delta i_{L1}+\Delta i_{L2})$
Turn-on switched current (i_{on})	$(I_{in}+I_{out}-\Delta i_{L1}-\Delta i_{L2})$	—
Turn-off switched current (i_{off})	$(I_{in}+I_{out}+\Delta i_{L1}+\Delta i_{L2})$	$(I_{in}+I_{out}-\Delta i_{L1}-\Delta i_{L2})$
Maximum voltage (v_{max})	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{Cin}\right)$	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{Cin}\right)$
Turn-on switched voltage (v_{on})	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{Cin}\right)$	—
Turn-off switched voltage (v_{off})	$\left(\frac{V_{in}}{(1-\delta)}-\Delta v_{C1}-\Delta v_{Cin}\right)$	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{Cin}\right)$

The average switching losses of S_1 are:

$$P_{sw\_S1}=\frac{\left(\frac{V_{in}}{(1-\delta)}-\Delta v_{C1}-\Delta v_{Cin}\right)}{T_{sw}\cdot V_{100FIT}}\cdot\begin{pmatrix}A_{off,S1}\cdot(I_{in}+I_{out}+\Delta i_{L1}+\Delta i_{L2})^2+\\+B_{off,S1}\cdot(I_{in}+I_{out}+\Delta i_{L1}+\Delta i_{L2})+C_{off,S1}\end{pmatrix}+$$
$$+\frac{\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{Cin}\right)}{T_{sw}\cdot V_{100FIT}}\cdot\begin{pmatrix}A_{on,S1}\cdot(I_{in}+I_{out}-\Delta i_{L1}-\Delta i_{L2})^2+\\+B_{on,S1}\cdot(I_{in}+I_{out}-\Delta i_{L1}-\Delta i_{L2})+C_{on,S1}\end{pmatrix} \quad (3.34)$$

where $A_{off,S1}$, $B_{off,S1}$ and $C_{off,S1}$ are the turn-off energy loss characteristic provided by the manufacturer for V_{100FIT}. Similarly, $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are the turn-on energy loss characteristic.

2.2.3 Sepic

In Fig 3.11 the sepic converter is depicted. It is a unidirectional step-up/down converter with no galvanic isolation. The converter comprises two inductors and three capacitors. Moreover, two semiconductors are required, a transistor and a diode.

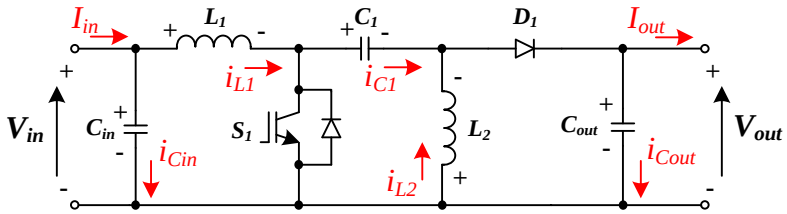
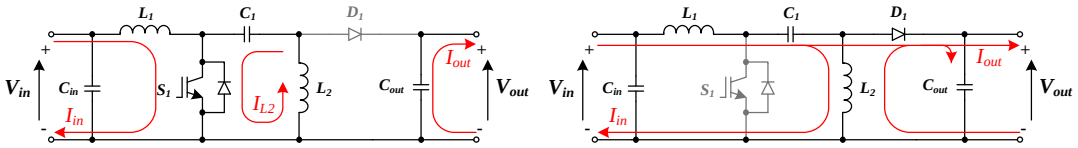


Fig 3.11. Sepic converter.

2.2.3.1 Converter design

In Fig 3.12a, when the transistor S_1 is on (T_{on} time interval), the energy coming from the input is stored in the inductor L_1. At the same time, the energy stored in capacitor C_1 is transferred to L_2 and the load is supplied by the output capacitor C_{out}. During the off-state of S_1 (T_{off} time interval), the energy coming from the input and the energy stored in L_1 are transferred to C_1 and C_{out} (Fig 3.12b). In addition, L_2 supplies the output load.



a) b)

Fig 3.12. Currents circulating through the sepic converter a) when S_1 is on and b) when S_1 is off.

As a consequence, the steady state voltages and currents in L_1, L_2, C_1 and C_{out} are drawn respectively as in Fig 3.13a, Fig 3.13b, Fig 3.13c and Fig 3.13d if a CCM operation is assumed.

As discussed for previous converters, the DC voltage/current transfer functions are obtained from the analysis of the voltage/current waveforms in the passive elements. On the one hand, the average voltage drop in the inductors L_1 and L_2 is zero. Therefore, from Fig 3.13a and Eq. (3.17), Eq. (3.35) is obtained. Similarly, from Fig 3.13b and Eq. (3.18), Eq. (3.36) is obtained.

$$V_{in} = \left(V_{out} + V_{C1}\right) \cdot \left(1 - \delta\right) \tag{3.35}$$

$$V_{out} = V_{C1} \cdot \frac{\delta}{\left(1 - \delta\right)} \tag{3.36}$$

where δ is the duty cycle of the converter (T_{on}/T_{sw}), V_{in} and V_{out} are the average input and output voltages respectively (cf. Fig 3.11) and V_{C1} is the average voltage of C_1.

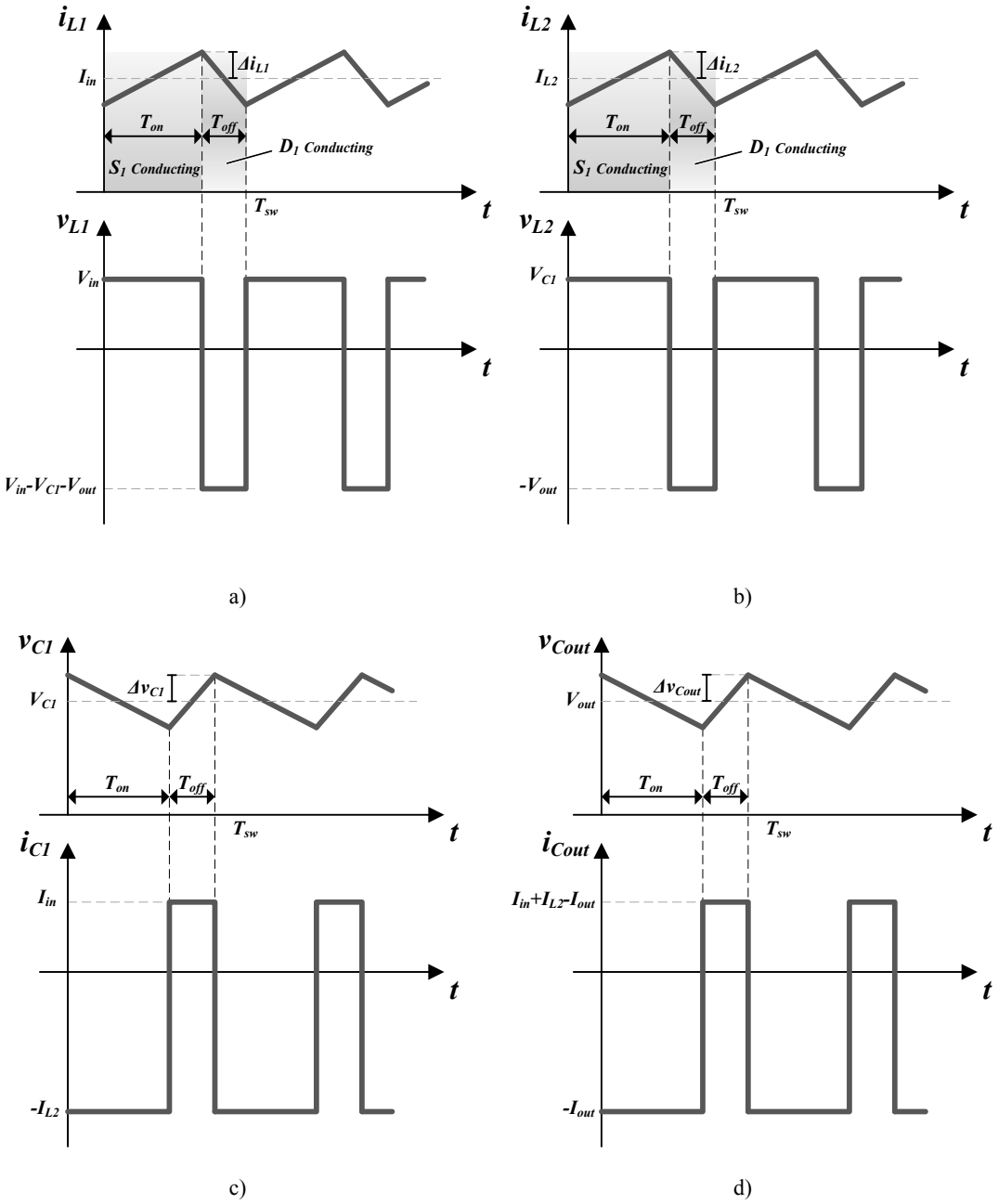


Fig 3.13. Typical voltage and current waveforms in sepic converter's a) inductor L_1, b) inductor L_2, c) capacitor C_1 and d) capacitor C_{out}.

The average voltage of C_1 is obtained introducing Eq. (3.36) into Eq. (3.35):

$$V_{C1} = V_{in} \tag{3.37}$$

Thus, the DC voltage transfer function is obtained introducing Eq. (3.37) into Eq. (3.36):

$$V_{out} = V_{in} \cdot \frac{\delta}{(1-\delta)} \tag{3.38}$$

From Eq. (3.38), if the duty cycle is lower than 0.5, V_{out} is greater than V_{in}. Conversely, if the duty cycle is higher than 0.5, V_{out} is lower than V_{in}. Thus, sepic converter is considered a step-up/down converter.

On the other hand, the current expressions given by Eq. (3.39) and Eq. (3.40) are obtained respectively from Fig 3.13c and Fig 3.13d considering the average current circulating through C_1 in a switching period is equal to zero:

$$I_{in} = I_{L2} \cdot \frac{\delta}{(1-\delta)} \tag{3.39}$$

$$I_{out} = (I_{in} + I_{L2}) \cdot (1-\delta) \tag{3.40}$$

where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.11) and I_{L2} is the average current circulating through L_2. Introducing Eq. (3.39) into Eq. (3.40) the average current circulating through L_2 is equal to the output current:

$$I_{L2} = I_{out} \tag{3.41}$$

From Eq. (3.39) and Eq. (3.41), the DC current transfer function is given as follows:

$$I_{out} = I_{in} \cdot \frac{(1-\delta)}{\delta} \tag{3.42}$$

The inductance values of L_1 and L_2 are obtained from the analysis of the voltage and currents of Fig 3.13a and Fig 3.13b during T_{on} time interval:

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L1}} \cdot \delta \cdot T_{sw} \tag{3.43}$$

$$L_2 = v_{L2} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L2}} \cdot \delta \cdot T_{sw} \tag{3.44}$$

where Δi_{L1} and Δi_{L2} are respectively the ripple of the currents circulating through L_1 and L_2.

Similarly, C_1 and C_{out} capacitances are obtained from Fig 3.13c and Fig 3.13d:

$$C_1 = i_{C1} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{C1}} \cdot \delta \cdot T_{sw} \tag{3.45}$$

$$C_{out} = i_{Cout} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{Cout}} \cdot \delta \cdot T_{sw} \tag{3.46}$$

where Δv_{Cout} and Δv_{C1} are respectively the desired voltage ripple in the output and C_1 capacitors.

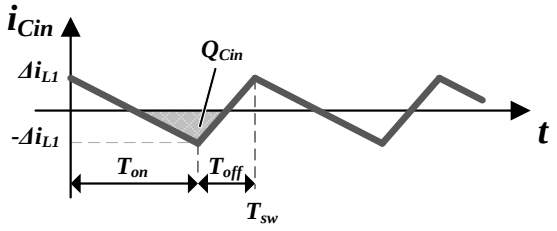


Fig 3.14. Current circulating through the input capacitor of the sepic converter.

In order to calculate the input DC bus capacitance, the current coming from the input is considered constant (I_{in}). As a consequence, the current circulating through C_{in} is equal to the current ripple Δi_{L1} and therefore, the Q_{Cin} charges circulating through the input capacitor can be trigonometrically calculated from Fig 3.14. So, the capacitance of C_{in} is given by:

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{\Delta i_{L1}}{8 \cdot \Delta v_{Cin}} \cdot T_{sw} \tag{3.47}$$

where Δv_{Cin} is the half of the desired peak to peak input voltage ripple.

Table 3.5 summarizes the expressions of the *rms* current circulating through the passive elements, their maximum voltage and the energy they store. The expressions are obtained from Fig 3.13 and Fig 3.14.

TABLE 3.5

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2} \cdot C_{in} \cdot (V_{in} + \Delta v_{Cin})^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$(V_{in} + \Delta v_{Cin})$
L_1	$\frac{1}{2} \cdot L_1 \cdot (I_{in} + \Delta i_{L1})^2$	$\sqrt{I_{in}^2 + \frac{\Delta i_{L1}^2}{3}}$	$\approx (V_{out} + \Delta v_{Cout} + \Delta v_{C1})$
C_1	$\frac{1}{2} \cdot C_1 \cdot (V_{in} + \Delta v_{C1})^2$	$I_{in} \cdot \sqrt{\frac{(1-\delta)}{\delta}}$	$(V_{in} + \Delta v_{C1})$
L_2	$\frac{1}{2} \cdot L_2 \cdot (I_{out} + \Delta i_{L2})^2$	$\sqrt{I_{out}^2 + \frac{\Delta i_{L2}^2}{3}}$	$(V_{out} + \Delta v_{Cout})$
C_{out}	$\frac{1}{2} \cdot C_{out} \cdot (V_{out} + \Delta v_{Cout})^2$	$I_{out} \cdot \sqrt{\frac{\delta}{(1-\delta)}}$	$(V_{out} + \Delta v_{Cout})$

The semiconductor utilization factor is given as:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{(1-\delta) \cdot \delta}{\sqrt{\delta} + \sqrt{1-\delta}} \tag{3.48}$$

As this semiconductor utilization factor is equal to that presented in Eq. (3.30) and Fig 3.10 for zeta converter, same conclusions are obtained. The maximum utilization factor and in consequence, its optimal design, is given by an operation with a duty cycle value of 0.5. In other words, if the input voltage is equal to the output voltage, the semiconductor utilization factor is optimum.

2.2.3.2 Power losses estimation

For the semiconductor power loss estimation, the currents and voltages in the semiconductors must be obtained. As the semiconductors conduct the input as well as the output current, the expressions are obtained from the sum of the currents depicted in Fig 3.13a and Fig 3.13b. Table 3.6 summarizes the current and voltage expressions required for the power loss estimation.

TABLE 3.6
EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistor S_1**	**Diode D_1**
Average current (I_{ave})	I_{in}	I_{out}
rms current (I_{rms})	$\sqrt{\frac{{I_{in}}^2}{\delta}+\delta\cdot\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{3}}$	$\sqrt{(1-\delta)\cdot\left(\left(\frac{I_{in}}{\delta}\right)^2+\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{3}\right)}$
Maximum current (i_{max})	$(I_{in}+I_{out}+\Delta i_{L1}+\Delta i_{L2})$	$(I_{in}+I_{out}+\Delta i_{L1}+\Delta i_{L2})$
Turn-on switched current (i_{on})	$(I_{in}+I_{out}-\Delta i_{L1}-\Delta i_{L2})$	—
Turn-off switched current (i_{off})	$(I_{in}+I_{out}+\Delta i_{L1}+\Delta i_{L2})$	$(I_{in}+I_{out}-\Delta i_{L1}-\Delta i_{L2})$
Maximum voltage (v_{max})	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{Cout}\right)$	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{Cout}\right)$
Turn-on switched voltage (v_{on})	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{Cout}\right)$	—
Turn-off switched voltage (v_{off})	$\left(\frac{V_{in}}{(1-\delta)}-\Delta v_{C1}-\Delta v_{Cout}\right)$	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{Cout}\right)$

Therefore, average conduction power losses of S_1 and D_1 are given respectively as:

$$P_{cond\_S1}=V_{th}\cdot I_{in}+r_d\cdot\left(\frac{{I_{in}}^2}{\delta}+\delta\cdot\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{3}\right) \tag{3.49}$$

$$P_{cond\_D1}=V_{th}\cdot I_{out}+r_d\cdot(1-\delta)\cdot\left(\left(\frac{I_{in}}{\delta}\right)^2+\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{3}\right) \tag{3.50}$$

where r_d is the semiconductor switch on-state resistance and V_{th} is the semiconductor threshold voltage.

Additionally, the average switching power losses of D_1 are expressed as:

$$P_{sw\_D1}=\frac{\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{Cout}\right)}{T_{sw}\cdot V_{100FIT}}\cdot\begin{pmatrix}A_{off,D1}\cdot(I_{in}+I_{out}-\Delta i_{L1}-\Delta i_{L2})^2+\\+B_{off,D1}\cdot(I_{in}+I_{out}-\Delta i_{L1}-\Delta i_{L2})+C_{off,D1}\end{pmatrix} \tag{3.51}$$

where $A_{off,D1}$, $B_{off,D1}$ and $C_{off,D1}$ are the turn-off energy loss characteristic provided by the manufacturer for the 100FIT test voltage (V_{100FIT}).

Finally, the average switching losses of S_1 are obtained as below:

$$P_{sw\_S1} = \frac{\left(\frac{V_{in}}{(1-\delta)} - \Delta v_{C1} - \Delta v_{Cout}\right)}{T_{sw} \cdot V_{100FIT}} \cdot \begin{pmatrix} A_{off,S1} \cdot (I_{in} + I_{out} + \Delta i_{L1} + \Delta i_{L2})^2 + \\ + B_{off,S1} \cdot (I_{in} + I_{out} + \Delta i_{L1} + \Delta i_{L2}) + C_{off,S1} \end{pmatrix} + \\ + \frac{\left(\frac{V_{in}}{(1-\delta)} + \Delta v_{C1} + \Delta v_{Cout}\right)}{T_{sw} \cdot V_{100FIT}} \cdot \begin{pmatrix} A_{on,S1} \cdot (I_{in} + I_{out} - \Delta i_{L1} - \Delta i_{L2})^2 + \\ + B_{on,S1} \cdot (I_{in} + I_{out} - \Delta i_{L1} - \Delta i_{L2}) + C_{on,S1} \end{pmatrix} \quad (3.52)$$

where $A_{off,S1}$, $B_{off,S1}$ and $C_{off,S1}$ are the turn-off energy loss characteristic provided by the manufacturer for V_{100FIT} and $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are the turn-on energy loss characteristic.

2.2.4 Isolated-sepic

If the output side inductor (L_2) of the sepic converter is substituted by a medium frequency transformer, the isolated-sepic converter is obtained, cf. Fig 3.15. The power transference in this step-up/down converter is unidirectional. The leakage inductance of the MFT has been neglected in the analysis presented hereafter.

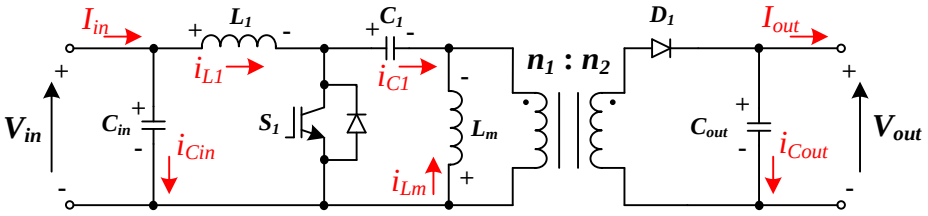


Fig 3.15. Isolated-sepic converter.

2.2.4.1 Converter design

When transistor S_1 is on (T_{on} time interval), the energy coming from the input is stored in L_1 inductor while the energy stored in the capacitor C_1 is transferred to the magnetizing inductance of the transformer (L_m). Additionally, Fig 3.16a shows that during this time interval, the output capacitor C_{out} supplies the output load. When S_1 is off (T_{off} time interval), the energy coming from the input and the energy stored in L_1 are transferred to C_1 and C_{out} as illustrated in Fig 3.16b. At the same time, L_m supplies the output load.

Assuming a CCM operation, Fig 3.17 illustrates the steady state voltage and current waveforms in the passive elements of the converter. From the voltage waveforms depicted in Fig 3.17a and Fig 3.17b, the voltage relations of the converter are obtained:

$$V_{in} = \left(V_{out} \cdot \frac{n_1}{n_2} + V_{C1}\right) \cdot (1-\delta) \quad (3.53)$$

$$V_{out} = V_{C1} \cdot \frac{\delta}{(1-\delta)} \cdot \frac{n_2}{n_1} \tag{3.54}$$

where n_1 and n_2 are respectively primary and secondary windings' number of turns, δ is the duty cycle of the converter (T_{on}/T_{sw}), V_{in} and V_{out} are the average input and output voltages respectively (cf. Fig 3.15) and V_{C1} is the mean voltage value of C_1.

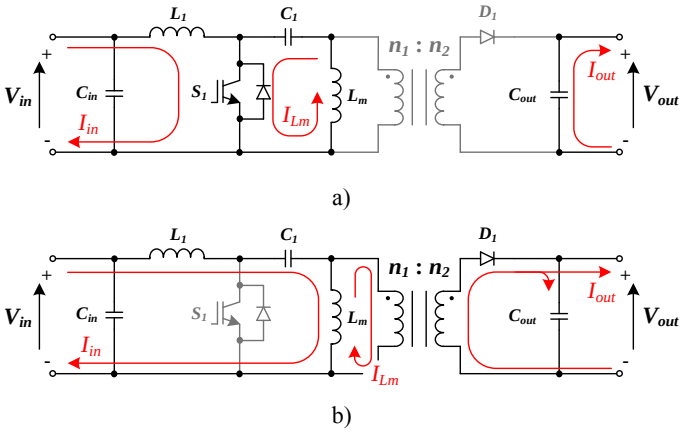


Fig 3.16. Currents circulating through the isolated-sepic converter a) when S_1 is on and b) when S_1 is off.

From the voltage relations of Eq. (3.53) and Eq. (3.54), the average voltage of C_1 is equal to the input voltage:

$$V_{C1} = V_{in} \tag{3.55}$$

Hence, the DC voltage transfer function is obtained rewriting Eq. (3.54):

$$V_{out} = V_{in} \cdot \frac{\delta}{(1-\delta)} \cdot \frac{n_2}{n_1} \tag{3.56}$$

The DC voltage transfer function of the previously discussed step-up/down converters depends only on the duty cycle, while that of the isolated-sepic depends also on the turn ratio of the MFT. This fact adds a degree of freedom for the design of the isolated-sepic (the voltage elevation can be fixed by the transformer or by the duty cycle).

The relations between the currents in the converter are obtained from the steady state analysis of the waveforms of Fig 3.17c and Fig 3.17d:

$$I_{in} = I_{Lm} \cdot \frac{\delta}{(1-\delta)} \tag{3.57}$$

$$I_{out} = (I_{in} + I_{Lm}) \cdot (1-\delta) \cdot \frac{n_1}{n_2} \tag{3.58}$$

where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.15) and I_{Lm} is the average current circulating through L_m.

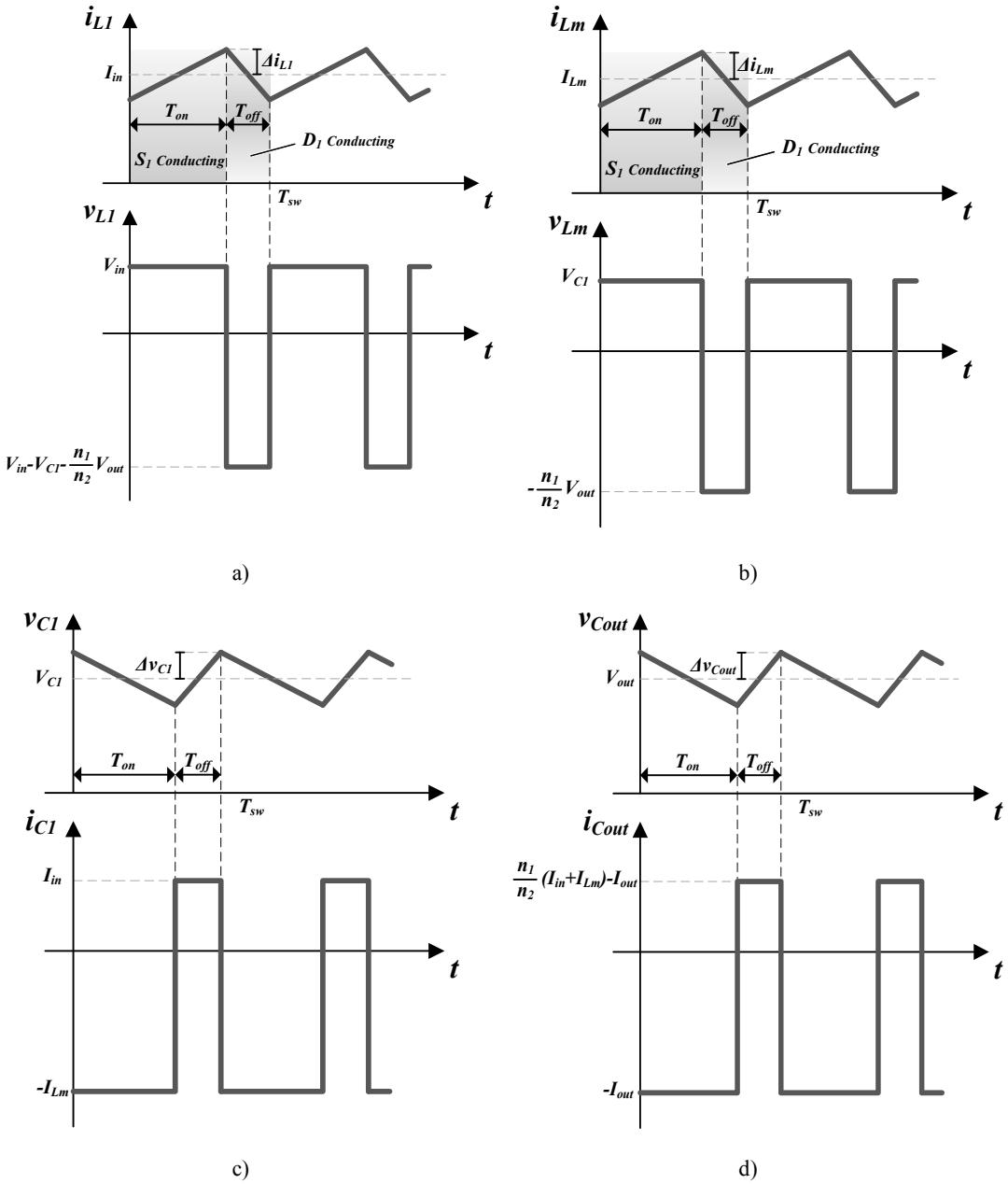


Fig 3.17. Typical voltage and current waveforms in isolated-sepic converter's a) inductor L_1, b) magnetizing inductance L_m, c) capacitor C_1 and d) output capacitor C_{out}.

Introducing Eq. (3.57) into Eq. (3.58) the average current circulating through L_m is obtained:

$$I_{Lm} = I_{out} \cdot \frac{n_2}{n_1} \tag{3.59}$$

From Fig 3.17b and Eq. (3.59), the magnetization of the MFT is unidirectional leading to a poor utilization of the transformer.

The transfer function of the DC current is obtained introducing Eq. (3.59) into Eq. (3.57):

$$I_{out} = I_{in} \cdot \frac{(1-\delta)}{\delta} \cdot \frac{n_1}{n_2} \tag{3.60}$$

Furthermore, the values of L_1 and L_m are obtained from the analysis of the waveforms of Fig 3.17a and Fig 3.17b during T_{on} time interval:

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L1}} \cdot \delta \cdot T_{sw} \tag{3.61}$$

$$L_m = v_{Lm} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{Lm}} \cdot \delta \cdot T_{sw} \tag{3.62}$$

where Δi_{L1} and Δi_{Lm} are respectively the current ripple in L_1 and L_m.

Similarly, the capacitive values of C_1 and C_{out} are obtained from Fig 3.17c and Fig 3.17d:

$$C_1 = i_{C1} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{C1}} \cdot \frac{n_2}{n_1} \cdot \delta \cdot T_{sw} \tag{3.63}$$

$$C_{out} = i_{Cout} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{Cout}} \cdot \delta \cdot T_{sw} \tag{3.64}$$

where Δv_{Cout} and Δv_{C1} are the desired voltage ripple in C_{out} and C_1 capacitors.

The input DC bus capacitance is calculated following the same criterion than for the sepic converter (assuming a constant input current I_{in}, Fig 3.14). Hence, it is given as:

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{\Delta i_{L1}}{8 \cdot \Delta v_{Cin}} \cdot T_{sw} \tag{3.65}$$

where Q_{Cin} are the charges circulating through the input capacitor and Δv_{Cin} is the half of the desired peak to peak input voltage ripple.

From Fig 3.17, Table 3.7 summarizes the expressions of the *rms* current circulating through passive elements, their maximum voltage stress and the energy they store.

Comparing Table 3.7 and Table 3.5, it can be observed that the voltage stress of the inductances of isolated-sepic converter is smaller than that of the inductances of the sepic converter if $n_2 > n_1$ is considered. However, the semiconductor utilization factor is equal for both converters:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{(1-\delta) \cdot \delta}{\sqrt{\delta} + \sqrt{1-\delta}} \tag{3.66}$$

Thus, similarly to zeta and sepic converters, the maximum utilization factor is given by a duty cycle value of 0.5 (Fig 3.10). Hence, the converter must be designed to operate with duty cycles close to 0.5 (optimal n_2/n_1 turn ratio must be chosen for each application, Eq. (3.56)).

TABLE 3.7

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2}\cdot C_{in}\cdot\left(V_{in}+\Delta v_{Cin}\right)^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$\left(V_{in}+\Delta v_{Cin}\right)$
L_1	$\frac{1}{2}\cdot L_1\cdot\left(I_{in}+\Delta i_{L1}\right)^2$	$\sqrt{{I_{in}}^2+\frac{{\Delta i_{L1}}^2}{3}}$	$\left(V_{out}+\Delta v_{Cout}\right)\cdot\frac{n_1}{n_2}$
C_1	$\frac{1}{2}\cdot C_1\cdot\left(V_{in}+\Delta v_{C1}\right)^2$	$I_{in}\cdot\sqrt{\frac{(1-\delta)}{\delta}}$	$\left(V_{in}+\Delta v_{C1}\right)$
L_m	$\frac{1}{2}\cdot L_m\cdot\left(I_{out}\cdot\frac{n_2}{n_1}+\Delta i_{Lm}\right)^2$	$\sqrt{\left(\frac{n_2}{n_1}\cdot I_{out}\right)^2+\frac{{\Delta i_{Lm}}^2}{3}}$	$\left(V_{out}+\Delta v_{Cout}\right)\cdot\frac{n_1}{n_2}$
C_{out}	$\frac{1}{2}\cdot C_{out}\cdot\left(V_{out}+\Delta v_{Cout}\right)^2$	$I_{out}\cdot\sqrt{\frac{\delta}{(1-\delta)}}$	$\left(V_{out}+\Delta v_{Cout}\right)$

2.2.4.2 Power losses estimation

The semiconductors of the isolated-sepic converter conduct the sum of the input and output currents as depicted in Fig 3.17a and Fig 3.17b. Therefore, from those figures, the currents circulating through S_1 and D_1, and their voltage drop are calculated and summarized in Table 3.8.

The average conduction power losses of S_1 and D_1 are obtained from Table 3.8 and Eq. (3.1):

$$P_{cond\_S1}=V_{th}\cdot I_{in}+r_d\cdot\left(\frac{{I_{in}}^2}{\delta}+\delta\cdot\frac{\left(\Delta i_{L1}+\Delta i_{Lm}\right)^2}{3}\right) \tag{3.67}$$

$$P_{cond\_D1}=V_{th}\cdot I_{out}+r_d\cdot(1-\delta)\cdot\left(\frac{n_1}{n_2}\right)^2\cdot\left(\left(\frac{I_{in}}{\delta}\right)^2+\frac{\left(\Delta i_{L1}+\Delta i_{Lm}\right)^2}{3}\right) \tag{3.68}$$

where r_d is the semiconductor switch on-state resistance and V_{th} is the semiconductor threshold voltage.

TABLE 3.8
EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistor S_1**	**Diode D_1**
Average current (I_{ave})	I_{in}	I_{out}
rms current (I_{rms})	$\sqrt{\frac{I_{in}^{\,2}}{\delta}+\delta\cdot\frac{(\Delta i_{L1}+\Delta i_{Lm})^2}{3}}$	$\sqrt{(1-\delta)\cdot\left(\frac{n_1}{n_2}\right)^2\cdot\left(\left(\frac{I_{in}}{\delta}\right)^2+\frac{(\Delta i_{L1}+\Delta i_{Lm})^2}{3}\right)}$
Maximum current (i_{max})	$\left(I_{in}+I_{out}\cdot\frac{n_2}{n_1}+\Delta i_{L1}+\Delta i_{Lm}\right)$	$\left((I_{in}+\Delta i_{L1}+\Delta i_{Lm})\cdot\frac{n_1}{n_2}+I_{out}\right)$
Turn-on switched current (i_{on})	$\left(I_{in}+I_{out}\cdot\frac{n_2}{n_1}-\Delta i_{L1}-\Delta i_{Lm}\right)$	—
Turn-off switched current (i_{off})	$\left(I_{in}+I_{out}\cdot\frac{n_2}{n_1}+\Delta i_{L1}+\Delta i_{Lm}\right)$	$\left((I_{in}-\Delta i_{L1}-\Delta i_{Lm})\cdot\frac{n_1}{n_2}+I_{out}\right)$
Maximum voltage (v_{max})	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\frac{n_1}{n_2}\cdot\Delta v_{Cout}\right)$	$\left(\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}\right)\cdot\frac{n_2}{n_1}+\Delta v_{Cout}\right)$
Turn-on switched voltage (v_{on})	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\frac{n_1}{n_2}\cdot\Delta v_{Cout}\right)$	—
Turn-off switched voltage (v_{off})	$\left(\frac{V_{in}}{(1-\delta)}-\Delta v_{C1}-\frac{n_1}{n_2}\cdot\Delta v_{Cout}\right)$	$\left(\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}\right)\cdot\frac{n_2}{n_1}+\Delta v_{Cout}\right)$

From the currents and voltages given by Table 3.8 and Eq. (3.2), the average switching power losses of D_1 are calculated:

$$P_{sw\_D1}=\frac{\left(\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}\right)\cdot\frac{n_2}{n_1}+\Delta v_{Cout}\right)}{T_{sw}\cdot V_{100FIT}}\cdot A_{off,D1}\cdot\left((I_{in}-\Delta i_{L1}-\Delta i_{Lm})\cdot\frac{n_1}{n_2}+I_{out}\right)^2+$$
$$+\frac{\left(\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}\right)\cdot\frac{n_2}{n_1}+\Delta v_{Cout}\right)}{T_{sw}\cdot V_{100FIT}}\cdot\left(\begin{array}{l}B_{off,D1}\cdot\left((I_{in}-\Delta i_{L1}-\Delta i_{Lm})\cdot\frac{n_1}{n_2}+I_{out}\right)+\\+C_{off,D1}\end{array}\right) \tag{3.69}$$

where $A_{off,D1}$, $B_{off,D1}$ and $C_{off,D1}$ are the turn-off energy loss characteristic provided by the manufacturer for the 100FIT test voltage (V_{100FIT}).

Moreover, the average switching losses of S_1 are obtained as below:

$$P_{sw\_S1} = \frac{\left(\frac{V_{in}}{(1-\delta)} - \Delta v_{C1} - \frac{n_1}{n_2}\cdot\Delta v_{Cout}\right)}{T_{sw}\cdot V_{100FIT}}\cdot A_{off,S1}\cdot\left(I_{in} + I_{out}\cdot\frac{n_2}{n_1} + \Delta i_{L1} + \Delta i_{Lm}\right)^2 +$$
$$+\frac{\left(\frac{V_{in}}{(1-\delta)} - \Delta v_{C1} - \frac{n_1}{n_2}\cdot\Delta v_{Cout}\right)}{T_{sw}\cdot V_{100FIT}}\cdot\left(B_{off,S1}\cdot\left(I_{in} + I_{out}\cdot\frac{n_2}{n_1} + \Delta i_{L1} + \Delta i_{Lm}\right) + C_{off,S1}\right) +$$
$$+\frac{\left(\frac{V_{in}}{(1-\delta)} + \Delta v_{C1} + \frac{n_1}{n_2}\cdot\Delta v_{Cout}\right)}{T_{sw}\cdot V_{100FIT}}\cdot A_{on,S1}\cdot\left(I_{in} + I_{out}\cdot\frac{n_2}{n_1} - \Delta i_{L1} - \Delta i_{Lm}\right)^2 + \tag{3.70}$$
$$+\frac{\left(\frac{V_{in}}{(1-\delta)} + \Delta v_{C1} + \frac{n_1}{n_2}\cdot\Delta v_{Cout}\right)}{T_{sw}\cdot V_{100FIT}}\cdot\left(B_{on,S1}\cdot\left(I_{in} + I_{out}\cdot\frac{n_2}{n_1} - \Delta i_{L1} - \Delta i_{Lm}\right) + C_{on,S1}\right)$$

where $A_{off,S1}$, $B_{off,S1}$ and $C_{off,S1}$ are the turn-off energy loss characteristic provided by the manufacturer for V_{100FIT} and $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are the turn-on energy loss characteristic.

Finally, comparing Table 3.6 to Table 3.8, it is noticed that considering n_2 greater than n_1, the voltages switched by S_1 in the isolated-sepic converter are slightly smaller than that in the sepic converter. Additionally, the diode of the isolated-sepic converter switches less current than the diode of the sepic converter. Conversely, the transistor S_1 of the latter switches less current than that transistor in the isolated-sepic converter.

2.2.5 Ćuk

The ćuk converter shown in Fig 3.18 is a unidirectional step-up/down converter with no galvanic isolation capability. The converter is composed of a transistor (S_1), a diode (D_1), two inductors (L_1, L_2) and three capacitors (C_{in}, C_1, C_{out}). As it can be observed, the polarities of the input and output voltages are inverted.

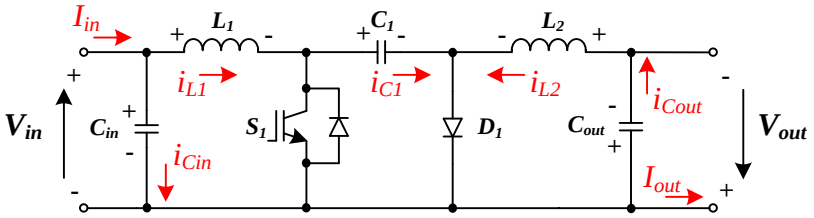


Fig 3.18. Ćuk converter.

2.2.5.1 Converter design

The converter operates transferring the energy coming from the input to L_1, C_1, L_2 and to the output. Thus, when transistor S_1 is on (T_{on} time interval), the energy coming from the

input is stored in the inductor L_1 while the energy stored in the capacitor C_1 is transferred to L_2 and the load (Fig 3.19a). As shown in Fig 3.19b, when S_1 is off (T_{off} time interval), the energy coming from the input and the energy stored in L_1 are transferred to C_1. The output load is supplied by the inductor L_2.

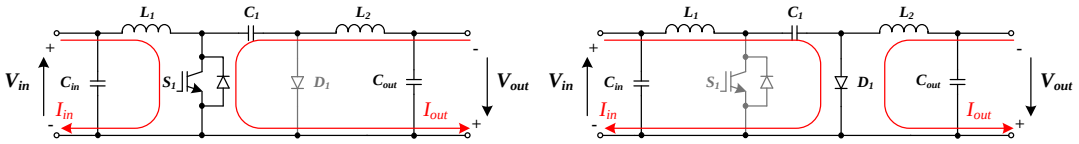


Fig 3.19. Currents circulating through the ćuk converter a) when S_1 is on and b) when S_1 is off.

Fig 3.20 shows the steady state voltage and current waveforms in L_1, L_2 and C_1 and C_{out} under a CCM operation. The voltage relations between the input, C_1 and the output are obtained from Fig 3.20a and Fig 3.20b assuming the average voltage drop in the inductors is zero (Eq. (3.17), Eq. (3.18)):

$$V_{in} = V_{C1} \cdot (1-\delta) \tag{3.71}$$

$$V_{out} = V_{C1} \cdot \delta \tag{3.72}$$

where δ is the duty cycle of the converter (T_{on}/T_{sw}), V_{in} and V_{out} are the average input and output voltages respectively (cf. Fig 3.18) and V_{C1} is the average voltage of C_1.

Thus, the DC voltage transfer function is obtained from above voltage relations:

$$V_{out} = V_{in} \cdot \frac{\delta}{(1-\delta)} \tag{3.73}$$

The step-up/down nature of the ćuk converter is observed in the DC transfer function equation, if δ is greater than *0.5*, V_{out} is greater than V_{in}, while if δ is lower than *0.5*, V_{out} is lower than V_{in}.

Introducing the DC voltage transfer function into Eq. (3.71), the average voltage of C_1 is:

$$V_{C1} = \frac{V_{in}}{(1-\delta)} = V_{in} + V_{out} \tag{3.74}$$

Similarly, the DC current transfer function is obtained from Fig 3.20c considering the average current circulating through C_1 is equal to zero (Eq. (3.23)):

$$I_{out} = I_{in} \cdot \frac{(1-\delta)}{\delta} \tag{3.75}$$

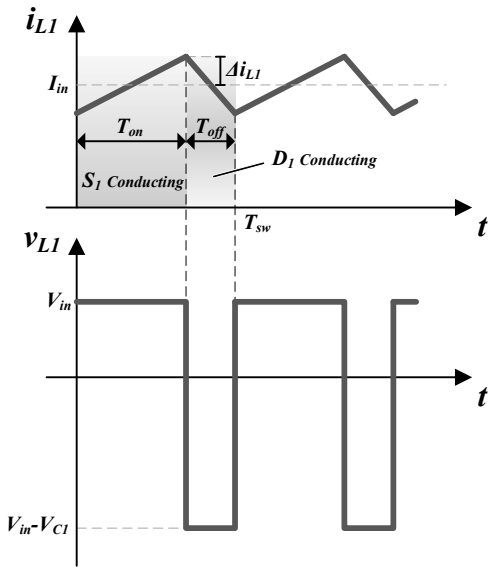
where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.18).

Moreover, from Fig 3.20a and Fig 3.20b, the expressions to calculate the inductances of L_1 and L_2 are obtained:

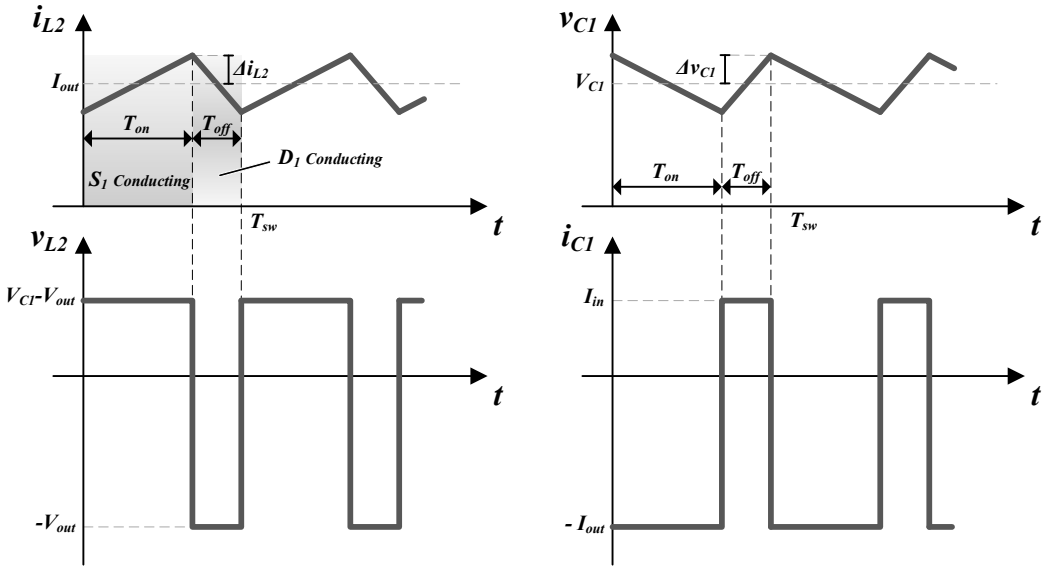
$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L1}} \cdot \delta \cdot T_{sw} \tag{3.76}$$

$$L_2 = v_{L2} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L2}} \cdot \delta \cdot T_{sw} \tag{3.77}$$

where Δi_{L1} is the current ripple through L_1 and Δi_{L2} is the current ripple through L_2.



a)



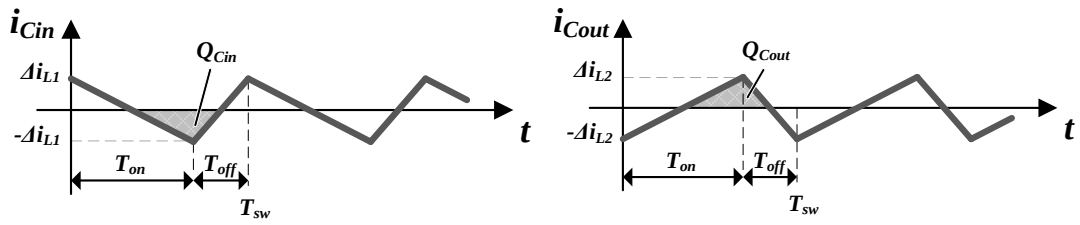
b) c)

Fig 3.20. Typical voltage and current waveforms in ćuk converter's a) inductor L_1, b) inductor L_2 and c) capacitor C_1.

The expression to calculate the capacitance of C_1 is obtained from Fig 3.20c:

$$C_1 = i_{C1} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{C1}} \cdot \delta \cdot T_{sw} \tag{3.78}$$

where Δv_{C1} is the desired voltage ripple in C_1.



a) b)

Fig 3.21. Currents circulating through a) the input capacitor and b) the output capacitor of the ćuk converter.

For calculating the capacitance values of C_{in} and C_{out}, the input current I_{in} and the output current I_{out} are assumed to be constant. Thus, the currents circulating through them can be drawn as in Fig 3.21. As a consequence, C_{in} and C_{out} capacitances are obtained by calculating the charges circulating through them (grey coloured in Fig 3.21a and Fig 3.21b):

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{\Delta i_{L1}}{8 \cdot \Delta v_{Cin}} \cdot T_{sw} \tag{3.79}$$

$$C_{out} = \frac{Q_{Cout}}{\Delta v} = \frac{\Delta i_{L2}}{8 \cdot \Delta v_{Cout}} \cdot T_{sw} \tag{3.80}$$

where Δv_{Cin} and Δv_{Cout} are the half of the desired peak to peak voltage ripple in the input capacitor and the output capacitor respectively.

In addition, from Fig 3.20 and Fig 3.21, Table 3.9 summarizes the main characteristics of the passive elements.

TABLE 3.9

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2} \cdot C_{in} \cdot (V_{in} + \Delta v_{Cin})^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$(V_{in} + \Delta v_{Cin})$
L_1	$\frac{1}{2} \cdot L_1 \cdot (I_{in} + \Delta i_{L1})^2$	$\sqrt{I_{in}^2 + \frac{\Delta i_{L1}^2}{3}}$	$(V_{out} + \Delta v_{C1})$
C_1	$\frac{1}{2} \cdot C_1 \cdot (V_{in} + V_{out} + \Delta v_{C1})^2$	$I_{in} \cdot \sqrt{\frac{(1-\delta)}{\delta}}$	$(V_{in} + V_{out} + \Delta v_{C1})$
L_2	$\frac{1}{2} \cdot L_2 \cdot (I_{out} + \Delta i_{L2})^2$	$\sqrt{I_{out}^2 + \frac{\Delta i_{L2}^2}{3}}$	$(V_{out} + \Delta v_{Cout})$
C_{out}	$\frac{1}{2} \cdot C_{out} \cdot (V_{out} + \Delta v_{Cout})^2$	$\frac{\Delta i_{L2}}{\sqrt{3}}$	$(V_{out} + \Delta v_{Cout})$

Finally, the semiconductor utilization factor is calculated from the *rms* current and v_{max} voltage expressions in Table 3.10 and Eq. (3.3):

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{(1-\delta)\cdot\delta}{\sqrt{\delta}+\sqrt{1-\delta}} \tag{3.81}$$

Again, the semiconductor utilization factor of this converter is the same as that of the zeta converter (which is drawn in Fig 3.10) and in consequence, same conclusions are obtained. The converter must be designed to operate with duty cycles close to 0.5 if the maximum semiconductor utilization is desired.

2.2.5.2 Power losses estimation

The semiconductor power losses are given by Eq. (3.1) and Eq. (3.2). Therefore, the currents and voltages in the semiconductors must be calculated. Obtained from the grey coloured areas of Fig 3.20a and Fig 3.20b, Table 3.10 summarizes the required current and voltage expressions for the power losses estimation.

TABLE 3.10
EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistor S_1**	**Diode D_1**
Average current (I_{ave})	I_{in}	I_{out}
rms current (I_{rms})	$\sqrt{\frac{{I_{in}}^2}{\delta}+\delta\cdot\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{3}}$	$\sqrt{(1-\delta)\cdot\left(\left(\frac{I_{in}}{\delta}\right)^2+\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{3}\right)}$
Maximum current (i_{max})	$(I_{in}+I_{out}+\Delta i_{L1}+\Delta i_{L2})$	$(I_{in}+I_{out}+\Delta i_{L1}+\Delta i_{L2})$
Turn-on switched current (i_{on})	$(I_{in}+I_{out}-\Delta i_{L1}-\Delta i_{L2})$	—
Turn-off switched current (i_{off})	$(I_{in}+I_{out}+\Delta i_{L1}+\Delta i_{L2})$	$(I_{in}+I_{out}-\Delta i_{L1}-\Delta i_{L2})$
Maximum voltage (v_{max})	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}\right)$	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}\right)$
Turn-on switched voltage (v_{on})	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}\right)$	—
Turn-off switched voltage (v_{off})	$\left(\frac{V_{in}}{(1-\delta)}-\Delta v_{C1}\right)$	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}\right)$

Therefore, introducing into Eq. (3.1) the current expressions of Table 3.10, average conduction power losses of S_1 and D_1 are given respectively as:

$$P_{cond\_S1} = V_{th}\cdot I_{in} + r_d\cdot\left(\frac{{I_{in}}^2}{\delta}+\delta\cdot\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{3}\right) \tag{3.82}$$

$$P_{cond\_D1} = V_{th} \cdot I_{out} + r_d \cdot (1-\delta) \cdot \left(\left(\frac{I_{in}}{\delta} \right)^2 + \frac{(\Delta i_{L1} + \Delta i_{L2})^2}{3} \right) \tag{3.83}$$

where r_d is the semiconductor switch on-state resistance and V_{th} is the semiconductor threshold voltage.

In addition, introducing into Eq. (3.2) the current and voltage expressions of Table 3.10, the average switching power losses of D_1 are expressed as:

$$P_{sw\_D1} = \frac{\left(\frac{V_{in}}{(1-\delta)} + \Delta v_{C1} \right)}{T_{sw} \cdot V_{100FIT}} \cdot \begin{pmatrix} A_{off,D1} \cdot (I_{in} + I_{out} - \Delta i_{L1} - \Delta i_{L2})^2 + \\ + B_{off,D1} \cdot (I_{in} + I_{out} - \Delta i_{L1} - \Delta i_{L2}) + C_{off,D1} \end{pmatrix} \tag{3.84}$$

where $A_{off,D1}$, $B_{off,D1}$ and $C_{off,D1}$ are the turn-off energy loss characteristic provided by the manufacturer for the 100FIT test voltage (V_{100FIT}).

Similarly, the average switching losses of S_1 are obtained:

$$\begin{aligned} P_{sw\_S1} = & \frac{\left(\frac{V_{in}}{(1-\delta)} - \Delta v_{C1} \right)}{T_{sw} \cdot V_{100FIT}} \cdot \begin{pmatrix} A_{off,S1} \cdot (I_{in} + I_{out} + \Delta i_{L1} + \Delta i_{L2})^2 + \\ + B_{off,S1} \cdot (I_{in} + I_{out} + \Delta i_{L1} + \Delta i_{L2}) + C_{off,S1} \end{pmatrix} + \\ & + \frac{\left(\frac{V_{in}}{(1-\delta)} + \Delta v_{C1} \right)}{T_{sw} \cdot V_{100FIT}} \cdot \begin{pmatrix} A_{on,S1} \cdot (I_{in} + I_{out} - \Delta i_{L1} - \Delta i_{L2})^2 + \\ + B_{on,S1} \cdot (I_{in} + I_{out} - \Delta i_{L1} - \Delta i_{L2}) + C_{on,S1} \end{pmatrix} \end{aligned} \tag{3.85}$$

where $A_{off,S1}$, $B_{off,S1}$ and $C_{off,S1}$ are the turn-off energy loss characteristic provided by the manufacturer for V_{100FIT} and $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are the turn-on energy loss characteristic.

2.2.6 Isolated-ćuk

Substituting ćuk converter's L_2 inductor by a medium frequency transformer, the isolated-ćuk converter shown in Fig 3.22 is obtained, thereby providing galvanic isolation. As noticed in Fig 3.22, the converter is unidirectional and comprises two inductors (L_1, L_2), four capacitors (C_{in}, C_1, C_2, C_{out}), a medium frequency transformer (the leakage inductance has been neglected in this analysis), a transistor (S_1) and a diode (D_1). Unlike the ćuk converter, the output voltage is not inverted.

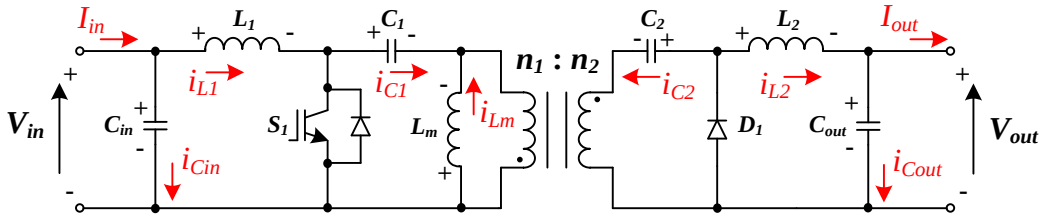


Fig 3.22. Isolated-ćuk converter.

2.2.6.1 Converter design

The operation of the converter is dependent to the transistor state. Thus, during S_1 transistor's on-state illustrated in Fig 3.23a (T_{on} time interval), the energy coming from the input is stored in the inductor L_1 while the energy stored in the capacitors C_1 and C_2 is transferred to L_2 and the load (Fig 3.19a). When S_1 is off (T_{off} time interval), the energy coming from the input and the energy stored in L_1 are transferred to C_1 and C_2 while L_2 supplies the load (Fig 3.23b).

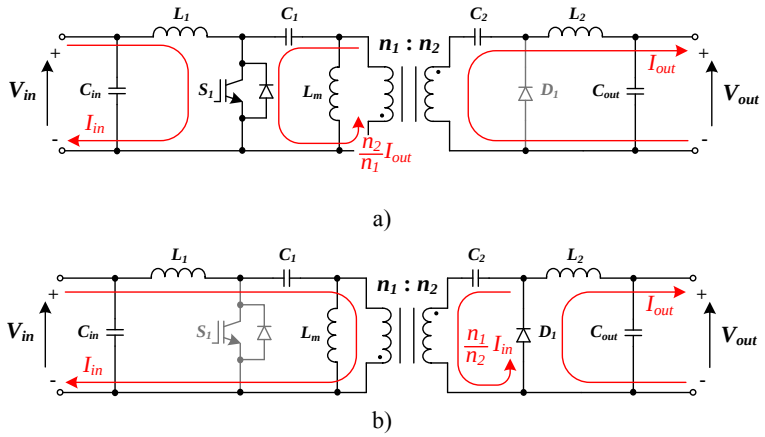


Fig 3.23. Currents circulating through the isolated-ćuk converter a) when S_1 is on and b) when S_1 is off.

Under a CCM operation, the steady state voltage and current waveforms are drawn as in Fig 3.24. The relation between the input/output voltages and the voltages of C_1 and C_2 are obtained from the steady state analysis of the inductors. Thus, from Fig 3.24a, Fig 3.24b and Fig 3.24c, the following voltage relations are obtained:

$$V_{in} = \left(V_{C2} \cdot \frac{n_1}{n_2} + V_{C1} \right) \cdot (1 - \delta) \tag{3.86}$$

$$V_{C1} = V_{C2} \cdot \frac{n_1}{n_2} \cdot \frac{(1 - \delta)}{\delta} \tag{3.87}$$

$$V_{out} = \left(V_{C1} \cdot \frac{n_2}{n_1} + V_{C2} \right) \cdot \delta \tag{3.88}$$

where n_1 and n_2 are the number of turns of primary and secondary windings respectively, δ is the duty cycle (T_{on}/T_{sw}), V_{in} and V_{out} are the average input and output voltages respectively (cf. Fig 3.22), V_{C1} is the average voltage of C_1 and V_{C2} is the average voltage of C_2.

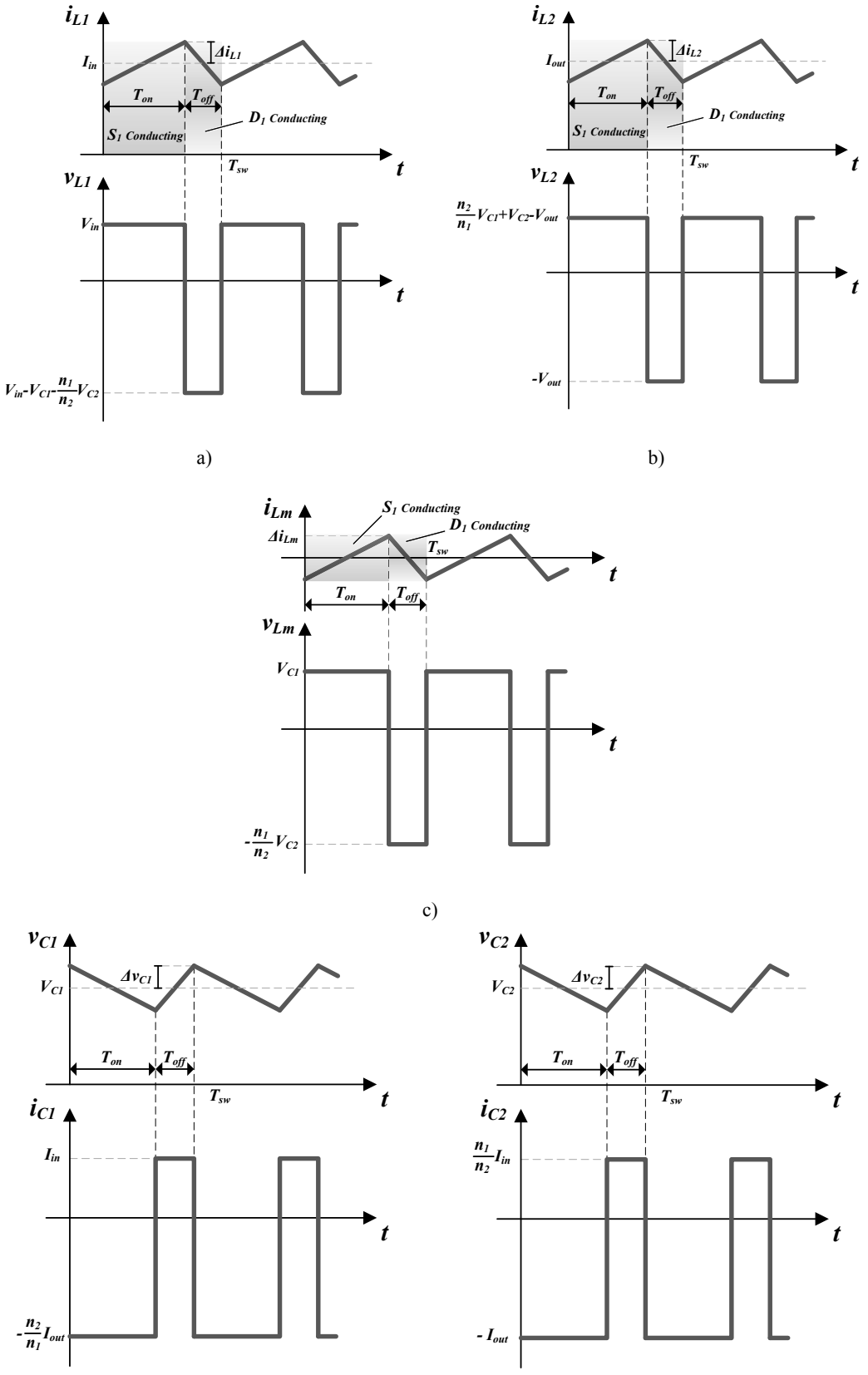


Fig 3.24. Typical voltage and current waveforms in isolated-ćuk converter's a) inductor L_1, b) inductor L_2, c) magnetizing inductance L_m, d) capacitor C_1 and e) capacitor C_2.

From the latter equations, V_{C1} and V_{C2} voltages and the DC voltage transfer function are calculated. The DC transfer function shows that isolated-ćuk converter's step-up/down nature depends on two terms, the duty cycle and the turn ratio of the MFT (n_2/n_1), which adds a degree of freedom for the design (the voltage elevation can be fixed by the transformer or by the duty cycle).

$$V_{C1} = V_{in} \tag{3.89}$$

$$V_{C2} = V_{out} \tag{3.90}$$

$$V_{out} = V_{in} \cdot \frac{\delta}{(1-\delta)} \cdot \frac{n_2}{n_1} \tag{3.91}$$

The DC current transfer function is obtained from the steady state analysis of the waveforms in the capacitors shown in Fig 3.24d and Fig 3.24e:

$$I_{out} = I_{in} \cdot \frac{(1-\delta)}{\delta} \cdot \frac{n_1}{n_2} \tag{3.92}$$

where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.22).

Additionally, Fig 3.24c shows the current circulating through the magnetizing inductance of the MFT is alternating, which means the magnetization of the transformer is bidirectional and in consequence, its utilization is good.

For calculating L_1 and L_2 inductances, the T_{on} time interval shown in Fig 3.24a, Fig 3.24b and Fig 3.24c has been analyzed:

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L1}} \cdot \delta \cdot T_{sw} \tag{3.93}$$

$$L_2 = v_{L2} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L2}} \cdot \frac{n_2}{n_1} \cdot \delta \cdot T_{sw} \tag{3.94}$$

$$L_m = v_{Lm} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{Lm}} \cdot \delta \cdot T_{sw} \tag{3.95}$$

where Δi_{L1}, Δi_{L2} and Δi_{Lm} are the current ripple through L_1 , L_2 and L_m respectively.

Similarly, the capacitances of C_1 and C_2 are obtained from the waveforms of Fig 3.24d and Fig 3.24e:

$$C_1 = i_{C1} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{C1}} \cdot \frac{n_2}{n_1} \cdot \delta \cdot T_{sw} \tag{3.96}$$

$$C_2 = i_{C2} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{C2}} \cdot \delta \cdot T_{sw} \tag{3.97}$$

where Δv_{C1} and Δv_{C2} are the desired voltage ripple in C_1 and C_2 respectively.

C_{in} and C_{out} capacitances have been calculated assuming the input current I_{in} and the output current I_{out} constant, Eq. (3.98) and (3.99). In consequence, the currents circulating through the capacitors are given by the ripple in L_1 and L_2 as depicted in Fig 3.21.

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{\Delta i_{L1}}{8 \cdot \Delta v_{Cin}} \cdot T_{sw} \tag{3.98}$$

$$C_{out} = \frac{Q_{Cout}}{\Delta v} = \frac{\Delta i_{L2}}{8 \cdot \Delta v_{Cout}} \cdot T_{sw} \tag{3.99}$$

where Δv_{Cin} and Δv_{Cout} are the half of the desired peak to peak voltage ripple in the input capacitor and the output capacitor respectively.

The main characteristics of the passive elements previously discussed are summarized in Table 3.11.

TABLE 3.11

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2} \cdot C_{in} \cdot (V_{in} + \Delta v_{Cin})^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$(V_{in} + \Delta v_{Cin})$
L_1	$\frac{1}{2} \cdot L_1 \cdot (I_{in} + \Delta i_{L1})^2$	$\sqrt{I_{in}^2 + \frac{\Delta i_{L1}^2}{3}}$	$\Delta v_{C1} + (V_{out} + \Delta v_{C2}) \cdot \frac{n_1}{n_2}$
C_1	$\frac{1}{2} \cdot C_1 \cdot (V_{in} + \Delta v_{C1})^2$	$I_{in} \cdot \sqrt{\frac{(1-\delta)}{\delta}}$	$(V_{in} + \Delta v_{C1})$
L_m	$\frac{1}{2} \cdot L_m \cdot \Delta i_{Lm}^2$	$\frac{\Delta i_{Lm}}{\sqrt{3}}$	$(V_{out} + \Delta v_{C2}) \cdot \frac{n_1}{n_2}$
C_2	$\frac{1}{2} \cdot C_2 \cdot (V_{out} + \Delta v_{C2})^2$	$I_{out} \cdot \sqrt{\frac{\delta}{(1-\delta)}}$	$(V_{out} + \Delta v_{C2})$
L_2	$\frac{1}{2} \cdot L_2 \cdot (I_{out} + \Delta i_{L2})^2$	$\sqrt{I_{out}^2 + \frac{\Delta i_{L2}^2}{3}}$	$(V_{out} + \Delta v_{Cout})$
C_{out}	$\frac{1}{2} \cdot C_{out} \cdot (V_{out} + \Delta v_{Cout})^2$	$\frac{\Delta i_{L2}}{\sqrt{3}}$	$(V_{out} + \Delta v_{Cout})$

At last, the semiconductor utilization factor U_f has been calculated:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{(1-\delta) \cdot \delta}{\sqrt{\delta} + \sqrt{1-\delta}} \tag{3.100}$$

As this utilization factor is equal to those of previously discussed step-up/down type converters, the optimal design point is given by δ=0.5 (graphically represented in Fig 3.10 for the zeta converter).

2.2.6.2 Power losses estimation

If the power losses are estimated by Eq. (3.1) and Eq. (3.2), the currents circulating through the semiconductors and the voltages they commutate must be calculated. The

currents conducted by transistor S_1 and diode D_1 are illustrated in Fig 3.24a, Fig 3.24b and Fig 3.24c. From those figures, the expressions summarized in Table 3.12 are obtained.

TABLE 3.12

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistor S_1**	**Diode D_1**
Average current (I_{ave})	I_{in}	I_{out}
rms current (I_{rms})	$\sqrt{\frac{{I_{in}}^2}{\delta}+\delta\cdot\frac{\left(\Delta i_{L1}+\Delta i_{Lm}+\Delta i_{L2}\cdot\frac{n_2}{n_1}\right)^2}{3}}$	$\sqrt{(1-\delta)\cdot\left(\left(\frac{I_{in}}{\delta}\cdot\frac{n_1}{n_2}\right)^2+\frac{\left((\Delta i_{L1}+\Delta i_{Lm})\cdot\frac{n_1}{n_2}+\Delta i_{L2}\right)^2}{3}\right)}$
Maximum current (i_{max})	$\left(I_{in}+\Delta i_{L1}+\Delta i_{Lm}+(I_{out}+\Delta i_{L2})\cdot\frac{n_2}{n_1}\right)$	$\left((I_{in}+\Delta i_{L1}+\Delta i_{Lm})\cdot\frac{n_1}{n_2}+I_{out}+\Delta i_{L2}\right)$
Turn-on switched current (i_{on})	$\left(I_{in}-\Delta i_{L1}-\Delta i_{Lm}+(I_{out}-\Delta i_{L2})\cdot\frac{n_2}{n_1}\right)$	—
Turn-off switched current (i_{off})	$\left(I_{in}+\Delta i_{L1}+\Delta i_{Lm}+(I_{out}+\Delta i_{L2})\cdot\frac{n_2}{n_1}\right)$	$\left((I_{in}-\Delta i_{L1}-\Delta i_{Lm})\cdot\frac{n_1}{n_2}+I_{out}-\Delta i_{L2}\right)$
Maximum voltage (v_{max})	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{C2}\cdot\frac{n_1}{n_2}\right)$	$\left(\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}\right)\cdot\frac{n_2}{n_1}+\Delta v_{C2}\right)$
Turn-on switched voltage (v_{on})	$\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}+\Delta v_{C2}\cdot\frac{n_1}{n_2}\right)$	—
Turn-off switched voltage (v_{off})	$\left(\frac{V_{in}}{(1-\delta)}-\Delta v_{C1}-\Delta v_{C2}\cdot\frac{n_1}{n_2}\right)$	$\left(\left(\frac{V_{in}}{(1-\delta)}+\Delta v_{C1}\right)\cdot\frac{n_2}{n_1}+\Delta v_{C2}\right)$

Therefore, from the *rms* and average current expressions in Table 3.12 and Eq. (3.1), the average conduction power losses of S_1 (P_{cond_S1}) and D_1 (P_{cond_D1}) are obtained:

$$P_{cond\_S1}=V_{th}\cdot I_{in}+r_d\cdot\left(\frac{{I_{in}}^2}{\delta}+\delta\cdot\frac{\left(\Delta i_{L1}+\Delta i_{Lm}+\Delta i_{L2}\cdot\frac{n_2}{n_1}\right)^2}{3}\right) \tag{3.101}$$

$$P_{cond\_D1}=V_{th}\cdot I_{out}+r_d\cdot(1-\delta)\cdot\left(\left(\frac{I_{in}}{\delta}\cdot\frac{n_1}{n_2}\right)^2+\frac{\left((\Delta i_{L1}+\Delta i_{Lm})\cdot\frac{n_1}{n_2}+\Delta i_{L2}\right)^2}{3}\right) \tag{3.102}$$

where r_d is the semiconductor switch on-state resistance and V_{th} is the semiconductor threshold voltage.

From the expressions of the current/voltage switched by D_1 in Table 3.12 and Eq. (3.2), the average switching power losses of D_1 are expressed as:

$$P_{sw\_D1} = \frac{\left(\left(\frac{V_{in}}{(1-\delta)} + \Delta v_{C1}\right)\cdot\frac{n_2}{n_1} + \Delta v_{C2}\right)}{T_{sw}\cdot V_{100FIT}}\cdot\left(\begin{array}{l} A_{off,D1}\cdot\left(\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm}\right)\cdot\frac{n_1}{n_2} + I_{out} - \Delta i_{L2}\right)^2 + \\ + B_{off,D1}\cdot\left(\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm}\right)\cdot\frac{n_1}{n_2} + I_{out} - \Delta i_{L2}\right) + \\ + C_{off,D1} \end{array}\right) \quad (3.103)$$

where $A_{off,D1}$, $B_{off,D1}$ and $C_{off,D1}$ are the turn-off energy loss characteristic provided by the manufacturer for the 100FIT test voltage (V_{100FIT}).

Similarly, the average switching losses of S_1 are obtained:

$$\begin{aligned} P_{sw\_S1} = {} & \frac{\left(\frac{V_{in}}{(1-\delta)} - \Delta v_{C1} - \Delta v_{C2}\cdot\frac{n_1}{n_2}\right)}{T_{sw}\cdot V_{100FIT}}\cdot\left(\begin{array}{l} A_{off,S1}\cdot\left(I_{in} + \Delta i_{L1} + \Delta i_{Lm} + \left(I_{out} + \Delta i_{L2}\right)\cdot\frac{n_2}{n_1}\right)^2 + \\ + B_{off,S1}\cdot\left(I_{in} + \Delta i_{L1} + \Delta i_{Lm} + \left(I_{out} + \Delta i_{L2}\right)\cdot\frac{n_2}{n_1}\right) + + \\ + C_{off,S1} \end{array}\right) \\ & + \frac{\left(\frac{V_{in}}{(1-\delta)} + \Delta v_{C1} + \Delta v_{C2}\cdot\frac{n_1}{n_2}\right)}{T_{sw}\cdot V_{100FIT}}\cdot\left(\begin{array}{l} A_{on,S1}\cdot\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} + \left(I_{out} - \Delta i_{L2}\right)\cdot\frac{n_2}{n_1}\right)^2 + \\ + B_{on,S1}\cdot\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} + \left(I_{out} - \Delta i_{L2}\right)\cdot\frac{n_2}{n_1}\right) + C_{on,S1} \end{array}\right) \end{aligned} \quad (3.104)$$

where $A_{off,S1}$, $B_{off,S1}$ and $C_{off,S1}$ are the turn-off energy loss characteristic provided by the manufacturer for V_{100FIT} and $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are the turn-on energy loss characteristic.

2.2.7 Flyback

The unidirectional flyback converter illustrated in Fig 3.25 is formed by two switches (transistor S_1 and diode D_1), a medium frequency transformer (the leakage inductance has been neglected in this analysis) and two filter capacitors at the input (C_{in}) and the output (C_{out}) sides of the converter. Hence, its few components make it a simple, cheap and a reliable converter. The flyback converter is a step-up/down converter.

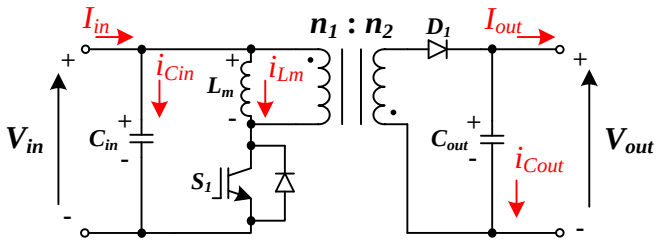
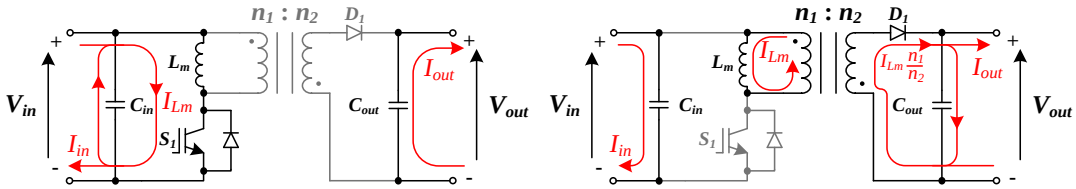


Fig 3.25. Flyback converter.

2.2.7.1 Converter design

The converter operates shifting the energy coming from the input between the magnetizing inductance of the MFT (L_m) and the output capacitor C_{out}. When transistor S_1 is on (T_{on} time interval), the energy coming from input and capacitor C_{in} is stored in L_m while the output is supplied by the output capacitor (Fig 3.26a). In turn, during the off-state of S_1 depicted in Fig 3.26b (T_{off} time interval), the input current flows through the input capacitor C_{in} and the energy stored by the magnetizing inductance is transferred to C_{out} and the load.



a) b)

Fig 3.26. Currents circulating through the flyback converter a) when S_1 is on and b) when S_1 is off.

Thus, considering a continuous current mode operation, the average input current I_{in} can be expressed as shown by Eq. (3.105). However, as in steady state the average current circulating through the input capacitor C_{in} is equal to zero, Eq. (3.105) can be simplified to Eq. (3.106). So, the input current is directly related to the average current through the magnetizing inductance I_{Lm}, which is always greater than I_{in}. In turn, this means the current through the transformer is DC and hence, the transformer utilization is poor as it is only positively magnetized.

$$I_{in} = \frac{\left(I_{Lm} - i_{Cin}\right) \cdot T_{on} + i_{Cin} \cdot T_{off}}{T_{sw}} \tag{3.105}$$

$$I_{in} = \frac{I_{Lm} \cdot T_{on}}{T_{sw}} = I_{Lm} \cdot \delta \tag{3.106}$$

where T_{sw} is the switching period, i_{Cin} is the current through the input capacitor and δ is the duty cycle of the transistor S_1.

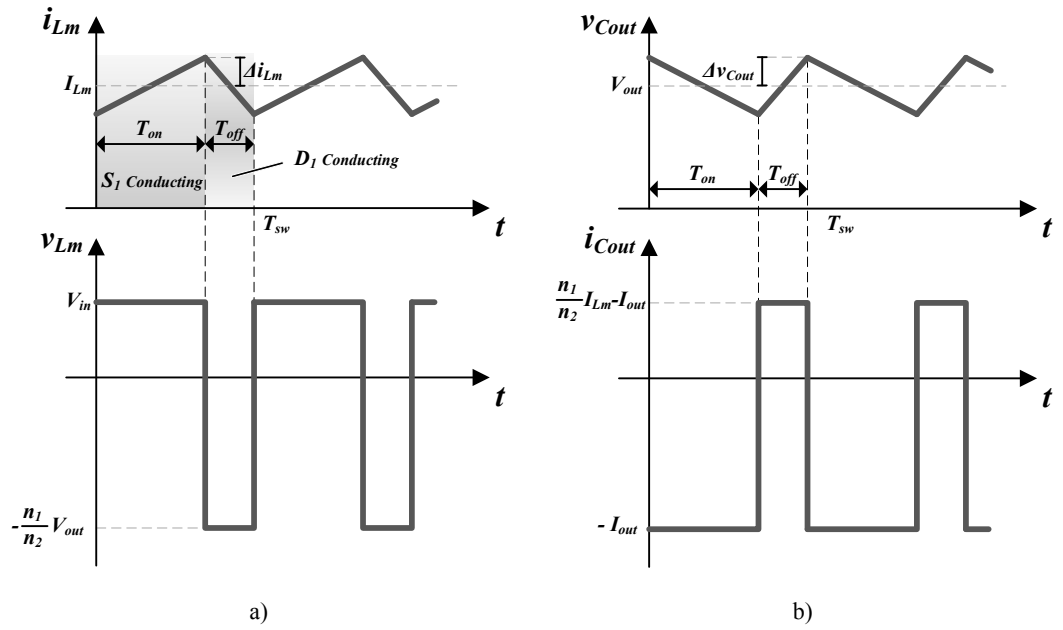
Moreover, neglecting the input and output voltage and current ripple, the steady state voltage and current waveforms in the converter are drawn as in Fig 3.27. From Fig 3.27a,

the DC voltage transfer function of Eq. (3.108) is obtained assuming the average voltage drop over the magnetizing inductance in a switching period (T_{sw}) is zero as given by Eq. (3.107). As noticed, with a unitary turn ratio n_2/n_1, V_{out} is lower than V_{in} when δ<0.5 and V_{out} is higher lower than V_{in} when δ>0.5. Hence, it can be considered that the flyback converter is a step-up/down converter.

$$\langle v_{Lm} \rangle = \frac{1}{T_{sw}} \cdot \left(\int_0^{T_{on}} v_{Lm}\ dt + \int_{T_{on}}^{T_{sw}} v_{Lm}\ dt \right) = 0 \tag{3.107}$$

$$V_{out} = V_{in} \cdot \frac{\delta}{(1-\delta)} \cdot \frac{n_2}{n_1} \tag{3.108}$$

where n_1 and n_2 are the number of turns of primary and secondary windings respectively, and V_{in} and V_{out} are the average input and output voltages respectively (cf. Fig 3.25).



a) b)

Fig 3.27. Typical voltage and current waveforms in flyback converter's a) L_m magnetizing inductance and b) output capacitor C_{out}.

Moreover, the DC current transfer function is obtained from the steady state analysis (i.e. assuming the average current through the capacitor is equal to zero) of the current waveforms illustrated in Fig 3.27b:

$$I_{out} = I_{in} \cdot \frac{(1-\delta)}{\delta} \cdot \frac{n_1}{n_2} \tag{3.109}$$

where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.25).

The magnetizing inductance L_m required by the transformer is calculated from the analysis of the waveforms of Fig 3.27a during the T_{on} period of time:

$$L_m = v_{Lm} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{Lm}} \cdot \delta \cdot T_{sw} \tag{3.110}$$

where Δi_{Lm} is the current ripple in the magnetizing inductance L_m.

Similarly, C_{out} capacitance is obtained from the waveforms of Fig 3.27b:

$$C_{out} = i_{Cout} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{Cout}} \cdot \delta \cdot T_{sw} \tag{3.111}$$

where Δv_{Cout} is the desired output voltage ripple.

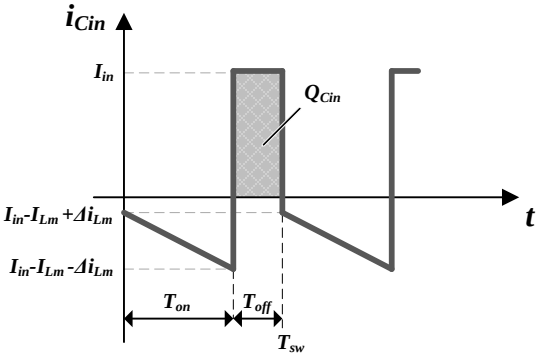


Fig 3.28. Current circulating through the input capacitor of the flyback converter.

Assuming a constant input current I_{in}, the current circulating through C_{in} can be illustrated as in Fig 3.28. Thus, the capacitance of C_{in} is obtained by calculating the Q_{Cin} charges depicted in Fig 3.28:

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{I_{in}}{2 \cdot \Delta v_{Cin}} \cdot T_{off} \tag{3.112}$$

where Δv_{Cin} is the half of the desired peak to peak voltage ripple in the input capacitor.

The main characteristics of the passive elements previously discussed are summarized in Table 3.13.

TABLE 3.13

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2} \cdot C_{in} \cdot \left(V_{in} + \Delta v_{Cin}\right)^2$	$\sqrt{I_{in}^{\,2} \cdot \frac{(1-\delta)}{\delta} + \delta \cdot \frac{\Delta i_{Lm}^{\,2}}{3}}$	$\left(V_{in} + \Delta v_{Cin}\right)$
L_m	$\frac{1}{2} \cdot L_m \cdot \left(I_{Lm} + \Delta i_{Lm}\right)^2$	$\sqrt{\left(\frac{I_{in}}{\delta}\right)^2 + \frac{\Delta i_{Lm}^{\,2}}{3}}$	$\left(V_{out} + \Delta v_{Cout}\right) \cdot \frac{n_1}{n_2}$
C_{out}	$\frac{1}{2} \cdot C_{out} \cdot \left(V_{out} + \Delta v_{Cout}\right)^2$	$I_{out} \cdot \sqrt{\frac{\delta}{(1-\delta)}}$	$\left(V_{out} + \Delta v_{Cout}\right)$

The semiconductor utilization factor (U_f) has been calculated from the voltage and current expressions of Table 3.14 and neglecting all the current and voltage ripple:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{(1-\delta)\cdot\delta}{\sqrt{\delta}+\sqrt{1-\delta}} \tag{3.113}$$

If Eq. (3.113) is illustrated for different duty cycle values Fig 3.29 is obtained. From the figure, same conclusion as for previously discussed step-up/down type converters is obtained: the optimal design point with maximum semiconductor utilization is provided with δ=0.5. Thus, according to this criteria, the converter must be designed to operate with duty cycles close to 0.5.

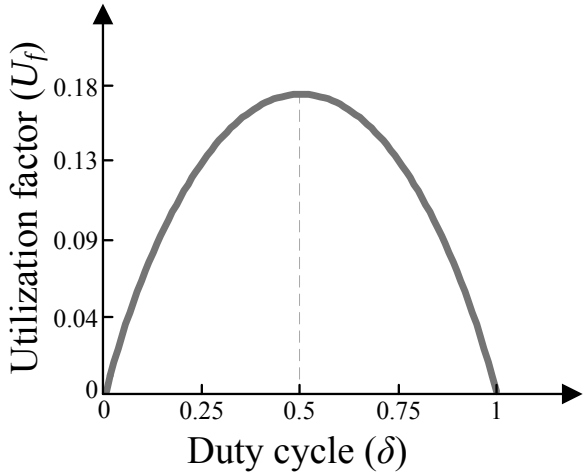


Fig 3.29. Semiconductor utilization factor of the flyback converter.

2.2.7.2 Power losses estimation

Obtained from Fig 3.27a, Table 3.14 summarizes switched currents and voltages as well as *rms* and average currents circulating through the different semiconductors. Therefore, average conduction power losses of transistor S_1 (P_{cond_S1}) and diode D_1 (P_{cond_D1}) are obtained from Eq. (3.1) and Table 3.14:

$$P_{cond\_S1} = V_{th}\cdot I_{in} + r_d \cdot \left(\frac{{I_{in}}^2}{\delta} + \delta \cdot \frac{{\Delta i_{Lm}}^2}{3} \right) \tag{3.114}$$

$$P_{cond\_D1} = V_{th}\cdot I_{out} + r_d \cdot (1-\delta)\cdot \left(\left(\frac{I_{in}}{\delta}\cdot\frac{n_1}{n_2} \right)^2 + \frac{\left(\Delta i_{Lm}\cdot\frac{n_1}{n_2} \right)^2}{3} \right) \tag{3.115}$$

where r_d is the semiconductor switch on-state resistance and V_{th} is the semiconductor threshold voltage.

From Eq. (3.2) and Table 3.14, the average switching power losses of D_1 are expressed as:

$$P_{sw\_D1} = \frac{\left(\frac{V_{out}}{\delta} + \Delta v_{Cout}\right)}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,D1} \cdot \left(\left(\frac{I_{in}}{\delta} - \Delta i_{Lm} \right) \cdot \frac{n_1}{n_2} \right)^2 + B_{off,D1} \cdot \left(\frac{I_{in}}{\delta} - \Delta i_{Lm} \right) \cdot \frac{n_1}{n_2} + C_{off,D1} \right) \quad (3.116)$$

where $A_{off,D1}$, $B_{off,D1}$ and $C_{off,D1}$ are the turn-off energy loss characteristic provided by the manufacturer for the 100FIT test voltage (V_{100FIT}).

TABLE 3.14

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistor S_1**	**Diode D_1**
Average current (I_{ave})	I_{in}	I_{out}
rms current (I_{rms})	$\sqrt{\frac{{I_{in}}^2}{\delta} + \delta \cdot \frac{{\Delta i_{Lm}}^2}{3}}$	$\sqrt{(1-\delta) \cdot \left(\left(\frac{I_{in}}{\delta} \cdot \frac{n_1}{n_2} \right)^2 + \frac{\left(\Delta i_{Lm} \cdot \frac{n_1}{n_2} \right)^2}{3} \right)}$
Maximum current (i_{max})	$\left(\frac{I_{in}}{\delta} + \Delta i_{Lm} \right)$	$\left(\frac{I_{in}}{\delta} + \Delta i_{Lm} \right) \cdot \frac{n_1}{n_2}$
Turn-on switched current (i_{on})	$\left(\frac{I_{in}}{\delta} - \Delta i_{Lm} \right)$	—
Turn-off switched current (i_{off})	$\left(\frac{I_{in}}{\delta} + \Delta i_{Lm} \right)$	$\left(\frac{I_{in}}{\delta} - \Delta i_{Lm} \right) \cdot \frac{n_1}{n_2}$
Maximum voltage (v_{max})	$\left(\frac{V_{in}}{(1-\delta)} + \Delta v_{Cout} \cdot \frac{n_1}{n_2} \right)$	$\left(\frac{V_{out}}{\delta} + \Delta v_{Cout} \right)$
Turn-on switched voltage (v_{on})	$\left(\frac{V_{in}}{(1-\delta)} + \Delta v_{Cout} \cdot \frac{n_1}{n_2} \right)$	—
Turn-off switched voltage (v_{off})	$\left(\frac{V_{in}}{(1-\delta)} - \Delta v_{Cout} \cdot \frac{n_1}{n_2} \right)$	$\left(\frac{V_{out}}{\delta} + \Delta v_{Cout} \right)$

Similarly, the average switching losses of S_1 are provided by:

$$\begin{aligned} P_{sw\_S1} = {} & \frac{\left(\frac{V_{in}}{(1-\delta)} - \Delta v_{Cout} \cdot \frac{n_1}{n_2} \right)}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,S1} \cdot \left(\frac{I_{in}}{\delta} + \Delta i_{Lm} \right)^2 + B_{off,S1} \cdot \left(\frac{I_{in}}{\delta} + \Delta i_{Lm} \right) + C_{off,S1} \right) + \\ & + \frac{\left(\frac{V_{in}}{(1-\delta)} + \Delta v_{Cout} \cdot \frac{n_1}{n_2} \right)}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{on,S1} \cdot \left(\frac{I_{in}}{\delta} - \Delta i_{Lm} \right)^2 + B_{on,S1} \cdot \left(\frac{I_{in}}{\delta} - \Delta i_{Lm} \right) + C_{on,S1} \right) \end{aligned} \quad (3.117)$$

where $A_{off,S1}$, $B_{off,S1}$ and $C_{off,S1}$ are the turn-off energy loss characteristic provided by the manufacturer for V_{100FIT} and $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are the turn-on energy loss characteristic.

2.2.8 Forward

The forward converter is a unidirectional converter as shown in Fig 3.30. Although it is a step-down converter it can step-up the input voltage depending on the turn ratio of the transformer. The converter comprises four switches (transistor S_1 and D_1-D_2-D_3 diodes), a medium frequency transformer (the leakage inductance has been neglected in this analysis), an input capacitor (C_{in}) and a LC filter at the output (L_1 inductor and C_{out} capacitor). As it will be explained later, the MFT of the forward converter has three windings, two for the energy transference and one for the demagnetization of the transformer.

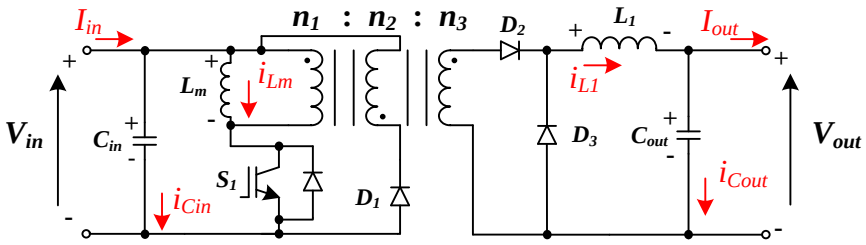


Fig 3.30. Forward converter.

2.2.8.1 Converter design

The converter operates storing the energy coming from the input into its inner passive elements and then transferring it to the output. This way, Fig 3.31a shows that during S_1 is on (T_{on} time interval), the energy coming from input and capacitor C_{in} is transferred to L_1 and the load. At the same time, the MFT is magnetized positively. When S_1 is off (T_{off} time interval), the energy coming from the input is stored in C_{in} and the load is supplied by the output inductor L_1 (Fig 3.31c). It must be highlighted that during the initial period at which S_1 is off (t_{off} time interval), the transformer is demagnetized through the demagnetization coil (n_2). Thus, the energy stored in the magnetizing inductance L_m is returned to the input as depicted in Fig 3.31b. Therefore, the transformer is only magnetized positively leading to a poor utilization of it.

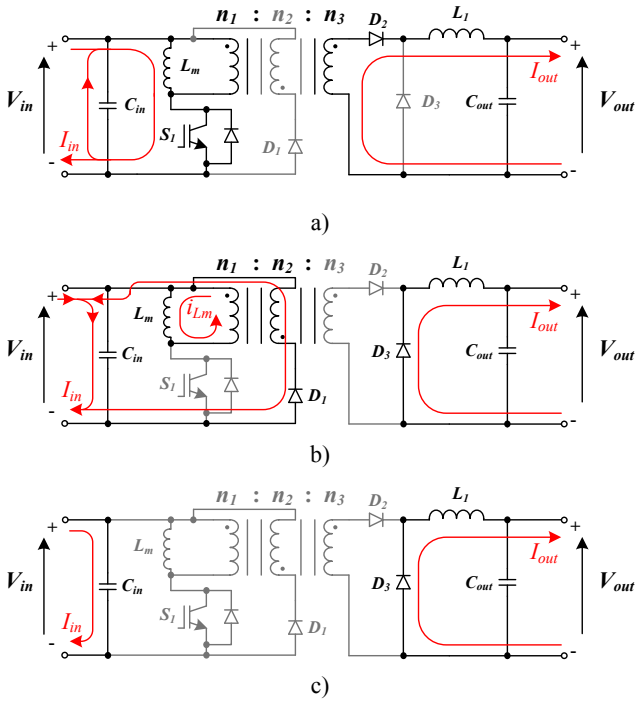


Fig 3.31. Currents circulating through the forward converter a) when S_1 is on, b) when S_1 is off and the energy stored in L_m is drawn by the input, and c) when S_1 is off and L_m has no energy stored.

Aforementioned operational behaviour is illustrated in the voltage and current waveforms of Fig 3.32, where a CCM operation has been considered and the input and output voltage ripple have been neglected.

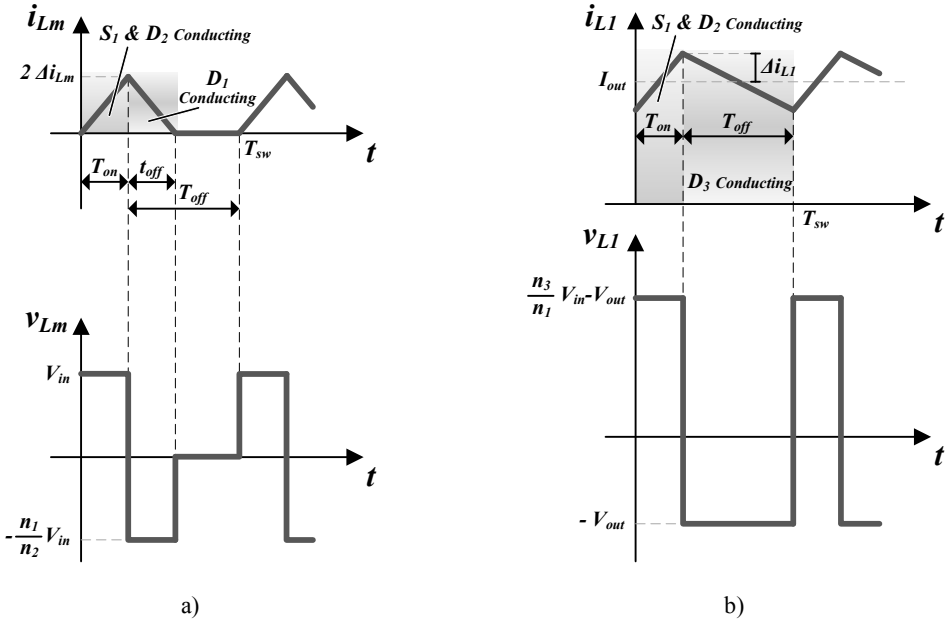


Fig 3.32. Typical voltage and current waveforms in forward converter's a) L_m magnetizing inductance and b) inductor L_1.

As shown by Fig 3.32a, the transformer demagnetization time interval (t_{off}) is not necessarily equal to the transistor's off-state period of time (T_{off}). Analyzing the waveforms of Fig 3.32a, it can be seen that the demagnetization period is dependant to the n_2/n_1 turn ratio as shown below:

$$\left.\begin{aligned} V_{in} &= \frac{2\cdot\Delta i_{Lm}}{T_{on}} \\ -V_{in}\cdot\frac{n_1}{n_2} &= -\frac{2\cdot\Delta i_{Lm}}{t_{off}} \end{aligned}\right\} \rightarrow t_{off} = T_{on}\cdot\frac{n_2}{n_1} \tag{3.118}$$

where V_{in} is the average input voltage (cf. Fig 3.30) and Δi_{Lm} is the current ripple in the magnetizing inductance L_m.

However, when the maximum energy is transferred, the demagnetization time is equal to the off-state time ($t_{off} = T_{off}$). From this fact, the maximum time at which the transistor S_1 can be on ($T_{on,\max}$) can be calculated, Eq. (3.119). As noticed, the transformer turn ratio n_2/n_1 limits the maximum duty cycle of the converter, which means this turn ratio must be carefully selected so as to optimize the design of the converter. The turn ratio that maximizes the utilization of the semiconductors is calculated later in this section.

$$\left.\begin{aligned} t_{off} &= T_{on}\cdot\frac{n_2}{n_1} \\ t_{off} &= T_{sw} - T_{on} \end{aligned}\right\} \rightarrow T_{on,\max} = \frac{T_{sw}}{1+\frac{n_2}{n_1}} \rightarrow \delta_{\max} = \frac{1}{1+\frac{n_2}{n_1}} \tag{3.119}$$

where T_{sw} is the switching period of S_1 and average input voltage and $\delta_{\max}$ is the maximum duty cycle of the converter.

The DC voltage transfer function of Eq. (3.120) is calculated from Fig 3.32b under the assumption of zero average voltage drop in the output inductor L_1 during a switching period (steady state analysis). Eq. (3.120) shows that the forward converter is a step-down converter as mentioned in the beginning of this section. Notice that with a unitary n_3/n_1 turn ratio the output voltage can never be greater than the input voltage.

$$V_{out} = V_{in}\cdot\delta\cdot\frac{n_3}{n_1} \tag{3.120}$$

where V_{out} is the average output voltage (cf. Fig 3.30) and δ is the duty cycle of the converter (T_{on}/T_{sw}).

In order to obtain the DC current transfer function it has been assumed that the average input power is equal to the average output power (ideal case with no losses):

$$\left.\begin{aligned} V_{in}\cdot I_{in} &= V_{out}\cdot I_{out} \\ V_{out} &= V_{in}\cdot\delta\cdot\frac{n_3}{n_1} \end{aligned}\right\} \rightarrow I_{out} = \frac{I_{in}}{\delta}\cdot\frac{n_1}{n_3} \tag{3.121}$$

where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.30).

The inductive value of L_1 is calculated analyzing the T_{off} time interval of Fig 3.32b:

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{out}}{2 \cdot \Delta i_{L1}} \cdot (1-\delta) \cdot T_{sw} \tag{3.122}$$

where Δi_{L1} is the current ripple in L_1. As expected, the lower the current ripple the higher will be the required inductance.

Similarly, the magnetizing inductance required by the MFT is calculated from Fig 3.32a:

$$L_m = v_{Lm} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{Lm}} \cdot \delta \cdot T_{sw} \tag{3.123}$$

where Δi_{Lm} is the current ripple in the magnetizing inductance.

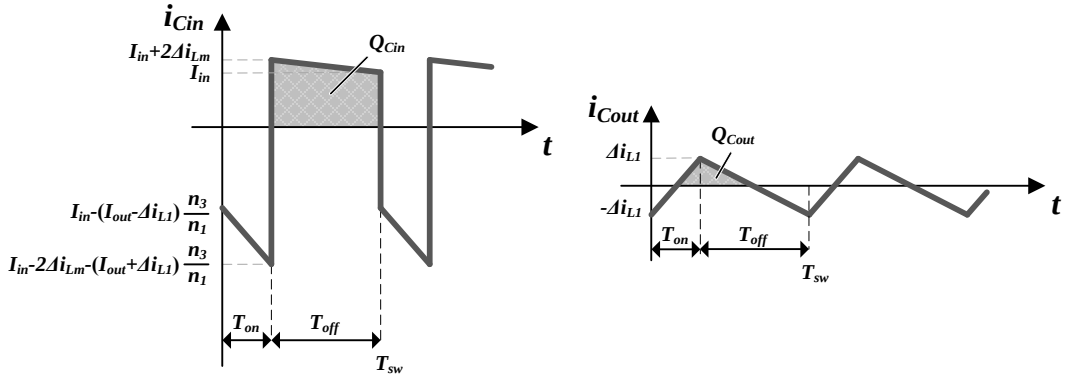
For the calculation of the input DC bus capacitance (C_{in}) a constant input current has been assumed. Therefore, considering δ_{max} is lower than 0.5 (as it will be discussed later, the maximum utilization of the semiconductors is achieved with δ_{max}=0.4435, for which, n_2/n_1 is about 1.2547 and t_{off} is equal to T_{off}), the current circulating through C_{in} can be drawn as in Fig 3.33a. In consequence, C_{in} capacitance is obtained from calculating the Q_{Cin} charges circulating through it and the desired voltage ripple Δv_{Cin}, Eq. (3.124).

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{(I_{in} + \Delta i_{Lm}) \cdot T_{off}}{2 \cdot \Delta v_{Cin}} \tag{3.124}$$

Moreover, as the output current I_{out} is assumed to be constant, it can be deduced from Fig 3.32b that the current through the output capacitor (i_{Cout}) is given by the current ripple in L_1. Thus, i_{Cout} can be illustrated as in Fig 3.33b and its capacitance calculated as follows:

$$C_{out} = \frac{Q_{Cout}}{\Delta v} = \frac{\Delta i_{L1}}{8 \cdot \Delta v_{Cout}} \cdot T_{sw} \tag{3.125}$$

where Δv_{Cout} is the half of the desired peak to peak output voltage ripple.



a) b)

Fig 3.33. Currents circulating through a) the input capacitor and b) the output capacitor of the forward converter.

The main characteristics of the passive elements are summarized in Table 3.15.

TABLE 3.15

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2}\cdot C_{in}\cdot\left(V_{in}+\Delta v_{Cin}\right)^2$	$\sqrt{\frac{\delta}{3}\cdot\chi}$	$\left(V_{in}+\Delta v_{Cin}\right)$
L_m	$\frac{1}{2}\cdot L_m\cdot\left(2\cdot\Delta i_{Lm}\right)^2$	$2\cdot\Delta i_{Lm}\cdot\sqrt{\frac{\delta}{3}\cdot\left(1+\frac{n_2}{n_1}\right)}$	$\left(V_{in}+\Delta v_{Cin}\right)$
L_1	$\frac{1}{2}\cdot L_1\cdot\left(I_{out}+\Delta i_{L1}\right)^2$	$\sqrt{{I_{out}}^2+\frac{{\Delta i_{L1}}^2}{3}}$	$\approx\left(\left(V_{in}+\Delta v_{Cin}\right)\cdot\frac{n_3}{n_1}-V_{out}\right)$
C_{out}	$\frac{1}{2}\cdot C_{out}\cdot\left(V_{out}+\Delta v_{Cout}\right)^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$\left(V_{out}+\Delta v_{Cout}\right)$
$\chi=$	$\left[\begin{array}{l}\frac{n_2}{n_1}\cdot\left(I_{in}+2\cdot\Delta i_{Lm}\right)^2-\frac{1}{2}\cdot\left(\Delta i_{L1}\cdot\frac{n_3}{n_1}+\Delta i_{Lm}\right)^{-1}\cdot\left(I_{in}-\left(I_{out}+\Delta i_{L1}\right)\cdot\frac{n_3}{n_1}-2\cdot\left(\Delta i_{L1}\cdot\frac{n_3}{n_1}+\Delta i_{Lm}\right)\right)^3+\\ +\frac{1}{2}\cdot\left(\Delta i_{L1}\cdot\frac{n_3}{n_1}+\Delta i_{Lm}\right)^{-1}\cdot\left(I_{in}-\left(I_{out}+\Delta i_{L1}\right).\frac{n_3}{n_1}\right)^3+2\cdot\frac{n_2}{n_1}\cdot\left({I_{in}}^2+I_{in}\cdot\Delta i_{Lm}\right)\end{array}\right]$		

The semiconductor utilization factor (U_f) of Eq. (3.126) is calculated from the voltages and currents of Table 3.16 and Table 3.17. Current and voltage ripple of those expressions have been neglected so as to simplify the U_f expression.

$$U_f=\frac{P_{Rated}}{\sum_{all\_switches}v_{\max}\cdot I_{rms}}=\frac{\left(1-\delta_{\max}\right)\cdot\delta}{\left(1+\delta_{\max}\right)\cdot\sqrt{\delta}+\left(1-\delta_{\max}\right)\cdot\sqrt{1-\delta}} \tag{3.126}$$

As noticed, the utilization factor is dependant to the maximum duty cycle ($\delta_{\max}$), which in turn depends on the transformer turn ratio n_2/n_1. This means, n_2/n_1 must be carefully chosen for maximizing the semiconductor utilization (hence, for optimizing the converter design). In Fig 3.34 the utilization factor is plotted for different $\delta_{\max}$ values in order to determine the optimal n_2/n_1 turn ratio. As noticed, the maximum utilization factor is given by $\delta_{\max}\approx0.4435$ and in consequence, the optimal n_2/n_1 turn ratio is $n_2/n_1\approx1.2547$, cf. Eq. (3.126). In turn, this makes the n_3/n_1 turn ratio must be chosen so as to ensure the converter operates with a duty cycle close to $\delta_{\max}$ (Eq. (3.120)).

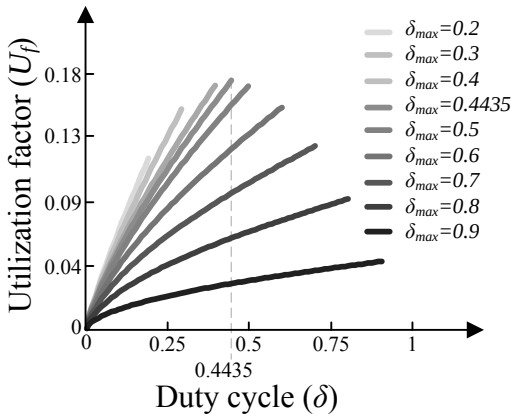


Fig 3.34. Semiconductor utilization factor of the forward converter.

2.2.8.2 Power losses estimation

The semiconductor power losses are calculated analytically by estimating average conduction power losses of Eq. (3.1) and average switching power losses of Eq. (3.2). The voltage and current expressions required for estimating those power losses are obtained from the waveforms of Fig 3.32 (note that the conduction time interval of each semiconductor is identified) and summarized in Table 3.16 and Table 3.17. Thus, the average conduction power losses of transistor S_1 (P_{cond_S1}), diode D_1 (P_{cond_D1}), diode D_2 (P_{cond_D2}) and diode D_3 (P_{cond_D3}) are given as follows:

$$P_{cond\_S1} = V_{th} \cdot \left(I_{in} + \Delta i_{Lm} \cdot \delta\right) + r_d \cdot \left[\left(I_{out} \cdot \frac{n_3}{n_1} + \Delta i_{Lm} \right)^2 + \frac{\left(\Delta i_{Lm} + \Delta i_{L1} \cdot \frac{n_3}{n_1} \right)^2}{3} \right] \cdot \delta \tag{3.127}$$

$$P_{cond\_D1} = V_{th} \cdot \Delta i_{Lm} \cdot \delta + r_d \cdot \left(2 \cdot \Delta i_{Lm}\right)^2 \cdot \frac{n_1}{n_2} \cdot \frac{\delta}{3} \tag{3.128}$$

$$P_{cond\_D2} = V_{th} \cdot I_{out} \cdot \delta + r_d \cdot \delta \cdot \left({I_{out}}^2 + \frac{{\Delta i_{L1}}^2}{3} \right) \tag{3.129}$$

$$P_{cond\_D3} = V_{th} \cdot I_{out} \cdot \left(1 - \delta\right) + r_d \cdot \left(1 - \delta\right) \cdot \left({I_{out}}^2 + \frac{{\Delta i_{L1}}^2}{3} \right) \tag{3.130}$$

where r_d is the on-state resistance and V_{th} is the threshold voltage.

TABLE 3.16

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE INPUT SIDE SEMICONDUCTORS

Current and voltage expressions	Transistor S_1	Diode D_1
Average current (I_{ave})	$I_{in} + \Delta i_{Lm} \cdot \delta$	$\Delta i_{Lm} \cdot \delta$
rms current (I_{rms})	$\sqrt{\left[\left(I_{out} \cdot \frac{n_3}{n_1} + \Delta i_{Lm}\right)^2 + \frac{\left(\Delta i_{Lm} + \Delta i_{L1} \cdot \frac{n_3}{n_1}\right)^2}{3}\right] \cdot \delta}$	$2 \cdot \Delta i_{Lm} \cdot \sqrt{\frac{n_1}{n_2} \cdot \frac{\delta}{3}}$
Maximum current (i_{max})	$\left(\left(I_{out} + \Delta i_{L1}\right) \cdot \frac{n_3}{n_1} + 2 \cdot \Delta i_{Lm}\right)$	$2 \cdot \frac{n_1}{n_2} \cdot \Delta i_{Lm}$
Turn-on switched current (i_{on})	$\left(I_{out} - \Delta i_{L1}\right) \cdot \frac{n_3}{n_1}$	—
Turn-off switched current (i_{off})	$\left(\left(I_{out} + \Delta i_{L1}\right) \cdot \frac{n_3}{n_1} + 2 \cdot \Delta i_{Lm}\right)$	0
Maximum voltage (v_{max})	$\left(1 + \frac{n_1}{n_2}\right) \cdot \left(V_{in} - \Delta v_{Cin}\right)$	$\left(1 + \frac{n_2}{n_1}\right) \cdot \left(V_{in} + \Delta v_{Cin}\right)$
Turn-on switched voltage (v_{on})	$\left(1 + \frac{n_1}{n_2}\right) \cdot \left(V_{in} + \Delta v_{Cin}\right)$	—
Turn-off switched voltage (v_{off})	$\left(1 + \frac{n_1}{n_2}\right) \cdot \left(V_{in} - \Delta v_{Cin}\right)$	$\left(1 + \frac{n_2}{n_1}\right) \cdot \left(V_{in} - \Delta v_{Cin}\right)$

Furthermore, the average switching power losses of transistor S_1 (P_{sw_S1}), diode D_2 (P_{sw_D2}) and diode D_3 (P_{sw_D3}) are given as follows:

$$P_{sw\_S1} = \frac{\left(1 + \frac{n_1}{n_2}\right) \cdot \left(V_{in} - \Delta v_{Cin}\right)}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,S1} \cdot \left(\left(I_{out} + \Delta i_{L1}\right) \cdot \frac{n_3}{n_1} + 2 \cdot \Delta i_{Lm} \right)^2 + \right.$$
$$\left. + B_{off,S1} \cdot \left(\left(I_{out} + \Delta i_{L1}\right) \cdot \frac{n_3}{n_1} + 2 \cdot \Delta i_{Lm} \right) + C_{off,S1} \right) +$$
$$+ \frac{\left(1 + \frac{n_1}{n_2}\right) \cdot \left(V_{in} + \Delta v_{Cin}\right)}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{on,S1} \cdot \left(\left(I_{out} - \Delta i_{L1}\right) \cdot \frac{n_3}{n_1} \right)^2 + B_{on,S1} \cdot \left(I_{out} - \Delta i_{L1}\right) \cdot \frac{n_3}{n_1} + C_{on,S1} \right) \quad (3.131)$$

$$P_{sw\_D2} = \frac{\frac{n_3}{n_2} \cdot \left(V_{in} - \Delta v_{Cin}\right)}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,D2} \cdot \left(I_{out} + \Delta i_{L1}\right)^2 + B_{off,D2} \cdot \left(I_{out} + \Delta i_{L1}\right) + C_{off,D2} \right) \quad (3.132)$$

$$P_{sw\_D3} = \frac{\frac{n_3}{n_1} \cdot \left(V_{in} + \Delta v_{Cin}\right)}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,D3} \cdot \left(I_{out} - \Delta i_{L1}\right)^2 + B_{off,D3} \cdot \left(I_{out} - \Delta i_{L1}\right) + C_{off,D3} \right) \quad (3.133)$$

where A_{XX}, B_{XX} and C_{XX} are the switching energy loss characteristic coefficients provided by the manufacturer for the 100FIT test voltage (V_{100FIT}) of each semiconductor switch.

TABLE 3.17
EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE OUTPUT SIDE SEMICONDUCTORS

Current and voltage expressions	Diode D_2	Diode D_3
Average current (I_{ave})	$I_{out} \cdot \delta$	$I_{out} \cdot (1-\delta)$
rms current (I_{rms})	$\sqrt{\delta \cdot \left({I_{out}}^2 + \frac{{\Delta i_{L1}}^2}{3} \right)}$	$\sqrt{(1-\delta) \cdot \left({I_{out}}^2 + \frac{{\Delta i_{L1}}^2}{3} \right)}$
Maximum current (i_{max})	$(I_{out} + \Delta i_{L1})$	$(I_{out} + \Delta i_{L1})$
Turn-off switched current (i_{off})	$(I_{out} + \Delta i_{L1})$	$(I_{out} - \Delta i_{L1})$
Maximum voltage (v_{max})	$\frac{n_3}{n_2} \cdot (V_{in} + \Delta v_{Cin})$	$\frac{n_3}{n_1} \cdot (V_{in} + \Delta v_{Cin})$
Turn-off switched voltage (v_{off})	$\frac{n_3}{n_2} \cdot (V_{in} - \Delta v_{Cin})$	$\frac{n_3}{n_1} \cdot (V_{in} + \Delta v_{Cin})$

The switching power losses of D_1 are considered negligible (P_{sw_D1}=0) since it is turned-off when the current through it reaches zero (noticeable in Fig 3.32a and Table 3.16).

2.2.9 Two-transistor forward

The two-transistor forward converter of Fig 3.35 is a unidirectional converter derived from the previously discussed forward converter. Therefore, the two-transistor forward converter is also a step-down converter. The main difference between the two converters is that the two-transistor forward does not have a third winding for the demagnetization of the medium frequency transformer. Hence, the design of its MFT is easier than that of the forward converter. However, the two-transistor forward converter requires one more semiconductor than that required by the forward converter. As depicted in Fig 3.35, two-transistor forward converter is composed of four diodes (D_1-D_2-D_3-D_4), two transistors (S_1-S_2), a medium frequency transformer (its leakage inductance has been neglected in this analysis), an input capacitor (C_{in}) and a LC filter at the output (inductor L_1 and capacitor C_{out}).

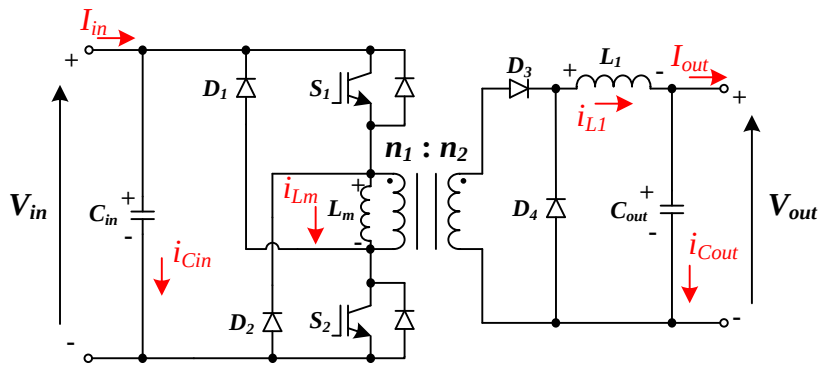


Fig 3.35. Two-transistor forward converter.

2.2.9.1 Converter design

The operation of the converter is based on the storage and subsequent transference of the energy coming from the input. The transistors of the converter are operated simultaneously. Thus, when transistors S_1 and S_2 are on (T_{on} time interval), the energy coming from input and C_{in} capacitor is transferred to the output inductor L_1 and the load while the MFT is magnetized positively (Fig 3.36a). On the other hand, when S_1 and S_2 transistors are off (T_{off} time interval), the C_{in} capacitor stores the energy coming from input and L_1 supplies the output load (Fig 3.36c). During the initial period in which S_1 and S_2 are off (t_{off} time interval) the transformer is demagnetized through the demagnetization diodes D_1 and D_2. As a consequence, the energy stored in the magnetizing inductance L_m is returned to the input (Fig 3.36b). This way, the transformer is only magnetized positively (cf. Fig 3.37a) and in consequence, its utilization is poor. Fig 3.37 illustrates the current and voltage waveforms resulting from afore described operation considering a CCM and neglecting the ripple of the input and output voltages.

From Fig 3.37a, the time t_{off} at which the transformer is demagnetized is equal to T_{on} as given by Eq. (3.134). To avoid transformer's core saturation, the most critical case at which the demagnetization is guaranteed is when t_{off} =T_{off}. Therefore, the maximum duty cycle of the converter is equal to 0.5 as provided by Eq. (3.135).

$$\left.\begin{aligned} V_{in} &= \frac{2\cdot\Delta i_{Lm}}{T_{on}} \\ -V_{in} &= -\frac{2\cdot\Delta i_{Lm}}{t_{off}} \end{aligned}\right\} \rightarrow t_{off} = T_{on} \tag{3.134}$$

$$\left.\begin{aligned} t_{off} &= T_{on} \\ t_{off} &= T_{sw} - T_{on} \end{aligned}\right\} \rightarrow \delta_{\max} = \frac{1}{2} \tag{3.135}$$

where V_{in} is the average input voltage (cf. Fig 3.35), Δi_{Lm} is the current ripple in the magnetizing inductance L_m, T_{sw} is the switching period and $\delta_{\max}$ is the maximum duty cycle of the converter (T_{on}/T_{sw}).

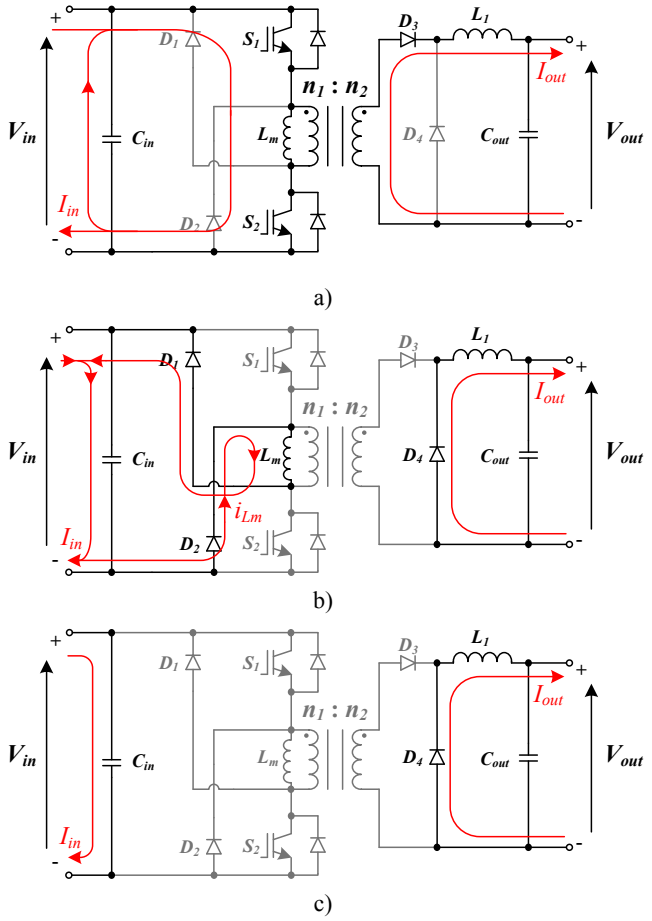


Fig 3.36. Currents circulating through the two-transistor forward converter a) when S_1-S_2 are on, b) when S_1-S_2 are off and the energy stored in L_m is drawn by the input, and c) when S_1-S_2 are off and L_m has no energy stored.

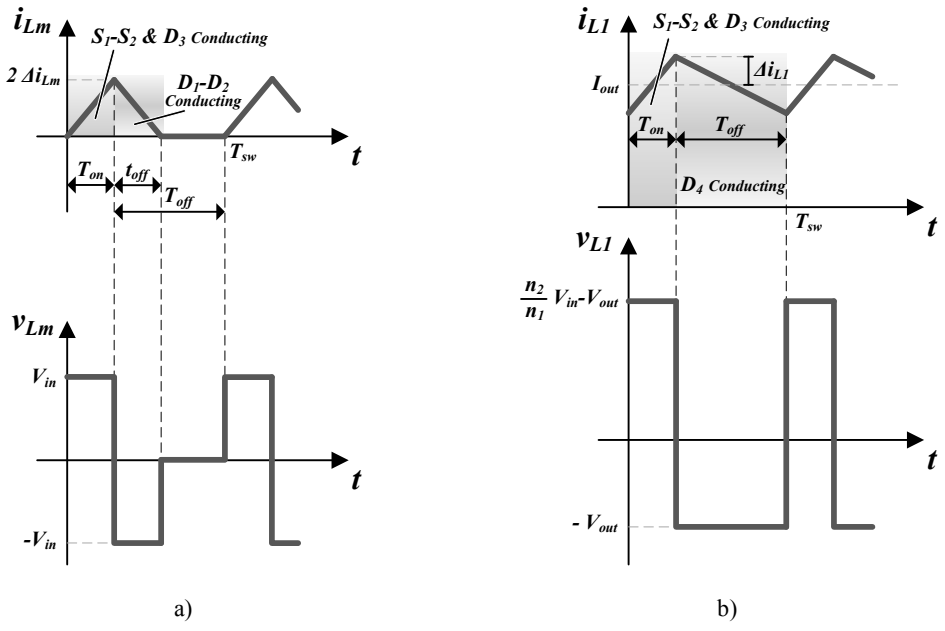


Fig 3.37. Typical voltage and current waveforms in two-transistor forward converter's a) magnetizing inductance L_m and b) inductor L_1.

In turn, the DC voltage transfer function is obtained from the steady state analysis of the waveforms of Fig 3.37b:

$$V_{out} = V_{in} \cdot \delta \cdot \frac{n_2}{n_1} \tag{3.136}$$

where V_{out} is the average output voltage (cf. Fig 3.35) and δ is the duty cycle of the converter.

Assuming an ideal operation with no losses, the average input power is equal to the average output power. Thus, the DC current transfer function is given as below:

$$\left.\begin{aligned} V_{in} \cdot I_{in} &= V_{out} \cdot I_{out} \\ V_{out} &= V_{in} \cdot \delta \cdot \frac{n_2}{n_1} \end{aligned}\right\} \rightarrow I_{out} = \frac{I_{in}}{\delta} \cdot \frac{n_1}{n_2} \tag{3.137}$$

where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.35).

Furthermore, analyzing the waveforms of Fig 3.37b, the inductive value of L_1 is obtained as follows:

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{out}}{2 \cdot \Delta i_{L1}} \cdot (1-\delta) \cdot T_{sw} \tag{3.138}$$

where Δi_{L1} is the current ripple in L_1. As expected, the lower the current ripple the higher will be the required inductance.

Similarly, the magnetizing inductance L_m is calculated from the waveforms of Fig 3.37a:

$$L_m = v_{Lm} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{Lm}} \cdot \delta \cdot T_{sw} \tag{3.139}$$

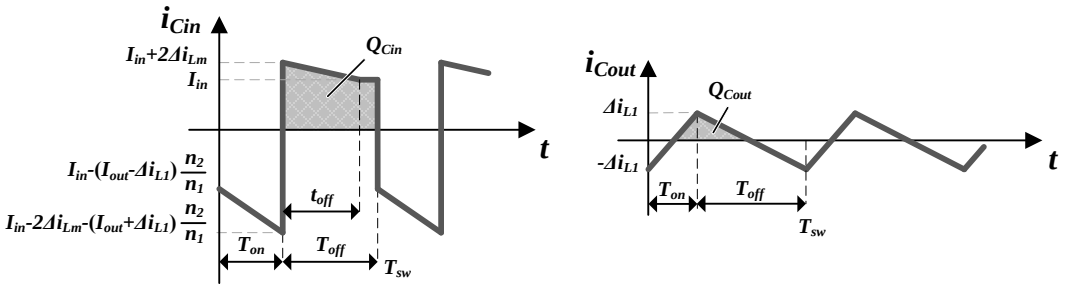
where Δi_{Lm} is the current ripple in L_m.

The capacitances of C_{in} and C_{out} can be calculated from Fig 3.38, where the currents though them are drawn assuming the average input and output currents (I_{in} and I_{out}) are constant. In Fig 3.38a, the duty cycle is slightly lower than 0.5 since due to the practical operational limitations of the semiconductors, in real conditions, the converter cannot be operated with the maximum ideal duty cycle δ_{max}=0.5. Thus, C_{in} capacitance is given by Eq. (3.140). Nonetheless, C_{out} capacitance is given by the charge circulation caused by the current ripple in L_1 as shown in Fig 3.38b, Eq. (3.141).

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{I_{in} \cdot T_{off} + \Delta i_{Lm} \cdot t_{off}}{2 \cdot \Delta v_{Cin}} \tag{3.140}$$

$$C_{out} = \frac{Q_{Cout}}{\Delta v} = \frac{\Delta i_{L1}}{8 \cdot \Delta v_{Cin}} \cdot T_{sw} \tag{3.141}$$

where Δv_{Cin} and Δv_{Cout} are the half of the desired peak to peak input and output voltage ripple respectively.



a) b)

Fig 3.38. Currents circulating through a) the input capacitor and b) the output capacitor of the two-transistor forward converter.

Table 3.18 summarizes the equations regarding to the maximum stored energy, the maximum voltage stress and the *rms* currents circulating through the passive elements of the converter.

TABLE 3.18

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2}\cdot C_{in}\cdot\left(V_{in}+\Delta v_{Cin}\right)^2$	$\sqrt{I_{in}{}^2\cdot\left(1-2\cdot\delta\right)+\frac{\delta}{3}\cdot\chi}$	$\left(V_{in}+\Delta v_{Cin}\right)$
L_m	$\frac{1}{2}\cdot L_m\cdot\left(2\cdot\Delta i_{Lm}\right)^2$	$2\cdot\Delta i_{Lm}\cdot\sqrt{\frac{2\cdot\delta}{3}}$	$\left(V_{in}+\Delta v_{Cin}\right)$
L_1	$\frac{1}{2}\cdot L_1\cdot\left(I_{out}+\Delta i_{L1}\right)^2$	$\sqrt{I_{out}{}^2+\frac{\Delta i_{L1}{}^2}{3}}$	$\approx\left(\left(V_{in}+\Delta v_{Cin}\right)\cdot\frac{n_2}{n_1}-V_{out}\right)$
C_{out}	$\frac{1}{2}\cdot C_{out}\cdot\left(V_{out}+\Delta v_{Cout}\right)^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$\left(V_{out}+\Delta v_{Cout}\right)$

$$\chi=\left[\begin{array}{l}\left(I_{in}+2\cdot\Delta i_{Lm}\right)^2-\frac{1}{2}\cdot\left(\Delta i_{L1}\cdot\frac{n_2}{n_1}+\Delta i_{Lm}\right)^{-1}\cdot\left(I_{in}-\left(I_{out}+\Delta i_{L1}\right)\cdot\frac{n_2}{n_1}-2\cdot\left(\Delta i_{L1}\cdot\frac{n_2}{n_1}+\Delta i_{Lm}\right)\right)^3+\\+\frac{1}{2}\cdot\left(\Delta i_{L1}\cdot\frac{n_2}{n_1}+\Delta i_{Lm}\right)^{-1}\cdot\left(I_{in}-\left(I_{out}+\Delta i_{L1}\right)\cdot\frac{n_2}{n_1}\right)^3+2\cdot\left(I_{in}{}^2+I_{in}\cdot\Delta i_{Lm}\right)\end{array}\right]$$

The semiconductor utilization factor (U_f) of Eq. (3.142) is calculated from the maximum voltages and *rms* currents of Table 3.19 and Table 3.20. It must be highlighted that the current and voltage ripple of those expressions have been neglected for the U_f expression calculation.

$$U_f=\frac{P_{Rated}}{\sum_{all\_switches}v_{\max}\cdot I_{rms}}=\frac{\delta}{3\cdot\sqrt{\delta}+\sqrt{1-\delta}} \tag{3.142}$$

For different duty cycle values, Eq. (3.142) is illustrated in Fig 3.39. As noticed, the semiconductor utilization increases along with the increase of the duty cycle. Therefore, given that the DC voltage transfer function of Eq. (3.136) depends on the duty cycle and

the transformer turn ratio, n_2/n_1 turn ratio must be carefully chosen to guarantee the converter's operation with duty cycles close to the maximum value of 0.5.

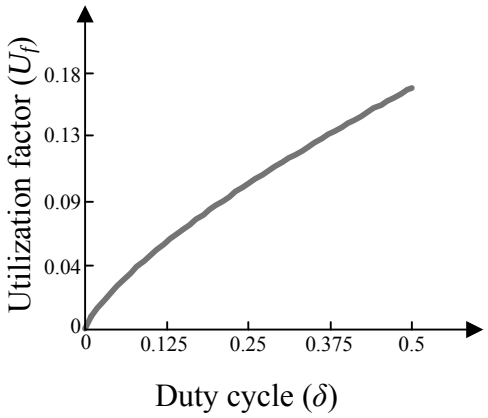


Fig 3.39. Semiconductor utilization factor of the two-transistor forward converter.

2.2.9.2 Power losses estimation

Semiconductor power losses are calculated analytically by estimating average conduction power losses, Eq. (3.1), and average switching power losses, Eq. (3.2). Obtained from Fig 3.37, the voltage and current expressions required for estimating those power losses are summarized in Table 3.19 and Table 3.20. It must be highlighted that due to the simultaneous operation of the two transistors of the converter, the currents through them and their blocking voltages are the same. Similarly, the current circulating through D_1 and D_2 diodes as well as their reverse blocking voltages are also same.

From Table 3.19 and Eq. (3.1), the average conduction power losses of the input side semiconductors are given as follows (P_{cond_S1} for transistors S_1-S_2 and P_{cond_D1} for diodes D_1-D_2):

$$P_{cond\_S1} = V_{th} \cdot \left(I_{in} + \Delta i_{Lm} \cdot \delta\right) + r_d \cdot \left[\left(I_{out} \cdot \frac{n_2}{n_1} + \Delta i_{Lm} \right)^2 + \frac{\left(\Delta i_{Lm} + \Delta i_{L1} \cdot \frac{n_2}{n_1} \right)^2}{3} \right] \cdot \delta \tag{3.143}$$

$$P_{cond\_D1} = V_{th} \cdot \Delta i_{Lm} \cdot \delta + r_d \cdot \left(2 \cdot \Delta i_{Lm}\right)^2 \cdot \frac{\delta}{3} \tag{3.144}$$

where r_d and V_{th} are each semiconductor's on-state resistance and threshold voltage respectively.

TABLE 3.19

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE INPUT SIDE SEMICONDUCTORS

Current and voltage expressions	**Transistors S_1-S_2**	**Diodes D_1-D_2**
Average current (I_{ave})	$I_{in} + \Delta i_{Lm} \cdot \delta$	$\Delta i_{Lm} \cdot \delta$
rms current (I_{rms})	$\sqrt{\left[\left(I_{out} \cdot \frac{n_2}{n_1} + \Delta i_{Lm}\right)^2 + \frac{\left(\Delta i_{Lm} + \Delta i_{L1} \cdot \frac{n_2}{n_1}\right)^2}{3}\right] \cdot \delta}$	$2 \cdot \Delta i_{Lm} \cdot \sqrt{\frac{\delta}{3}}$
Maximum current (i_{max})	$\left(\left(I_{out} + \Delta i_{L1}\right) \cdot \frac{n_2}{n_1} + 2 \cdot \Delta i_{Lm}\right)$	$2 \cdot \Delta i_{Lm}$
Turn-on switched current (i_{on})	$\left(I_{out} - \Delta i_{L1}\right) \cdot \frac{n_2}{n_1}$	—
Turn-off switched current (i_{off})	$\left(\left(I_{out} + \Delta i_{L1}\right) \cdot \frac{n_2}{n_1} + 2 \cdot \Delta i_{Lm}\right)$	0
Maximum voltage (v_{max})	$\left(V_{in} - \Delta v_{Cin}\right)$	$\left(V_{in} + \Delta v_{Cin}\right)$
Turn-on switched voltage (v_{on})	$\frac{\left(V_{in} + \Delta v_{Cin}\right)}{2}$	—
Turn-off switched voltage (v_{off})	$\left(V_{in} - \Delta v_{Cin}\right)$	$\frac{\left(V_{in} + \Delta v_{Cin}\right)}{2}$

TABLE 3.20

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE OUTPUT SIDE SEMICONDUCTORS

Current and voltage expressions	**Diode D_3**	**Diode D_4**
Average current (I_{ave})	$I_{out} \cdot \delta$	$I_{out} \cdot (1 - \delta)$
rms current (I_{rms})	$\sqrt{\delta \cdot \left({I_{out}}^2 + \frac{{\Delta i_{L1}}^2}{3}\right)}$	$\sqrt{(1-\delta) \cdot \left({I_{out}}^2 + \frac{{\Delta i_{L1}}^2}{3}\right)}$
Maximum current (i_{max})	$\left(I_{out} + \Delta i_{L1}\right)$	$\left(I_{out} + \Delta i_{L1}\right)$
Turn-off switched current (i_{off})	$\left(I_{out} + \Delta i_{L1}\right)$	$\left(I_{out} - \Delta i_{L1}\right)$
Maximum voltage (v_{max})	$\frac{n_2}{n_1} \cdot \left(V_{in} + \Delta v_{Cin}\right)$	$\frac{n_2}{n_1} \cdot \left(V_{in} + \Delta v_{Cin}\right)$
Turn-off switched voltage (v_{off})	$\frac{n_2}{n_1} \cdot \left(V_{in} - \Delta v_{Cin}\right)$	$\frac{n_2}{n_1} \cdot \left(V_{in} + \Delta v_{Cin}\right)$

Similarly, from Table 3.20 and Eq. (3.1), average conduction power losses of the output side D_3 diode (P_{cond_D3}) and D_4 diode (P_{cond_D4}) are obtained:

$$P_{cond\_D3} = V_{th} \cdot I_{out} \cdot \delta + r_d \cdot \delta \cdot \left({I_{out}}^2 + \frac{\Delta {i_{L1}}^2}{3} \right) \tag{3.145}$$

$$P_{cond\_D4} = V_{th} \cdot I_{out} \cdot (1-\delta) + r_d \cdot (1-\delta) \cdot \left({I_{out}}^2 + \frac{\Delta {i_{L1}}^2}{3} \right) \tag{3.146}$$

The switching power losses of D_1 and D_2 are negligible as they are turned-off when the current through them is equal to zero (Table 3.19 and Fig 3.37a). Conversely, average switching power losses of the transistors (P_{sw_S1}), diode D_3 (P_{sw_D3}) and diode D_4 (P_{sw_D4}) are given as follows:

$$\begin{aligned} P_{sw\_S1} = {} & \frac{(V_{in} - \Delta v_{Cin})}{T_{sw} \cdot V_{100FIT}} \cdot \left(\begin{array}{l} A_{off,S1} \cdot \left((I_{out} + \Delta i_{L1}) \cdot \frac{n_2}{n_1} + 2 \cdot \Delta i_{Lm} \right)^2 + \\ + B_{off,S1} \cdot \left((I_{out} + \Delta i_{L1}) \cdot \frac{n_2}{n_1} + 2 \cdot \Delta i_{Lm} \right) + C_{off,S1} \end{array} \right) + \\ & + \frac{(V_{in} + \Delta v_{Cin})}{2 \cdot T_{sw} \cdot V_{100FIT}} \cdot \left(A_{on,S1} \cdot \left((I_{out} - \Delta i_{L1}) \cdot \frac{n_2}{n_1} \right)^2 + B_{on,S1} \cdot (I_{out} - \Delta i_{L1}) \cdot \frac{n_2}{n_1} + C_{on,S1} \right) \end{aligned} \tag{3.147}$$

$$P_{sw\_D3} = \frac{\frac{n_2}{n_1} \cdot (V_{in} - \Delta v_{Cin})}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,D3} \cdot (I_{out} + \Delta i_{L1})^2 + B_{off,D3} \cdot (I_{out} + \Delta i_{L1}) + C_{off,D3} \right) \tag{3.148}$$

$$P_{sw\_D4} = \frac{\frac{n_2}{n_1} \cdot (V_{in} + \Delta v_{Cin})}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,D4} \cdot (I_{out} - \Delta i_{L1})^2 + B_{off,D4} \cdot (I_{out} - \Delta i_{L1}) + C_{off,D4} \right) \tag{3.149}$$

where $A_{off,XX}$, $B_{off,XX}$ and $C_{off,XX}$ are the turn-off energy loss characteristic coefficients provided by the manufacturer for the 100FIT test voltage (V_{100FIT}) of each semiconductor switch and $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are the turn-on energy loss characteristic coefficients of the transistors.

2.2.10 Push-pull

The push-pull converter of Fig 3.40 is a unidirectional converter derived from buck converter. The converter is composed of an input capacitor (C_{in}), two transistors at the input side (S_1-S_2), a medium frequency transformer with three windings (the leakage inductances have been neglected for the analysis), a diode rectifier (D_1-D_2-D_3-D_4) and an output side LC filter (inductor L_1 and capacitor C_{out}).

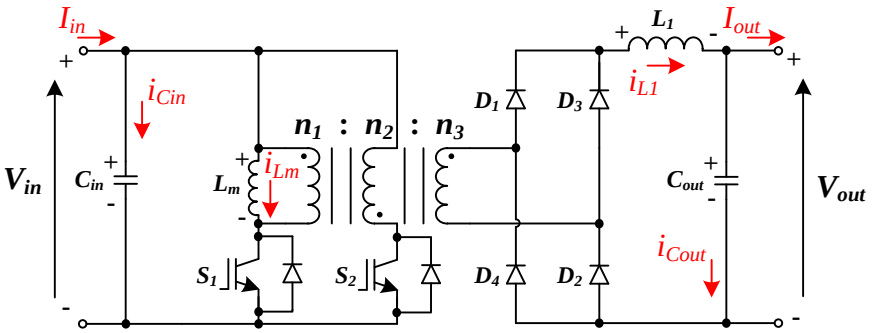


Fig 3.40. Push-pull converter.

2.2.10.1 Converter design

The converter operates alternating the switching orders of the transistors. Thus, when transistor S_1 is on, transistor S_2 is off and vice versa. During the on-state of transistor S_1 shown in Fig 3.41a (T_{on} time interval), the energy coming from the input and the capacitor C_{in} is transferred to the inductor L_1 and the load. At the same time, the magnetizing inductance L_m is magnetized positively.

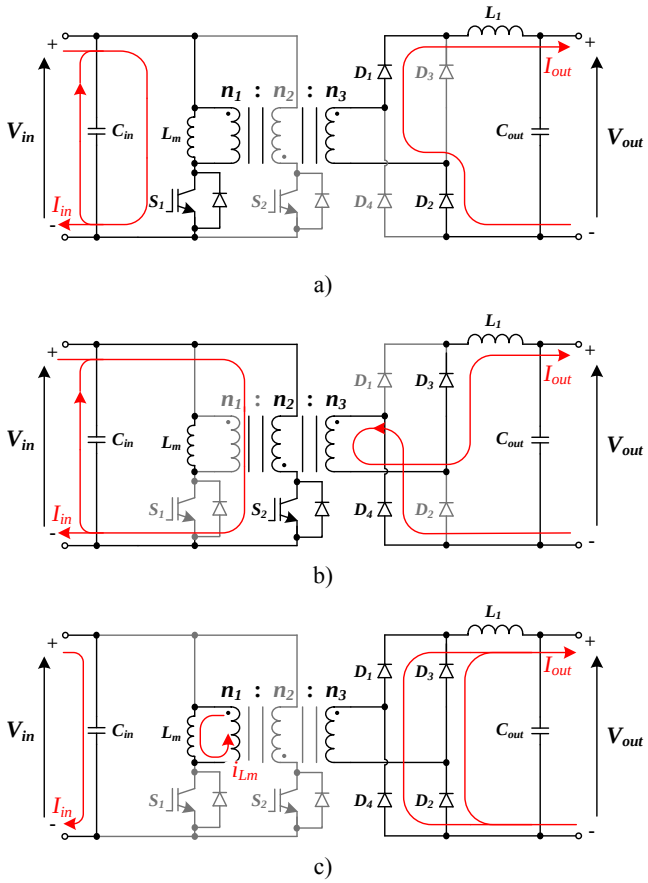
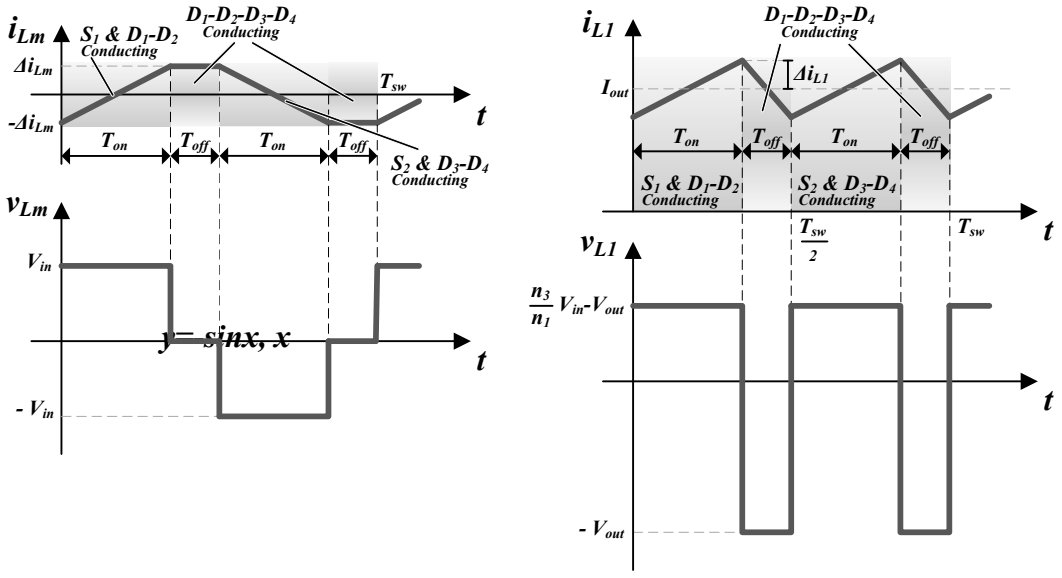


Fig 3.41. Currents circulating through the push-pull converter a) when S_1 is on and S_2 is off, b) when S_1 is off and S_2 is on, and c) when S_1-S_2 are off and the current in L_m flows through the output rectifier diodes.

When transistor S_2 is on, the converter operates similarly with the only difference that the magnetizing inductance is magnetized negatively (cf. Fig 3.41b). Conversely, when both transistors are off (T_{off} time interval), inductor L_1 supplies the load and the magnetizing current flows through the output diodes (cf. Fig 3.41c).

Assuming the number of turns of the primary windings n_1 and n_2 are equal, a continuous current mode operation and neglecting the ripple of the input and output voltages, Fig 3.42 shows the current and voltage waveforms resulting from the afore described operation.



a) b)

Fig 3.42. Typical voltage and current waveforms in push-pull converter's a) magnetizing inductance L_m and b) inductor L_1.

As it can be noticed in Fig 3.42a, the transformer is magnetized bidirectionally leading to a good utilization of it. In turn, it can be deduced that each transistor cannot be on more than half of the switching period ($T_{sw}/2$), otherwise, the transformer core will be saturated inevitably, cf. Eq. (3.150). In fact, even respecting this limit, the control scheme must guarantee the average voltage applied to the transformer is zero in order to avoid transformer saturation (no DC injection).

$$T_{on,\max} = \frac{T_{sw}}{2} \rightarrow \delta_{\max} = \frac{1}{2} \tag{3.150}$$

where $\delta_{\max}$ is the maximum duty cycle of the converter ($T_{on,\max}/T_{sw}$).

The DC voltage transfer function is derived from steady state analysis of the waveforms of Fig 3.42b:

$$V_{out} = 2 \cdot V_{in} \cdot \delta \cdot \frac{n_3}{n_1} \tag{3.151}$$

where V_{in} and V_{out} are the average input and output voltages respectively, δ is the duty cycle of the converter and n_3 represents the number of turns of the secondary winding of the MFT (cf. Fig 3.40).

Assuming that the average input power is equal to the average output power, the DC current transfer function is given by:

$$\left.\begin{aligned} V_{in} \cdot I_{in} &= V_{out} \cdot I_{out} \\ V_{out} &= 2 \cdot V_{in} \cdot \delta \cdot \frac{n_3}{n_1} \end{aligned}\right\} \rightarrow I_{out} = \frac{I_{in}}{2 \cdot \delta} \cdot \frac{n_1}{n_3} \tag{3.152}$$

where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.40).

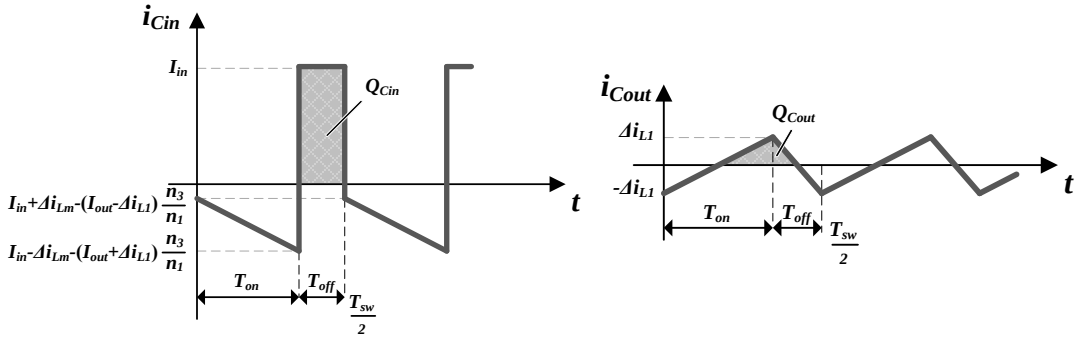
The values of the magnetizing inductance L_m and the output side inductor L_1 are obtained from the steady state analysis of the waveforms in Fig 3.42a and Fig 3.42b respectively:

$$L_m = v_{Lm} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{Lm}} \cdot \delta \cdot T_{sw} \tag{3.153}$$

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{out}}{4 \cdot \Delta i_{L1}} \cdot (1 - 2 \cdot \delta) \cdot T_{sw} \tag{3.154}$$

where Δi_{Lm} is the current ripple in L_m and Δi_{L1} is the current ripple in L_1.

The currents through input and output capacitors are depicted in Fig 3.43, where it has been assumed that the average input and output currents (I_{in} and I_{out}) are constant.



a) b)

Fig 3.43. Currents circulating through a) the input capacitor and b) the output capacitor of the push-pull converter.

Therefore, C_{in} capacitance is calculated from Fig 3.43a, where the charges variation in the capacitor is illustrated (Q_{Cin}):

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{I_{in} \cdot \left(\frac{T_{sw}}{2} - T_{on} \right)}{2 \cdot \Delta v_{Cin}} \tag{3.155}$$

where Δv_{Cin} is the half of the desired peak to peak input voltage ripple.

Similarly, C_{out} capacitance can be obtained from Fig 3.43b:

$$C_{out} = \frac{Q_{Cout}}{\Delta v} = \frac{\Delta i_{L1}}{16 \cdot \Delta v_{Cout}} \cdot T_{sw} \tag{3.156}$$

where Δv_{Cout} is the half of the desired peak to peak output voltage ripple.

Additionally, the expressions of the maximum energy stored by the passive elements, their maximum voltage stress and the *rms* currents circulating through them are derived from the waveforms of Fig 3.42 and Fig 3.43. These expressions are summarized Table 3.21.

TABLE 3.21

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2} \cdot C_{in} \cdot (V_{in} + \Delta v_{Cin})^2$	$\sqrt{2 \cdot \delta \cdot \chi + (1 - 2 \cdot \delta) \cdot {I_{in}}^2}$	$(V_{in} + \Delta v_{Cin})$
L_m	$\frac{1}{2} \cdot L_m \cdot {\Delta i_{Lm}}^2$	$\Delta i_{Lm} \cdot \sqrt{1 - \frac{4 \cdot \delta}{3}}$	$(V_{in} + \Delta v_{Cin})$
L_1	$\frac{1}{2} \cdot L_1 \cdot (I_{out} + \Delta i_{L1})^2$	$\sqrt{{I_{out}}^2 + \frac{{\Delta i_{L1}}^2}{3}}$	$(V_{out} + \Delta v_{Cout})$
C_{out}	$\frac{1}{2} \cdot C_{out} \cdot (V_{out} + \Delta v_{Cout})^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$(V_{out} + \Delta v_{Cout})$
$\chi = \left(\left(I_{in} - I_{out} \cdot \frac{n_3}{n_1} \right)^2 + \frac{\left(\Delta i_{L1} \cdot \frac{n_3}{n_1} + \Delta i_{Lm} \right)^2}{3} \right)$			

The semiconductor utilization factor (U_f) is calculated from the voltage and current expressions of Table 3.22:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{\delta}{2 \cdot \sqrt{\delta} + \sqrt{1 - 2 \cdot \delta}} \tag{3.157}$$

This semiconductor utilization factor is plotted in Fig 3.44 for different duty cycle values. As it can be noticed, the higher the duty cycle the better the semiconductor utilization. Therefore, in order to minimize the semiconductor installed power in the converter, n_2/n_1 turn ratio must be carefully chosen to guarantee that the converter operates with duty cycles close to 0.5.

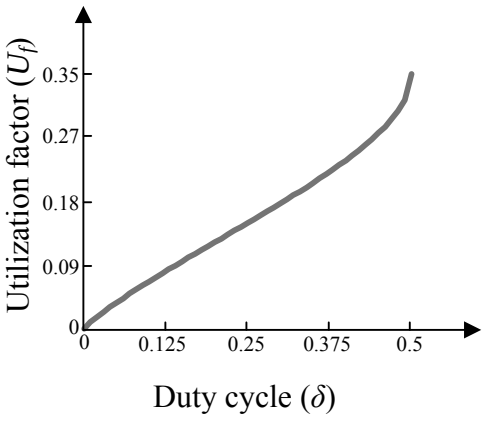


Fig 3.44. Semiconductor utilization factor of the push-pull converter.

2.2.10.2 Power losses estimation

The transistors S_1 and S_2 conduct the same current. Thus, average power losses in both transistors are equal. As it can be noticed in Fig 3.42, this is applicable to output side rectifier diodes D_1-D_2-D_3-D_4. Thus, power losses expressions are calculated just for one semiconductor in each group. Table 3.22 summarizes the expressions of the currents through the semiconductors as well as of the voltages they block.

TABLE 3.22

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistors S_1-S_2**	**Diodes D_1-D_2-D_3-D_4**
Average current (I_{ave})	$\frac{I_{in}}{2}$	$\frac{I_{out}}{2}$
rms current (I_{rms})	$\sqrt{\left[\left(I_{out}\cdot\frac{n_3}{n_1}\right)^2+\frac{\left(\Delta i_{Lm}+\Delta i_{L1}\cdot\frac{n_3}{n_1}\right)^2}{3}\right]\cdot\delta}$	$\sqrt{(1+2\cdot\delta)\cdot\left[\left(\frac{I_{out}}{2}\right)^2+\frac{1}{3}\cdot\left(\frac{\Delta i_{L1}}{2}\right)^2\right]+(1-2\cdot\delta)\cdot\left(\frac{\Delta i_{Lm}}{2}\cdot\frac{n_1}{n_3}\right)^2}$
Maximum current (i_{max})	$\left(\left(I_{out}+\Delta i_{L1}\right)\cdot\frac{n_3}{n_1}+\Delta i_{Lm}\right)$	$\left(I_{out}+\Delta i_{L1}\right)$
Turn-on switched current (i_{on})	$\left(\left(I_{out}-\Delta i_{L1}\right)\cdot\frac{n_3}{n_1}-\Delta i_{Lm}\right)$	—
Turn-off switched current (i_{off})	$\left(\left(I_{out}+\Delta i_{L1}\right)\cdot\frac{n_3}{n_1}+\Delta i_{Lm}\right)$	$\frac{\left(I_{out}-\Delta i_{L1}\right)}{2}$
Maximum voltage (v_{max})	$2\cdot\left(V_{in}+\Delta v_{Cin}\right)$	$\left(V_{in}+\Delta v_{Cin}\right)\cdot\frac{n_3}{n_1}$
Turn-on switched voltage (v_{on})	$\left(V_{in}+\Delta v_{Cin}\right)$	—
Turn-off switched voltage (v_{off})	$\left(V_{in}-\Delta v_{Cin}\right)$	$\left(V_{in}+\Delta v_{Cin}\right)\cdot\frac{n_3}{n_1}$

Thus, average conduction power losses of transistor S_1 (P_{cond_S1}) and diode D_1 (P_{cond_D1}) are derived from Table 3.22 and Eq. (3.1):

$$P_{cond\_S1} = V_{th} \cdot \frac{I_{in}}{2} + r_d \cdot \left[\left(I_{out} \cdot \frac{n_3}{n_1} \right)^2 + \frac{\left(\Delta i_{Lm} + \Delta i_{L1} \cdot \frac{n_3}{n_1} \right)^2}{3} \right] \cdot \delta \tag{3.158}$$

$$\begin{aligned} P_{cond\_D1} &= V_{th} \cdot \frac{I_{out}}{2} + \\ &+ r_d \cdot \left[(1 + 2 \cdot \delta) \cdot \left[\left(\frac{I_{out}}{2} \right)^2 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L1}}{2} \right)^2 \right] + (1 - 2 \cdot \delta) \cdot \left(\frac{\Delta i_{Lm}}{2} \cdot \frac{n_1}{n_3} \right)^2 \right] \end{aligned} \tag{3.159}$$

where r_d and V_{th} are respectively each semiconductor's on-state resistance and threshold voltage.

On the other hand, average switching power losses of the transistor S_1 (P_{sw_S1}) and diode D_1 (P_{sw_D1}) are derived from Table 3.22 and Eq. (3.2):

$$\begin{aligned} P_{sw\_S1} = &\frac{(V_{in} - \Delta v_{Cin})}{T_{sw} \cdot V_{100FIT}} \cdot \left(\begin{array}{l} A_{off,S1} \cdot \left((I_{out} + \Delta i_{L1}) \cdot \frac{n_3}{n_1} + \Delta i_{Lm} \right)^2 + \\ + B_{off,S1} \cdot \left((I_{out} + \Delta i_{L1}) \cdot \frac{n_3}{n_1} + \Delta i_{Lm} \right) + C_{off,S1} \end{array} \right) + \\ &+ \frac{(V_{in} + \Delta v_{Cin})}{T_{sw} \cdot V_{100FIT}} \cdot \left(\begin{array}{l} A_{on,S1} \cdot \left((I_{out} - \Delta i_{L1}) \cdot \frac{n_3}{n_1} - \Delta i_{Lm} \right)^2 + \\ + B_{on,S1} \cdot \left((I_{out} - \Delta i_{L1}) \cdot \frac{n_3}{n_1} - \Delta i_{Lm} \right) + C_{on,S1} \end{array} \right) \end{aligned} \tag{3.160}$$

$$P_{sw\_D1} = \frac{(V_{in} + \Delta v_{Cin}) \cdot \frac{n_3}{n_1}}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,D1} \cdot \frac{(I_{out} - \Delta i_{L1})^2}{4} + B_{off,D1} \cdot \frac{(I_{out} - \Delta i_{L1})}{2} + C_{off,D1} \right) \tag{3.161}$$

where $A_{off,XX}$, $B_{off,XX}$ and $C_{off,XX}$ are the turn-off energy loss characteristic coefficients provided by the manufacturer for the 100FIT test voltage (V_{100FIT}) of each semiconductor switch and $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are the turn-on energy loss characteristic coefficients of the transistors.

2.2.11 Push-pull isolated-boost

The push-pull isolated-boost converter is a unidirectional step-up converter. As it can be noticed in Fig 3.45, the converter is formed of two transistors at the input side (S_1-S_2) and a diode bridge at the output side (D_1-D_2-D_3-D_4). In turn, it requires a DC bus capacitor (C_{in}) and an inductor (L_1) in the input side, a medium frequency transformer with three windings and an output filter capacitor (C_{out}).

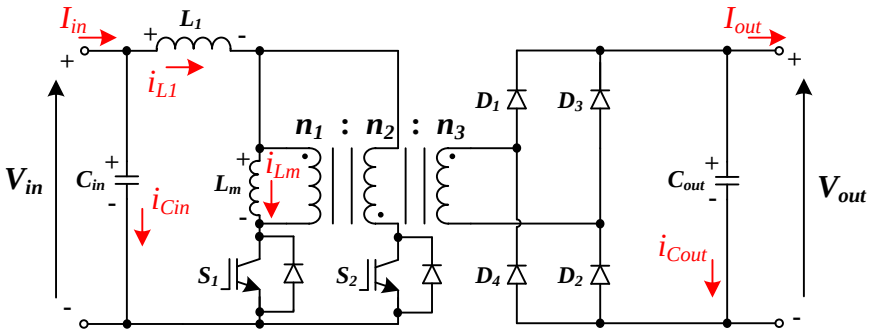
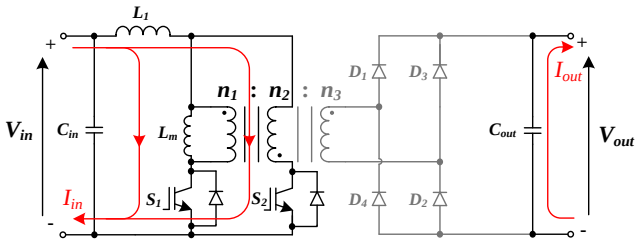


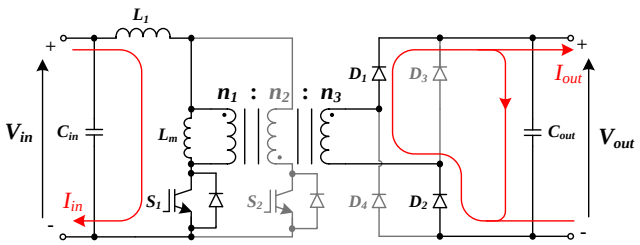
Fig 3.45. Push-pull isolated-boost converter.

2.2.11.1 Converter design

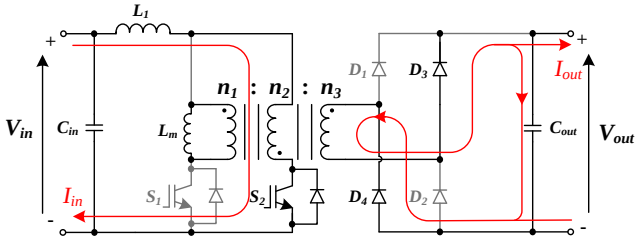
The operation of the converter is similar to that of a boost converter. The energy coming from the input is stored in the inductor L_1 and then, transferred to the output. This way, when transistors S_1 and S_2 are on (T_{on} time interval), the energy coming from the input is stored in the inductor L_1 and the current through the magnetizing inductance remains constant (cf. Fig 3.46a). Meanwhile, the output capacitor C_{out} supplies the load. Next, transistor S_2 is turned-off and, during the T_{off} time interval (cf. Fig 3.46b), the energy coming from the input as well as the energy stored in L_1 are transferred to the output capacitor and the load. In turn, the transformer is magnetized positively.



a)



b)



c)

Fig 3.46. Currents circulating through the push-pull isolated-boost converter a) when S_1 and S_2 are on, b) when S_1 is on and S_2 is off, and c) when S_1 is off and S_2 is on.

Subsequently, transistor S_2 is turned-on and a new T_{on} time interval begins (cf. Fig 3.46a) until transistor S_1 is turned-off. Then, a second T_{off} time interval begins and the transformer is magnetized negatively (cf. Fig 3.46c). As the transformer is magnetized bidirectionally, its utilization is good. However, it requires to control the average voltage applied to it so as to avoid the saturation of the core.

Although the leakage inductance of the MFT has been neglected in this analysis, this parasitic inductance has to be considered in real cases. With the described operation, the current circulating through it is interrupted and in consequence, the voltage drop over it will increase suddenly. This voltage will appear over transistors increasing their voltage stress. Therefore, in real cases, snubber circuits must be considered in order to protect the transistors.

Assuming the number of turns of the windings n_1 and n_2 are equal, the currents and voltages in a push-pull isolated-boost converter with a CCM operation are depicted in Fig 3.47. For simplicity, the voltage ripple have been neglected in Fig 3.47a and Fig 3.47b. For the same reason, the current ripple have been neglected in Fig 3.47c.

As it can be deduced from Fig 3.47a, the maximum period of time in which both transistors are on is $T_{sw}/2$. If this limit is exceeded, the transformer is not magnetized equally in both senses and in consequence, the core is saturated. Therefore, the maximum duty cycle of the converter is given by:

$$T_{on,\max} = \frac{T_{sw}}{2} \rightarrow \delta_{\max} = \frac{1}{2} \tag{3.162}$$

where $\delta_{\max}$ is the maximum duty cycle of the converter ($T_{on,\max}/T_{sw}$).

The DC voltage transfer function is derived from the steady state analysis of the waveforms of Fig 3.47b:

$$V_{out} = \frac{V_{in}}{1-2\cdot\delta}\cdot\frac{n_3}{n_1} \tag{3.163}$$

where V_{in} and V_{out} are the average input and output voltages respectively, δ is the duty cycle of the converter and n_3 represents the number of turns of the secondary winding of the MFT (cf. Fig 3.45).

In turn, from the steady state analysis of the waveforms in Fig 3.47c, the DC current transfer function is given by:

$$I_{out} = (1-2\cdot\delta)\cdot I_{in}\cdot\frac{n_1}{n_3} \tag{3.164}$$

where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.45).

The values of the magnetizing inductance L_m, Eq. (3.165), and the output side inductor L_1, Eq. (3.166), are obtained from the steady state analysis of the waveforms of Fig 3.47a and Fig 3.47b respectively.

$$L_m = v_{Lm} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{out}}{4 \cdot \Delta i_{Lm}} \cdot \frac{n_1}{n_3} \cdot (1 - 2 \cdot \delta) \cdot T_{sw} \tag{3.165}$$

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L1}} \cdot \delta \cdot T_{sw} \tag{3.166}$$

where Δi_{Lm} is the current ripple in L_m and Δi_{L1} is the current ripple in L_1.

Similarly, the capacitance value of C_{out} is derived from the steady state analysis of the waveforms in Fig 3.47c:

$$C_{out} = i_{Cout} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{C1}} \cdot \delta \cdot T_{sw} \tag{3.167}$$

where Δv_{Cout} is the desired output voltage ripple.

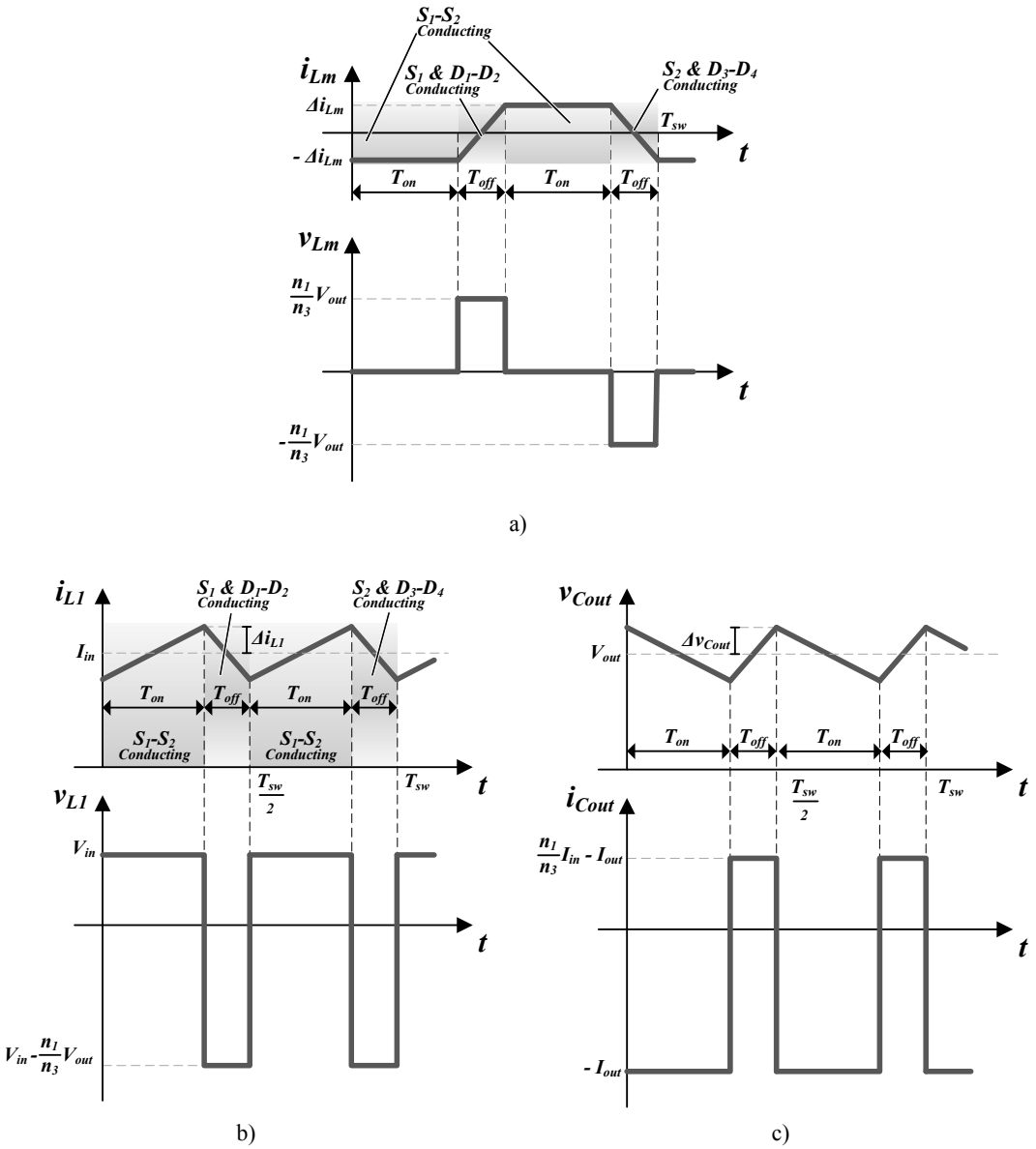


Fig 3.47. Typical voltage and current waveforms in push-pull isolated-boost converter's a) magnetizing inductance L_m, b) inductor L_1 and c) capacitor C_{out}.

The input DC bus capacitance can be derived from Fig 3.48. As it can be noticed, assuming the input current I_{in} is constant, the current through the input capacitor is dependent to the ripple in L_1. Therefore, C_{in} capacitance is given by:

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{\Delta i_{L1}}{16 \cdot \Delta v_{Cin}} \cdot T_{sw} \tag{3.168}$$

where Δv_{Cin} is the half of the desired peak to peak input voltage ripple.

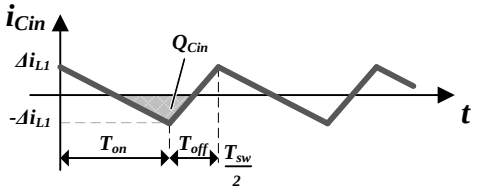


Fig 3.48. Current through the input capacitor of the push-pull isolated-boost converter.

The equations of the maximum energy stored by the passive elements, their maximum voltage stress and the *rms* currents circulating through them are derived from the waveforms of Fig 3.47 and Fig 3.48. These expressions are outlined in Table 3.23.

TABLE 3.23

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2} \cdot C_{in} \cdot \left(V_{in} + \Delta v_{Cin}\right)^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$\left(V_{in} + \Delta v_{Cin}\right)$
L_m	$\frac{1}{2} \cdot L_m \cdot \Delta i_{Lm}{}^2$	$\Delta i_{Lm} \cdot \sqrt{\frac{1+4 \cdot \delta}{3}}$	$\left(V_{out} + \Delta v_{Cout}\right) \cdot \frac{n_1}{n_3}$
L_1	$\frac{1}{2} \cdot L_1 \cdot \left(I_{in} + \Delta i_{L1}\right)^2$	$\sqrt{I_{in}{}^2 + \frac{\Delta i_{L1}{}^2}{3}}$	$\left(V_{in} + \Delta v_{Cin}\right)$
C_{out}	$\frac{1}{2} \cdot C_{out} \cdot \left(V_{out} + \Delta v_{Cout}\right)^2$	$\sqrt{2 \cdot \delta \cdot I_{out}{}^2 + \left(1-2 \cdot \delta\right) \cdot \left(I_{in} \cdot \frac{n_1}{n_3} - I_{out}\right)^2}$	$\left(V_{out} + \Delta v_{Cout}\right)$

Last, in order to select the appropriate operational point for the design, the semiconductor utilization factor (U_f) is calculated from the voltage and current expressions of Table 3.24:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{1-2 \cdot \delta}{4 \cdot \left(\sqrt{\frac{1-\delta}{2}} + \sqrt{\frac{1-2 \cdot \delta}{2}}\right)} \tag{3.169}$$

As illustrated in Fig 3.49, the lower the duty cycle the better the semiconductor utilization. Hence, n_2/n_1 turn ratio must be chosen to make sure the converter operates with low duty cycle values.

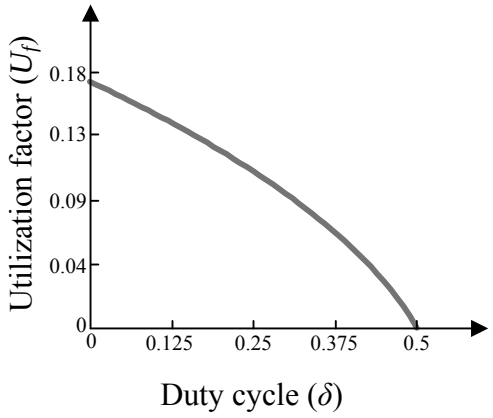


Fig 3.49. Semiconductor utilization factor of the push-pull isolated-boost converter.

2.2.11.2 Power losses estimation

As transistors S_1 and S_2 conduct the same current, their average power losses are the same. This is also applicable to output side rectifier diodes D_1-D_2-D_3-D_4. Therefore, power losses expressions are calculated just for one semiconductor in each group. The semiconductor power losses depend on conduction power losses of Eq. (3.1) and switching power losses of Eq. (3.2). Table 3.24 summarizes the current expressions (average, *rms* and switched currents) as well as the switched voltage expressions required to calculate the mentioned power losses.

Thus, average conduction power losses of transistor S_1 (P_{cond_S1}) and diode D_1 (P_{cond_D1}) are given by:

$$P_{cond\_S1} = V_{th} \cdot \frac{I_{in}}{2} + r_d \cdot \left[{I_{in}}^2 \cdot \frac{(1-\delta)}{2} + \delta \cdot \left(\frac{{\Delta i_{Lm}}^2}{2} + \frac{{\Delta i_{L1}}^2}{6} \right) + \left(\frac{1}{2} - \delta \right) \cdot \frac{{\Delta i_{L1}}^2}{3} \right] \tag{3.170}$$

$$P_{cond\_D1} = V_{th} \cdot \frac{I_{out}}{2} + r_d \cdot \left[\left(I_{in} \cdot \frac{n_1}{n_3} \right)^2 + \left(\frac{n_1}{n_3} \right)^2 \cdot \frac{(\Delta i_{Lm} + \Delta i_{L1})^2}{3} \right] \cdot \left(\frac{1}{2} - \delta \right) \tag{3.171}$$

where r_d and V_{th} are each semiconductor's on-state resistance and threshold voltage.

TABLE 3.24
EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistors S_1-S_2**	**Diodes D_1-D_2-D_3-D_4**
Average current (I_{ave})	$\frac{I_{in}}{2}$	$\frac{I_{out}}{2}$
rms current (I_{rms})	$\sqrt{\left[I_{in}{}^2 \cdot \frac{(1-\delta)}{2} + \delta \cdot \left(\frac{\Delta i_{Lm}{}^2}{2} + \frac{\Delta i_{L1}{}^2}{6} \right) + \left(\frac{1}{2} - \delta \right) \cdot \frac{\Delta i_{L1}{}^2}{3} \right]}$	$\sqrt{\left[\left(I_{in} \cdot \frac{n_1}{n_3} \right)^2 + \left(\frac{n_1}{n_3} \right)^2 \cdot \frac{(\Delta i_{Lm} + \Delta i_{L1})^2}{3} \right] \cdot \left(\frac{1}{2} - \delta \right)}$
Maximum current (i_{max})	$\left(I_{in} + \Delta i_{L1} \right)$	$\left(I_{in} + \Delta i_{L1} + \Delta i_{Lm} \right) \cdot \frac{n_1}{n_3}$
Turn-on switched current (i_{on})	$\frac{\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right)}{2}$	—
Turn-off switched current (i_{off})	$\frac{\left(I_{in} + \Delta i_{L1} + \Delta i_{Lm} \right)}{2}$	$\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right) \cdot \frac{n_1}{n_3}$
Maximum voltage (v_{max})	$2 \cdot \left(V_{out} + \Delta v_{Cout} \right) \cdot \frac{n_1}{n_3}$	$\left(V_{out} + \Delta v_{Cout} \right)$
Turn-on switched voltage (v_{on})	$2 \cdot \left(V_{out} + \Delta v_{Cout} \right) \cdot \frac{n_1}{n_3}$	—
Turn-off switched voltage (v_{off})	$2 \cdot \left(V_{out} - \Delta v_{Cout} \right) \cdot \frac{n_1}{n_3}$	$\frac{\left(V_{out} + \Delta v_{Cout} \right)}{2}$

In turn, average switching power losses of the transistor S_1 (P_{sw_S1}) and diode D_1 (P_{sw_D1}) are provided by:

$$P_{sw\_S1} = \frac{2 \cdot \left(V_{out} - \Delta v_{Cout} \right) \cdot \frac{n_1}{n_3}}{T_{sw} \cdot V_{100FIT}} \cdot \left(\begin{array}{l} A_{off,S1} \cdot \left(\frac{\left(I_{in} + \Delta i_{L1} + \Delta i_{Lm} \right)}{2} \right)^2 + \\ + B_{off,S1} \cdot \frac{\left(I_{in} + \Delta i_{L1} + \Delta i_{Lm} \right)}{2} + C_{off,S1} \end{array} \right) + \\ + \frac{2 \cdot \left(V_{out} + \Delta v_{Cout} \right) \cdot \frac{n_1}{n_3}}{T_{sw} \cdot V_{100FIT}} \cdot \left(\begin{array}{l} A_{on,S1} \cdot \left(\frac{\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right)}{2} \right)^2 + \\ + B_{on,S1} \cdot \frac{\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right)}{2} + C_{on,S1} \end{array} \right) \quad (3.172)$$

$$P_{sw\_D1} = \frac{\left(V_{out} + \Delta v_{Cout} \right)}{2 \cdot T_{sw} \cdot V_{100FIT}} \cdot \left(\begin{array}{l} A_{off,D1} \cdot \left(\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right) \cdot \frac{n_1}{n_3} \right)^2 + \\ + B_{off,D1} \cdot \left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right) \cdot \frac{n_1}{n_3} + C_{off,D1} \end{array} \right) \quad (3.173)$$

where $A_{off,XX}$, $B_{off,XX}$ and $C_{off,XX}$ are the turn-off energy loss characteristic coefficients provided by the manufacturer for the 100FIT test voltage (V_{100FIT}) of each semiconductor

switch and $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are transistors' turn-on energy loss characteristic coefficients.

2.2.12 Half-bridge

The half-bridge converter is a unidirectional converter derived from buck converter. As it can be noticed in Fig 3.50, the converter is composed of two series connected input capacitors (C_{in1} and C_{in2}), two transistors (S_1-S_2), a medium frequency transformer (in which the leakage inductances have been neglected), a diode bridge (D_1-D_2-D_3-D_4) and a LC filter at the output (inductor L_1 and capacitor C_{out}).

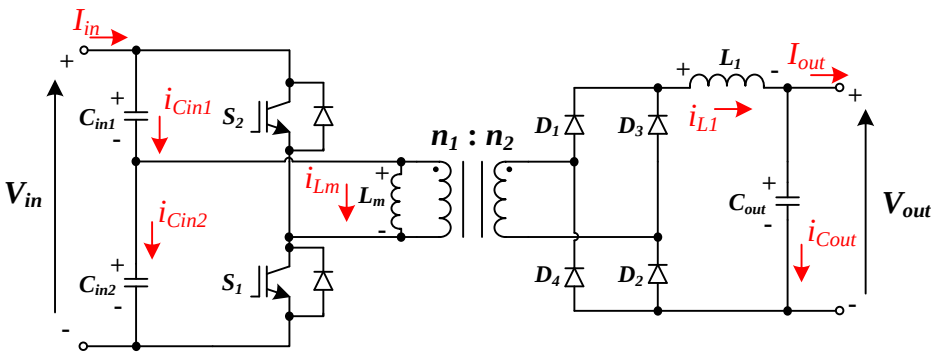


Fig 3.50. Half-bridge converter.

2.2.12.1 Converter design

As it can be noticed in Fig 3.51, the half-bridge converter operates alternating the switching orders of the transistors S_1 and S_2. Thus, when transistor S_1 is on (T_{on} time interval), transistor S_2 is off (cf. Fig 3.51a). During this time interval, the input current (I_{in}) flows through the upper capacitor C_{in1} and the energy coming from input as well as the energy stored in the lower capacitor C_{in2} are transferred to the output and the inductor L_1. At the same time, the inductance L_m is magnetized positively. After this T_{on} time interval, transistor S_1 is turned-off and the input current circulates through the two input side capacitors while the load is supplied by the output side inductor L_1 (T_{off} time interval illustrated in Fig 3.51b). During this time interval, the current through the magnetizing inductance remain constant and circulates through the diodes of the output side rectifier. When transistor S_2 is turned-on (cf. Fig 3.51c) a second T_{on} time interval begins. Thus, the input current circulates through the lower capacitor C_{in2} and the energy coming from the input as well as the energy stored in the upper capacitor C_{in1} are transferred to the load and the inductor L_1.

The voltage of each input capacitor is half of the DC bus voltage. Thus, the voltage applied to the MFT is half of the DC bus voltage (cf. Fig 3.52a). As a consequence, the current through the input side of the converter is higher than that of the converters where the entire DC bus voltage is applied to the transformer.

It must be highlighted that the leakage and magnetizing inductances of the MFT and the input capacitors of the converter conform a resonant circuit. So, in order to avoid undesired current and voltage oscillations, this phenomena must be taken into account in the design and the selection of the switching frequency of the converter.

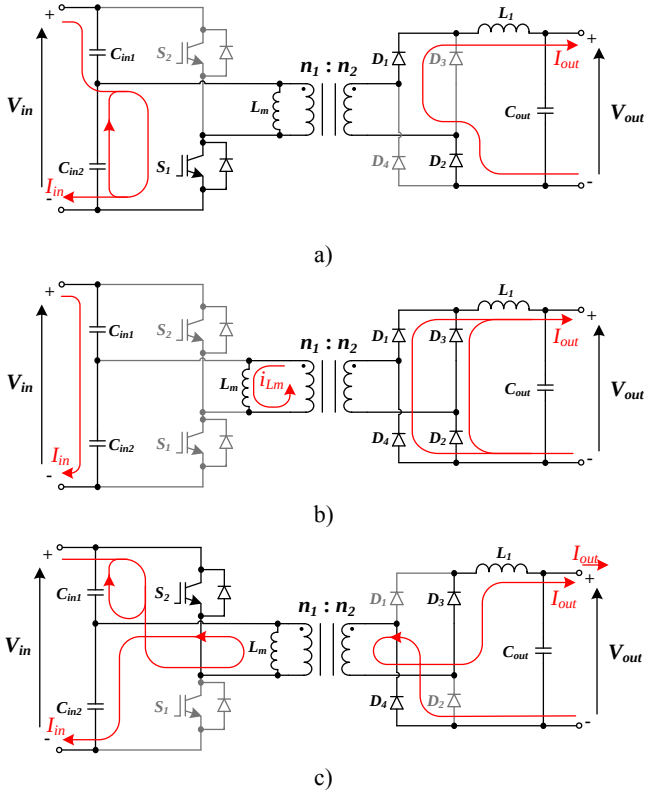


Fig 3.51. Currents circulating through the half-bridge converter a) when S_1 is on and S_2 is off, b) when S_1-S_2 are off and c)when S_1 is off and S_2 is on.

Considering a continuous current mode operation and neglecting input and output voltage ripple, the waveforms in the converter derived from this operation are illustrated in Fig 3.52. Fig 3.52a shows, the utilization of the transformer is good as it is magnetized bidirectionally. However, the T_{on} time interval cannot be higher than half of the switching period ($T_{sw}/2$), otherwise, the transformer core will be saturated, Eq. (3.174). Thus, the control scheme in the converter must avoid the transformer's core saturation.

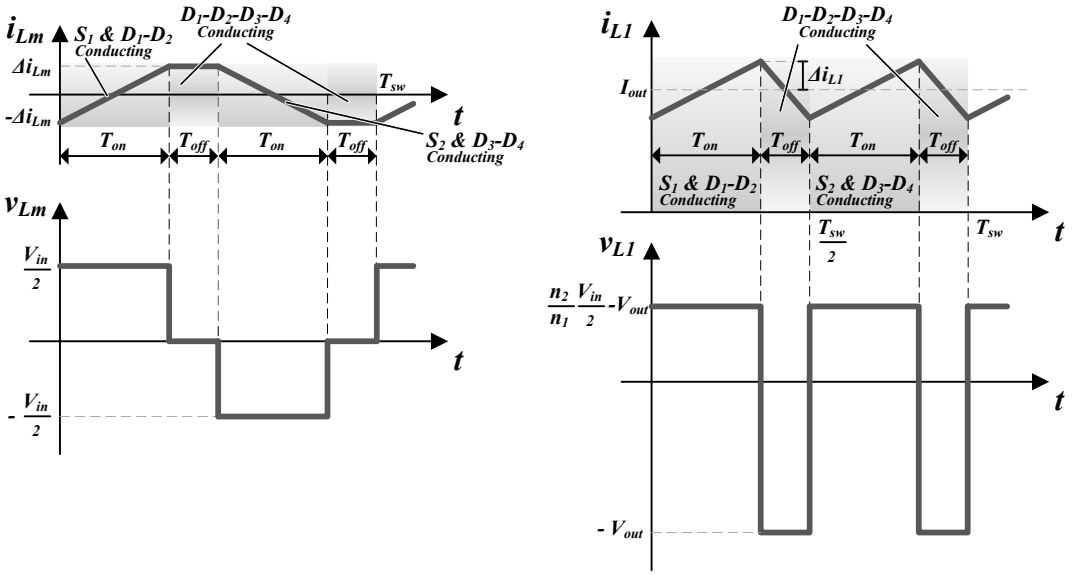
$$T_{on,\max} = \frac{T_{sw}}{2} \rightarrow \delta_{\max} = \frac{1}{2} \tag{3.174}$$

where $\delta_{\max}$ is the maximum duty cycle of the converter ($T_{on,\max}/T_{sw}$).

Assuming the average voltage applied to inductor L_1 within a switching period is zero, the DC voltage transfer function can be derived from the waveforms of Fig 3.52b:

$$V_{out} = V_{in} \cdot \delta \cdot \frac{n_2}{n_1} \tag{3.175}$$

where V_{in} and V_{out} are the average input and output voltages respectively, δ is the duty cycle of the converter and n_2/n_1 is the turn ratio of the MFT (cf. Fig 3.50).



a) b)

Fig 3.52. Typical voltage and current waveforms in half-bridge converter's a) L_m magnetizing inductance and b) inductor L_1.

Moreover, assuming ideal operation with no losses, the DC current transfer function is given by:

$$\left.\begin{aligned} V_{in}\cdot I_{in} &= V_{out}\cdot I_{out} \\ V_{out} &= V_{in}\cdot\delta\cdot\frac{n_2}{n_1} \end{aligned}\right\} \rightarrow I_{out} = \frac{I_{in}}{\delta}\cdot\frac{n_1}{n_2} \tag{3.176}$$

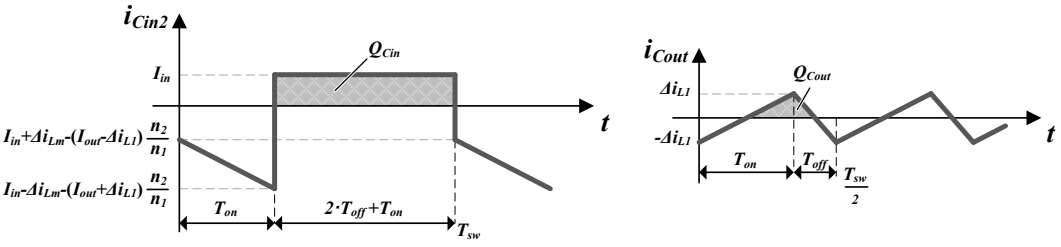
where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.50).

On the other hand, the inductances of L_m and L_1 can be derived from the waveforms in Fig 3.52:

$$L_m = v_{Lm}\cdot\frac{\Delta t}{\Delta i} = \frac{V_{in}}{4\cdot\Delta i_{Lm}}\cdot\delta\cdot T_{sw} \tag{3.177}$$

$$L_1 = v_{L1}\cdot\frac{\Delta t}{\Delta i} = \frac{V_{out}}{4\cdot\Delta i_{L1}}\cdot(1-2\cdot\delta)\cdot T_{sw} \tag{3.178}$$

where Δi_{Lm} is the current ripple in L_m and Δi_{L1} is the current ripple in L_1.



a) b)

Fig 3.53. Currents circulating through a) the input capacitor and b) the output capacitor of the half-bridge converter.

The current flowing in each input DC bus capacitor is the same and in consequence, their capacitance is equal. Under the assumption of constant input and output currents (I_{in} and I_{out}), the currents through input and output capacitors can be depicted as in Fig 3.53.

Thus, from Fig 3.53a, the capacitance of the lower capacitor C_{in2} is derived:

$$C_{in2} = \frac{Q_{Cin2}}{\Delta v} = \frac{I_{in} \cdot (T_{sw} - T_{on})}{2 \cdot \Delta v_{Cin2}} \tag{3.179}$$

where Δv_{Cin2} is the half of the desired peak to peak voltage ripple in the capacitor C_{in2}.

The capacitance of C_{out} is obtained similarly from Fig 3.53b:

$$C_{out} = \frac{Q_{Cout}}{\Delta v} = \frac{\Delta i_{L1}}{16 \cdot \Delta v_{Cout}} \cdot T_{sw} \tag{3.180}$$

where Δv_{Cout} is the half of the desired peak to peak voltage ripple in the output.

Table 3.25 summarizes the expressions of the maximum energy stored by the passive elements, their maximum voltage stress and the *rms* currents circulating through them. These expressions are derived from the waveforms of Fig 3.52 and Fig 3.53.

TABLE 3.25

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in2}	$\frac{1}{2} \cdot C_{in} \cdot \left(\frac{V_{in}}{2} + \Delta v_{Cin2} \right)^2$	$\sqrt{\delta \cdot \chi + (1-\delta) \cdot {I_{in}}^2}$	$\left(\frac{V_{in}}{2} + \Delta v_{Cin2} \right)$
L_m	$\frac{1}{2} \cdot L_m \cdot {\Delta i_{Lm}}^2$	$\Delta i_{Lm} \cdot \sqrt{1 - \frac{4 \cdot \delta}{3}}$	$\left(\frac{V_{in}}{2} + \Delta v_{Cin2} \right)$
L_1	$\frac{1}{2} \cdot L_1 \cdot (I_{out} + \Delta i_{L1})^2$	$\sqrt{{I_{out}}^2 + \frac{{\Delta i_{L1}}^2}{3}}$	$(V_{out} + \Delta v_{Cout})$
C_{out}	$\frac{1}{2} \cdot C_{out} \cdot (V_{out} + \Delta v_{Cout})^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$(V_{out} + \Delta v_{Cout})$
$\chi = \left(\left(I_{in} - I_{out} \cdot \frac{n_2}{n_1} \right)^2 + \frac{\left(\Delta i_{L1} \cdot \frac{n_2}{n_1} + \Delta i_{Lm} \right)^2}{3} \right)$			

At last, derived from the maximum voltage and *rms* current expressions of Table 3.26, the semiconductor utilization factor (U_f) is given by:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{\delta}{2 \cdot \sqrt{\delta} + \sqrt{1 - 2 \cdot \delta}} \tag{3.181}$$

As it can be noticed, this semiconductor utilization factor is same as that presented for the push-pull converter (section 3.2.10). Therefore, the higher the duty cycle the better the semiconductor utilization (cf. Fig 3.44). Hence, the chosen turn ratio of the transformer must ensure that the converter operates with high duty cycles close to 0.5.

2.2.12.2 Power losses estimation

As mentioned in the beginning of section 3.2, semiconductor power losses are estimated by Eq. (3.1) and Eq. (3.2). In order to estimate these losses, the expressions of the currents and voltages in the semiconductors are outlined in Table 3.26. Provided that the currents circulating through the transistors are the same and that the currents circulating through the output diodes are the same, power losses are calculated only for one semiconductor in each group.

TABLE 3.26

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistors S_1-S_2**	**Diodes D_1-D_2-D_3-D_4**
Average current (I_{ave})	I_{in}	$\frac{I_{out}}{2}$
rms current (I_{rms})	$\sqrt{\left[\left(I_{out}\cdot\frac{n_2}{n_1}\right)^2+\frac{\left(\Delta i_{Lm}+\Delta i_{L1}\cdot\frac{n_2}{n_1}\right)^2}{3}\right]\cdot\delta}$	$\sqrt{(1+2\cdot\delta)\cdot\left[\left(\frac{I_{out}}{2}\right)^2+\frac{1}{3}\cdot\left(\frac{\Delta i_{L1}}{2}\right)^2\right]+(1-2\cdot\delta)\cdot\left(\frac{\Delta i_{Lm}}{2}\cdot\frac{n_1}{n_2}\right)^2}$
Maximum current (i_{max})	$\left(\left(I_{out}+\Delta i_{L1}\right)\cdot\frac{n_2}{n_1}+\Delta i_{Lm}\right)$	$\left(I_{out}+\Delta i_{L1}\right)$
Turn-on switched current (i_{on})	$\left(\left(I_{out}-\Delta i_{L1}\right)\cdot\frac{n_2}{n_1}-\Delta i_{Lm}\right)$	—
Turn-off switched current (i_{off})	$\left(\left(I_{out}+\Delta i_{L1}\right)\cdot\frac{n_3}{n_1}+\Delta i_{Lm}\right)$	$\frac{\left(I_{out}-\Delta i_{L1}\right)}{2}$
Maximum voltage (v_{max})	$\approx\left(V_{in}+\Delta v_{Cin2}\right)$	$\left(\frac{V_{in}}{2}+\Delta v_{Cin2}\right)\cdot\frac{n_2}{n_1}$
Turn-on switched voltage (v_{on})	$\left(\frac{V_{in}}{2}+\Delta v_{Cin2}\right)$	—
Turn-off switched voltage (v_{off})	$\left(\frac{V_{in}}{2}-\Delta v_{Cin2}\right)$	$\left(\frac{V_{in}}{2}+\Delta v_{Cin2}\right)\cdot\frac{n_2}{n_1}$

Consequently, average conduction power losses of transistor S_1 (P_{cond_S1}) and diode D_1 (P_{cond_D1}) are given by:

$$P_{cond\_S1} = V_{th} \cdot I_{in} + r_d \cdot \left[\left(I_{out} \cdot \frac{n_2}{n_1} \right)^2 + \frac{\left(\Delta i_{Lm} + \Delta i_{L1} \cdot \frac{n_2}{n_1} \right)^2}{3} \right] \cdot \delta \tag{3.182}$$

$$\begin{aligned} P_{cond\_D1} &= V_{th} \cdot \frac{I_{out}}{2} + \\ &+ r_d \cdot \left[\left(1 + 2 \cdot \delta\right) \cdot \left[\left(\frac{I_{out}}{2} \right)^2 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L1}}{2} \right)^2 \right] + \left(1 - 2 \cdot \delta\right) \cdot \left(\frac{\Delta i_{Lm}}{2} \cdot \frac{n_1}{n_2} \right)^2 \right] \end{aligned} \tag{3.183}$$

where r_d is the on-state resistance and V_{th} is the threshold voltage.

Moreover, average switching power losses of the transistor S_1 (P_{sw_S1}) and diode D_1 (P_{sw_D1}) are given by:

$$\begin{aligned} P_{sw\_S1} = &\frac{\left(\frac{V_{in}}{2} - \Delta v_{Cin2} \right)}{T_{sw} \cdot V_{100FIT}} \cdot \left(\begin{array}{l} A_{off,S1} \cdot \left(\left(I_{out} + \Delta i_{L1}\right) \cdot \frac{n_2}{n_1} + \Delta i_{Lm} \right)^2 + \\ + B_{off,S1} \cdot \left(\left(I_{out} + \Delta i_{L1}\right) \cdot \frac{n_2}{n_1} + \Delta i_{Lm} \right) + C_{off,S1} \end{array} \right) + \\ &+ \frac{\left(\frac{V_{in}}{2} + \Delta v_{Cin2} \right)}{T_{sw} \cdot V_{100FIT}} \cdot \left(\begin{array}{l} A_{on,S1} \cdot \left(\left(I_{out} - \Delta i_{L1}\right) \cdot \frac{n_2}{n_1} - \Delta i_{Lm} \right)^2 + \\ + B_{on,S1} \cdot \left(\left(I_{out} - \Delta i_{L1}\right) \cdot \frac{n_2}{n_1} - \Delta i_{Lm} \right) + C_{on,S1} \end{array} \right) \end{aligned} \tag{3.184}$$

$$P_{sw\_D1} = \frac{\left(\frac{V_{in}}{2} + \Delta v_{Cin2} \right) \cdot \frac{n_2}{n_1}}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,D1} \cdot \frac{\left(I_{out} - \Delta i_{L1}\right)^2}{4} + B_{off,D1} \cdot \frac{\left(I_{out} - \Delta i_{L1}\right)}{2} + C_{off,D1} \right) \tag{3.185}$$

where $A_{off,XX}$, $B_{off,XX}$ and $C_{off,XX}$ are the turn-off energy loss characteristic coefficients provided by the manufacturer for the 100FIT test voltage (V_{100FIT}) of each semiconductor switch and $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are the turn-on energy loss characteristic coefficients of the transistors.

2.2.13 Half-bridge isolated-boost

The half-bridge isolated-boost converter is a unidirectional converter derived from boost type converters (cf. Fig 3.54). The converter is formed of two transistors (S_1-S_2) and a DC bus capacitor (C_{in}) at the input side, a medium frequency transformer (MFT) and a diode rectifier (D_1-D_2-D_3-D_4) as well as a capacitor (C_{out}) at the output side.

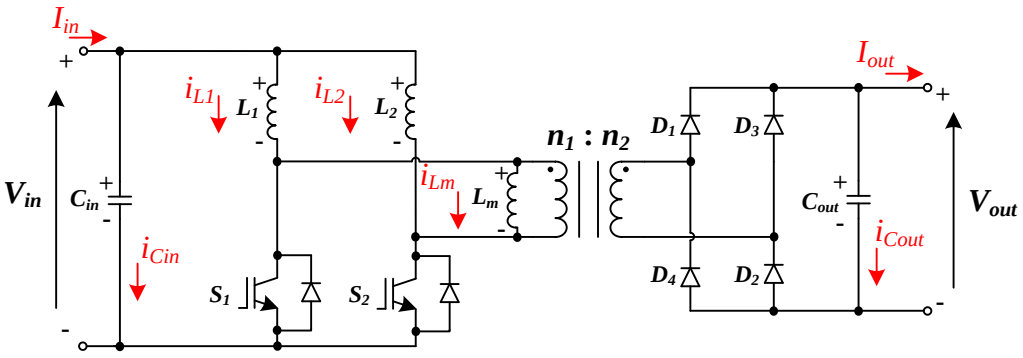


Fig 3.54. Half-bridge isolated-boost converter.

2.2.13.1 Converter design

The operation of the converter is based on alternating the transistors commands as illustrated in Fig 3.55. When transistors S_1 and S_2 are on (t_{on} time interval), the energy coming from the input is stored in the inductors L_1 and L_2 (cf. Fig 3.55a). In turn, zero voltage is applied to the MFT and in consequence, the current through the magnetizing inductance is constant. This current circulates through the transistors. During this t_{on} time interval, the load is supplied by the output capacitor C_{out}.

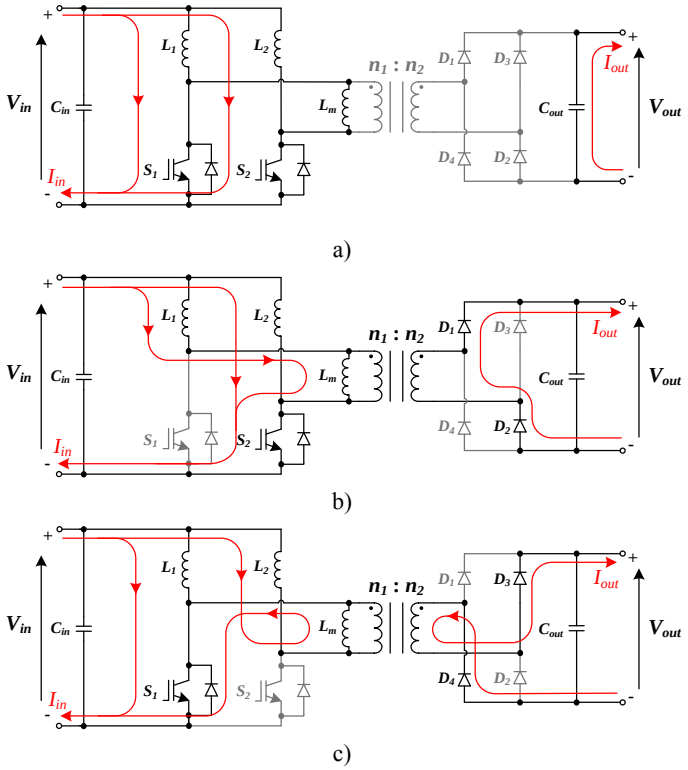


Fig 3.55. Currents circulating through the half-bridge isolated-boost converter a) when S_1 and S_2 are on, b) when S_1 is off and S_2 is on, and c) when S_1 is on and S_2 is off.

Then, transistor S_1 is turned-off and T_{off} time interval begins (cf. Fig 3.55b), where the energy stored in L_1 is transferred to the output while the transformer is magnetized

positively. Inductor L_2 continues storing energy. When transistor S_1 is turned-on the second t_{on} period of time begins (cf. Fig 3.55a). This time interval finishes when transistor S_2 is turned-off and the second T_{off} time interval begins (cf. Fig 3.55c). During the second T_{off}, the energy stored by inductor L_2 is transferred to the output and L_1 continues storing the energy coming from the input. Meanwhile, the transformer is magnetized negatively.

From this operational behaviour, it can be deduced that the on-state time interval (T_{on}) of each transistor is given by Eq. (3.186). Furthermore, this time interval must be always higher than $T_{sw}/2$, which leads to the minimum duty cycle value given by Eq. (3.187).

$$T_{on} = 2 \cdot t_{on} + T_{off} = T_{sw} - T_{off} \tag{3.186}$$

$$T_{on,\min} = \frac{T_{sw}}{2} \rightarrow \delta_{\min} = \frac{1}{2} \tag{3.187}$$

where T_{sw} is the switching period of the transistors and $\delta_{\min}$ is the minimum duty cycle of the converter ($T_{on,\min}/T_{sw}$).

The leakage inductance of the MFT has been neglected in this analysis (cf. Fig 3.54 and Fig 3.55). Nevertheless, this leakage inductance has to be considered in real cases. The described operation interrupts the current circulating through the leakage inductance and in consequence, in real cases, the voltage in the leakage inductance will raise leading to overvoltages in the transistors. To avoid these overvoltages, the use of snubber circuits must be taken under consideration.

The waveforms derived from the afore described operational behaviour are depicted in Fig 3.56. For simplicity, voltage ripple have been neglected in the waveforms related to the magnetic elements while current ripple have been neglected in the waveforms related to the output capacitor. As it can be deduced from Fig 3.56a, the transformer is magnetized bidirectionally, thereby leading to a good utilization of it. Moreover, even though the waveform shows no DC current is injected, a control scheme is required in order to avoid transformer saturation.

On the other hand, the DC voltage transfer function is obtained from the waveforms of Fig 3.56b:

$$V_{out} = \frac{V_{in}}{1-\delta} \cdot \frac{n_2}{n_1} \tag{3.188}$$

where V_{in} and V_{out} are the average input and output voltages respectively, δ is the duty cycle of the converter and n_1 and n_2 are the number of turns of the primary and secondary windings of the MFT respectively (cf. Fig 3.54).

The DC current transfer function is derived from the steady state analysis of the waveforms in Fig 3.56d:

$$I_{out} = (1-\delta) \cdot I_{in} \cdot \frac{n_1}{n_2} \tag{3.189}$$

where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.54).

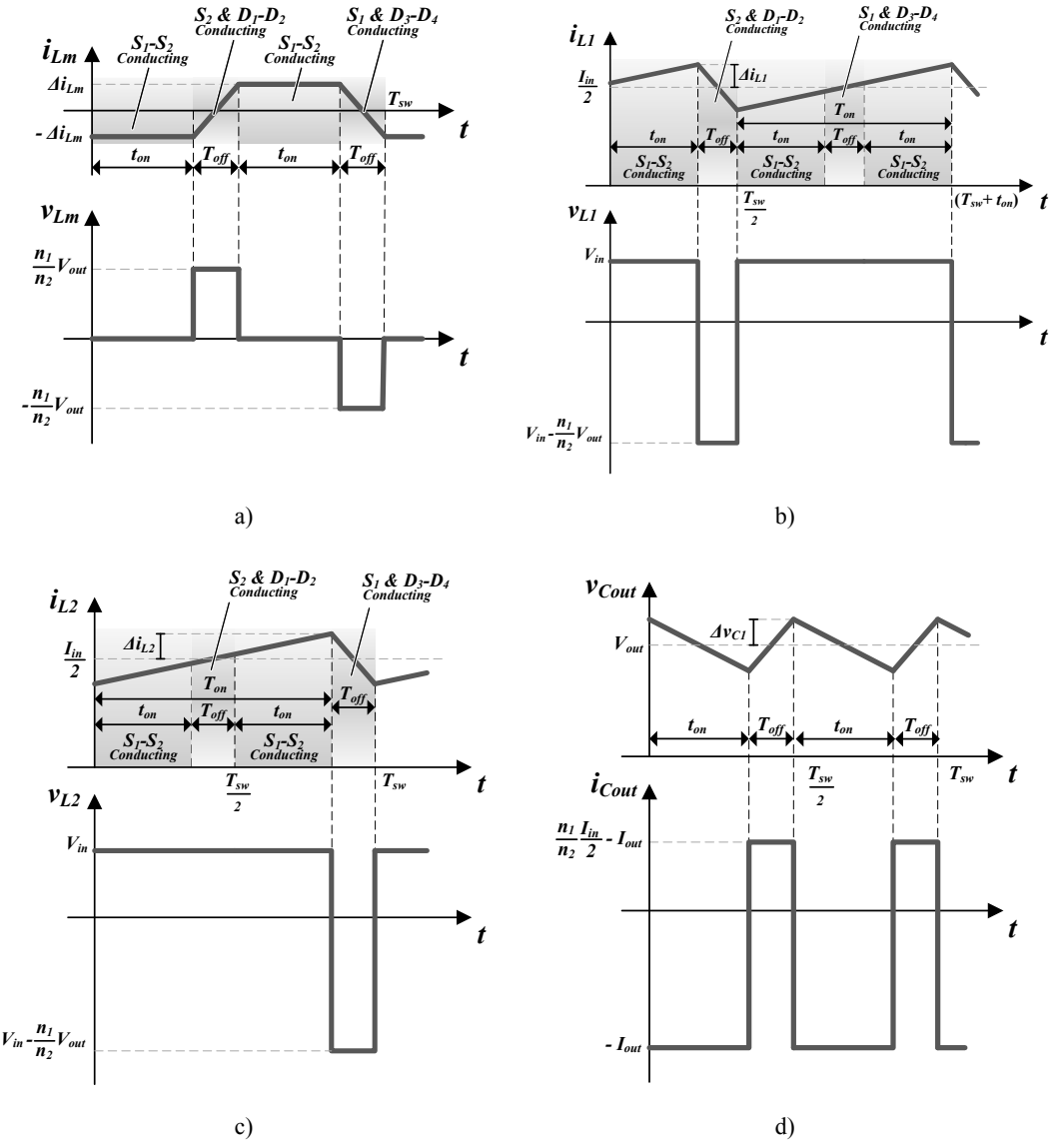


Fig 3.56. Typical voltage and current waveforms in half-bridge isolated-boost converter's a) magnetizing inductance L_m, b) inductor L_1, b) inductor L_2 and c) capacitor C_{out}.

The inductances of the input side inductors L_1 and L_2 are derived from the steady state analysis of their respective waveforms of Fig 3.56b and Fig 3.56c, while the value of the magnetizing inductance is obtained from Fig 3.56a:

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L1}} \cdot \delta \cdot T_{sw} \tag{3.190}$$

$$L_2 = v_{L2} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L2}} \cdot \delta \cdot T_{sw} \tag{3.191}$$

$$L_m = v_{Lm} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{out}}{2 \cdot \Delta i_{Lm}} \cdot \frac{n_1}{n_2} \cdot (1-\delta) \cdot T_{sw} \tag{3.192}$$

where Δi_{L1}, Δi_{L2} and Δi_{Lm} are respectively the current ripple in L_1, L_2 and L_m.

Similarly, C_{out} capacitance is derived from Fig 3.56d:

$$C_{out} = i_{Cout} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{4 \cdot \Delta v_{C1}} \cdot (2 \cdot \delta - 1) \cdot T_{sw} \tag{3.193}$$

where Δv_{Cout} is the output voltage ripple.

The current through the input capacitor C_{in} is determined by the current ripple in L_1 and L_2. Assuming the current ripple Δi_{L1} and Δi_{L2} are equal and considering the input current I_{in} is constant, the maximum current through the input capacitor is:

$$\Delta i_{in} = \Delta i_{L1} \cdot \left(2 - \frac{1}{\delta}\right) = \Delta i_{L2} \cdot \left(2 - \frac{1}{\delta}\right) \tag{3.194}$$

Therefore, the input DC bus capacitance (C_{in}) is determined by the charges Q_{Cin} illustrated in Fig 3.57:

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{\Delta i_{in}}{8 \cdot \Delta v_{Cin}} \cdot T_{sw} = \frac{\Delta i_{L1}}{16 \cdot \Delta v_{Cin}} \cdot \left(2 - \frac{1}{\delta}\right) \cdot T_{sw} \tag{3.195}$$

where Δv_{Cin} is the half of the desired peak to peak input voltage ripple.

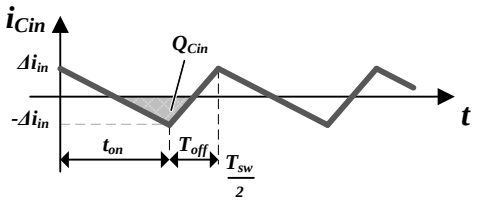


Fig 3.57. Current through the input capacitor of the half-bridge isolated-boost converter.

Table 3.27 summarizes the expressions of the maximum energy stored by the passive elements, their maximum voltage stress and the *rms* currents circulating through them. These expressions can be derived from the waveforms in Fig 3.56 and Fig 3.57.

From the maximum voltage and *rms* current expressions of Table 3.28, the semiconductor utilization factor (U_f) of the half-bridge isolated-boost converter is:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{1 - \delta}{2 \cdot \sqrt{1 - \delta} + \sqrt{3 - 2 \cdot \delta}} \tag{3.196}$$

TABLE 3.27

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2}\cdot C_{in}\cdot\left(V_{in}+\Delta v_{Cin}\right)^2$	$\frac{\Delta i_{in}}{\sqrt{3}}$	$\left(V_{in}+\Delta v_{Cin}\right)$
L_m	$\frac{1}{2}\cdot L_m\cdot {\Delta i_{Lm}}^2$	$\Delta i_{Lm}\cdot\sqrt{\frac{4\cdot\delta-1}{3}}$	$\left(V_{out}+\Delta v_{Cout}\right)\cdot\frac{n_1}{n_2}$
L_1	$\frac{1}{2}\cdot L_1\cdot\left(\frac{I_{in}}{2}+\Delta i_{L1}\right)^2$	$\sqrt{\left(\frac{I_{in}}{2}\right)^2+\frac{{\Delta i_{L1}}^2}{3}}$	$\approx\left(V_{in}-\left(V_{out}+\Delta v_{Cout}\right)\cdot\frac{n_1}{n_2}\right)$
L_2	$\frac{1}{2}\cdot L_2\cdot\left(\frac{I_{in}}{2}+\Delta i_{L2}\right)^2$	$\sqrt{\left(\frac{I_{in}}{2}\right)^2+\frac{{\Delta i_{L2}}^2}{3}}$	$\approx\left(V_{in}-\left(V_{out}+\Delta v_{Cout}\right)\cdot\frac{n_1}{n_2}\right)$
C_{out}	$\frac{1}{2}\cdot C_{out}\cdot\left(V_{out}+\Delta v_{Cout}\right)^2$	$\sqrt{\begin{matrix}\left(2\cdot\delta-1\right)\cdot {I_{out}}^2+\\+2\cdot\left(1-\delta\right)\cdot\left(\frac{I_{in}}{2}\cdot\frac{n_1}{n_2}-I_{out}\right)^2\end{matrix}}$	$\left(V_{out}+\Delta v_{Cout}\right)$

In order to determine the operational point at which the utilization factor is maximized (i.e. the installed semiconductor power is the minimum), Eq. (3.196) is depicted in Fig 3.58 for different duty cycles. As it can be noticed, the lower the duty cycle the better the semiconductor utilization. In consequence, n_2/n_1 turn ratio must be that which guarantees the operation of the converter with duty cycle values close to 0.5.

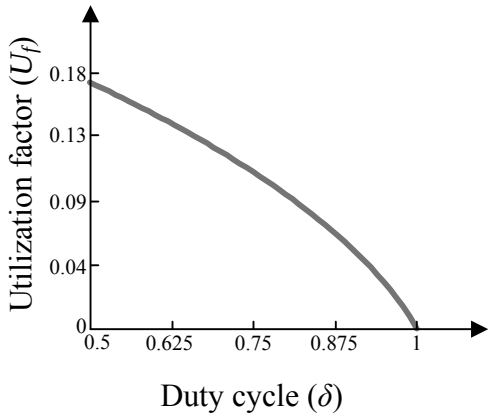


Fig 3.58. Semiconductor utilization factor of the half-bridge isolated-boost converter.

2.2.13.2 Power losses estimation

Assuming ideal passive elements with no losses, the power losses of the converter are given by the semiconductor power losses. In turn, semiconductor power losses depend on conduction power losses of Eq. (3.1) and switching power losses of Eq. (3.2). To estimate

these losses, average and *rms* currents through the semiconductors must be known along with the switched currents and voltages. Furthermore, the maximum current through them and the maximum voltage they must block determine the required semiconductor. Once the semiconductor is selected, the on-state as well as the switching characteristics are determined.

Aforementioned expressions are summarized in Table 3.28 and can be deduced from Fig 3.56. The expressions of transistors are the same because they conduct the same current. Similarly, the expressions of diodes are the same because they conduct the same current.

TABLE 3.28

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistors S_1-S_2**	**Diodes D_1-D_2-D_3-D_4**
Average current (I_{ave})	$\frac{I_{in}}{2}$	$\frac{I_{out}}{2}$
rms current (I_{rms})	$\sqrt{\chi}$	$\sqrt{\left[\left(\frac{I_{in}}{2}\cdot\frac{n_1}{n_2}\right)^2+\left(\frac{n_1}{n_2}\right)^2\cdot\frac{(\Delta i_{Lm}+\Delta i_{L1})^2}{3}\right]\cdot(1-\delta)}$
Maximum current (i_{max})	$\left(I_{in}+\Delta i_{in}\right)$	$\left(\frac{I_{in}}{2}+\Delta i_{L1}+\Delta i_{Lm}\right)\cdot\frac{n_1}{n_2}$
Turn-on switched current (i_{on})	$\left(\frac{I_{in}}{2}-\Delta i_{L1}-\Delta i_{Lm}\right)$	—
Turn-off switched current (i_{off})	$\left(\frac{I_{in}}{2}+\Delta i_{L1}+\Delta i_{Lm}\right)$	$\left(\frac{I_{in}}{2}-\Delta i_{L1}-\Delta i_{Lm}\right)\cdot\frac{n_1}{n_2}$
Maximum voltage (v_{max})	$\left(V_{out}+\Delta v_{Cout}\right)\cdot\frac{n_1}{n_2}$	$\left(V_{out}+\Delta v_{Cout}\right)$
Turn-on switched voltage (v_{on})	$\left(V_{out}+\Delta v_{Cout}\right)\cdot\frac{n_1}{n_2}$	—
Turn-off switched voltage (v_{off})	$\left(V_{out}-\Delta v_{Cout}\right)\cdot\frac{n_1}{n_2}$	$\frac{\left(V_{out}+\Delta v_{Cout}\right)}{2}$
$\chi=\left[I_{in}{}^2\cdot\frac{(3-2\cdot\delta)}{4}+(\Delta i_{L1}\cdot\Delta i_{Lm})\cdot\left(\frac{1}{\delta}-2\right)+\Delta i_{Lm}{}^2\cdot(2\cdot\delta-1)+\frac{\Delta i_{L1}{}^2}{3}\cdot\left(5-\frac{2}{\delta}-2\cdot\delta\right)\right]$		

From Table 3.28 and Eq. (3.1), average conduction power losses of transistor S_1 (P_{cond_S1}) and diode D_1 (P_{cond_D1}) are:

$$P_{cond\_S1}=V_{th}\cdot\frac{I_{in}}{2}+r_d\cdot\left[\begin{array}{l}I_{in}{}^2\cdot\frac{(3-2\cdot\delta)}{4}+(\Delta i_{L1}\cdot\Delta i_{Lm})\cdot\left(\frac{1}{\delta}-2\right)+\Delta i_{Lm}{}^2\cdot(2\cdot\delta-1)+\\+\frac{\Delta i_{L1}{}^2}{3}\cdot\left(5-\frac{2}{\delta}-2\cdot\delta\right)\end{array}\right] \tag{3.197}$$

$$P_{cond\_D1} = V_{th} \cdot \frac{I_{out}}{2} + r_d \cdot \left[\left(I_{in} \cdot \frac{n_1}{n_2} \right)^2 + \left(\frac{n_1}{n_2} \right)^2 \cdot \frac{(\Delta i_{Lm} + \Delta i_{L1})^2}{3} \right] \cdot (1 - \delta) \tag{3.198}$$

where r_d and V_{th} are each semiconductor's on-state resistance and threshold voltage respectively.

From Table 3.28 and Eq. (3.2), average switching power losses of transistor S_1 (P_{sw_S1}) and diode D_1 (P_{sw_D1}) are:

$$\begin{aligned} P_{sw\_S1} = & \frac{(V_{out} - \Delta v_{Cout}) \cdot \frac{n_1}{n_2}}{T_{sw} \cdot V_{100FIT}} \cdot \left(\begin{array}{l} A_{off,S1} \cdot \left(\frac{I_{in}}{2} + \Delta i_{L1} + \Delta i_{Lm} \right)^2 + \\ + B_{off,S1} \cdot \left(\frac{I_{in}}{2} + \Delta i_{L1} + \Delta i_{Lm} \right) + C_{off,S1} \end{array} \right) + \\ & + \frac{(V_{out} + \Delta v_{Cout}) \cdot \frac{n_1}{n_2}}{T_{sw} \cdot V_{100FIT}} \cdot \left(\begin{array}{l} A_{on,S1} \cdot \left(\frac{I_{in}}{2} - \Delta i_{L1} - \Delta i_{Lm} \right)^2 + \\ + B_{on,S1} \cdot \left(\frac{I_{in}}{2} - \Delta i_{L1} - \Delta i_{Lm} \right) + C_{on,S1} \end{array} \right) \end{aligned} \tag{3.199}$$

$$P_{sw\_D1} = \frac{(V_{out} + \Delta v_{Cout})}{2 \cdot T_{sw} \cdot V_{100FIT}} \cdot \left(\begin{array}{l} A_{off,D1} \cdot \left(\left(\frac{I_{in}}{2} - \Delta i_{L1} - \Delta i_{Lm} \right) \cdot \frac{n_1}{n_2} \right)^2 + \\ + B_{off,D1} \cdot \left(\frac{I_{in}}{2} - \Delta i_{L1} - \Delta i_{Lm} \right) \cdot \frac{n_1}{n_2} + C_{off,D1} \end{array} \right) \tag{3.200}$$

where $A_{off,XX}$, $B_{off,XX}$ and $C_{off,XX}$ are the turn-off energy loss characteristic coefficients provided by the manufacturer for the 100FIT test voltage (V_{100FIT}) of each semiconductor switch and $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are transistors' turn-on energy loss characteristic coefficients.

2.2.14 Full-bridge

The full-bridge converter of Fig 3.59 is a unidirectional step-down type converter. The converter is composed of a DC bus filter capacitor (C_{in}) and a H-bridge converter (S_1-S_2-S_3-S_4) at the input side. The H-bridge converter is connected through a medium frequency transformer to the diode bridge (D_1-D_2-D_3-D_4) and the output side LC filter (inductor L_1 and capacitor C_{out}).

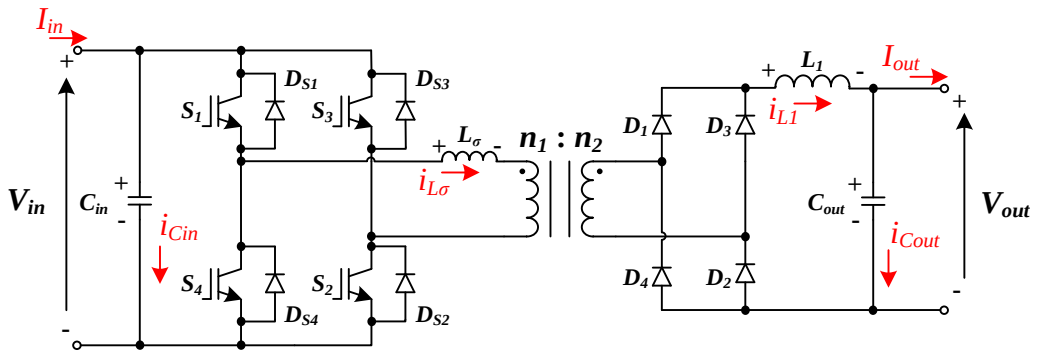


Fig 3.59. Full-bridge converter.

2.2.14.1 Converter design

For the converter design a phase-shifted pulse width modulation technique has been considered. As it can be observed in Fig 3.60, each transistor is on during half of the switching period ($T_{sw}/2$). The switching orders of transistors $S_1$and S_4, and transistors S_2 and S_3 are complementary. Furthermore, the commands of transistors S_1-S_4 are phase-shifted (φ) to that of transistors S_2-S_3. This way, three different voltage levels ($-V_{in}$, 0, V_{in}) are applied to the primary side winding of the medium frequency transformer.

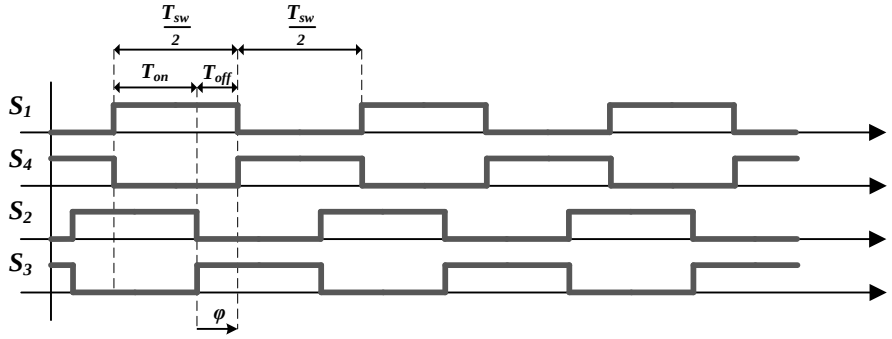


Fig 3.60. Switching orders in the full-bridge converter.

Hence, when S_1-S_2 are on and S_3-S_4 are off (t_{on} time interval), the energy coming from the input and the energy stored in C_{in} capacitor are transferred to the leakage inductance of the MFT (L_σ), the output inductor (L_1) and the load (cf. Fig 3.61a). Then, S_2 is turned-off while S_3 is turned-on (cf. Fig 3.61b). During this time interval (T_{off}), the energy coming from the input is stored in C_{in} and zero voltage is applied to the MFT. Thus, the output load is supplied by the leakage inductance and the inductor L_1. Subsequently, S_1 is turned-off and S_4 is turned-on (cf. Fig 3.61c). Therefore, input voltage is applied to the leakage inductance and the current circulating through it flows through the freewheel diodes D_{S3} and D_{S4}. The energy stored in the leakage inductance is transferred to the input side capacitor along with the energy coming from the input. Meanwhile, the load is supplied by L_1. When the current sense in the MFT is inverted (cf. Fig 3.61d), transistors S_3-S_4 start conducting current and the energy stored in the capacitor C_{in} and the energy coming from the input are transferred to L_σ, L_1 and the load (second t_{on} time interval). Next, S_3 is turned-off while S_2 is turned-on and during a T_{off} time interval (cf. Fig 3.61e), C_{in} stores the energy coming from the input while the output load is supplied by the leakage inductance and the output side inductor. During this time interval, zero voltage is applied to the MFT. Last, S_4 is turned-off and S_1 is turned-on (cf. Fig 3.61f). While the current through the leakage inductance remains negative, input voltage is applied to the leakage inductance and the current flows through the freewheel diodes D_{S1} and D_{S2}. Therefore, the energy coming from the input as well as the energy stored in the leakage inductance are transferred to the input side capacitor. The load is supplied by the output side inductor.

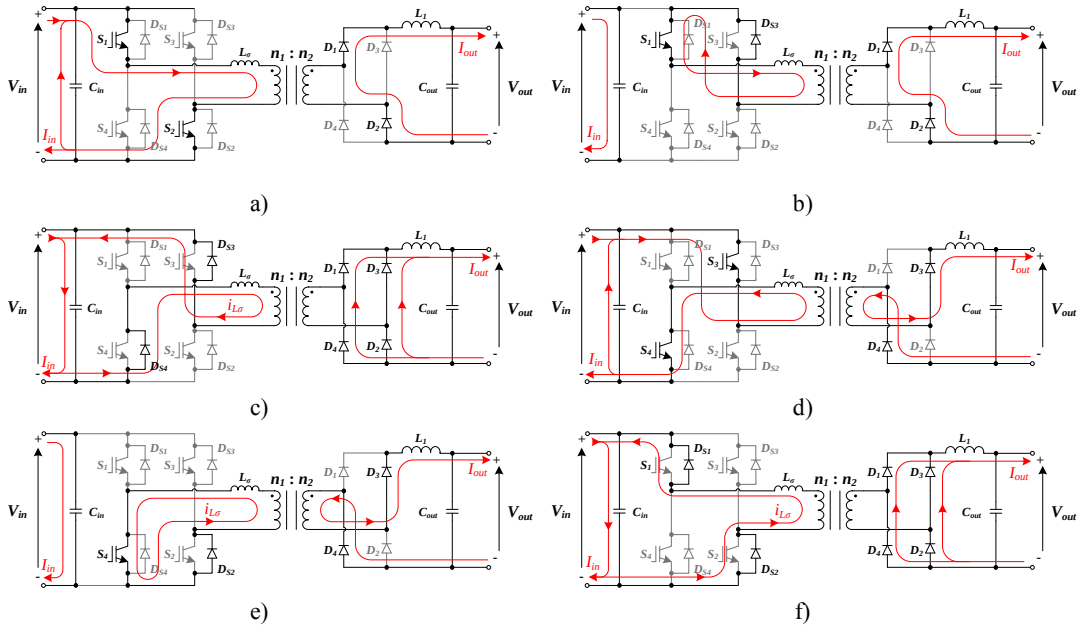


Fig 3.61. Currents circulating through the full-bridge converter a) when S_1-S_2 are on and S_3-S_4 are off, b) when S_1-S_3 are on and S_2-S_4 are off, c) when S_3-S_4 are on and S_1-S_2 are off (the current circulates through the freewheel diodes D_{S3}-D_{S4}), d) when S_3-S_4 are on and S_1-S_2 are off, e) when S_4-S_2 are on and S_1-S_3 are off, and f) when S_1-S_2 are on and S_3-S_4 are off (the current circulates through the freewheel diodes D_{S1}-D_{S2}).

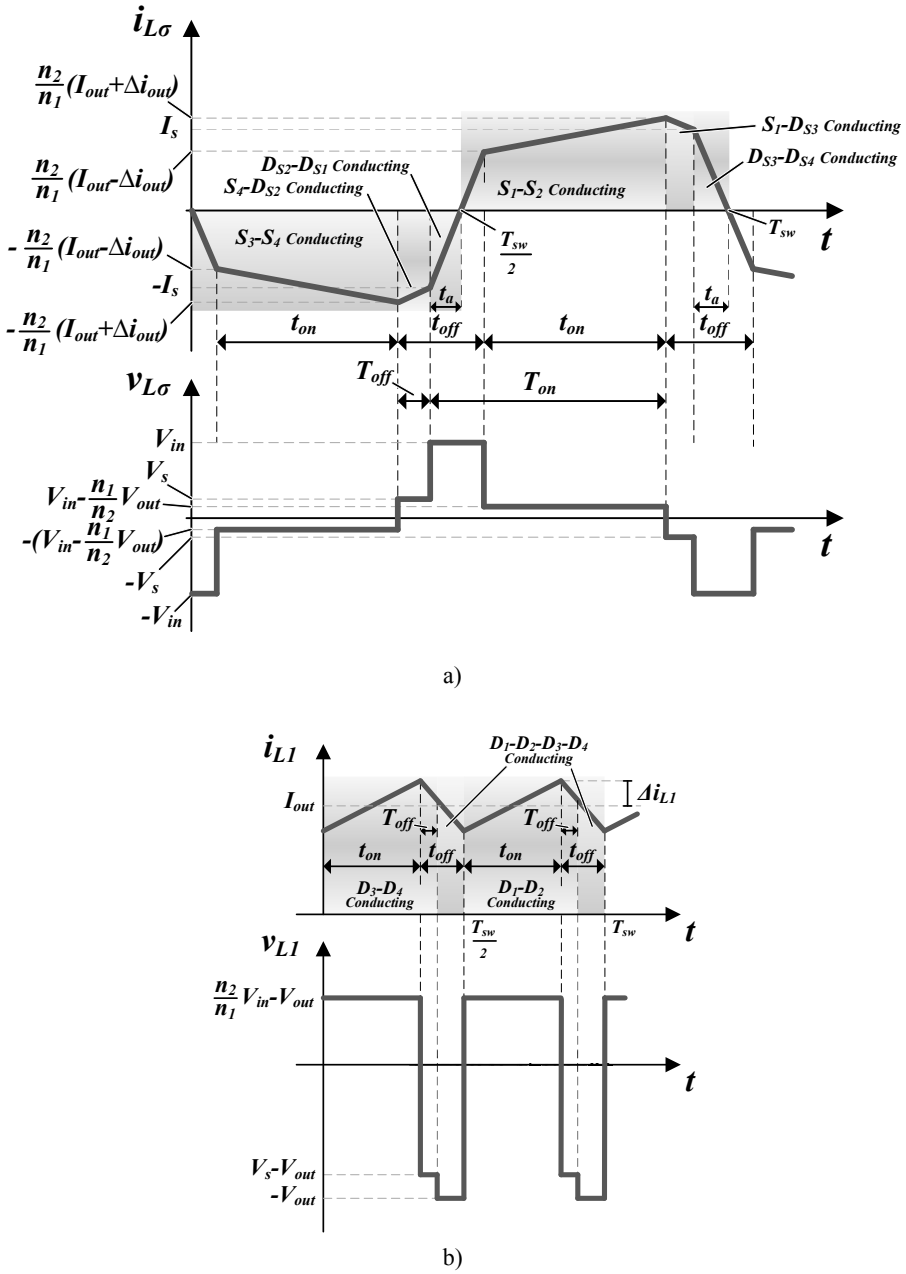
In a continuous current mode operation, the waveforms derived from the afore described operation are illustrated in Fig 3.62. As it can be noticed in Fig 3.62a, the current through the transformer is alternating. So, the magnetization of the transformer is bidirectional, thereby leading to a good utilization of the element. However, in order to prevent the saturation of the transformer, a control strategy must be considered to guarantee that the average voltage applied to the MFT is zero.

During the time interval T_{off} at which zero voltage is applied to the MFT (cf. Fig 3.61b and Fig 3.62a), the leakage inductance is in series with the output inductor. Hence, part of the output voltage drops over the leakage inductance until non-complementary transistors (S_1-S_2 or S_3-S_4) are on (end of T_{off} time interval). The voltage drop in the leakage inductance during T_{off} (V_s) and the current through it at the end of T_{off} (I_s) are respectively approached as:

$$V_s = \frac{V_{out} \cdot L_\sigma}{L_\sigma \cdot \left(\frac{n_2}{n_1}\right)^2 + L_1} \tag{3.201}$$

$$I_s = \frac{n_2}{n_1} \cdot \left(I_{out} + \Delta i_{L1} - \frac{V_s \cdot (0.5 - \delta) \cdot T_{sw}}{L_\sigma} \right) \tag{3.202}$$

where V_{out} is the average output voltage, n_2/n_1 is the turn ratio of the MFT, I_{out} is the average output current (cf. Fig 3.59), Δi_{L1} is the current ripple in L_1 (cf. Fig 3.62b), T_{sw} is the switching frequency and δ is the duty cycle of the converter (T_{on}/T_{sw}).



a)

b)

Fig 3.62. Typical voltage and current waveforms in full-bridge converter's a) leakage inductance L_σ and b) inductor L_1.

When non-complementary transistors are on, there is a time interval (t_{off}-T_{off}) at which all the DC bus voltage (V_{in}) is applied to the leakage inductance (cf. Fig 3.62a). In consequence, the energy coming from the input is used to invert the polarity of the current through L_σ. This results in a reduction of the duty cycle of the converter:

$$\delta_{eff} = \frac{t_{on}}{T_{sw}} = \frac{T_{on} - \left(t_{off} - T_{off}\right)}{T_{sw}} = \delta - L_\sigma \cdot \left(\frac{2 \cdot I_{out}}{V_{in} \cdot T_{sw}} \cdot \frac{n_2}{n_1} \right) \tag{3.203}$$

where T_{on} is the time interval at which non-complementary transistors are on (cf. Fig 3.60), t_{off} is the time interval at which the energy coming from the input side is not

transferred to the output (cf. Fig 3.62) and V_{in} and I_{in} are respectively average input DC voltage and average input current (cf. Fig 3.59).

Therefore, the DC voltage transfer function derived from steady state analysis of the waveforms of Fig 3.62b is expressed in function of the effective duty cycle:

$$V_{out} = 2 \cdot V_{in} \cdot \delta_{eff} \cdot \frac{n_2}{n_1} \tag{3.204}$$

If an ideal operation without losses is assumed (P_{in}=P_{out}), the DC current transfer function is given by:

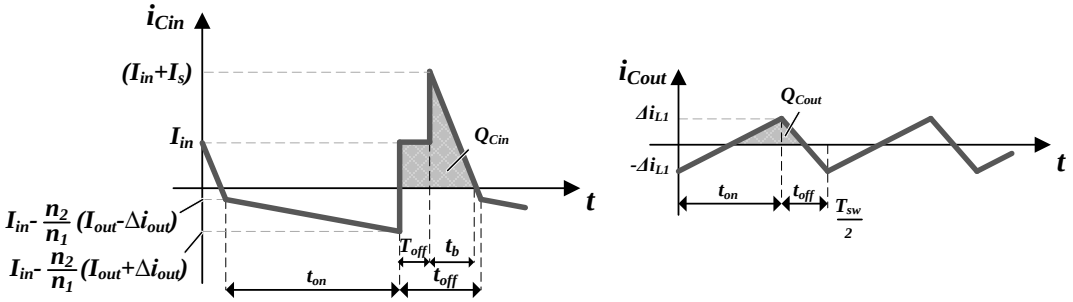
$$\left.\begin{aligned} V_{in} \cdot I_{in} &= V_{out} \cdot I_{out} \\ V_{out} &= 2 \cdot V_{in} \cdot \delta_{eff} \cdot \frac{n_2}{n_1} \end{aligned}\right\} \rightarrow I_{out} = \frac{I_{in}}{2 \cdot \delta_{eff}} \cdot \frac{n_1}{n_2} \tag{3.205}$$

On the other hand, the value of the leakage inductance L_σ can be derived from Eq. (3.201) while the value of the output side inductor L_1 is obtained from the steady state analysis of the waveforms in Fig 3.62b:

$$L_\sigma = \frac{L_1}{\left(\frac{V_{out}}{V_s}\right) - \left(\frac{n_2}{n_1}\right)^2} \tag{3.206}$$

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{\left(V_{in} \cdot \frac{n_2}{n_1} - V_{out}\right)}{2 \cdot \Delta i_{L1}} \cdot \delta_{eff} \cdot T_{sw} \tag{3.207}$$

Assuming input and output currents (I_{in} and I_{out}) are constant, the currents through input and output capacitors can be illustrated as in Fig 3.63.



a) b)

Fig 3.63. Currents circulating through a) the input capacitor and b) the output capacitor of the full-bridge converter.

Therefore, calculating the charges circulating through the capacitors (grey colored areas) the input DC bus capacitance (C_{in}) and the output capacitance (C_{out}) can be derived:

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{2 \cdot I_{in} \cdot T_{off} + t_b \cdot \left(I_{in} + I_s\right)}{4 \cdot \Delta v_{Cin}} \tag{3.208}$$

$$C_{out} = \frac{Q_{Cout}}{\Delta v} = \frac{\Delta i_{L1}}{16 \cdot \Delta v_{Cout}} \cdot T_{sw} \tag{3.209}$$

where Δv_{Cin} and Δv_{Cout} are respectively the half of the desired peak to peak voltage ripple in the input and in the output, and t_b is a time interval given by:

$$t_b = \frac{I_{in} + I_s}{\frac{n_2}{n_1} \cdot (I_{out} - \Delta i_{L1}) + I_s} \cdot (t_{off} - T_{off}) \tag{3.210}$$

Additionally, from the waveforms of Fig 3.62 and Fig 3.63, the expressions of the maximum energy stored by the passive elements, their maximum voltage stress and the *rms* currents circulating through them are derived. These expressions are summarized in Table 3.29.

TABLE 3.29

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2} \cdot C_{in} \cdot (V_{in} + \Delta v_{Cin})^2$	$\sqrt{\frac{2 \cdot \chi}{3 \cdot T_{sw}}}$	$(V_{in} + \Delta v_{Cin})$
L_σ	$\frac{1}{2} \cdot L_\sigma \cdot (I_{out} + \Delta i_{L1})^2 \cdot \left(\frac{n_2}{n_1}\right)^2$	$\sqrt{\frac{2 \cdot \kappa}{3 \cdot T_{sw}}}$	$\approx (V_{in} + \Delta v_{Cin})$
L_1	$\frac{1}{2} \cdot L_1 \cdot (I_{out} + \Delta i_{L1})^2$	$\sqrt{{I_{out}}^2 + \frac{{\Delta i_{L1}}^2}{3}}$	$\approx (V_{out} + \Delta v_{Cout})$
C_{out}	$\frac{1}{2} \cdot C_{out} \cdot (V_{out} + \Delta v_{Cout})^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$(V_{out} + \Delta v_{Cout})$

$$\chi = \left[\begin{array}{l} (t_{off} - T_{off} - t_b) \cdot \left(I_{in} - \frac{n_2}{n_1} \cdot (I_{out} - \Delta i_{L1}) \right)^2 + t_{on} \cdot \left(\frac{n_2}{n_1} \cdot \Delta i_{L1} \right)^2 + 3 \cdot T_{off} \cdot {I_{in}}^2 + t_b \cdot (I_{in} + I_s)^2 + \\ + 3 \cdot t_{on} \cdot \left(I_{in} - \frac{n_2}{n_1} \cdot I_{out} \right)^2 \end{array} \right]$$

$$\kappa = \left[\begin{array}{l} (t_{off} - T_{off} - t_a) \cdot \left(\frac{n_2}{n_1} \cdot (I_{out} - \Delta i_{L1}) \right)^2 + t_{on} \cdot \left(\frac{n_2}{n_1} \right)^2 \cdot \left(3 \cdot {I_{out}}^2 + {\Delta i_{L1}}^2 \right) + t_a \cdot {I_s}^2 + \\ + T_{off} \cdot \left(\frac{n_2}{n_1} \cdot (I_{out} + \Delta i_{L1}) \right)^2 + T_{off} \cdot I_s \cdot \left(I_s + \frac{n_2}{n_1} \cdot (I_{out} + \Delta i_{L1}) \right) \end{array} \right]$$

where t_a is given by:

$$t_a = \frac{I_s}{\frac{n_2}{n_1} \cdot (I_{out} - \Delta i_{L1}) + I_s} \cdot (t_{off} - T_{off})$$

Considering a very small leakage inductance it can be assumed that $t_{on} \approx T_{on}$. Under this assumption and neglecting the current and voltage ripple in the expressions of Table 3.32, the semiconductor utilization factor (U_f) is provided by:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{2 \cdot \delta}{2 \cdot \left(\sqrt{2} + \sqrt{\delta} + \sqrt{1-\delta}\right) + \sqrt{2}} \tag{3.211}$$

This utilization factor is illustrated in Fig 3.64 for different duty cycle values. As it can be noticed, the higher the duty cycle the better the semiconductor utilization. Therefore, in order to minimize the installed semiconductor power in the converter, the n_2/n_1 turn ratio must be carefully chosen to guarantee that the converter operates with duty cycles values close to 0.5.

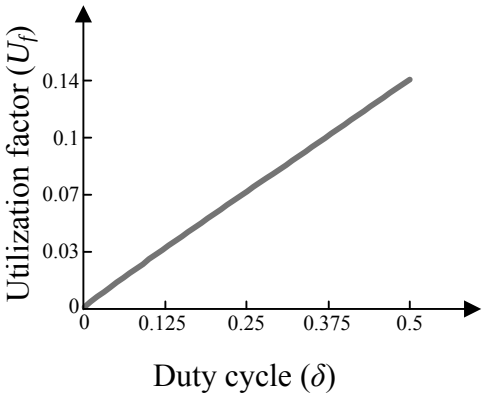


Fig 3.64. Semiconductor utilization factor of the full-bridge converter.

2.2.14.2 Power losses estimation

Generally speaking, the power losses of the converters are given by the semiconductor power losses, which can be estimated through Eq. (3.1) and Eq. (3.2), discussed at the beginning of section 3.2.1.

As it can be noticed in Fig 3.62a, the current conducted by transistors S_1-S_4 is the same, but differs from the current conducted by transistors S_2-S_3 (the current conducted by this latter transistors is also the same). This also happens with their respective freewheel diodes (D_{S1}-D_{S4} and D_{S2}-D_{S3}). Conversely, the current through the diodes of the output side diode bridge is the same (cf. Fig 3.62b). In consequence, power losses are calculated for one semiconductor in each group (S_1, S_2, D_{S1}, D_{S2} and D_1). The tables below summarize the expressions of the currents through the semiconductors as well as of the voltages they block.

TABLE 3.30

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE FREEWHEEL DIODES

Current and voltage expressions	**Freewheel diodes D_{S1}-D_{S4}**	**Freewheel diodes D_{S2}-D_{S3}**
Average current (I_{ave})	$\frac{I_s \cdot t_a}{2 \cdot T_{sw}}$	$\frac{I_s}{2 \cdot T_{sw}} \cdot \left(t_a + T_{off} \cdot \left(1 + \frac{(I_{out} + \Delta i_{L1})}{I_s} \cdot \frac{n_2}{n_1} \right) \right)$
rms current (I_{rms})	$I_s \cdot \sqrt{\frac{t_a}{3 \cdot T_{sw}}}$	$\sqrt{\frac{c}{3 \cdot T_{sw}}}$
Maximum current (i_{max})	I_s	$(I_{out} + \Delta i_{L1}) \cdot \frac{n_2}{n_1}$
Maximum voltage (v_{max})	$(V_{in} + \Delta v_{Cin})$	$(V_{in} + \Delta v_{Cin})$
$c = \left[t_a \cdot {I_s}^2 + T_{off} \cdot \left({I_s}^2 + I_s \cdot (I_{out} + \Delta i_{L1}) \cdot \left(\frac{n_2}{n_1} \right) + (I_{out} + \Delta i_{L1})^2 \cdot \left(\frac{n_2}{n_1} \right)^2 \right) \right]$		

TABLE 3.31

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE DIODE BRIDGE

Current and voltage expressions	**Diodes D_1-D_2-D_3-D_4**
Average current (I_{ave})	$\left[(t_{off} - T_{off} - t_a) \cdot \frac{(I_{out} - \Delta i_{L1})}{2 \cdot T_{sw}} + \frac{t_{on} \cdot I_{out}}{T_{sw}} + \frac{T_{off}}{2 \cdot T_{sw}} \cdot \left(I_{out} + \Delta i_{L1} + I_s \cdot \frac{n_1}{n_2} \right) + \frac{t_a \cdot I_s \cdot n_1}{2 \cdot T_{sw} \cdot n_2} \right]$
rms current (I_{rms})	$\sqrt{\left[\begin{array}{l} (t_{off} - T_{off} - t_a) \cdot \frac{(I_{out} - \Delta i_{L1})^2}{3 \cdot T_{sw}} + \frac{T_{off}}{3 \cdot T_{sw}} \cdot \frac{\left(\left(I_s \cdot \frac{n_1}{n_2} \right)^3 - (I_{out} + \Delta i_{L1})^3 \right)}{\left(I_s \cdot \frac{n_1}{n_2} - (I_{out} + \Delta i_{L1})^3 \right)} + \\ + \frac{t_a}{3 \cdot T_{sw}} \cdot \left(I_s \cdot \frac{n_1}{n_2} \right)^2 + t_{on} \cdot \frac{\left(3 \cdot {I_{out}}^2 + {\Delta i_{L1}}^2 \right)}{3 \cdot T_{sw}} \end{array} \right]}$
Maximum current (i_{max})	$(I_{out} + \Delta i_{L1})$
Maximum voltage (v_{max})	$(V_{in} + \Delta v_{Cin}) \cdot \frac{n_2}{n_1}$

TABLE 3.32

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE TRANSISTORS

Current and voltage expressions	**Transistors S_1-S_4**	**Transistors S_2-S_3**
Average current (I_{ave})	$\frac{n_2}{n_1}\cdot\left(I_{out}\cdot\delta_{eff}+\frac{T_{off}\cdot\left(I_{out}+\Delta i_{L1}+I_s\cdot\frac{n_1}{n_2}\right)}{2\cdot T_{sw}}+\frac{\left(I_{out}-\Delta i_{L1}\right)\cdot\left(t_{off}-T_{off}-t_a\right)}{2\cdot T_{sw}}\right)$	$\frac{n_2}{n_1}\cdot\left(I_{out}\cdot\delta_{eff}+\frac{\left(I_{out}-\Delta i_{L1}\right)\cdot\left(t_{off}-T_{off}-t_a\right)}{2\cdot T_{sw}}\right)$
rms current (I_{rms})	$\left(\frac{n_2}{n_1}\right)\cdot\sqrt{\frac{a}{3\cdot T_{sw}}}$	$\left(\frac{n_2}{n_1}\right)\cdot\sqrt{\frac{b}{3\cdot T_{sw}}}$
Maximum current (i_{max})	$\left(I_{out}+\Delta i_{L1}\right)\cdot\frac{n_2}{n_1}$	$\left(I_{out}+\Delta i_{L1}\right)\cdot\frac{n_2}{n_1}$
Turn-off switched current (i_{off})	I_s	$\left(I_{out}+\Delta i_{L1}\right)\cdot\frac{n_2}{n_1}$
Maximum voltage (v_{max})	$\left(V_{in}+\Delta v_{Cin}\right)$	$\left(V_{in}+\Delta v_{Cin}\right)$
Turn-off switched voltage (v_{off})	$\approx V_{in}$	$\left(V_{in}-\Delta v_{Cin}\right)$
$a=$	$\left[\left(t_{off}-T_{off}-t_a\right)\cdot\left(I_{out}-\Delta i_{L1}\right)^2+\frac{t_{on}}{2\cdot\Delta i_{L1}}\cdot\left(\left(2\cdot\Delta i_{L1}+I_{out}-\Delta i_{L1}\right)^3-\left(I_{out}-\Delta i_{L1}\right)^3\right)+T_{off}\cdot\frac{\left(I_s{}^3\cdot\left(\frac{n_1}{n_2}\right)^2-\left(I_{out}+\Delta i_{L1}\right)^3\cdot\frac{n_2}{n_1}\right)}{\left(I_s-\left(I_{out}+\Delta i_{L1}\right)\cdot\frac{n_2}{n_1}\right)}\right]$	
$b=$	$\left[\left(t_{off}-T_{off}-t_a\right)\cdot\left(I_{out}-\Delta i_{L1}\right)^2+\frac{t_{on}}{2\cdot\Delta i_{L1}}\cdot\left(\left(2\cdot\Delta i_{L1}+\left(I_{out}-\Delta i_{L1}\right)\right)^3-\left(I_{out}-\Delta i_{L1}\right)^3\right)\right]$	

From Eq. (3.1) and the expressions in Table 3.30, Table 3.31 and Table 3.32, the expressions of the average conduction power losses of transistors S_1 (P_{cond_S1}) and S_2 (P_{cond_S2}), freewheel diodes D_{S1} (P_{cond_Ds1}) and D_{S2} (P_{cond_Ds2}) and output diode D_1 (P_{cond_D1}) are given by:

$$P_{cond\_S1}=V_{th}\cdot\frac{n_2}{n_1}\cdot\left(I_{out}\cdot\delta_{eff}+\frac{T_{off}\cdot\left(I_{out}+\Delta i_{L1}+I_s\cdot\frac{n_1}{n_2}\right)}{2\cdot T_{sw}}+\frac{\left(I_{out}-\Delta i_{L1}\right)\cdot\left(t_{off}-T_{off}-t_a\right)}{2\cdot T_{sw}}\right)+ \\ +r_d\cdot\left[\frac{a}{3\cdot T_{sw}}\cdot\left(\frac{n_2}{n_1}\right)^2\right] \tag{3.212}$$

$$P_{cond\_S2} = V_{th} \cdot \frac{n_2}{n_1} \cdot \left(I_{out} \cdot \delta_{eff} + \frac{\left(I_{out} - \Delta i_{L1}\right) \cdot \left(t_{off} - T_{off} - t_a\right)}{2 \cdot T_{sw}} \right) + r_d \cdot \left[\frac{b}{3 \cdot T_{sw}} \cdot \left(\frac{n_2}{n_1} \right)^2 \right] \tag{3.213}$$

$$P_{cond\_Ds1} = V_{th} \cdot \frac{I_s \cdot t_a}{2 \cdot T_{sw}} + r_d \cdot \frac{{I_s}^2 \cdot t_a}{3 \cdot T_{sw}} \tag{3.214}$$

$$P_{cond\_Ds2} = V_{th} \cdot \frac{I_s}{2 \cdot T_{sw}} \cdot \left(t_a + T_{off} \cdot \left(1 + \frac{\left(I_{out} + \Delta i_{L1}\right)}{I_s} \cdot \frac{n_2}{n_1} \right) \right) + r_d \cdot \frac{c}{3 \cdot T_{sw}} \tag{3.215}$$

$$\begin{aligned} P_{cond\_D1} = V_{th} \cdot & \left[\begin{array}{l} \left(t_{off} - T_{off} - t_a\right) \cdot \frac{\left(I_{out} - \Delta i_{L1}\right)}{2 \cdot T_{sw}} + \frac{t_{on} \cdot I_{out}}{T_{sw}} + \frac{t_a}{2 \cdot T_{sw}} \cdot I_s \cdot \frac{n_1}{n_2} + \\ + \frac{T_{off}}{2 \cdot T_{sw}} \cdot \left(I_{out} + \Delta i_{L1} + I_s \cdot \frac{n_1}{n_2} \right) \end{array} \right] + \\ + r_d \cdot & \left[\begin{array}{l} \left(t_{off} - T_{off} - t_a\right) \cdot \frac{\left(I_{out} - \Delta i_{L1}\right)^2}{3 \cdot T_{sw}} + \frac{T_{off}}{3 \cdot T_{sw}} \cdot \frac{\left(\left(I_s \cdot \frac{n_1}{n_2} \right)^3 - \left(I_{out} + \Delta i_{L1}\right)^3 \right)}{\left(I_s \cdot \frac{n_1}{n_2} - \left(I_{out} + \Delta i_{L1}\right)^3 \right)} + \\ + \frac{t_a}{3 \cdot T_{sw}} \cdot \left(I_s \cdot \frac{n_1}{n_2} \right)^2 + t_{on} \cdot \frac{\left(3 \cdot {I_{out}}^2 + {\Delta i_{L1}}^2\right)}{3 \cdot T_{sw}} \end{array} \right] \end{aligned} \tag{3.216}$$

where r_d and V_{th} are the on-state resistance and the threshold voltage of each semiconductor.

Since the freewheel diodes as well as the output side rectifier diodes do not present a hard turn-off behaviour, their switching losses are neglected (cf. Fig 3.60 and Fig 3.62). Furthermore, the transistors operate at zero voltage switching (ZVS) conditions and in consequence, their turn-on power losses are also negligible. Hence, switching power losses are only given in the turn-off of the transistors:

$$P_{sw\_S1} = \frac{V_{in}}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,S1} \cdot \left(I_s\right)^2 + B_{off,S1} \cdot I_s + C_{off,S1} \right) \tag{3.217}$$

$$P_{sw\_S2} = \frac{\left(V_{in} - \Delta v_{Cin}\right)}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,S2} \cdot \left(\left(I_{out} + \Delta i_{L1}\right) \cdot \frac{n_2}{n_1} \right)^2 + B_{off,S2} \cdot \left(I_{out} + \Delta i_{L1}\right) \cdot \frac{n_2}{n_1} + C_{off,S2} \right) \tag{3.218}$$

where $A_{off,XX}$, $B_{off,XX}$ and $C_{off,XX}$ are the turn-off energy loss characteristic coefficients provided by the manufacturer for the 100FIT test voltage (V_{100FIT}).

All the previously presented equations can be simplified assuming the leakage inductance as well as voltage and current ripple are negligible. This simplified equations are described in [21].

2.2.15 Full-bridge isolated-boost

The full-bridge isolated-boost converter illustrated in Fig 3.65 is a unidirectional boost type converter. At the input side, the converter contains a capacitor (C_{in}), an inductor (L_1) and a H-bridge converter (S_1-S_2-S_3-S_4). In turn, a diode bridge (D_1-D_2-D_3-D_4) and a filter

capacitor (C_{out}) form the output side. Both sides of the converter are connected via a medium frequency transformer.

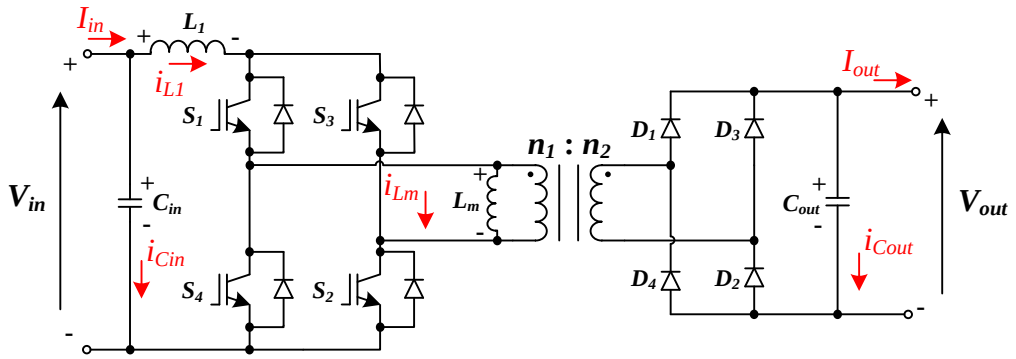


Fig 3.65. Full-bridge isolated-boost converter.

2.2.15.1 Converter design

This converter operates repeatedly storing/transferring the energy in/from inductor L_1. Thus, when all the transistors of the H-bridge are on (T_{on} time interval of Fig 3.66a), the energy coming from the input is stored in the inductor L_1 and the output capacitor C_{out} supplies the load. As zero voltage is applied to the primary of the transformer, the current through the magnetizing inductance remains constant and it flows through the input side transistors. Next, transistors S_3-S_4 are turned-off and the energy coming from the input as well as the energy stored in L_1 are transferred to the output capacitor and the load (T_{off} time interval illustrated in Fig 3.66b). In this time interval, the transformer is magnetized positively. Then, transistors S_3-S_4 are turned-on and again, energy is stored in L_1 while the output capacitor C_{out} supplies the load and the current through L_m remains constant (second T_{on} time interval). Subsequently, transistors S_1-S_2 are turned-off and the energy coming from the input as well as the energy stored in L_1 are transferred to the output, while the transformer is magnetized negatively (second T_{off} time interval illustrated in Fig 3.66c).

Given that the transformer is magnetized bidirectionally, its utilization is good. However, the converter requires a control scheme to avoid the DC current injection that leads to the transformer saturation.

The leakage inductance of the MFT has been neglected in this analysis. Nonetheless, this parasitic inductance has to be considered in real cases. With the described operation, the current circulating through the primary of the MFT is interrupted and in consequence, the voltage over the leakage inductance will raise in a short period of time. This leads to overvoltages in the transistors. This overvoltages can be avoided, or at least reduced, using snubber circuits.

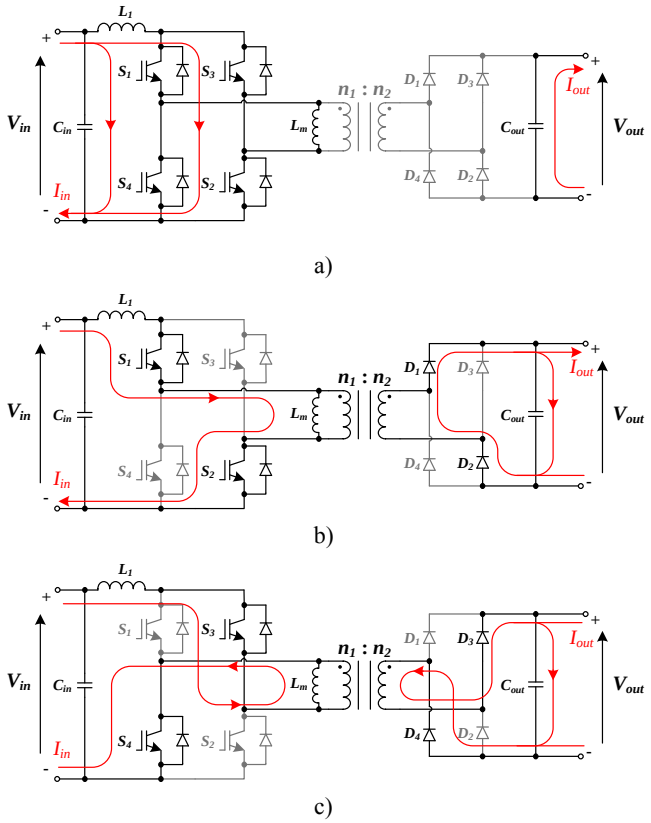


Fig 3.66. Currents circulating through the full-bridge isolated-boost converter a) when all the transistors are on, b) when S_1-S_2 are on and S_3-S_4 are off, and c) when S_1-S_2 are off and S_3-S_4 are on.

The typical current and voltage waveforms of the full-bridge isolated-boost converter in continuous current mode (CCM) are shown in Fig 3.67. From Fig 3.67a, it can be deduced that the theoretical maximum time interval in which all the transistors are on is $T_{sw}/2$. Thus, the maximum duty cycle of the converter is given by:

$$T_{on,\max} = \frac{T_{sw}}{2} \rightarrow \delta_{\max} = \frac{1}{2} \tag{3.219}$$

where $\delta_{\max}$ is the maximum duty cycle of the converter ($T_{on,\max}/T_{sw}$).

During a switching period (T_{sw}), the average current through the input inductor is constant and in consequence, the average voltage drop over the input side inductor is zero. Therefore, from Eq. (3.220) and the voltages drawn in Fig 3.67b, the DC voltage transfer function is derived, Eq. (3.221).

$$\langle v_{L1} \rangle = \frac{1}{T_{sw}} \cdot \left(\int_0^{T_{on}} v_{L1}\, dt + \int_{T_{on}}^{T_{sw}} v_{L1}\, dt \right) = 0 \tag{3.220}$$

$$V_{out} = \frac{V_{in}}{1 - 2 \cdot \delta} \cdot \frac{n_2}{n_1} \tag{3.221}$$

where V_{in} and V_{out} are the average input and output voltages respectively, δ is the duty cycle of the converter and n_1 and n_2 are respectively the number of turns of the primary and secondary windings of the medium frequency transformer (cf. Fig 3.65).

Similarly, the DC current transfer function is obtained from the waveforms shown Fig 3.67c:

$$I_{out} = (1 - 2 \cdot \delta) \cdot I_{in} \cdot \frac{n_1}{n_2} \tag{3.222}$$

where I_{in} and I_{out} are the average input and output currents respectively (cf. Fig 3.65).

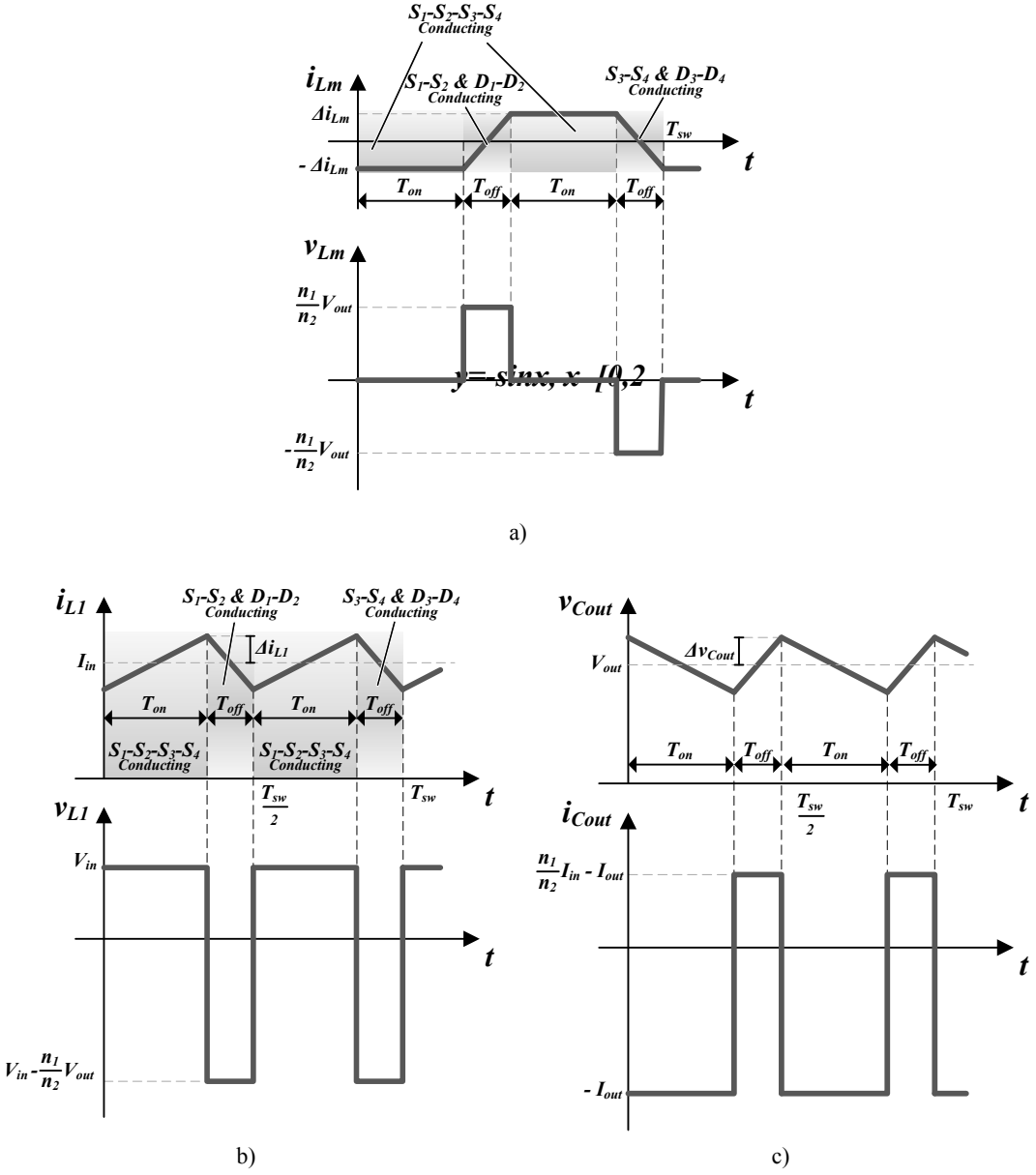


Fig 3.67. Typical voltage and current waveforms in full-bridge isolated-boost converter's a) magnetizing inductance L_m, b) inductor L_1 and c) capacitor C_{out}.

On the other hand, the inductances of the magnetic elements in the converter can be calculated from the waveforms depicted in Fig 3.67a and Fig 3.67b:

$$L_m = v_{Lm} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{out}}{4 \cdot \Delta i_{Lm}} \cdot \frac{n_1}{n_2} \cdot (1 - 2 \cdot \delta) \cdot T_{sw} \tag{3.223}$$

$$L_1 = v_{L1} \cdot \frac{\Delta t}{\Delta i} = \frac{V_{in}}{2 \cdot \Delta i_{L1}} \cdot \delta \cdot T_{sw} \tag{3.224}$$

where Δi_{Lm} is the current ripple in L_m and Δi_{L1} is the current ripple in L_1.

Similarly, the value of C_{out} can be calculated from the steady state analysis of the waveforms of Fig 3.67c:

$$C_{out} = i_{Cout} \cdot \frac{\Delta t}{\Delta v} = \frac{I_{out}}{2 \cdot \Delta v_{Cout}} \cdot \delta \cdot T_{sw} \tag{3.225}$$

where Δv_{Cout} is the output voltage ripple.

Assuming the input current I_{in} is constant, the current circulating through the input capacitor is the same as the current ripple in the input side inductor. Thus, the input DC bus capacitance (C_{in}) can be calculated from Fig 3.68:

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{\Delta i_{L1}}{16 \cdot \Delta v_{Cin}} \cdot T_{sw} \tag{3.226}$$

where Δv_{Cin} is the half of the desired peak to peak input voltage ripple.

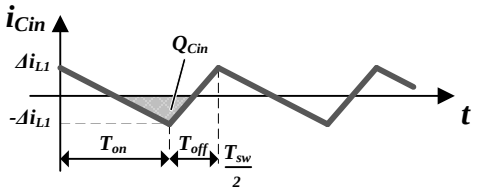


Fig 3.68. Current through the input capacitor of the full-bridge isolated-boost converter.

The equations of the maximum energy stored by the passive elements, their maximum voltage stress and the *rms* currents circulating through them are summarized in Table 3.33. These expressions can be derived from the waveforms in Fig 3.67 and Fig 3.68.

The optimal design point is determined by the semiconductor utilization factor (U_f). Calculated from Table 3.34, the semiconductor utilization factor of the full-bridge isolated-boost converter is given by:

$$U_f = \frac{P_{Rated}}{\sum_{all\_switches} v_{\max} \cdot I_{rms}} = \frac{1 - 2 \cdot \delta}{4 \cdot \left(\sqrt{\frac{1-\delta}{2}} + \sqrt{\frac{1-2\cdot\delta}{2}} \right)} \tag{3.227}$$

As it can be noticed, this U_f factor is the same as that discussed for the push-pull isolated-boost converter in Eq. (3.169) and illustrated in Fig 3.49. Therefore, as discussed for that converter, the lower the duty cycle the better the semiconductor utilization. In

consequence, the n_2/n_1 turn ratio must be chosen to make sure the converter operates with low duty cycle values.

TABLE 3.33

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2}\cdot C_{in}\cdot\left(V_{in}+\Delta v_{Cin}\right)^2$	$\frac{\Delta i_{L1}}{\sqrt{3}}$	$\left(V_{in}+\Delta v_{Cin}\right)$
L_m	$\frac{1}{2}\cdot L_m\cdot {\Delta i_{Lm}}^2$	$\Delta i_{Lm}\cdot\sqrt{\frac{1+4\cdot\delta}{3}}$	$\left(V_{out}+\Delta v_{Cout}\right)\cdot\frac{n_1}{n_2}$
L_1	$\frac{1}{2}\cdot L_1\cdot\left(I_{in}+\Delta i_{L1}\right)^2$	$\sqrt{{I_{in}}^2+\frac{{\Delta i_{L1}}^2}{3}}$	$\left(V_{in}+\Delta v_{Cin}\right)$
C_{out}	$\frac{1}{2}\cdot C_{out}\cdot\left(V_{out}+\Delta v_{Cout}\right)^2$	$\sqrt{2\cdot\delta\cdot{I_{out}}^2+\left(1-2\cdot\delta\right)\cdot\left(I_{in}\cdot\frac{n_1}{n_2}-I_{out}\right)^2}$	$\left(V_{out}+\Delta v_{Cout}\right)$

2.2.15.2 Power losses estimation

Generally speaking, the power losses of the converter are given by semiconductor power losses. Semiconductor power losses depend on conduction power losses, Eq. (3.1), and switching power losses, Eq. (3.2). In turn, conduction power losses depend on average and *rms* currents through the switches, while switching power losses depend on the switched current and voltages. Assuming all the transistors of the input side H-bridge converter conduct the same current, it can be said that their average power losses are equal. This is applicable to output side rectifier diodes D_1-D_2-D_3-D_4. Therefore, power losses expressions are calculated just for one semiconductor in each group. The expressions required for calculating these power losses are summarized in Table 3.34.

All in all, average conduction power losses of transistor S_1 (P_{cond_S1}) and diode D_1 (P_{cond_D1}) are:

$$P_{cond\_S1}=V_{th}\cdot\frac{I_{in}}{2}+r_d\cdot\left[{I_{in}}^2\cdot\frac{\left(1-\delta\right)}{2}+\delta\cdot\left(\frac{{\Delta i_{Lm}}^2}{2}+\frac{{\Delta i_{L1}}^2}{6}\right)+\left(\frac{1}{2}-\delta\right)\cdot\frac{{\Delta i_{L1}}^2}{3}\right] \tag{3.228}$$

$$P_{cond\_D1}=V_{th}\cdot\frac{I_{out}}{2}+r_d\cdot\left[\left(I_{in}\cdot\frac{n_1}{n_2}\right)^2+\left(\frac{n_1}{n_2}\right)^2\cdot\frac{\left(\Delta i_{Lm}+\Delta i_{L1}\right)^2}{3}\right]\cdot\left(\frac{1}{2}-\delta\right) \tag{3.229}$$

where r_d and V_{th} are each semiconductor's on-state resistance and threshold voltage respectively.

TABLE 3.34
EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

Current and voltage expressions	**Transistors S_1-S_2**	**Diodes D_1-D_2-D_3-D_4**
Average current (I_{ave})	$\frac{I_{in}}{2}$	$\frac{I_{out}}{2}$
rms current (I_{rms})	$\sqrt{\left[{I_{in}}^2 \cdot \frac{(1-\delta)}{2} + \delta \cdot \left(\frac{{\Delta i_{Lm}}^2}{2} + \frac{{\Delta i_{L1}}^2}{6} \right) + \left(\frac{1}{2} - \delta \right) \cdot \frac{{\Delta i_{L1}}^2}{3} \right]}$	$\sqrt{\left[\left(I_{in} \cdot \frac{n_1}{n_2} \right)^2 + \left(\frac{n_1}{n_2} \right)^2 \cdot \frac{(\Delta i_{Lm} + \Delta i_{L1})^2}{3} \right] \cdot \left(\frac{1}{2} - \delta \right)}$
Maximum current (i_{max})	$\left(I_{in} + \Delta i_{L1} \right)$	$\left(I_{in} + \Delta i_{L1} + \Delta i_{Lm} \right) \cdot \frac{n_1}{n_2}$
Turn-on switched current (i_{on})	$\frac{\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right)}{2}$	—
Turn-off switched current (i_{off})	$\frac{\left(I_{in} + \Delta i_{L1} + \Delta i_{Lm} \right)}{2}$	$\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right) \cdot \frac{n_1}{n_2}$
Maximum voltage (v_{max})	$\left(V_{out} + \Delta v_{Cout} \right) \cdot \frac{n_1}{n_2}$	$\left(V_{out} + \Delta v_{Cout} \right)$
Turn-on switched voltage (v_{on})	$\left(V_{out} + \Delta v_{Cout} \right) \cdot \frac{n_1}{n_2}$	—
Turn-off switched voltage (v_{off})	$\left(V_{out} - \Delta v_{Cout} \right) \cdot \frac{n_1}{n_2}$	$\frac{\left(V_{out} + \Delta v_{Cout} \right)}{2}$

Average switching power losses of the transistor S_1 (P_{sw_S1}) and diode D_1 (P_{sw_D1}) are given by:

$$P_{sw\_S1} = \frac{\left(V_{out} - \Delta v_{Cout} \right) \cdot \frac{n_1}{n_2}}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,S1} \cdot \left(\frac{\left(I_{in} + \Delta i_{L1} + \Delta i_{Lm} \right)}{2} \right)^2 + B_{off,S1} \cdot \frac{\left(I_{in} + \Delta i_{L1} + \Delta i_{Lm} \right)}{2} + C_{off,S1} \right) + \frac{\left(V_{out} + \Delta v_{Cout} \right) \cdot \frac{n_1}{n_2}}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{on,S1} \cdot \left(\frac{\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right)}{2} \right)^2 + B_{on,S1} \cdot \frac{\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right)}{2} + C_{on,S1} \right) \tag{3.230}$$

$$P_{sw\_D1} = \frac{\left(V_{out} + \Delta v_{Cout} \right)}{2 \cdot T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,D1} \cdot \left(\left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right) \cdot \frac{n_1}{n_3} \right)^2 + B_{off,D1} \cdot \left(I_{in} - \Delta i_{L1} - \Delta i_{Lm} \right) \cdot \frac{n_1}{n_3} + C_{off,D1} \right) \tag{3.231}$$

where $A_{off,XX}$, $B_{off,XX}$ and $C_{off,XX}$ are the turn-off energy loss characteristic coefficients provided by the manufacturer for the 100FIT test voltage (V_{100FIT}) switch whereas $A_{on,S1}$, $B_{on,S1}$ and $C_{on,S1}$ are turn-on energy loss characteristic coefficients.

2.2.16 Single-active-bridge

The single-active-bridge converter depicted in Fig 3.69 is a unidirectional converter derived from buck. The converter is composed of a medium frequency transformer, a H-bridge converter (S_1-S_2-S_3-S_4) at the input side, a diode bridge (D_1-D_2-D_3-D_4) at the output side and two DC bus filter capacitors, one at the input side (C_{in}) and another one at the output side (C_{out}).

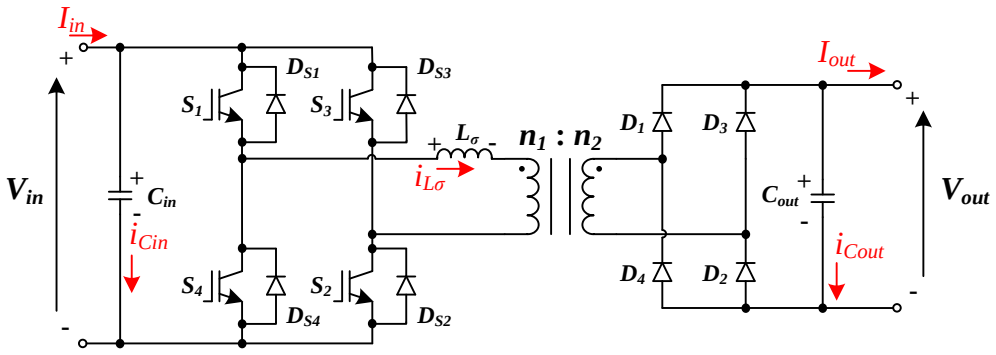


Fig 3.69. Single-active-bridge converter.

2.2.16.1 Converter design

The converter operates alternating the switching orders of the transistors S_1-S_2 and S_3-S_4. With light loads, the converter operates in discontinuous current more (DCM) while with nominal and heavy loads, the converter operates in continuous current mode (CCM) [22]. Under nominal load operation conditions, if S_1-S_2 are on and S_3-S_4 are off (T_{on} time interval), the energy coming from the input and the energy stored in the input capacitor (C_{in}) are transferred to the leakage inductance of the MFT (L_σ) and the load (cf. Fig 3.70a). Then, S_1-S_2 are turned-off while S_3-S_4 are turned-on. During a T_{off} time interval (cf. Fig 3.70b), the current polarity is opposite to the natural conduction sense of the transistors and hence, current flows through freewheel diodes D_{S3} and D_{S4}. The load is supplied by the energy stored in the leakage inductance and in the output capacitor (C_{out}) while the energy coming from the input is stored in C_{in}. Once the current polarity is inversed, transistors S_3-S_4 begin to conduct the current coming from the input and a second T_{on} time interval begins (cf. Fig 3.70c). Again, the energy coming from input and the energy stored in C_{in} are transferred to L_σ and the load. Next, S_1-S_2 are turned-off and S_3-S_4 are turned-on (cf. Fig 3.70d). Until its polarity is inversed, the current in the leakage inductance circulates through freewheel diodes D_{S1} and D_{S2} (second T_{off} time interval).

For light loads, the transferred power is reduced diminishing the duty cycle. In consequence, there are time intervals at which all the transistors are off, the load is supplied by the output capacitor and the energy coming from the input is stored in the input capacitor (cf. Fig 3.70f).

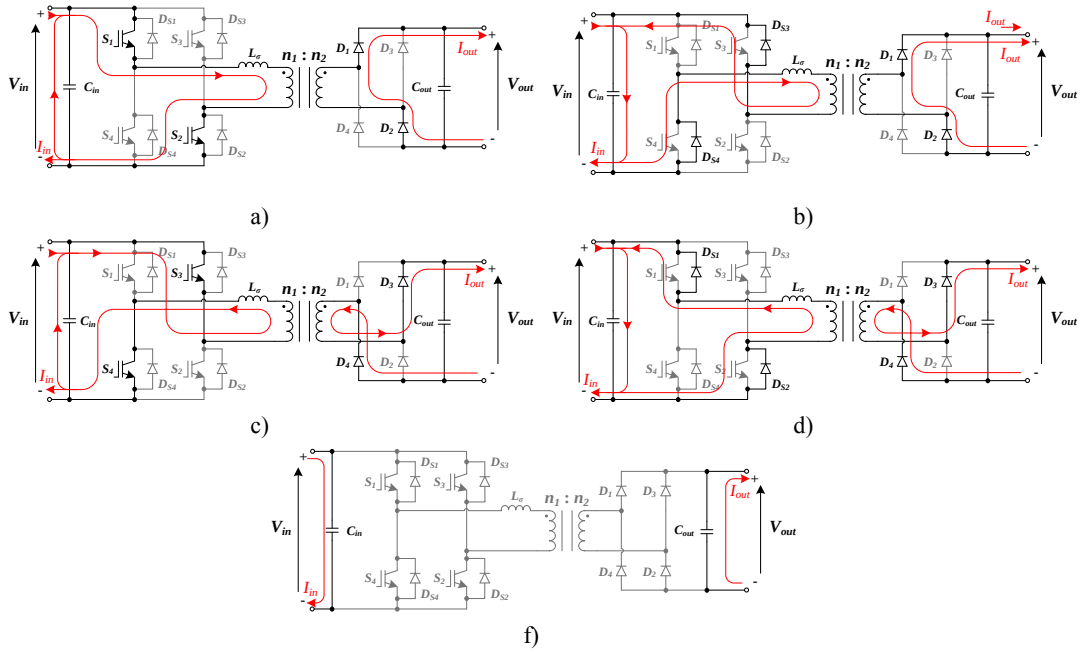


Fig 3.70. Currents circulating through the single-active-bridge converter a) when S_1-S_2 are on and S_3-S_4 are off, b) when S_3-S_4 are on and S_1-S_2 are off (the current circulates through the freewheel diodes D_{S3}-D_{S4}), c) when S_1-S_3 are on and S_2-S_4 are off, d) when S_1-S_2 are on and S_3-S_4 are off (the current circulates through the freewheel diodes D_{S1}-D_{S2}) and f) when S_1-S_2 and S_3-S_4 are off.

The current and voltage waveforms in the leakage inductance of the MFT are illustrated in Fig 3.71. As it can be noticed, the current through the medium frequency transformer is alternating. Thus, the magnetization of the transformer is bidirectional and therefore, the utilization of the medium frequency transformer is good. In order to prevent the saturation of the transformer, a control strategy must guarantee that the average voltage applied to the MFT is zero.

As it has been said, the power is only transferred during the T_{on} time interval. Hence, from Fig 3.71a it can be deduced that the maximum current through the leakage inductance i_{max} is given by:

$$P_{in} = V_{in} \cdot I_{in} = V_{in} \cdot \frac{i_{\max}}{2} \cdot \frac{2 \cdot T_{on}}{T_{sw}} - V_{in} \cdot \frac{i_{\max}}{2} \cdot \frac{2 \cdot T_{off}}{T_{sw}} \rightarrow$$
$$\rightarrow i_{\max} = I_{in} \cdot \frac{T_{sw}}{\left(T_{on} - T_{off}\right)} \tag{3.232}$$

where V_{in} and I_{in} are respectively the average input voltage and current (cf. Fig 3.69), T_{on} and T_{off} are respectively the conduction times of the transistors and the freewheel diodes and T_{sw} is the switching period.

For any conduction mode (continuous or discontinuous, Fig 3.71), the relation between the current through the leakage inductance and the voltage drop over this parasitic element can be expressed as:

$$v_{L\sigma} = L_\sigma \cdot \frac{\Delta i}{\Delta t} \rightarrow \left(V_{in} - V_{out} \cdot \frac{n_1}{n_2} \right) = \frac{L_\sigma \cdot i_{\max}}{T_{on}} \tag{3.233}$$

$$v_{L\sigma} = L_\sigma \cdot \frac{\Delta i}{\Delta t} \rightarrow \left(V_{in} + V_{out} \cdot \frac{n_1}{n_2} \right) = \frac{L_\sigma \cdot i_{\max}}{T_{off}} \tag{3.234}$$

where V_{out} is the average output voltage and n_2/n_1 is the turn ratio of the MFT (cf. Fig 3.69).

Developing these equations, the relation between the duty cycle of the converter and the conduction time of the freewheel diodes (T_{off}) is obtained, Eq. (3.235). This expression is valid for continuous and discontinuous current mode conditions.

$$T_{off} = T_{on} \cdot \frac{1 - M}{1 + M} \tag{3.235}$$

$$M = \frac{V_{out}}{V_{in}} \cdot \frac{n_1}{n_2} \tag{3.236}$$

From the same equations, and assuming the converter operates with nominal load conditions (hence, $2T_{on}+2T_{off}=T_{sw}$), the DC voltage transfer function can be obtained:

$$V_{out} = V_{in} \cdot (4 \cdot \delta - 1) \cdot \frac{n_2}{n_1} \tag{3.237}$$

where δ is the duty cycle of the converter ($T_{on}/T_{sw} \leq 0.5$).

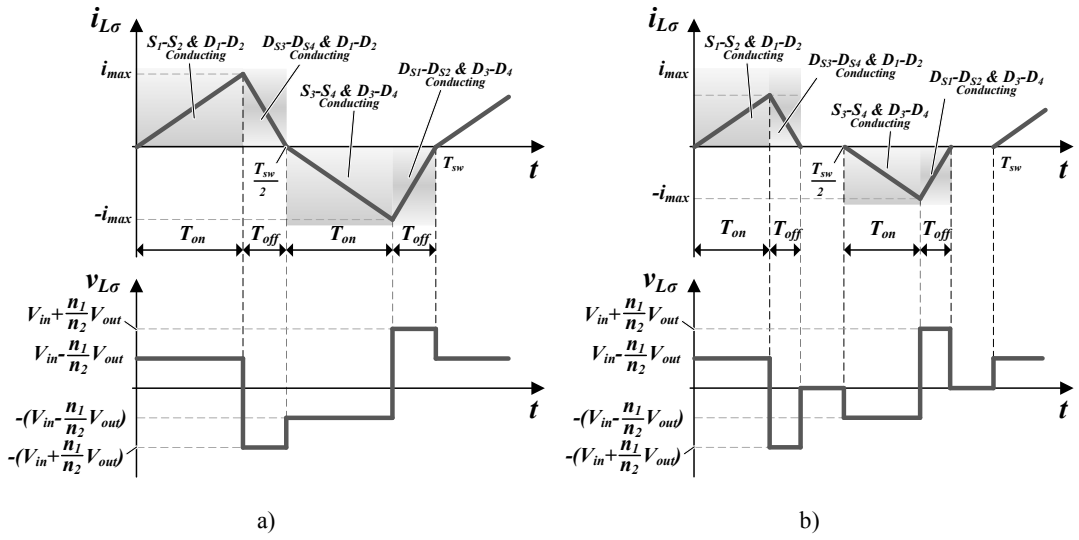


Fig 3.71. Typical voltage and current waveforms in the leakage inductance (L_σ) of the single-active-bridge converter in a) continuous current mode operation and b) discontinuous current mode operation.

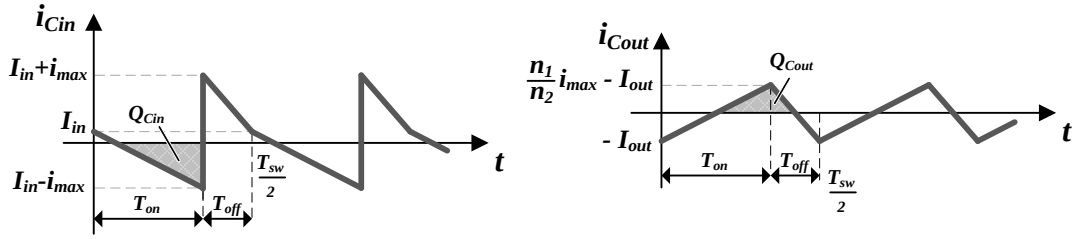
Considering an ideal operation without losses (P_{in}=P_{out}), the DC current transfer function for nominal conditions is given by:

$$\left.\begin{aligned} V_{in}\cdot I_{in} &= V_{out}\cdot I_{out} \\ V_{out} &= V_{in}\cdot(4\cdot\delta-1)\cdot\frac{n_2}{n_1}\end{aligned}\right\}\rightarrow I_{out}=\frac{I_{in}}{(4\cdot\delta-1)}\cdot\frac{n_1}{n_2} \tag{3.238}$$

On the other hand, the value of the leakage inductance L_σ can be derived from Fig 3.71:

$$L_\sigma = v_{L\sigma}\cdot\frac{\Delta t}{\Delta i}=\frac{\left(V_{in}-V_{out}\cdot\frac{n_1}{n_2}\right)}{i_{\max}}\cdot\delta\cdot T_{sw} \tag{3.239}$$

Under the assumption of a CCM operation and constant input and output currents (I_{in} and I_{out}), the currents through input and output capacitors can be drawn as in Fig 3.72.



a) b)

Fig 3.72. Currents circulating through a) the input capacitor and b) the output capacitor of the single-active-bridge converter under the assumption of a continuous current mode operation.

As a consequence, calculating the charges circulating through the capacitors (grey colored areas in Fig 3.72) the input DC bus capacitance (C_{in}) and the output capacitance (C_{out}) can be derived:

$$C_{in}=\frac{Q_{Cin}}{\Delta v}=\frac{(I_{in}-i_{\max})\cdot T_{on}\cdot\left(1-\frac{I_{in}}{i_{\max}}\right)}{4\cdot\Delta v_{Cin}} \tag{3.240}$$

$$C_{out}=\frac{Q_{Cout}}{\Delta v}=\frac{\left(i_{\max}\cdot\frac{n_1}{n_2}-I_{out}\right)}{16\cdot\Delta v_{Cout}}\cdot T_{sw} \tag{3.241}$$

where Δv_{Cin} and Δv_{Cout} are respectively the half of the desired peak to peak voltage ripple in the input and in the output capacitors.

Additionally, from Fig 3.71a and Fig 3.72, the expressions of the maximum energy stored by the passive elements, their maximum voltage stress and the *rms* currents circulating through them are derived and summarized in Table 3.35.

TABLE 3.35

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2}\cdot C_{in}\cdot\left(V_{in}+\Delta v_{Cin}\right)^2$	$\sqrt{\frac{2\cdot\chi}{3\cdot i_{\max}\cdot T_{sw}}}$	$\left(V_{in}+\Delta v_{Cin}\right)$
L_σ	$\frac{1}{2}\cdot L_\sigma\cdot {i_{\max}}^2$	$\frac{i_{\max}}{\sqrt{3}}$	$\approx\left(V_{in}+V_{out}\cdot\frac{n_1}{n_2}\right)$
C_{out}	$\frac{1}{2}\cdot C_{out}\cdot\left(V_{out}+\Delta v_{Cout}\right)^2$	$\sqrt{\frac{1}{6}\cdot\left[{I_{out}}^2+\left(i_{\max}\cdot\frac{n_1}{n_2}-I_{out}\right)^2\right]}$	$\left(V_{out}+\Delta v_{Cout}\right)$

$$\chi=\left[T_{on}\cdot\left({I_{in}}^3-\left(I_{in}-i_{\max}\right)^3\right)+T_{off}\cdot\left(\left(I_{in}+i_{\max}\right)^3-{I_{in}}^3\right)\right]$$

From the expression in Table 3.36 and Table 3.37, the semiconductor utilization factor (U_f) is provided by:

$$U_f=\frac{P_{Rated}}{\sum_{all\_switches}v_{\max}\cdot I_{rms}}=\frac{\sqrt{3}\cdot M\cdot\delta}{2\cdot\left(1+M\right)\cdot\left(\sqrt{\delta}+\sqrt{\frac{\left(1-M\right)\cdot\delta}{1+M}}+M\cdot\sqrt{\frac{2\cdot\delta}{1+M}}\right)} \tag{3.242}$$

In Fig 3.73, the semiconductor utilization factor is illustrated for a given M value (M=0.6) and different duty cycles. As for previously discussed buck derived converters, the higher the duty cycle the better the semiconductor utilization. Therefore, in order to minimize the installed semiconductor power in the converter, the converter must be designed to operate with duty cycles values close to 0.5.

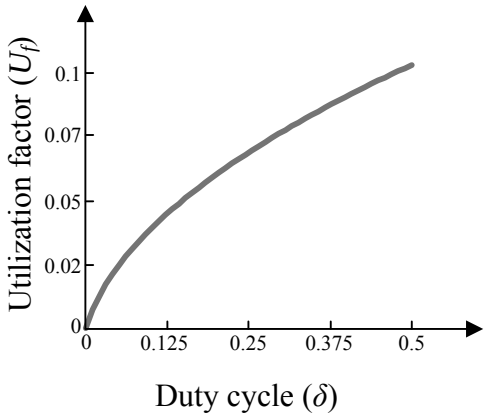


Fig 3.73. Semiconductor utilization factor of the single-active-bridge converter.

2.2.16.2 Power losses estimation

Assuming ideal passive elements with no losses, the power losses of the converter are given by the semiconductor power losses. These, can be estimated through Eq. (3.1) and Eq. (3.2) discussed at the beginning of section 3.2.1. The current and voltage expressions

required by the mentioned equations have been obtained from Fig 3.71 and are summarized in Table 3.36 and Table 3.37.

TABLE 3.36

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS OF THE INPUT SIDE H-BRIDGE

Current and voltage expressions	**Transistors** S_1-S_2-S_3-S_4	**Freewheel diodes** D_{S1}-D_{S2}-D_{S3}-D_{S4}
Average current (I_{ave})	$\frac{i_{\max}}{2}\cdot\delta$	$\frac{i_{\max}}{2}\cdot\left(\frac{1-M}{1+M}\right)\cdot\delta$
rms current (I_{rms})	$i_{\max}\cdot\sqrt{\frac{\delta}{3}}$	$i_{\max}\cdot\sqrt{\left(\frac{1-M}{1+M}\right)\cdot\frac{\delta}{3}}$
Maximum current (i_{max})	$i_{\max}$	$i_{\max}$
Turn-off switched current (i_{off})	$i_{\max}$	0
Maximum voltage (v_{max})	$\left(V_{in}+\Delta v_{Cin}\right)$	$\left(V_{in}+\Delta v_{Cin}\right)$
Turn-off switched voltage (v_{off})	$\left(V_{in}-\Delta v_{Cin}\right)$	0

TABLE 3.37

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE DIODE BRIDGE

Current and voltage expressions	**Diodes** D_1-D_2-D_3-D_4
Average current (I_{ave})	$\frac{i_{\max}\cdot\delta}{(1+M)}\cdot\frac{n_1}{n_2}$
rms current (I_{rms})	$i_{\max}\cdot\frac{n_1}{n_2}\cdot\sqrt{\frac{\delta}{(1+M)}\cdot\frac{2}{3}}$
Maximum current (i_{max})	$i_{\max}\cdot\frac{n_1}{n_2}$
Turn-off switched current (i_{off})	0
Maximum voltage (v_{max})	$\left(V_{out}+\Delta v_{Cout}\right)$
Turn-off switched voltage (v_{off})	$\approx V_{out}$

Since the current and voltage expressions of all the transistors are the same, the power losses expressions are calculated for one transistor only. This is also applied to the freewheel diodes and the output rectifier diodes.

Thus, from Eq. (3.1) and Table 3.36, the expressions of the average conduction power losses of transistor S_1 (P_{cond_S1}) and freewheel diode D_{S1} (P_{cond_Ds1}) are given by:

$$P_{cond\_S1} = V_{th} \cdot \frac{i_{\max}}{2} \cdot \delta + r_d \cdot {i_{\max}}^2 \cdot \frac{\delta}{3} \tag{3.243}$$

$$P_{cond\_Ds1} = V_{th} \cdot \frac{i_{\max}}{2} \cdot \left(\frac{1-M}{1+M}\right) \cdot \delta + r_d \cdot {i_{\max}}^2 \cdot \frac{\delta}{3} \cdot \left(\frac{1-M}{1+M}\right) \tag{3.244}$$

where r_d and V_{th} are the on-state resistance and the threshold voltage of each semiconductor.

Similarly, average conduction power losses of the output diode D_1 (P_{cond_D1}) are expressed as:

$$P_{cond\_D1} = V_{th} \cdot \frac{i_{\max} \cdot \delta}{(1+M)} \cdot \frac{n_1}{n_2} + r_d \cdot \left(i_{\max} \cdot \frac{n_1}{n_2}\right)^2 \cdot \frac{\delta}{(1+M)} \cdot \frac{2}{3} \tag{3.245}$$

In this converter, the freewheel diodes and the rectifier diodes are turned-off with a relatively low current slope and hence, their switching losses can be neglected [22-23]. Moreover, the turn-on of the transistors is given at zero voltage switching (ZVS) conditions in CCM (cf. Fig 3.71a) and in zero current switching (ZCS) conditions in DCM (cf. Fig 3.71b). In consequence, their turn-on power losses are also negligible. Therefore, switching power losses are only given in the turn-off of the transistors:

$$P_{sw\_S1} = \frac{(V_{in} - \Delta v_{Cin})}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,S1} \cdot (i_{\max})^2 + B_{off,S1} \cdot i_{\max} + C_{off,S1}\right) \tag{3.246}$$

where $A_{off,XX}$, $B_{off,XX}$ and $C_{off,XX}$ are the turn-off energy loss characteristic coefficients provided by the manufacturer for the 100FIT test voltage (V_{100FIT}).

2.2.17 Dual-active-bridge

The dual-active-bridge converter is a bidirectional step-up/down converter composed of two H-bridge converters (one at the input side and the other at the output side), two DC bus capacitors (C_{in} and C_{out}) and a medium frequency transformer.

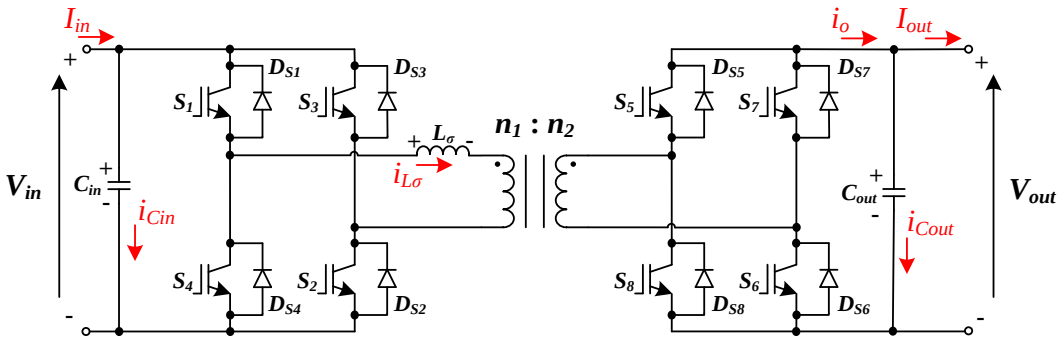


Fig 3.74. Dual-active-bridge converter.

2.2.17.1 Converter design

The dual-active-bridge converter operates phase-shifting the square wave voltages applied at each side of the medium frequency transformer (cf. Fig 3.75). The voltage resulting from the subtraction of these voltages drops over the leakage inductance (L_σ). The voltage applied to the leakage inductance determines the current circulating through the transformer and thus, the power transferred by the converter. This voltage drop varies changing the phase-shift (φ) between the square wave voltages and in consequence, the power transference can be managed by means of controlling this phase-shift.

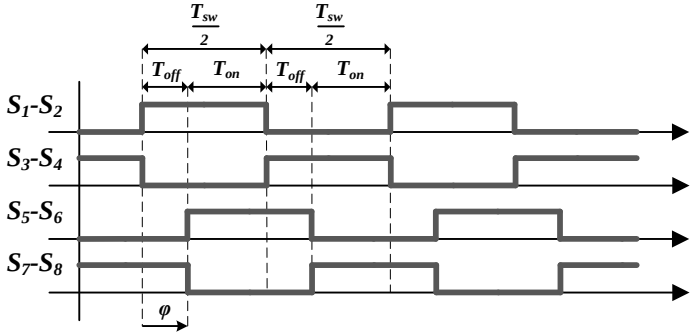


Fig 3.75. Switching orders in the dual-active-bridge converter.

As it can be noticed in Fig 3.75, each transistor is on during half of the switching period ($T_{sw}/2$). The switching orders of transistors S_1-S_2 and transistors S_3-S_4 are complementary. In the same way, the switching orders of transistors S_5-S_6 and transistors S_7-S_8 are complementary. The operation of the converter during a switching period is illustrated in Fig 3.76 assuming constant input and output currents (I_{in} and I_{out} in Fig 3.74). When S_1-S_2 are turned-on, S_7-S_8 are still on (cf. Fig 3.75) and the energy coming from the input is used to invert the polarity of the current through the leakage inductance from negative to positive (cf. Fig 3.77). During the inversion process of the current polarity, the current circulates through freewheel diodes D_{S1}-D_{S2} and D_{S7}-D_{S8} (cf. Fig 3.76a). Once the current through the leakage inductance is positive it flows through transistors S_1-S_2 and S_7-S_8 (cf. Fig 3.76b). Then, transistors S_7-S_8 are turned-off while S_5-S_6 are turned-on and, during their T_{on} time interval (cf. Fig 3.76c), the energy coming from the input is transferred to the output. When transistors S_1-S_2 are turned-off and S_3-S_4 are turned-on, the energy coming from the input is used to invert the polarity of the current through the leakage inductance. While the polarity of this current is positive, the current flows through freewheel diodes D_{S3}-D_{S4} and D_{S5}-D_{S6} (cf. Fig 3.76d). When the current is negative, it circulates through transistors S_3-S_4 and S_5-S_6 (cf. Fig 3.76e). Then, transistors S_7-S_8 are turned-on and transistors S_5-S_6 are turned-off. During the second T_{on} time interval (cf. Fig 3.76f), the energy coming from the input is transferred to the output.

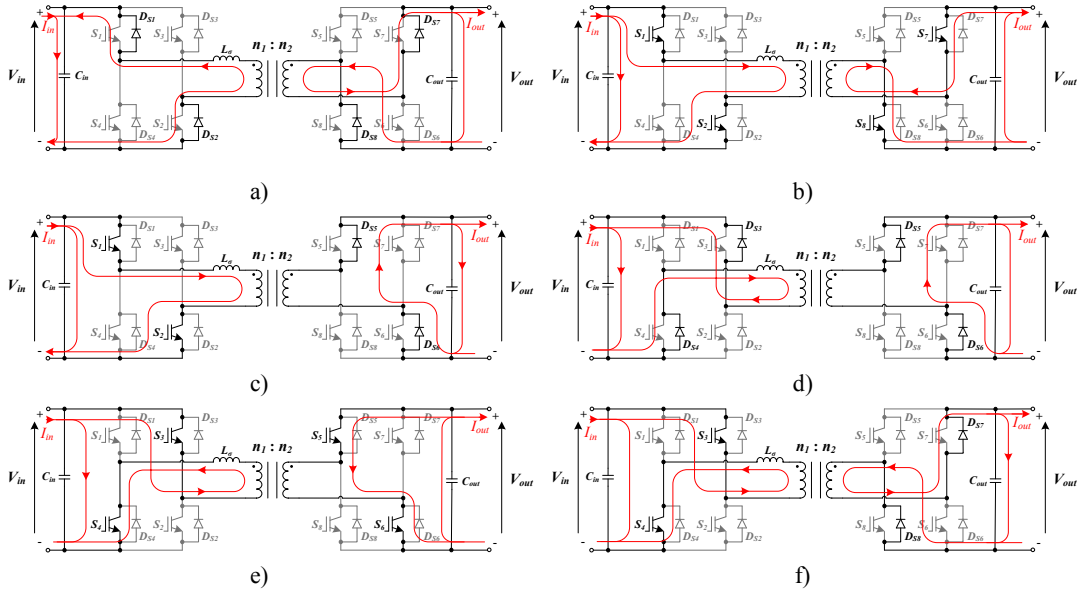


Fig 3.76. Currents circulating through the dual-active-bridge converter a) when S_1-S_2 are on (current circulates through the freewheel diodes D_{S1}-D_{S2}) and S_7-S_8 are on (current circulates through the freewheel diodes D_{S7}-D_{S8}), b) when S_1-S_2 are on and S_7-S_8 are on, c) when S_1-S_2 are on and S_5-S_6 are on (current circulates through the freewheel diodes D_{S5}-D_{S6}), d) when S_3-S_4 are on (current circulates through the freewheel diodes D_{S3}-D_{S4}) and S_5-S_6 are on (current circulates through the freewheel diodes D_{S5}-D_{S6}), e) when S_3-S_4 are on and S_5-S_6 are on, and f) when S_3-S_4 are on and S_7-S_8 are on (current circulates through the freewheel diodes D_{S7}-D_{S8}).

The leakage inductance current and voltage waveforms are depicted in Fig 3.77. As it can be noticed, the current through the transformer is alternating. Thus, the magnetization of the transformer is bidirectional and in consequence, the utilization of the transformer is good. However, a control strategy must guarantee that the average voltage applied to the transformer is zero in order to prevent its saturation.

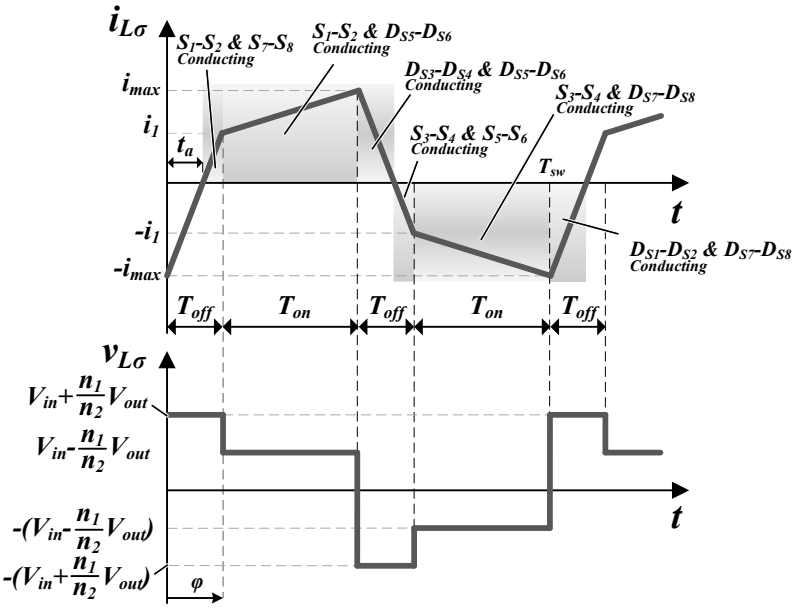


Fig 3.77. Typical voltage and current waveforms in the leakage inductance (L_σ) of the dual-active-bridge converter.

The time interval at which there is no power transference from the input to the output is given by the phase-shift (φ) of the square wave voltages:

$$T_{off} = \frac{\varphi \cdot T_{sw}}{2 \cdot \pi} \tag{3.247}$$

where T_{sw} is the switching period.

While the time interval at which the power is transferred from the input to the output is:

$$T_{on} = \frac{T_{sw}}{2} - T_{off} = \frac{T_{sw}}{2} \cdot \left(1 - \frac{\varphi}{\pi}\right) \tag{3.248}$$

From Fig 3.77, the relation between the current through the leakage inductance and its voltage is provided by:

$$v_{L\sigma} = L_{\sigma} \cdot \frac{\Delta i}{\Delta t} \rightarrow \left(V_{in} + V_{out} \cdot \frac{n_1}{n_2}\right) = L_{\sigma} \cdot \frac{\left(i_{\max} + i_1\right)}{T_{off}} \tag{3.249}$$

$$v_{L\sigma} = L_{\sigma} \cdot \frac{\Delta i}{\Delta t} \rightarrow \left(V_{in} - V_{out} \cdot \frac{n_1}{n_2}\right) = L_{\sigma} \cdot \frac{\left(i_{\max} - i_1\right)}{T_{on}} \tag{3.250}$$

where V_{in} and V_{out} are the average input and output voltages, n_2/n_1 is the turn ratio of the MFT (cf. Fig 3.74), i_{max} is the maximum current through the leakage inductance and i_1 is the value of the current at the end of the T_{off} time interval (cf. Fig 3.77).

Developing Eq. (3.249) and Eq. (3.250), the values of i_1 and i_{max} can be calculated:

$$i_1 = \frac{\left(V_{in} \cdot \left(2 \cdot \varphi - \pi\right) + V_{out} \cdot \frac{n_1}{n_2} \cdot \pi\right) \cdot T_{sw}}{4 \cdot \pi \cdot L_{\sigma}} \tag{3.251}$$

$$i_{\max} = \frac{\left(V_{in} \cdot \pi + V_{out} \cdot \frac{n_1}{n_2} \cdot \left(2 \cdot \varphi - \pi\right)\right) \cdot T_{sw}}{4 \cdot \pi \cdot L_{\sigma}} \tag{3.252}$$

The value of the input current (I_{in}) is derived from the waveforms in Fig 3.77 taking into account the sense of the current circulating through the input side H-bridge (see Fig 3.76):

$$\begin{aligned} I_{in} &= \frac{2}{T_{sw}} \cdot \left[\left(\frac{\varphi \cdot T_{sw}}{2 \cdot \pi} - t_a\right) \cdot \frac{i_1}{2} + \frac{\left(i_{\max} + i_1\right)}{2} \cdot \frac{T_{sw}}{2} \cdot \left(1 - \frac{\varphi}{\pi}\right) - \frac{i_{\max}}{2} \cdot t_a\right] \Rightarrow \\ &\Rightarrow I_{in} = \frac{V_{out} \cdot \frac{n_1}{n_2} \cdot T_{sw}}{2 \cdot \pi \cdot L_{\sigma}} \cdot \varphi \cdot \left(1 - \frac{\varphi}{\pi}\right) \end{aligned} \tag{3.253}$$

where t_a is:

$$t_a = \frac{i_{\max}}{\left(i_1 + i_{\max}\right)} \cdot \frac{\varphi \cdot T_{sw}}{2 \cdot \pi} = \frac{\left[V_{in} \cdot \pi + V_{out} \cdot \frac{n_1}{n_2} \cdot \left(2 \cdot \varphi - \pi\right)\right] \cdot T_{sw}}{4 \cdot \pi \cdot \left(V_{in} + V_{out} \cdot \frac{n_1}{n_2}\right)} \tag{3.254}$$

As the input power depends on the average input current as well as the DC bus voltage, the same statement as in [23] can be obtained from Eq. (3.253) assuming ideal operation with no power losses:

$$P_{out} = P_{in} = V_{in} \cdot I_{in} = \frac{{V_{in}}^2 \cdot T_{sw}}{2 \cdot \pi \cdot L_\sigma} \cdot d \cdot \varphi \cdot \left(1 - \frac{\varphi}{\pi}\right) \tag{3.255}$$

$$d = \frac{V_{out} \cdot n_1}{V_{in} \cdot n_2} \tag{3.256}$$

As it can be noticed, the power transfer is dependent on the phase-shift φ. In turn, if Eq. (3.255) is plotted in function of the phase-shift (see Fig 3.78), it can be observed that the maximum power transference is given at $\varphi=\pi/2$.

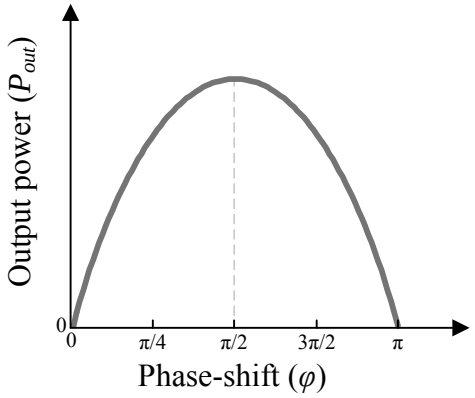


Fig 3.78. Output power of the dual-active-bridge converter in function of the phase-shift.

On the other hand, the value of the leakage inductance L_σ can be derived from Eq. (3.249):

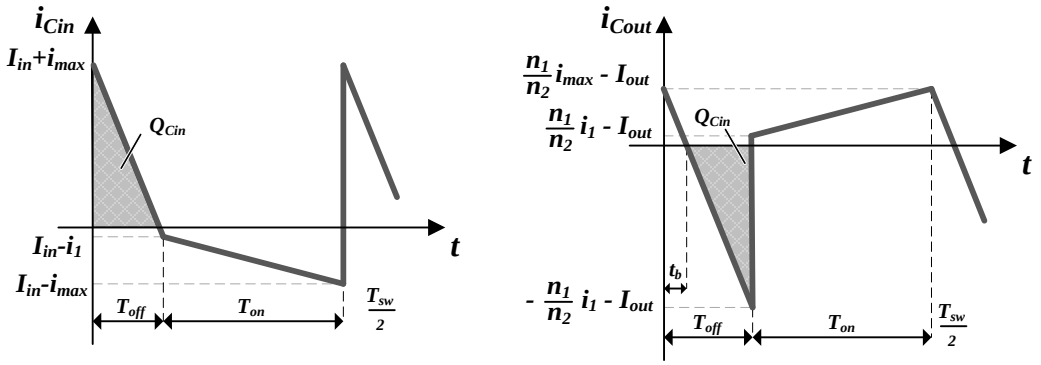
$$L_\sigma = \left(V_{in} + V_{out} \cdot \frac{n_1}{n_2}\right) \cdot \frac{\varphi \cdot T_{sw}}{2 \cdot \pi \cdot \left(i_{\max} + i_1\right)} \tag{3.257}$$

Under the assumption of constant input and output currents (I_{in} and I_{out}), Fig 3.79 shows the waveforms of the currents through input and output capacitors. Thus, the input and output side capacitors can be derived from the waveforms in Fig 3.79:

$$C_{in} = \frac{Q_{Cin}}{\Delta v} = \frac{\varphi \cdot T_{sw} \cdot \left(I_{in} + i_{\max}\right)^2}{8 \cdot \pi \cdot \left(i_{\max} + i_1\right) \cdot \Delta v_{Cin}} \tag{3.258}$$

$$C_{out} = \frac{Q_{Cout}}{\Delta v} = \left(i_1 \cdot \frac{n_1}{n_2} + I_{out}\right) \cdot \left(i_1 + I_{out} \cdot \frac{n_2}{n_1}\right) \cdot \frac{\varphi \cdot T_{sw} \cdot n_2}{8 \cdot \pi \cdot \left(i_{\max} + i_1\right) \cdot \Delta v_{Cout} \cdot n_1} \tag{3.259}$$

where Δv_{Cin} and Δv_{Cout} are the half of the desired peak to peak voltage ripple in the input and output capacitors.



a) b)

Fig 3.79. Currents circulating through a) the input capacitor and b) the output capacitor of the dual-active-bridge converter.

Furthermore, the expressions for the maximum energy stored by the passive elements, their maximum voltage stress and the *rms* currents circulating through them can be derived from the waveforms in Fig 3.77 and Fig 3.79. Table 3.38 summarizes the latter expressions.

TABLE 3.38

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

Element	Maximum stored energy	*rms* current	Maximum voltage stress
C_{in}	$\frac{1}{2}\cdot C_{in}\cdot\left(V_{in}+\Delta v_{Cin}\right)^2$	$\sqrt{\frac{\chi}{3\cdot\pi}}$	$\left(V_{in}+\Delta v_{Cin}\right)$
L_σ	$\frac{1}{2}\cdot L_\sigma\cdot {i_{\max}}^2$	$\left(i_{\max}+i_1\right)\cdot\sqrt{\frac{\kappa}{3\cdot\pi}}$	$\approx\left(V_{in}+V_{out}\cdot\frac{n_1}{n_2}\right)$
C_{out}	$\frac{1}{2}\cdot C_{out}\cdot\left(V_{out}+\Delta v_{Cout}\right)^2$	$\sqrt{{I_{out}}^2+\frac{n_1\cdot\rho}{3\cdot n_2}}$	$\left(V_{out}+\Delta v_{Cout}\right)$

$$\chi=\left[\varphi\cdot\left(\frac{\left(i_{\max}+I_{in}\right)^3}{\left(i_{\max}+i_1\right)}+\left(I_{in}-i_1\right)^2\cdot\left(\frac{\left(i_1-i_{\max}-2\cdot I_{in}\right)}{\left(i_{\max}+i_1\right)}\right)\right)+\frac{\left(\pi-\varphi\right)}{\left(i_1-i_{\max}\right)}\cdot\left(\left(I_{in}-i_{\max}\right)^3-\left(I_{in}-i_1\right)^3\right)\right]$$

$$\kappa=\left[\left(1-i_{\max}\cdot i_1\right)\cdot\left(\pi-\varphi\right)+\frac{\varphi\cdot\left({i_{\max}}^3+{i_1}^3\right)}{\left(i_{\max}+i_1\right)^3}\right]$$

$$\rho=\left[\frac{n_1}{n_2}\cdot\left(\left(i_{\max}+i_1\right)^2-\frac{i_{\max}\cdot i_1}{\pi}\cdot\left(\pi+2\cdot\varphi\right)\right)+\frac{3\cdot I_{out}\cdot i_1}{\pi}\left(2\cdot\varphi-\pi\right)-3\cdot I_{out}\cdot i_{\max}\right]$$

Neglecting the voltage ripple, the semiconductor utilization factor can be calculated from the *rms* currents and maximum voltage expressions in Table 3.39 and Table 3.40:

$$U_f=\frac{P_{Rated}}{4\cdot V_{in}\cdot\left(I_{S1RMS}+I_{Ds1RMS}\right)+4\cdot V_{out}\cdot\left(I_{S5RMS}+I_{Ds5RMS}\right)} \tag{3.260}$$

In Fig 3.80, the semiconductor utilization factor has been illustrated in function of the phase-shift φ. As it can be noticed, the utilization of the semiconductors is maximized

with phase-shifts close to 0 and π. However, as shown by Fig 3.78, the power transference at these points is low, which suggests that the converter is underused. Hence, in spite of the low semiconductor utilization, it is preferable to design the converter for operating with phase-shifts close to $\varphi=\pi/2$, where the maximum power transference is given.

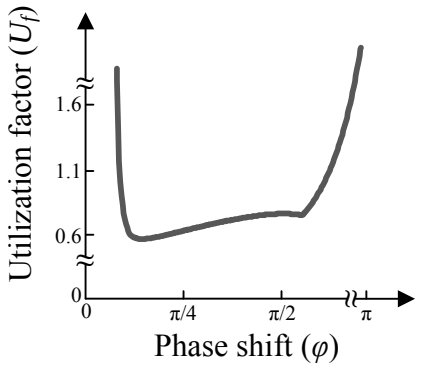


Fig 3.80. S Semiconductor utilization factor of the dual-active-bridge converter.

2.2.17.2 Power losses estimation

The power losses of the converters are calculated estimating the average semiconductor conduction losses of Eq. (3.1) and the average semiconductor switching losses of Eq. (3.2). As the input side transistors conduct the same current, their power losses are the same. This can be applied to the input side freewheel diodes and the output side transistors as well as freewheel diodes. Therefore, power losses are calculated for one semiconductor in each group (S_1, S_5, D_{S1} and D_{S5}). In Table 3.39 and Table 3.40, main current and voltage expressions required to estimate the power losses are summarized. These expressions are obtained from Fig 3.77.

Therefore, average conduction power losses of transistors S_1 (P_{cond_S1}) and S_5 (P_{cond_S5}), and conduction losses of freewheel diodes D_{S1} (P_{cond_Ds1}) and D_{S5} (P_{cond_Ds5}) are given by:

$$P_{cond\_S1} = V_{th}\cdot\left[\frac{i_1}{2}\cdot\left(\frac{\varphi}{2\cdot\pi}-\frac{t_a}{T_{sw}}\right)+\frac{(i_1+i_{\max})}{4}\cdot\left(1-\frac{\varphi}{\pi}\right)\right]+ \\ +\frac{r_d}{3}\cdot\left[{i_1}^2\cdot\left(\frac{\varphi}{2\cdot\pi}-\frac{t_a}{T_{sw}}\right)+\left({i_1}^2+i_{\max}\cdot i_1+{i_{\max}}^2\right)\cdot\left(\frac{1}{2}-\frac{\varphi}{2\cdot\pi}\right)\right] \tag{3.261}$$

$$P_{cond\_S5} = V_{th}\cdot\frac{i_1}{2}\cdot\frac{n_1}{n_2}\cdot\left(\frac{\varphi}{2\cdot\pi}-\frac{t_a}{T_{sw}}\right)+\frac{r_d}{3}\cdot\left(i_1\cdot\frac{n_1}{n_2}\right)^2\cdot\left(\frac{\varphi}{2\cdot\pi}-\frac{t_a}{T_{sw}}\right) \tag{3.262}$$

$$P_{cond\_Ds1} = V_{th}\cdot\frac{i_{\max}}{2}\cdot\frac{t_a}{T_{sw}}+r_d\cdot\frac{{i_{\max}}^2\cdot t_a}{3\cdot T_{sw}} \tag{3.263}$$

$$P_{cond\_Ds5} = V_{th} \cdot \frac{n_1}{n_2} \cdot \left[\frac{i_{\max}}{2} \cdot \frac{t_a}{T_{sw}} + \frac{(i_1 + i_{\max})}{4} \cdot \left(1 - \frac{\varphi}{\pi}\right) \right] + r_d \cdot \frac{c}{3 \cdot T_{sw}} + \frac{r_d}{3} \cdot \left(\frac{n_1}{n_2}\right)^2 \cdot \left[\left({i_1}^2 + i_{\max} \cdot i_1 + {i_{\max}}^2 \right) \cdot \left(\frac{1}{2} - \frac{\varphi}{2 \cdot \pi} \right) + {i_{\max}}^2 \cdot \frac{t_a}{T_{sw}} \right] \quad (3.264)$$

where r_d and V_{th} are the on-state resistance and the threshold voltage of each semiconductor.

TABLE 3.39

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS OF THE INPUT SIDE H-BRIDGE

Current and voltage expressions	**Transistors** S_1-S_2-S_3-S_4	**Freewheel diodes** D_{S1}-D_{S2}-D_{S3}-D_{S4}
Average current (I_{ave})	$\left[\frac{i_1}{2} \cdot \left(\frac{\varphi}{2 \cdot \pi} - \frac{t_a}{T_{sw}} \right) + \frac{(i_1 + i_{\max})}{4} \cdot \left(1 - \frac{\varphi}{\pi}\right) \right]$	$\frac{i_{\max}}{2} \cdot \frac{t_a}{T_{sw}}$
rms current (I_{rms})	$\sqrt{\frac{1}{3} \cdot \left[{i_1}^2 \cdot \left(\frac{\varphi}{2 \cdot \pi} - \frac{t_a}{T_{sw}} \right) + \left({i_1}^2 + i_{\max} \cdot i_1 + {i_{\max}}^2 \right) \cdot \left(\frac{1}{2} - \frac{\varphi}{2 \cdot \pi} \right) \right]}$	$i_{\max} \cdot \sqrt{\frac{t_a}{3 \cdot T_{sw}}}$
Maximum current (i_{max})	$i_{\max}$	$i_{\max}$
Turn-off switched current (i_{off})	$i_{\max}$	0
Maximum voltage (v_{max})	$(V_{in} + \Delta v_{Cin})$	$(V_{in} + \Delta v_{Cin})$
Turn-off switched voltage (v_{off})	$(V_{in} - \Delta v_{Cin})$	0

In this converter, transistors operate under ZVS conditions and freewheel diodes operate under ZCS conditions. Thus, transistors turn-on losses and freewheel diodes turn-off losses are neglected [23]. In consequence, switching power losses are given by the turn-off losses of transistors:

$$P_{sw\_S1} = \frac{(V_{in} - \Delta v_{Cin})}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,S1} \cdot (i_{\max})^2 + B_{off,S1} \cdot i_{\max} + C_{off,S1} \right) \quad (3.265)$$

$$P_{sw\_S5} = \frac{(V_{out} - \Delta v_{Cout})}{T_{sw} \cdot V_{100FIT}} \cdot \left(A_{off,S5} \cdot \left(i_1 \cdot \frac{n_1}{n_2} \right)^2 + B_{off,S5} \cdot i_1 \cdot \frac{n_1}{n_2} + C_{off,S5} \right) \quad (3.266)$$

where $A_{off,XX}$, $B_{off,XX}$ and $C_{off,XX}$ are the turn-off energy loss characteristic coefficients provided by the manufacturer for the 100FIT test voltage (V_{100FIT}) of each semiconductor switch.

TABLE 3.40
EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS OF THE OUTPUT SIDE H-BRIDGE

Current and voltage expressions	**Transistors** S_5-S_6-S_7-S_8	**Freewheel diodes** D_{S5}-D_{S6}-D_{S7}-D_{S8}
Average current (I_{ave})	$\frac{i_1}{2}\cdot\frac{n_1}{n_2}\cdot\left(\frac{\varphi}{2\cdot\pi}-\frac{t_a}{T_{sw}}\right)$	$\frac{n_1}{n_2}\cdot\left[\frac{i_{\max}}{2}\cdot\frac{t_a}{T_{sw}}+\frac{(i_1+i_{\max})}{4}\cdot\left(1-\frac{\varphi}{\pi}\right)\right]$
rms current (I_{rms})	$i_1\cdot\frac{n_1}{n_2}\cdot\sqrt{\frac{1}{3}\cdot\left(\frac{\varphi}{2\cdot\pi}-\frac{t_a}{T_{sw}}\right)}$	$\frac{n_1}{n_2}\cdot\sqrt{\frac{1}{3}\cdot\left[\left({i_1}^2+i_{\max}\cdot i_1+{i_{\max}}^2\right)\cdot\left(\frac{1}{2}-\frac{\varphi}{2\cdot\pi}\right)+{i_{\max}}^2\cdot\frac{t_a}{T_{sw}}\right]}$
Maximum current (i_{max})	$i_{\max}\cdot\frac{n_1}{n_2}$	$i_{\max}\cdot\frac{n_1}{n_2}$
Turn-off switched current (i_{off})	$i_1\cdot\frac{n_1}{n_2}$	0
Maximum voltage (v_{max})	$\left(V_{out}+\Delta v_{Cout}\right)$	$\left(V_{out}+\Delta v_{Cout}\right)$
Turn-off switched voltage (v_{off})	$\left(V_{out}-\Delta v_{Cout}\right)$	0

2.3 Resonant mode DC-DC converters

The main benefit of resonant mode DC-DC converters resides in the reduction of the switching stress due to the soft switching conditions they provide (zero current and/or zero voltage switching). Consequently, switching power losses can be decreased and therefore, higher efficiencies and lower EMIs are achieved. In turn, switching frequency could be also increased in order to reduce the volume of the passive components. However, their main drawback is the voltage/current stress in passive elements.

Generally speaking, resonant mode DC-DC converters can be divided in two groups: resonant load converters and resonant switch (or quasi-resonant) converters [2]. In the latter, the resonance is given in a smaller time interval than the switching period. This way, the resonance is used to adapt the voltages and/or currents through the semiconductors so as to achieve zero voltage switching (ZVS) and/or zero current switching (ZCS) conditions. Conversely, in resonant load type converters, a resonant-tank is excited to create oscillating voltages and currents that last all the switching period. Controlling the switching instants of the semiconductors, a ZCS or a ZVS can be achieved.

In this section, only resonant load DC-DC converters are considered. In these converters, the amplitude of the output voltage is defined by the characteristic DC voltage gain (voltage gain versus frequency) of the resonant-tank and the frequency of the applied voltage. Furthermore, the resonant-tank acts as a filter, letting pass to determined frequencies. If a DC output voltage is required, a rectifier must be used at the output stage. The transferred power can be controlled varying the frequency of the square wave voltage. However, despite of its effectiveness, this control method increases the difficulty of the design of the passive elements [24]. This drawback can be addressed if the converter is operated at a constant frequency and the applied fundamental voltage is controlled varying the duty cycle [2].

In Fig 3.81, the general layout considered for the resonant load converters is shown. A H-bridge converter has been considered as the input side inverter. Despite of the higher semiconductor number, this converter has a better switch utilization than the half-bridge inverter [2]. In addition, a diode bridge rectifier is considered in the output stage due to its reliability and simplicity.

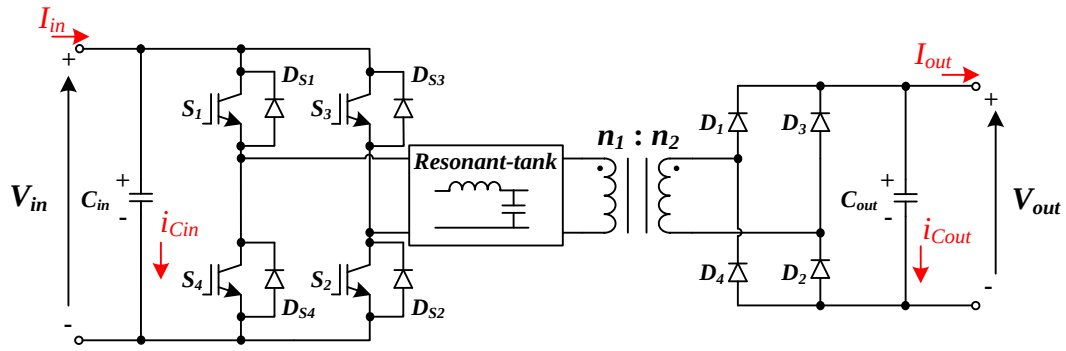


Fig 3.81. Layout of the considered resonant load DC-DC converters.

As stated in [25-26], the characteristics of the resonant-tank depend on its topology. When two or more passive elements are connected in series (see Fig 3.82a), the resonant-tank performs as a band-pass filter. If the switching frequency is close to the resonance frequency, this topology offers low semiconductor switching losses and low energy circulating through the tank. On the other hand, when the passive elements are connected as shown by Fig 3.82b, the resonant-tank performs as a low-pass filter or a high-pass filter. If a capacitor is shunt connected, a low-pass filter is obtained, whereas if an inductor is shunt connected, a high-pass filter is obtained. This topology is a good choice if a variable output voltage is required. A notch filter is obtained when the elements are parallel connected as depicted in Fig 3.82c and Fig 3.82d. The notch filter is useful to provide soft start-up to the converter and for protecting it against load side short circuits. As it will be discussed later in this section, the resonant-tanks resulting from the combination of the basic topologies of Fig 3.82 maintain the characteristics of each basic topology.

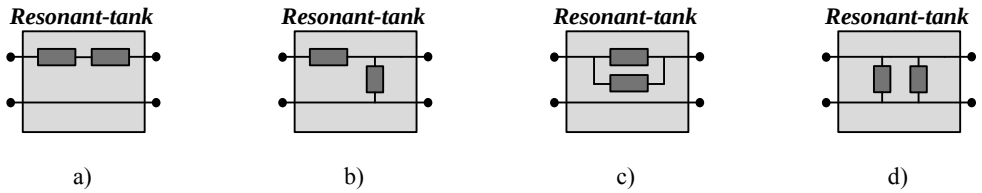


Fig 3.82. Different resonant-tank topologies in which each dark-greyed box represents one or more passive elements.

In this section, 10 different resonant-tank topologies are analysed and discussed. In order to understand the behaviour of each tank, the DC voltage gain of each converter is calculated. With these DC gain functions, the resonant-tank can be designed to operate at any input and output voltages. Contrarily to the switch mode converters, it is easier and more straightforward to calculate the power losses, and input and output DC bus capacitances (C_{in} and C_{out} of Fig 3.81 respectively) by means of simulation (instead of estimating them through analitycal approaches). In consequence, those analytical expressions are not discussed in this chapter.

2.3.1 Series LC resonant-tank

The series LC resonant-tank shown in Fig 3.83a is a simple tank that can use the leakage inductance of the MFT as part of the resonant-tank. Thereby, the total the amount of components of the converter is reduced. Generally, the converter that includes this resonant-tank is known as series-resonant converter [2, 8].

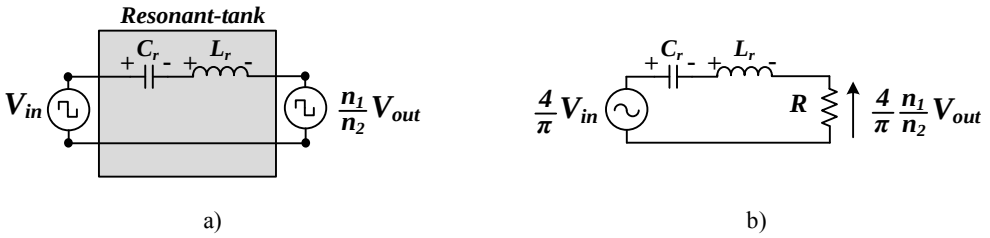


Fig 3.83. a) Series LC resonant-tank. b) Equivalent circuit of the series-resonant converter for fundamental voltage.

From Fig 3.83a, the impedance of the resonant-tank can be calculated:

$$Z_R = j \cdot \omega \cdot L_r + \frac{1}{j \cdot \omega \cdot C_r} \tag{3.267}$$

where ω is the fundamental frequency of the input square wave voltage and depends on the switching frequency (f_{sw}) of the converter:

$$\omega = 2 \cdot \pi \cdot f_{sw} \tag{3.268}$$

The frequency at which the impedance of the resonant-tank is zero is known as the resonance frequency (f_0):

$$f_0 = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{1}{L_r \cdot C_r}} \tag{3.269}$$

In turn, the impedance of each passive element at the resonance frequency is known as the characteristic impedance (Z_0):

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \tag{3.270}$$

In a first approach, assuming a purely resistive load and neglecting the non-linear behaviour of the output rectifier (diode bridge and output capacitive filter, C_{out}), the equivalent circuit of the series-resonant converter can be drawn as in Fig 3.83b. From this equivalent circuit, the DC voltage gain can be calculated as:

$$\frac{V_R}{V_{in}} = \frac{V_{out} \cdot n_1}{V_{in} \cdot n_2} = \frac{1}{1 + j \cdot \omega_n \cdot Q_s \cdot \left(1 - \frac{1}{{\omega_n}^2}\right)} \tag{3.271}$$

where V_{in} and V_{out} are the input and output voltages in the converter, n_1/n_2 is the turn ratio of the MFT (see Fig 3.81), ω_n is the normalized frequency (see Eq. (3.272)) and Q_s is the load factor, which represents the load intensity (see Eq. (3.273)). Therefore, the higher Q_s the heavier is the load and conversely, the lower Q_s the lighter is the load.

$$\omega_n = \frac{f_{sw}}{f_0} \tag{3.272}$$

$$Q_s = \frac{Z_0}{R} = \frac{Z_0}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2}\right)^2} \tag{3.273}$$

In Fig 3.84 the DC voltage gain is illustrated in function of the normalized frequency and for different load factors. As it can be noticed, the resonant-tank performs as a band-pass filter with no voltage gain (the output voltage of the resonant-tank is, at most, the same as the input voltage). With light loads, the output voltage cannot be regulated by varying the frequency. So, duty cycle control is preferred. Conversely, the output voltage varies dramatically with heavy loads, especially, with switching frequencies close to the resonance frequency. For convenience, this resonance frequency will be named as series resonance frequency (SRF). At SRF and independently of the load intensity, the DC voltage gain is always equal to 1 and the energy circulating through the tank is minimum.

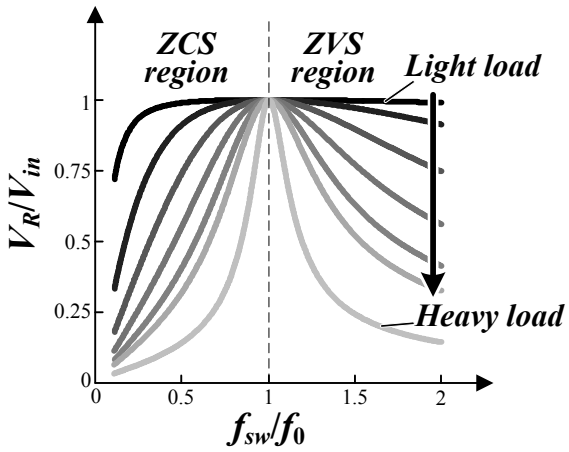


Fig 3.84. DC voltage gain of the series-resonant converter.

On the other hand, two regions are distinguished in Fig 3.84, the zero current switching (ZCS) region and the zero voltage switching (ZVS) region. When the switching frequency is lower than the SRF, the resonant-tank behaves as a capacitor, Eq. (3.267), and the current through the tank leads the input voltage (cf. Fig 3.85a). Therefore, input side transistors are turned-on in hard switching conditions while the turn-off is given in ZCS conditions. Freewheel diodes are turned-off under hard switching conditions. Furthermore, when the switching frequency is lower than $f_0/2$, the current in the resonant-tank result discontinuous. The commutations of all the switches are given at ZCS conditions, so, switching losses are zero. If the power transmitted under these DCM conditions is high, the maximum conduced current can achieve relatively high values.

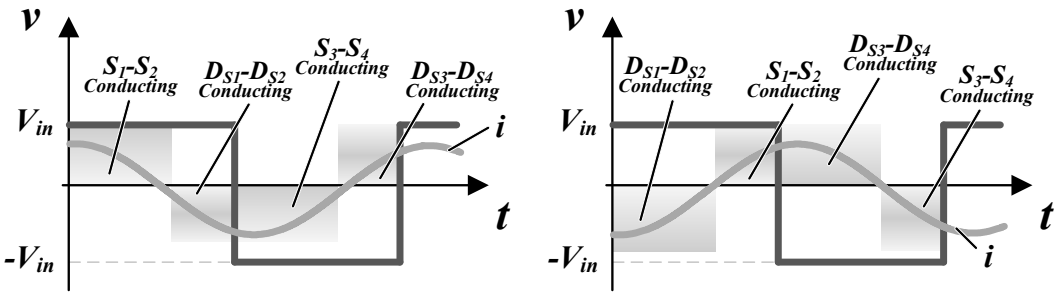


Fig 3.85. Voltage applied to the resonant-tank of the series-resonant converter and the current circulating through it when a) the resonant-tank behaves as a capacitor and b) when the resonant-tank behaves as an inductor.

Conversely, when the switching frequency is higher than the resonance frequency, the resonant-tank behaves as an inductor (cf. Fig 3.85b). Thus, the current through the tank lags the input voltage. In consequence, input side transistors are turned-on in ZVS conditions and freewheel diodes are turned-off under soft switching conditions. The turn-off of the transistors is given under hard switching conditions. As the ZVS turn-on condition allows the use of snubbers to reduce the turn-off losses of the transistors as well as the diode switching stress, the operation in ZVS region is preferred.

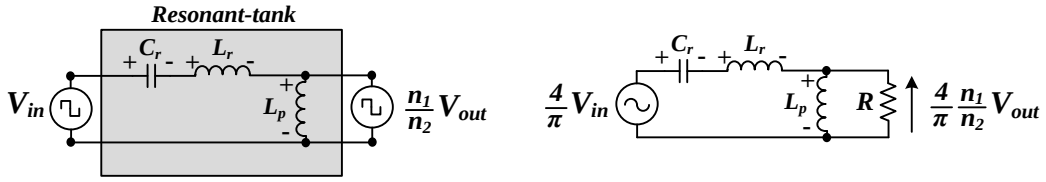
The power losses of the converter are minimized when it operates with a switching frequency close to the SRF. In theory, if the converter operates at the SRF, the impedance of the resonant-tank is zero and the voltage is in phase with the current. This leads to negligible switched currents. However, if snubbers are used, the switching frequency must be slightly higher than the SRF to guarantee the operation in the ZVS region and avoid the operation in the ZCS region.

2.3.2 Three-element resonant-tanks

Resonant-tanks with three passive elements provide the ability to combine and exploit the advantages of two basic tank topologies (cf. Fig 3.82).

2.3.2.1 LLC

The LLC resonant-tank of Fig 3.86a is one of the most popular tanks in resonant mode DC-DC converters [2, 18, 26-29]. This resonant-tank is a combination of the series and parallel tanks in Fig 3.82a and Fig 3.82b. Therefore, it can be deduced that the LLC tank behaves as a combination of a band-pass filter and a high-pass or low-pass filter (this will be discussed later in this section). One advantage of this resonant-tank is that it can use the leakage inductance and the magnetizing inductance of the MFT as part of the resonant-tank. In that case, the transformer must be designed thoroughly to that end. The resonant mode converter composed of this resonant-tank is known as LLC converter.



a) b)

Fig 3.86. a) LLC resonant-tank. b) Equivalent circuit of the LLC converter for fundamental voltage.

The equivalent circuit shown in Fig 3.86b makes possible to obtain the DC gain voltage of this converter assuming a purely resistive load and neglecting the non-linearity of the rectifier stage (output diode bridge and C_{out} capacitor):

$$\frac{V_R}{V_{in}} = \frac{V_{out} \cdot n_1}{V_{in} \cdot n_2} = \frac{j \cdot \omega_n \cdot Q_1}{j \cdot \omega_n \cdot \left(1 + Q_1 - \frac{1}{\omega_n^{\,2}}\right) + Q_1 \cdot Q_s \cdot \left(1 - \omega_n^{\,2}\right)} \tag{3.274}$$

where V_{in} and V_{out} are the input and output voltages in the DC-DC converter, n_1/n_2 is the turn ratio of the MFT (cf. Fig 3.81) and ω_n, Q_1 and Q_s are given by:

$$\omega_n = \frac{f_{sw}}{f_0} = f_{sw} \cdot 2 \cdot \pi \cdot \sqrt{L_r \cdot C_r} \tag{3.275}$$

$$Q_1 = \frac{L_p}{L_r} \tag{3.276}$$

$$Q_s = \frac{Z_0}{R} = \frac{Z_0}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} = \sqrt{\frac{L_r}{C_r}} \cdot \frac{1}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} \tag{3.277}$$

where f_{sw} is the switching frequency of the converter, Q_s is the load factor, f_0 is the SRF and Z_0 is the characteristic impedance of the SRF.

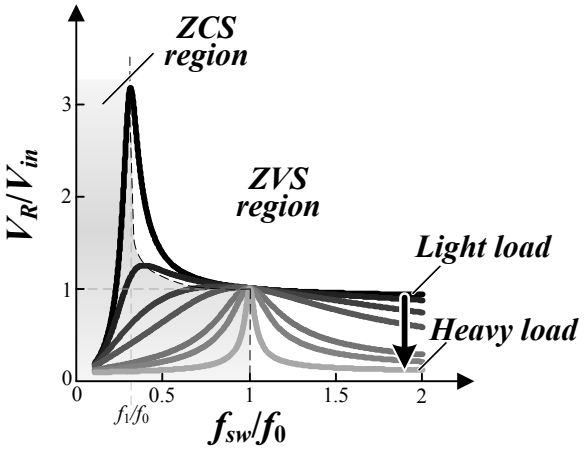


Fig 3.87. DC voltage gain of the LLC converter.

If Eq. (3.274) is graphed in function of ω_n and for different load factors (Q_s), Fig 3.87 is obtained. As it can be noticed, under heavy load conditions the resonant-tank behaves as a band-pass filter. In fact, the DC voltage gain at the SRF is always 1. However, if the converter operates with light loads, the resonant-tank behaves as a high-pass filter. The frequency at which the output voltage tend to infinity depends on the relation of the series and parallel connected inductors, Eq. (3.278). For convenience, this resonance frequency will be named as parallel resonance frequency (PRF). Close to PRF, if the converter operates with light loads, it is possible to regulate the output voltage in a wide range. Nevertheless, the operation in frequencies below SRF leads to high oscillating voltages and currents in the passive elements, thereby increasing the switching power losses as well as the amount of stored energy.

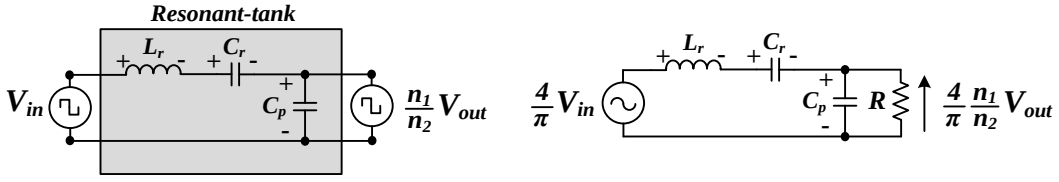
$$f_1 = f_0 \cdot \sqrt{\frac{1}{(Q_1 + 1)}} \tag{3.278}$$

As depicted in Fig 3.87, if the DC voltage gain has a positive slope, the current through the tank leads the input voltage and thus, the transistors operate under ZCS conditions. If the DC voltage gain slope is negative, the current through the tank lags the input voltage and thus, the transistors operate under ZVS conditions. As discussed in the previous section 3.3.1, operating in the ZVS region is more beneficial than operating in the ZCS region since snubbers can be used in transistors, thereby reducing their turn-off switching losses and increasing the overall efficiency of the converter. Moreover, if the converter is

designed to operate with light loads and with frequencies comprehended between the PRF and the SRF (the converter must operate with variable frequency), the benefits of each resonance can be combined. Thus, switching losses are reduced and the energy circulating in the tank is minimum if the converter operates at switching frequencies close to SRF for nominal loads. If the output voltage require to be increased, the switching frequency is reduced and the converter takes advantage of the PRF (the voltage is increased guaranteeing the operation in the ZVS region). In any case, the diodes in the output side rectifier and the freewheel diodes are turned-off under soft switching conditions.

2.3.2.2 LCC

The resonant-tank shown in Fig 3.88a is known as LCC and the DC-DC converter composed of this resonant-tank is known as LCC converter.



a) b)

Fig 3.88. a) LCC resonant-tank. b) Equivalent circuit of the LCC converter for fundamental voltage.

The DC voltage gain is obtained from the equivalent circuit of the LCC converter drawn in Fig 3.88b:

$$\frac{V_R}{V_{in}} = \frac{V_{out} \cdot n_1}{V_{in} \cdot n_2} = \frac{1}{j \cdot \omega_n \cdot Q_s \cdot \left(1 - \frac{1}{\omega_n{}^2}\right) + 1 + Q_1 \cdot \left(1 - \omega_n{}^2\right)} \tag{3.279}$$

where V_{in} and V_{out} are respectively the input and output voltages, n_1/n_2 is the turn ratio of the MFT (cf. Fig 3.81) and ω_n, Q_1 and Q_s are given by:

$$\omega_n = \frac{f_{sw}}{f_0} = f_{sw} \cdot 2 \cdot \pi \cdot \sqrt{L_r \cdot C_r} \tag{3.280}$$

$$Q_1 = \frac{C_p}{C_r} \tag{3.281}$$

$$Q_s = \frac{Z_0}{R} = \frac{Z_0}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2}\right)^2} = \sqrt{\frac{L_r}{C_r}} \cdot \frac{1}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2}\right)^2} \tag{3.282}$$

where f_{sw} is the switching frequency of the converter, Q_s is the load factor, f_0 is the SRF and Z_0 is the characteristic impedance of the SRF.

Fig 3.89 shows the DC voltage gain in function of ω_n and with different load factors (Q_s). With heavy loads, the tank behaves as a band-pass filter while with light loads, the tank behaves as a low-pass filter. At the SRF, independently of the load factor, the DC voltage gain is always 1. Conversely, at the PRF, the output voltage tend to infinity. For a given SRF, this resonance frequency depends on Q_1:

$$f_1 = f_0 \cdot \sqrt{1+\frac{1}{Q_1}} \tag{3.283}$$

The output voltage can be regulated in a wide range if the converter operates close to the PRF. However, the energy stored by the resonant-tank is larger than that operating at the SRF.

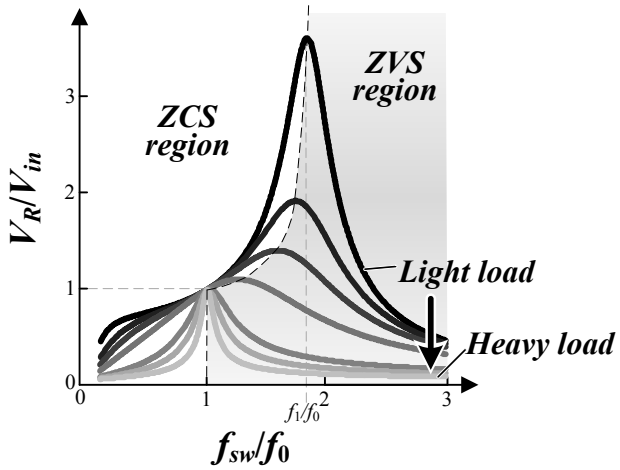


Fig 3.89. DC voltage gain of the LCC converter.

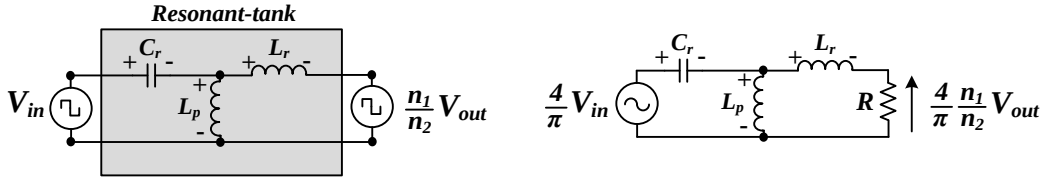
As it can be noticed in Fig 3.89, two different operational regions can be distinguished. When the DC voltage gain has a positive slope, the resonant-tank behaves as a capacitor and thus, the transistors operate under ZCS conditions. If the DC voltage gain slope is negative, the resonant tank behaves as an inductor and thus, the transistors operate under ZVS conditions. Finally, if $f_{sw}/f_0<0.5$, the converter operates in discontinuous current mode (DCM) and in consequence, switching losses can be neglected.

In order to take advantage of the benefits of series and parallel resonance frequencies (low energy circulation through the resonant-tank and voltage regulation capability), the LCC converter must be operated in the ZCS region. In order to achieve negligible switching power losses, it could be interesting to operate with a switching frequency below $f_0/2$ [30].

2.3.2.3 CLL

The CLL resonant-tank is depicted in Fig 3.90a. Similarly to the LLC resonant-tank (section 3.3.2.1), the tank under discussion can use the leakage inductance and the magnetizing inductance of the medium frequency transformer as part of the resonant-

tank. The converter composed of this resonant-tank is patented [31] and for convenience, in this book will be named as CLL converter.



a) b)

Fig 3.90. a) CCL resonant-tank. b) Equivalent circuit of the CLL converter for fundamental voltage.

For a purely resistive load and neglecting the non-linear behaviour of the output stage rectifier, the equivalent circuit of the CLL converter can be illustrated as in Fig 3.90b. From this circuit, the DC voltage gain is given by:

$$\frac{V_R}{V_{in}} = \frac{V_{out} \cdot n_1}{V_{in} \cdot n_2} = \frac{1}{j \cdot \omega_n \cdot Q_s \cdot \left(1 + \frac{1}{Q_1}\right) \cdot \left(1 - \frac{1}{\omega_n{}^2}\right) + 1 - \frac{1}{\omega_n{}^2 \cdot (1 + Q_1)}} \tag{3.284}$$

where V_{in} and V_{out} are respectively the input and output voltages in the DC-DC converter, n_1/n_2 is the turn ratio of the MFT (cf. Fig 3.81) and ω_n, Q_1 and Q_s are given by:

$$\omega_n = \frac{f_{sw}}{f_0} = f_{sw} \cdot 2 \cdot \pi \cdot \sqrt{\frac{L_r \cdot L_p \cdot C_r}{(L_r + L_p)}} \tag{3.285}$$

$$Q_1 = \frac{L_p}{L_r} \tag{3.286}$$

$$Q_s = \frac{Z_0}{R} = \frac{Z_0}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2}\right)^2} = \sqrt{\frac{L_r \cdot L_p}{C_r \cdot (L_r + L_p)}} \cdot \frac{1}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2}\right)^2} \tag{3.287}$$

where f_{sw} is the switching frequency of the converter, Q_s is the load factor, f_0 is the SRF and Z_0 is the characteristic impedance of the SRF.

Fig 3.91 is obtained from Eq. (3.284). As illustrated in Fig 3.91, the tank behaves as a band-pass filter with heavy loads, whereas with light loads, it behaves as a high-pass filter. Conversely to the resonant-tanks discussed previously, the DC voltage gain of this tank at SRF is not equal to 1. This voltage gain depends on the relation between the parallel and series connected inductors:

$$SRF_G = 1 + \frac{1}{Q_1} \tag{3.288}$$

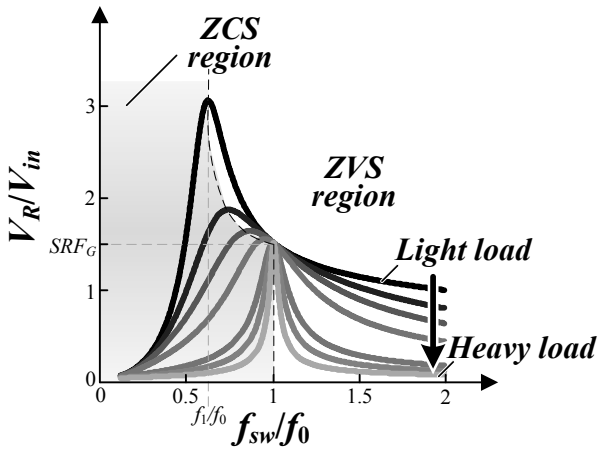


Fig 3.91. DC voltage gain of the CCL converter.

The PRF at which the output voltage tends to infinity is given by:

$$f_1 = f_0 \cdot \sqrt{\frac{1}{(Q_1 + 1)}} \tag{3.289}$$

It must be highlighted that to achieve a unity gain at the SRF_G, a large shunt inductor is required and in consequence, the tank will perform as a series-resonant tank (the effect of the PRF will be negligible unless the converter operates with very light loads).

Depending on the switching frequency, the CLL converter can operate under ZCS or ZVS conditions. If the converter is designed to operate with a light load between PRF and SRF, the output voltage can be regulated in a wide range and the transistors operate under ZVS conditions. At nominal conditions, the converter can operate close to SRF thereby reducing the switching losses and the energy circulating through the tank. Under these conditions, the diodes of the rectifier bridge as well as the freewheel diodes operate under soft switching conditions.

2.3.2.4 LCL type 1

Fig 3.92a shows the LCL type 1 resonant-tank. Since it has an inductive element connected in series with the load, the leakage inductance of the medium frequency transformer could be integrated in the tank in order to optimize the converter design.

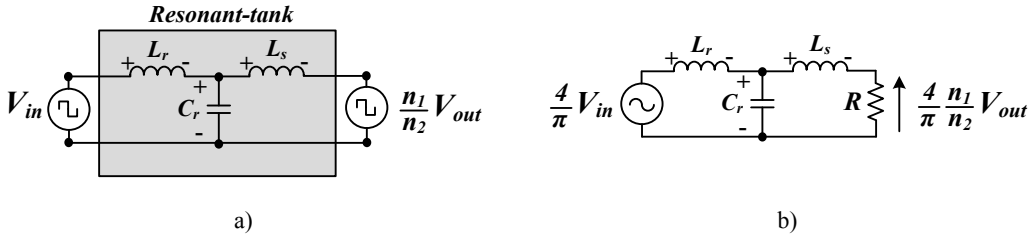


Fig 3.92. a) LCL type 1 resonant-tank. b) Equivalent circuit of the LCL type 1 converter for fundamental voltage.

For the resonant-tank analysis, a purely resistive load has been assumed. In consequence, its equivalent circuit can be depicted as in Fig 3.92b, from which, the DC voltage gain is obtained:

$$\frac{V_R}{V_{in}} = \frac{V_{out} \cdot n_1}{V_{in} \cdot n_2} = \frac{1}{j \cdot \omega_n \cdot Q_s \cdot \left(1 + Q_1 - Q_1 \cdot \omega_n{}^2\right) + 1 - \omega_n{}^2} \tag{3.290}$$

where V_{in} and V_{out} are respectively the input and output DC voltages in the DC-DC converter, n_1/n_2 is the turn ratio of the MFT (cf. Fig 3.81) and ω_n, Q_1 and Q_s are given by:

$$\omega_n = \frac{f_{sw}}{f_0} = f_{sw} \cdot 2 \cdot \pi \cdot \sqrt{L_r \cdot C_r} \tag{3.291}$$

$$Q_1 = \frac{L_s}{L_r} \tag{3.292}$$

$$Q_s = \frac{Z_0}{R} = \frac{Z_0}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2}\right)^2} = \sqrt{\frac{L_r}{C_r}} \cdot \frac{1}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2}\right)^2} \tag{3.293}$$

where f_{sw} is the switching frequency of the converter, Q_s is the load factor, f_0 is the PRF and Z_0 is the characteristic impedance of the PRF.

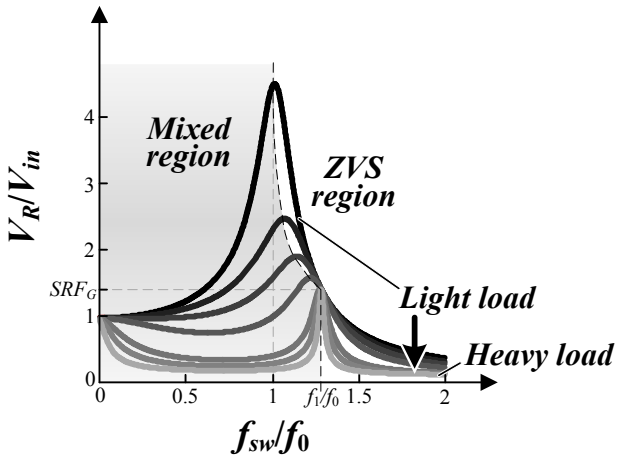


Fig 3.93. DC voltage gain of the LCL type 1 converter.

As it can be noticed in Fig 3.93, the performance of the tank depends on the load. At heavy loads (high Q_s) the tank performs as a band-pass filter, whereas for light loads, it performs as a low-pass filter. The SRF is given by Eq. (3.294) and the voltage gain at this frequency (SRF_G) is given by Eq. (3.295). It can be observed that this voltage gain depends on the relation between the inductive elements. Furthermore, the higher the SRF_G value, the lighter must be the load if significant voltage gain at the PRF is desired.

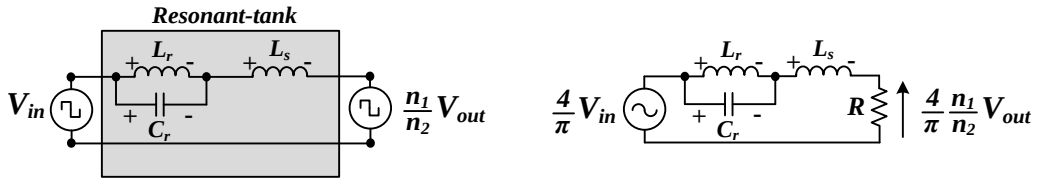
$$f_1 = f_0 \cdot \sqrt{1 + \frac{1}{Q_1}} \tag{3.294}$$

$$SRF_G = Q_1 \tag{3.295}$$

In general, this converter must be designed to operate with light loads and between parallel and series resonance frequencies of the ZVS region. Thus, the energy circulating through the tank is minimum at nominal loads while the output voltage can be increased reducing the switching frequency. Since the converter performs at the ZVS region, snubbers connected in parallel to the transistors can be used. Under this conditions, turn-off losses in the output rectifier are negligible.

2.3.2.5 LCL type 2

The LCL type 2 resonant-tank combines the tank topologies shown in Fig 3.82a and Fig 3.82c (see Fig 3.94a). Therefore, it can be deduced that the tank performs as a combination of a band-pass filter and a notch filter. The latter can be useful for the start-up process of the converter or short circuit protection. With an appropriate transformer design, the series connected inductive element in Fig 3.94a (L_s) could be substituted by the leakage inductance of the MFT. For convenience, the resonant mode converter composed of a LCL type 2 resonant-tank will be named as LCL type 2 converter.



a) b)

Fig 3.94. a) LCL type 2 resonant-tank. b) Equivalent circuit of the LCL type 2 converter for fundamental voltage.

Assuming a resistive load and neglecting the non-linear behaviour of the output rectifier, the equivalent circuit of the LCL type 2 converter can be drawn as in Fig 3.94b. From this circuit, the DC voltage gain is:

$$\frac{V_R}{V_{in}} = \frac{V_{out} \cdot n_1}{V_{in} \cdot n_2} = \frac{1}{j \cdot \omega_n \cdot Q_s \cdot \left(Q_1 + \frac{1}{1-\omega_n^{\,2}} \cdot \right) + 1} \tag{3.296}$$

where V_{in} and V_{out} are respectively the input and output DC voltages in the DC-DC converter, n_1/n_2 is the turn ratio of the MFT (cf. Fig 3.81) and ω_n, Q_1 and Q_s are given by:

$$\omega_n = \frac{f_{sw}}{f_0} = f_{sw} \cdot 2 \cdot \pi \cdot \sqrt{L_r \cdot C_r} \tag{3.297}$$

$$Q_1 = \frac{L_s}{L_r} \tag{3.298}$$

$$Q_s = \frac{Z_0}{R} = \frac{Z_0}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} = \sqrt{\frac{L_r}{C_r}} \cdot \frac{1}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} \tag{3.299}$$

where f_{sw} is the switching frequency of the converter, Q_s is the load factor, f_0 is the notch resonance frequency (NRF) and Z_0 is the characteristic impedance of the NRF.

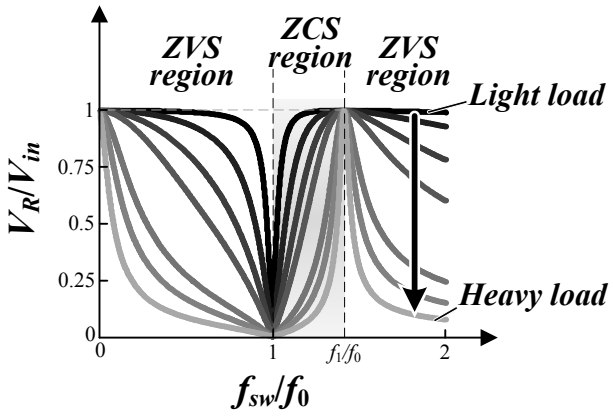


Fig 3.95. DC voltage gain of the LCL type 2 converter.

The DC voltage gain is illustrated in Fig 3.95 for different load factors. As it can be observed, the maximum DC voltage gain of the tank is 1 (obtained at SRF), which means the output voltage in the tank cannot be higher than the input voltage. In turn, it can be noticed that the notch resonance frequency is lower than the series resonance frequency. The latter depends on Q_1 and the NRF as shown by the following expression:

$$f_1 = f_0 \cdot \sqrt{1+\frac{1}{Q_1}} \tag{3.300}$$

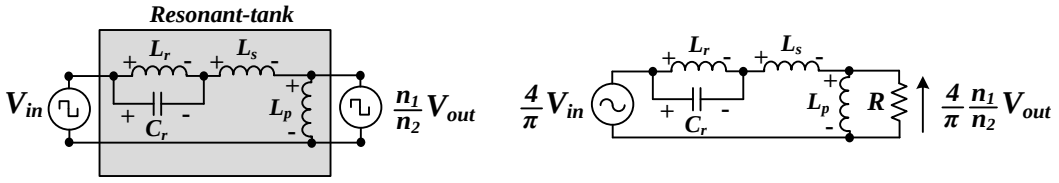
If the converter is operated with variable switching frequencies below SRF and above NRF, the transistors operate under ZCS conditions. At any other frequency, the transistors operate under ZVS conditions and snubbers can be connected in parallel to them. However, in general, the LCL type 2 converter should be designed to take advantage of the characteristics provided by the SRF (low energy circulation and low losses) and the benefits of operating in NRF (soft star-up and short circuit protection). In consequence, the converter should operate in the ZCS region.

2.3.3 Four-element resonant-tanks

Four-element based resonant-tanks combine three different resonant-tank topologies and in consequence, three different resonance frequencies can be obtained. Therefore, the benefits provided by each resonance frequency can be exploited in a single converter.

2.3.3.1 LCLL

In the LCLL resonant-tank of Fig 3.96a, L_s and L_p inductors can be substituted by the leakage inductance and the magnetizing inductance of the medium frequency transformer. In consequence, the number of additional passive elements in the converter is kept low. For convenience, the converter comprising this resonant-tank will be named as LCLL converter.



a) b)

Fig 3.96. a) LCLL resonant-tank. b) Equivalent circuit of the LCLL converter for fundamental voltage.

Under the assumption of a resistive load, the equivalent circuit of the LCLL converter can be drawn as in Fig 3.96b. From this equivalent circuit, the DC voltage gain is obtained as:

$$\frac{V_R}{V_{in}} = \frac{V_{out} \cdot n_1}{V_{in} \cdot n_2} = \frac{1}{j \cdot \omega_n \cdot Q_s \cdot \left(Q_2 + \frac{1}{1-{\omega_n}^2} \right) + \frac{1}{Q_1} \cdot \left(Q_1 + Q_2 + \frac{1}{1-{\omega_n}^2} \right)} \tag{3.301}$$

where V_{in} and V_{out} are the input and output DC voltages in the DC-DC converter, n_1/n_2 is the turn ratio of the MFT (cf. Fig 3.81) and ω_n, Q_1, Q_2 and Q_s are given by:

$$\omega_n = \frac{f_{sw}}{f_0} = f_{sw} \cdot 2 \cdot \pi \cdot \sqrt{L_r \cdot C_r} \tag{3.302}$$

$$Q_1 = \frac{L_p}{L_r} \tag{3.303}$$

$$Q_2 = \frac{L_s}{L_r} \tag{3.304}$$

$$Q_s = \frac{Z_0}{R} = \frac{Z_0}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} = \sqrt{\frac{L_r}{C_r}} \cdot \frac{1}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} \tag{3.305}$$

where f_{sw} is the switching frequency of the converter, Q_s is the load factor, f_0 is the NRF and Z_0 is the characteristic impedance of the NRF.

Fig 3.97 shows the DC voltage gain for different load factors. As it can be observed, the resonant-tank performs as a combination of a notch filter, a high-pass filter and a band-pass filter. At heavy loads, the band-pass filter prevails to the high-pass filter, whereas at light loads the opposite occurs. The DC voltage gain is equal to 1 at the SRF. Furthermore, for a given notch resonance frequency, the parallel and series resonance frequencies are given by Eq. (3.306) and Eq. (3.307) respectively. As it can be noticed, the SRF depends on L_s while the PRF depends on L_s and L_p.

$$f_1 = f_0 \cdot \sqrt{\frac{\left(1 + Q_1 + Q_2\right)}{\left(Q_1 + Q_2\right)}} \tag{3.306}$$

$$f_2 = f_0 \cdot \sqrt{\frac{(1+Q_2)}{Q_2}} \tag{3.307}$$

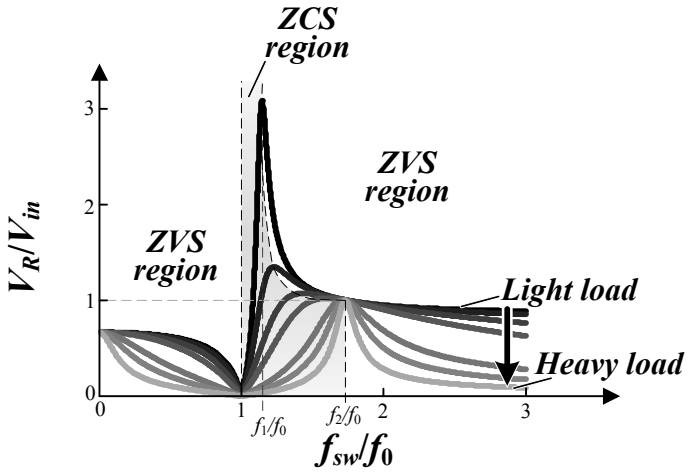
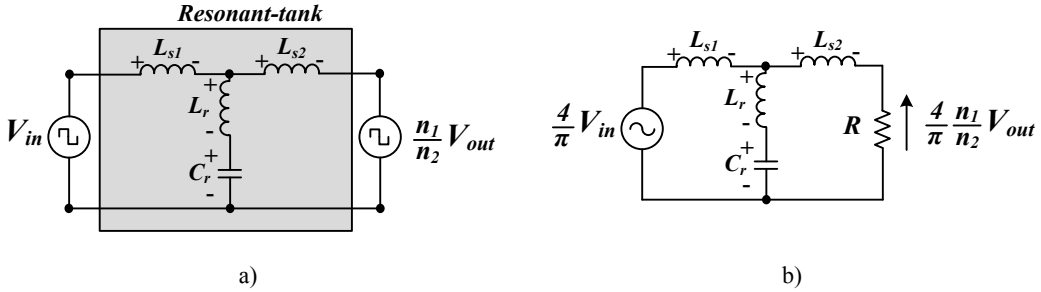


Fig 3.97. DC voltage gain of the LCLL converter.

If the converter is designed to operate in the ZVS region (cf. Fig 3.97), with light loads and with frequencies comprehended between the PRF and the SRF, the benefits of each resonance can be combined (low power losses and low energy circulation at nominal conditions and wide voltage regulation capability). In addition, the rectifier diodes operate under ZCS conditions and the switching losses of the freewheel diodes are negligible. Under this conditions, the ZCS region must be crossed to reach the NRF.

2.3.3.2 LLCL

The LLCL resonant-tank shown in Fig 3.98a can integrate the leakage inductance of the medium frequency transformer and in consequence, the number of passive elements in the converter can be slightly reduced. For convenience, the converter comprising this resonant-tank will be named as LLCL converter.



a) b)

Fig 3.98. a) LLCL resonant-tank. b) Equivalent circuit of the LLCL converter for fundamental voltage.

The performance of the resonant-tank can be easily analyzed under the assumption of a resistive load. Hence, the equivalent circuit of the LLCL converter can be illustrated as in Fig 3.98b, from which, the DC voltage gain is calculated as given by Eq. (3.308).

$$\frac{V_R}{V_{in}} = \frac{V_{out} \cdot n_1}{V_{in} \cdot n_2} = \frac{1}{j \cdot \omega_n \cdot Q_s \cdot \left(Q_1 + Q_2 + \frac{Q_1 \cdot Q_2 \cdot {\omega_n}^2}{{\omega_n}^2 - 1} \right) + 1 + \frac{Q_2 \cdot {\omega_n}^2}{{\omega_n}^2 - 1}} \tag{3.308}$$

where V_{in} and V_{out} are respectively the input and output DC voltages in the DC-DC converter, n_1/n_2 is the turn ratio of the MFT (cf. Fig 3.81) and ω_n, Q_1, Q_2 and Q_s are given by:

$$\omega_n = \frac{f_{sw}}{f_0} = f_{sw} \cdot 2 \cdot \pi \cdot \sqrt{L_r \cdot C_r} \tag{3.309}$$

$$Q_1 = \frac{L_{s2}}{L_r} \tag{3.310}$$

$$Q_2 = \frac{L_{s1}}{L_r} \tag{3.311}$$

$$Q_s = \frac{Z_0}{R} = \frac{Z_0}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} = \sqrt{\frac{L_r}{C_r}} \cdot \frac{1}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} \tag{3.312}$$

where f_{sw} is the switching frequency of the converter, Q_s is the load factor, f_0 is the NRF and Z_0 is the characteristic impedance of the NRF.

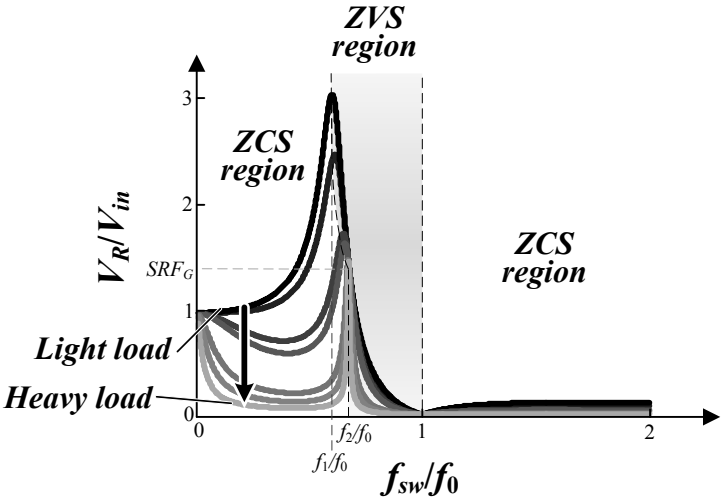


Fig 3.99. DC voltage gain of the LLCL converter.

The DC voltage gain of the tank is illustrated in Fig 3.99. As it can be noticed, DC voltage gain depends on the load factor and the switching frequency of the converter. The DC voltage gain at the series resonance frequency can be derived from Eq. (3.308) and depends on L_{s1} and L_{s2}:

$$SRF_G = \frac{Q_1}{Q_2} = \frac{L_{s2}}{L_{s1}} \tag{3.313}$$

In turn, the parallel and series resonance frequencies are given by Eq. (3.314) and Eq. (3.315) respectively. For a given notch resonance frequency, the PRF depends on L_{s1} while the SRF depends on the two series connected inductive elements.

$$f_1 = f_0 \cdot \sqrt{\frac{1}{(1+Q_2)}} \tag{3.314}$$

$$f_2 = f_0 \cdot \sqrt{\frac{(Q_1+Q_2)}{(Q_1+Q_2+Q_2 \cdot Q_1)}} \tag{3.315}$$

Determined by the inductive or the capacitive behaviour of the resonant-tank, three different regions can be distinguished in Fig 3.99. When the tank performs capacitively, transistors are turned-off in ZCS conditions (ZCS region). Whereas, when the tank performs inductively, transistors are turned-on in ZVS conditions and the reverse recovery current in the freewheel diodes is negligible (ZVS region). In turn, capacitive snubbers can be used to reduce the turn-off switching losses. Operating in the ZVS region, low power losses and low energy storage can be achieved close to the SRF. Furthermore, wide voltage regulation capability is achieved if the converter is designed to operate with light loads and, additionally, the converter can take advantage of the short circuit protection and soft start-up provided by the NRF.

2.3.3.3 CLCL

In the CLCL resonant-tank of Fig 3.100a, the leakage inductance of the medium frequency transformer can be integrated in the tank, thereby reducing the number of passive elements in the converter. In this book, the converter comprising the CLCL resonant-tank is named as CLCL converter.

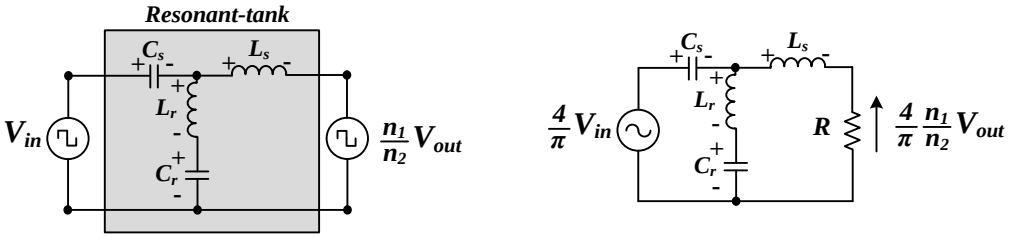


Fig 3.100. a) CLCL resonant-tank. b) Equivalent circuit of the CLCL converter for fundamental voltage.

Assuming a purely resistive load, the equivalent circuit of the CLCL converter can be illustrated as in Fig 3.100b. From this circuit, the DC voltage gain is expressed as:

$$\frac{V_R}{V_{in}} = \frac{V_{out} \cdot n_1}{V_{in} \cdot n_2} = \frac{1}{j \cdot \omega_n \cdot Q_s \cdot \frac{Q_1}{Q_2} \cdot \left(Q_2 + \frac{1}{1-\omega_n{}^2} - \frac{1}{Q_1 \cdot \omega_n{}^2} \right) + 1 + \frac{1}{Q_2} \cdot \frac{1}{1-\omega_n{}^2}} \tag{3.316}$$

where V_{in} and V_{out} are the input and output DC voltages in the DC-DC converter, n_1/n_2 is the turn ratio of the MFT (cf. Fig 3.81) and ω_n, Q_1, Q_2 and Q_s are given by:

$$\omega_n = \frac{f_{sw}}{f_0} = f_{sw} \cdot 2 \cdot \pi \cdot \sqrt{L_r \cdot C_r} \tag{3.317}$$

$$Q_1 = \frac{L_s}{L_r} \tag{3.318}$$

$$Q_2 = \frac{C_s}{C_r} \tag{3.319}$$

$$Q_s = \frac{Z_0}{R} = \frac{Z_0}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} = \sqrt{\frac{L_r}{C_r}} \cdot \frac{1}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} \tag{3.320}$$

where f_{sw} is the switching frequency of the converter, Q_s is the load factor, f_0 is the NRF and Z_0 is the characteristic impedance of the NRF.

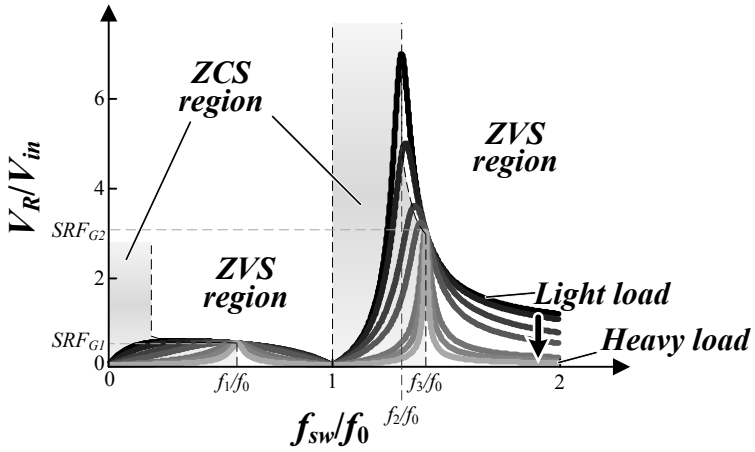


Fig 3.101. DC voltage gain of the CLCL converter.

The DC voltage gain is depicted in Fig 3.101 for different load factors. As it can be noticed, apart from the notch resonance frequency, the tank has three additional resonance frequencies, two series resonance frequencies and a parallel resonance frequency. The DC voltage gains at the series resonance frequencies are provided by:

$$SRF_{G1} = \frac{Q_1 \cdot Q_2 - 1 - Q_1 + \sqrt{\lambda}}{Q_1 \cdot Q_2 - 1 + Q_1 + \sqrt{\lambda}} \tag{3.321}$$

$$SRF_{G2} = \frac{1 - Q_1 \cdot Q_2 + Q_1 + \sqrt{\lambda}}{1 - Q_1 \cdot Q_2 - Q_1 + \sqrt{\lambda}} \tag{3.322}$$

where λ is given as:

$$\lambda = 1 - 2 \cdot Q_1 \cdot (Q_2 - 1 - Q_1 \cdot Q_2) + (Q_1 \cdot Q_2)^2 + {Q_1}^2 \tag{3.323}$$

In turn, the mentioned series and parallel resonance frequencies can be expressed as:

$$f_1 = f_0 \cdot \sqrt{\frac{1+Q_1\cdot(Q_2+1)-\sqrt{(1+Q_1\cdot(Q_2+1))^2-4\cdot Q_2\cdot Q_1}}{2\cdot Q_2\cdot Q_1}} \tag{3.324}$$

$$f_2 = f_0 \cdot \sqrt{1+\frac{1}{Q_2}} \tag{3.325}$$

$$f_3 = f_0 \cdot \sqrt{\frac{1+Q_1\cdot(Q_2+1)+\sqrt{(1+Q_1\cdot(Q_2+1))^2-4\cdot Q_2\cdot Q_1}}{2\cdot Q_2\cdot Q_1}} \tag{3.326}$$

As it can be observed, for a given notch resonance frequency, the parallel resonance frequency depends on the series connected capacitor C_s.

Operating between the PRF and SRF of the ZVS region, low energy storage and low power losses are achieved. Furthermore, the output voltage regulation capability is wide. However, the ZCS region must be crossed to reach the NRF.

2.3.4 CLCLL resonant-tank

With five passive elements the resonant tank provides the benefits of five different resonant frequencies. Conversely, the reliability is reduced due to the high number of passive components. Among the different resonant-tanks composed of five passive elements, only the CLCLL resonant-tank shown in Fig 3.102a has been analyzed due to its capability to transfer the energy though the third harmonic current component. In turn, the leakage and magnetizing inductances of the MFT can be included in the CLCLL tank and therefore, the design of the converter can be optimized in terms of volume. For convenience, the converter comprising this resonant-tank will be named as CLCLL converter.

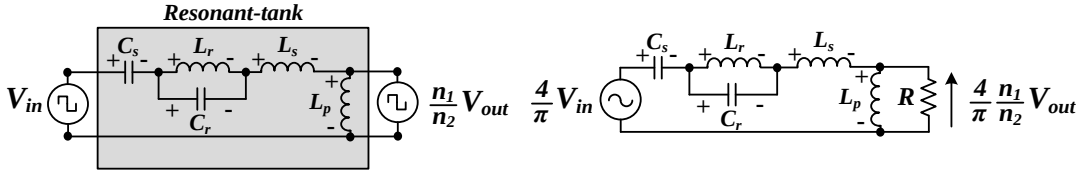


Fig 3.102. a) CLCLL resonant-tank. b) Equivalent circuit of the CLCLL converter for fundamental voltage.

The equivalent circuit of the CLCLL converter can be illustrated as in Fig 3.102b if a resistive load is assumed. From this equivalent circuit, the DC voltage gain of the converter is expressed as shown by Eq. (3.327).

$$\frac{V_R}{V_{in}} = \frac{V_{out} \cdot n_1}{V_{in} \cdot n_2} =$$

$$= \frac{1}{j \cdot \omega_n \cdot Q_s \cdot \left(Q_2 + \frac{1}{1-\omega_n{}^2} - \frac{1}{Q_3 \cdot \omega_n{}^2} \right) + \frac{1}{Q_1} \cdot \left(Q_1 + Q_2 + \frac{1}{1-\omega_n{}^2} - \frac{1}{Q_3 \cdot \omega_n{}^2} \right)} \tag{3.327}$$

where V_{in} and V_{out} are respectively the input and output voltages, n_1/n_2 is the turn ratio of the MFT (cf. Fig 3.81) and ω_n, Q_1, Q_2, Q_3 and Q_s are given by:

$$\omega_n = \frac{f_{sw}}{f_0} = f_{sw} \cdot 2 \cdot \pi \cdot \sqrt{L_r \cdot C_r} \tag{3.328}$$

$$Q_1 = \frac{L_p}{L_r} \tag{3.329}$$

$$Q_2 = \frac{L_s}{L_r} \tag{3.330}$$

$$Q_3 = \frac{C_s}{C_r} \tag{3.331}$$

$$Q_s = \frac{Z_0}{R} = \frac{Z_0}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} = \sqrt{\frac{L_r}{C_r}} \cdot \frac{1}{\frac{8}{P_{out}} \cdot \left(\frac{V_{out} \cdot n_1}{\pi \cdot n_2} \right)^2} \tag{3.332}$$

where f_{sw} is the switching frequency of the converter, Q_s is the load factor, f_0 is the NRF and Z_0 is the characteristic impedance of the NRF.

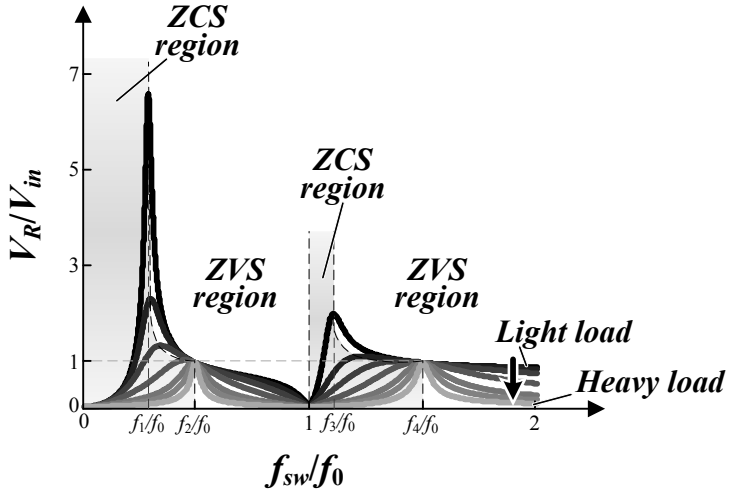


Fig 3.103. DC voltage gain of the CLCLL converter.

The DC voltage gain can be illustrated as in Fig 3.103 for different load factors. As it can be observed, the resonant-tank performs as a combination of a notch filter, two high-pass filters and two band-pass filters. The DC voltage gain at the series resonance frequencies

is always equal to 1 and the parallel and the series resonance frequencies in Fig 3.103 can be derived from Eq. (3.327):

$$f_1 = f_0 \cdot \sqrt{\frac{Q_3 \cdot (Q_2 + Q_1 + 1) + 1 - \sqrt{(Q_3 \cdot (Q_2 + Q_1 + 1) + 1)^2 - 4 \cdot Q_3 \cdot (Q_2 + Q_1)}}{2 \cdot Q_3 \cdot (Q_2 + Q_1)}} \tag{3.333}$$

$$f_2 = f_0 \cdot \sqrt{\frac{Q_3 \cdot (Q_2 + 1) + 1 - \sqrt{(Q_3 \cdot (Q_2 + 1) + 1)^2 - 4 \cdot Q_3 \cdot Q_2}}{2 \cdot Q_3 \cdot Q_2}} \tag{3.334}$$

$$f_3 = f_0 \cdot \sqrt{\frac{Q_3 \cdot (Q_2 + Q_1 + 1) + 1 + \sqrt{(Q_3 \cdot (Q_2 + Q_1 + 1) + 1)^2 - 4 \cdot Q_3 \cdot (Q_2 + Q_1)}}{2 \cdot Q_3 \cdot (Q_2 + Q_1)}} \tag{3.335}$$

$$f_4 = f_0 \cdot \sqrt{\frac{Q_3 \cdot (Q_2 + 1) + 1 + \sqrt{(Q_3 \cdot (Q_2 + 1) + 1)^2 - 4 \cdot Q_3 \cdot Q_2}}{2 \cdot Q_3 \cdot Q_2}} \tag{3.336}$$

As it can be observed in Eq. (3.334) and in Eq. (3.336), the series resonance frequencies depend on Q_2 and Q_3. In order to transfer the energy through the third harmonic component, the frequency of the second band-pass filter (f_4) must be three times higher than the first band-pass frequency (f_2). In consequence, Q_2 and Q_3 must satisfy the following relations:

$$Q_2 = \frac{16}{15} \tag{3.337}$$

$$Q_3 = \frac{5}{3} \tag{3.338}$$

If the converter is designed according to Eq. (3.337) and Eq. (3.338), and is operated in the ZVS region between the first parallel and series resonance frequencies, low energy storage and low power losses are achieved. In addition, the output voltage can be regulated in a wide range. Moreover, the converter can operate in the NRF for providing soft star-up and for protecting it against output side short circuits.

2.4 Summary

In this chapter, several switch mode and resonant mode DC-DC converter topologies have been thoroughly analysed and modelled.

In the first part of this chapter, 17 different switch mode DC-DC converters have been discussed, found among them, converters with or without galvanic isolation capability, and complex or simple (composed of few elements) converters. High reliability and cost reduction can be achieved by using simple converters. However, depending on the input and output voltage, power ranges of the application, etc. more complex converter

topologies must be considered. In a similar way, depending on the secondary side voltage level and galvanic isolation requirements, the use of a converter with a medium frequency transformer that provides galvanic isolation must be assumed. For all switch mode DC-DC converters, design and efficiency evaluation tools are discussed, i.e. analitycal equations for passive element sizing and semiconductor power loss estimation expressions are shown. Furthermore, by means of the semiconductor utilization factor expression, the optimal design point of the converters is calculated.

In the second part of this chapter, 10 different resonant mode DC-DC converters have been studied. All of them provide galvanic isolation by means of a medium frequency transformer. Furthermore, the structure of the analysed converters is the same, a H-bridge at the input side followed by a medium frequency transformer and a diode rectifier at the output side. Thus, the resonant-tank topology is the only differece between the discussed converters. By analysing the transfer function of these resonant-tanks, the DC voltage gain expression of each resonant mode DC-DC converter topology is estimated. Additionally, switching frequency dependent operational regions of the converters are identified, i.e. zero voltage switching and zero current switching regions. Based on the reduction of the semiconductor power losses in these regions, optimal converter design regions are adviced.

All in all, it can be said that this chapter provides the basic tools to select the appropriate DC-DC converter for a given application.

Chapter 3

Medium frequency transformer

The medium frequency transformer is a key component of some of the DC-DC converters analysed in the previous chapter. Generally, although the behaviour of these converters can be understood considering an ideal transformer, the leakage and the magnetizing inductances affect the behaviour of the real converters. So, these parameters must be carefully designed. In addition, the thermal behaviour and the space requirements of the transformers must be considered during the design process. The design of the medium frequency transformer is challenging due to the operation at high frequency and with non-sinusoidal current and voltage waveforms. Therefore, this chapter details the design of the medium frequency transformer.

3.1 Introduction

The transformer is an electrical device that magnetically couples two or more electrical circuits that, generally, have different voltage levels. The design of low frequency transformers is an addressed process [32], however, when the operating frequency increases, the design of the transformer becomes challenging [33]. At high frequencies, the influence of the skin and the proximity effects in the windings is more noticeable. These effects increase the resistance of the conductors and in consequence, the power losses and the temperature of the transformer are increased. The operation at high temperature increases even more the windings resistance. On the other hand, core power

losses also increase along with the frequency. So, it can be concluded that the thermal stability of the medium frequency transformer is a challenging design issue.

The standard transformer design criteria considers sinusoidal current and voltage waveforms. However, the medium frequency transformers (MFTs) in the analysed DC-DC converters (cf. Chapter 3) operate with non-sinusoidal waveforms. This makes invalid the standard design criteria and demands more advanced calculation methods [34]. Hence, this chapter analyses the design of the MFT. The selection of the transformer geometry (core and winding geometry) is discussed and appropriate conductor and core materials are introduced. Furthermore, methods for the calculation of the leakage inductance, the magnetizing inductance and the power losses are described. Finally, a design procedure for the MFT is presented, which, for given technical specifications (nominal power, operational frequency, isolation requirement, etc.), outputs the optimum transformer design.

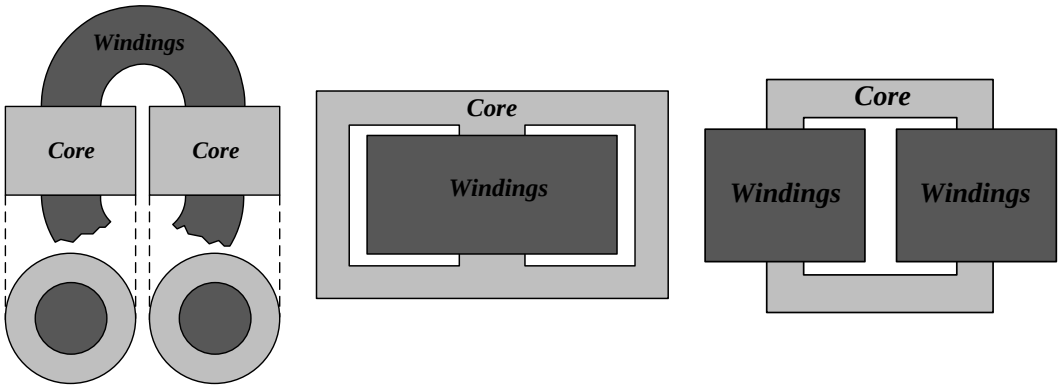
3.2 Geometry of the transformer

Generally speaking, the geometry of the transformer depends on the operational specifications, the core shape and the selected core materials, insulators and conductors.

3.2.1 Core

So far, the constructed MFT prototypes are mainly based on four core materials (amorphous alloys, nanocrystallines, ferrites and silicon-steel materials) and three different transformer geometries (coaxial-type, shell-type and core-type) [35-36]. On the one hand, the use of core materials with high saturation flux minimizes the core cross sectional area (S_{core}) compared to that required by the materials with a low saturation flux, see Eq. (4.12). This leads to a higher power density transformer design. Generally speaking, the saturation flux of amorphous alloys, nanocrystallines and silicon-steel based materials are above 1.1T while that of ferrites is about 0.45T [37]. However, it must be highlighted that due to their demanding manufacturing process, the cost of these materials is higher than the cost of ferrites [36].

On the other hand, coaxial-type transformers (Fig 4.1a) are built through ring shaped core structures while shell-type (Fig 4.1b) and core-type (Fig 4.1c) transformers are built through C-shaped core structures. Due to their orbital shaped geometry, coaxial-type transformers are appropriate for high power applications [34]. Nonetheless, even though they achieve high isolation levels, the difficulty of independently selecting the number of primary and secondary turns due to the coaxial cable they use limits their design flexibility [36]. Therefore, this type transformers are discarded in this book.



a) b) c)

Fig 4.1. a)Typical coaxial-type transformer. b) Typical shell-type transformer. c) Typical core-type transformer.

An advantage of shell-type and core-type transformers is that the use of C-shaped core structures is very common in industrial applications and therefore, its availability is very high. Compared to core-type transformers, shell-type transformers make easier the design of the MFT to achieve a desired leakage inductance. In turn, when the windings in the core-type transformer are placed in different legs, the minimization of the leakage inductance is a very difficult task. In [33] it is stated that for the same volume, a shell-type transformer requires 15% more core material and 36% less winding material than a core-type transformer. As discussed in [35], this suggests that shell-type transformers are more suitable for high voltage applications than core-type transformers. All in all, in the present book only shell-type transformers are considered (cf. Fig 4.2a).

The volume of a shell-type core depends on the required window area (W_a), the core cross sectional area (A_{core}) and the depth of the core (z). As it can be noticed in Fig 4.2b, the window area depends on the diameter of the winding cables, their number of turns, the number of layers and the required amount of insulating material. Therefore, the window area can be expressed as:

$$W_a = l \cdot h = \left(m_1 \cdot d_{c1} + m_2 \cdot d_{c2} + d_{ins1} + d_{f2} + d_{f1}\right) \cdot h \tag{4.1}$$

where m_1 and m_2 are respectively the number of layers of the primary and the secondary windings, d_{c1} and d_{c2} are the diameters of the cables in the primary and the secondary windings, d_{ins1} is the insulation distance between the primary and the secondary windings, d_{f1} is the insulation distance between the primary winding and the core, d_{f2} is the insulation distance between the secondary winding and the core and h is the height of the window.

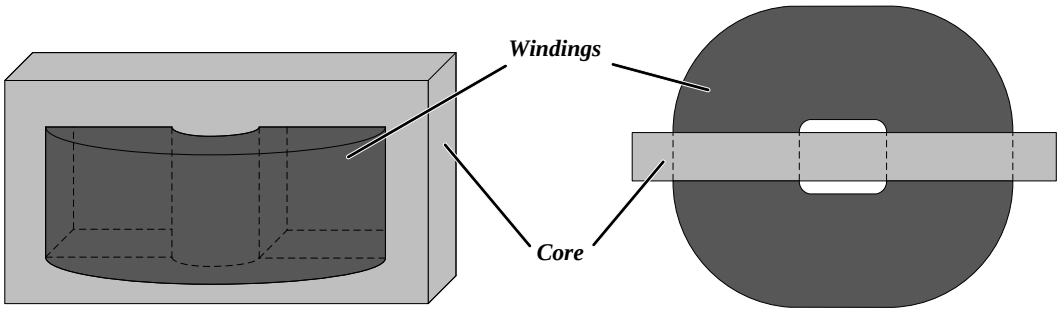
The window height must be large enough to shelter the primary and secondary windings. Since both windings are different, the winding with the larger window height requirement determines the window height (note that the last turn of the ending loop in each winding must be taken into account):

$$h = \max\left(h_{x,\min}\right) \tag{4.2}$$

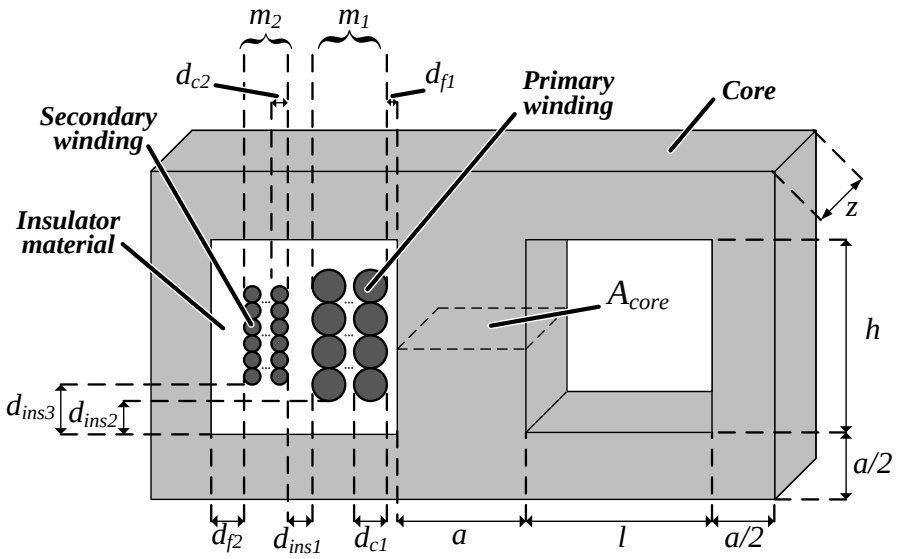
$$h_{1,\min} = \left(\frac{n_1}{m_1} + 1 \right) \cdot d_{c1} + 2 \cdot d_{f1} \tag{4.3}$$

$$h_{2,\min} = \left(\frac{n_2}{m_2} + 1 \right) \cdot d_{c1} + 2 \cdot d_{f2} \tag{4.4}$$

where $h_{1,\min}$ is the minimum height of the primary winding, $h_{2,\min}$ is the minimum height of the secondary winding and n_1 and n_2 are respectively the primary and the secondary turn numbers.



a)



b)

Fig 4.2. a)Typical shell-type transformer's frontal and upper views. b) Detailed illustration of the considered shell-type transformer.

Vertical isolation distances d_{ins2} and d_{ins3} are given by the winding that determines the maximum height. Therefore, if the maximum height is determined by the primary winding ($h_{1,\min}$), d_{ins2} and d_{ins3} will be respectively expressed as in Eq. (4.5) and Eq. (4.6). Whereas, if the maximum height is determined by the secondary winding ($h_{2,\min}$), d_{ins2} and d_{ins3} will be respectively expressed as in Eq. (4.7) and Eq. (4.8).

$$d_{ins2} = d_{f1} \tag{4.5}$$

$$d_{ins3} = d_{f2} + \frac{\left(h_{1,\min} - h_{2,\min}\right)}{2} \tag{4.6}$$

$$d_{ins2} = d_{f1} + \frac{\left(h_{2,\min} - h_{1,\min}\right)}{2} \tag{4.7}$$

$$d_{ins3} = d_{f2} \tag{4.8}$$

The isolation distances inside the window depend on the required isolation level (voltages in the primary and the secondary sides) and the used insulation material. Dry-type soft potted insulators as EPOXY or Micares are attractive insulator materials due to their flexible mechanical characteristics and their high dielectric strengths, 16 kV/mm and 8-24 kV/mm respectively [38]. Thus, isolation distances can be expressed as follows:

$$d_{f1} = \frac{V_{pri}}{\nu \cdot E_{ins}} \tag{4.9}$$

$$d_{f2} = \frac{V_{se}}{\nu \cdot E_{ins}} \tag{4.10}$$

$$d_{ins2} = \frac{\left(V_{se} - V_{pri}\right)}{\nu \cdot E_{ins}} \tag{4.11}$$

where V_{pri} and V_{se} are the voltages in the primary and the secondary windings respectively, E_{ins} is the dielectric strength of the used insulator material and ν is the safety margin considered for the isolation distances.

For given technical specifications, the core cross sectional area (A_{core}) depends on the maximum saturation flux (B_{sat}) of the selected core material:

$$A_{core} = \frac{V_{pri,avg} \cdot \Delta T}{2 \cdot n_1 \cdot (1-\xi) \cdot B_{sat}} \tag{4.12}$$

where $V_{pri,avg}$ is the average voltage applied to the primary side winding in a ΔT time period and ξ is the safety margin considered for the saturation flux (typically 0.1-0.2 [38]).

The width of the central leg of the core (a) depends on the depth of the core itself (z):

$$a = \frac{A_{core}}{z} \tag{4.13}$$

Considering that the transformer is made up by four C-shaped cores, it can be said that the width of the central leg is two times that of the lateral legs as it has been illustrated in Fig 4.2b. Thus, the core volume of the discussed shell-type MFT can be expressed as:

$$V_{core} = A_{core} \cdot (2 \cdot a + 2 \cdot l + h) \tag{4.14}$$

3.2.2 Windings

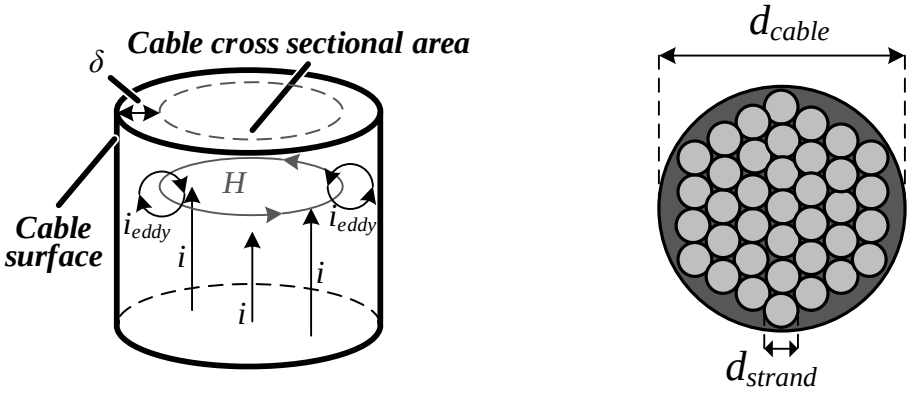
In the design process the medium frequency transformer, the skin and proximity effects must be taken into account. The skin effect is a non-uniform current distribution through

the cable caused by the magnetic field created by the AC current circulating in the cable. This magnetic field induces opposite currents, known as eddy currents, that increase the current density in the outer surface area and reduce it in the inner area (cf. Fig 4.3a). The penetration of these currents is known as the skin depth:

$$\delta = \sqrt{\frac{1}{\pi \cdot f \cdot \mu \cdot \sigma}} \tag{4.15}$$

where f is the frequency of the current, μ is the permeability of the material ($\approx 1.256 \cdot 10^{-6}$ turns/A^2 for copper) and σ is the conductivity of the material ($\approx 5.688 \cdot 10^7$ S/m for copper).

Similarly, the proximity effect is a non-uniform current distribution through the cable caused by the magnetic field created by the AC current circulating in the adjacent cables. The use of stranded, insulated and twisted cables reduces the influence of the skin and proximity effects. The reduced surface area of each strand reduces the skin effect (the skin depth is equal or smaller than the cable radius) while the proximity effect is reduced twisting the strands [35]. The twisted and stranded conductors are known as Litz-cables (cf. Fig 4.3b). Consequently, these cables are usually preferred for MFT applications [36].



a) b)

Fig 4.3. a) Graphical representation of the skin effect. b) Cross sectional illustration of a Litz-cable.

In [33] a procedure to calculate the optimal strand diameter is presented, however, manufacturers tend to provide standard strand diameters (d_{strand}) for certain operation frequencies [39]. For this reason, the strand diameters considered in this book are the ones provided by the manufacturers. The number of strands required by the cable depends on the assumed current density and the copper area required by the current circulating through the cable. For naturally cooled transformers, the maximum allowable current density in the cables (J) is about 1.7-2 A/mm^2 [33]. Hence, for a specific *rms* current circulating through the cable (I_{rms}), the required copper area is given by:

$$A_{ideal} = \frac{I_{rms}}{J} \tag{4.16}$$

From a given copper area, the number of strands can be derived from:

$$n_s = \frac{A_{ideal} \cdot 4}{d_{strand}{}^2 \cdot \pi} \tag{4.17}$$

The diameter of the Litz-cable (d_{cable}) is determined by the number of strands and the thickness of the insulator material. As a first approach, it can be assumed that the insulator material is distributed in the outer side of the cable as illustrated in Fig 4.4.

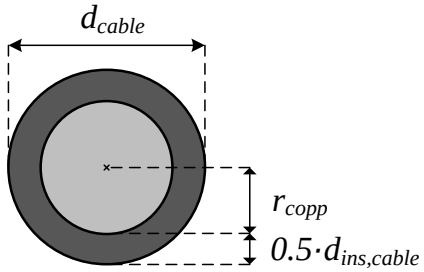
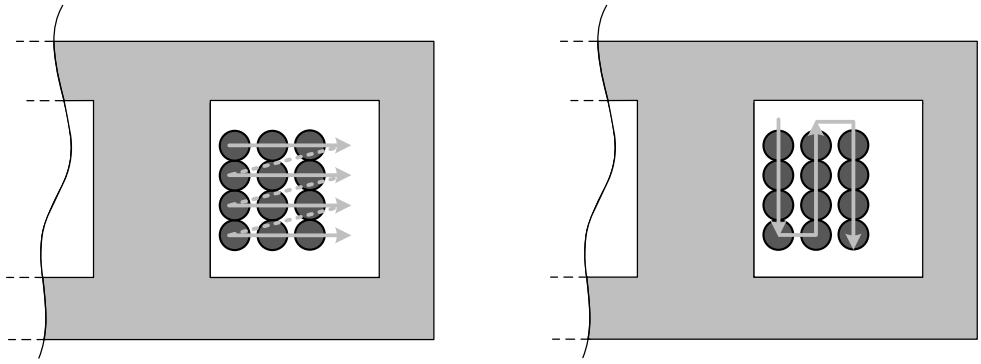


Fig 4.4. Simplified approach of the required copper and insulator in a Litz-cable.

The thickness of the insulator material depends on its dielectric strength and the winding process, which determines the voltage isolation requirements.



a) b)

Fig 4.5. Graphical representation of different coil winding processes where the direction of the winding process is pointed by the arrow. a) The horizontal layers are coiled first. b) The vertical layers are coiled first.

If the winding process is the one illustrated in Fig 4.5a (where the layers are coiled first), the required insulation thickness can be estimated by Eq. (4.18). This winding process leads to a good distribution of the parasitic capacitances between the cables and is a good solution if few layers are required. Conversely, if the winding process is the one illustrated in Fig 4.5b, the required insulation thickness can be estimated by Eq. (4.19). This winding process is a good solution if high number of layers are required. However, this second solution leads to a non-uniform parasitic capacitances distribution.

$$d_{ins,cable} = \frac{V_x}{\nu \cdot E_{ins,cable}} \cdot \frac{m_x}{2 \cdot n_x} \tag{4.18}$$

$$d_{ins,cable} = \frac{V_x}{\nu \cdot E_{ins,cable} \cdot m_x} \tag{4.19}$$

where V_x is the voltage applied to the winding, n_x and m_x are respectively the number of turns and the number of layers, $E_{ins,cable}$ is the dielectric strength of the selected insulator material and v is the safety margin considered for the isolation distances. A commonly used insulator material in Litz-cables is nylon [39], whose dielectric strength is about 14kV/mm.

Therefore, the cable diameter can be approached as:

$$d_{cable} = 2 \cdot r_{copp} + d_{ins,cable} \tag{4.20}$$

r_{copp} is the equivalent copper radius given by Eq. (4.21), where the distances between each strand as well as the thickness of the isolator material of each strand have been neglected.

$$r_{copp} = \frac{d_{strand}}{2} \cdot \sqrt{n_s} \tag{4.21}$$

Once the cable diameter is known, the packing factor (i.e. the relation between the area of the cable and the area of each strand) of the cables is calculated with:

$$pf = n_s \cdot \left(\frac{d_{strand}}{d_{cable}} \right)^2 \tag{4.22}$$

On the other hand, the volume required by the windings can be calculated from Fig 4.2, which gives:

$$V_w = l \cdot h \cdot \left[2 \cdot (a + z) + l \cdot \pi \right] \tag{4.23}$$

3.2.3 Magnetizing and leakage inductances

Transformers can be ideally represented by a magnetizing inductance (L_m), the leakage inductance of each winding ($L_{\sigma 1}$ and $L_{\sigma 2}$) and their equivalent series resistances (cf. Fig 4.6). Since the leakage and the magnetizing inductances affect the behaviour of the converters analysed in section 3.3, these parameters must be carefully designed.

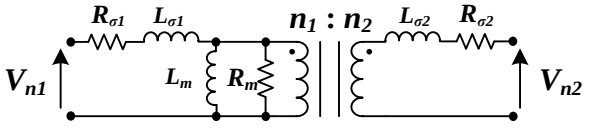


Fig 4.6. Equivalent circuit of a transformer.

3.2.3.1 Magnetizing inductance

The magnetizing inductance of the transformer can be estimated in a relatively easy way through the equivalent magnetic circuit of the transformer. The magnetic circuit of the shell-type transformer can be drawn as in Fig 4.7a under the assumption of uniform magnetic flux distribution in the core and considering the leakage flux is negligible comparing to the magnetizing flux.

a) b)

Fig 4.7. a) Equivalent magnetic circuit of the shell-type transformer. b) Equivalent magnetic circuit of the shell-type transformer with an air gap.

From Ampere's law, the magnetomotive force (F) in Fig 4.7a can be defined as:

$$F = \oint \vec{H} \cdot d\vec{l} = \sum \vec{H} \cdot l = N \cdot i = n_1 \cdot i = \phi \cdot R_{core} \tag{4.24}$$

where ϕ is the magnetic flux through the core, n_1 represents the number of turns in the primary winding and R_{core} is the core reluctance, which depend on the core cross sectional area (A_{core}) and its length (l_{core}):

$$R_{core} = \frac{l_{core}}{A_{core} \cdot \mu_{r,core} \cdot \mu_0} \tag{4.25}$$

where $\mu_{r,core}$ is the relative permeability of the core material (generally between 10^4 and 10^5 for nanocrystalline materials [40]) and μ_0 is the vacuum permeability ($4\pi \cdot 10^{-7}$ turns/A^2).

Hence, the magnetizing inductance can be expressed as:

$$L_m = \frac{N^2}{R} = \frac{{n_1}^2}{R_{core}} = \frac{{n_1}^2 \cdot A_{core} \cdot \mu_{r,core} \cdot \mu_0}{l_{core}} = \frac{{n_1}^2 \cdot A_{core} \cdot \mu_{r,core} \cdot \mu_0}{2 \cdot (l + h + a)} \tag{4.26}$$

If an air gap is introduced in the core (Fig 4.7b), the magnetizing inductance becomes very dependent on the air gap length (l_{gap}). Thus, the desired magnetizing value can be accomplished with a good accuracy:

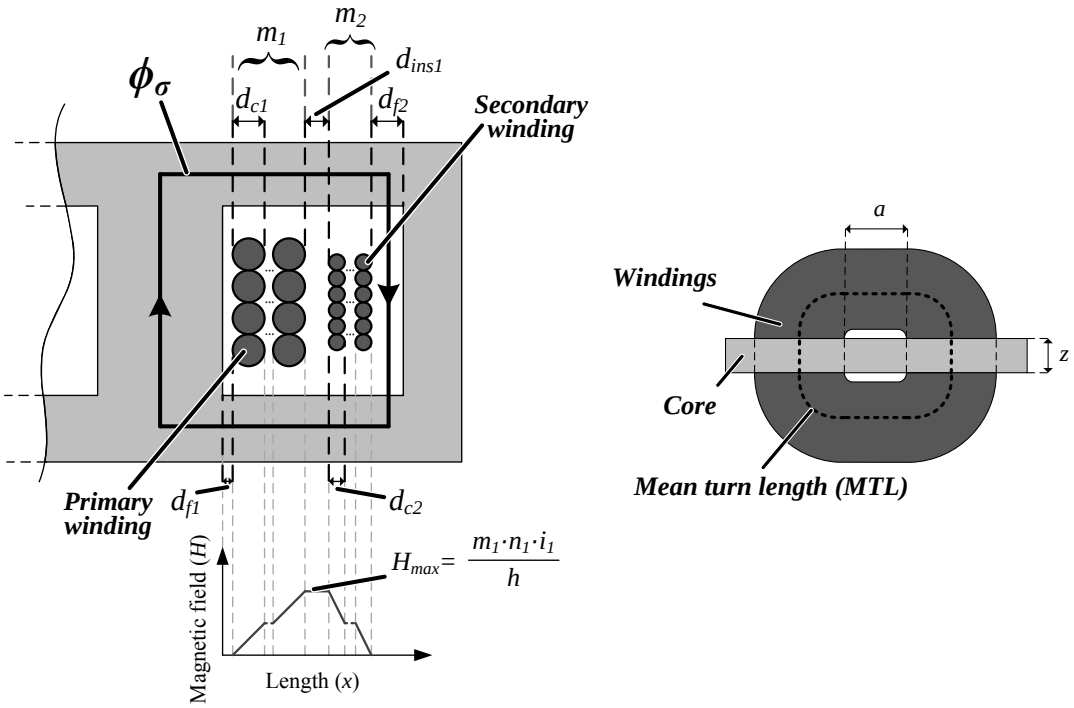
$$L_m = \frac{N^2}{R} = \frac{{n_1}^2}{R_{core}} = \frac{{n_1}^2 \cdot A_{core} \cdot \mu_0}{l_{gap} + \frac{l_{core}}{\mu_{r,core}}} = \frac{{n_1}^2 \cdot A_{core} \cdot \mu_0}{l_{gap} + \frac{2 \cdot (l + h + a) - l_{gap}}{\mu_{r,core}}} \tag{4.27}$$

3.2.3.2 Leakage inductance

The flux that leaks from the core and returns through the air is represented by the leakage inductance. Neglecting the skin and proximity effects and assuming a constant current density in the windings, this phenomena can be represented as in Fig 4.8a. As it can be noticed, the magnetic field in the core window increases linearly until the maximum value is achieved in the region between the primary and the secondary windings. Then, the magnetic field decreases linearly until the field value reaches to zero (after the last layer of the secondary winding). From this magnetic field distribution, the energy stored in the core window and in consequence, in the leakage inductance, can be estimated through Eq. (4.28).

$$
\begin{aligned}
W_\sigma &= \frac{1}{2}\cdot\int_V H\cdot B\ dV = \frac{\mu_0}{2}\cdot\int_V H^2 dV = \frac{\mu_0}{2}\cdot\int_0^l H^2\cdot(MTL\cdot h)\ dx = \\
&= \frac{\mu_0}{2}\cdot(MTL\cdot h)\cdot\left[\int_0^{m_1\cdot d_{c1}}\left(\frac{n_1\cdot i_1\cdot x}{h\cdot m_1\cdot d_{c1}}\right)^2 dx + \int_{m_1\cdot d_{c1}}^{m_1\cdot d_{c1}+d_{ins1}}\left(\frac{m_1\cdot n_1\cdot i_1}{h}\right)^2 dx + \right. \\
&\left. + \int_{m_1\cdot d_{c1}+d_{ins1}}^{m_1\cdot d_{c1}+d_{ins1}+m_2\cdot d_{c2}}\left(\frac{m_1\cdot n_1\cdot i_1}{h}\right)^2\cdot\left(\frac{m_1\cdot d_{c1}+d_{ins1}-x}{m_2\cdot d_{c2}}+1\right)^2 dx\right] = \\
&= \frac{\mu_0\cdot(n_1\cdot i_1)^2\cdot MTL}{2\cdot h}\cdot\left(\frac{m_1\cdot d_{c1}}{3}+d_{ins1}+\frac{m_2\cdot d_{c2}}{3}\right)
\end{aligned}
\tag{4.28}
$$

where h is the height of the window and MTL is the mean turn length of the windings illustrated in Fig 4.8b.



a) b)

Fig 4.8. Schematics for the leakage inductance calculation. a) Magnetic field distribution and leakage flux representation. b) Representation of the mean turn length of the windings.

The value of the MTL can be easily calculated from Fig 4.8 as follows:

$$MTL = 2\cdot(a+z)+\pi\cdot(l-d_{f2}+d_{f1}) \tag{4.29}$$

Furthermore, the energy stored by the leakage inductance can also be expressed as follows:

$$W_\sigma = \frac{1}{2}\cdot L_\sigma\cdot i_1^{\,2} \tag{4.30}$$

Thus, introducing Eq. (4.28) into Eq. (4.30), the leakage inductance of the transformer referenced on the primary is approached by:

$$L_\sigma = \frac{\mu_0 \cdot {n_1}^2 \cdot MTL}{h} \cdot \left(\frac{m_1 \cdot d_{c1}}{3} + d_{ins1} + \frac{m_2 \cdot d_{c2}}{3} \right) \tag{4.31}$$

As it can be observed, the value of the leakage inductance highly depends on the number of turns, the number of layers in the windings and the insulation distance. Nonetheless, the value of the leakage inductance can be reduced by increasing the height of the core window.

It must be highlighted that if the primary and secondary windings are interleaved, the maximum magnetic field in the window is reduced, thereby considerably reducing the value of the leakage inductance [33], Eq. (4.32). However, this increases the difficulty of the transformer construction and makes more complex the estimation of the winding power losses.

$$L_{\sigma,\text{int}} = \left(\frac{n_1}{p} \right)^2 \cdot \frac{\mu_0 \cdot MTL}{h} \cdot \left(\frac{m_1 \cdot d_{c1}}{3} + p \cdot d_{ins1} + \frac{m_2 \cdot d_{c2}}{3} \right) \tag{4.32}$$

where p represents the number of times that the windings are interleaved.

3.3 Power losses estimation

The power losses of a transformer are divided into core power losses and winding power losses.

3.3.1 Core power losses

Generally, core power losses are calculated using the Steinmetz equation, which gives the volumetric power losses for a given material (w/dm^3). This equation, Eq. (4.33), is an improved version of the empirical equation proposed in 1892 by C.P. Steinmetz.

$$P_v = K \cdot f^{\alpha} \cdot {B_{\max}}^{\beta} \tag{4.33}$$

where K and α represents the dependency of the losses in a given material, $B_{\max}$ is the peak flux density value and β is the maximum flux density. Generally, K, α and β parameters are known as the Steinmetz parameters.

Although this expression provides good results for sinusoidal excitations, it is not valid for the typical non-sinusoidal waveforms in DC-DC converters [34]. In order to address this issue, different empirical expression have been introduced so far [33]. Among them, the improved generalized Steinmetz equation (IGSE) introduced in [41] is generally accepted as the estimation method that most accurate results provides [34] and the method that better copes with a variety of excitation waveforms [42]. Furthermore, IGSE

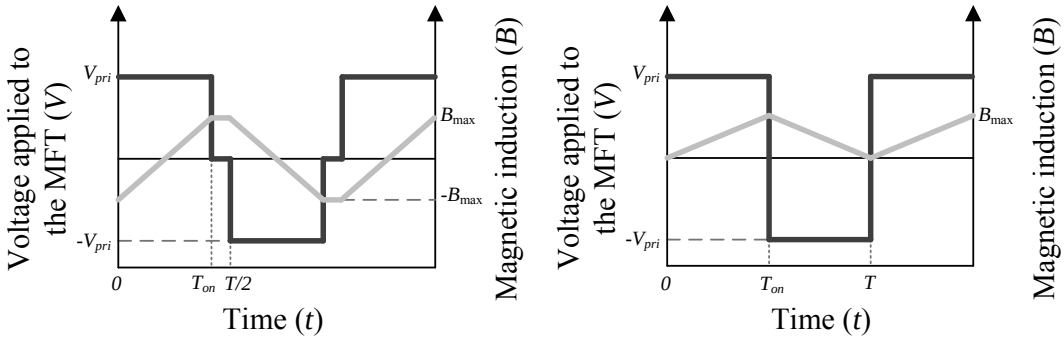
results in Steinmetz equation for sinusoidal excitation waveforms [33, 43]. The IGSE is expressed as follows:

$$P_v = \frac{1}{T}\cdot\int_0^T k_i \cdot \left|\frac{dB(t)}{dt}\right|^{\alpha} \cdot (\Delta B)^{\beta-\alpha}\, dt \tag{4.34}$$

$$k_i = \frac{K}{(2\cdot\pi)^{\alpha-1}\int_0^{2\cdot\pi} |\cos\theta|^{\alpha}\cdot 2^{\beta-\alpha}\, d\theta} \tag{4.35}$$

where K, α and β are the Steinmetz parameters, ΔB is the peak to peak flux density value and θ is the phase angle of the sinusoidal waveform.

As discussed in Eq. (4.12), the magnetic induction is proportional to the voltage applied to the transformer. DC-DC converters apply square wave voltages in the MFTs (see Chapter 3) and in consequence, the magnetic inductions in the MFTs required by different DC-DC converters can be depicted as in Fig 4.9.



a) b)

Fig 4.9. Typical voltage and magnetic induction waveforms in a) bidirectionally magnetized MFTs and b) unidirectionally magnetized MFTs.

From these waveforms, piecewise linear (PWL) models of the magnetic induction can be calculated [42]. Thus, in order to provide an easy to use equation, the expression in Eq. (4.34) can be simplified. For bidirectionally magnetized transformers (cf. Fig 4.9a), the PWL model of the magnetic induction is given by:

$$B(t) = B_{\max}\cdot\begin{cases} \dfrac{2\cdot t - T_{on}}{T_{on}} & 0 < t < T_{on} \\ 1 & T_{on} < t < \dfrac{T}{2} \\ \dfrac{T_{on} + T - 2\cdot t}{T_{on}} & \dfrac{T}{2} < t < \left(\dfrac{T}{2} + T_{on}\right) \\ -1 & \left(\dfrac{T}{2} + T_{on}\right) < t < T \end{cases} \tag{4.36}$$

where T is the period of the square wave voltage applied to the MFT, T_{on} is the time interval at which the DC bus voltage (V_{in}) is applied to the primary winding and $B_{\max}$ is the maximum magnetic induction in the core given by Eq. (4.37).

$$B_{\max} = \frac{V_{in} \cdot T_{on}}{2 \cdot n_1 \cdot A_{core}} \tag{4.37}$$

where A_{core} is the cross sectional area of the core and n_1 represents the number of turns of the primary winding.

Introducing the PWL model of Eq. (4.36) into Eq. (4.34), a straightforward expression for the calculation of the core power losses in bidirectionally magnetized transformers is obtained:

$$P_v = 2^{\beta+1} \cdot k_i \cdot f^{\alpha} \cdot {B_{\max}}^{\beta} \cdot \delta^{1-\alpha} \tag{4.38}$$

where δ is the duty cycle of the converter (T_{on}/T).

Furthermore, according to [41], the calculation of k_i can be simplified as follows when PWL models are used:

$$k_i = \frac{K}{2^{\beta+1} \cdot \pi^{\alpha-1} \cdot \left(0.2761 + \frac{1.7061}{\alpha + 1.354}\right)} \tag{4.39}$$

On the other hand, for unidirectionally magnetized transformers (cf. Fig 4.9b), the PWL model of the magnetic induction is given by:

$$B(t) = B_{\max} \cdot \begin{cases} \dfrac{t}{T_{on}} & 0 < t < T_{on} \\ \dfrac{T - t}{T - T_{on}} & T_{on} < t < T \end{cases} \tag{4.40}$$

Introducing this PWL model into Eq. (4.34), core power losses in unidirectionally magnetized transformers are provided by:

$$P_v = k_i \cdot f^{\alpha} \cdot {B_{\max}}^{\beta} \cdot \left(\delta^{1-\alpha} + (1-\delta)^{1-\alpha}\right) \tag{4.41}$$

where δ is the duty cycle of the converter (T_{on}/T).

All in all, the total power losses in the core are obtained by means of:

$$P_{core} = P_v \cdot V_{core} \tag{4.42}$$

where V_{core} is the total core volume.

3.3.2 Winding power losses

The power losses in a conductor where a DC current is flowing can be expressed as:

$$P_{DC} = I^2 \cdot R_{DC} \tag{4.43}$$

where R_{DC} is the DC resistance of the conductor and I is the value of the current through the conductor.

Analogously, it can be said that the power losses in a conductor with a purely sinusoidal AC current flowing through it are given by:

$$P_{AC} = \left(\frac{I}{\sqrt{2}}\right)^2 \cdot R \tag{4.44}$$

where I is the maximum amplitude of the current and R is the resistance of the conductor.

In medium frequency applications, the skin and proximity effects are considerable (see section 4.2.2). Thus, these effects must be taken into account when calculating the resistance of the conductors. The expression modelling the resistance of the foil conductors in transformer windings was introduced by P.L Dowell in [44]:

$$R = R_{DC} \cdot F_r \tag{4.45}$$

where F_r is a resistance factor (known as Dowell's resistance factor) given by:

$$F_r = \Delta \cdot \left[S + \frac{2}{3} \cdot \left(m^2 - 1\right) \cdot P \right] \tag{4.46}$$

$$S = \frac{\sinh\left(2 \cdot \Delta\right) + \sin\left(2 \cdot \Delta\right)}{\cosh\left(2 \cdot \Delta\right) - \cos\left(2 \cdot \Delta\right)} \tag{4.47}$$

$$P = \frac{\sinh\left(\Delta\right) - \sin\left(\Delta\right)}{\cosh\left(\Delta\right) + \cos\left(\Delta\right)} \tag{4.48}$$

$$\Delta = \frac{d_{cable}}{\delta} \cdot \frac{\sqrt{\eta_w \cdot \pi}}{2} \tag{4.49}$$

where S and P are the expressions that gives the skin and proximity effects respectively, m is the number of layers of the winding, d_{cable} is the diameter of the conductor, δ is the skin depth (see Eq. (4.15)) and η_w is the porosity factor, which relates the round or rectangular conductors with their equivalent whole window foil conductors.

For the round Litz-cables considered in this book, Dowell's resistance factor can be rewritten as follows [33]:

$$F_r = 1 + \frac{\gamma^4}{192} \cdot \left[\frac{1}{6} + \frac{pf \cdot n_s \cdot \pi^2}{4} \cdot \left(16 \cdot m^2 - 1 + \frac{24}{\pi^2} \right) \right] \tag{4.50}$$

$$\gamma = \frac{d_{strand}}{\delta \cdot \sqrt{2}} \tag{4.51}$$

where d_{strand} is the diameter of each Litz strand, n_s represents the number of strands (see Eq. (4.17)) and pf is the packing factor of the Litz-cable (see Eq. (4.22)). As it can be noticed, an increase in the strand diameter as well as in the number of layers leads to higher resistance factors and in consequence, to higher power losses.

On the other hand, the DC resistance of each winding can be estimated by means of:

$$R_{DC} = \frac{4 \cdot n_x \cdot MTL_x}{n_s \cdot \sigma \cdot \pi \cdot {d_{strand}}^2} \tag{4.52}$$

where σ is the conductivity of the material, n_x represents the number of turns of each winding and MTL_x is the mean turn length of each winding. For the shell-type transformer's geometry (cf. Fig 4.2b), the MTLs of the primary and the secondary windings are expressed respectively as:

$$MTL_1 = 2\cdot(a+z)+\pi\cdot(m_1\cdot d_{c1}+2\cdot d_{f1}) \tag{4.53}$$

$$MTL_2 = 2\cdot(a+z)+2\cdot\pi\cdot\left(\frac{m_2\cdot d_{c2}}{2}+m_1\cdot d_{c1}+d_{f1}+d_{ins1}\right) \tag{4.54}$$

The current through the MFTs in the DC-DC converters is generally a non-sinusoidal current. Hence, the current circulating through the windings is composed of several harmonics. As Dowell's resistance factor varies for each current harmonic (the skin depth varies depending on the frequency), the expression of the power losses in Eq. (4.44) must be rewritten in order to take into account the losses due to each current harmonic. Thus, power losses in each winding can be expressed as:

$$P_w = \sum_i \left(\frac{I_i}{\sqrt{2}}\right)^2 \cdot R_{DC}\cdot F_{ri} \tag{4.55}$$

where I_i is the amplitude of each current harmonic and F_{ri} is the resistance factor of each current harmonic.

3.3.3 Thermal behaviour

Core and winding power losses discussed in previous sections generate heat, which leads to an increase of the transformer temperature. In order to keep this temperature within allowable levels, the thermal behaviour of the transformer must be modelled. In [34, 38, 45-47] detailed thermal models are discussed. Whereas in [48], a more simple method is proposed.

Assuming that the transformer is naturally cooled and avoiding the use of heat sinks, complicated nodal models can be avoided (these models usually require detailed heat sink specifications) and in consequence, the approach proposed in [48] is suitable for estimating the thermal performance of the transformer. Considering the thermal energy is dissipated uniformly through the surface area of the transformer, the temperature raise of the transformer is expressed as:

$$\Delta T = \left(\frac{P_{core}+P_{w1}+P_{w2}}{10\cdot S_T}\right)^{0.833} \tag{4.56}$$

where S_T is the total surface area of the transformer, P_{w1} and P_{w2} are respectively the power losses in the primary and the secondary windings and P_{core} are the core power losses.

3.4 Optimization procedure

The optimized design of a MFT is given by the definition of its best dimensions. However, the transformer designs for certain specifications can be infinite. Therefore, optimization procedures must be used in order to find an optimum MFT design. The flowchart of the design optimization procedure presented in this book is shown by Fig 4.10.

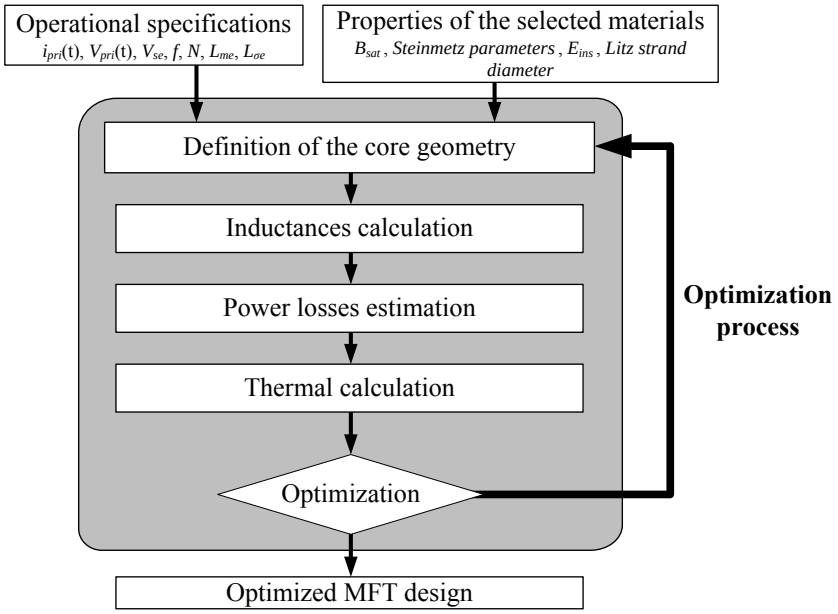


Fig 4.10. Flowchart of the design optimization procedure.

As it can be observed, the procedure has few steps. First, insulator material as well as core and windings materials must be selected and their properties must be introduced in the optimization program. Furthermore, operational specifications must be defined. These specifications, imposed by the application and the converter topology, can be listed as follows: the voltages to be isolated in the primary and the secondary windings, the required transformer turn ratio, the operational frequency, the voltage and current waveforms in the conductors and the expected leakage and magnetizing inductances.

Then, the geometry of the core is defined and the values of the inductances derived from that geometry are calculated (as discussed in section 4.2).

Next, the power losses are estimated and the temperature raise due to these losses is calculated (as discussed in section 4.3).

Finally, the optimal designs are found by means of an iterative process based on the multi objective genetic algorithm provided by MATLAB simulation platform. The use of a genetic algorithm requires to define objectives, optimization variables and constraints. As the desired MFT design is that which fulfils high efficiency and low volume requirements, the cost functions or objectives to optimize by the genetic algorithm are the total power losses of the transformer (P_{loss}) and the total volume of it (V_{tot}):

$$\begin{cases} \min\limits_{x} f_1(x) = \min\limits_{x} \left| P_{loss}(x) \right| \\ \\ \min\limits_{x} f_2(x) = \min\limits_{x} \left| V_{tot}(x) \right| \end{cases} \tag{4.57}$$

To achieve this objectives, optimization variables must be defined. Through the different values given to these variables, different optimal designs will be provided. In this optimization procedure, the optimization variables are the following ones:

- The depth of the core (z).
- The number of turns in the primary winding (n_1).
- The number of layers in the primary winding (m_1).
- The number of layers in the secondary winding (m_2).
- The current density in the windings (J).
- The margin of the maximum magnetic induction in the core (ξ).
- In the cases where small magnetizing inductance values are demanded, an air gap is required in the core. In consequence, the length of the air gap (l_{gap}) is treated as an optimization variable.

Furthermore, so as to penalize the undesired designs, the design constraints have to be defined. Two constraints have been defined in this design procedure. On the one hand, the integration of the magnetic elements within the transformer provides higher power density to the DC-DC converters. Thus, the error between the desired inductances and the inductances derived from the design is treated as a constraint. In switch mode DC-DC converters a high magnetizing inductance is required whereas in resonant mode DC-DC converters an specific magnetizing inductance value is required. Thus, the constraint for the latter is given by Eq. (4.59) while the constraint of the switch mode converters is given by Eq. (4.60). The leakage inductance is treated equally for both type of DC-DC converters, Eq. (4.58).

$$0.95 \cdot L_{\sigma d} < L_{\sigma} < 1.05 \cdot L_{\sigma d} \tag{4.58}$$

$$0.95 \cdot L_{md} < L_{m} < 1.05 \cdot L_{md} \tag{4.59}$$

$$0.95 \cdot L_{md} < L_{m} \tag{4.60}$$

where $L_{\sigma d}$ and L_{md} are respectively the desired leakage and magnetizing inductance values.

On the other hand, the temperature of the transformer must be kept within allowable levels, which makes the maximum surface temperature of the transformer the second design constraint. Following the results of [33], the maximum surface temperature could be limited to 100ºC as a first approach.

The genetic algorithm will output a curve containing the best solutions with minimum power losses and volume. This curve is known as the Pareto front, from which, the designer can select the design that better suits with the requirements of the application with the security of knowing that all the results are optimal.

3.5 Summary

Medium frequency transformers provide galvanic isolation and adapt the voltage levels between the input and the output of DC-DC converters. The design of these medium frequency transformers is challenging due to the frequency at which they operate and the non-sinusoidal current and voltage waveforms applied to them. At high frequencies, the skin and proximity effects in the windings are considerable. Those effects, increase the winding power losses thereby reducing the efficiency of the transformer. In turn, the non-sinusoidal voltages that excite these transformers require the use of more complex core power losses estimation methods than that used for the transformers excited with sinusoidal voltages. Furthermore, the current harmonics of the non-sinusoidal waveforms increase the power losses in the windings.

In order to achieve high power densities, the volume of the transformer must be reduced. To do so, appropriate core materials with high magnetic induction saturation levels must be selected (e.g. nanocrystalline), which reduce the core volume and in consequence, the volume of the transformer. The selection of insulator materials with high dielectric strength also reduces the total volume of the transformer. Moreover, selecting appropriate conductor material as Litz-cables, skin and proximity effects are minimized, thereby diminishing the power losses in the windings and increasing the efficiency of the transformer.

In this chapter, the design of the medium frequency transformers required by the isolated DC-DC converters has been discussed. Among coaxial-type, core-type and shell-type transformers, the latter results the more attractive for the MFTs for high voltage applications. Thus, detailed design equations for naturally cooled shell-type transformers are presented. Furthermore, the calculation of the leakage and magnetizing inductances of the transformer is discussed. It is deduced that an increase in the number of turns, number of layers in the windings and insulation distance leads to high leakage inductances, whereas an increase of the core window height reduces the leakage inductance value. In turn, adding an air gap, the value of the magnetizing inductance is reduced. Moreover, the power losses in the windings increase with a high number of layers. Straightforward and easy to implement piecewise linear models for the estimation of the core power losses in unidirectionally and bidirectionally magnetized transformers have been presented together with a design optimization procedure. This optimization procedure outputs a Pareto front that determines which are the optimum transformer designs for certain operational specifications.

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Appendix A

Validation of switch mode DC-DC converter models

The simulations for validating the models of switch mode DC-DC converters have been carried out through Synopsys/SABER. A constant input DC bus voltage has been considered. Since a resistive load has been assumed, in the converters with an output LC filter, some deviations in the capacitor *rms* currents can be observed. Furthermore, the simulations have been carried out without any output voltage control strategy. Hence, there are small differences between the estimated and simulated stored energy values. Additionally, the lack of an average voltage control applied to the MFT leads to deviations in the stored energy and *rms* currents in the magnetizing inductance.

The converters have been designed with the voltages, rated power and switching frequency summarized in Table B.1.

TABLE B.1
VALIDATION SCENARIO

	Design characteristics
P_{in}	555.555 kW
V_{in}	1833 V
V_{out}	2780 V
f_{sw}	1 kHz

B.1 Boost

TABLE B.2
PASSIVE ELEMENTS

	Boost converter
C_{in}	20.668 µF
L_1	20.601 mH
C_{out}	244.874 µF

TABLE B.3
EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_1	C_{out}
Simulation	Maximum stored energy	34.72 J	1.049 kJ	1.040 kJ
	rms current	8.82 A	304.1 A	144.4 A
	Maximum voltage stress	1833 V	1830 V	2915 V
Analytical estimation	Maximum stored energy	34.72 J	1.043 kJ	1.043 kJ
	rms current	8.74 A	303.2 A	143.6 A
	Maximum voltage stress	1833 V	1833 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**0.57**	**0.28**
	rms current	**0.91**	**0.29**	**0.55**
	Maximum voltage stress	**0**	**0.16**	**0.13**

TABLE B.4

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistor S_1			**Diode D_1**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	103.2 A	104 A	**0.76**	199.8 A	199.9 A	**0.05**
rms current (I_{rms})	176.9 A	177.8 A	**0.50**	246.2 A	246.7 A	**0.20**
Maximum current (i_{max})	318.2 A	319.1 A	**0.28**	318.2 A	319.1 A	**0.28**
Turn-on switched current (i_{on})	287.9 A	288.1 A	**0.06**	-	-	**-**
Turn-off switched current (i_{off})	318.2 A	319.1A	**0.28**	287.9 A	288.2 A	**0.10**
Maximum voltage (v_{max})	2919 V	2918 V	**0.03**	2919 V	2912 V	**0.24**
Turn-on switched voltage (v_{on})	2919 V	2918 V	**0.03**	-	-	**-**
Turn-off switched voltage (v_{off})	2641 V	2635 V	**0.22**	2919 V	2912 V	**0.24**

B.2 Zeta

TABLE B.5

PASSIVE ELEMENTS

	Zeta converter
C_{in}	657.024 µF
L_1	36.446 mH
L_2	55.276 mH
C_1	433.21 µF
C_{out}	6.98 µF

TABLE B.6

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_1	C_1	L_2	C_{out}
Simulation	Maximum stored energy	1.103 kJ	1.841 kJ	1.833 kJ	1.209 kJ	28.9 J
	rms current	246.5 A	302.9 A	245.9 A	199.3 A	3.1 A
	Maximum voltage stress	1833 V	2912 V	2909 V	2881 V	2878 V
Analytical estimation	Maximum stored energy	1.103 kJ	1.845 kJ	1.845 kJ	1.216 kJ	38.28 J
	rms current	246.3 A	303.2 A	246.1 A	199.9 A	5.76 A
	Maximum voltage stress	1833 V	2919 V	2919 V	2919 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**0.21**	**0.65**	**0.57**	**24.50**
	rms current	**0.08**	**0.09**	**0.08**	**0.30**	**46.18**
	Maximum voltage stress	**0**	**0.23**	**0.34**	**1.30**	**1.40**

TABLE B.7

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistor S_1			**Diode D_1**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	303 A	300.5 A	**0.83**	199.8 A	201.6 A	**0.89**
rms current (I_{rms})	390.5 A	388.6 A	**0.48**	317.1 A	318.2 A	**0.34**
Maximum current (i_{max})	528 A	527 A	**0.18**	528 A	527 A	**0.18**
Turn-on switched current (i_{on})	477.7 A	476.6 A	**0.23**	-	-	**-**
Turn-off switched current (i_{off})	528 A	527 A	**0.18**	477.7 A	476.6 A	**0.23**
Maximum voltage (v_{max})	4752 V	4745 V	**0.14**	4752 V	4738 V	**0.29**
Turn-on switched voltage (v_{on})	4752 V	4745 V	**0.14**	-	-	**-**
Turn-off switched voltage (v_{off})	4474 V	4465 V	**0.20**	4752 V	4738 V	**0.29**

B.3 Sepic

TABLE B.8
PASSIVE ELEMENTS

	Sepic converter
C_{in}	20.668 µF
L_1	36.446 mH
L_2	55.276 mH
C_1	657.024 µF
C_{out}	433.21 µF

TABLE B.9
EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_1	C_1	L_2	C_{out}
Simulation	Maximum stored energy	34.72 J	1.923 kJ	1.328 kJ	1.174 kJ	1.828 kJ
	rms current	8.93 A	307.9 A	245.3 A	193 A	245.2 A
	Maximum voltage stress	1833 V	3086 V	2011 V	2908 V	2905 V
Analytical estimation	Maximum stored energy	34.72 J	1.845 kJ	1.216 kJ	1.216 kJ	1.845 kJ
	rms current	8.74 A	303.2 A	246.1 A	199.9 A	246.1 A
	Maximum voltage stress	1833 V	3010 V	1924 V	2919 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**4.23**	**9.21**	**3.45**	**0.92**
	rms current	**2.17**	**1.55**	**0.33**	**3.45**	**0.37**
	Maximum voltage stress	**0**	**2.52**	**4.52**	**0.38**	**0.48**

TABLE B.10

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistor S_1			**Diode D_1**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	303 A	301.8 A	**0.40**	199.8 A	198.9 A	**0.45**
rms current (I_{rms})	390.5 A	388.8 A	**0.44**	317.1 A	315.8 A	**0.41**
Maximum current (i_{max})	528 A	526.2 A	**0.34**	528 A	526.1 A	**0.36**
Turn-on switched current (i_{on})	477.7 A	475.4 A	**0.48**	-	-	**-**
Turn-off switched current (i_{off})	528 A	526.2 A	**0.34**	477.7 A	475.8 A	**0.40**
Maximum voltage (v_{max})	4843 V	4919 V	**1.55**	4843 V	4912 V	**1.40**
Turn-on switched voltage (v_{on})	4843 V	4919 V	**1.55**	-	-	**-**
Turn-off switched voltage (v_{off})	4382 V	4370 V	**0.27**	4843 V	4912 V	**1.40**

B.4 Isolated-sepic

TABLE B.11

PASSIVE ELEMENTS

	Isolated-sepic converter
C_{in}	20.668 µF
L_1	30.239 mH
L_m	30.239 mH
C_1	826.746 µF
C_{out}	359.424 µF
n_2 / n_1	1.5166

TABLE B.12

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_1	C_1	L_m	C_{out}
Simulation	Maximum stored energy	34.72 J	1.638 kJ	1.683 kJ	1.630 kJ	1.522 kJ
	rms current	11.48 A	303 A	303.1 A	302.8 A	199.7 A
	Maximum voltage stress	1833 V	2105 V	2017 V	1921 V	2910 V
Analytical estimation	Maximum stored energy	34.72 J	1.531 kJ	1.531 kJ	1.531 kJ	1.531 kJ
	rms current	8.74 A	303.2 A	303 A	303.2 A	199.8 A
	Maximum voltage stress	1833 V	1924 V	1924 V	1924 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**6.99**	**9.93**	**6.47**	**0.59**
	rms current	**31.35**	**0.07**	**0.03**	**0.13**	**0.05**
	Maximum voltage stress	**0**	**9.41**	**4.83**	**0.16**	**0.31**

TABLE B.13

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistor S_1			**Diode D_1**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	303 A	303.1 A	**0.03**	199.8 A	199.3 A	**0.25**
rms current (I_{rms})	428.8 A	428.5 A	**0.07**	282.7 A	282.3 A	**0.14**
Maximum current (i_{max})	636.4 A	636.3 A	**0.02**	419.6 A	419.5 A	**0.02**
Turn-on switched current (i_{on})	575.8 A	574.3 A	**0.26**	-	-	**-**
Turn-off switched current (i_{off})	636.4 A	636.3 A	**0.02**	369.3 A	378.7 A	**2.48**
Maximum voltage (v_{max})	3849 V	3938 V	**2.26**	5838 V	5963 V	**2.10**
Turn-on switched voltage (v_{on})	3849 V	3938 V	**2.26**	-	-	**-**
Turn-off switched voltage (v_{off})	3482 V	3535 V	**1.50**	5838 V	5963 V	**2.10**

B.5 Ćuk

TABLE B.14
PASSIVE ELEMENTS

	Ćuk converter
C_{in}	20.668 µF
L_1	36.446 mH
L_2	55.276 mH
C_1	261.072 µF
C_{out}	8.985 µF

TABLE B.15
EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_1	C_1	L_2	C_{out}
Simulation	Maximum stored energy	34.72 J	1.841 kJ	3.050 kJ	1.209 kJ	36.98 J
	rms current	8.73 A	303 A	246 A	199.3 A	3.68 A
	Maximum voltage stress	1833 V	3004 V	4833 V	2872 V	2869 V
Analytical estimation	Maximum stored energy	34.72 J	1.845 kJ	3.062 kJ	1.216 kJ	38.28 J
	rms current	8.74 A	303.2 A	246.1 A	199.9 A	5.76 A
	Maximum voltage stress	1833 V	3010 V	4843 V	2919 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**0.22**	**0.39**	**0.58**	**3.40**
	rms current	**0.11**	**0.07**	**0.04**	**0.30**	**36.11**
	Maximum voltage stress	**0**	**0.20**	**0.21**	**1.61**	**1.71**

TABLE B.16

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistor S_1			**Diode D_1**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	303 A	302.8 A	**0.07**	199.8 A	199.3 A	**0.25**
rms current (I_{rms})	390.5 A	390.1 A	**0.10**	317.1 A	316.4 A	**0.22**
Maximum current (i_{max})	528 A	526.9 A	**0.21**	528 A	526.9 A	**0.21**
Turn-on switched current (i_{on})	477.7 A	476.9 A	**0.17**	-	-	**-**
Turn-off switched current (i_{off})	528 A	526.9 A	**0.21**	477.7 A	476.6 A	**0.23**
Maximum voltage (v_{max})	4843 V	4837 V	**0.12**	4843 V	4829 V	**0.29**
Turn-on switched voltage (v_{on})	4843 V	4837 V	**0.12**	-	-	**-**
Turn-off switched voltage (v_{off})	4382 V	4374 V	**0.18**	4843 V	4829 V	**0.29**

B.6 Isolated-ćuk

TABLE B.17

PASSIVE ELEMENTS

	Isolated-ćuk converter
C_{in}	20.668 µF
L_1	30.239 mH
L_m	30.239 mH
C_1	826.746 µF
L_2	69.555 mH
C_2	359.424 µF
C_{out}	8.985 µF
n_2 / n_1	1.5166

TABLE B.18

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_1	C_1	L_m	C_2	L_2	C_{out}
Simulation	Maximum stored energy	34.72 J	1.540 kJ	1.627 kJ	13.35 J	1.625 kJ	1.529 kJ	37.06 J
	rms current	8.74 A	304.3 A	303.9 A	13.6 A	200.3 A	199.8 A	3.64 A
	Maximum voltage stress	1833 V	2016 V	1984 V	1979 V	3007 V	2875 V	2872 V
Analytical estimation	Maximum stored energy	34.72 J	1.531 kJ	1.531 kJ	3.47 J	1.531 kJ	1.531 kJ	38.28 J
	rms current	8.74 A	303.2 A	303 A	8.74 A	199.8 A	199.9 A	5.76 A
	Maximum voltage stress	1833 V	2016 V	1924 V	1924 V	2919 V	2919 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**0.59**	**6.27**	**284.73**	**6.14**	**0.13**	**3.19**
	rms current	**0**	**0.36**	**0.30**	**55.61**	**0.25**	**0.05**	**36.81**
	Maximum voltage stress	**0**	**0**	**3.12**	**2.86**	**3.01**	**1.51**	**1.61**

TABLE B.19

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistor S_1			**Diode D_1**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	303 A	303.1 A	**0.03**	199.8 A	201.5 A	**0.84**
rms current (I_{rms})	429 A	428.7 A	**0.07**	282.8 A	284 A	**0.42**
Maximum current (i_{max})	651.6 A	666.1 A	**2.18**	429.6 A	439.2 A	**2.19**
Turn-on switched current (i_{on})	560.7 A	569.9 A	**1.61**	-	-	-
Turn-off switched current (i_{off})	651.6 A	666.1 A	**2.18**	369.7 A	378.9 A	**2.43**
Maximum voltage (v_{max})	3849 V	3849 V	**0**	5838 V	5828 V	**0.17**
Turn-on switched voltage (v_{on})	3849 V	3849 V	**0**	-	-	-
Turn-off switched voltage (v_{off})	3482 V	3475 V	**0.20**	5838 V	5828V	**0.17**

B.7 Flyback

TABLE B.20
PASSIVE ELEMENTS

	Flyback converter
C_{in}	826.746 µF
L_m	15.119 mH
C_{out}	359.424 µF
n_2 / n_1	1.5166

TABLE B.21
EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_m	C_{out}
Simulation	Maximum stored energy	1.388 kJ	3.055 kJ	1.522 kJ
	rms current	302.9 A	605.9 A	199.8 A
	Maximum voltage stress	1833 V	1921 V	2910 V
Analytical estimation	Maximum stored energy	1.388 kJ	3.062 kJ	1.531 kJ
	rms current	303.3 A	606.4 A	199.8 A
	Maximum voltage stress	1833 V	1924 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**0.23**	**0.59**
	rms current	**0.13**	**0.08**	**0**
	Maximum voltage stress	**0**	**0.16**	**0.31**

TABLE B.22

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistor S_1			**Diode D_1**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	303 A	303.2 A	**0.07**	199.8 A	199.4 A	**0.20**
rms current (I_{rms})	428.8 A	428.6 A	**0.05**	282.7 A	282.3 A	**0.14**
Maximum current (i_{max})	636.4 A	635.7 A	**0.11**	419.6 A	419.1 A	**0.12**
Turn-on switched current (i_{on})	575.8 A	575.1 A	**0.12**	-	-	**-**
Turn-off switched current (i_{off})	636.4 A	635.7 A	**0.11**	379.6 A	379.1 A	**0.13**
Maximum voltage (v_{max})	3757 V	3754 V	**0.08**	5699 V	5683 V	**0.28**
Turn-on switched voltage (v_{on})	3757 V	3754 V	**0.08**	-	-	**-**
Turn-off switched voltage (v_{off})	3574 V	3570 V	**0.11**	5699 V	5683 V	**0.28**

B.8 Forward

TABLE B.23

PASSIVE ELEMENTS

	Forward converter
C_{in}	1.023 mF
L_m	11.895 mH
L_1	77.415 mH
C_{out}	8.985 µF
n_2 / n_1	1.2547
n_3 / n_1	3.4197

TABLE B.24

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_m	L_1	C_{out}
Simulation	Maximum stored energy	1.878 kJ	27.52 J	1.688 kJ	36.65 J
	rms current	369.2 A	39.20 A	198.8 A	3.64 A
	Maximum voltage stress	1833 V	1828 V	3579 V	2856 V
Analytical estimation	Maximum stored energy	1.878 kJ	27.77 J	1.840 kJ	38.28 J
	rms current	374.69 A	39.45 A	199.9 A	5.76 A
	Maximum voltage stress	1833 V	1833 V	3488 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**0.90**	**8.26**	**4.26**
	rms current	**1.47**	**0.63**	**0.55**	**36.81**
	Maximum voltage stress	**0**	**0.27**	**2.61**	**2.16**

TABLE B.25

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE INPUT SIDE SEMICONDUCTORS

	Transistor S_1			**Diode D_1**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	318.2 A	316.2 A	**0.63**	15.15 A	14.99 A	**1.07**
rms current (I_{rms})	478.5 A	475.9 A	**0.55**	23.45 A	23.27 A	**0.77**
Maximum current (i_{max})	785.9 A	782.3 A	**0.46**	54.46 A	54.16 A	**0.55**
Turn-on switched current (i_{on})	649.2 A	645.3 A	**0.60**	-	-	**-**
Turn-off switched current (i_{off})	785.9 A	782.3 A	**0.46**	0 A	0 A	**0**
Maximum voltage (v_{max})	3293 V	3295 V	**0.06**	4133 V	4126 V	**0.17**
Turn-on switched voltage (v_{on})	3293 V	3294 V	**0.03**	-	-	**-**
Turn-off switched voltage (v_{off})	3293 V	3293 V	**0**	4133 V	4126 V	**0.17**

TABLE B.26

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE OUTPUT SIDE SEMICONDUCTORS

	Diode D_2			**Diode D_3**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	88.62 A	88.07 A	**0.62**	111.2 A	110.7 A	**0.45**
rms current (I_{rms})	133.1 A	132.4 A	**0.53**	149.1 A	148.3 A	**0.54**
Maximum current (i_{max})	209.8 A	208.9 A	**0.43**	209.8 A	208.9 A	**0.43**
Turn-off switched current (i_{off})	209.8 A	208.9 A	**0.43**	189.8 A	188.7 A	**0.58**
Maximum voltage (v_{max})	4995 V	4997 V	**0.04**	6268 V	6249 V	**0.30**
Turn-off switched voltage (v_{off})	4995 V	4997 V	**0.04**	6268 V	6249 V	**0.30**

B.9 Two-transistor forward

TABLE B.27

PASSIVE ELEMENTS

	Two-transistor forward converter
C_{in}	925.956 µF
L_m	14.520 mH
L_1	70.946 mH
C_{out}	8.985 µF
n_2 / n_1	3.0951

TABLE B.28

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_m	L_1	C_{out}
Simulation	Maximum stored energy	1.555 kJ	27.56 J	1.549 kJ	36.74 J
	rms current	339.2 A	35.19 A	198.9 A	3.62 A
	Maximum voltage stress	1833 V	1824 V	2969 V	2859 V
Analytical estimation	Maximum stored energy	1.555 kJ	27.77 J	1.561 kJ	38.28 J
	rms current	340.6 A	35.35 A	199.9 A	5.76 A
	Maximum voltage stress	1833 V	1833 V	2893 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**0.76**	**0.77**	**4.02**
	rms current	**0.41**	**0.45**	**0.50**	**37.15**
	Maximum voltage stress	**0**	**0.49**	**2.63**	**2.06**

TABLE B.29

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE INPUT SIDE SEMICONDUCTORS

	Transistor S_1-S_2			**Diode D_1-D_2**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	318.2 A	317.4 A	**0.25**	15.15 A	15 A	**1**
rms current (I_{rms})	455.3 A	453.8 A	**0.33**	24.99 A	24.82 A	**0.68**
Maximum current (i_{max})	711.3 A	708.4 A	**0.41**	61.85 A	61.55 A	**0.49**
Turn-on switched current (i_{on})	587.6 A	584.5 A	**0.53**	-	-	**-**
Turn-off switched current (i_{off})	711.3 A	708.4 A	**0.41**	0 A	0 A	**0**
Maximum voltage (v_{max})	1833 V	1833 V	**0**	1833 V	1833 V	**0**
Turn-on switched voltage (v_{on})	916 V	916 V	**0**	-	-	**-**
Turn-off switched voltage (v_{off})	1833 V	1833 V	**0**	916 V	916 V	**0**

TABLE B.30

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE OUTPUT SIDE SEMICONDUCTORS

	Diode D_3			**Diode D_4**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	97.92 A	97.68 A	**0.25**	101.9 A	101.2 A	**0.69**
rms current (I_{rms})	139.9 A	139.49 A	**0.29**	142.7 A	141.9 A	**0.56**
Maximum current (i_{max})	209.8 A	208.9 A	**0.43**	209.8 A	208.9 A	**0.43**
Turn-off switched current (i_{off})	209.8 A	208.9 A	**0.43**	189.8 A	188.9 A	**0.48**
Maximum voltage (v_{max})	5673 V	5679 V	**0.11**	5673 V	5643 V	**0.53**
Turn-off switched voltage (v_{off})	5673 V	5679 V	**0.11**	5673 V	5643 V	**0.53**

B.10 Push-pull

TABLE B.31

PASSIVE ELEMENTS

	Push-pull converter
C_{in}	82.674 µF
L_m	24.493 mH
L_1	6.955 mH
C_{out}	4.492 µF
n_2 / n_1	1
n_3 / n_1	1.6851

TABLE B.32

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_m	L_1	C_{out}
Simulation	Maximum stored energy	138.8 J	3.82 J	151.66 J	18.59 A
	rms current	101.3 A	10.66 A	199.6 A	4.20 A
	Maximum voltage stress	1833 V	1830 V	2880 V	2877 V
Analytical estimation	Maximum stored energy	138.8 J	3.47 J	153.12 J	19.14 J
	rms current	102.62 A	10.64 A	199.9 A	5.76 A
	Maximum voltage stress	1833 V	1833 V	2919 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**10.09**	**0.95**	**2.87**
	rms current	**1.29**	**0.19**	**0.15**	**27.08**
	Maximum voltage stress	**0**	**0.16**	**1.34**	**1.44**

TABLE B.33

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistors S_1-S_2			**Diodes D_1-D_2-D_3-D_4**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	151.5 A	152 A	**0.33**	99.9 A	99.7 A	**0.20**
rms current (I_{rms})	226.2 A	226.8 A	**0.26**	137.7 A	137.6 A	**0.07**
Maximum current (i_{max})	370.4 A	369.5 A	**0.24**	209.8 A	208.8 A	**0.48**
Turn-on switched current (i_{on})	303 A	302.3 A	**0.23**	-	-	**-**
Turn-off switched current (i_{off})	370.4 A	369.5 A	**0.24**	94.92 A	89.1 A	**6.53**
Maximum voltage (v_{max})	3666 V	3663 V	**0.08**	3088 V	3082 V	**0.19**
Turn-on switched voltage (v_{on})	1833 V	1833 V	**0**	-	-	**-**
Turn-off switched voltage (v_{off})	1833 V	1833 V	**0**	3088 V	3082 V	**0.19**

B.11 Push-pull isolated-boost

TABLE B.34
PASSIVE ELEMENTS

	Push-pull isolated-boost converter
C_{in}	10.334 µF
L_m	37.798 mH
L_1	6.047 mH
C_{out}	71.884 µF
n_2 / n_1	1
n_3 / n_1	1.2133

TABLE B.35
EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_m	L_1	C_{out}
Simulation	Maximum stored energy	17.36 J	2.84 J	304 J	300.1 J
	rms current	8.93 A	8.30 A	302.9 A	100.8 A
	Maximum voltage stress	1833 V	2385 A	1832 V	2890 V
Analytical estimation	Maximum stored energy	17.36 J	2.77 J	306.2 J	306.2 J
	rms current	8.74 A	8.28 A	303.2 A	99.9 A
	Maximum voltage stress	1833 V	2405 V	1833 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**2.53**	**0.72**	**1.99**
	rms current	**2.17**	**0.24**	**0.10**	**0.90**
	Maximum voltage stress	**0**	**0.83**	**0.05**	**0.99**

TABLE B.36
EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistors S_1-S_2			**Diodes D_1-D_2-D_3-D_4**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	151.5 A	151.3 A	**0.13**	99.9 A	99.6 A	**0.30**
rms current (I_{rms})	203.4 A	203.1 A	**0.15**	158.2 A	158 A	**0.13**
Maximum current (i_{max})	318.2 A	317 A	**0.38**	272.2 A	271.1 A	**0.41**
Turn-on switched current (i_{on})	137.9 A	137.1 A	**0.58**	-	-	**-**
Turn-off switched current (i_{off})	165.1 A	164.5 A	**0.36**	227.3 A	226.1 A	**0.53**
Maximum voltage (v_{max})	4811 V	4770 V	**0.86**	2919 V	2890 V	**1**
Turn-on switched voltage (v_{on})	4811 V	4770 V	**0.86**	-	-	**-**
Turn-off switched voltage (v_{off})	4353 V	4311 V	**0.97**	1459 V	1435 V	**1.67**

B.12 Half-bridge

TABLE B.37
PASSIVE ELEMENTS

	Half-bridge converter
C_{in1}	1.818 mF
C_{in2}	1.818 mF
L_m	6.123 mH
L_1	6.955 mH
C_{out}	4.492 µF
n_2 / n_1	3.3703

TABLE B.38

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in1}	L_m	L_1	C_{out}
Simulation	Maximum stored energy	763.8 J	7.80 J	151.9 J	18.72 J
	rms current	331.7 A	24.17 A	199.1 J	4.27 A
	Maximum voltage stress	1833 V	916 V	2890 V	2887 V
Analytical estimation	Maximum stored energy	763.8 J	3.47 J	153.1 J	19.44 J
	rms current	336 A	21.29 A	199.9 A	5.76 A
	Maximum voltage stress	1833 V	916 V	2919 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**124.78**	**0.78**	**3.70**
	rms current	**1.28**	**13.53**	**0.40**	**25.87**
	Maximum voltage stress	**0**	**0**	**0.99**	**1.10**

TABLE B.39

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistors S_1-S_2			**Diodes D_1-D_2-D_3-D_4**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	303 A	299.4 A	**1.20**	99.9 A	99.3 A	**0.60**
rms current (I_{rms})	452.5 A	446.9 A	**1.25**	137.7 A	137.1 A	**0.44**
Maximum current (i_{max})	740.8 A	745 A	**0.56**	209.8 A	208.9 A	**0.43**
Turn-on switched current (i_{on})	606.1 A	614.1 A	**1.30**	-	-	**-**
Turn-off switched current (i_{off})	740.8 A	745 A	**0.56**	94.9 A	91 A	**4.29**
Maximum voltage (v_{max})	1833 V	1835 V	**0.11**	3088 V	3145 V	**1.81**
Turn-on switched voltage (v_{on})	916 V	917 V	**0.11**	-	-	**-**
Turn-off switched voltage (v_{off})	916 V	917 V	**0.11**	3088 V	3145 V	**1.81**

B.13 Half-bridge isolated-boost

TABLE B.40
PASSIVE ELEMENTS

	Half-bridge isolated-boost converter
C_{in}	0.9394 µF
L_m	134.395 mH
L_1	66.525 mH
L_2	66.525 mH
C_{out}	35.942 µF
n_2 / n_1	0.6824

TABLE B.41
EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_m	L_1	C_{out}
Simulation	Maximum stored energy	1.57 J	4.17 J	817.7 J	145.3 J
	rms current	0.81 A	3.65 A	149.3 A	66.16 A
	Maximum voltage stress	1833 V	4173 V	2336 V	2843 V
Analytical estimation	Maximum stored energy	1.57 J	3.12 J	842.1 J	153.1 J
	rms current	0.79 A	4.31 A	151.6 A	64.9 A
	Maximum voltage stress	1833 V	4277 V	2444 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**33.65**	**2.90**	**5.09**
	rms current	**2.53**	**15.31**	**1.52**	**1.94**
	Maximum voltage stress	**0**	**2.43**	**4.42**	**2.60**

TABLE B.42

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistors S_1-S_2			**Diodes D_1-D_2-D_3-D_4**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	151.5 A	149.9 A	**1.07**	99.9 A	99.3 A	**0.60**
rms current (I_{rms})	208.8 A	206.8 A	**0.97**	149.1 A	148.2 A	**0.61**
Maximum current (i_{max})	304.4 A	301.1 A	**1.10**	243.1 A	241.1 A	**0.83**
Turn-on switched current (i_{on})	137.1 A	135.7 A	**1.03**	-	-	**-**
Turn-off switched current (i_{off})	165.9 A	163.9 A	**1.22**	200.9 A	198.9 A	**1.01**
Maximum voltage (v_{max})	4277 V	4169 V	**2.59**	2919 V	2842 V	**2.71**
Turn-on switched voltage (v_{on})	4277 V	4169 V	**2.59**	-	-	**-**
Turn-off switched voltage (v_{off})	3869 V	3775 V	**2.49**	1459 V	1417 V	**2.96**

B.14 Full-bridge

TABLE B.43

PASSIVE ELEMENTS

	Full-bridge converter
C_{in}	174.820 µF
L_σ	217.720 µH
L_1	13.911 mH
C_{out}	4.492 µF
n_2 / n_1	1.8957

TABLE B.44

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_σ	L_1	C_{out}
Simulation	Maximum stored energy	293.6 J	16.92 J	300.9 J	18.36 J
	rms current	179.6 A	353.8 A	198.6 A	3.79 A
	Maximum voltage stress	1833 V	1839 V	2862 V	2859 V
Analytical estimation	Maximum stored energy	293.6 J	17.22 J	306.2 J	19.14 J
	rms current	183 A	355.8 A	199.9 A	5.76 A
	Maximum voltage stress	1833 V	1833 V	2919 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**1.74**	**1.73**	**4.08**
	rms current	**1.86**	**0.56**	**0.65**	**34.20**
	Maximum voltage stress	**0**	**0.33**	**1.95**	**2.06**

TABLE B.45

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE TRANSISTORS

	Transistors S_1-S_4			**Transistors S_2-S_3**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	167.1 A	162.5 A	**2.83**	159.2 A	159.5 A	**0.19**
rms current (I_{rms})	246.7 A	245.4 A	**0.53**	243.5 A	243 A	**0.21**
Maximum current (i_{max})	397.7 A	394.3 A	**0.86**	397.7 A	394.5 A	**0.81**
Turn-off switched current (i_{off})	394.2 A	392.6 A	**0.41**	397.7 A	394.5 A	**0.81**
Maximum voltage (v_{max})	1833 V	1836 V	**0.16**	1833 V	1836 V	**0.16**
Turn-off switched voltage (v_{off})	1833 V	1836 V	**0.16**	1833 V	1836 V	**0.16**

TABLE B.46

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE FREEWHEEL DIODES

	Freewheel diodes D_{S1}-D_{S4}			**Freewheel diodes D_{S2}-D_{S3}**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	9.27 A	9.05 A	**2.43**	13.2 A	12 A	**10**
rms current (I_{rms})	49.3 A	48.5 A	**1.65**	63.8 A	59.3 A	**7.59**
Maximum current (i_{max})	394.2 A	392.6 A	**0.41**	397.7 A	394.5 A	**0.81**
Maximum voltage (v_{max})	1833 V	1836 V	**0.16**	1833 V	1836 V	**0.16**

TABLE B.47

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE DIODES

	Diodes D_1-D_2-D_3-D_4		
	Analytical estimation	**Simulation**	**Estimation error**
Average current (I_{ave})	90.9 A	99.2 A	**8.37**
rms current (I_{rms})	131.1 A	136.2 A	**3.74**
Maximum current (i_{max})	209.8 A	208 A	**0.87**
Maximum voltage (v_{max})	3474 V	3420 V	**1.58**

B.15 Full-bridge isolated-boost

TABLE B.48
PASSIVE ELEMENTS

	Full-bridge isolated-boost converter
C_{in}	10.334 µF
L_m	37.798 mH
L_1	6.047 mH
C_{out}	71.884 µF
n_2 / n_1	1.2133

TABLE B.49
EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_m	L_1	C_{out}
Simulation	Maximum stored energy	17.36 J	2.83 J	303.7 J	299.9 A
	rms current	8.92 A	8.30 A	302.7 A	100.7 A
	Maximum voltage stress	1833 V	2384 V	1832 V	2888 V
Analytical estimation	Maximum stored energy	17.36 J	2.77 J	306.2 J	306.2 J
	rms current	8.74 A	8.28 A	303.2 A	99.9 A
	Maximum voltage stress	1833 V	2405 V	1833 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**2.17**	**0.82**	**2.06**
	rms current	**2.06**	**0.24**	**0.16**	**0.80**
	Maximum voltage stress	**0**	**0.87**	**0.05**	**1.06**

TABLE B.50

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE SEMICONDUCTORS

	Transistors S_1-S_2-S_3-S_4			**Diodes D_1-D_2-D_3-D_4**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	151.5 A	151.3 A	**0.13**	99.9 A	99.6 A	**0.30**
rms current (I_{rms})	203.4 A	203 A	**0.20**	158.2 A	157.9 A	**0.19**
Maximum current (i_{max})	318.2 A	316.9 A	**0.41**	272.2 A	271 A	**0.44**
Turn-on switched current (i_{on})	137.9 A	137 A	**0.66**	-	-	**-**
Turn-off switched current (i_{off})	165.1 A	164.4 A	**0.43**	227.3 A	225.5 A	**0.80**
Maximum voltage (v_{max})	2405 V	2384 V	**0.88**	2919 V	2890 V	**1.00**
Turn-on switched voltage (v_{on})	2405 V	2384 V	**0.88**	-	-	**-**
Turn-off switched voltage (v_{off})	2176 V	2154 V	**1.02**	1459 V	1441 V	**1.25**

B.16 Single-active-bridge

TABLE B.51

PASSIVE ELEMENTS

	Single-active-bridge converter
C_{in}	334.832 µF
L_σ	217.720 µH
C_{out}	89.856 µF
n_2 / n_1	1.8957

TABLE B.52

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_σ	C_{out}
Simulation	Maximum stored energy	562.5 J	61.67 J	396.7 J
	rms current	318.5 A	443 A	119.8 A
	Maximum voltage stress	1833 V	3409 V	2971 V
Analytical estimation	Maximum stored energy	562.5 J	62.49 J	382.8 J
	rms current	315.4 A	437.4 A	115.3 A
	Maximum voltage stress	1833 V	3299 V	2919 V
Estimation error [%]	Maximum stored energy	**0**	**1.31**	**3.63**
	rms current	**0.98**	**1.28**	**3.90**
	Maximum voltage stress	**0**	**3.33**	**1.78**

TABLE B.53

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE INPUT SIDE SEMICONDUCTORS

	Transistors S_1-S_2-S_3-S_4			**Freewheel diodes D_{S1}-D_{S2}-D_{S3}-D_{S4}**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	170.4 A	171.9 A	**0.87**	18.9 A	18 A	**5**
rms current (I_{rms})	293.4 A	298.4 A	**1.68**	97.8 A	95.1 A	**2.84**
Maximum current (i_{max})	757.7 A	752.6 A	**0.68**	757.7 A	748.2 A	**1.27**
Turn-off switched current (i_{off})	757.7 A	752.6 A	**0.68**	0 A	0 A	**0**
Maximum voltage (v_{max})	1833 V	1837 V	**0.22**	1833 V	1837 V	**0.22**
Turn-off switched voltage (v_{off})	1833 V	1837 V	**0.22**	0 V	0 V	**0**

TABLE B.54
EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE OUTPUT SIDE SEMICONDUCTORS

	Diodes D_1-D_2-D_3-D_4		
	Analytical estimation	**Simulation**	**Estimation error**
Average current (I_{ave})	99.9 A	100.2 A	**0.30**
rms current (I_{rms})	163.1 A	165.2 A	**1.27**
Maximum current (i_{max})	399.6 A	397 A	**0.65**
Turn-off switched current (i_{off})	0 A	0 A	**0**
Maximum voltage (v_{max})	2919 V	2973 V	**1.82**
Turn-off switched voltage (v_{off})	2919 V	2973 V	**1.82**

B.17 Dual-active-bridge

TABLE B.55
PASSIVE ELEMENTS

	Dual-active-bridge converter
C_{in}	508.255 µF
L_{σ}	680.377 µH
C_{out}	156.203 µF
n_2 / n_1	1.6851

TABLE B.56

EXPRESSIONS OF THE RMS CURRENTS CIRCULATING THROUGH THE PASSIVE ELEMENTS, THEIR MAXIMUM VOLTAGE STRESS AND THE ENERGY THEY STORE

		C_{in}	L_σ	C_{out}
Simulation	Maximum stored energy	853.8 J	156.8 J	680.5 J
	rms current	428.2 A	531 A	241.6 A
	Maximum voltage stress	1833 V	3592 V	2951 V
Analytical estimation	Maximum stored energy	853.8 J	154.3 J	677.3 J
	rms current	412.4 A	523.1 A	237.5 A
	Maximum voltage stress	1833 V	3482 V	2944 V
Estimation error [%]	Maximum stored energy	**0**	**1.62**	**0.47**
	rms current	**3.83**	**1.51**	**1.73**
	Maximum voltage stress	**0**	**3.16**	**0.24**

TABLE B.57

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE INPUT SIDE SEMICONDUCTORS

	Transistors S_1-S_2-S_3-S_4			**Freewheel diodes D_{S1}-D_{S2}-D_{S3}-D_{S4}**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	195.8 A	200.8 A	**2.49**	44.3 A	43.2 A	**2.55**
rms current (I_{rms})	341.9 A	349.1 A	**2.06**	141 A	139.6 A	**1.00**
Maximum current (i_{max})	673.5 A	678.9 A	**0.80**	673.5 A	674.6 A	**0.16**
Turn-off switched current (i_{off})	673.5 A	678.9 A	**0.80**	0 A	0 A	**0**
Maximum voltage (v_{max})	1833 V	1837 V	**0.22**	1833 V	1837 V	**0.22**
Turn-off switched voltage (v_{off})	1833 V	1837 V	**0.22**	0 V	0 V	**0**

TABLE B.58

EXPRESSIONS OF THE VOLTAGES/CURRENTS IN THE OUTPUT SIDE SEMICONDUCTORS

	Transistors S_5-S_6-S_7-S_8			**Freewheel diodes D_{S5}-D_{S6}-D_{S7}-D_{S8}**		
	Analytical estimation	**Simulation**	**Estimation error [%]**	**Analytical estimation**	**Simulation**	**Estimation error [%]**
Average current (I_{ave})	21.2 A	21.7 A	**2.30**	121.2 A	123.1 A	**1.54**
rms current (I_{rms})	71.4 A	72.5 A	**1.52**	207.5 A	211 A	**1.66**
Maximum current (i_{max})	359.7 A	361.5 A	**0.50**	399.6 A	402.9 A	**0.82**
Turn-off switched current (i_{off})	359.7 A	361.5 A	**0.50**	0 A	0 A	**0**
Maximum voltage (v_{max})	2944 V	2953 V	**0.30**	2944 V	2953 V	**0.30**
Turn-off switched voltage (v_{off})	2615 V	2615 V	**0**	0 V	0 V	**0**

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