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50 kW Partial Power Converter for EV Charging

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Abstract- This paper presents the design and assembly of a 50 kW dual active bridge partial power converter. Due to the reduction in the power processed by the converter, the maximum power observed by the converter is set to 4.7 kW. In consequence, the implementation of silicon-based discrete switching devices is enabled, which reduces the final cost and volume. Additionally, this document presents the design and assembly of the rest of the passive components: transformer, capacitors, heatsink… Finally, all the power stage is embedded inside a standardized enclosure: a 19 inch (482.6 mm) 4U front panel rack.

Index Terms- Partial power converter, Dual active bridge, High power converter, Electric vehicle charging.

I. INTRODUCTION

Partial power converters (PPC) are architecture solutions that reduce the power processed by the converter [1]–[4]. The most popular PPC architectures are the input-parallel-output-series (IPOS) and the input-series-output-parallel (ISOP) architectures, see Fig. 1. The parameter that measures the reduction of the power processed by the converter is the partial power ratio (K_{pr}) and it is defined as the division between the converter power (P_{conv}) and the source power (P_{source}) (1). Applying Kirchhoff's laws, the K_{pr} curves of both architectures are obtained as a function of the static voltage gain (G_V), see (2)-(4), [1].

$$K_{pr} = \frac{P_{conv}}{P_{source}} \tag{1}$$

$$K_{pr_{IPOS}} = 1 - \frac{1}{G_V} \tag{2}$$

$$K_{pr_{ISOP}} = 1 - G_V \tag{3}$$

$$G_V = \frac{V_{load}}{V_{source}} \tag{4}$$

where $K_{pr_{IPOS}}$ and $K_{pr_{ISOP}}$ are the processed power ratios of the IPOS and ISOP architectures. Fig. 2 shows the resulting curves.

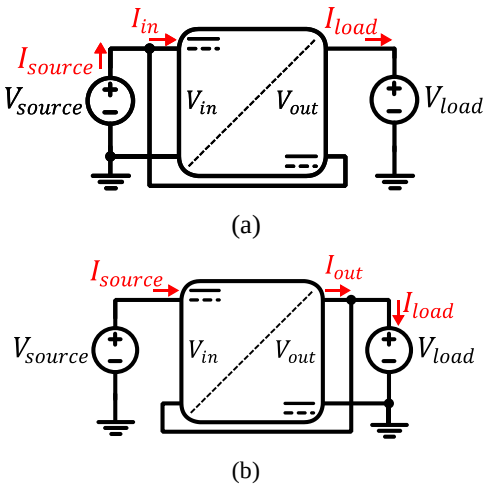

Fig. 1. Connection of PPCs. (a) IPOS. (b) ISOP.

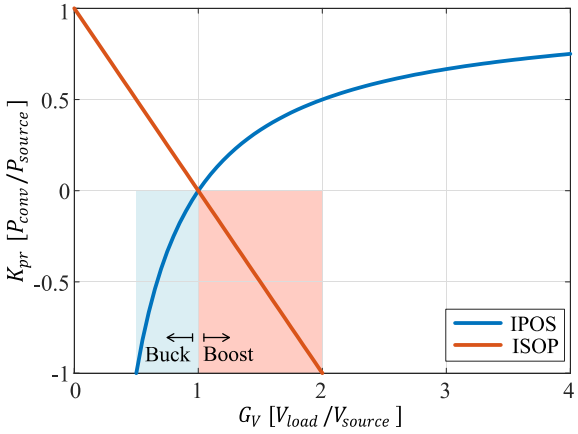

Fig. 2. K_{pr} curves of IPOS and ISOP architectures.

As illustrated, as G_V approaches 1, K_{pr} is reduced in both IPOS-ISOP architectures. Thus, the smaller the difference between the source and load voltages, the less power processed by the converter.

In recent years, PPCs have emerged as highly efficient solutions [5]–[7]. Their ability to process reduced power not only enhances efficiency, but it also allows for the development of high-density converters with reduced electrical stress. These advantages have sparked significant interest in their application across various fields [8]–[10]. Despite numerous prototypes presented in the literature, the majority are limited to a few kilowatts. This results in a notable gap in evidence for the design and assembly of high-power PPCs. Authors from [11] present the design and implementation of a 22 kW prototype, but it can only handle unidirectional power flow and its design is not optimized for a standardized enclosure. Therefore, the authors of this paper conclude that further research is required to demonstrate that the implementation of PPC solutions in high-power applications can bring interesting benefits, for example: the implementation of Silicon (Si)-based discrete devices [12]. This technology ensures maturity, robustness, low cost and large supply. Bearing this in mind, this paper aims to contribute to the PPC literature by demonstrating the viability of these solutions in high-power applications. The primary contributions include:

- The design and assembly of a 50 kW PPC.
- The implementation of Si-based discrete devices for a high-power application.

II. Application Selection and Description

The main benefits of IPOS-ISOP type PPC architectures are obtained at low K_{pr} conditions. However, a great voltage variability affects negatively to their efficiency and thermal stress. In fact, compared to full power converter (FPC) solutions, one of the main disadvantages of IPOS-ISOP type architectures is the extended operation range of the converter [1]. Considering this, a suitable application for the high-power PPC must ensure a low K_{pr} and a low voltage variability of the source and the load. In this case, the selected application consists of an electric vehicle (EV) fast charging DC-DC unit. Fig. 3 presents the typical configuration of an EV fast charging station. The AC-DC stage is out of the scope of this paper.

Depending on the EV model, the voltage level at the output of the DC-DC can vary from 400 V up to 800 V [14]. This is not beneficial for a PPC converter, whose performance is highly dependent on the low voltage variability. However, if the charging station consists of a fleet of EVs, the implementation of PPCs is more adequate. In this case, the only variability between V_{EV} is related to the Open Circuit Voltage (OCV) curve of the battery. Typically, fast chargers operate only in the constant current (CC) mode, from a 10 % state-of-charge (SoC) up to a SoC of 80 % or 90 % [14]. So, the voltage operation range is limited to the values shown in Fig. 4. On the other hand, the application's power peak value is set to 50 kW. Table 1 resumes the main electrical parameters of the DC-DC stage. Since it consists of a step-down application, the ISOP architecture is selected due to its reduced K_{pr} in buck operation, as shown by Fig. 2.

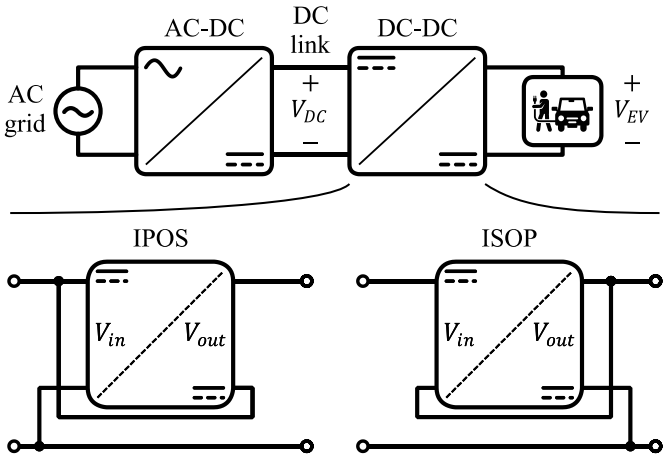

Fig. 3. Simplified electric diagram of the high-power DC-DC charging unit under analysis.

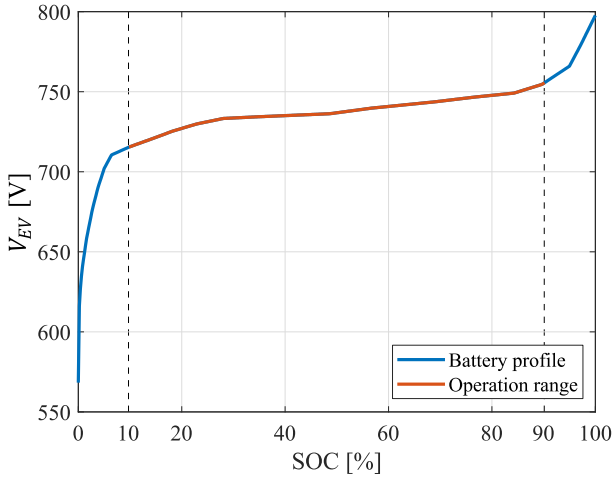

Fig. 4. Operation range of the EV fast charging DC-DC under analysis. Based on the OCV curve of a LiFePo cell [13].

Table 1. Main electrical parameters of the DC-DC stage, where $V_{EV_{o.e.}}$ refers to the operation range from Fig. 4. For simplicity reasons, through the rest of the document $V_{EV_{o.e.}}$ will be substituted by V_{EV}.

Parameter	Value
$V_{DC} = V_{source}$	800 V
$V_{load} = V_{out} = V_{EV_{o.e.}}$	From 715 V to 755 V @ From 10 % to 90 % SOC
$P_{load} = P_{EV}$	From 44.84 kW to 47.63 kW @ Constant I_{EV} at 62.68 A

III. Design of the Prototype

The selected topology for this analysis is the dual active bridge PPC (DAB-PPC). The reasons are galvanic isolation (essential to avoid a short-circuit [15]), bi-directionality and controllability. The switching frequency is stablished at 20 kHz. This switching frequency is compatible with both MOSFET and IGBT devices, which enables the comparison of both technologies.

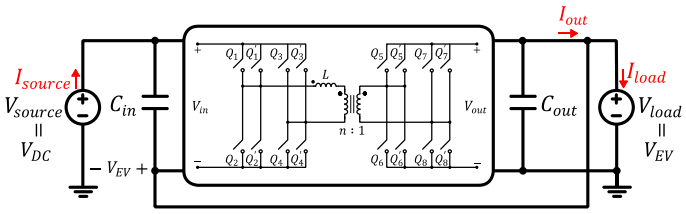

Fig. 5. DAB-PPC under analysis.

Table 2. Main electrical parameters of the PPC through the charging of the EV.

Parameter	Value
$V_{in,min}$ to $V_{in,max}$	45 V to 85 V
$V_{out,min}$ to $V_{out,max}$	715 V to 755 V
$I_{in,min}$ to $I_{in,max}$	56 A to 59 A
$I_{out,min}$ to $I_{out,max}$	3.47 A to 6.62 A
$K_{pr,min}$ to $K_{pr,max}$	0.055 to 0.105
$P_{conv,min}$ to $P_{conv,max}$	2.6 kW to 4.7 kW
f_{sw}	20 kHz

Fig. 5 shows a simplified diagram of the DAB-PPC. The number of semiconductors is doubled (connected in parallel) to decrease their thermal and electrical stress. Then, Table 2 shows the main electrical parameters of the converter. The primary side presents low-voltage high-current values, whereas the secondary side presents high-voltage and low-current. These diverging electric conditions are critical for the appropriate selection of the respective switches.

A. *Inductance value*

The inductance value of the DAB-PPC is a key parameter that directly affects the performance of the rest of the devices. Its value defines the RMS currents inside the converter and it also decides whether the semiconductors work under zero voltage switching (ZVS) or hard switching conditions.

Table 2 defines the range of the main parameters of the converter. These parameters are necessary for the design of the inductance and they are obtained considering equation (3), Fig. 5, Table 1 and Table 2. As example:

$$V_{in,min} = V_{source} - V_{EV,max} \tag{5}$$

$$V_{in,max} = V_{source} - V_{EV,min} \tag{6}$$

$$P_{conv,min} = P_{EV,max} \cdot K_{pr,min} \tag{7}$$

The first step is to define the transformer transformation ratio (n). The voltage and current values from Table 2 show that a 10 times ratio exists between the primary side and the secondary side. Therefore, n is defined at 0.1, which consists of a round value that simplifies the assembly. The second step is to obtain an inductance value that ensures ZVS operation through all the CC charging process. To do so, the boundaries of the ZVS regions are calculated following the steps described in [16]. Fig. 6 shows the ZVS regions for the concerned application. The dashed lines represent the trajectory of the operating points of the converter through a CC charging process. Each dashed line corresponds to an inductor value, which is given by (8). In this application, both phase-shift trajectories consist of a vertical line because as V_{out} increases (due to the OCV curve), V_{in} decreases the same amount (due to the IPOS architecture). Therefore, through the CC period the phase-shift remains constant.

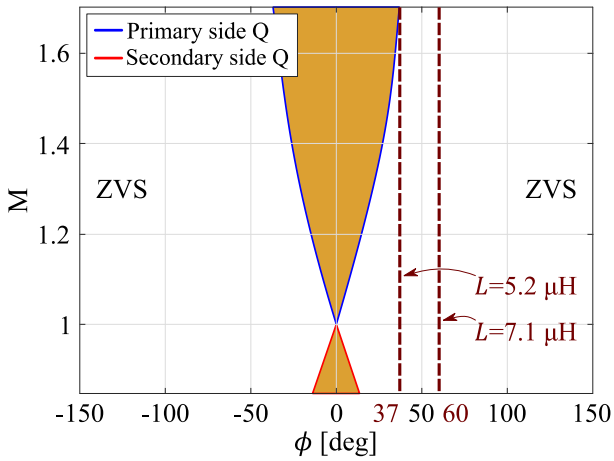

Fig. 6. ZVS regions and boundaries for primary and secondary side semiconductors using phase-shifted modulation (PSM) M is defined as $\frac{V_{in}}{V_{out} \cdot n}$.

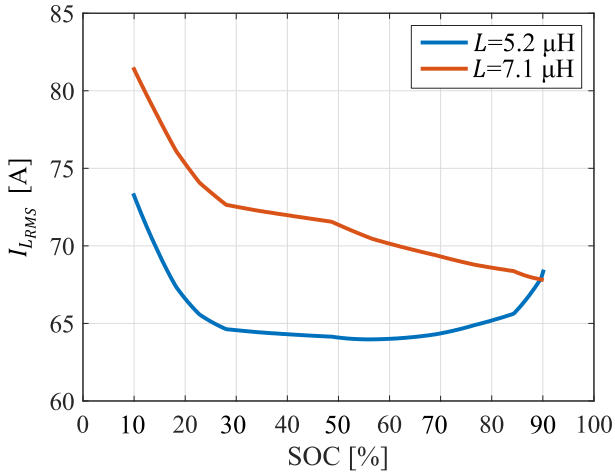

*Fig. 7. Inductor RMS current for **L**=5.2 µH and **L**=7.1 µH through the operation range.*

$$L = \frac{n \cdot V_{in} \cdot V_{out} \cdot \phi_{rad} \cdot (\pi - |\phi_{rad}|)}{2 \cdot \pi^2 \cdot f_{sw} \cdot P_{conv}} \tag{8}$$

where, ϕ_{rad} is the phase-shift in radians.

In (8), two different values are given to ϕ_{rad}: $\pi/5$ (37º), which is the minimum value that ensures ZVS for all the devices, and $\pi/3$ (60º), the maximum value that keeps a safe margin to compensate the power losses. $\phi_{rad} = \pi/5$ requires an inductance of 5.2 µH, and $\phi_{rad} = \pi/3$ requires and inductance of 7.1 µH.

Table 3. Selected switching devices for comparison.

Device	Manufacturer ID (Technology)	Voltage class	Conduction characteristics
Primary Q_{1-4}	STGW75H65DFB2-4 (IGBT)	650 V	$V_{CE_{sat}}$=1.9 V @ T_j= 175ºC
	IPZ60R017C7 (MOSFET)	650 V	R_{DS}=33 mΩ @ T_j= 150ºC
Secondary Q_{1-4}	IKY40N120CS6 (IGBT)	1200 V	$V_{CE_{sat}}$=2.25 V @ T_j= 175ºC
	-	-	-

Then, Fig. 7 compares the inductor RMS current achieved with each solution. Both solutions present their maximum values at initial charging conditions. However, their curves behave differently as the battery charges. The L=5.2 µH design shows a convex curve, whereas the L=7.1 µH shows a decreasing slope. In overall, it is clear that L=5.2 µH presents lower RMS values through all the CC charging process. Therefore, it is concluded that the selection of the inductance value entails a trade-off between low inductor RMS current and ZVS operation. In this case, an intermediate value is selected for the design: L=6.3 µH. The required phase-shift for this design is 49º.

B. Switching devices

As it can be observed in Table 2, the current/voltage requirements from the primary and secondary side are very different: low voltage (80 V) and high current (60 A) at the primary side, and high voltage (800 V) and low current (6 A) at the secondary side. This subsection selects the appropriate transistor technology for each side. In order to emphasize the benefits of PPC architectures, the search is limited to:

- **TO-247-4 package.** High power converters usually implement module type package for the switching devices. This work aims to show that PPC solutions enable the implementation of discrete devices. In this case, the TO-247-4 package is selected due to its extra Kelvin emitter connection, which improves the switching characteristics.

- **Silicon technology.** The wide and large variety of Si devices is an important advantage against SiC-based devices. The low current/voltage class Si-based devices in the market boost their implementation in PPC architectures. Furthermore, their reduced cost and maturity turn these devices into ideal solutions for PPC architectures.

Table 3 shows the selected devices under analysis. Regarding the primary side, two transistor technologies are compared: IGBT and MOSFET. Although the maximum voltage expected in the primary side is around 80 V, 600 V devices are selected. This is because there is no IGBT for a voltage class lower than 600 V. So, in order to make a fair comparison a 600 V MOSFET is also selected. Regarding the secondary side, a voltage class of 1200 V is defined. No MOSFET is considered for the secondary side bridge. At this voltage level, the on-state resistance of Si-based MOSFETs reaches up to units or tens of ohms.

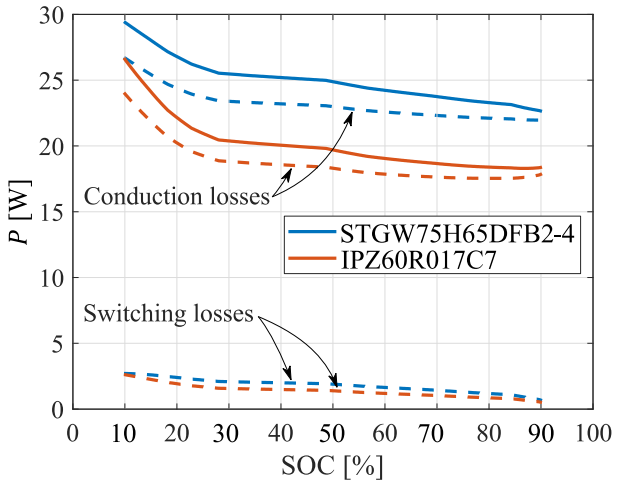

Fig. 8. Power losses of a single device at the primary side. The solid line represents the sum of the conduction and switching losses.

Fig. 8 compares the power losses of a single switching device at the primary side. The solid lines represent the total power losses of each technology and the dashed lines represent the conduction and switching losses. In both cases, the predominant losses are due to the conduction. This is because of the high current at the primary side. The switching losses are minimum due to the ZVS operation and the low blocking voltage. The results demonstrate that the MOSFET devices present a more efficient performance. So, they are selected for implementation at the primary side of the prototype. Indeed, the simulations show a maximum value of power losses of 450 W. This means that the efficiency of the system would be higher than 99 %. Also, it must be mentioned that the MOSFETs under analysis are designed for a voltage class of 600 V. Selecting lower voltage class devices would decrease the $R_{DS,on}$ value and improve the efficiency. However, in order to achieve a robust prototype, the IPZ60R017C7 device is kept. At the secondary side, the IKY40N120CS6 device is implemented.

C. Input-output capacitor

The output capacitance (C_{out}) is defined to achieve a maximum ripple voltage of 1 %. In this case, an output capacitance of 70 µF ensures a maximum peak-to-peak voltage (V_{pk-pk}) of 8 V through all the operation range.

Regarding the input capacitance (C_{in}), its value is defined to protect the primary side semiconductors. To explain this, Fig. 9 presents the overvoltage issue that exists with ISOP architectures at no load conditions. Assuming the case in which the source is connected to the converter, but no load is connected yet, the resulting circuit is simplified to a voltage divider defined by C_{in} and C_{out}. Thus, the voltages V_{in} and V_{out} are defined by (9), (10).

$$V_{in} = V_{source} \cdot \frac{C_{out}}{C_{in}} \tag{9}$$

$$V_{out} = V_{source} \cdot \frac{C_{in}}{C_{out}} \tag{10}$$

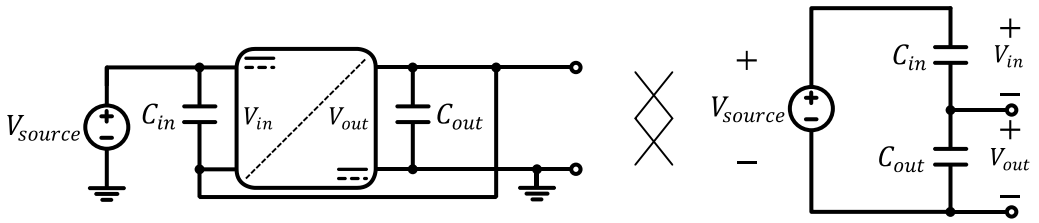

Fig. 9. Overvoltage issue with ISOP architectures at no load conditions.

Fig. 10. Image of the assembled 19 inch rack.

Since the primary side semiconductors are designed for a reduced voltage, C_{in} is defined to keep a maximum voltage of 170 V (double of $\widehat{V_{in}}$ from Table 2). The result is given by (11).

$$C_{in} = V_{source} \cdot \frac{C_{out}}{V_{in}} = 800\ \text{V} \cdot \frac{70\ \mu\text{F}}{170\ \text{V}} = 330\ \mu\text{F} \qquad (11)$$

IV. Prototype Assembly

Apart from the design of a 50 kW prototype, one of the main objectives of this work is to assemble it inside a standardized enclosure. This type of solutions are highly implemented in the industry due to their ease of assembly and modularization. Therefore, in order to get closer to a real case scenario, this work aims to fit the 50 kW converter inside a 19 inch (482.6 mm) 4U front panel rack.

Fig. 10 shows a real image of the assembled 19 inch rack. The front panel is custom-built to fit all the power connectors, manual switches and communication ports, as well as the air intake of the cooling system.

A. Transformer with integrated inductor

With the aim of reducing the volume of the magnetic elements, the leakage inductance (L_{lk}) of the transformer is designed to match the required inductance by the DAB-PPC. To achieve this, a magnetic design tool developed in Mondragon University is used. Table 4 describes the input-output parameters of the tool and the experimental results of the assembled transformer.

The inputs or design specifications of the design tool are: the most restrictive current and voltage waveforms, the switching frequency, the transformation ratio and the desired leakage inductance. The outputs or assembly parameters are: the core, the wire, the number of turns and the winding geometry. The litz wire is defined as the number of strands (N_{st}) times the diameter of each strand in µm. Also, the expected magnetizing inductance and the leakage inductance range is defined. Based on the assembly parameters, the transformer shown in Fig. 11 is assembled. The difference between Fig. 11a and Fig. 11b is the distance between the primary and secondary windings. The closer they are (Fig. 11a), the less flux leakage exists. Thus, the minimum leakage inductance is achieved: L_{min}=5.75 µH. The further they are (Fig. 11b), the higher the flux leakage. Hence, the maximum leakage inductance is achieved: L_{max}=8.89 µH. By adjusting the gap, the leakage inductance is set to 6.3 µH.

Table 4. Parameters of the assembled transformer with integrated inductance.

Parameter	Design specs.	Assembly parameters	Experimental results
Current waveform	Most restrictive	-	-
Voltage waveform	Most restrictive	-	-
f_{sw}	20 kHz	-	-
n	0.1	-	0.0999
L_m (magnetizing)	-	324 µH	269.9 µH
L_{lk} (leakage)	6.3 µH	[3.14, 17] µH	[5.75, 8.9] µH
Core	-	EE8020	EE8020
Prim. side wire Sec. side wire	-	400x200 200x100	400x200 200x100
Turns	-	6 60	6 60

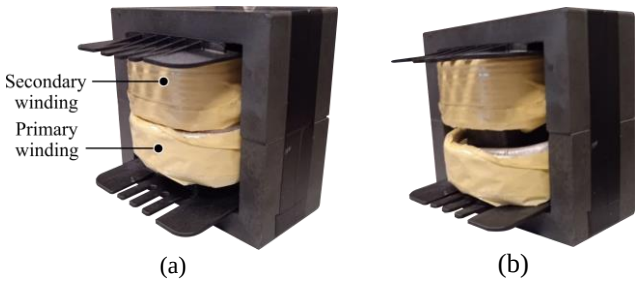

Fig. 11. Assembled transformer. Configuration for (a) minimum leakage inductance. (b) maximum leakage inductance.

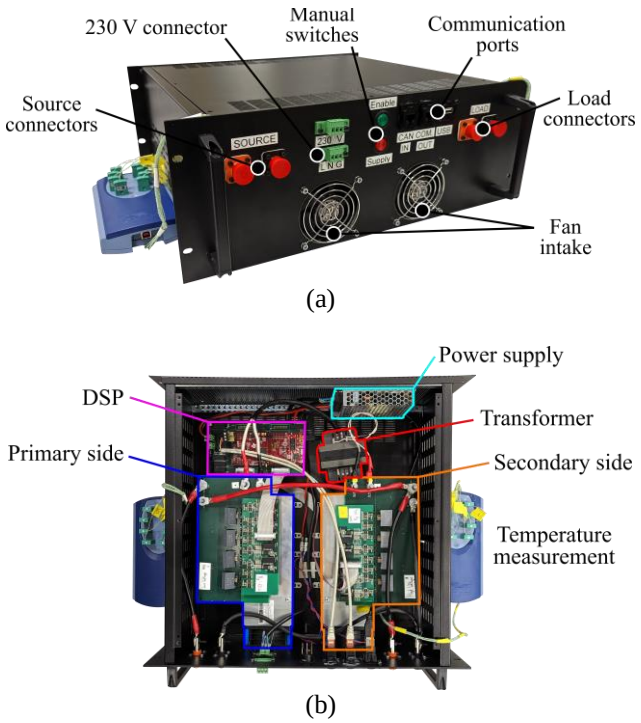

Fig. 12. Assembled rack. (a) Front view. (b) Internal arrangement.

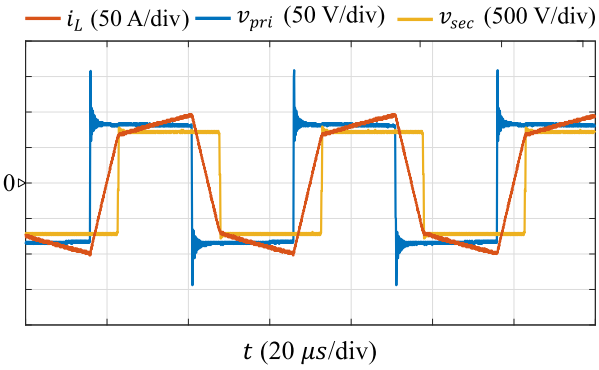

Fig. 13. Experimental steady state waveforms of the DAB-PPC at 10 % SoC.

B. Rack assembly

Fig. 12a shows the front view design of the rack. First, there are the source connectors and load power connectors. A 230V AC grid connector is also present to power the control hardware and cooling systems. Additionally, manual switches are added to the front panel: a supply switch (red) to feed/cut the 230 V AC power, and an enable switch (green) to enable/disable the power flow by activating/deactivating the PWM signals. Three communication ports are also added for connecting to the DSP: one allowing quick access to the USB type-A and two ports for CAN communication. The intake holes for the cooling system (forced convection) are in the lower middle area of the panel.

In Fig. 12b, the top view of the arrangement of the different components is shown. Great part of the volume is occupied by the primary side and secondary side power blocks (including the heatsinks and fans). The DSP is located on the back-left corner and the power supply is attached to the back-side panel. The transformer is highlighted to observe its volume. Finally, the top-case temperature measurements are taken out via thermocouples.

To demonstrate the correct operation of the converter, Fig. 13 shows the main experimental waveforms of the DAB-PPC: transformer current (i_L), primary side voltage (v_{pri}) and secondary side voltage (v_{sec}). As it can be observed, at the primary side of the transformer, an RMS current of 77.5 A appears, but with an AC voltage of ± 85 V. This reduced voltage consists of the difference between the source and the load.

V. Conclusion

This paper presents the design and assembly of a 50 kW DAB-PPC for EV charging. In order to achieve a modular solution, all the components are assembled inside a standardized enclosure (4U front panel rack). The benefits of the assembled DAB-PPC include the implementation of Si-based discrete switching devices (TO-247 type package) for a high power application and reduced voltage class. Indeed, although the application is rated for 800 V, the primary side semiconductors consist of 600 V devices. Also, ZVS in ensured for all the semiconductors. This way, the switching losses are minimized, which turns the performance of the converter into a purely conduction application. Apart from that, the volume of the magnetics is reduced by matching the leakage inductance of transformer with the required inductance of the DAB. Finally, the main experimental waveforms of the assembled prototype are shown to demonstrate its correct operation. The next steps involve extended experimental testing of the converter to obtain its efficiency and thermal behaviour.

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