J. Anzola, I. Aizpuru and A. Arruti, "Non-Isolated Partial Power Converter for Electric Vehicle Fast Charging Stations," *2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Dubrovnik, Croatia, 2020, pp. 18-22.

DOI: https://doi.org/10.1109/PEDG48541.2020.9244345

Non-Isolated Partial Power Converter for Electric Vehicle Fast Charging Stations

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***Abstract*— In the present paper a partial power converter is proposed for an electric vehicle fast charging station. The main advantage of this type of converter is that it only processes a reduced percentage of the power consumed by the load. Apart from that, the classical partial power converter architectures presented in the literature require an isolated topology for the stage of conversion. However, in this document a non-isolated topology is applied, specifically, an interleaved single ended primary inductor converter. In addition, in order to observe its benefits, the proposed converter is compared with a conventional full power converter. Finally, it is concluded that the proposed partial power architecture is an attractive solution due to its reduction in the processed power by the converter and its improvement in the efficiency of the application.**

Keywords—electric vehicle, fast charging station, partial power processing, partial power converter, non-isolated

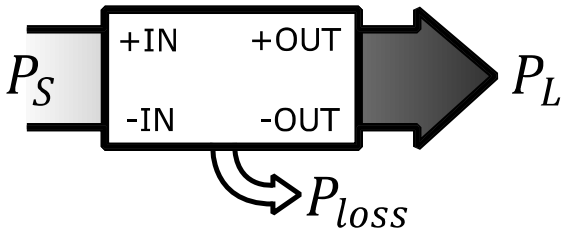
I. INTRODUCTION

Due to its efficient performance and reduced green-house emissions, the electric vehicle (EV) is turning into a real alternative to conventional combustion based vehicles. Indeed, its shelling data increases year by year [1], together with the number of EV charging stations [2]. When it comes to the installation of EV charging stations, one can find different types of solutions divided by their power level [3]. On one hand, up to 10kW AC charging stations can be found. On the other hand, DC wise, two main groups exist: fast charging stations (between 20kW and 120kW) and extreme fast charging stations (higher than 120 kW). Due to the high peak power values, the charging times can be reduced up to 15 minutes or higher [4], which makes the EV more attractive to the customer. Regarding fast charging stations, they are structures that are divided in different phases [5]. Usually, they are connected to a medium voltage AC grid and, then, the voltage level is reduced and rectified. Finally, several DC/DC power converters are implemented to charge each EV at the station. This paper will focus on the design of this DC/DC converter, which is connected between a common DC bus and the energy storage system (ESS) of the EV. Since the mentioned converter is required to process great power values (≥120kW), its size, cost and performance are key factors that must be optimized through its design. Due to this, recent literature around EV fast charging applications presents advance architectures based on partial power processing (PPP) [6]. This type of architectures aim to reduce the power processed by the converter, achieving reduced size and more efficient converters [7], [8]. Therefore, it is concluded that PPP based converters are very suitable for the concerned application. The literature around PPP presents different strategies that achieve a reduction of the total power processed by the converter [9]. On one side, differential power converters (DPC) can be found, whose main objective is to correct current unbalances between series connected elements. On the other side, there are the partial power converters (PPC), which can achieve step-up/step-down and power flow control between a source and a load. For example, authors from [3], [4], [6] present a PPC based on an isolated full bridge for a fast charging application. There, it is concluded that PPCs achieve converter rating reduction and efficiency improvements. Bearing this in mind, due to the lack of research around PPC based on non-isolated topologies, the objective of this paper is to implement an interleaved single ended primary inductor converter (SEPIC) on a PPC for an EV fast charging application. In order to achieve this, section II explains the term PPP and its basis. Then, section III describes the case studio together with the comparison parameters. Later, section IV shows the obtained results and, finally, sections V and VI present the conclusions obtained through the paper and the proposed future lines, respectively.

II. BASIS OF PPP

As its name indicates, a power converter based on the PPP concept only processes a reduced percentage of the total power that goes from the source to the load. As example, Fig. 1 shows the power flow of a converter based on Full Power Processing (FPP) and a converter based on PPP. On one hand, as it can be observed in Fig. 1a, the FPP converter is designed to process the 100% of the power consumed by the load, generating a given quantity of losses. On the other hand, Fig. 1b shows the PPP concept, which is based on achieving a reduction of the power processed by the converter. This way, the losses generated by the power converter are reduced, as well as its size. Furthermore, maintaining the same efficiency for the power converter, the global efficiency of the system increases.

The PPP concept was presented for the first time in spacecraft industry [10], where downsizing power converters connected to photovoltaic panels was the main priority. This way, a more efficient converter with higher power density is achieved without affecting the robustness of the system. As mentioned before, there are different advanced architectures that achieve a reduction of the total power processed by the converter



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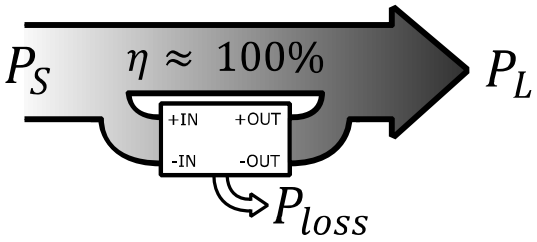


B)

Fig. 1. Power flow diagram. A) FPP. B) PPP.

but, this paper only focuses on PPCs. In the literature, different types of PPC architectures can be found and Fig. 2 presents several examples for step-down applications[6], [11]–[13]. On one hand, architectures from Fig. 2a and Fig. 2b are referred as "Input-Series-Output-Parallel" (ISOP) and "Input-Parallel-Output-Series" (IPOS), respectively. On the other hand, architecture from Fig. 2c is defined as "Fractional Converter" (FC) [13]. As it can be observed, the three architectures from Fig. 2 are designed for step-down applications, however, architectures from Fig. 2a and Fig. 2b require an isolated topology inside the converter that prevents a short-circuit in V_L [7]. Instead, Fig. 2c allows non-isolated topologies inside the converter, which simplifies the power conversion.

In order to compare the architectures shown in Fig. 2, the next step is to calculate the processed active power ratio of the converter at each one. For that purpose, the architecture from Fig. 2a is taken as an example. Firstly, Kirchhoff's laws are applied on the architecture, obtaining equations (1) and (2). In addition, the efficiency of the system can be defined as shown in (3).

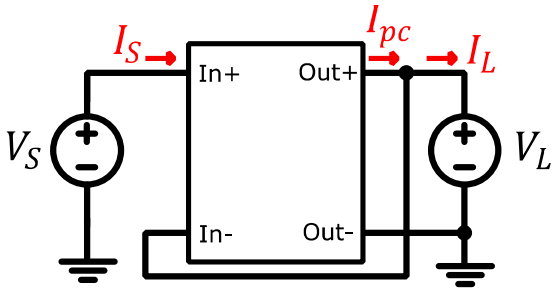
$$V_S - V_{in} = V_L \quad (1)$$

$$I_S + I_{pc} = I_L \quad (2)$$

$$\eta_{system} = \frac{V_L \cdot I_L}{V_S \cdot I_S} \quad (3)$$

On the other hand, the processed active power ratio of the converter (K_{pr}) is defined as the division between the processed power of the converter and the source's power (4).

$$K_{pr} = \frac{P_{conv}}{P_S} = \frac{V_{out} \cdot I_{pc}}{V_S \cdot I_S} \quad (4)$$



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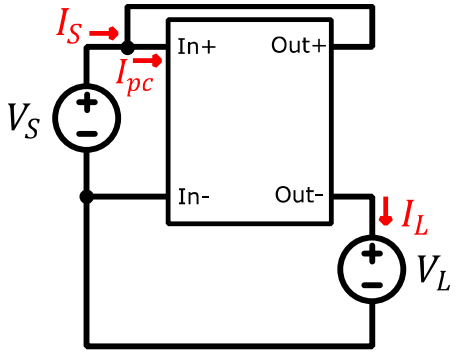

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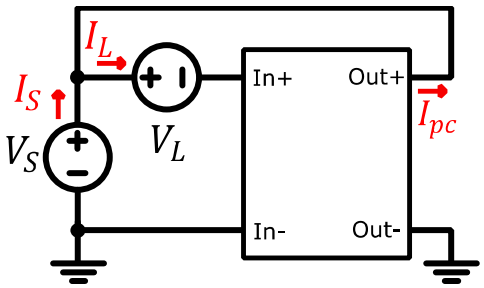


C)

Fig. 2. Step-down PPC architectures. A) ISOP. B) IPOS. C) FC.

Applying equations (1),(2) and (3) on (4), it is possible to obtain the K_{pr} curve of an ISOP step-down architecture in function of the static voltage gain $\left(G_V = \frac{V_L}{V_S}\right)$, see (5).

$$K_{pr} = \eta_{system} - G_V \quad (5)$$

Then, Fig. 3 shows the K_{pr} curve of each converter from Fig. 2 compared to a FPC. In first place, it is evident that the FPC always processes the 100% of the power that flows from the source to the load. Then, PPC wise, it is observed that the architecture that obtains the lowest K_{pr} curve is the ISOP. When it comes to the IPOS and FC architectures, when G_V is lower than 0.5, the K_{pr} value achieved by both architectures is higher than 1. This means that the converter is no longer working on the PPP range. In conclusion, depending on the G_V value of the application, the implementation of an ISOP step-down or a FC step-down entails a trade-off between the processed power ratio and the simplicity of the power conversion circuit.

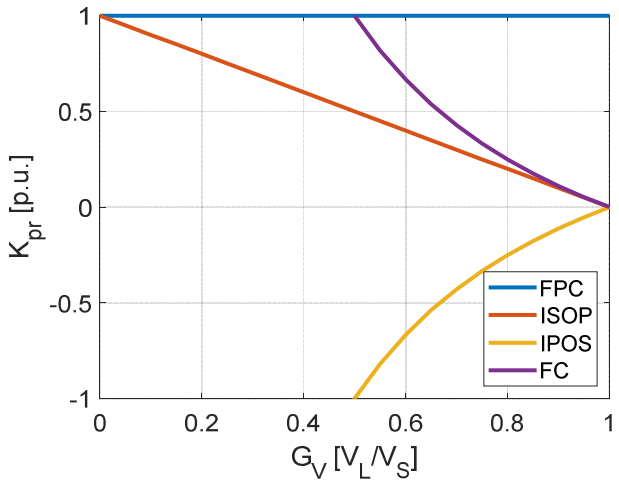


Fig. 3. Processed power ratio of each converter from Fig. 2.

III. CASE STUDIO

The aim of the present section is to describe the comparison between a conventional FPC and a PPC. With this purpose, Table 1 and Fig. 4 present an EV fast charging application example.

Table 1. Electrical parameters of an EV fast charging station.

Parameter	Value
V_S [V]	520
V_{EV} [V]	300 ÷ 500
P_{EV} [kW]	100

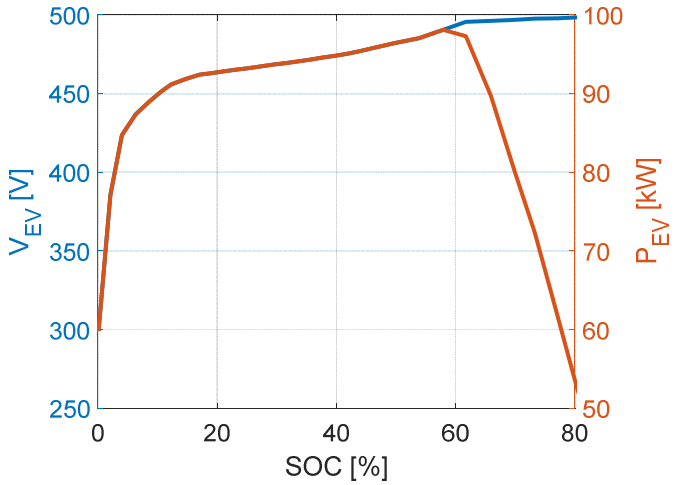


Fig. 4. Voltage and power level of the EV during the charging process.

A. Selected architecture and topology

Since the main objective of the paper is to observe the behaviour of non-isolated topologies on PPC architectures, the only solution from Fig. 2 that allows it is the FC, see Fig. 2c. On the other hand, topology wise, a 4 times interleaved SEPIC has been implemented due to its step-up/step-down capabilities and true shutdown. As a result, Fig. 5 shows the two solutions to compare: a SEPIC on a FPC and on a PPC architecture.

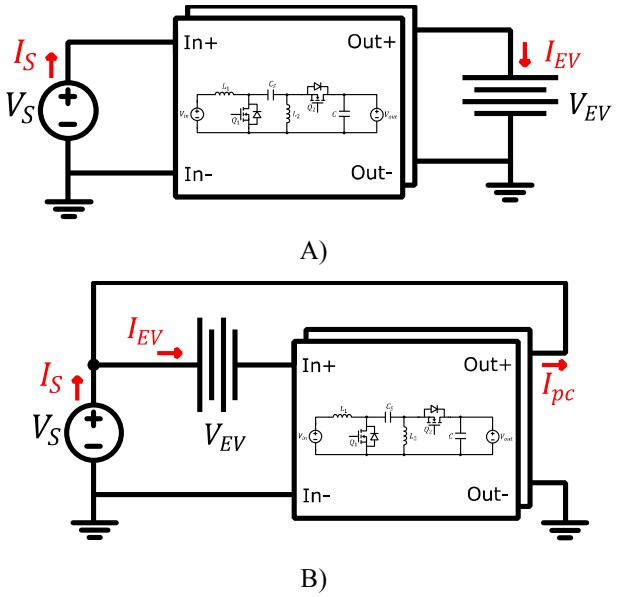


Fig. 5. Simplified diagram of the simulated architectures. A) SEPIC-FPC. B) SEPIC-PPC.

B. Comparison parameters

This paper proposes three main factors when comparing the architectures from Fig. 5: the processed active power ratio of the converter, the component stress factor (CSF) and the efficiency of the system and the power converter. In first place, the processed active power ratio is defined by (4), where the power processed by the converter is divided by the power supplied by the source. Then, when it comes to the CSF, equations (6)-(9) are applied for calculating the stress suffered by the semiconductors and inductors, respectively [14].

$$SCSF_i = \frac{V_{max}^2 \cdot I_{rms}^2}{P_S^2} \quad (6)$$

$$WCSF_i = \frac{V_{max}^2 \cdot I_{rms}^2}{P_S^2} \quad (7)$$

$$SCSF_{tot} = \sum_{i=1}^{n} SCSF_i \quad (8)$$

$$WCSF_{tot} = \sum_{i=1}^{n} WCSF_i \quad (9)$$

Where, V_{max} for the SCSF represents the maximum voltage that the semiconductor withstands in steady state and V_{max} for the WCSF represents the maximum average voltage in the winding.

Finally, there are the system's and converter's efficiency. In the case of the FPC both terms are the same. However, PPC wise, since the converter processes a reduced percentage of the power that flows from the source to the load, the efficiency obtained by the system will be higher (10).

$$\eta_{system} = 1 - K_{pr} \cdot (1 - \eta_{converter}) \quad (10)$$

IV. RESULTS

Once the case studio has been introduced, the present section details the obtained results from each architecture. Firstly, Fig. 6 shows the K_{pr} curve obtained by each solution through the charging period. As it can be observed, the FPC always processes the 100% of the power provided by the source no matter the state of charge (SOC). However, when it comes to the SEPIC-PPC, as the EV charges (voltage level increases Fig. 4), the K_{pr} decreases from 80% to 5%. This is because the static voltage gain gets closer to 1.

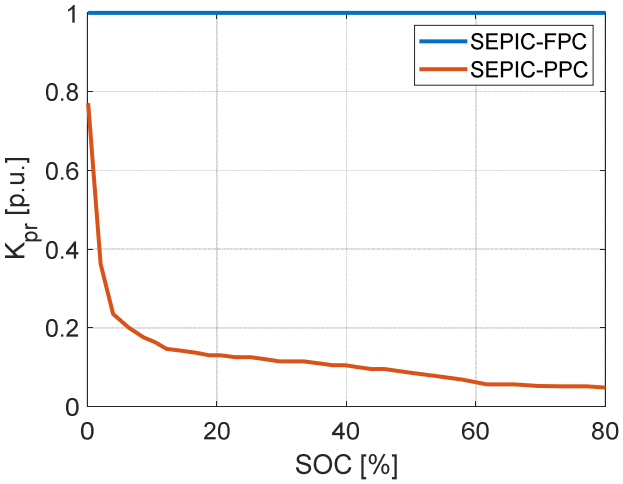
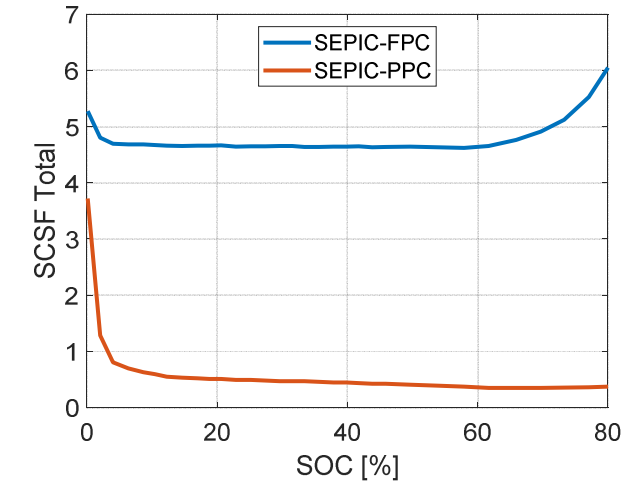


Fig. 6. Processed active power ratio of the converters.

Secondly, there is the CSF of the semiconductors and inductors (Fig. 7a and Fig. 7b, respectively). Analyzing Fig. 7, it can be concluded that the PPC solution achieves reduced CSF values on both type of components through great part of the charging process. This can lead to a lower converter rating, reduced size and cheaper solution. When it comes to the WCSF curve (Fig. 7b), the SEPIC-PPC obtains higher values than the FPC with SOC values bellow 5%. The reason of this behavior is still to be defined, however, it will not be common to start charging an EV from a such a low SOC.

Finally, Fig. 8 presents both, system's and converter's efficiency obtained by the SEPIC-FPC and the SEPIC-PPC (in case of the SEPIC-FPC, they are the same). As it is shown, the PPC obtains higher system efficiency than the FPC through all the charging period. When it comes to the converter efficiency, the one obtained by the PPC decreases as the battery charges. Indeed, at the last working points, PPC's converter efficiency is lower than the one obtained by the FPC. However, the PPC system remains more efficient than the FPC due to the reduction of the processed power by the converter. This is explained by equation (10).



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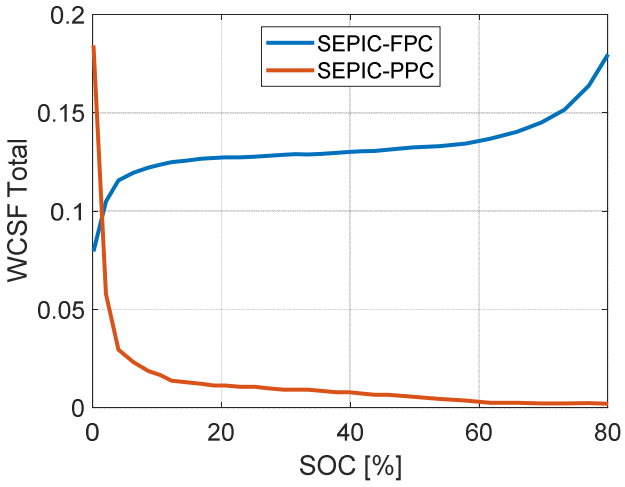

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Fig. 7. Component stress factor. A) SCSF. B) WCSF.

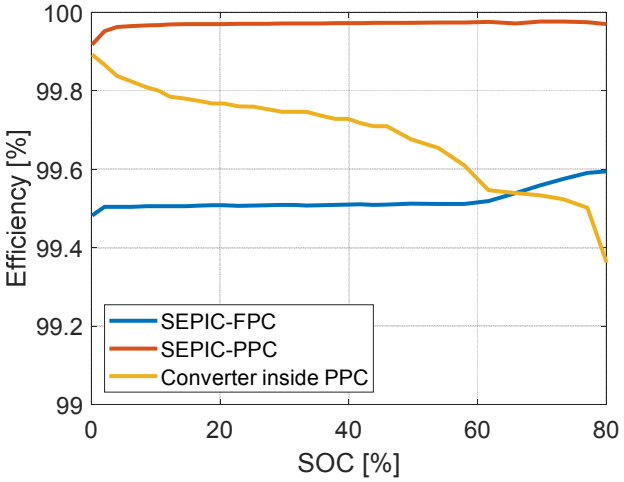

Fig. 8. Efficiency obtained by the architectures from Fig. 5.

V. CONCLUSIONS

This paper presents the benefits of using a non-isolated FC type PPC for EV fast charging applications. In first place, the main advantage of this type of architectures is that an isolated topology is not required for the conversion stage, which simplifies the design of the circuit. Then, apart from the fact that the processed power ratio by the FC type PPC is reduced between a 20% and 95%, the CSF of the semiconductors and inductors is also reduced through great part of the charging period. Furthermore, considering that the great majority of the EVs will reach the charging station with SOC values higher than a 5%, the processed power ratio by the FC type PPC would be at least an 80% lower than the FPC. Finally, when it comes to the efficiency, it is concluded that due to the reduction of the processed power by the converter, the efficiency of the system is improved, and, in consequence, cheaper power converters can be applied on FC type PPC architectures without compromising system's efficiency.

VI. FUTURE LINES

With the aim of improving the present paper, the next future lines are proposed:

- Build a small-scale prototype that confirms the obtained conclusions.
- Extend the analysis to other non-isolated topologies.

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