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PARTIAL POWER CONVERTERS FOR DC-DC APPLICATIONS

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PhD Student: JON ANZOLA GARCÍA

Supervisor: IOSU AIZPURU LARRAÑAGA

Mondragon Goi Eskola Politeknikoa

Mondragon Unibertsitatea

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ABSTRACT

This thesis studies partial power processing (PPP) based architectures for DC-DC applications. This type of solutions aim to reduce the power processed by the power converter. This way, the power losses and the volume of the power converter is reduced.

The work starts with an overview on the PPP strategies. In this sense, the different solutions found in the literature are classified into three main strategies: differential power converters, partial power converters (PPC) and mixed strategies. Due to their numerous applications and high efficiency results, the thesis focuses on the PPC architectures.

PPC architectures are divided into two groups: input-parallel-output-series (IPOS) or input-series-output-parallel (ISOP) type architectures, and fractional charging converters (FCC) type architectures. The main difference between the IPOS-ISOP type architectures and the FCC is the fact that the former requires isolated topologies. This thesis analyses the benefits that both type of architectures bring in comparison to conventional full power converter architectures. Simulations and experimental results conclude that IPOS-ISOP type architectures are the most promising solution in terms of volume reduction, high efficiency and low cost. Then, three applications of IPOS-ISOP type PPC architectures are studied for future implementation: electric vessel, hydrogen generation and electric vehicle (EV) fast charging.

Finally, a 50 kW PPC is designed and validated for EV charging. The converter consists of a dual active bridge and, due to the PPC configuration, it processes a maximum power of 5 kW. This way, the implementation of Silicon-based discrete devices is enabled. The converter achieves a peak efficiency of 99.47 %.

LABURPENA

Tesi honek DC-DC aplikazioetarako potentziaren prozesamendu partzialean (partial power processing, PPP) oinarritutako arkitekturak aztertzen ditu. Horrelako arkitekturen helburua potentzia-bihurgailuak prozesatutako potentzia murriztea da. Horrela, bihurgailuaren potentzia-galerak eta bolumena murrizten dira.

Lana PPP estrategiei buruzko ikuspegi orokor batekin hasten da. Alde horretatik, literaturan aurkitutako soluzioak hiru estrategia nagusitan sailkatzen dira: potentzia diferentzialeko bihurgailuak, potentzia partzialeko bihurgailuak (partial power converter PPC) eta estrategia mistoak. Bere aplikazio ugariengatik eta efizientzia handiko emaitzengatik, tesia PPC arkitekturetan zentratzen da.

PPC arkitekturak bi multzotan banatzen dira: sarrera-paralelo-irteera-seriea motako (input-parallel-output-series, IPOS) edo sarrera-serie-irteera-paraleloa (input-serie-output-parallel, ISOP) motako arkitekturak, eta karga zatikatuko bihurgailu motako arkitekturak (fractional charging converter, FCC). IPOS-ISOP motako arkitekturen eta FCC arkitekturen arteko desberdintasun nagusia da lehenengoek topologia isolatuak behar dituztela. Tesi honetan, bi arkitektura motek potentzia osoko bihurgailuen arkitektura konbentzionalekin alderatuta ematen dituzten abantailak aztertzen dira. Simulazioen eta emaitza esperimentalen arabera, IPOS-ISOP motako arkitekturak dira irtenbiderik oparoena bolumen-murrizketari, efizientzia handiari eta kostu txikiari dagokienez. Ondoren, IPOS-ISOP motako PPC arkitekturen hiru aplikazio aztertzen dira, etorkizunean inplementatzeko: ontzi elektrikoa, hidrogenoa sortzea eta ibilgailu elektrikoen karga azkarra.

Azkenik, 50 kW-eko PPC bat diseinatu eta baliozkotzen da ibilgailu elektrikoa kargatzeko. Bihurgailua zubi aktibo bikoitz bat da eta, PPCaren konfigurazioa dela eta, 5 kW-ko potentzia maximoa prozesatzen du. Horrela, Silizion oinarritutako gailu diskretuak inplementatzeko aukera ematen da. Bihurgailuak % 99.47-ko gehieneko efizientzia lortzen du.

RESUMEN

Esta tesis estudia las arquitecturas basadas en el procesamiento parcial de potencia (partial power processing, PPP) para aplicaciones DC-DC. Este tipo de soluciones tienen como objetivo reducir la potencia procesada por el convertidor de potencia. De este modo, se reducen las pérdidas de potencia y el volumen del convertidor.

El trabajo comienza con una revisión de las estrategias PPP. En este sentido, las diferentes soluciones encontradas en la literatura se clasifican en tres estrategias principales: convertidores de potencia diferencial, convertidores de potencia parcial (partial power converter, PPC) y estrategias mixtas. Debido a sus numerosas aplicaciones y a los resultados de alta eficiencia, la tesis se centra en las arquitecturas PPC.

Las arquitecturas PPC se dividen en dos grupos: arquitecturas del tipo entrada-serie-salida-series (input-parallel-output-series, IPOS) o entrada-serie-salida-paralelo (input-series-output-parallel, ISOP), y arquitecturas de tipo convertidores de carga fraccionada (fractional charging converter, FCC). La principal diferencia entre las arquitecturas de tipo IPOS-ISOP y las FCC es el hecho de que las primeras requieren topologías aisladas. En esta tesis se analizan las ventajas que aportan ambos tipos de arquitecturas en comparación con las arquitecturas convencionales de convertidores de potencia completa. Las simulaciones y los resultados experimentales concluyen que las arquitecturas de tipo IPOS-ISOP son la solución más prometedora en términos de reducción de volumen, alta eficiencia y bajo coste. Después, se estudian tres aplicaciones de las arquitecturas PPC de tipo IPOS-ISOP para su futura implementación: buque eléctrico, generación de hidrógeno y carga rápida de vehículos eléctricos (VE).

Por último, se diseña y valida un PPC de 50 kW para la carga de VE. El convertidor consiste en un puente activo doble y, debido a la configuración del PPC, procesa una potencia máxima de 5 kW. De este modo, se permite la implementación de dispositivos discretos basados en Silicio. El convertidor alcanza una eficiencia máxima del 99.47 %.

CONTENTS

GLOSSARY OF ABBREVIATIONS AND VARIABLES

Abbreviations

AC	Alternating current
B2E	Bus to element
BOL	Beginning of life
CAN	Controller area network
CC	Constant current
CCM	Continuous conduction mode
CCSF	Capacitor component stress factor
CSF	Component stress factor
CSIFB	Current source isolated full bridge
DAB	Dual active bridge
DC	Direct current
DFIG	Doubly-fed induction generator
DPC	Differential power converter
E2E	Element to element
EMI	Electromagnetic interference
EOL	End of life
ESR	Equivalent series resistance
ESS	Energy storage system
EV	Electric vehicle
FCC	Fractional charging converter
FPP	Full power processing
FPC	Full power converter
GaN	Gallium nitride
HB	Half bridge
HE	High energy
HESS	Hybrid energy storage system
HP	High power
iZVS	Incomplete zero voltage switching
IEEE	Institute of electrical and electronic engineers
IGBT	Insulated-gate bipolar transistor
IHB	Interleaved half bridge
IMS	Insulated metal substrate

IPOS	Input-parallel-output-series
ISOP	Input-series-output-parallel
LED	Light emitting diode
LFP	Lithium-iron-phosphate
LMO	Lithium-manganese-oxide
MGEP	Mondragon goi eskola politeknikoa
MOSFET	Metal-oxide-semiconductor field-effect-transistor
MPPT	Maximum power point tracking
MSIBC	Modified switched inductor boost converter
NaN	Not a number
NMC	Nickel-manganese-cobalt
OBC	On-board charger
OCV	Open-circuit voltage
PCB	Printed circuit board
PPC	Partial power converter
PPP	Partial power processing
PSFB	Phase shifted full bridge
PSM	Phase shift modulation
PV	Photovoltaic
RMS	Root mean square
SAE	Society of automotive engineers
SCBU	Series converter boost unit
SCSF	Semiconductor component stress factor
SEABAT	Solutions for large batteries for waterborne transport
SOC	State of charge
SiC	Silicon carbide
TIM	Thermal interface material
USB	Universal serial bus
VA	Voltage-ampere
WCSF	Winding component stress factor
ZVS	Zero voltage switching

Symbols and variables

A	Area [m^2]
C	Capacitance [F]
D	Duty
d	Phase-shift
E	Energy [Wh]

ESR	Equivalent series resistance [Ω]
I	Current [A]
L	Inductance [H]
N	Non-active power [VAr]
n	Transformation ratio of the transformer
η	Efficiency [%]
P	Active power [W]
Q	Switching device
R	Resistance [Ω]
t	Time [s]
V	Voltage [V]
ϕ	Phase-shift [deg]

Subscripts

C_{in}	Input capacitor [F]
C_{out}	Output capacitor [F]
$E_{charged}$	Energy charged [Wh]
E_{loss}	Energy losses [Wh]
E_{off}	Turn-off energy losses [Wh]
E_{on}	Turn-on energy losses [Wh]
E_{oss}	Output capacitance energy [J]
f_{sw}	Switching frequency [Hz]
G_V	Static voltage gain [p.u.]
I_0	Switching current [A]
I_{base}	Base current [A]
I_{DC}	DC current [A]
I_{in}	Converter input current [A]
I_L	Inductor current [A]
I_{load}	Load current [A]
I_{out}	Converter output current [A]
I_{RMS}	RMS current [A]
I_{source}	Source current [A]
k	Thermal conductivity [W/m·K]
K_{pr}	Partial power ratio
L_{lk}	Leakage inductance [H]
n_{cell_m}	Number of series connected cells per module
n_s	Number of series connected modules
N_C	Non-active power processed by the capacitor [VAr]

N_{in}	Non-active power at the input terminals of the converter [VAr]
N_{int}	Non-active power internally processed by the converter [VAr]
N_L	Non-active power processed by the inductor [VAr]
N_{out}	Non-active power at the output terminals of the converter [VAr]
N_p	Number of turns in the primary side winding
N_s	Number of turns in the secondary side winding
N_{st}	Number of strands
N_t	Number of turns of an inductor
N_w	Number of wires
η_{sys}	System efficiency [%]
η_{conv}	Converter efficiency [%]
P_{cond}	Conduction losses [W]
P_{cond}	Converter power [W]
P_E	Perimeter of EE type core [m]
P_{EV}	Electric vehicle power [W]
P_{in}	Converter input power [W]
P_{load}	Load power [W]
P_{loss}	Power losses [W]
P_{oss}	Output capacitance power [W]
P_{out}	Converter output power [W]
P_{rr}	Reverse recovery power [W]
P_{source}	Source power [W]
P_{sw}	Switching losses [W]
P_{sys}	System power [W]
P_{VI}	Overlapping power [W]
Q_{oss}	Output capacitance charge [C]
Q_{rr}	Reverse recovery charge [C]
R_{CE}	Collector-emitter resistance [Ω]
R_{DS}	On-state resistance of a MOSFET [Ω]
R_{SD}	Body diode resistance [Ω]
R_{th}	Thermal resistance [ºC/W]
t_{db}	Dead-band time [s]
t_{fv}	Voltage falling time [s]
t_{iZVS}	ZVS time [s]
t_{ri}	Current rising time [s]
T_{amb}	Ambient temperature [ºC]
T_H	Heatsink temperature [ºC]
T_j	Junction temperature [ºC]
T_s	Period [s]

T_{ss}	Time-step [s]
V_0	Switching voltage [V]
V_{base}	Base voltage [V]
V_{bat}	Battery voltage [V]
$V_{CE_{sat}}$	Collector-emitter saturation voltage [V]
$V_{CE_{test}}$	Test voltage [V]
V_{cell}	Battery cell voltage [V]
V_{DC}	DC voltage [V]
V_{DS}	Drain to source voltage [V]
V_E	Series connected element voltage [V]
V_{EV}	Electric vehicle voltage [V]
V_F	Forward voltage of the diode [V]
V_{in}	Converter input voltage [V]
V_{load}	Load voltage [V]
V_{mod}	Module voltage [V]
V_{out}	Converter output voltage [V]
V_{pk}	Peak voltage [V]
V_{pl}	Plateau voltage [V]
V_{RMS}	RMS voltage [V]
V_{sd}	Source to drain voltage [V]
V_{source}	Source voltage [V]
V_{th}	Thevenin voltage [V]

Chapter 1

INTRODUCTION

This Chapter introduces the research work with a brief description of the current energy transition plan and the role of power converters inside the electric system. Regarding power converters, these are classified according to its current/voltage waveforms and partial power processing is suggested for improving their efficiency and reducing their size. Together with this, the main concepts and terminology related to partial power processing are described. Finally, an overview of the most important applications where partial power processing strategies have potential benefits is carried out.

1.1 Background

Nowadays, climate change is one of the main challenges for society. Proof of this is the statement issued by the Group of 20 (G20) during the G20 summit in Rome [1]. For the first time, the leaders acknowledged officially that its members' emissions reduction plans needed to be firmed up over this decade to put them on track for net zero by 2050.

In order to achieve this objective, the document states necessary to design an energy transition plan towards to sustainable energy. This implies radical structural changes in today's energy system, for example: distributed generation, transition to renewable energy and more electric transportation (train, aircraft or electric vehicle, EV). Renewables are expected to account for 90 % of total global power capacity increases in 2022 [2] and the emergence of the EV through the last 3 years is unquestionable [3]. Still, it is important to highlight the importance of public administrations to promote renewable energy production and develop energy efficiency plans.

Regarding energy efficiency, this can be defined as the reduction of the amount of energy required to provide products and services. It is estimated that the consumed energy only consists of a 33 % of the total energy produced [5], which means that more energy is wasted than used. Over the last 40 years, massive generation and consumption points have been built to meet society's energy needs. Fig. 1.1 shows the increment of the

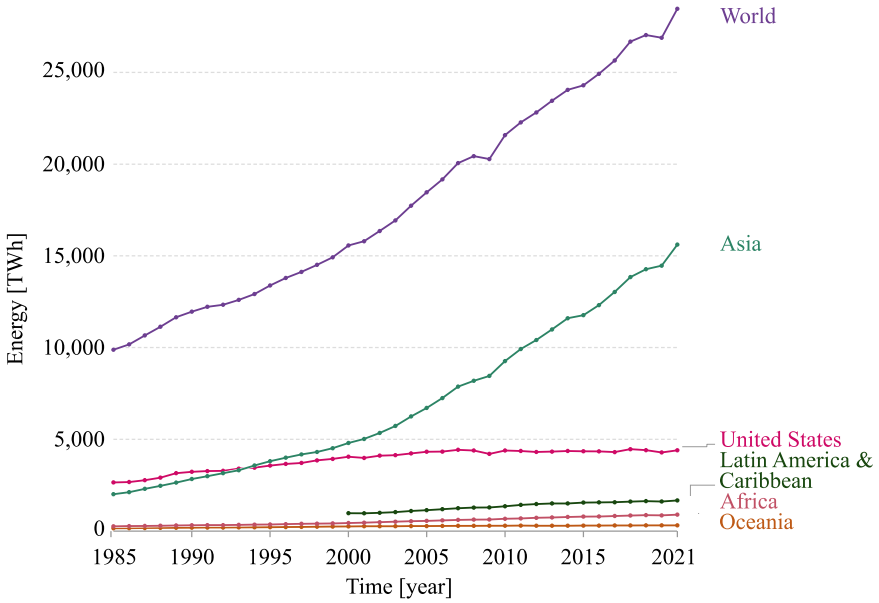


Fig. 1.1. Electricity generation evolution since 1985 [4].

electricity generation since 1985. As it can be observed, the world energy generation is constantly growing, especially due to the Asian continent. Inside the energy generation, renewables sources are gaining more importance. Indeed, in 2018, renewable sources produced the 28 % of global electricity, and they will provide 49 % by 2050 (Fig. 1.2).

On the other hand, there also exist large consumption points, such as, EV fast charging stations (few MW [7]) and data centers (hundreds of MW [8], [9]). Due to its efficient performance and reduced green-house emissions, the EV is turning into a real alternative to conventional combustion based vehicles. Authors from [10] expect a total charging energy demand increment from roughly 20 billion kWh to about 280 billion kWh for 2030 (Fig. 1.3a). Regarding data centers, they accounted for 1.1 % to 1.5 % of worldwide electricity consumption in 2010 [11] and they will use around 3 % to 13 % of global electricity in 2030 [12] (Fig. 1.3b). Considering all this, energy efficiency has turned into a great concern when it comes to the installation of these massive facilities. A slight efficiency improvement of 1 % in any of them can lead to a reduction in power losses of tens of MW.

From its production to its consumption, the electrical energy is transported and converted several times (Fig. 1.4). In each of these steps, a certain amount of power losses is produced: generation losses, conversion losses, transportation losses and consumption losses. Focusing on the conversion losses, these are related to the energy transformations performed by a combination of passive (power transformers) and active (power converters) devices. The aim of both is to transfer electric power between two points with

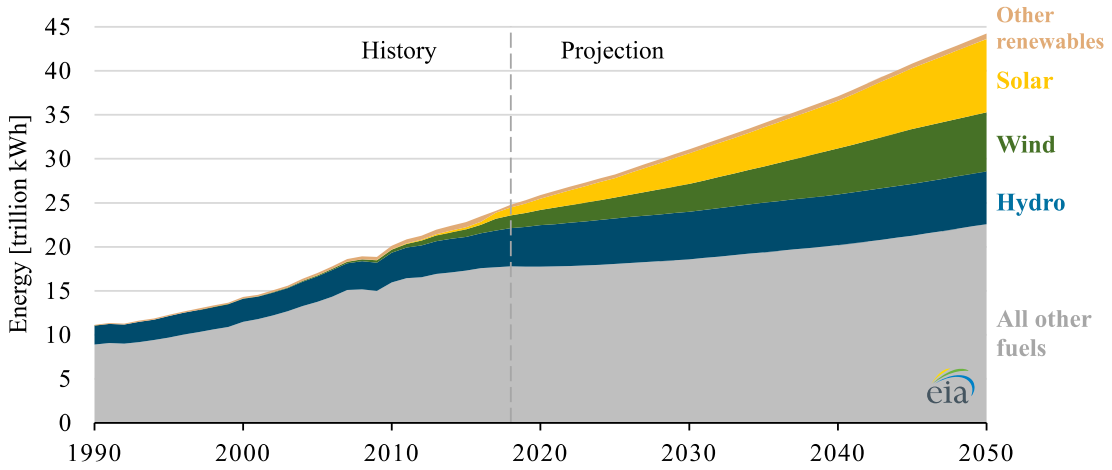


Fig. 1.2. World net electricity generation [6].

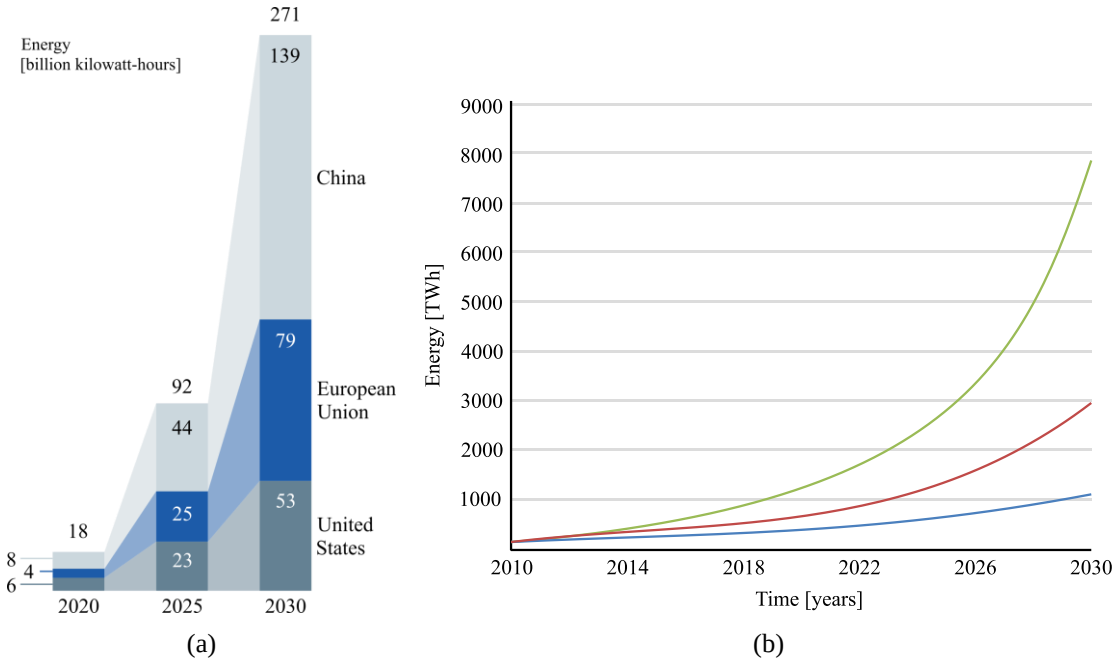


Fig. 1.3. Large consumption applications usage. (a) Expected EV energy demand for 2025 and 2030 [10]. (b) Global electricity demand of data centers from 2010 to 2030 [12].

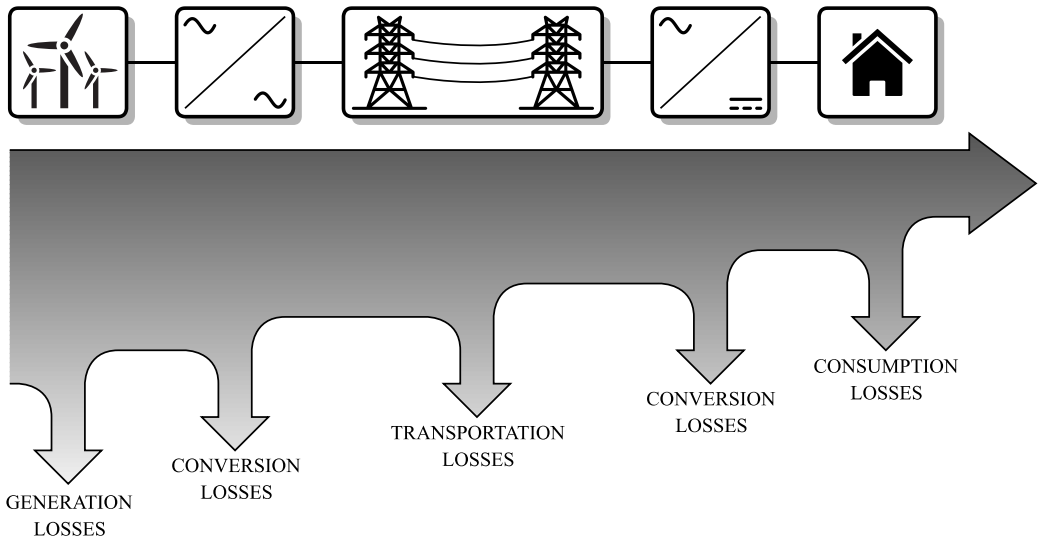


Fig. 1.4. Simplified single-wire diagram of the electric power distribution and its main power losses.

different voltage levels or waveforms. Therefore, their application extends to the entire electric grid: power drives, electronic devices supply, home appliance… Bearing this in mind, power converters are considered as a key component whose performance and efficiency must be improved for achieving a sustainable future.

1.2 Overview of Power Converters

There exist many different criteria to classify power converters: number of components, galvanic isolation, current/voltage source… But, when it comes to the current's waveform, there exist 3 types of power converters: (i) DC-AC or AC-DC, (ii) AC-AC and (iii) DC-DC.

First, a DC-AC (power inverter, Fig. 1.5a) or an AC-DC (power rectifier, Fig. 1.5b) is implemented on applications where it is required to change from direct current to alternating current or vice versa. Inverters have as input a constant voltage or current and by switching a series of semiconductors, they are capable of generating at the output an AC signal. Rectifiers aim to transform a periodically reversing current into a unidirectional flow.

Second, there are the AC-AC converters, which convert a source of alternating current from one voltage level and/or frequency to another (Fig. 1.5c). The simplest example is the power transformer, which can be considered as a passive AC-AC converter capable of elevating or reducing the voltage. Also, there exist AC-AC solutions were a rectifier and an inverter are connected in series with a DC bus in between.

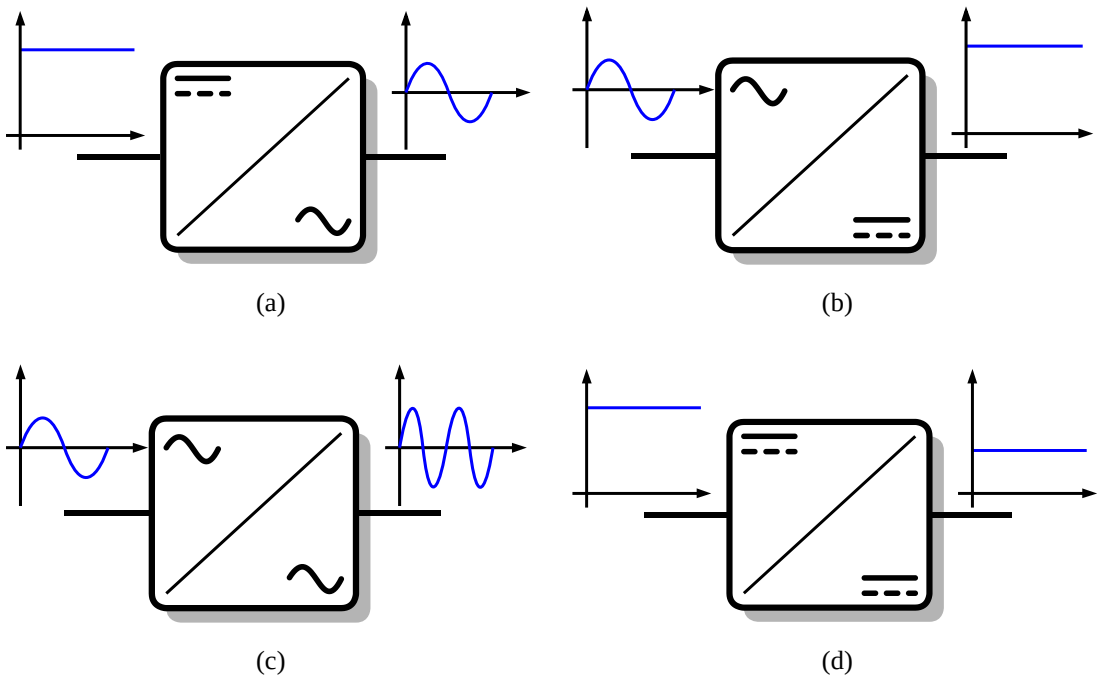


Fig. 1.5. Simplified single-wire diagram of a (a) DC-AC. (b) AC-DC. (c) AC-AC. (d) DC-DC.

Finally, there are the DC-DC converters, which transform a source of direct current from one voltage level to another (Fig. 1.5d). Similar to AC-AC converters, a DC-DC can be compound by an inverter and a rectifier with a high frequency transformer in between. This type of solutions are known as isolated topologies and they provide galvanic isolation to the system where they are applied. The galvanic isolation refers to the fact that the output and input power circuits are electrically and physically isolated between them [13]. This can be effective to prevent from current flow between two circuits with different potential.

1.3 Efficiency Improvement Trends

Power conversion is considered as a key sector inside the energy transition and, hence, great efforts are being made to improve the performance of power converters. These are divided in two main groups: component level and system level (Fig. 1.6). Inside the component level, improvements related to specific devices are included. These devices can be active or passive. On the other hand, the system level comprehends advanced or novel converter topologies and architectures.

Regarding active components, there is the transition towards wide-bandgap (WBG) semiconductors. Higher energy efficiency and reduced power converter size are the main benefits that WBG devices present against conventional Silicon (Si) based semiconductors [14], [15]. Furthermore, these WBG semiconductors permit devices to operate at much higher voltages and temperatures (typical application of Silicon Carbide, SiC), and higher frequencies (typical application of Gallium Nitride, GaN) than the conventional Si semiconductors [16]. Apart from that, WBG semiconductors offer a better performance in terms of conduction and switching losses. Fig. 1.7a compares the

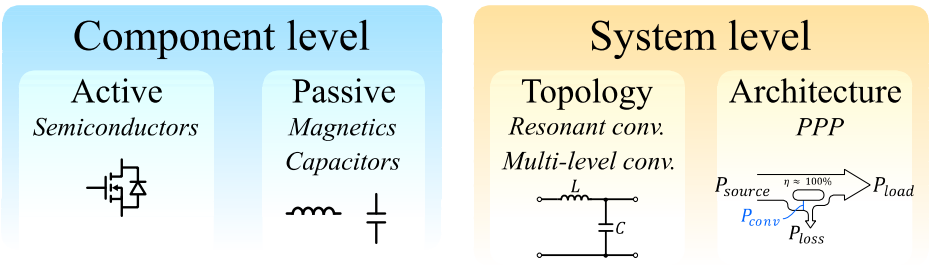
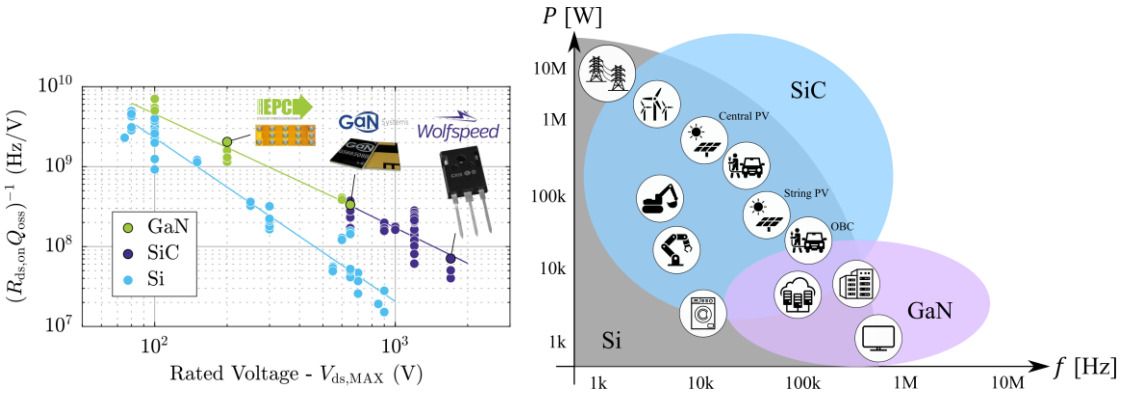


Fig. 1.6. Block diagram of the main efficiency improvement trends.



(a) (b)

Fig. 1.7. Comparison between Si and WBG devices. (a) $FoM = \frac{1}{R_{DS} \cdot Q_{oss}}$ for the majority of commercially available Si, SiC and GaN [19]. (b) Applications [20].

on-state resistance (R_{DS}, representative for conduction losses) and the charge stored in the transistor's output capacitance (Q_{oss}, representative for switching losses). As it can be observed, WBG semiconductors clearly outperform Si devices. Consequently, solar, traction, and EV applications are already implementing power converters with WBG based devices [17]. Fig. 1.7b shows the typical applications of Si and WBG semiconductors.

However, semiconductors' progress is not enough when high power density converters are required. The passive components and the cooling system inside the power converter are limiting the performance [18]. Therefore, the design of the magnetics and the capacitors has turned into an important topic to put the effort on.

System level wise, a research trend that aims to enhance the characteristics of power converters is the design of high efficient topologies. An example of this are resonant tanks that seek soft-switching conditions of the semiconductors [21], [22], and multi-level topologies that reduce the final cost of the converter by using lower voltage class devices [23], [24]. Last but not least, over the last decade, novel power delivery architectures based on partial power processing (PPP) have been presented. This type of architectures aim to reduce the power to be processed by the converter and they are considered as attractive solutions regarding power converter downsizing and efficiency improvement.

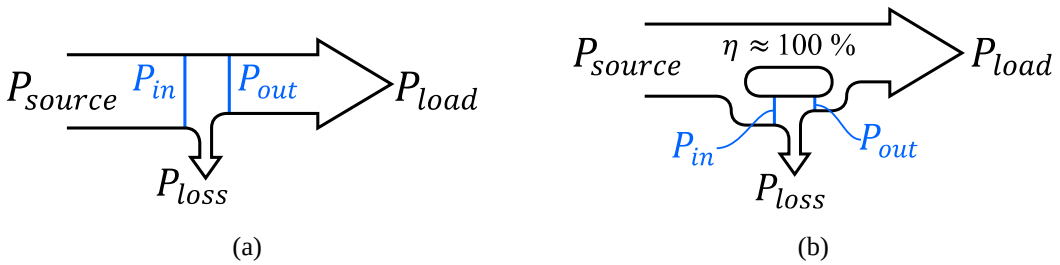
1.4 Basis of Partial Power Processing

1.4.1 Concept Description

The PPP concept was presented for the first time in spacecraft industry [25], where downsizing power converters connected to photovoltaic (PV) panels was the main priority. This way, a more efficient converter with higher power density was achieved without affecting the robustness of the system. As time passed by, this same concept was developed for further renewables applications based on wind generation [26], energy storage system (ESS) [27] and EV fast charging applications [28].

A power converter based on the PPP concept only processes a reduced percentage of the total power that goes from the source to the load. As example, Fig. 1.8 compares the power flow of a Full Power Processing (FPP) based converter and PPP-based converter. The FPP-based converter (Fig. 1.8a) is designed to process the 100 % of the power that flows from the source to the load. On the other hand, Fig. 1.8b shows the PPP concept, which is based on achieving a reduction of the power processed by the converter. In other words, the PPP-based converter processes only a fraction of the power that flows from the source to the load. This way, it is expected to implement lower rated components, reduce the power losses and achieve a smaller solution.

In the FPP case, since the system power and the converter power are the same, it is concluded that the efficiency of the system (η_{sys}) and the efficiency of the converter (η_{conv}) are identical (1.1). On the other hand, a PPP-based converter processes a reduced amount of the system power, thus their efficiencies must be treated as different parameters. However, they will be related by the processed power ratio of the converter



(a) (b)

Fig. 1.8. Power flow diagram. (a) FPP. (b) PPP.

Table 1.1. Definition of the main electrical parameters of an electric circuit.

Parameter	Meaning
V_{in}, I_{in}, P_{in}	Input voltage/current/power of the converter
V_{out}, I_{out}, P_{out}	Output voltage/current/power of the converter
V_{source}, I_{source}, P_{source}	Source voltage/current/power
V_{load}, I_{load}, P_{load}	Load voltage/current/power
η_{conv}, η_{sys}	Converter/system efficiency

(K_{pr}), which consists of the division between the converter power and the system power (1.2). The term K_{pr} will be further explained in detail.

$$\eta_{sys_{FPP}} = \frac{P_{load}}{P_{source}} = \eta_{conv} = \frac{P_{out}}{P_{in}} \quad \textbf{(1.1)}$$

$$\eta_{sys_{PPP}} = \frac{P_{load}}{P_{source}} = 1 - \frac{P_{in}}{P_{source}} \cdot (1 - \eta_{conv}) = 1 - K_{pr} \cdot (1 - \eta_{conv}) \quad \textbf{(1.2)}$$

As shown in equation (1.2), in the PPP case, it is important to differentiate the voltage, current or power characteristics of the converter and the system. Therefore, with the aim of clarifying the difference between the performance of a power converter and the performance of the whole system, Table 1.1 describes the main electrical parameters and their corresponding naming. Through the rest of the document, the terms input and output will refer to the converter. The terms source and load will refer to the system.

1.4.2 Applications of Partial Power Processing

Through the last decade, PPP based architectures have been presented as promising solutions to many different types of applications.

In the first place, there are the renewable sources applications such as, photovoltaic (PV) generation (Fig. 1.9a). In order to inject into the electrical grid the energy generated by the PV modules, two different power converters are required: a DC-DC and a DC-AC. The first one is in charge of implementing the maximum power point tracking (MPPT) at the PV module and keeping a constant voltage level of the DC bus between both converters. The second one injects to the electrical grid the produced energy at a correct phase. Authors from [29]–[31] present different PPP solutions that focus on the design of the DC-DC converter.

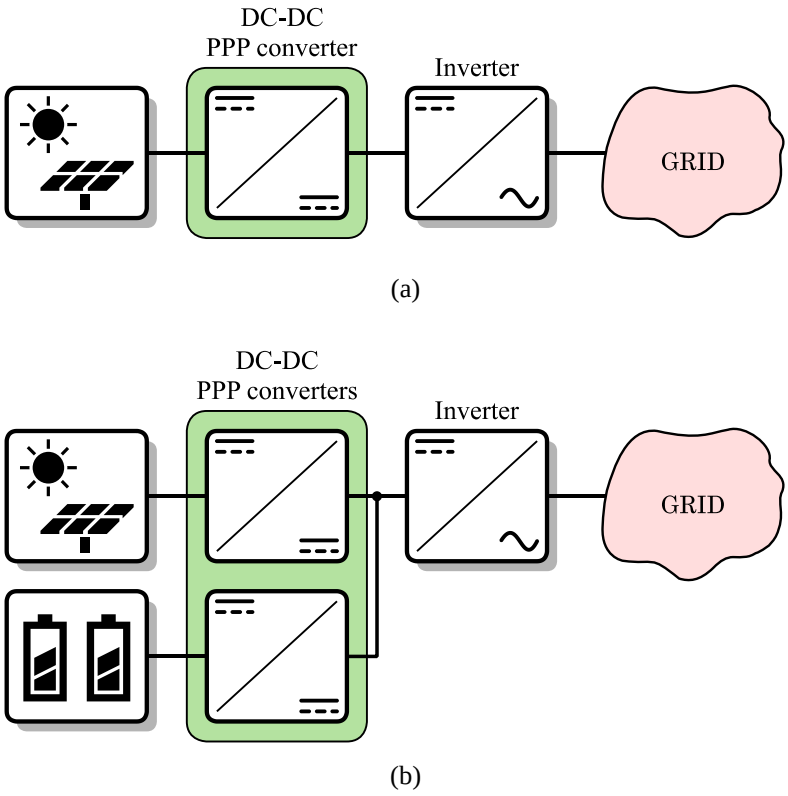


Fig. 1.9. Simplified single-wire diagram of a PV application. (a) Simple. (b) Supported with an ESS.

Related to the previous application, due to the fluctuation of PV generation, the final solution usually requires an ESS to fit the energy production and the consumption profiles (Fig. 1.9b). Actually, ESSs are considered as a key tool for achieving a flexible European power system through its transition to net zero emissions [32]. Therefore, the development of new technologies that can improve the performance of this type of applications are highly requested, for example, PPP based converters. Due to the fact that an ESS suffers both, charging and discharging processes, the concerned DC-DC converter must be capable of handling a bidirectional power flow. Through the literature, several examples with bidirectional PPP strategies can be found [27], [33].

Another interesting application of PPP inside renewable energies is its implementation on wind generation. For example, authors from [34], [35] suggest PPP based converters for a DC collection system (Fig. 1.10). In this case, it consists of a series of DC-DC converters that connect to the same DC bus. Then, a single or various inverters inject the generated energy into the grid.

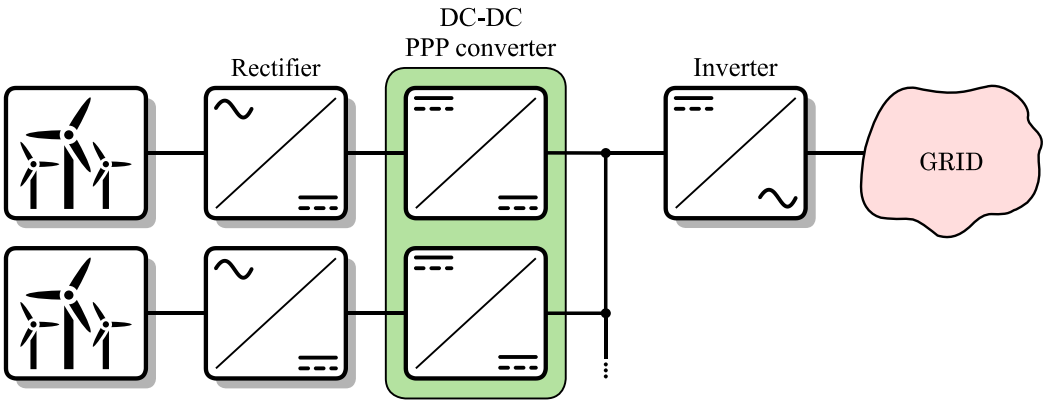


Fig. 1.10. Simplified single-wire diagram of a wind farm application.

Another sector that is showing great interest on the development of PPP based architectures is the one of the EV. Indeed, due to its efficient performance and reduced green-house emissions, the EV is turning into a real alternative to conventional combustion based vehicles. However, EVs' main disadvantage is their low autonomy, which can reach up to 550 km [36]. In addition, the lack of charging infrastructure can lead to driving range anxiety [37]. Therefore, in order to avoid this, an extensive and solid EV charging stations grid is required.

When it comes to the installation of the charging stations, one can find different types of solutions divided by their power level. On the one hand, up to 10 kW AC charging stations can be found. Usually, this type of charging structures are located where people spend great part of the day, for example: at home or at work. On the other hand, DC wise, two main groups exist: fast charging stations (between 20 kW and 120 kW) and extreme fast charging stations (higher than 120 kW). Due to the high peak power values, the charging times can be reduced up to 15 minutes, which makes the EV more attractive to the customer. Regarding fast charging stations, they are structures that are divided in different phases [38] (Fig. 1.11). Usually, fast charging stations are connected to a medium voltage AC grid and, then, the voltage level is reduced and rectified. Finally, several DC-DC power converters are implemented to charge each EV at the station. Concerning the DC-DC converter, several authors from the literature suggest to implement PPP based converters [28], [39], [40].

Another application of PPP inside the EV is the power drive, which is located between the ESS and the inverter connected to the motor (Fig. 1.12). In this case, since it

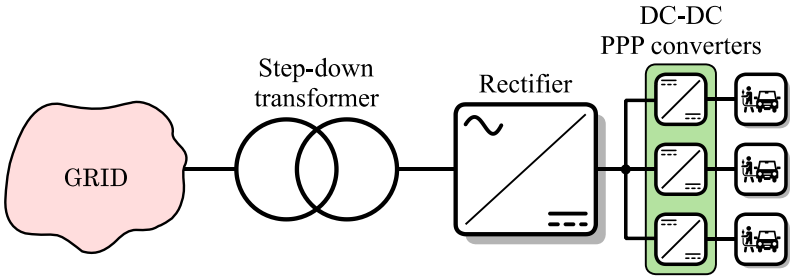


Fig. 1.11. Simplified single-wire diagram of EV fast charging station.

exists a power flow towards and from the ESS (acceleration or brake), the concerned converter must be bidirectional. At present, there are not publications that propose or mention specific PPP solutions for this type of applications. But, regarding the benefits that PPP offers (reduced sized converter and lower rated components), it is obvious that this type of technology suits very well in an EV's power drive application.

Apart from the power drive of the EV, PPP architectures can also be applied for supplying the car headlights (Fig. 1.13.) The great majority of the headlights implemented on vehicles are based on light emitting diodes (LED) technology. Through the literature, there can be found examples of PPP solutions for LED current balancing. Authors from [41] comment that the voltage-current characteristic of the LEDs is not always the same, specially when a failure occurs. Therefore, when LED strings are connected in parallel, the illumination is not uniform if the same voltage is applied to all strings. In consequence,

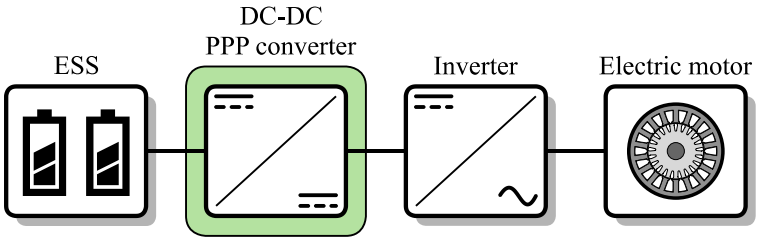


Fig. 1.12. Simplified single-wire diagram of the power drive of an EV.

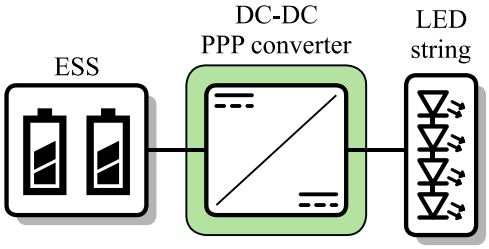


Fig. 1.13. Simplified single-wire diagram of a LED string supply.

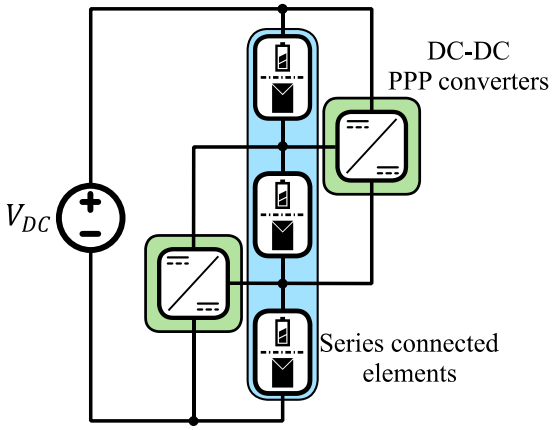


Fig. 1.14. Simplified electric circuit of a current balancing application.

PPP architectures are implemented to correct the concerned unbalance with reduced processed power.

Additionally, authors from [42]–[45] propose PPP techniques for current balancing purposes of series connected elements, for example: PV modules or individual cells inside a whole energy storage pack (Fig. 1.14). The main objective of this type of solutions is to optimize the individual performance of an element inside a series string. In order to achieve it, these current diverters are designed to process the mentioned imbalance, and not the total power consumed/supplied by the sum of the elements.

Until this point, only DC-DC converters have been considered as possible PPP applications. However, there also exists literature around power inverters that are based on PPP strategies [46]–[48]. Some of these solutions were motivated by Google's "little box challenge" [49], which was launched together with the Institute of Electrical and Electronic Engineers (IEEE) in 2014. The challenge required to build a power inverter that was about one-tenth the size of the state of the art at the time (6.5 dm^3). In addition, it had to have an efficiency greater than 95 % and handle loads of 2 kW. This lead to multiple strategies, in which PPP was one of them. As example, Fig. 1.15 presents a high-level schematic of the proposed solution in [46]. There, a "buffer architecture is proposed for power pulsation decoupling in power conversion between DC and single phase AC".

In conclusion, the literature proves that PPP strategies offer a wide variety of applications.

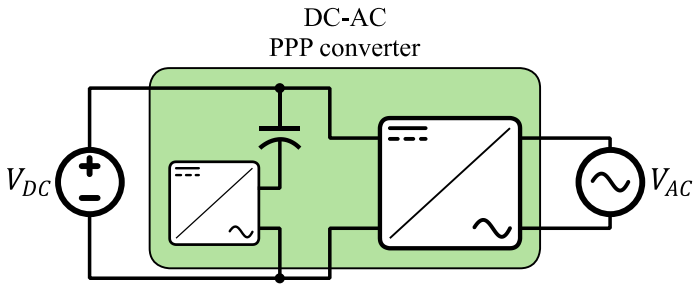


Fig. 1.15. Simplified electric circuit of a PPP based DC-AC application.

1.5 Objectives and New Contributions of the Work

The main objective of this work is to improve the performance of the DC-DC converter through PPP. Bearing this in mind, the sub-objectives are set to:

- Tackle the challenges and drawbacks of PPP-based converters.
- Demonstrate the benefits that PPP-based converters bring compared to conventional FPP solutions.

The new contributions of this work are:

- Review of the PPP literature and classification of the different strategies.
- Demystifying the application of DC-DC non-isolated topologies on partial power architectures.
- Demonstrate that the Si-based PPP converter has improved performance than SiC-based FPP converter in all metrics: thermal stress, efficiency, volume and cost.
- Design and assembly of a 50 kW DC-DC converter based on PPP.

Different parts of this thesis including texts, tables, figures and equations have been previously published in scientific international journals and conference proceedings. The publications are listed in the following:

Conference papers

[C1] J. Anzola, I. Aizpuru, and A. Arruti, "*Non-Isolated Partial Power Converter for Electric Vehicle Fast Charging Stations*," 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG) 2020.

[C2] J. Anzola et al., "*Partial power processing based charging unit for electric vehicle extreme fast charging stations*," 2020 IEEE Vehicle Power Propulsion Conference (VPPC) 2020.

[C3] J. Anzola et al., "*Resonant Dual Active Bridge Partial Power Converter for Electric Vehicle Fast Charging Stations*," 2021 IEEE Vehicle Power and Propulsion Conference (VPPC) 2021.

[C4] J. Anzola, S. Sharma, I. Aizpuru, and S. Bhattacharya, "*Silicon Application Extension Versus WBG Due to Partial Power Processing*," 2022 IEEE Applied Power Electronics Conference (APEC) 2022.

[C5] J. S. Artal-Sevil, C. Bernal-Ruiz, J. Anzola, I. Aizpuru, A. Bono-Nuez, and J. M. Sanz-Alcaine, "*Partial power processing architecture applied to a battery energy storage system*," 2020 IEEE Vehicle Power Propulsion Conference (VPPC) 2020.

[C6] J. S. Artal-Sevil, V. Ballestín-Bernard, J. Anzola, and J.A. Domínguez-Navarro, "*High-Gain Non-isolated DC-DC Partial-Power Converter for Automotive Applications*," 2021 IEEE Vehicle Power Propulsion Conference (VPPC) 2021.

[C7] J. S. Artal-Sevil, J. Anzola, V. Ballestín-Bernad, and J.L. Bernal- Agustín, "*Analysis and Implementation of different non-isolated Partial-Power Processing Architectures based on the Cuk Converter*," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe) 2022.

[C8] J. S. Artal-Sevil , J. Anzola, V. Ballestín-Bernad, and I. Aizpuru, "*Bidirectional Cuk Converter in Partial-Power Architecture with Current Mode Control for Battery Energy Storage System in Electric Vehicles*," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe) 2022.

Other contributions out of the thesis:

[C9] J. Anzola, I. Aizpuru, and A. Arruti, "*Development of an Algorithm for the Automation of the Modelling Process of Power Converters*," 2020 22nd European Conference on Power Electronics (EPE'20 ECCE Europe) 2020.

[C10] A. Aizpuru, A. Arruti, J. Anzola, U. Iraola, M. Mazuela, and A. Rujas, "*Universal electric vehicle charging infrastructure analysis tool*," 2020 IEEE Vehicle Power Propulsion Conference (VPPC) 2020.

[C11] A. Arruti, F. J. Perez-Cebolla. J. Anzola, I. Aizpuru, and M. Mazuela, "*Analytical, FEM and Experimental Study of the Influence of the Airgap Size in Different Types of Ferrite Cores*," 2022 24nd European Conference on Power Electronics (EPE'20 ECCE Europe) 2022.

Journal papers

[J1] J. Anzola et al., "*Review of Architectures Based on Partial Power Processing for DC-DC Applications*," IEEE Access, vol. 8, pp. 103405–103418, 2020.

[J2] J. Anzola, I. Aizpuru, and A. Arruti, "*Partial power processing based converter for electric vehicle fast charging stations*," Electronics, vol. 10, no. 3, pp. 1–17, 2021.

[J3] J. Anzola, I. Aizpuru, A. Arruti, J. S. Artal-Sevil, and C. Bernal-Ruiz, "*Demystifying non-isolated DC-DC topologies on partial power processing architectures*," Electronics, vol. 11, no. 3, p. 480, 2022.

[J4] J. Anzola, S. Sharma, I. Aizpuru, S. Bhattacharya, J. S. Artal-Sevil, "*Performance Improvement of a Silicon Partial Power Converter over a Silicon Carbide Full Power Converter*" **Under revision in Transactions on Transportation Electrification**

[J5] J. Anzola, E. Garayalde, J. Urkizu, A. Alacano, R. Lopez-erauskin, "*High Efficiency Converters based on Modular Partial Power Processing for Fully Electric Maritime Applications*" **Under revision in Energy Reports**

1.6 Chapter Overview

Fig. 1.16 describes the structure of the thesis, gathering the different Chapters according to the part of the work they represent:

Chapter 1 introduces power converters by describing their role inside the electric grid, the different types that exist and advanced solutions that improve their performance. One of the suggested solutions is PPP, which is the main topic of this document.

Chapter 2 reviews the literature on PPP, classifies the different strategies according to their characteristics and explains their working principles. Then, their main drawbacks and challenges are detailed. At the end of the Chapter, the comparison parameters that are considered for converters analysis are defined.

Chapter 3 discusses the possibility of achieving partial power processing with non-isolated DC-DC topologies. The results from simulations and experimental tests conclude that single inductor non-isolated topologies cannot achieve partial power processing. However, double inductor non-isolated topology can improve its efficiency with PPP-based architectures.

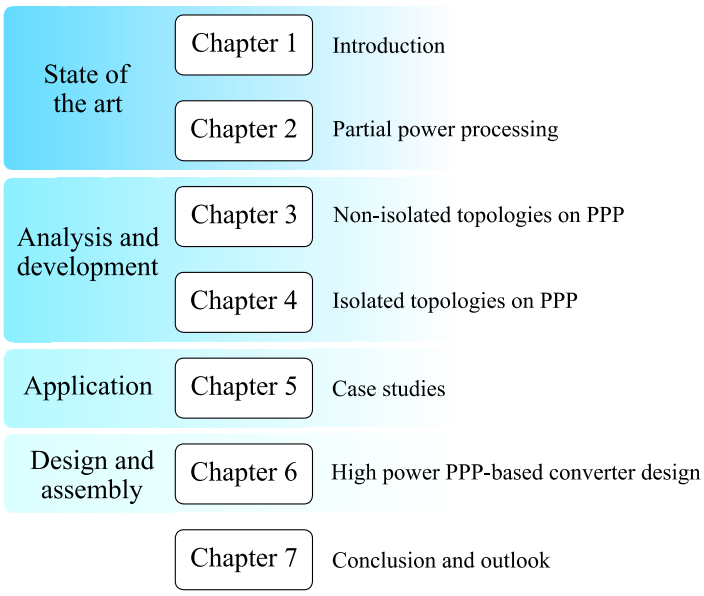


Fig. 1.16. Structure of the thesis Chapters.

Chapter 4 compares the performance of a conventional FPP-based and a PPP-based converter. The comparison focuses on the switching mode of the devices, their thermal stress and the system efficiency.

Chapter 5 presents three different applications where PPP-based converters are considered for implementation: electric vessel, hydrogen generation and EV charging. Each case study analyses the benefits of the PPP solution and it describes its design steps.

Chapter 6 describes the steps followed to design and assemble a 50 kW DC-DC PPP-based converter. Due to the reduced converter power, the prototype is enabled with discrete devices and efficiencies above 99 % are achieved.

Chapter 7 defines the main conclusions reached in this research project.

Chapter 2

PARTIAL POWER PROCESSING OVERVIEW

This Chapter gives an overview of the most repeated PPP strategies in the literature. With this purpose, three main strategies are identified and classified according to their characteristics: differential power converters, partial power converters (PPC) and mixed strategies. Especial interest is shown to PPCs due to their diverse literature and numerous applications. Together with this, the main disadvantages and challenges that PPP strategies present are detailed and discussed.

Finally, different factors that affect the behaviour of the converter and which will be used for converters comparison are presented.

Significant content from this Chapter corresponds to the journal article [J1].

2.1 Partial Power Processing Based Architectures

Although the first steps taken on the PPP area were in the 1990s [25], [50], the interest in this type of architectures did not began until 10 years ago. For this reason, the recent literature around PPP presents a confusing nomenclature. Indeed, identical architectures receive different names and, vice versa, the same name is used to refer to different architectures. Therefore, with the aim of setting a universal naming criteria, the present Chapter proposes to differentiate 3 main PPP strategies (Fig. 2.1):

- *Differential Power Converters (DPC):* they consist of active balancing circuits that aim to optimize the individual performance in series-connected DC voltage domains.

- *Partial power converters (PPC):* their main goal is to control the power flow between a source and a load with different voltage level.

- *Mixed strategies:* they offer a better performance at specific applications where DPC and PPC converters present considerable disadvantages.

2.1.1 Differential Power Converter

The architectures based on the DPC concept are well defined in [42] as power converters that aim to correct current imbalances that exist between different elements connected in series to the same voltage bus. In consequence, instead of processing the total power consumed/supplied by the sum of the elements, this type of converters only process the mismatch by providing the difference between the elements' current. DPCs

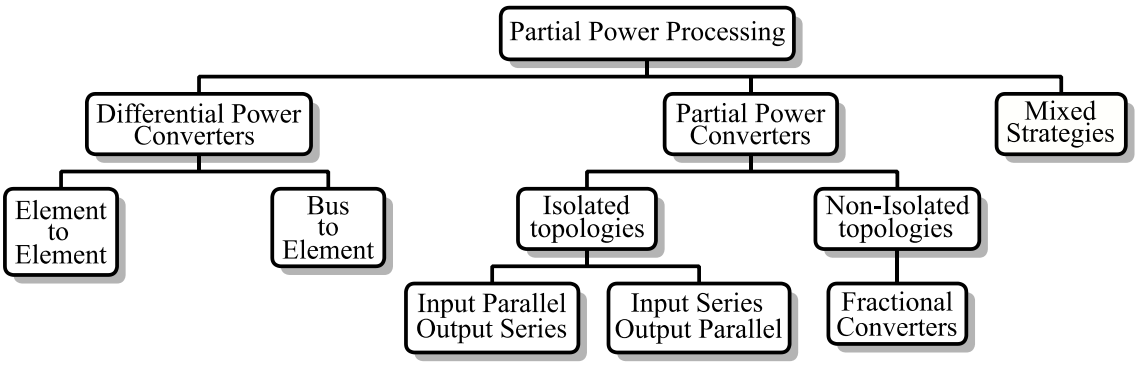


Fig. 2.1. Overview of PPP strategies.

were presented in [50]–[52] for ESS applications as a "new technique for equalizing a series battery stack". There, different active balancing solutions are proposed, such as, parallel connected Flyback modules and buck-boost current diverters. Later, the same architectures are further developed in [43], [53]–[56] by implementing improved topologies, for example: a buck-boost with shared-core inductors and a dual active bridge (DAB). In consequence, the implementation of this type of architectures is extended to PV applications with current balancing purposes [44], [45], [57]–[59] and more efficient DC power distribution of data centers [56]. The research from [60] is recommended for extended information around DPC architectures, specifically, Sections 4 and 5.

Inside the literature around DPCs, there is a considerable confusion in their naming. In the first place, authors from [51], [53] introduce the term "equalizer" or "battery system equalizer" to refer to an active balancing circuit. However, years after, authors from [44], [58], [59] started to use the terms DPC and "current diverter converter", and in [45], [57] the term "parallel-connected PPC" is used to refer to the same current balancing solution. Also, authors from [43], [54]–[56] use a different term to refer to the same architecture: "returned energy architecture", "Parallel connected submodule integrated converter", "input series output parallel" and DPC.

As it can be observed, within the active balancing literature, there is a lack of agreement on the naming criteria. Therefore, this document proposes to use the term DPC to refer to a power converter that has current balancing purposes.

Depending on the energy flow strategy, DPC architectures are divided into 2 main groups:

1. *Element to Element (E2E):* the energy is transferred between neighbouring elements.
2. *Bus to Element (B2E):* the energy is transferred from a common bus to each individual element and/or vice versa.

Element to element

In order to optimize the performance of individual series connected elements, E2E type architectures are focused on transferring the energy between neighbour elements

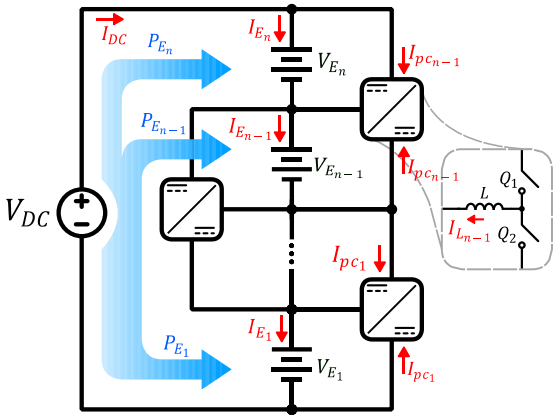


Fig. 2.2. E2E type DPC architecture with a single inductor HB topology.

[43]–[45], [51], [53], [57], [58], [61]. To explain this, Fig. 2.2, presents the current and power flows by red and blue arrows, respectively. The power delivered by the source is divided by the number of elements (n). However, the power processed by each converter is given by the current that flows through the inductor (I_{L_i}), which depends on the currents of the neighbouring elements.

The main advantages of E2E architectures are the number of necessary converters (n−1 converters for n elements) and the fact that the devices are designed for lower voltage and current values. Nevertheless, the switching states of the converters are not independent and the DC link voltage (V_{DC}) is the result of the sum of the elements connected in series. Therefore, if the application requires to raise or reduce this voltage, an additional converter would be necessary.

Focusing on Fig. 2.2, it can be seen that each power converter consists of a conventional single inductor half-bridge (HB). The total power processed by the converters (P_{E2E}) is the sum of the power processed by each one (2.1).

$$P_{E2E} = \sum_{i=1}^{n-1} V_{E_i} \cdot \left| I_{L_i} \right| \tag{2.1}$$

Where V_{E_i} is the average element voltage of the i^{th} converter and I_{L_i} is the average inductor current of the i^{th} converter.

On the other hand, by applying Kirchhoff's current law to the intermediate nodes between the series connected elements, the average inductor current value of each converter is obtained (2.2). As it can be observed, the average inductance current inside the converter depends on the currents of the adjacent elements.

$$I_{L_i} = I_{E_i} - I_{E_{i+1}} + D_{i-1} \cdot I_{L_{i-1}} + (1 - D_{i+1}) \cdot I_{L_{i+1}} \quad \textbf{(2.2)}$$

Where, I_{E_i} is the current of the i^{th} element and D_i is the duty ratio of the high side switch of the i^{th} converter.

Bus to element

B2E type architectures (Fig. 2.3) are aimed to transfer energy between an element in series and the common bus [50], [52], [54]–[56], [62]–[64]. This common bus can be a virtual bus voltage (represented as C_{bus} in Fig. 2.3a) or the same input/output bus (represented as V_{DC} in Fig. 2.3b). The main purpose of the common bus is to compensate an instantaneous power mismatch by injecting or rejecting current to the series connected elements. Compared to E2E architectures, B2E type offers greater modularity and independence between converters. However, a higher number of converters is required (n converters for n elements) and the components are designed for higher voltage and

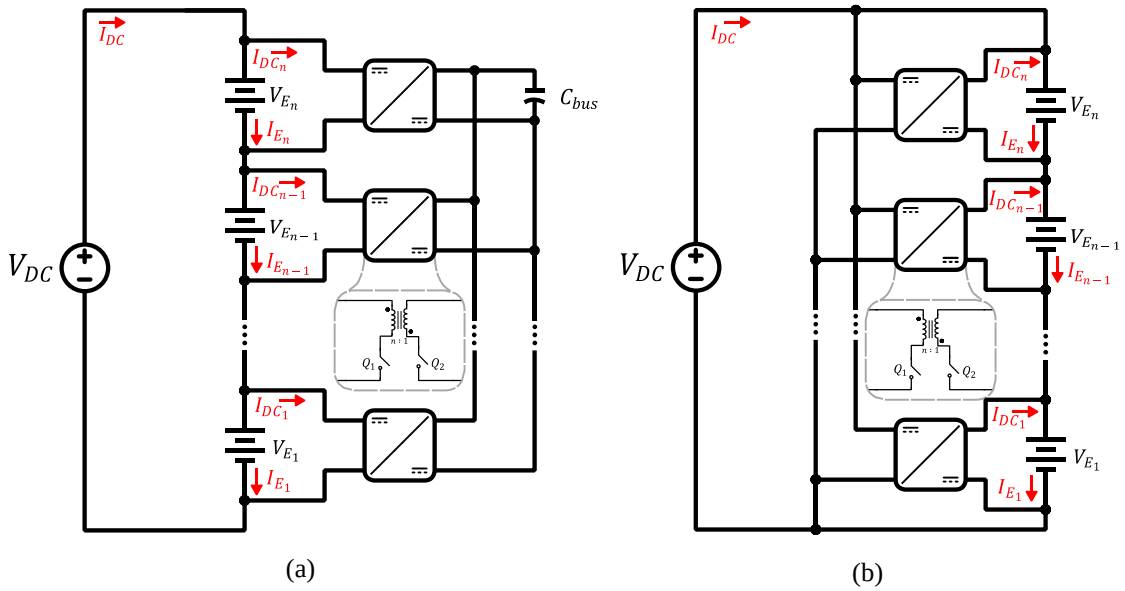


Fig. 2.3. B2E architecture with bidirectional Flyback topology. (a) Virtual bus. (b) Common bus.

current values [42], [44]. As E2E type architectures, in case it is desired to regulate the value of V_{DC}, B2E architectures also require an additional converter.

Regarding the converters' topology from Fig. 2.3, it is observed that an isolated topology is necessary to avoid a string short-circuit. In this case, a bidirectional Flyback converter is shown as example. The total power processed by the sum of each converter is given by equation (2.3).

$$P_{B2E} = \sum_{i=1}^{n} V_{E_i} \cdot \left| I_{DC_i} \right| \tag{2.3}$$

Finally, equation (2.4) shows the current that each converter must process.

$$I_{DC,i} = I_i - I_{i+1} + I_{DC,i+1} \tag{2.4}$$

Overview

With the aim of resuming the main results extracted from the DPC literature, Table 2.1 points out the key characteristics of the main articles. Since each prototype is tested under different conditions, the aim of Table 2.1 is not to compare the obtained results by each reference, but to make the reader see the goals achieved by each converter presented in the literature (together with their corresponding solutions and applications).

At first glance, it can be observed that there is no predominant architecture, both, E2E and B2E are implemented equally. However, it is clear that the main application of this type of solutions is the PV, followed by state of charge (SOC) balancing. Regarding the topologies of the converters, the most popular topology in E2E architectures is the single inductor HB and, in B2E, the Flyback. When it comes to the K_{pr}, the first references around this type of architecture do not specify this value, since it was not their main objective. The rest of the articles present K_{pr} values that go from 0 % to 66 %. This value depends on the mismatch to correct.

Table 2.1. Key parameters extracted from the literature around DPC.

Ref.	Architectures	K_{pr}	η_{sys}	Topology	Application
[50]	B2E	-	-	Flyback	ESS balancing
[51]	E2E	-	-	Single inductor HB	ESS balancing
[52]	B2E	-	-	Multi input Flyback	ESS balancing
[53]	E2E	-	-	Buck-Boost	ESS balancing
[55]	B2E	From 0 to 0.66	98 %	Flyback	PV local MPPT
[43]	E2E	-	92 %	Single inductor HB	-
[56]	B2E	-	95 %	DAB	Data center
[44]	E2E	From 0 to 0.66	95 %	Single inductor HB	PV local MPPT
[58]	E2E	From 0 to 0.5	95 %	Single inductor HB	PV local MPPT
[61]	E2E	From 0 to 0.15	-	Single inductor HB	PV local MPPT
[62]	B2E	From 0 to 0.66	97 %	Flyback	PV local MPPT
[63]	B2E	-	93.3 %	Switched capacitor	PV local MPPT
[64]	B2E	From 0 to 0.3	95 %	LLC resonant voltage multiplier	PV local MPPT
[54][1]	B2E	From 0 to 0.6	-	Flyback	PV local MPPT

2.1.2 Partial Power Converters

PPCs main goal is to control the power flow between a source and a load with different voltage level. In PPC literature, there also exists a wide variety of names to refer to the same architecture, which leads to confusion.

The first time that this type of architectures were presented, they were defined as series connected boost units (SCBU) [25]. Later, novel architectures were presented and the name SCBU became obsolete. Therefore, authors from [65] introduced the terms "Input-Parallel-Output-Series" (IPOS) and "Input-Series-Output-Parallel" (ISOP), which describe the way in which the converter is connected to the source and the load. However, terms such as "partial rated charging converter" [28], [66] or "series connected PPP converter" [67] still can be found in the literature. Apart from that, the term "step-down PPC" is used in [68]–[70] to refer to different architectures. In conclusion, there exists a lack of agreement on the terms used for naming the different PPC architectures. Therefore, in order to propose a naming criteria, this document will follow the criteria

[1] The results are not experimental. They are obtained from simulations.

proposed in [65]. This means describing the connection options between the source, the load and the power converter: Input-Series/Parallel-Output-Parallel/Series.

PPC architectures are divided into two main groups: PPC architectures that require galvanically isolated topologies (such as, Flyback) and PPC architectures that do not require galvanically isolated topologies.

PPC architectures that require isolated topologies

Fig. 2.4 shows the six PPC architectures found through the literature that require isolated topologies. If a non-isolated topology is implemented in any of these architectures, there exists the risk of short-circuiting V_{source} (Fig. 2.4a, Fig. 2.4b and Fig. 2.4c) or V_{load} (Fig. 2.4d, Fig. 2.4e, and Fig. 2.4f).

Despite the literature presents the six PPC architectures from Fig. 2.4 as different solutions, by analysing their K_{pr} it is concluded that all of them are the same. To explain this, the IPOS step-up architecture from Fig. 2.4a is taken as example. Applying Kirchhoff's laws, equations (2.5),(2.6) are obtained. Then, K_{pr} is defined as the division between the power processed by the converter (P_{in}) and the load power (P_{load}), see (2.7). Applying equations (2.5), (2.6) on (2.7), the K_{pr} curve of the IPOS step-up is obtained as a function of the static voltage gain (G_V), given in (2.8),(2.9).

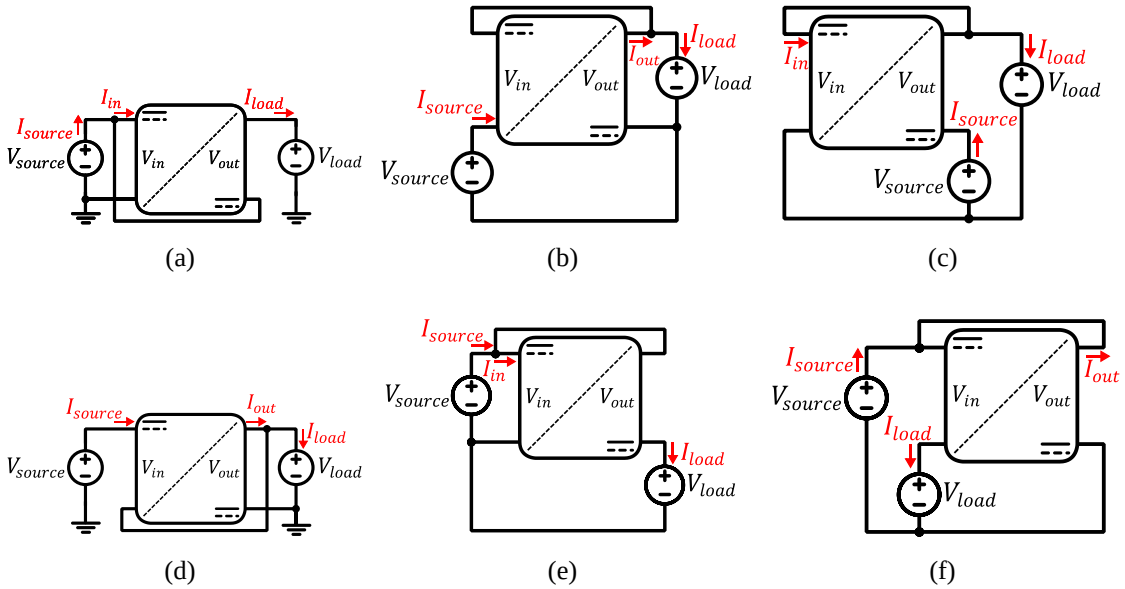


Fig. 2.4. PPC architectures that require isolated topologies. (a) IPOS step-up. (b) ISOP-I step-up. (c) ISOP-II step-up. (d) ISOP step-down. (e) IPOS-I step-down. (f) IPOS-II step-down.

$$V_{source} + V_{out} = V_{load} \tag{2.5}$$

$$I_{source} = I_{in} + I_{load} \tag{2.6}$$

$$K_{pr} = \frac{P_{in}}{P_{load}} = \frac{V_{source} \cdot I_{in}}{V_{load} \cdot I_{load}} \tag{2.7}$$

$$K_{pr_{IPOS\ step-up}} = \frac{1}{\eta_{sys}} - \frac{1}{G_V} \tag{2.8}$$

$$G_V = \frac{V_{load}}{V_{source}} \tag{2.9}$$

Where, $K_{pr_{IPOS\ step-up}}$ is the processed power ratio of the IPOS step-up and η_{sys} is the efficiency of the system, which is given in (2.10).

$$\eta_{sys} = \frac{V_{load} \cdot I_{load}}{V_{source} \cdot I_{source}} \tag{2.10}$$

Applying the same procedure to the rest of the architectures from Fig. 2.4, the expressions shown in Table 2.2 are obtained. In order to simplify them, η_{sys} is substituted by η. The results from Table 2.2 are plotted in Fig. 2.5, where η is considered ideal (η=1).

Table 2.2. K_{pr} curves of the IPOS-ISOP type architectures. In order to simplify the expressions, η_{sys} is substituted by η.

Architecture	K_{pr}
IPOS step-up	$\frac{1}{\eta} - \frac{1}{G_V}$
ISOP-I step-up	$\frac{1 - G_V}{\eta}$
ISOP-II step-up	$\frac{G_V}{\eta} - 1$
ISOP step-down	$\frac{1 - G_V}{\eta}$
IPOS-I step-down	$\frac{1}{\eta} - \frac{1}{G_V}$
IPOS-II step-down	$\frac{1}{G_V} - 1$

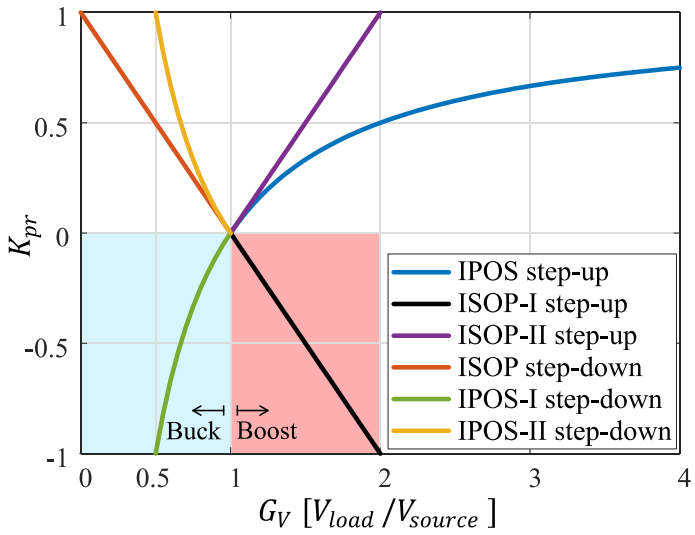


Fig. 2.5. Ideal K_{pr} curves IPOS-ISOP type architectures.

From Fig. 2.5, several conclusions can be obtained:

- **Voltage gain dependency:** As G_V approaches 1, K_{pr} decreases for all the architectures. This means that the smaller the difference between the source and load voltage, the less power the converter will process (main objective of PPCs).
- **All the architectures can be represented in one:** By comparing the K_{pr} curves of the ISOP-I step-up and the ISOP-II step-up architectures, it is observed that they obtain the same absolute values. Apart from that, if the terms V_{in} and V_{out} from the ISOP-I step-up exchange their position, one can observed that the ISOP-I step-up and ISOP-II step-up architectures are the same. The only difference between them is the way in which the authors assumed their power flow as positive. The same applies to the IPOS-I step-down and IPOS-II step-down architectures.

  Then, as it can be observed in Table 2.2, the K_{pr} curves of the IPOS step-up and the IPOS-I step-down architectures are the same. This is easily demonstrated by inverting the polarity of V_{out} in the IPOS step-up (Fig. 2.4a). The same applies to the ISOP step-down and the ISOP-I step-up architectures by inverting the polarity of V_{in} in the ISOP step-down (Fig. 2.4c).

  Also, by comparing the IPOS step-up and the ISOP step-down architectures (Fig. 2.4a and Fig. 2.4c), it can be observed that they are the same architecture, but considering a contrary system power flow (from the source to the load and vice

versa). In conclusion, the six architectures presented by the literature (Fig. 2.4) can be considered as the same solution.

- **Optimal architecture for boost applications:** If the application requires only voltage boost (G_V>1), the architecture that obtains lower K_{pr} values is the IPOS step-up. In fact, its K_{pr} curve never exceeds 1 when working in boost mode. On the contrary, the ISOP-I step-up and the ISOP-II step-up obtain $|K_{pr}|$ values greater than 1 when G_V is higher than 2. When K_{pr} is higher than 1, the converter does not operate in the partial power range, thus losing all benefits.
- **Optimal architecture for buck applications:** If the application requires only to reduce the voltage (0<G_V<1), the architecture that obtains lower K_{pr} values is the ISOP step-down. As in the previous case, in buck mode, the ISOP step-down architecture never exceeds the value of 1 for K_{pr}. On the other hand, the IPOS-I step-down and the IPOS-II step-down architectures obtain $|K_{pr}|$ values greater than 1 when G_V is lower than 0.5.

Based on these conclusions, from now on, the only two architectures that will be analysed from Fig. 2.4 are the IPOS step-up and the ISOP step-down. Also, in order to simplify the explanation, they will be referred just as IPOS and ISOP, respectively.

If the application requires buck-boost functionality, the selection between the IPOS and the ISOP is not so evident and it requires a more complex comparison. In other to work in voltage step-up/down applications, the power converter of a PPC architecture will enter in the shaded blue (IPOS case) and red (ISOP case) areas from Fig. 2.5. At these regions, the K_{pr} curve achieves negatives values, which means that the power flow inside the converter is reversed. This reversed power flow of the converter is demonstrated in [35], [71], [72]. In the case of the IPOS (for buck mode), the polarity of V_{out} is inverted and the flow of I_{in} changes its direction to the opposite way. Same thing occurs with the ISOP for boost mode. In this case, the polarity of V_{in} and the direction of I_{out} must be inverted. Bearing this in mind, in order to offer buck-boost functionality, the converter topology must enable bipolar voltage and bidirectional current. To explain this, a four quadrant analysis is proposed.

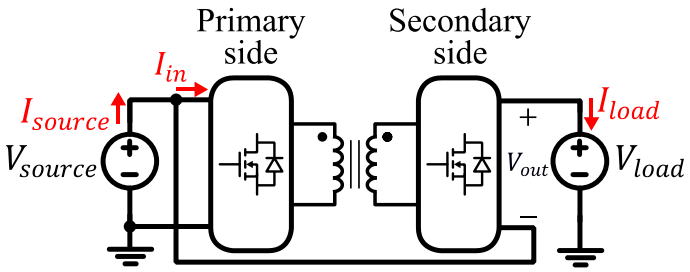


Fig. 2.6. Simplified electric diagram of an IPOS architecture.

Fig. 2.6 presents an IPOS architecture with its primary and secondary sides clearly divided by the transformer. The main objective of this analysis is to conclude the type of semiconductors required at each side. Fig. 2.7 presents the different configurations of semiconductors that exist. As it can be observed, a diode (Fig. 2.7a) is unipolar (it can only block the voltage in one direction) and unidirectional (it can only handle the current in a single direction). Therefore, it is defined as a one-quadrant semiconductor (1 or 3). Then, there is the active switch (represented as a MOSFET, Fig. 2.7b). This type of device is unipolar, but bidirectional (it can handle current in both directions). Therefore, it is considered as a two-quadrant semiconductor (1 & 4 or 2 & 3). Next, there is the back-to-back configuration between two semiconductors. On the one hand, Fig. 2.7c shows a

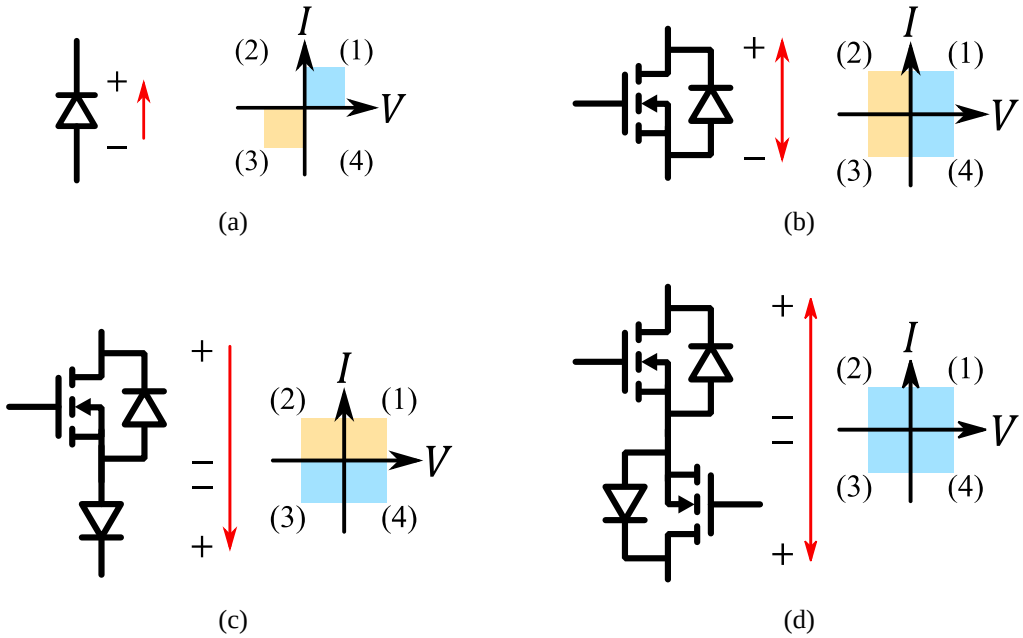


Fig. 2.7. Semiconductors' quadrants. (a) Diode. (b) Active switch (MOSFET or IGBT with an extra body diode). (c) Back-to-back connected active switch and diode. (d) Back-to-back connected active switches. The blue area represents the quadrant in which the semiconductor can work. The orange area represents the same but with the component inverted.

back-to-back between an active switch and a diode. This solution is bipolar (it can block voltage in both directions) and unidirectional. This solution is also considered as a two-quadrant (1 & 2 or 3 & 4). On the other hand, Fig. 2.7d shows a back-to-back between two active switches. Thus, a bipolar and bidirectional solution is achieved. This solution is the only four-quadrant (1 & 2 & 3 & 4).

Turning back to Fig. 2.6, depending on the requirements of the application, the currents (I_{source}, I_{in} and I_{load}) and voltage (V_{out}) from the figure may be bidirectional or bipolar. For example, in a bidirectional application, the semiconductors on both sides must be able to conduct current in both directions. Therefore, it is obvious that they have to work in quadrants 1 & 4 or 2 & 3. Apart from that, if the application requires buck-boost functionality, the secondary side semiconductor have to be able to block a bipolar V_{out}. In other words, they have to be able to work in quadrants 1 & 2 or 3 & 4.

Bearing this in mind, Table 2.3 (IPOS case) and Table 2.4 (ISOP case) specify the quadrants in which the semiconductors on each side of the transformer must operate for different types of applications. As it can be observed, the simplest configurations are achieved with unidirectional boost (IPOS) and unidirectional buck (ISOP) applications. In both cases, active switches are required in the primary side (quadrant 4, Fig. 2.7b) and diodes in the secondary side (quadrant 1, Fig. 2.7a). The next configurations are obtained

Table 2.3. Possible semiconductors that can be implemented on an IPOS architecture.

Voltage	Power flow	Primary side semiconductor	Secondary side semiconductor
Boost	Unidirectional	Quadrant 4	Quadrant 1
	Bidirectional	Quadrant 1 & 4	Quadrant 1 & 4
Buck-boost	Unidirectional	Quadrant 1 & 4	Quadrant 3 & 4
	Bidirectional	Quadrant 1 & 4	Quadrant 1, 2, 3 & 4

Table 2.4. Possible semiconductors that can be implemented on an ISOP architecture.

Voltage	Power flow	Primary side semiconductor	Secondary side semiconductor
Buck	Unidirectional	Quadrant 4	Quadrant 1
	Bidirectional	Quadrant 1 & 4	Quadrant 1 & 4
Buck-boost	Unidirectional	Quadrant 3 & 4	Quadrant 1 & 4
	Bidirectional	Quadrant 1, 2, 3 & 4	Quadrant 1 & 4

with a bidirectional boost (IPOS case) or bidirectional buck (ISOP case) applications. In both cases, active switches are necessary on both sides of the transformer (quadrants 1 & 4, Fig. 2.7b).

Regarding voltage buck-boost, a back-to-back solution must be implemented at the secondary side (IPOS) or primary side (ISOP). If the application is unidirectional, a back-to-back between an active switch and a diode is enough (quadrants 3 & 4, Fig. 2.7c). If the application is bidirectional, a four quadrant solution is necessary (quadrants 1 & 2 & 3 & 4, Fig. 2.7d). In this case, a back-to-back between two active switches must be implemented.

The results from Table 2.3 and Table 2.4 show the minimum required quadrants to fulfil the requirements imposed by the application. This means that they only take into account the currents shown in Fig. 2.6 (I_{source}, I_{in} and $I_{out} = I_{load}$). However, depending on the selected topology and modulation, it is possible that the fluxes of I_{in} and I_{out} do not match those of the semiconductors. For example, in a DAB with phase-shift modulation (PSM), the input current (I_{in}) only flows in a single direction, but the current that flows through the semiconductors (I_{conv}) has a positive and a negative flow, see Fig. 2.8. This can be a problem in unidirectional buck-boost applications. According to Table 2.4, an ISOP architecture would only require its primary side semiconductors to work in quadrants 3 & 4, thus by implementing a back-to-back between an active switch and a diode would be enough. However, the converter would not work properly due to the incompatibility between the bidirectional flow of I_{conv} and the unidirectional flow of a

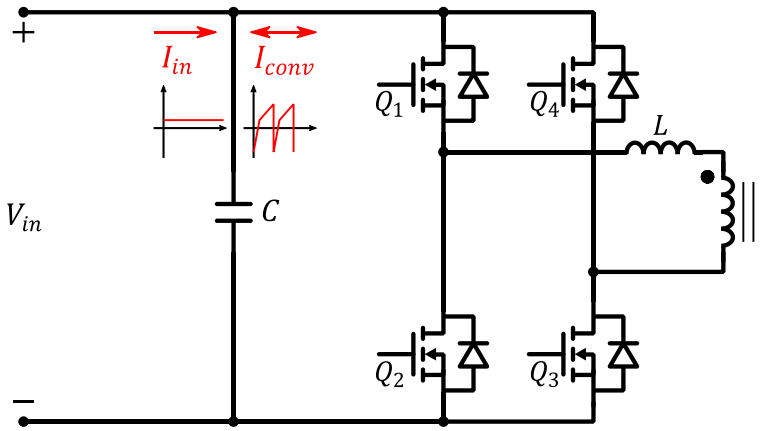


Fig. 2.8. Current flow on the primary side of a DAB topology.

back-to-back between an active switch and a diode. The converter could work if the back-to-back is between two active switches. In summary, the results from Table 2.3 and Table 2.4 are obtained from the analysis of the currents and voltages from Fig. 2.6. But, once the topology and modulation are defined, the requirements for unidirectional buck-boost applications may vary.

On another subject, the K_{pr} curves from Fig. 2.5 assume an ideal efficiency of the system (η_{sys}=100 %). However, this is never true when testing an experimental PPC prototype. All the passive and active components inside a power converter generate power losses in form of heat. Due to the non-ideal behaviour of η_{sys}, it is important to understand its effect on the K_{pr} curves.

In the first place, it must be discussed the way in which K_{pr} is defined. K_{pr} is defined as the ratio between the converter power and the system power (2.11).

$$K_{pr} = \frac{P_{conv}}{P_{sys}} \tag{2.11}$$

The converter power can be substituted by two variables: input power (P_{in}) or output power (P_{out}). The same occurs with the system power, which can by substituted by the source power (P_{source}) or the load power (P_{load}). Depending on which of these parameters are included in the division, the expression of K_{pr} is different. Table 2.5 defines the IPOS and ISOP K_{pr} curves for each combination. As it can be observed, if η_{sys} is considered as ideal, the K_{pr} expressions from each row are identical. But, with a non-ideal η_{sys}, the K_{pr} curves are different. This is shown in Fig. 2.9a (IPOS case) and Fig. 2.9b (ISOP case) for η_{sys}=90 %.

Table 2.5. K_{pr} expression under different parameters.

Architecture	$K_{pr} = \frac{P_{in}}{P_{load}}$	$K_{pr} = \frac{P_{out}}{P_{load}}$	$K_{pr} = \frac{P_{in}}{P_{source}}$	$K_{pr} = \frac{P_{out}}{P_{source}}$
IPOS	$\frac{1}{\eta_{sys}} - \frac{1}{G_V}$	$1 - \frac{1}{G_V}$	$1 - \frac{\eta_{sys}}{G_V}$	$\eta_{sys} - \frac{\eta_{sys}}{G_V}$
ISOP	$\frac{1 - G_V}{\eta_{sys}}$	$1 - \frac{G_V}{\eta_{sys}}$	$1 - G_V$	$\eta_{sys} - G_V$

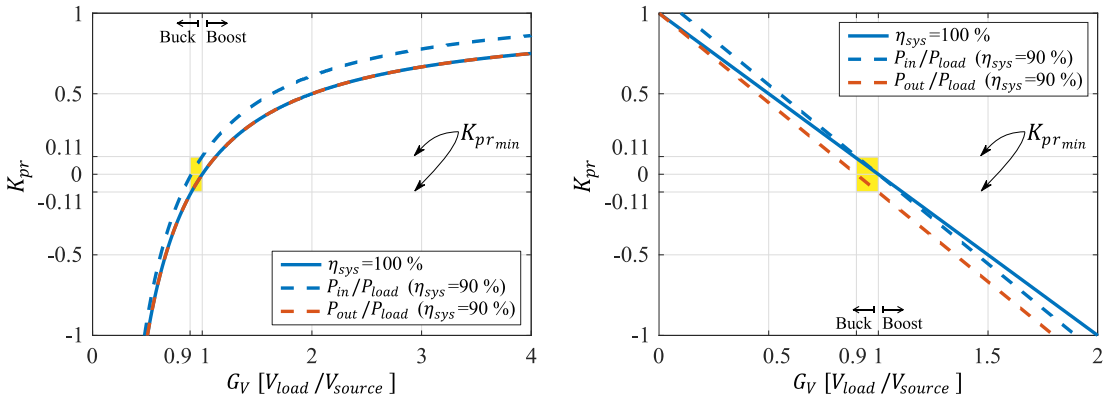


Fig. 2.9. Non-ideal K_{pr} curves (η_{sys}=90 %) in function of G_V. (a) IPOS. (b) ISOP.

Focusing on Fig. 2.9a, under boost conditions a non-ideal η_{sys} provokes higher K_{pr} values when is defined with P_{in} than with P_{out}. This difference represents the power losses, see (2.12).

$$P_{loss_{IPOS_{Boost}}} = |P_{in}| - |P_{out}| \tag{2.12}$$

Under buck conditions, it happens the contrary. Now the power flow is reversed. Consequently, the power that enters into the converter is P_{out} and the power that exits is P_{in} (2.13).

$$P_{loss_{IPOS_{Buck}}} = |P_{out}| - |P_{in}| \tag{2.13}$$

Inside the buck operation mode, there is a working region (coloured in yellow) where P_{in} and P_{out} have opposite power flows (P_{in}>0 & P_{out}<0). This means that both powers enter into the converter and no power exits the converter. Applying (2.14), it is observed that inside this region all the power processed by the converter are losses. In conclusion, the minimum K_{pr} achievable by the converter is proportional to its power losses. This is given by (2.15), where the minimum value of P_{conv} is given by P_{loss}.

$$P_{loss_{IPOS_{yellow}}} = |P_{in}| + |P_{out}| \tag{2.14}$$

$$K_{pr_{min}} = \frac{\min(P_{conv})}{P_{sys}} = \frac{P_{loss}}{P_{load}} = \frac{P_{source} \cdot (1 - \eta_{sys})}{P_{source} \cdot \eta_{sys}} = \frac{0.1}{0.9} = 0.\hat{1} \quad \textbf{(2.15)}$$

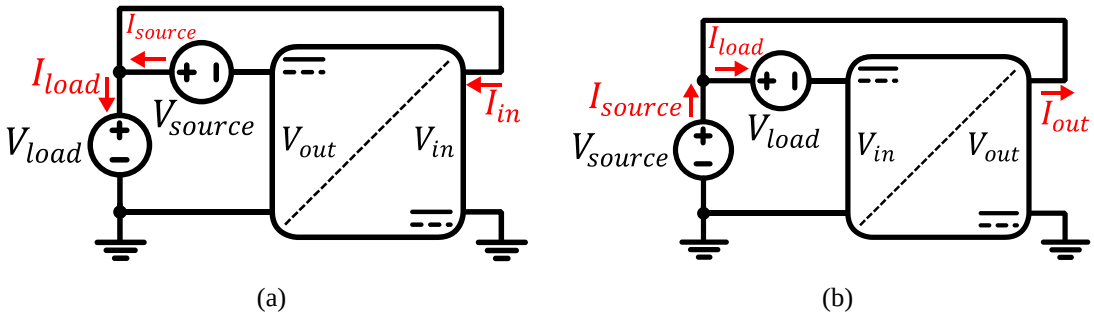
Regarding the ISOP architecture (Fig. 2.9b), similar conclusions are obtained. Under buck conditions, a non-ideal η_{sys} provokes a higher K_{pr} when it is defined with P_{in} than with P_{out}. Under boost conditions, the contrary occurs. Apart from that, it also exists a region in which P_{in} and P_{out} have opposite power flow (P_{in}>0 & P_{out}<0) and it is located exactly in the same range as in the IPOS case (η_{sys}=0.9<G_V<1). Again, inside this region all the power processed by the converter are losses.

To sum up, the efficiency of the system sets the minimum K_{pr} value that can be achieved with IPOS-ISOP type PPC architectures. This occurs when P_{in} and P_{out} have opposite flows and all the power processed by the converter are losses. This operation mode extends to η_{sys}<G_V<1.

PPCs that do not require isolated topologies

In [33], [73] a PPC architecture that allows non-isolated topologies is presented. Authors name it as "fractional charging converter (FCC)" and in comparison to the IPOS-ISOP architectures, the FCC has the positive poles of V_{source} and V_{load} connected to each other. Fig. 2.10 shows its configuration for step-up and step-down applications. As it can be observed, if a non-isolated topology is implemented, there is no risk of short-circuiting V_{source} or V_{load}. Usually, non-isolated topologies contain a lower number of components and they do not require a transformer, which simplifies the design and manufacturability of the conversion stage.

The FCC can be applied for voltage step-up and voltage step-down applications, but assuming that a non-isolated topology is implemented (main benefit of FCCs), it cannot achieve buck-boost functionality. This is demonstrated in Fig. 2.11, where the polarity of V_{out} of a FCC step-up architecture (Fig. 2.10a) is inverted to work in buck mode ($V_{source} - V_{out} = V_{load}$). Since a non-isolated topology is implemented, the negative poles of V_{in} and V_{out} are connected to each other, which results in a parallel connection between the source and the load.



(a) (b)

Fig. 2.10. PPC architectures that do not require isolated topologies. (a) FCC step-up. (b) FCC step-down.

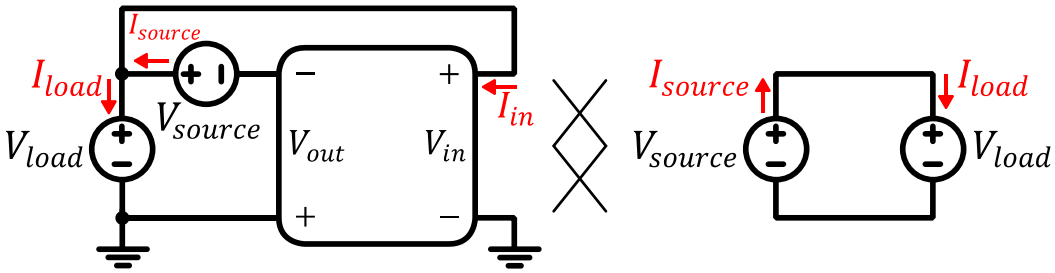


Fig. 2.11. Buck-boost functionality issue of a FCC architecture with a non-isolated topology.

On the other hand, applying the procedure described in equations (2.5)-(2.8) the K_{pr} achieved by the FCC architectures is obtained. Table 2.6 and Fig. 2.12 present the results. As it can be observed in Fig. 2.12, the FCC step-up architecture is limited to a G_V value of 2 and the FCC step-down to a G_V value of 0.5. Compared to the IPOS-ISOP architectures, the FCC also obtains lower K_{pr} values as G_V approximates to 1. Nevertheless, their K_{pr} curves present higher values than the IPOS-ISOP architectures for the same G_V.

In conclusion, the FCC architectures do not outperform IPOS-ISOP architectures in terms of K_{pr}. However, if a non-isolated topology is implemented, interesting results may be obtained regarding converter simplicity.

Table 2.6. K_{pr} of the FCC type architectures.

Architecture	K_{pr}
FCC step-up	$\frac{G_V}{\eta} - 1$
FCC step-down	$\frac{1}{G_V} - 1$

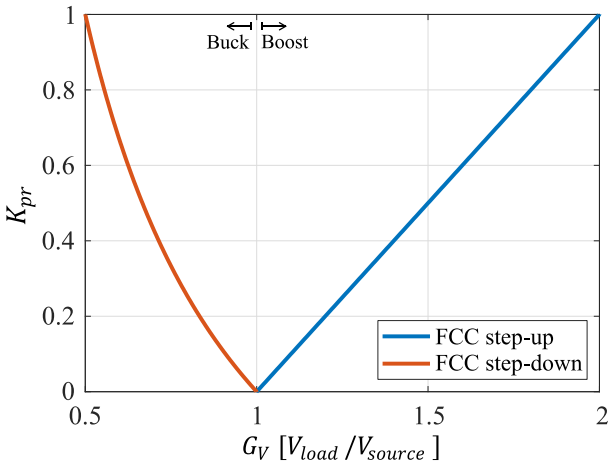


Fig. 2.12. Ideal K_{pr} curves of FCC type architectures.

Overview

With the aim of resuming the main points extracted from the PPC literature, Table 2.7 details different characteristics of each reference. Since each prototype is tested under different conditions, the purpose of Table 2.7 is not to compare the obtained results by each reference, but to make the reader see the goals achieved by each solution presented in the literature.

In the first place, architecture wise, the IPOS step-up is the most popular. On the other hand, when it comes to the K_{pr}, a wide variety of values are obtained. This is due to the fact that K_{pr} is directly proportional to the G_V of the application, which varies from one case study to another. Due to the low K_{pr} values, higher efficiencies than 99 % are achieved. Regarding the topology, all the presented works implement isolated topologies. Even authors from [33], [73] decide to implement an isolated full-bridge boost (IFBB) inside the FCC architecture. This demonstrates that there exists a lack of research on non-isolated topology based PPC architectures. Inside isolated topologies, the phase shifted full-bridge (PSFB) is the most popular one. It must be remarked that although isolated topologies are used for the stage conversion, the system is not. Indeed, there is not galvanically isolated solution that achieves PPP.

Table 2.7. Key parameters extracted from the PPC literature.

Ref.	Architecture	K_{pr}	η_{sys}	Topology	Application	Power flow	
						Conv.	Sys.
[28]	IPOS-II step-down	0.33	-	PSFB	EV fast charging	Uni.	Uni.
[29]	IPOS step up ISOP-I step up ISOP step down	- 0.15 0.1	- 99 % 98.5 %	Flyback PSFB PSFB	PV	Uni.	Uni.
[40]	IPOS step up	0.3	98.55 %	PSFB	EV fast charging	Uni.	Uni.
[65]	IPOS step up ISOP-I step up	0.4 0.5	95.5 % 92 %	Flyback	PV	Uni.	Uni.
[68]	ISOP step down	0.8	96.74 %	DAB	-	Bi.	Bi.
[70]	ISOP step down	0.3	98.6 %	PSFB	PV	Uni.	Uni.
[71]	IPOS step up	0.15	99.5 %	PSFB-CT[2]	PV	Bi.	Uni.
[72]	ISOP-II step up	-	98.8 %	Cuk isolated+ Unfolder	PV+ESS	Bi.	Uni.
[73]	FCC-step-down	0.21	98.2 %	IFBB	ESS	Bi.	Bi.
[74]	IPOS step up	0.25	98.9 %	DAB	ESS integration	Bi.	Bi.
[75]	IPOS step up	0.2	96.25 %	PSFB	PV	Uni.	Uni.
[76]	ISOP-II step up	0.2	96 %	Flyback	PV	Uni.	Uni.
[77]	IPOS step up	From 0.1 to 0.7	90 %	Flyback	PV	Uni.	Uni.
[78]	IPOS step up	0.41	99.3 %	DAB	EV charging	Bi.	Bi.
[79]	ISOP step-down	0.21	99.04 %	PSFB	EV fast charge	Uni.	Uni.
[80]	IPOS step-up IPOS step-up	0.15 0.15	99.01 % 98.95 %	SHB/CFPP[3] FBPS/CFPP[4]	PV	Bi.	Uni.
[81]	IPOS step-up	-	99.5 %	PSFB-3q[5]	-	Bi.	Uni.
[27][6]	IPOS step up	0.4	-	DAB	PV+ESS	Bi.	Bi.
[31][6]	IPOS step up	0.83	97.6 %	Flyback	PV	Uni.	Uni.
[35][6]	IPOS step up	-	96 %	DAB+Unfolder	Wind generation	Bi.	Uni.
[66][6]	ISOP-I step up	0.5	99 %	PSFB	PV	Uni.	Uni.
[69][6]	ISOP step down	0.35	98 %	PSFB	EV fast charging	Uni.	Uni.
[82][6]	IPOS step up	0.4	-	DAB	PV+ESS	Bi.	Bi.
[83][6]	IPOS step-up	0.1	-	PSFB-4q[7]	-	Bi.	Uni.
[84][6]	ISOP-I step up	0.15	98.76 %	Flyback	PV	Uni.	Uni.

[2] Phase-shifted with Centre Tap Transformer.
[3] Symmetrical Half-Bridge/Current-Fed Push–Pull
[4] Full-Bridge Phase-Shift/ Current-Fed Push–Pull
[5] Phase-shifted full bridge with a 3 quadrant back-to-back (active switch and a diode)
[6] The results are not experimental. They are obtained from simulations.
[7] Phase-shifted full bridge with a 4 quadrant back-to-back (two active switches)

Apart from that, the great majority of the applications are related to PV systems, followed by ESS and EV charging. Also, applications that require a buck-boost functionality are presented in [35], [71], [72]. As it can be observed, although the system's power flow is unidirectional, a bidirectional power flow is obtained in the converter. In consequence, the power flow of the converter is reversed and the power converter enters in the shaded blue or red areas from Fig. 2.5.

2.1.3 Mixed Strategies

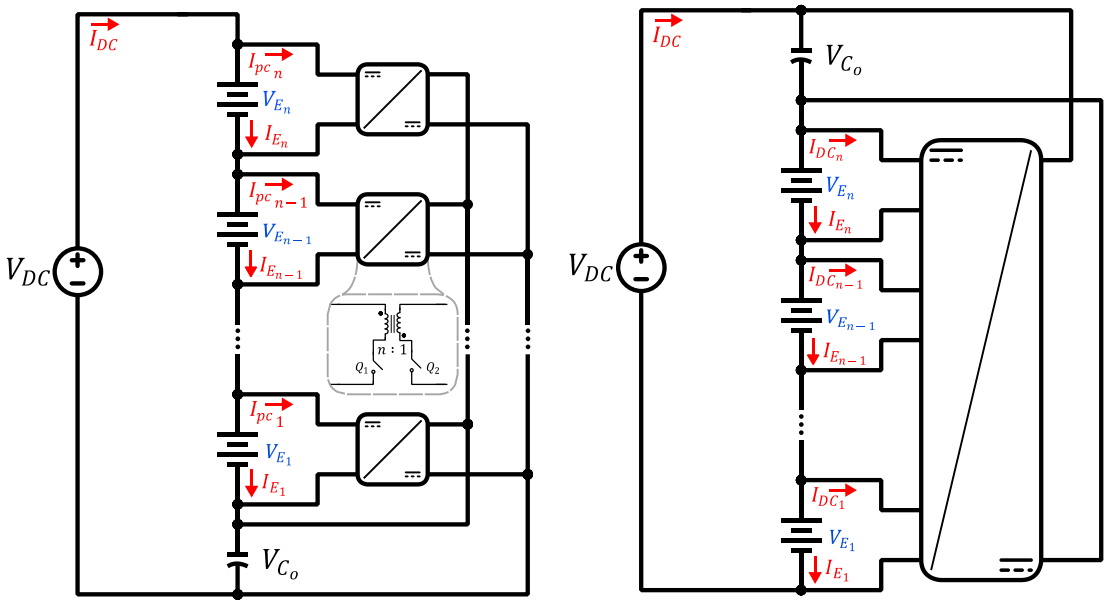
The disadvantages and limitations of DPC and PPC architectures give reason to investigate alternative architectures that can offer a better performance for specific applications. This type of architectures also aim to achieve PPP, but they do not share common characteristics between them.

In the first place, there is the series parallel partial power (SPPP) architecture. Fig. 2.13 shows its configuration. This type of architecture mixes the characteristics of DPC and PPC solutions: it has balancing purposes (typical application of a DPC) and power flow control between a source and a load with different voltage level (typical application of PPC). Indeed, the SPPPs from Fig. 2.13 are very similar to a B2E architecture, since the energy is transferred between the elements in series and a common bus (V_{C_o}). However, the SPPP contains the common bus connected in series with the rest of the elements. Also, it is observed that SPPP require isolated topologies. If a non-isolated topology is implemented, the series connected elements are shot-circuited.

The K_{pr} achieved by this type of solutions is defined by the voltage value of the series connected capacitor, see (2.16) [85].

$$K_{pr} = \frac{V_{C_o}}{V_{E_1} + \cdots + V_{E_n}} \tag{2.16}$$

When it comes to the topology, the solutions are very varied. Authors from [85] implement modular flybacks, and in [86], PSFB converters are selected. However, authors from [87] decide to make use of a multi-input DAB converter, resulting in the configuration shown in Fig. 2.13b.



(a) (b)

Fig. 2.13. SPPP architecture. (a) Modular flyback [85], [86]. (b) Multi input converter [87].

Another alternative to DPC and PPC architectures is to implement a multi-source converter (Fig. 2.14). In this case, a single converter is used for charging and discharging 2 different ESS. V_{LV} can be part of the battery V_{HV} or a separate battery. Authors from [88] claim that the multi-source converter from Fig. 2.14 reduces the cost of the converter and it achieves high efficiency and high power density due to the reduction of power processed. When it comes to the stage of conversion, authors from [88] compare the duty

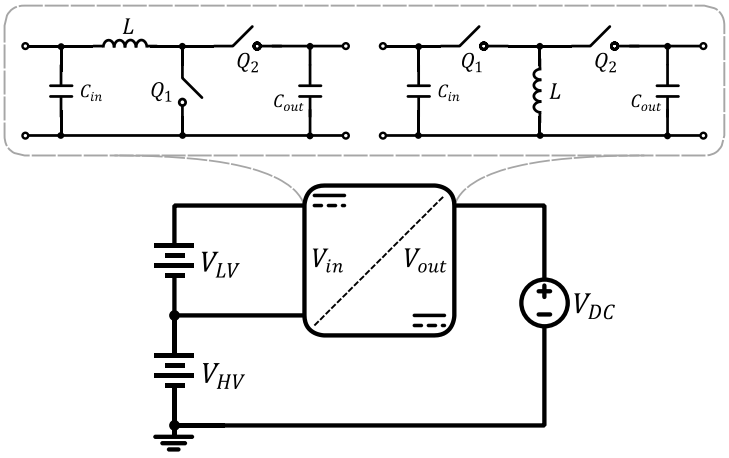


Fig. 2.14. Multi source converter.

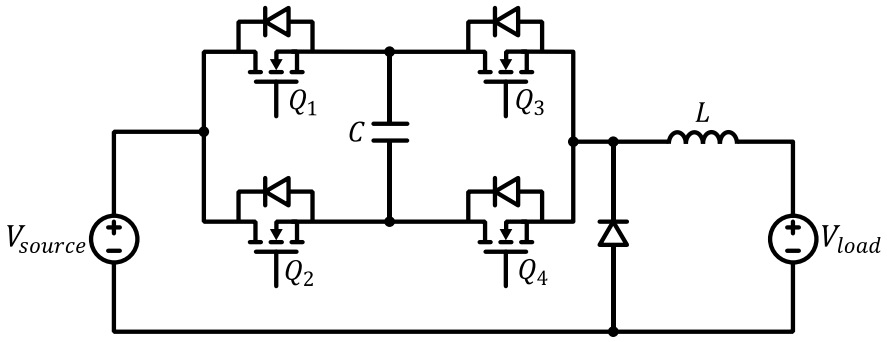


Fig. 2.15. Pseudo partial power converter based proposed in [89].

ratio, K_{pr} and the connection polarity of different non-isolated topologies, such as: buck, boost, buck-boost, and Cuk.

In third place, authors from [89] propose a pseudo partial power converter based on a switched capacitor topology, see Fig. 2.15. The presented converter is designed for step-down applications and allows the implementation of semiconductors with lower ratings. Its operation principle is based on regulating the voltage level of the switched capacitor by adjusting the duty cycles of the pair semiconductors $Q_{1,4}$ and $Q_{2,3}$.

Finally, there is the auxiliary series converter (Fig. 2.16). In this case, two power converters are required. The main converter always works in a peak efficiency working point. Instead, the auxiliary converter regulates the output voltage by adding or subtracting voltage from V_{source}. The polarity of this auxiliary voltage affects directly to the K_{pr} of the main converter. However, the auxiliary series converter is referred in [90] as a PPP solution, it can not be considered as such. Indeed, the sum of the power processed by both converters is never lower than the system power. Apart from that, authors from

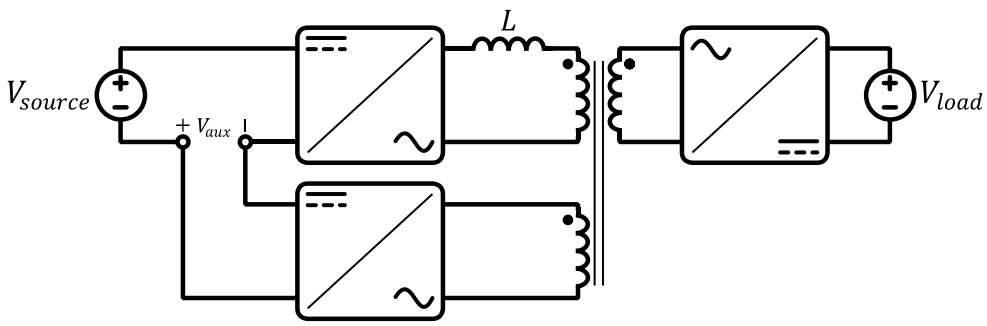


Fig. 2.16. Auxiliary series converter [90].

Table 2.8. Key parameters extracted from the literature around mixed PPP strategies.

Source	Architectures	K_{pr}	η_{sys}	Topology	Application
[85]	SPPP	0.5	95 %	Flyback	ESS
[86]	SPPP	0.48	-	PSFB	ESS
[87]	SPPP	-	97.5 %	Multi-input DAB	ESS
[88]	Multi-ESS	0.3	99.63 %	Buck-boost	EV power train
[90]	Auxiliary	-	97.7 %	DAB-LLC +Auxiliary IFB	-
[89][8]	Pseudo partial	0.57	99.3 %	Switched capacitor	EV fast charging

[90] conclude that adding an extra power converter results in a bigger volume and lower efficiency.

Overview

With the aim of summarizing the main points extracted from the literature around mixed PPP strategies, Table 2.8 details the key characteristics of each reference. Since each prototype is tested under different conditions, the aim of Table 2.8 is not to compare the obtained results by each one, but to make the reader see the goals achieved by each converter presented in the literature (together with their corresponding solutions).

It is observed that each solution presents different characteristics and topologies, both isolated and non-isolated. When it comes to the multi-ESS architecture [88], it can be considered as the most promising one due to its high efficiency and simple power conversion circuit. The pseudo partial converter solution also present an efficient performance, but no experimental results are shown. Then, there is the auxiliary architecture proposed in [90]. However, authors conclude that the obtained converter is slightly less efficient (-0.3 %) and bigger (+10).

2.2 Main Benefits and Drawbacks of Partial Power Processing

2.2.1 Benefits

This subchapter summarizes the main benefits of the PPP strategies.

[8] The results are not experimental. They are obtained from simulations.

- **Less power processed by the converter:** The principal advantage of PPP based solutions is the reduced power processed by the converter. In the case of DPC architectures, the power processed by the converter is proportional to the current mismatch between the series connected elements. Whereas in PPC architectures, the power processed by the converter is in function of G_V.
- **Lower current/voltage class devices:** In both strategies reduced current/voltage class devices can be implemented. In the case of semiconductors, lower voltage class entails better conducting devices ($R_{DS}{\sim}V_{DS}^{2.5}$ [91]). Also, when it comes to passive devices, lower voltage and current stress implies a smaller volume and less costly devices.

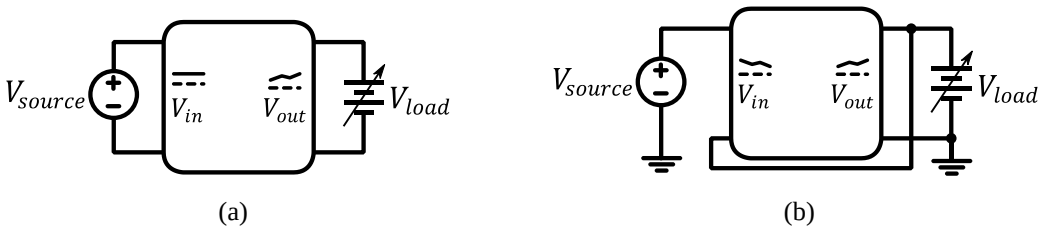
2.2.2 Drawbacks

The main drawbacks and challenges that PPP based strategies present are:

- **No galvanic isolation:** There is no PPP based architecture that provides galvanic isolation between the source and load. This fact can be unacceptable in applications where the normative demands it. In these cases, an extra element or power converter that provides the concerned isolation border must be added.
- **Higher risk at start-up conditions:** Since the devices inside the converter are rated for lower voltage class, an over voltage protection circuit or control must be added for start-up conditions [88]. This may affect to the efficiency, volume and complexity of the power converter.
- **DPC architectures:**
    - **Limited applications:** The implementation of DPCs is limited to applications where the voltage V_{DC} is the result of the sum of the elements connected in series. If buck or boost functionalities are required, an extra power converter must be implemented to correct the voltage mismatch. Apart from that, regarding E2E architectures, there is a risk of exceeding the power rating of the converter if an adequate dimensioning is not carried out in function of the mismatch to correct [45].

- **PPC architectures:**
    - **Voltage gain dependency:** The K_{pr} is directly dependent on the G_V value of the application. So, if there is a high voltage difference between the source and the load, PPCs may result inadequate.
    - **Topology complexity:** The most promising PPC architectures are the ones that require isolated topologies. However, they cannot be considered as isolated solutions (due to the ground connection between the source and the load). Therefore, when comparing to a full power converter (FPC), this type of architectures must face against non-isolated topologies (for example, buck or boost), which usually contain a lower number of components and do not include a high frequency transformer.
    - **Wider operation range:** Compared to FPCs, PPCs cause a larger operation range inside the power converter [40]. To explain this, Fig. 2.17 compares the input/output voltage operation range of the converter for a battery charging application. The voltage source is assumed as constant and the battery voltage is variable in function of its SOC. As it can be observed, a FPC works with a fixed V_{in} and a variable V_{out} (Fig. 2.17a). However, if an ISOP architecture is implemented (Fig. 2.17b), both V_{in} and V_{out} are variable and proportionally inverted. As V_{out} increases, V_{in} decreases. Consequently, the operation range of the converter is increased, which affects to its design and performance.

Bearing all this in mind, it is decided to focus the research on PPC architectures. As observed in the literature, the great amount of recent publications shows a great interest on the analysis and implementation of this type of architectures. The efficiencies achieved by PPCs are above 99 % and their application is very wide: PV generation, ESS



(a) (b)

Fig. 2.17. Operation range comparison. (a) FPC. (b) ISOP.

integration, EV fast charging… For all these reasons, PPC architectures stand out as promising solutions to substitute conventional FPCs regarding power converter downsizing (smaller volume), cost reduction (lower current/voltage class devices) and efficiency improvement (reduced losses).

2.3 Comparison Parameters

The two main types of PPC architectures that exist are the IPOS-ISOP and the FCC. The former requires an isolated topology to avoid a short-circuit, but the latter allows the implementation of non-isolated topologies. Through the rest of the document both PPC solutions are studied in detail, which involves the analysis and comparison of different topologies. Each of these topologies has a different number of semiconductors, passive elements or modulation strategies and a fair comparison between them entails a challenge regarding the selection of the parameters to compare.

2.3.1 Processed Power by the Converter

The power processed by the converter is a key factor that directly affects the rating of the components, as well as, the size and cost of the final solution. Apart from that, when comparing the performance between PPP and FPP strategies, authors from [92], [93] claim that an exhaustive analysis on the power processed by the converter helps to discover which strategies do really achieve PPP and which ones do not.

Besides the active power (P), according to the definition given by IEEE [94], during the steady state of a DC-DC converter, the energy processed by storage components (capacitors and inductors) and that is not transferred from the source to the load is considered as non-active power flow (N). Do not confuse with reactive power (Q). Bearing this in mind, both types of powers (active and non-active) are described.

Active power

Considering an ideal power converter, the active power processed by the converter at the input and at the output is the same, and it is calculated as shown in (2.17).

$$P_{in} = \frac{E_{in}}{T_s} = \frac{1}{T_s} \cdot \int_0^{T_s} v_{in}(t) \cdot i_{in}(t) \cdot dt \quad \textbf{(2.17)}$$

Where, E_{in} is the input energy of the converter, T_s is the period, and v_{in} and i_{in} are the input instantaneous voltage and current of the converter.

In case the input voltage consists of a constant voltage source, equation (2.17) can be simplified as shown in (2.18).

$$P_{in} = V_{in} \cdot \overline{I_{in}} \quad \textbf{(2.18)}$$

Where, V_{in} is the constant input voltage of the converter and $\overline{I_{in}}$ is the average input current of the converter.

Non-active power

The power that does not result in active power at any frequency is considered as non-active power [71],[93]. The energy that is stored and delivered by reactive components causes losses, and therefore, the main components that consume non-active power are inductors and capacitors (2.19),(2.20).

$$E_L(t) = \frac{1}{2} \cdot L \cdot i_L^2(t) \quad \textbf{(2.19)}$$

$$E_C(t) = \frac{1}{2} \cdot C \cdot v_C^2(t) \quad \textbf{(2.20)}$$

Where, E_L is the stored energy by the inductor, E_C is the stored energy by the capacitor, i_L is the instantaneous inductor current and v_C is the instantaneous capacitor voltage.

In steady state operation, inductors and capacitors always have a charging and a discharging process. The time required for each charging and discharging period can have a different value, but the energy charged at the component is the same as the one that is discharged. In conclusion, in steady state, the average energy of an inductor or a capacitor must be zero (2.21),(2.22).

$$E_L = \int_0^{T_s} v_L(t) \cdot i_L(t) \cdot dt = 0 \tag{2.21}$$

$$E_C = \int_0^{T_s} v_C(t) \cdot i_C(t) \cdot dt = 0 \tag{2.22}$$

The amount of energy that is absorbed or released by the storage elements, is given by equations (2.23) and (2.24).

$$\Delta E_L = \int_0^{D \cdot T_s} |v_L(t) \cdot i_L(t)| \cdot dt = \int_{D \cdot T_s}^{T_s} |v_L(t) \cdot i_L(t)| \cdot dt \tag{2.23}$$

$$\Delta E_C = \int_0^{D \cdot T_s} |v_C(t) \cdot i_C(t)| \cdot dt = \int_{D \cdot T_s}^{T_s} |v_C(t) \cdot i_C(t)| \cdot dt \tag{2.24}$$

Where D is the duty cycle.

Then, the non-active power processed by an inductor (N_L) and a capacitor (N_C) is obtained (2.25),(2.26). Equation (2.27) represents the total non-active power processed by the converter.

$$N_L = \frac{2 \cdot \Delta E_L}{T_s} \tag{2.25}$$

$$N_C = \frac{2 \cdot \Delta E_C}{T_s} \tag{2.26}$$

$$N_{tot} = \sum_{j=1}^{n_L} N_{L_j} + \sum_{k=1}^{n_C} N_{C_k} \tag{2.27}$$

2.3.2 Electrical Stress of Components

All the components inside the power converter are subjected to an electrical stress defined by their maximum voltage and current. In order to compute this stress, the literature presents different alternatives. Authors from [95] suggest the component stress factor (CSF), a dimensionless parameter that correlates with the power dissipated in the

component. To be more precise, the calculus is divided in 3 groups: semiconductors (SCSF), windings (WCSF) and capacitors (CCSF).

$$SCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{pk}^2 \cdot I_{rms}^2}{P_S^2} \quad \textbf{(2.28)}$$

$$WCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{\widehat{V_{pk}^2} \cdot I_{rms}^2}{P_S^2} \quad \textbf{(2.29)}$$

$$CCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{pk}^2 \cdot I_{rms}^2}{P_S^2} \quad \textbf{(2.30)}$$

Where, V_{pk} for SCSF and for CCSF represents the maximum voltage that the semiconductor or the capacitor withstands in steady state, and $\widehat{V_{pk}}$ for WCSF represents the maximum average voltage in the winding. $\frac{\sum_j W_j}{W_i}$ consists of a weighting factor component given by the amount of resources to be assigned to the component.

Nevertheless, authors from [95] comment that all of the candidate topologies must have available exactly the same amount of silicon, magnetic winding area and capacitor volume. This condition does not suit with the intended comparison of the present document, where topologies with different number of devices are implemented.

Another alternative to compute the electrical stress of passive and active elements is the VA rating [40]. This method is also dimensionless, since it divides the maximum current/voltage value of a device by a base current and base voltage. Table 2.9 describes the expressions for each component. Due to its ease of implementation, the VA rating is selected for electrical stress comparison.

Table 2.9. Electrical stress of active and passive components.

Parameter	Meaning
$\frac{V_{rms} \cdot I_{rms}}{V_{base} \cdot I_{base}}$	VA rating of the inductor/transformer
$\frac{V_{pk} \cdot I_{rms}}{V_{base} \cdot I_{base}}$	Stress in the capacitor
$\frac{V_{pk} \cdot I_{rms}}{V_{base} \cdot I_{base}}$	Stress in the semiconductor

2.3.3 Thermal Stress: Top-Case Temperature of Semiconductors

The heat caused by the power losses puts the devices under a thermal stress. In consequence, their electrical characteristics vary and, in a worst-case scenario, the device could fail. To avoid this, the top-case temperature of the semiconductors is measured. This way, the semiconductors are protected from over temperatures and valuable information around the thermal performance and its distribution is obtained. For example, the on-state resistance of a semiconductor increases with the temperature. So, more precise models can be developed by measuring their temperature. Also, if low temperatures are achieved, the heat sink could even be reduced.

In order to compare the behavior of the PPC converters, the top-case temperature of the semiconductor is measured as one of the main parameters. Fig. 2.18 shows the top-case temperature measurement of a TO-247-4 type capsule. As it can be observed, the thermocouple is attached directly to the center of the device. It is important to mention that the term "top-case" does not refer to the case temperature of the device. Usually, manufactures use the term "case" to refer to the side at which the heatsink is connected. In the case of Fig. 2.18, this is the bottom side. However, this point is less accessible; therefore, the top-side or top-case is measured.

2.3.4 Efficiency

The efficiency of a power converter computes the power losses produced by the converter. This is obtained through the division between the output power of the converter and the input power (2.31). The efficiency of the system is similarly calculated, but the load power is divided by the source power (2.32).

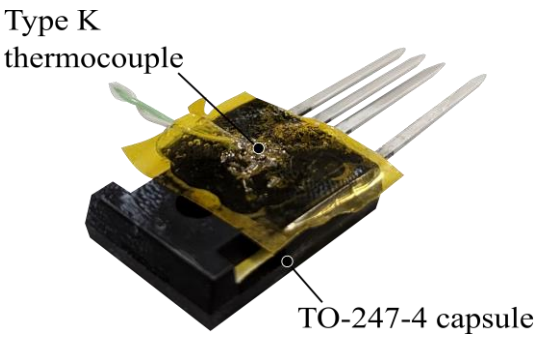


Fig. 2.18. Top-case temperature measurement using a thermocouple.

$$\eta_{conv} = \frac{P_{out}}{P_{in}} \tag{2.31}$$

$$\eta_{sys} = \frac{P_{load}}{P_{source}} \tag{2.32}$$

When implementing FPP strategies, the power processed by the converter is the same as the one that flows from the source to the load. Therefore, both efficiencies result in the same value. In the case of a PPP-based solution, the converter power and system power are different, and so are their efficiencies. However, the values of η_{conv} and η_{sys} can be related by the K_{pr} (2.33).

$$\eta_{sys} = 1 - K_{pr} \cdot (1 - \eta_{conv}) \tag{2.33}$$

Comparing the efficiency results of two different converters at specific working points may not be completely loyal to a real case scenario. In ESS charging applications, the load is usually variable in voltage and power. Therefore, the power converter is forced to work at different working conditions that constantly vary the efficiency of the converter through the charging process. For this reason, it is important to consider a time domain analysis and compute the energy efficiency. Bearing this in mind, this work also provides the efficiency oriented to energy losses (Wh) and not to power losses (W) as classical design. The total energy losses produced by the power converter are computed by applying (2.34) and (2.35). The energy loss at the i^{th} time is given by E_{loss_i} and it is obtained by using (2.34). Here, P_{loss_i} is the power loss at the i^{th} time instant and $P_{loss_{i-1}}$ is the power loss at the $i-1^{\text{th}}$ time instant. The total energy loss over the complete cycle is obtained by summing the energy loss at each time instant and it is given by (2.35).

$$E_{loss} = \frac{P_{loss_i} + P_{loss_{i-1}}}{2} \cdot (t_i - t_{i-1}) \tag{2.34}$$

$$E_{loss_{total}} = \sum_{i=1}^{k} E_{loss_i} \tag{2.35}$$

Where k is the total number of time instants.

Chapter 3

PARTIAL POWER CONVERTERS THAT DO NOT REQUIRE ISOLATED TOPOLOGIES

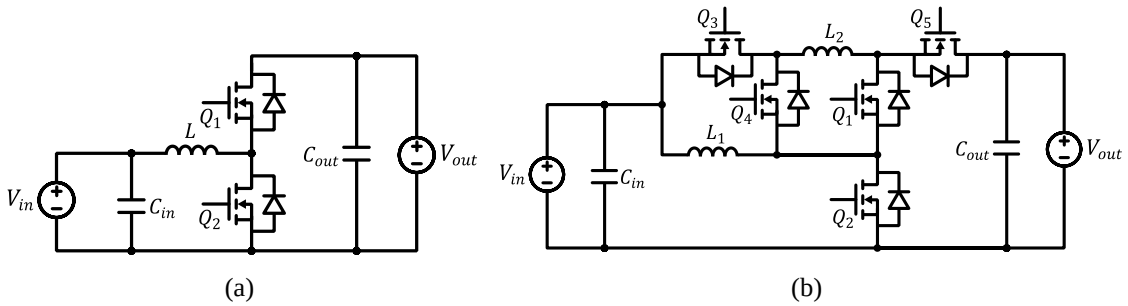
This Chapter discusses the possibility of achieving PPP with non-isolated DC-DC topologies. With this purpose, FCC architectures are selected for the analysis since they are the only PPC architectures that enable non-isolated topologies. Via simulations, it is observed that single inductor non-isolated topologies cannot achieve partial power processing, since the obtained current and voltage waveforms are the same as in a FPC. However, double inductor non-isolated topologies achieve reduced inductor current, lower thermal stress of the semiconductors and improved efficiency on FCC type architectures. In order to confirm the results obtained from the simulations, the single and double inductor topologies are tested experimentally.

Significant content from this Chapter corresponds to the journal article [J3].

3.1 Motivation, Investigated Topologies

The only PPC architectures that enable non-isolated topologies are the FCC type. These architectures do not present any short-circuit risk if a non-isolated topology is implemented on them. Thus, a high frequency transformer is avoided. This is an advantaged compared to the IPOS and the ISOP architectures, which require an isolated topology. However, there is no article in the literature that analyses the performance of non-isolated topologies on FCC architectures. Even the authors from [33], [73] (who presented FCC architectures for the first time) decide to implement isolated topologies on their work.

This Chapter aims to extend the analysis around non-isolated topology based FCC architectures. To be more precise, its objective is to conclude if non-isolated DC-DC topologies can improve their performance by implementing them on a FCC architecture. The two non-isolated DC-DC topologies under analysis are a single inductor HB (Fig. 3.1a) and a modified switched inductor boost converter (MSIBC, Fig. 3.1b). The HB consists of two active switches and a single inductor. The MSIBC consists of 5 active switches and two inductors. It is proposed in [96] with reduced voltage stress across the active switches by modifying the structure of classical switched inductor boost converter (SIBC). The MSIBC is based on the principle of parallel charging and series discharging of inductors L_1 and L_2. The reason for selecting these topologies is their number of inductors. As it will be explained later, this is a determining factor in the results.



(a) (b)

Fig. 3.1. Non-isolated DC-DC topologies under analysis. (a) HB. (b) MSIBC.

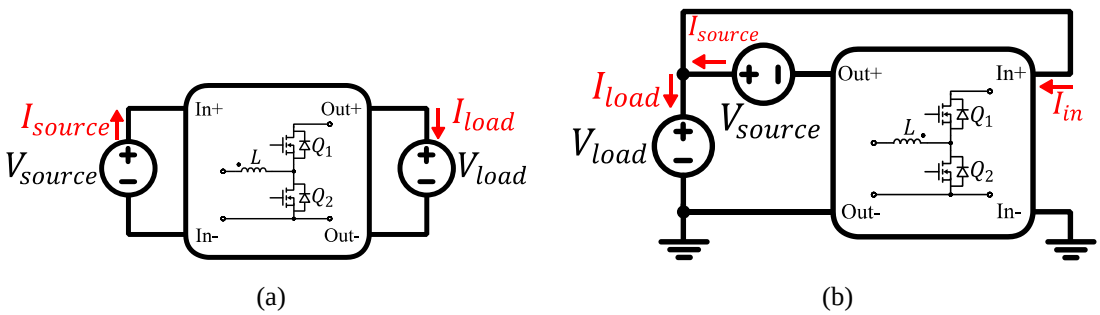
3.2 Single Inductor Case Study

The first topology to analyze is the conventional single inductor HB. The HB topology is implemented in a FPC architecture (HB-FPC, Fig. 3.2a) and in a FCC type PPC architecture (HB-PPC, Fig. 3.2b). The main objective of this comparison is to observe the benefits that the FCC architecture may present to the HB.

Table 3.1 presents the system level electrical parameters that define the simulation conditions. As it can be observed, it consists of a voltage boost application, where G_V stays bellow 2. This way, a K_{pr} value lower than 1 is ensured for the HB-PPC. Please remember that the PPP region of FCC architectures is limited to $0.5<G_V<2$ (see Fig. 2.12). Table 3.2 defines the design parameters of the HB-FPC and the HB-PPC. The first difference that exists between both solutions are V_{in} and V_{out}. V_{in} and V_{out} from the HB-FPC correspond to the source and load voltage from Table 3.1. This is because the input-output ports are directly connected to the source and the load. However, the results of the HB-PPC are not that obvious. Its input port is connected in parallel to V_{load} (thus, $V_{in} = V_{load}$) and its output port is connected in series between V_{source} and V_{load} (thus, $V_{out} = V_{load} - V_{source}$). As a result, the HB-FPC works in boost mode, whereas the HB-PPC works in buck mode. Regarding the K_{pr}, four times lower power is expected in the HB-PPC, achieving a maximum processed power of 375 W. The same storage elements and semiconductors are implemented in both cases.

3.2.1 Simulation Results

The power losses considered in the simulated circuits are the semiconductor power losses. These include conduction losses, given by (2.1), and switching losses. In order to



(a) (b)

Fig. 3.2. Single inductor case study. (a) HB-FPC. (b) HB-PPC.

Table 3.1. System level electrical parameters for the single inductor case study.

Parameter	Value
V_{source}	100 V
V_{load}	125 V
G_V	1.25
P_{load}	1.5 kW

Table 3.2. Converter level design parameters for the single inductor case study.

Parameter	Value	
	HB-FPC	HB-PPC
V_{in}	100 V	125 V
V_{out}	125 V	25 V
Operation mode	Boost	Buck
K_{pr}	1	0.25
P_{conv}	1.5 kW	0.375 kW
f_{sw}	50 kHz	50 kHz
L	150 µH	150 µH
C	200 µF	200 µF
Q_{1-2}	IPT65R033G7[9]	IPT65R033G7[9]

calculate the theoretical switching losses of the semiconductors, previously characterized curves have been used. The passive elements are considered as ideal and their internal resistances are neglected. The simulations are carried out with an open loop control.

$$P_{cond} = R_{DS} \cdot I_{RMS}^2 \tag{3.1}$$

In the first place, Fig. 3.3 compares the steady state current and voltage waveforms of the main devices from each solution. Fig. 3.3a shows the inductor current/voltage waveforms and as it can be observed, both architectures obtain exactly the same results. Fig. 3.3b presents the current/voltage waveforms of the semiconductors. Since the HB-FPC and the HB-PPC work in boost and buck mode, respectively, the semiconductors to compare are contrary. Again, the waveforms are similar in both solutions. Same thing happens with the output capacitor (Fig. 3.3c). It is concluded that the HB-PPC does not

[9] V_{DS}=650 V, R_{DS}=29 mΩ @T_j=25 ºC

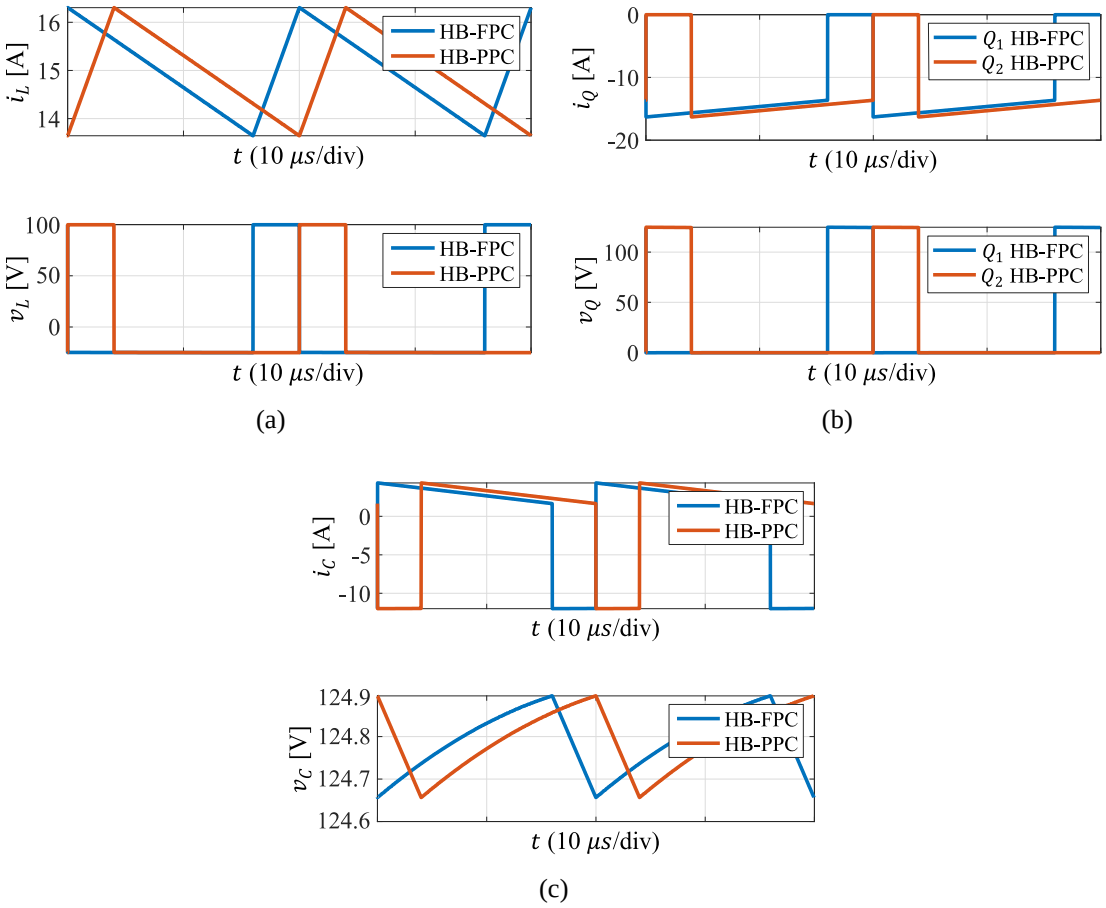


Fig. 3.3. Current and voltage steady state waveforms in the single inductor case study. (a) Inductor. (b) Semiconductor. (c) Output capacitor.

Table 3.3. Power losses, efficiency and K_{pr} results of the single inductor case study.

Parameter	Value	
	HB-FPC	HB-PPC
η_{conv}	96.23 %	84.8 %
η_{sys}	96.23 %	96.23 %
P_{cond}	6.5 W	6.5 W
P_{sw}	50 W	50 W
K_{pr}	1	0.248

offer any improvement in terms of current or voltage reduction. It results in FPP rather than PPP.

Table 3.3 presents the obtained power losses, efficiency and K_{pr} results from the simulations. There, the correlation between the converter-system efficiency and the K_{pr} is observed. Although the HB-FPC presents a higher η_{conv} than the HB-PPC, both

solutions achieve the same η_{sys}. As it can be observed, the same amount of power losses are achieved with the HB-FPC and the HB-PPC.

To explain the reason for not achieving improvements with a PPP-based HB topology, Fig. 3.4 simplifies its configuration into a three-pole converter. Since the HB contains its two negative ports connected to each other ("In-" and "Out-" from Fig. 3.2), the HB can be represented as a three-pole converter, see Fig. 3.4a. On the other hand, the electrical circuit of the single inductor HB can be simplified as in Fig. 3.4b, where the inductor voltage is defined by two switching states, given by (3.2).

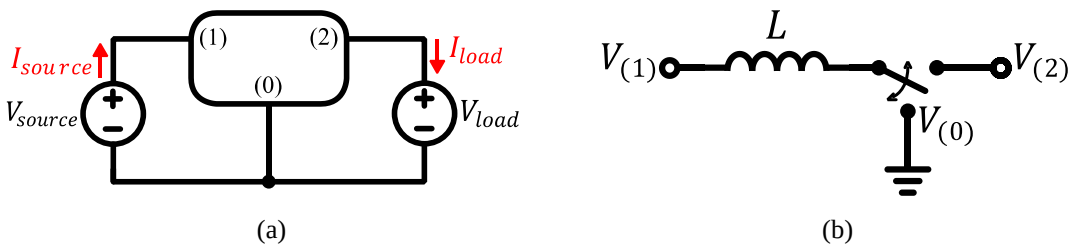
$$V_L = \begin{Bmatrix} \text{State 1: } V_{(1)} - V_{(0)} \\ \text{State 2: } V_{(1)} - V_{(2)} \end{Bmatrix} \tag{3.2}$$

Where, $V_{(0)}$, $V_{(1)}$ and $V_{(2)}$ are the voltage at ports (1), (2) and (3) in Fig. 3.4a.

Substituting $V_{(0)}$, $V_{(1)}$ and $V_{(2)}$ by their corresponding values from Table 3.2, equations (3.3),(3.4) demonstrate that the HB-FPC and the HB-PPC obtain the same absolute inductor voltage. In consequence, the current through the inductor results into the same, as it can be observed in Fig. 3.3a.

$$V_{L_{HB-FPC}} = \begin{Bmatrix} V_{(1)} - V_{(0)} = 100 - 0 = 100\ \text{V} \\ V_{(1)} - V_{(2)} = 100 - 125 = -25\ \text{V} \end{Bmatrix} \tag{3.3}$$

$$V_{L_{HB-PPC}} = \begin{Bmatrix} V_{(1)} - V_{(0)} = 25 - 0 = 25\ \text{V} \\ V_{(1)} - V_{(2)} = 25 - 125 = -100\ \text{V} \end{Bmatrix} \tag{3.4}$$



(a) (b)

Fig. 3.4. (a) Diagram of a three-pole converter. (b) Simplified electrical circuit of a single inductor HB.

3.3 Double Inductor Case Study

The second topology to compare is the MSIBC. The MSIBC is also implemented on a FPC architecture (MISBC-FPC, Fig. 3.5a) and a on a FCC type PPC architecture (MSIBC-PPC, Fig. 3.5b). Fig. 3.5c shows the switching sequence of the MSIBC in buck and boost mode. As it can be observed, inductors L_1 and L_2 are connected in parallel when Q_1, Q_2 and Q_3 turn on, and in series when Q_4 and Q_5 turn on. Note that the polarity of L_1 and L_2 is inverted from Fig. 3.5a to Fig. 3.5b.

Table 3.4 presents the system level electrical parameters. Compared to the single inductor case study, the source and load voltages are kept the same to ensure a K_{pr} value bellow 1. P_{load} is halved for manufacturability issues with the experimental prototype. Table 3.5 defines the design parameters of the MSIBC-FPC and the MSIBC-PPC. As it can be observed, the input-output voltage values and the operation mode of the power

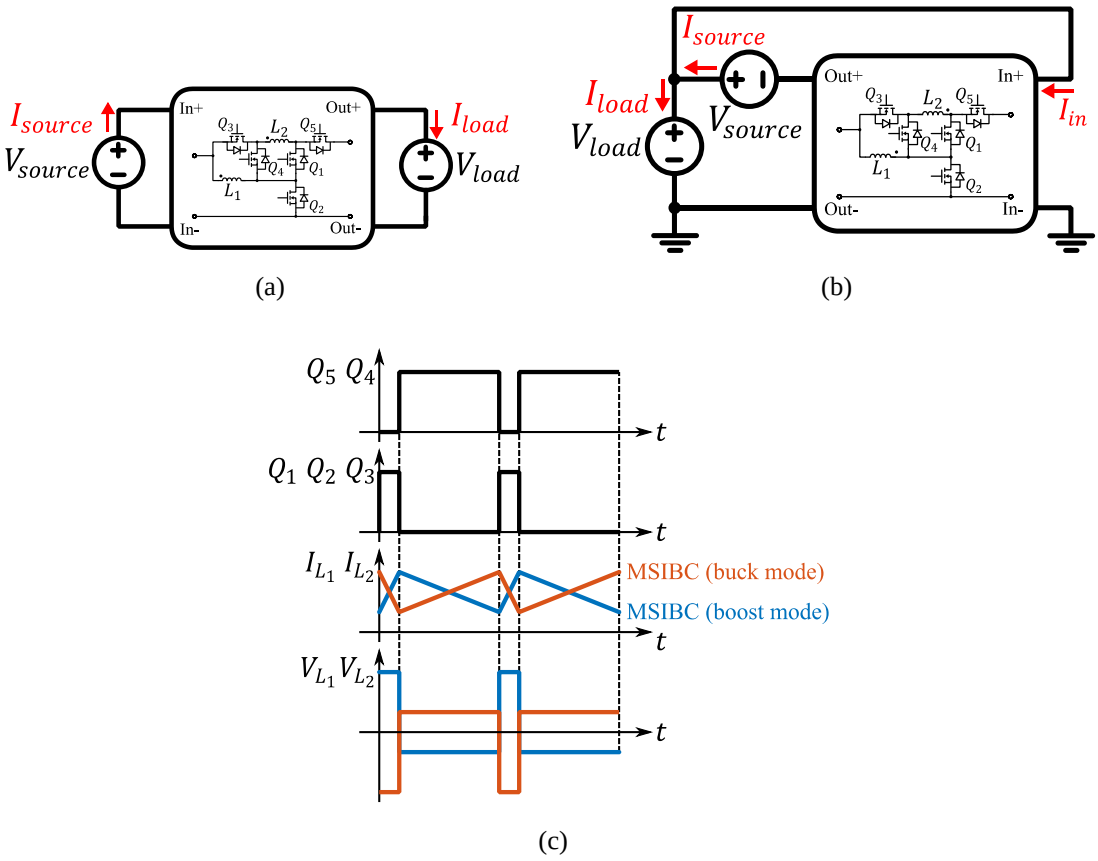


Fig. 3.5. Double inductor case study. (a) MSIBC-FPC. (b) MSIBC-PPC. (c) Switching sequence of the MSIBC in buck and boost mode.

Table 3.4. System level electrical parameters for the double inductor case study.

Parameter	Value
V_{source}	100 V
V_{load}	125 V
G_V	1.25
P_{load}	0.75 kW

Table 3.5. Converter level design parameters for the double inductor case study.

Parameter	Value	
	MSIBC-FPC	MSIBC-PPC
V_{in}	100 V	125 V
V_{out}	125 V	25 V
Operation mode	Boost	Buck
K_{pr}	1	0.25
P_{conv}	0.75 kW	0.187 kW
f_{sw}	50 kHz	50 kHz
L	75 µH	75 µH
C	200 µF	200 µF
Q_{1-2}	IPT65R033G7[10]	IPT65R033G7[9]

converter vary from the MSIBC-FPC to the MSIBC-PPC. When it comes to the passive and active components, same devices are implemented in both solutions.

Applying the three pole analysis on the MSIBC, equation (3.5) is obtained. In this case, the inductor voltage is divided by two at the second switching state. This is because both inductors are connected in series.

$$V_{L_1,L_2} = \begin{Bmatrix} \text{State 1: } V_{(1)} - V_{(0)} \\ \text{State 2: } \dfrac{V_{(1)} - V_{(2)}}{2} \end{Bmatrix} \quad \textbf{(3.5)}$$

Substituting $V_{(0)}$, $V_{(1)}$ and $V_{(2)}$ by their corresponding values from Table 3.5, equations (3.6),(3.7) show that the inductors from the MSIBC-FPC and the MSIBC-PPC

[10] V_{DS}=650 V, R_{DS}=29 mΩ @T_j=25 ºC

observe different voltage values. This will directly have an effect on their currents. To confirm this, the MSIBC-FPC and the MSIBC-PPC are simulated.

$$V_{L_{MSIBC-FPC}} = \left\{ \begin{matrix} V_{(1)} - V_{(0)} = 100 - 0 = 100\ \text{V} \\ \dfrac{V_{(1)} - V_{(2)}}{2} = \dfrac{100 - 125}{2} = -12.5\ \text{V} \end{matrix} \right\} \quad \textbf{(3.6)}$$

$$V_{L_{MSIBC-PPC}} = \left\{ \begin{matrix} V_{(1)} - V_{(0)} = 25 - 0 = 25\ \text{V} \\ \dfrac{V_{(1)} - V_{(2)}}{2} = \dfrac{25 - 125}{2} = -50\ \text{V} \end{matrix} \right\} \quad \textbf{(3.7)}$$

3.3.1 Simulation Results

The simulations do only consider semiconductors' conduction and switching losses. The latter are obtained from previously characterized curves. The implemented control in the simulations is an open loop.

Fig. 3.6 presents the current/voltage steady state waveforms of the inductors and the output capacitor. Fig. 3.6a shows that a 1.45 times lower inductor RMS current is obtained with the MISBC-PPC: 6.8 A (MSIBC-FPC case) and 4.67 A (MSIBC-PPC case). This directly affects the current that the semiconductors handle. Fig. 3.6b presents the output capacitor current/voltage steady state waveforms. In this case, the resulting capacitor RMS current of the MSIBC-PPC is two times higher than the one of the MSIBC-FPC: 4.72 A and 2.27 A, respectively. Consequently, for the same capacitance value, the output voltage ripple is higher at the MSIBC-PPC. In short, in the MSIBC-

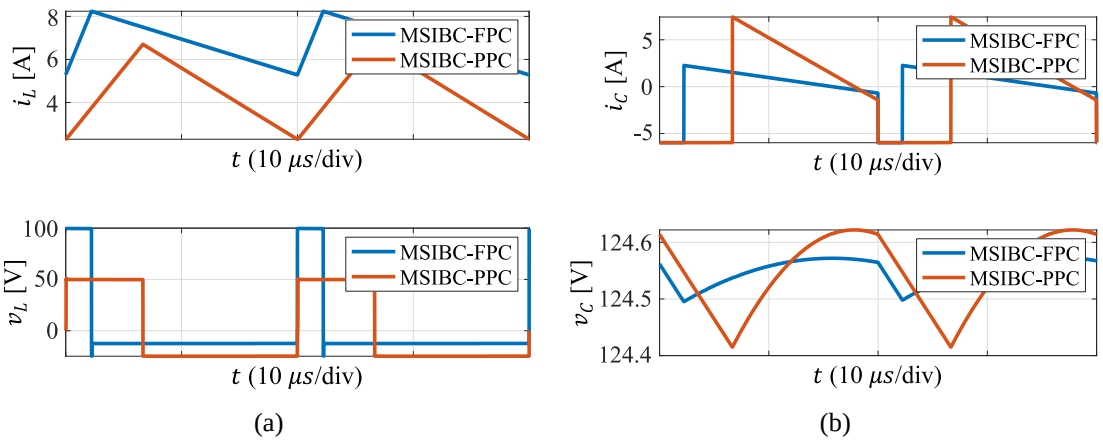


Fig. 3.6. Current and voltage steady state waveforms in the double inductor case study. (a) Inductor. (b) Capacitor.

Table 3.6. Power losses, efficiency and K_{pr} results of the double inductor case study.

Parameter	Value	
	MSIBC-FPC	MSIBC-PPC
η_{conv}	94.89 %	88.31 %
η_{sys}	94.89 %	97.1 %
P_{cond}	3.3 W	0.66 W
P_{sw}	35 W	21 W
K_{pr}	1	0.248

PPC, the current through the inductors is reduced, whereas the output capacitor current is increased.

Table 3.6 shows the obtained power losses, efficiency and K_{pr} results. The converter efficiency of the MSIBC-FPC is higher than with the MSIBC-PPC. However, this percentage corresponds to the low converter power of the MSIBC-PPC. Comparing the system efficiency, the MSIBC-PPC achieves a higher value. Indeed, its losses are 1.76 times lower than the MSIBC-FPC. Therefore, simulations conclude that the MSIBC topology can improve its performance by implementing it on a FCC type PPC architecture.

3.4 Experimental Results

In order to validate the simulation results, four experimental prototypes are assembled and tested: HB-FPC, HB-PPC, MSIBC-FPC and MSIBC-PPC. The first two correspond to the single inductor case study and the last two to the double inductor case study.

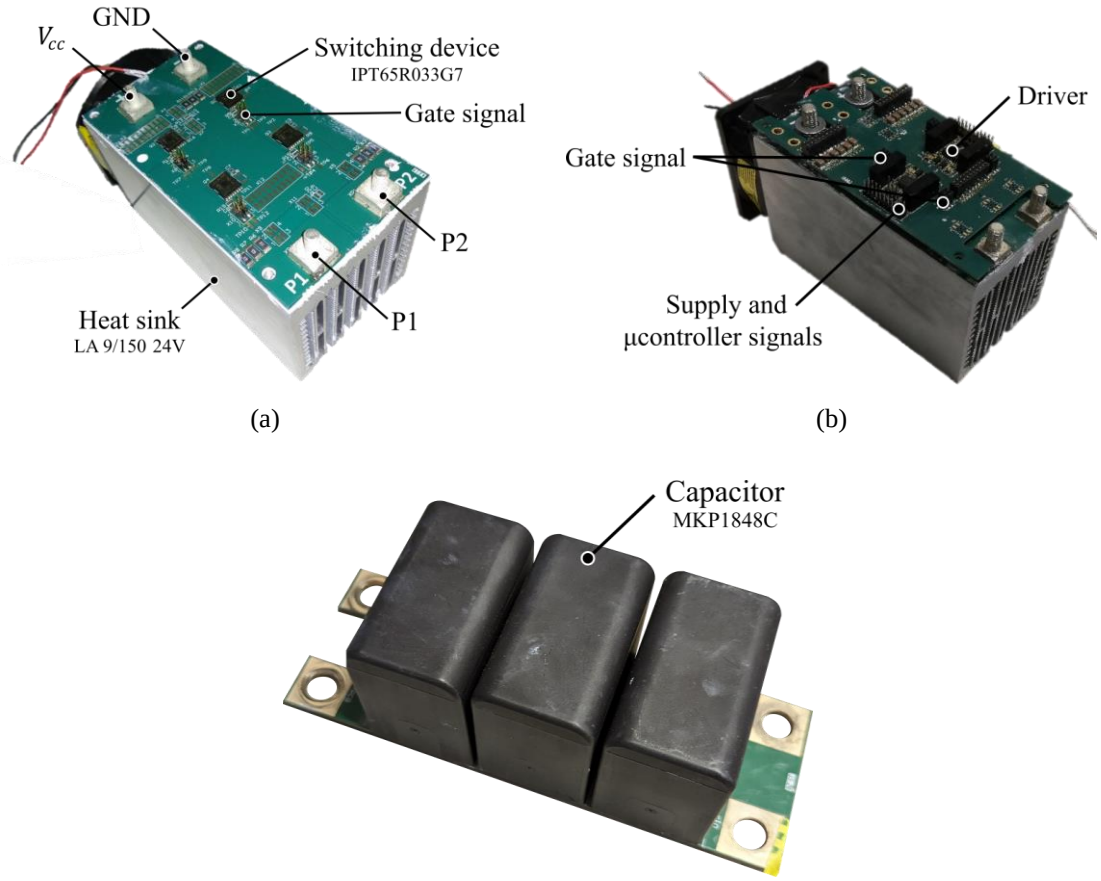
3.4.1 Prototypes Design

Regarding the design of the experimental prototypes, the same values presented in Table 3.2 (single inductor case) and Table 3.5 (double inductor case) are selected.

When it comes to the inductors, two different designs are assembled in the laboratory: a single 150 µH inductance (Fig. 3.7a) and two 75 µH inductances (Fig. 3.7b). The 150 µH inductance corresponds to the HB and the 75 µH inductances to the MSIBC.

(a) (b)

Fig. 3.7. Assembled inductances. (a) Single inductor case study (L=150 µH and R_L=26 mΩ). (b) Double inductor case study (L=75 µH and R_L=31 mΩ).



(a) (b)

(c)

Fig. 3.8. Assembled FB prototype. (a) Power layer. (b) Driver layer. (c) Capacitor PCB.

For the magnetic cores, a PM8770H and a PM6249 have been used respectively (both cases with CF139 ferrite).

Fig. 3.8 shows the assembled full-bridge (FB) for the experimental tests. Fig. 3.8a presents the power PCB layer, which contains the power connectors and the four

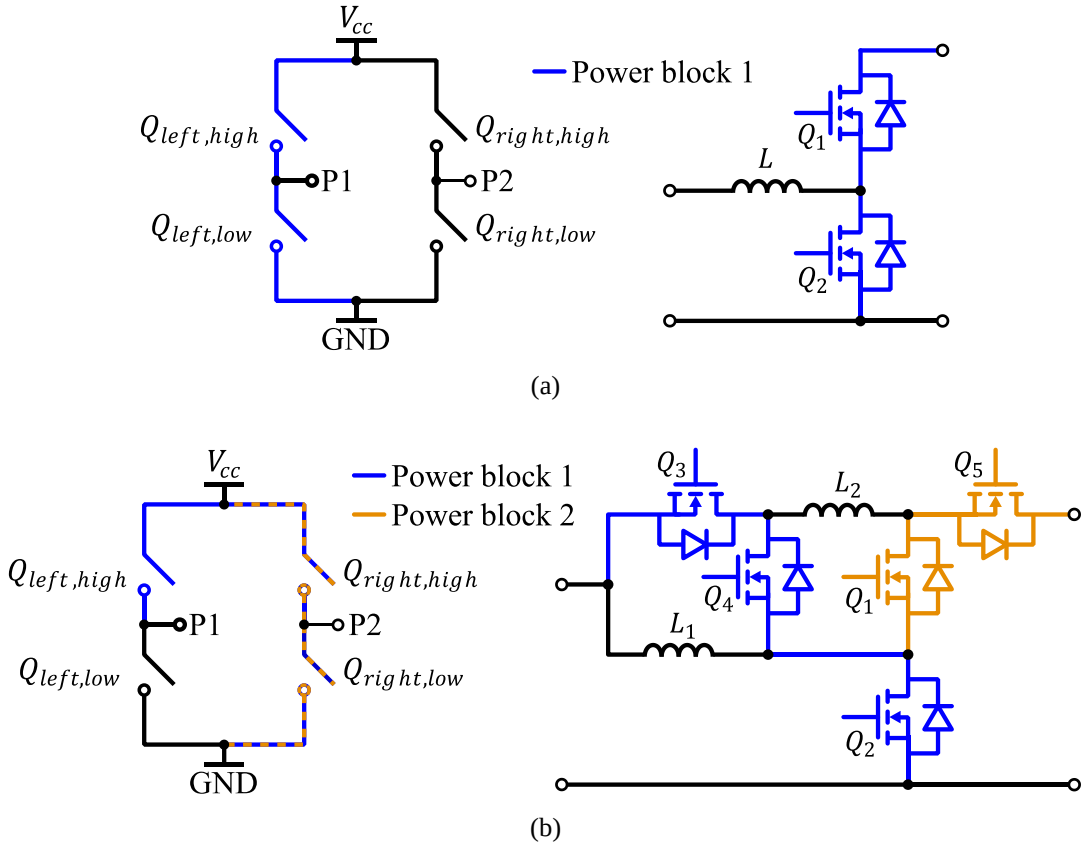


Fig. 3.9. FB configuration. (a) HB. (b) MSIBC.

semiconductors. The designed power PCB is based on insulated metal substrate (IMS) technology and it allows better thermal transference than a traditional FR4. Fig. 3.8b shows the driver PCB layer, which contains the drivers and the supplies to adapt the signals coming from the micro-controller to the gate of the semiconductors. Apart from that, an external PCB is added to increase the capacitance of the input-output DC filter, see Fig. 3.8c.

Fig. 3.9 details the configuration implemented for each solution. In the case of the HB (Fig. 3.9a), a single branch is required. Therefore, $Q_{left,high}$ and $Q_{left,low}$ act as Q_1 and Q_2. $Q_{right,high}$ and $Q_{right,low}$ are not used. On the other hand, the MSIBC topology contains 5 semiconductors. So, two power blocks are needed:

- Power block 1: $Q_{left,high}$, $Q_{right,high}$ and $Q_{right,low}$ act as Q_3, Q_4 and Q_2, respectively. These are coloured in blue in Fig. 3.9b.
- Power block 2: $Q_{right,high}$ and $Q_{right,low}$ act as Q_5 and Q_1. These are coloured in orange in Fig. 3.9b.

Of course, the resulting layout of the MSIBC is not optimized, which will have a negative impact on its performance. However, this will affect similarly to the MSIBC-FPC and the MSIBC-PPC.

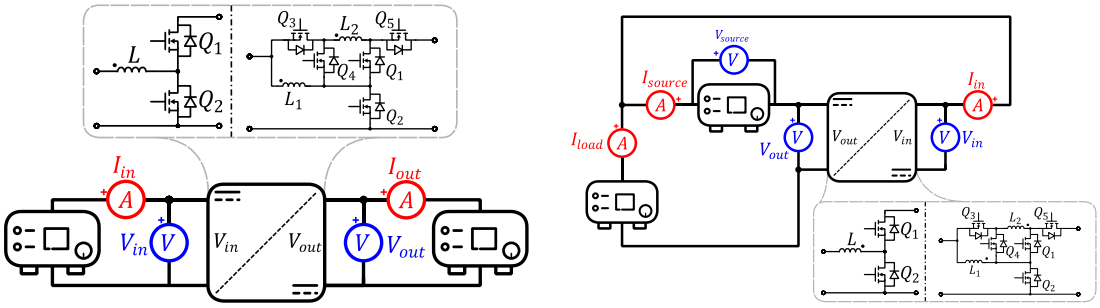
3.4.2 Description of the Experimental Set-Up

Fig. 3.10 shows a simplified electrical diagram of how each of the FPC and PPC solutions are mounted and measured. Fig. 3.10a presents the FPC set-up and its corresponding current and voltage measures. In this case, the system and converter current/voltage coincide. So, just two voltage and two current measures are necessary:

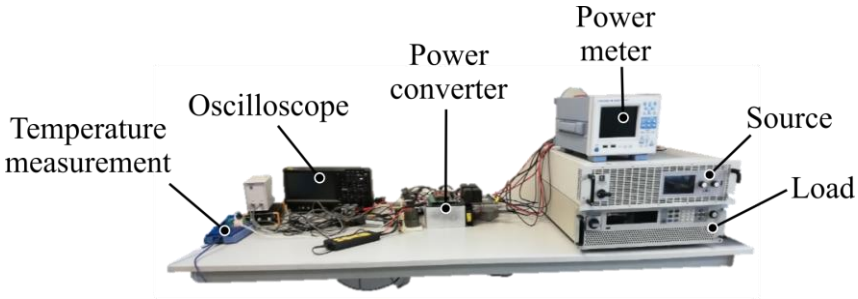
- V_{in} and V_{out}, which also represent V_{source} and V_{load}.
- I_{in} and I_{out}, which also represent I_{source} and I_{load}.

In the case of the FCC architecture (Fig. 3.10b), 3 voltage and 3 current measures are required:

- V_{source}, V_{out} and V_{in}, this last one coincides with V_{load}.
- I_{load}, I_{in} and I_{source}, this last one coincides with I_{out}.



(a) (b)



(c)

Fig. 3.10. Experimental set-up. (a) FPC configuration. (b) FCC type PPC configuration. (c) Real image.

Apart from that, the current through the inductor and the top-case temperature of each semiconductor are measured. Fig. 3.10c shows a real image of the experimental set-up.

3.4.3 Experimental Results

Single inductor case study

Fig. 3.11 shows the experimental steady state inductor current and semiconductor voltage of the HB-FPC and the HB-PPC. Concerning the inductor current, both solutions present exactly the same waveforms. As in the simulations, there is no inductor current reduction when implementing the HB-PPC. Also, when it comes to the semiconductor voltage, similar waveforms are obtained with the HB-FPC and the HB-PPC. Analysing in detail the overshoot, the HB-PPC provokes higher values.

Table 3.7 presents the experimental power losses, efficiency and K_{pr} values. Compared to the simulation results from Table 3.3, higher conduction losses are achieved. This is mainly due to the inherent resistance of the inductor. It can also be observed that the system efficiency of the HB-FPC and the HB-PPC are the same. Indeed, there exists just a negligible difference of 0.2 %. In conclusion, it is experimentally demonstrated that a single inductor topology, such as the HB, does not improve its performance when it is

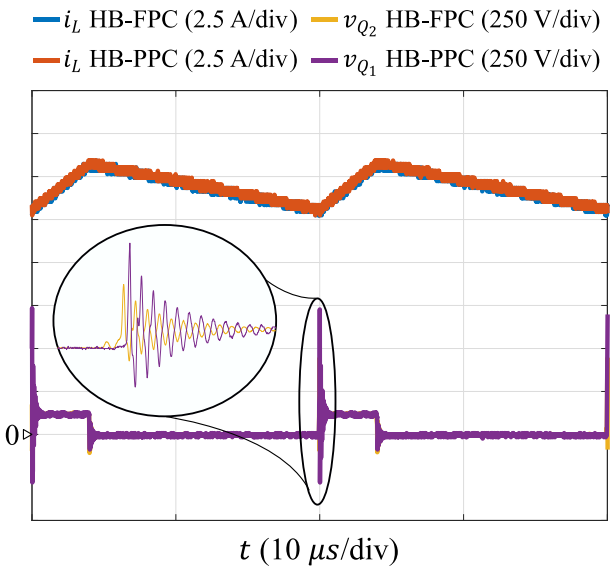


Fig. 3.11. Experimental inductor current and semiconductor voltage obtained with the HB-FPC and the HB-PPC.

Table 3.7. Experimental power losses, efficiency and K_{pr} results obtained with the single inductor case study.

Parameter	Value	
	HB-FPC	HB-PPC
η_{conv}	95.93 %	84.27 %
η_{sys}	95.93 %	96.13 %
P_{cond}	11.36 W	11.49 W
P_{sw}	49.63 W	46.5 W
K_{pr}	1	0.246

implemented on a FCC type PPC architecture. So, it cannot be considered as a PPP solution.

Double inductor case study

Fig. 3.12 presents the steady state inductor current obtained with the MSIBC-FPC and the MSIBC-PPC. As it can be observed, the obtained current waveforms are very similar to the ones presented in the simulations (Fig. 3.6a). Indeed, the RMS current with the MSIBC-FPC is around 6.45 A, whereas with the MSIBC-PPC is 4.62 A.

With the aim of observing the effect of this on the semiconductors, the top-case temperature of each device is measured. Fig. 3.13a (MSIBC-FPC case) and Fig. 3.13b (MSIBC-PPC case) present the results until the steady state temperature is achieved. In both solutions, there is a critical semiconductor that heats easier than the rest of the components. In the case of the MSIBC-FPC, the semiconductor that heats the most is Q_1, achieving a maximum temperature of 50 °C. The next semiconductor heats up to 28 °C. When it comes to the MSIBC-PPC, Q_3 is the most critical semiconductor, which achieves

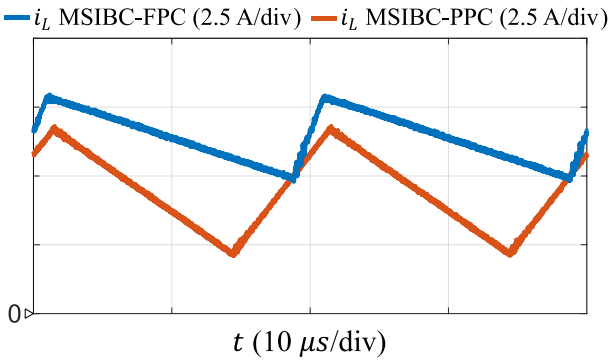


Fig. 3.12. Experimental inductor current obtained with the MSIBC-FPC and the MSIBC-PPC.

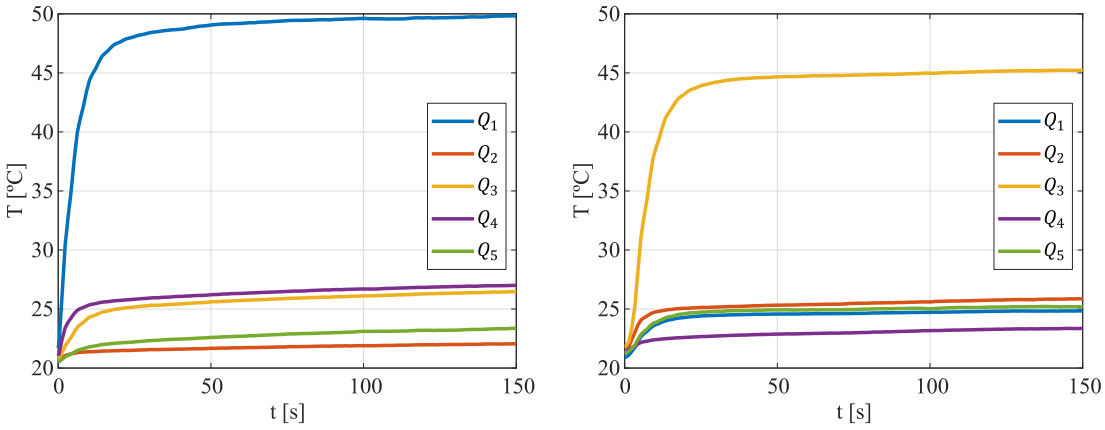


Fig. 3.13. Semiconductors' top-case temperature evolution. (a) MSIBC-FPC. (b) MSIBC-PPC.

Table 3.8. Experimental power losses, efficiency and K_{pr} results obtained with the double inductor case study.

Parameter	Value	
	MSIBC-FPC	MSIBC-PPC
η_{conv}	94.67 %	86.9 %
η_{sys}	94.67 %	96.8 %
P_{cond}	5.63 W	3.38 W
P_{sw}	34.36 W	20.61 W
K_{pr}	1	0.245

a maximum temperature of 45.8 °C (5 °C less than Q_1 in the MSIBC-FPC). The rest of the semiconductors barely reach 25 °C. These results confirm that the switching devices suffer a lower thermal stress in the MSIBC-PPC than in the MSIBC-FPC.

Finally, Table 3.8 shows the experimental power losses, efficiency and K_{pr} results. Implementing the MSIBC topology on a PPC architecture, both the conduction losses and the switching losses are reduced by 40 %. Although the converter efficiency of the MSIBC-PPC is poor, its system efficiency is two points higher than the one of the MSIBC-FPC. This confirms the importance of differentiating the converter and system efficiency in PPC-based solutions.

In conclusion, a MSIBC topology reduces the inductor RMS current, decreases the thermal stress of the switching devices, and improves the system efficiency. So, it can achieve PPP.

3.5 Conclusion

This Chapter studies the possibility of achieving PPP with DC-DC non-isolated topologies. It is concluded that the conventional HB topology performs equally on FPC and PPC architectures. No benefits are observed by implementing it on a FCC architecture. Neither the inductor current nor the power losses are reduced. This is demonstrated via simulations and experimental results.

Regarding the MSIBC, both simulation and experimental results demonstrate that a MSIBC-PPC has improved performance than a MSIBC-FPC. This supposes a first step in the PPC literature regarding the analysis of the benefits of non-isolated topology based PPC architectures. However, the next points should be cleared out:

- In order to ensure a K_{pr} bellow 1, the application under analysis fixes a G_V value of 1.25. The MSIBC is presented as a "DC-DC converter recommended to achieve high voltage" and authors from [96] test it for G_V values around 4. Table 3.9 compares the static voltage gain observed by the converter through this work. In the MSIBC-PPC case, the result of $G_{V_{conv}}$ is inverted due to its buck operation mode. As it can be seen, the MSIBC-FPC observes a 1.25 gain, whereas the MSIBC-PPC observes a 5 gain. Therefore, the considered application does not benefit the MSIBC-FPC.

- Comparing the performance of the MSIBC-PPC and the conventional HB-FPC, a slight 0.7 % efficiency improvement is observed. However, this is not a meaningful comparison. Indeed, the power of the MSIBC-PPC is limited to 750 W because its semiconductors easily heated to 100 ºC during the experimental 1.5 kW test. So, although the MSIBC-PPC outperforms its analogous FPC, it does not outperform a conventional HB-FPC. Furthermore, the HB-FPC just requires a single inductor and 2 switching devices.

Table 3.9. Static voltage gain of the converter in both solutions.

MSIBC-FPC $\left(G_{V_{conv}} = \frac{V_{out}}{V_{in}}\right)$	MSIBC-PPC $\left(\frac{1}{G_{V_{conv}}} = \frac{V_{in}}{V_{out}}\right)$
1.25	5

Taking into account these conclusions, the next future lines are proposed for further research:

1. Search for additional non-isolated topologies that present improved performance in PPC architectures than in FPC.
2. Demonstrate if a PPC-based non-isolated topology can outperform a conventional single inductor HB-FPC.

After this Chapter, the analysis of PPC architectures is focused on the IPOS-ISOP type architectures. This type of solutions require the implementation of galvanically isolated topologies.

Chapter 4

PARTIAL POWER CONVERTERS THAT REQUIRE ISOLATED TOPOLOGIES

This Chapter studies the benefits that IPOS-ISOP type PPC architectures bring in comparison to FPC based solutions. To this end, two case studies are presented:

1. *Isolated topology based PPC vs. non-isolated topology based FPC. This study aims to observe if an isolated topology with reduced power level has a better performance than a full power non-isolated topology.*
2. *Si-based PPC vs. SiC-based FPC. This study aims to research the new benefits that PPC architectures bring to Si devices compared to WBG technologies.*

Both studies include simulation and experimental results.

The power losses model and the second case study presented in this Chapter correspond to the article in revision [J4].

4.1 Motivation, Investigated Topologies

As concluded in subchapter 2.1.2, the PPC architectures that require isolated topologies can be summarized in two architectures: the IPOS (optimal for voltage boost applications, Fig. 4.1a) and the ISOP (optimal for voltage buck applications, Fig. 4.1b). Although both architectures require an isolated topology, this type of solutions cannot be considered as galvanically isolated. This is because the grounds of V_{source} and V_{load} must be connected to each other. Therefore, the performance of IPOS-ISOP type PPC architectures should be compared with that of a non-isolated FPC solution.

This Chapter presents two different case studies where an IPOS-ISOP type PPC architecture is compared to a FPC based solution:

1. **IPOS-ISOP type PPC vs. non-isolated topology based FPC.** This study compares the performance of an isolated topology based PPC to a non-isolated topology based FPC. The main objective of this study is to observe if an isolated topology with reduced power level has a better performance than a full power non-isolated topology.
2. **Si-based PPC vs. SiC-based FPC.** This study compares the performance of a Si-based DAB-PPC to a SiC-based DAB-FPC. Although a non-isolated solution (DAB-PPC case) is compared to an isolated solution (DAB-FPC case), the main objective of this study is to research the new benefits that PPP brings to Si devices compared to WBG technologies.

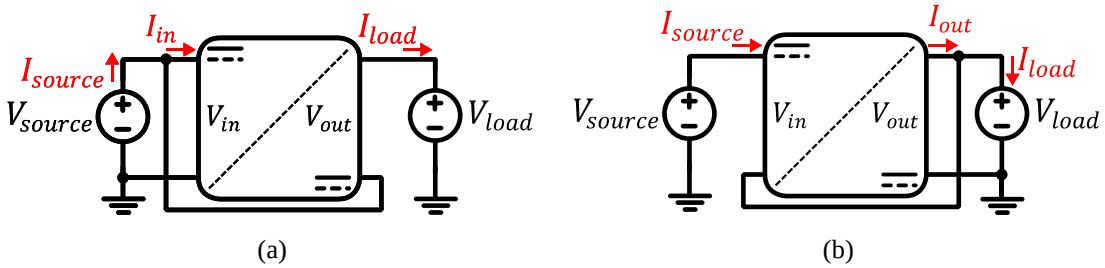


Fig. 4.1. PPC architectures that require isolated topologies. (a) IPOS. (b) ISOP.

4.2 IPOS-ISOP Type PPC vs. Non-Isolated Topology Based FPC

Since IPOS-ISOP type PPC architectures cannot be considered as galvanically isolated solutions, the major challenge that they face is to improve the performance of non-isolated based FPCs. Usually, non-isolated topologies require a lower number of components and result in more simple circuits. However, the literature does not present extended information on this topic. For example, authors from [29], [40], [65], [97], [98] compare the results of an isolated topology by implementing it in a PPC and a FPC architecture. This way, the comparison consists of an isolated solution (FPC case) against a non-isolated solution (PPC case), which is not completely fair. The only two articles that compare a PPC architecture against a non-isolated FPC are [92], [99]. In [92] authors compare a full-bridge phase-shifted PPC (FBPS-PPC) against a conventional boost converter. The authors conclude that despite the FBPS-PPC prototype has a greater number of components, it is more efficient than the conventional boost converter. Authors from [99] analyze a buck-boost application. For this purpose, they compare a full-bridge push-pull PPC (FBPP-PPC) against a two-switch buck-boost (TSBB). Authors from [99] also conclude that the FBPP-PPC is superior to TSBB in terms of efficiency and dynamic response.

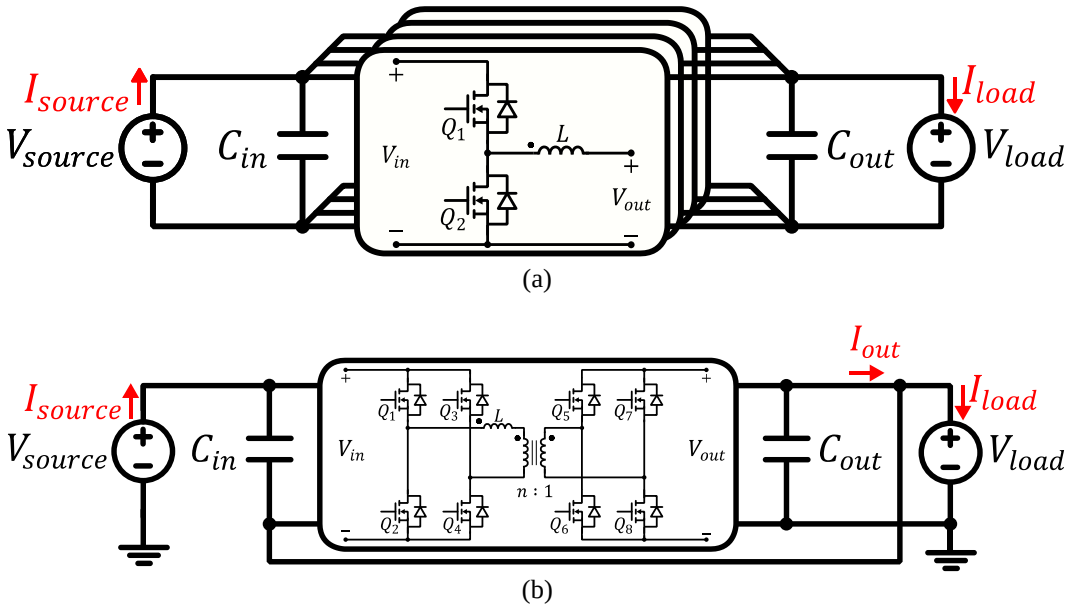


Fig. 4.2. Comparison under analysis. (a) IHB-FPC. (b) DAB-PPC.

Following the analysis from [92], [99], the present Chapter extends the comparison between an IPOS-ISOP type PPC and a non-isolated FPC. The two solutions under analysis are shown in Fig. 4.2a (interleaved HB FPC, IHB-FPC) and Fig. 4.2b (dual active bridge PPC, DAB-PPC). In the case of the IHB-FPC, four converters are connected in parallel to equal in number of semiconductors.

4.2.1 System Description

Table 4.1 defines the main system parameters of the application under analysis. As it can be observed, it consists of a constant DC source and a variable load. The load power can have a positive flow (P_{load}=+2.5 kW) or negative flow (P_{load}=−2.5 kW). A positive value of P_{load} means that the power flows from V_{source} to V_{load}, thus buck operation mode. A negative value means that the power flows from V_{load} to V_{source}, thus boost operation mode.

The design parameters of the converters are detailed in Table 4.2. The first noticeable difference between the two solutions is V_{in}. In the case of the DAB-PPC, a maximum voltage of 75 V is expected, which permits the implementation of better conducting semiconductors in the primary side bridge (Q_{1-4}). The maximum power processed by the converter ($\widehat{|P_{conv}|}$) is four times lower in the DAB-PPC. Although each IHB-FPC module processes 0.625 kW, the total power processed by the converter is equal to P_{load}. The frequency seen by C_{out} is the same for both solutions. This provokes a different switching frequency (f_{sw}) in each solution. The switching frequency of the IHB-FPC is the result of the division between the frequency seen by C_{out} and the number of modules connected in parallel. The switching frequency of the DAB-PPC is half of the frequency seen by C_{out}. Finally, three different transformer turn ratios (n) are defined for the DAB-PPC. The objective of this is to analyze the effect of n on the performance of the converter.

Table 4.1. System parameters.

Parameter	Value
V_{source}	300 V
V_{load}	From 225 V to 300 V
P_{load}	±2.5 kW

Table 4.2. Design parameters.

Parameter	Value			
	IHB-FPC	DAB-PPC		
V_{in}	300 V	From 75 V to 0 V		
V_{out}	From 225 V to 300 V	From 225 V to 300 V		
K_{pr}	1	From 0.25 to 0		
$\lvert\widehat{P_{conv}}\rvert$	4x0.625 kW	0.625 kW		
f_{sw}	20 kHz	40 kHz		
Frequency seen by C_{out}	80 kHz	80 kHz		
C_{in}	200 µF	200 µF		
C_{out}	300 µF	300 µF		
n	-	0.1	0.2	0.3
L	200 µH (per module)	7.5 µH	15 µH	22.5 µH
Q_{1-4}	IPBE65R075CFD7A[11]	IRFS4115-7P[12]		
Q_{5-8}	IPBE65R075CFD7A[11]	IPBE65R075CFD7A[11]		

Each value of n is defined by applying expression (4.1), which ensures a low inductor RMS current. At an initial working condition, where V_{in}=75 V and V_{out}=225 V, the optimal n value is 0.33 (rounding off to 0.3). At an intermediate point, where V_{in}=50 V and V_{out}=250 V, the optimal n value is 0.2. Finally, if V_{in}=25 V and V_{out}=275 V, the optimal n value is 0.099 (rounding off to 0.1).

$$M = \frac{V_{in}}{V_{out} \cdot n} = 1 \tag{4.1}$$

4.2.2 Power Converter Model

Numerical simulations are performed with a MATLAB script to model both solutions: IHB-FPC and DAB-PPC.

[11] V_{DS}=650 V , R_{DS}=139 mΩ @T_j=150 ºC
[12] V_{DS}=150 V , R_{DS}=35 mΩ @T_j=150 ºC

4.2.2.1 IHB-FPC

In the first place, the steady state current and voltage waveforms of the inductor are obtained. Assuming that the IHB-FPC works in continuous conduction mode (CCM), two switching states are analyzed, see Fig. 4.3.

Time interval $0 < t \leq D \cdot T_s$

The high side semiconductor Q_1 is conducting, while Q_2 blocks the input voltage. As a result, the inductor observes the voltage difference between V_{in} and V_{out}. Expression (4.2) defines the inductor current in function of time.

$$i_L(t) = \frac{v_L(t)}{L} \cdot (t - t_0) + i_L(t_0) = \frac{V_{in} - V_{out}}{L} \cdot (t - 0) + i_L(0) \qquad \textbf{(4.2)}$$

Where, $i_L(0)$ is the initial value of the current, which is given by (4.3).

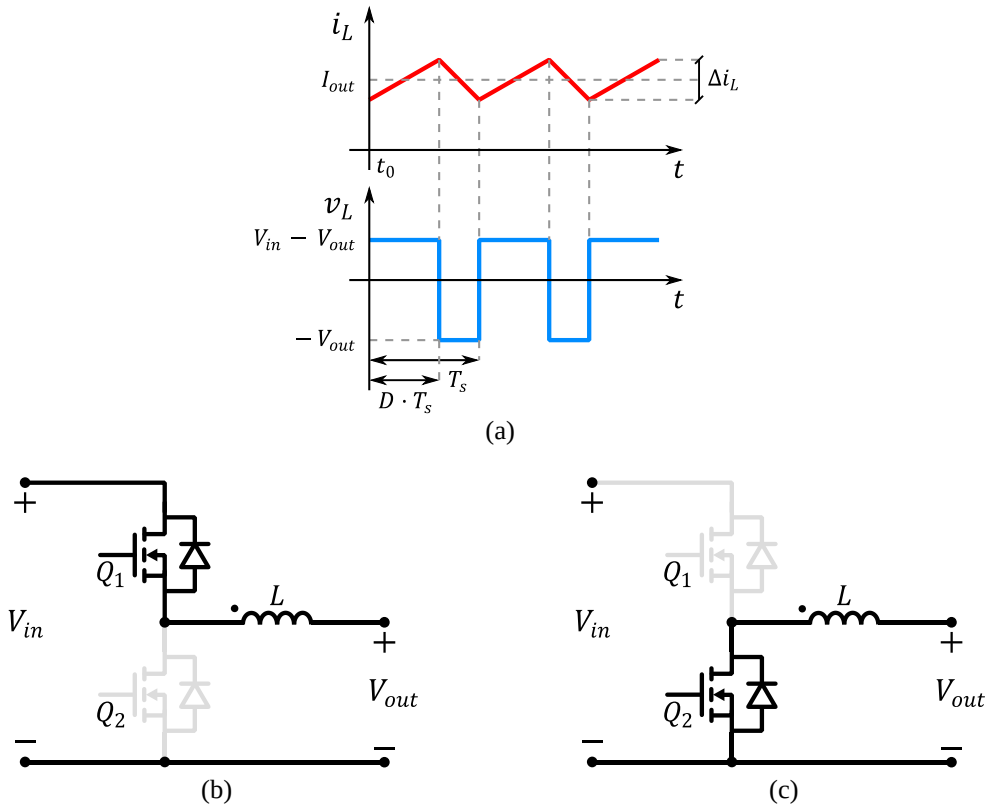


Fig. 4.3. (a) Typical steady state inductor current and voltage waveforms of an IHB-FPC in buck mode. (b) Time interval $0 < t \leq D \cdot T_s$. (c) Time interval $D \cdot T_s < t \leq T_s$.

$$i_L(0) = I_{out} - \frac{\Delta i_L}{2} = \frac{I_{load}}{N_{mod}} - \frac{V_{in} - V_{out}}{2 \cdot L} \cdot D \cdot T_s \quad \textbf{(4.3)}$$

N_{mod} is the number of IHB-FPC modules connected in parallel, N_{mod}=4.

Time interval $D \cdot T_s < t \leq T_s$

In this case, Q_1 turns off and Q_2 turns on, provoking a negative voltage in the inductor ($-V_{out}$). Expression (4.4) defines the inductor current in function of time.

$$i_L(t) = \frac{v_L(t)}{L} \cdot \left(t - t_{D \cdot T_s}\right) + i_L(t_{D \cdot T_s}) = \frac{-V_{out}}{L} \cdot (t - D \cdot T_s) + i_L(D \cdot T_s) \quad \textbf{(4.4)}$$

Where, $i_L(D \cdot T_s)$ is the last value from the previous time interval.

Semiconductors and capacitors

Once the steady state waveform of the inductor current is defined, the steady state waveforms of the rest of the components is obtained. Expressions (4.5)-(4.8) describe the current and voltage waveforms of Q_1 and Q_2. The same equations are applied for the rest of the semiconductors, but considering a current phase-shift of 90º (ϕ=360º/N_{mod}).

On the other hand, expressions (4.9)-(4.10) describe the current and voltage waveforms of the output capacitor.

$$i_{Q_1}(t) = \begin{cases} i_L(t) & 0 < t \leq D \cdot T_s \\ 0 & D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.5)}$$

$$i_{Q_2}(t) = \begin{cases} 0 & 0 < t \leq D \cdot T_s \\ -i_L(t) & D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.6)}$$

$$v_{Q_1}(t) = \begin{cases} 0 & 0 < t \leq D \cdot T_s \\ V_{in} & D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.7)}$$

$$v_{Q_2}(t) = \begin{cases} V_{in} & 0 < t \leq D \cdot T_s \\ 0 & D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.8)}$$

$$i_{C_{out}}(t_i) = i_{L_{eq}}(t_i) - I_{load} \quad \textbf{(4.9)}$$

$$v_{C_{out}}(t_i) = \frac{i_{C_{out}}(t_i)}{C_{out}} \cdot T_{ss} + v_{C_{out}}(t_{i-1}) \quad \textbf{(4.10)}$$

Where, T_{ss} is the time step of the numerical simulation (T_{ss}<<T_s), t_i is the time at the i^{th} time instant and $i_{L_{eq}}$ is the sum of the inductors' current.

4.2.2.2 DAB-PPC

Due to its ease of implementation, the modulation selected for the DAB-PPC is the PSM. Therefore, four different switching states are considered, see Fig. 4.4.

Time interval $0 < t \leq d \cdot D \cdot T_s$

In the primary side, the semiconductors $Q_{1,4}$ start conducting and $Q_{2,3}$ are turned off blocking the input voltage. In the secondary side, the semiconductors $Q_{6,7}$ are turned on and $Q_{5,8}$ are turned off blocking the output voltage. The resulting voltage at the inductor is the sum of V_{in} and $V_{out} \cdot n$. The term $V_{out} \cdot n$ represents the output voltage referred to the primary side. Expression (4.11) defines the inductor current in function of time.

$$i_L(t) = \frac{v_L(t)}{L} \cdot (t - t_0) + i_L(t_0) = \frac{V_{in} + V_{out} \cdot n}{L} \cdot (t - 0) + i_L(0) \quad \textbf{(4.11)}$$

Where, $i_L(0)$ is the initial value of the current (4.12) [100].

$$i_L(0) = \frac{\Delta i_L}{2} = \frac{V_{out} \cdot n - V_{in} - 2 \cdot V_{out} \cdot n \cdot d}{4 \cdot f_{sw} \cdot L} \quad \textbf{(4.12)}$$

Where, d represents the phase-shift and it goes from 0 (0º) to 0.5 (90º).

Time interval $d \cdot D \cdot T_s < t \leq D \cdot T_s$

The primary side semiconductors remain in their switching state. In the secondary side, the semiconductors $Q_{6,7}$ are turned off and $Q_{5,8}$ are turned on. As a result, the inductor observes the voltage difference between V_{in} and $V_{out} \cdot n$. Expression (4.13) defines the inductor current in function of time.

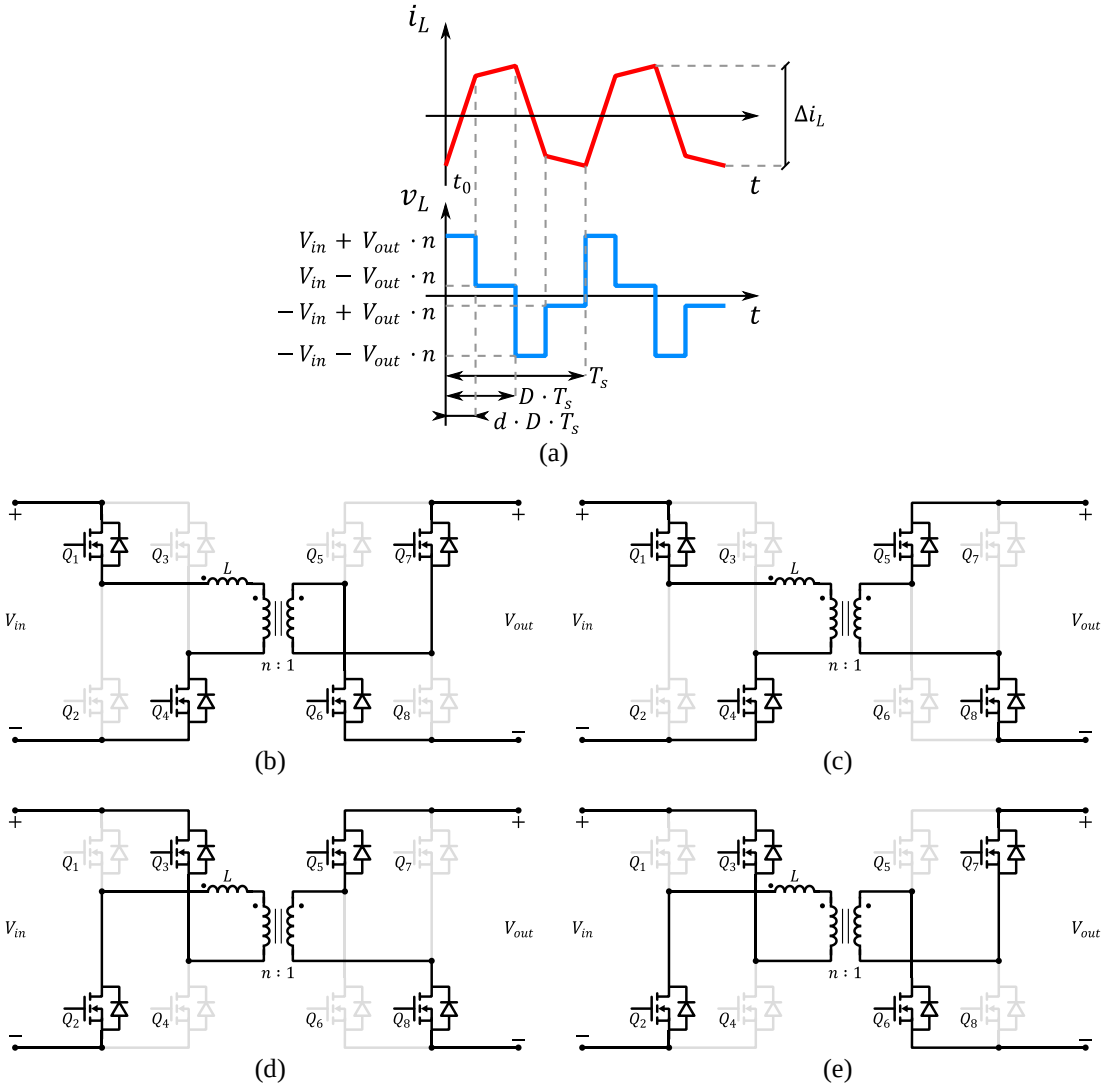


Fig. 4.4. (a) Typical steady state inductor current and voltage waveforms of a DAB-PPC in buck mode. (b) Time interval $0 < t \leq d \cdot D \cdot T_s$. (c) Time interval $d \cdot D \cdot T_s < t \leq D \cdot T_s$. (d) Time interval $D \cdot T_s < t \leq D \cdot T_s + d \cdot D \cdot T_s$. (e) Time interval $D \cdot T_s + d \cdot D \cdot T_s < t \leq T_s$.

$$i_L(t) = \frac{v_L(t)}{L} \cdot \left(t - t_{d \cdot D \cdot T_s}\right) + i_L(t_{d \cdot D \cdot T_s}) = \frac{V_{in} - V_{out} \cdot n}{L} \cdot (t - d \cdot D \cdot T_s) + i_L(d \cdot D \cdot T_s) \tag{4.13}$$

Where, $i_L(d \cdot D \cdot T_s)$ is the last value from the previous time interval.

Time interval $D \cdot T_s < t \leq D \cdot T_s + d \cdot D \cdot T_s$

In the primary side, the semiconductors $Q_{1,4}$ are turned off and $Q_{2,3}$ are turned on. The secondary side semiconductors do not change their switching state. The resulting

inductor voltage is the sum of two negative voltages ($-V_{in}$ and $-V_{out} \cdot n$). Expression (4.14) defines the inductor current in function of time.

$$\begin{aligned} i_L(t) &= \frac{v_L(t)}{L} \cdot \left(t - t_{D \cdot T_s}\right) + i_L(t_{D \cdot T_s}) \\ &= \frac{-V_{in} - V_{out} \cdot n}{L} \cdot (t - D \cdot T_s) + i_L(D \cdot T_s) \end{aligned} \quad \textbf{(4.14)}$$

Where, $i_L(D \cdot T_s)$ is the last value from the previous time interval.

Time interval $\boldsymbol{D \cdot T_s + d \cdot D \cdot T_s < t \leq T_s}$

The primary side semiconductors do not change their switching state. In the secondary side, the semiconductors $Q_{6,7}$ are turned on and $Q_{5,8}$ are turned off. As a result, the inductor observes the voltage difference between $-V_{in}$ and $V_{out} \cdot n$. Expression (4.15) defines the inductor current in function of time.

$$\begin{aligned} i_L(t) &= \frac{v_L(t)}{L} \cdot \left(t - t_{D \cdot T_s + d \cdot D \cdot T_s}\right) + i_L(t_{D \cdot T_s + d \cdot D \cdot T_s}) \\ &= \frac{-V_{in} + V_{out} \cdot n}{L} \cdot (t - (1 + d) \cdot D \cdot T_s) + i_L((1 + d) \cdot D \cdot T_s) \end{aligned} \quad \textbf{(4.15)}$$

Where, $i_L((1 + d) \cdot D \cdot T_s)$ is the last value from the previous time interval.

Semiconductors and capacitors

Expressions (4.16)-(4.23) describe the current and voltage waveforms of the semiconductors Q_{1-8}. On the other hand, equations (4.24),(4.25) define the current and voltage of the output capacitor.

$$i_{Q_1}(t) = i_{Q_4}(t) = \begin{cases} i_L(t) & 0 < t \leq D \cdot T_s \\ 0 & D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.16)}$$

$$i_{Q_2}(t) = i_{Q_3}(t) = \begin{cases} 0 & 0 < t \leq D \cdot T_s \\ -i_L(t) & D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.17)}$$

$$i_{Q_5}(t) = i_{Q_8}(t) = \begin{cases} 0 & 0 < t \leq d \cdot D \cdot T_s \\ -i_L(t) \cdot n & d \cdot D \cdot T_s < t \leq D \cdot T_s \\ -i_L(t) \cdot n & D \cdot T_s < t \leq D \cdot T_s + d \cdot D \cdot T_s \\ 0 & D \cdot T_s + d \cdot D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.18)}$$

$$i_{Q_6}(t) = i_{Q_7}(t) = \begin{cases} i_L(t) \cdot n & 0 < t \leq d \cdot D \cdot T_s \\ 0 & d \cdot D \cdot T_s < t \leq D \cdot T_s \\ 0 & D \cdot T_s < t \leq D \cdot T_s + d \cdot D \cdot T_s \\ i_L(t) \cdot n & D \cdot T_s + d \cdot D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.19)}$$

$$v_{Q_1}(t) = v_{Q_4}(t) = \begin{cases} 0 & 0 < t \leq D \cdot T_s \\ V_{in} & D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.20)}$$

$$v_{Q_2}(t) = v_{Q_3}(t) = \begin{cases} V_{in} & 0 < t \leq D \cdot T_s \\ 0 & D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.21)}$$

$$v_{Q_5}(t) = i_{Q_8}(t) = \begin{cases} V_{out} & 0 < t \leq d \cdot D \cdot T_s \\ 0 & d \cdot D \cdot T_s < t \leq D \cdot T_s \\ 0 & D \cdot T_s < t \leq D \cdot T_s + d \cdot D \cdot T_s \\ V_{out} & D \cdot T_s + d \cdot D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.22)}$$

$$v_{Q_6}(t) = v_{Q_7}(t) = \begin{cases} 0 & 0 < t \leq d \cdot D \cdot T_s \\ V_{out} & d \cdot D \cdot T_s < t \leq D \cdot T_s \\ V_{out} & D \cdot T_s < t \leq D \cdot T_s + d \cdot D \cdot T_s \\ 0 & D \cdot T_s + d \cdot D \cdot T_s < t \leq T_s \end{cases} \quad \textbf{(4.23)}$$

$$i_{C_{out}}(t_i) = -(i_{Q_5}(t_i) + i_{Q_6}(t_i)) - (I_{out}) \quad \textbf{(4.24)}$$

$$v_{C_{out}}(t_i) = \frac{i_{C_{out}}(t_i)}{C_{out}} \cdot T_{ss} + v_{C_{out}}(t_{i-1}) \quad \textbf{(4.25)}$$

4.2.3 Power Losses

The power losses computed with this model are the ones related to the passive and active components inside the converter: magnetics, capacitors and semiconductors.

4.2.3.1 Magnetic Element Power Losses

The power losses in the magnetic components are divided in the series inductance (IHB-FPC and DAB-PPC case) and the isolation transformer (DAB-PPC case).

The series inductances of the designed converters use a high density litz wire. Therefore, skin and proximity losses in the working frequency range are neglected. The peak flux is also selected as low so the core losses are also negligible. Due to these assumptions, the losses in the inductor are modelled in function of the inductor RMS current and the DC resistance of the inductor coil ($R_{DC_{inductor}}$), see (4.26).

$$P_{inductor} = R_{DC_{inductor}} \cdot I_{RMS}^2 \tag{4.26}$$

The transformer losses computation continues the same criteria as the inductor. As the transformer optimization is not the main contribution of this work, high density litz wire and low saturation flux permits to neglect skin, proximity and core losses. Due to that, only DC resistance losses are modelled as given by (4.27). The DC resistance of the transformer are calculated in the primary side (R_{DC_p}) and secondary side (R_{DC_s}).

$$P_{transformer} = R_{DC_p} \cdot I_{RMS_p}^2 + R_{DC_s} \cdot I_{RMS_s}^2 \tag{4.27}$$

4.2.3.2 Capacitive Element Power Losses

The power losses in the capacitive elements are dependent on the equivalent series resistance (ESR) of the used capacitors. The ESR is obtained from the datasheet for the fundamental frequency value of the current flowing through the capacitor. The capacitor leakage losses are taken as negligible (4.28).

$$P_{capacitor} = ESR \cdot I_{RMS}^2 \tag{4.28}$$

4.2.3.3 Semiconductor Power Losses

The power losses in the semiconductors are divided into conduction and switching losses.

Conduction losses

The conduction losses occur due to the current flowing through the inherent resistance of the device. This resistance is the on-state resistance (R_{DS}) of MOSFETs. The conduction loss of a MOSFET is given by (4.29).

$$P_{cond} = R_{DS} \cdot I_{RMS}^2 \tag{4.29}$$

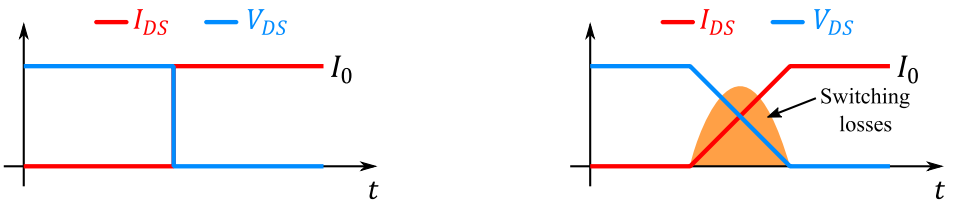
Switching losses

Ideally, when a MOSFET switches from an ON state to an OFF state or vice versa, an instantaneous switch of its voltage and current is assumed (Fig. 4.5a). In reality, MOSFET's current and voltage coexist for a certain amount of time, which generates power losses each time they turn on and turn off (Fig. 4.5b). Turning a MOSFET off is often assumed to result in negligible losses. Turning a MOSFET off is often assumed to result in negligible losses and they can be up to five times lower than the turn on losses [101], [102]. Bearing this in mind, with the aim of simplifying the analysis, only turn on losses will be considered. These can be classified into three types: ideal soft switching (or ZVS, incomplete ZVS (iZVS) and hard switching.

Ideal soft switching

Soft switching or ZVS occurs when a MOSFET turns on when its output capacitor is completely discharged. Fig. 4.6a shows a simplified ZVS transition. The switching events in waveforms are exaggerated for explanation purpose.

At interval 0a, the inductor current is free-wheeling through Q_1 and the output capacitor of Q_2 is fully charged to the source voltage (V_{DC}). Then, the gate signal of Q_1 is turned off and the current stops flowing through its channel. Consequently, the positive flow of the inductor current helps to charge and discharge the output capacitors of Q_1 and Q_2, respectively (interval 1a or t_{ZVS}). Once the output capacitor of Q_2 is fully discharged, its body diode starts conducting until the dead band (t_{db}) time finishes (interval 2a). At this point, the gate signal of Q_2 reaches the threshold voltage and the inductor current



(a) (b)

Fig. 4.5. Switching transition. (a) Ideal switching. (b) Simplified non-ideal switching.

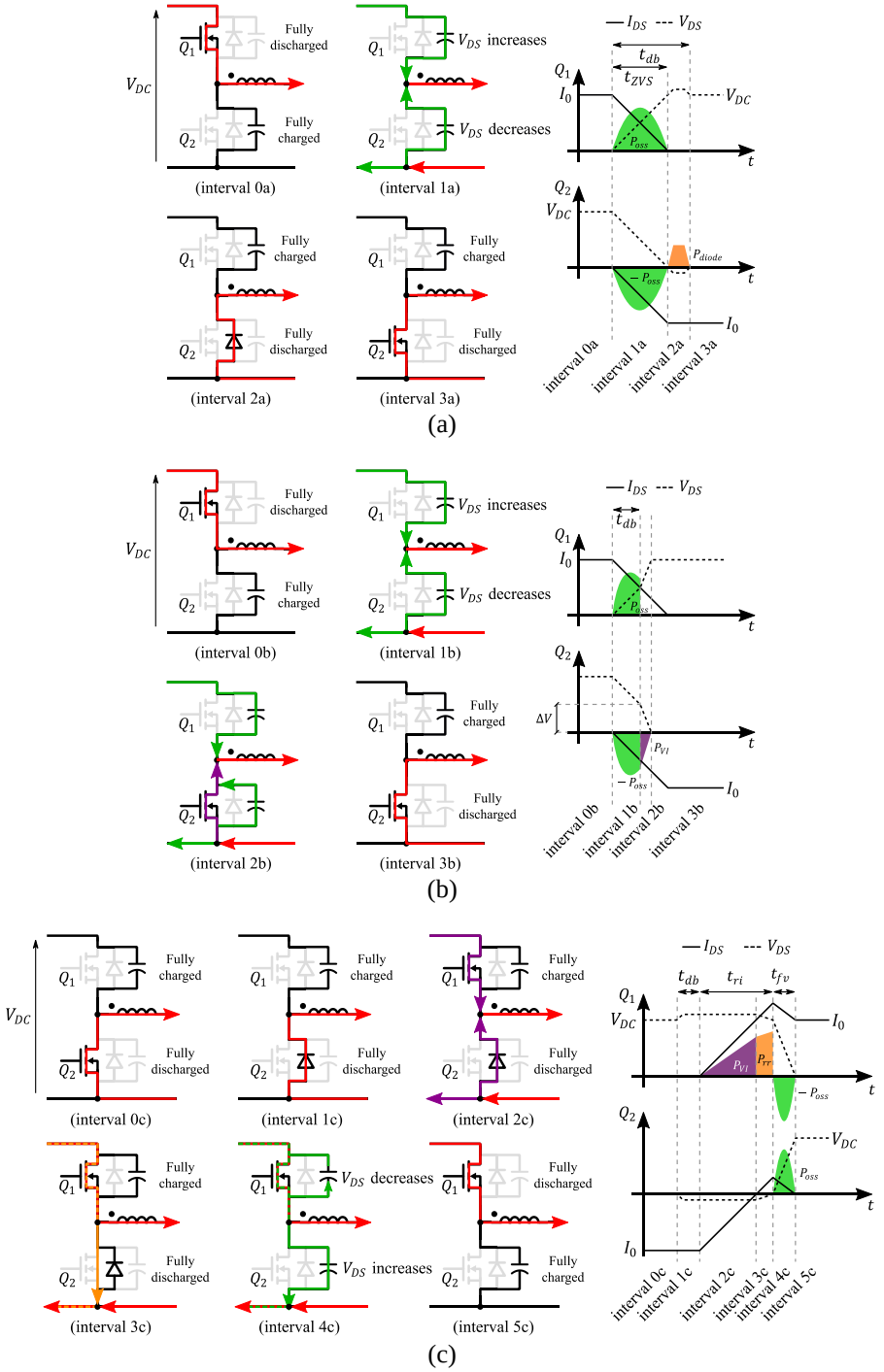


Fig. 4.6. Turn on of a MOSFET. (a) ZVS. (b) iZVS. (c) Hard switching.

flows through its conduction channel (interval 3a). The voltage drop that exits between interval 2a and interval 3a is just due to the transition from Q_2's body diode to its channel.

To sum up, the power losses in ZVS operation occur due to the resonant transition (interval 1a) and the conduction losses of the body diode (interval 2a). These losses are given in (4.30) and (4.31).

$$P_{oss} = E_{oss} \cdot f_{sw} \cdot \lambda_{oss} \quad \textbf{(4.30)}$$

$$P_{diode} = (V_{SD} \cdot I_{SD} + R_{SD} \cdot I_{SD}^2) \cdot \frac{t_{db} - t_{ZVS}}{T_S} \quad \textbf{(4.31)}$$

Where, λ_{oss}=0.5 (the charging/discharging process might dissipate more than 50 % of the stored energy [103]), t_{db} is the dead time and t_{ZVS} is the resonant period. t_{ZVS} is computed using the charge stored by the MOSFET and the average switching current (4.32).

$$t_{ZVS} = \frac{Q_{oss}(V_{DC})}{\frac{I_0}{2}} \quad \textbf{(4.32)}$$

In conclusion, Q_2 works under ZVS conditions when it is turned on with $I_{DS_{Q_2}} < 0$. Regarding Q_1, ZVS conditions are also achieved with $I_{DS_{Q_1}}$<0. However, in this case, a negative flow of the inductor current is required.

Incomplete soft switching

Although a semiconductor turns on with I_{DS}<0, if the stored energy in the inductor is not high enough, it would not be able to completely charge and discharge both capacitances. This is known as iZVS and is shown in Fig. 4.6b.

Compared to ideal soft switching, in this case, t_{db} is not sufficient to complete the charge/discharge process. Therefore, at the end of interval 1b, Q_2 starts conducting while its output capacitor is charged to ΔV. Bearing this in mind, the losses that will be considered during iZVS are related to the resonant transition (interval 1b) and the conduction losses (interval 2b), (4.33),(4.34) respectively.

$$P_{oss} = E_{oss}(V_{DC} - \Delta V) \cdot f_{sw} \cdot \lambda_{oss} \quad \textbf{(4.33)}$$

$$P_{VI} = \frac{\Delta V^2}{R_{DS}} \cdot \frac{t_{iZVS}}{T_S} \quad \textbf{(4.34)}$$

Where, t_{iZVS} is the time left to completely charge/discharge the output capacitors and is given by (4.35).

$$t_{iZVS} = \frac{Q_{oss}(\Delta V)}{\frac{\Delta V}{R_{DS}}} \quad \textbf{(4.35)}$$

The boundary of the iZVS region is calculated by using (4.36) [103]. Expression (4.36) determines if the energy stored by the inductor is enough for the charging and discharging process of the MOSFETs' output capacitors.

$$\frac{1}{2} \cdot L \cdot I_0^2 \geq Q_{oss}(V_{DC}) \cdot V_{DC} \quad \textbf{(4.36)}$$

Hard switching losses

Hard switching occurs when a MOSFET starts conducting while its output capacitor is still charged to the source voltage. Fig. 4.6c shows a simplified hard switching.

At the beginning of the transition (interval 0c), the inductor current is free-wheeling through Q_2 and the output capacitor of Q_1 is fully charged to the output voltage (V_{DC}). Then, the gate signal of Q_2 is turned off and immediately, the inductor current flows through its body diode until the end of t_{db} (interval 1c). Contrary to the previous case, the positive flow of the inductor current does not help to discharge the output capacitor of Q_1 and charge the output capacitor Q_2. Therefore, when Q_1 starts conducting, it does with all the DC voltage and a current that rises to I_0 (interval 2c). However, the drain current of Q_1 continues increasing due to the reverse recovery effect of Q_2's body diode (interval 3c). Once the diode reaches its reverse recovery current, the rising current period (t_{ri}) finishes and it starts blocking voltage. At this point, the output capacitor of Q_1 discharges and the output capacitor of Q_2 charges to V_{DC} (interval 4c). Finally, the only current flowing through the channel of Q_1 is the inductor current (interval 5c).

In conclusion, Q_1 works under hard switching conditions when it is turned on with $I_{DS_{Q_1}} > 0$. Same thing occurs with Q_2 if it is turned on with $I_{DS_{Q_2}} > 0$.

To sum up, the power losses that will be considered when hard switching occurs are related to the VI losses (4.37), the reverse recovery losses (4.38) and the resonant transition (4.39).

$$P_{VI} = \frac{1}{2} \cdot I_0 \cdot V_{DC} \cdot \frac{t_{ri} + t_{fv}}{T_S} \quad \textbf{(4.37)}$$

$$P_{rr} = Q_{rr} \cdot V_{DC} \cdot f_{sw} \quad \textbf{(4.38)}$$

$$P_{oss} = \left(E_{oss_{Q1}} + E_{oss_{Q2}}\right) \cdot f_{sw} \quad \textbf{(4.39)}$$

The parameters t_{ri} and t_{fv} are computed using (4.40),(4.41). Where, Q_{GS} is the amount of charge that must be supplied while the gate voltage increases from the threshold voltage to the plateau voltage and Q_v is the amount of charge that must be supplied through the plateau. Both values can be extracted from the datasheet of the semiconductor.

$$t_{ri} = \frac{Q_{GS}}{I_{gate}} = \frac{Q_{GS} \cdot R_{gate}}{V_{driver} - \frac{\left(V_{th} + V_{pl}\right)}{2}} \quad \textbf{(4.40)}$$

$$t_{fv} = \frac{Q_v}{I_{gate}} = \frac{Q_v \cdot R_{gate}}{V_{driver} - V_{pl}} \quad \textbf{(4.41)}$$

Table 4.3 summarizes the applied equations for each switching condition.

4.2.4 Experimental Prototype

The experimental prototype under analysis consists of 5 PCBs: two power PCBs (Fig. 4.7a), two driver PCBs (Fig. 4.7b) and a micro-controller PCB (Fig. 4.7c). Fig. 4.7d shows the final solution. As it can be observed, the power and the driver PCBs are connected through the gate signals and the micro-controller PCB is upon the driver PCBs.

Table 4.3. ZVS, iZVS and hard-switching boundaries.

Turn on semiconductor current	iZVS condition	Applied equations
I_{DS}<0	$\frac{1}{2} \cdot L \cdot I_0^2 \geq Q_{oss}(V_{DC}) \cdot V_{DC}$	(4.30)-(4.32)
	$\frac{1}{2} \cdot L \cdot I_0^2 < Q_{oss}(V_{DC}) \cdot V_{DC}$	(4.33)-(4.35)
I_{DS}>0	±2.5 kW	(4.37)-(4.41)

Each power PCB contains three HBs connected in parallel, but in order to test the IHB-FPC and the DAB-PPC from Fig. 4.2, 4 HBs are required. Therefore, each power PCB operates with two HBs. As it can be observed in Fig. 4.7a, HB3 is unused. The driver PCBs contain the necessary circuit to adapt the PWM signals to the gate signals of the

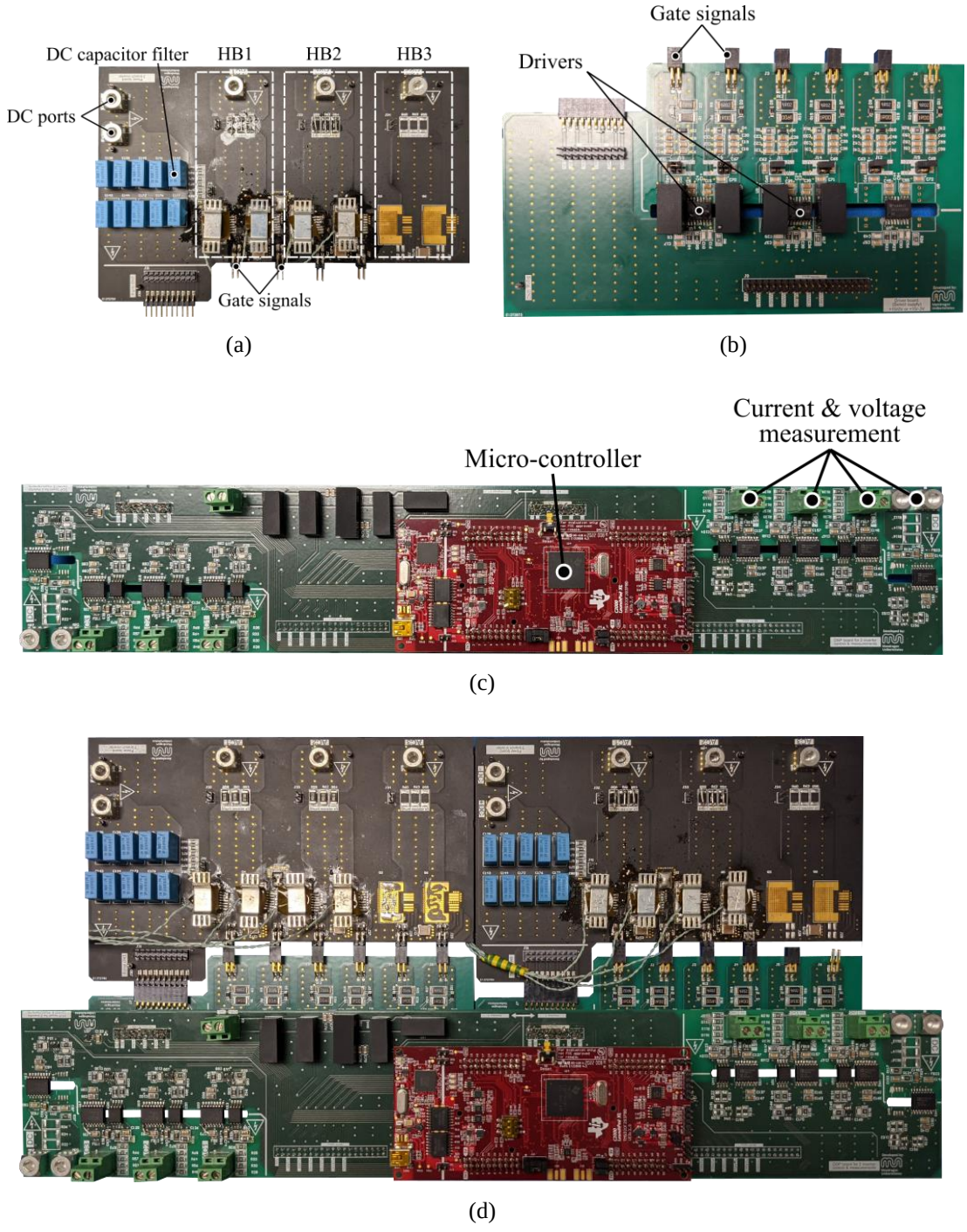


Fig. 4.7. Experimental prototype. (a) Power PCB. (b) Driver PCB. (c) DSP PCB. (d) Complete solution.

MOSFETs. The micro-controller PCB contains the LAUNCHXL-F28379D, 2 current measuring ports and 6 voltage measuring ports. This PCB is prepared to send the PWM signals to both driver PCBs, since it can be connected upon them.

Table 4.4 details the manufacturing parameters of the magnetics implemented at the IHB-FPC and the DAB-PPC. Regarding the core, two different EE type designs are selected: EE5521 (IHB-FPC case) and EE6527 (DAB-PPC case). The final volume is slightly higher in the IHB-FPC, since 4 cores are required. The volume is defined as the minimum box which can be put around the active part of the core and windings [104], which is given by (4.42).

$$Magnetic\ volume = A \cdot 2C \cdot (B - E + F) \tag{4.42}$$

Where, A, B, C E and F are based on the scheme from Fig. 4.8.

Due to the fact that Table 4.2 presents three different designs for the DAB-PPC, Table 4.4 details the implemented number of turns for each case. To achieve this, three

Table 4.4. Magnetics' manufacturing parameters.

Parameter	IHB-FPC	DAB-PPC	
	Inductor	Inductor	Transformer
Core	EE5521 (CF 139)	EE6527 (CF 139)	EE6527 (CF 139)
Volume	4x126 cm^3	223 cm^3	223 cm^3
Nº of turns	32	7 10 (7+3) 12 (7+3+2)	3:30 @ n=0.1 6 (3+3):30 @ n=0.2 9 (3+3+3):30 @ n=0.3

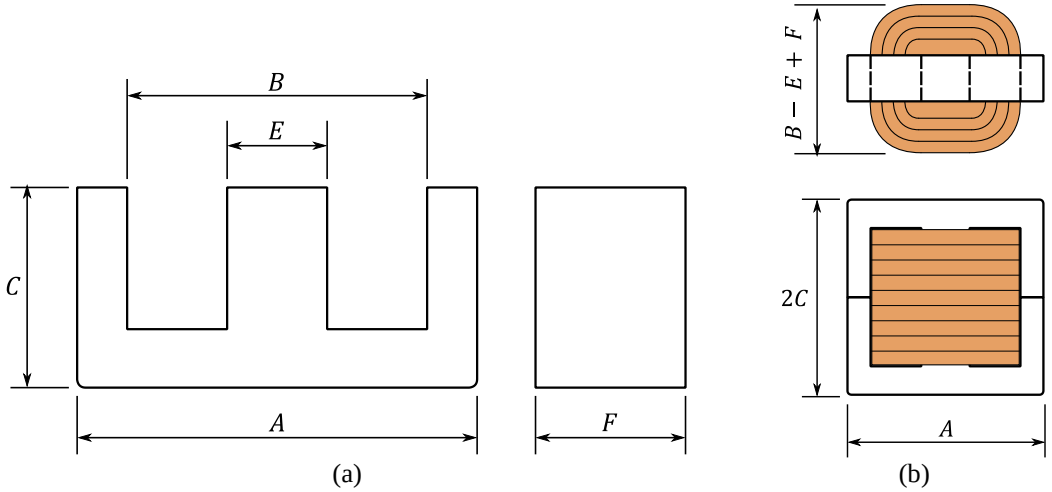


Fig. 4.8. EE core volume. (a) Drawing. (b) Minimum box volume assumption.

different windings are assembled and connected in series according to the desired design. In the case of n=0.1, the inductor contains a winding of 7 turns, and the transformer contains a primary side winding of 3 turns and a secondary of 30 turns. In the case of n=0.2, the same 7 turns winding of n=0.1 is connected in series with a 3 turns winding. Also, extra 3 turns are connected in series to the primary side winding.

4.2.5 Simulation and Experimental Results

4.2.5.1 Buck Mode (P_{load}=+2.5 kW)

DAB-PPC transformation ratio selection

Before comparing the results between the IHB-FPC and the DAB-PPC, the optimal transformation ratio for the DAB-PPC is selected. As shown in Table 4.2, there are three different designs: n=0.1, n=0.2 and n=0.3. Then, the selected design is compared against the IHB-FPC.

Table 4.5 defines the experimental test points for the n selection. As it can be observed, P_{load} and V_{source} are kept constant. The only parameter that varies is V_{load}, which increases from 225 V to 300 V in steps of 25 V.

Table 4.5. Experimental test points, buck mode.

Parameter	Test point 1	Test point 2	Test point 3	Test point 4[13]
P_{load}	2.5 kW	2.5 kW	2.5 kW	2.5 kW
V_{source}	300 V	300 V	300 V	300 V
V_{load}	225 V	250 V	275 V	300 V

[13] At "Test point 4", V_{load} is not set to 300 V, but to 299.8 V. K_{pr}=0 is not possible and its minimum value is dependent of the power losses of the converter. Therefore, the load voltage is slightly decreased.

In the first place, Fig. 4.9 presents the steady state waveforms of the inductor current (i_L) and the AC voltages (v_{pri} and v_{sec}). Fig. 4.9a, Fig. 4.9c and Fig. 4.9e show the results at "Test point 1" for n=0.1, n=0.2 and n=0.3, respectively. Fig. 4.9b, Fig. 4.9d and Fig. 4.9f show the results at "Test point 4" for n=0.1, n=0.2 and n=0.3, respectively. The main differences between the three designs are observed at "Test point 1". As it can be observed, i_L presents very different waveforms depending on the n value. Please observe that for n=0.1 (Fig. 4.9a), the scale of the current is 20 A/div. Focusing on the AC voltages, Fig. 4.9 demonstrates that the primary side semiconductors must only withstand

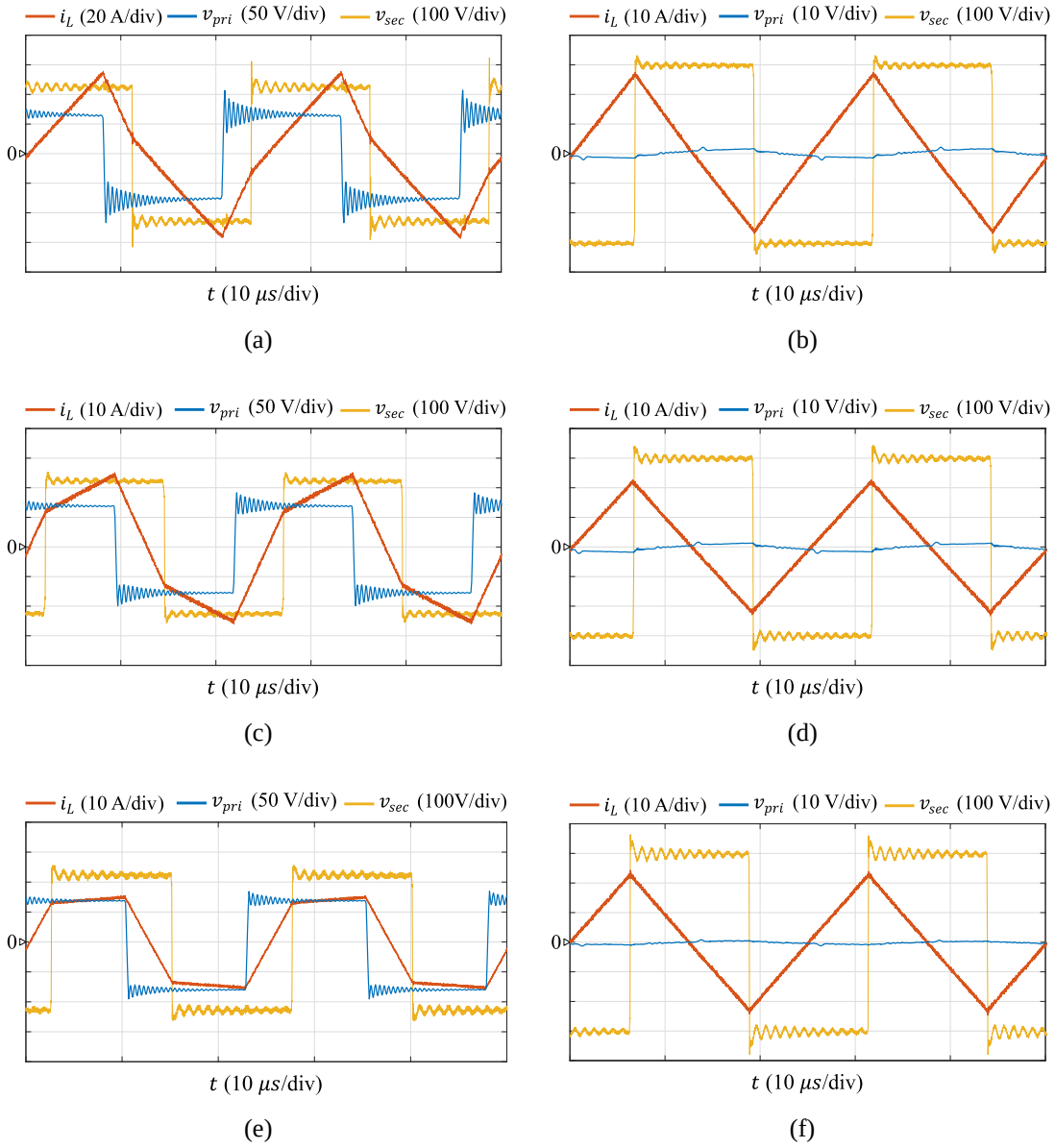


Fig. 4.9. Experimental steady state waveforms, buck mode. Results with DAB-PPC n=0.1 (a) At "Test point 1". (b) At "Test point 4". Results with DAB-PPC n=0.2 (c) At "Test point 1". (d) At "Test point 4". Results with DAB-PPC n=0.3 (e) At "Test point 1". (f) At "Test point 4".

a maximum voltage of 100 V (including voltage overshoot). The results at "Test point 4" show that the three designs obtain very similar waveforms. At this working point, K_{pr} is near to zero and the n value has no major impact.

In the second place, Table 4.6 presents the K_{pr} results for each design. As it can be observed, from "Test point 1" to "Test point 4", P_{in} decreases from 0.63 kW to 0.21 kW. The slight difference that exists in the K_{pr} between the different n designs is due to η_{sys}. This is demonstrated in expression (4.43). A lower efficiency entails higher power losses and, in consequence, the converter must process a higher power.

$$K_{pr_{ISOP}} = \frac{1 - G_V}{\eta_{sys}} \tag{4.43}$$

When it comes to "Test point 4", the value of P_{in} is not given. This is due to the measuring issues presented by the power meter with very low voltage (V_{in} case) and current (I_{out} case). Nevertheless, it is demonstrated that the DAB-PPC still can provide 2.5 kW to the load when the source and the load have the same voltage level.

In the third place, Fig. 4.10 presents the system efficiency and inductor RMS current results. The dashed lines represent the simulation results and the markers represent the experimental results. At "Test point 1", the efficiency achieved with n=0.1 decreases down to 92 % (Fig. 4.10a). This is due to the high inductor RMS current obtained with n=0.1 (Fig. 4.10b). At "Test point 2" and "Test point 3", the efficiency obtained with n=0.1 improves considerably as the inductor RMS current is reduced. A peak efficiency of 99.4 % is achieved at "Test point 3". The designs with n=0.2 and n=0.3 show more

Table 4.6. Experimental K_{pr} results of the DAB-PPC, buck mode.

	Parameter	Test point 1	Test point 2	Test point 3	Test point 4
n=0.1	P_{in}	0.668 kW	0.427 kW	0.208 kW	NaN
	P_{load}	2.482 kW	2.492 kW	2.505 kW	2.505
	(K_{pr})	(0.269)	(0.171)	(0.083)	NaN
n=0.2	P_{in}	0.635 kW	0.418 kW	0.208 kW	NaN
	P_{load}	2.507 kW	2.503 kW	2.504 kW	2.503
	(K_{pr})	(0.253)	(0.167)	(0.083)	NaN
n=0.3	P_{in}	0.631 kW	0.419 kW	0.210 kW	NaN
	P_{load}	2.498 kW	2.493 kW	2.502 kW	2.488
	(K_{pr})	(0.252)	(0.168)	(0.084)	NaN

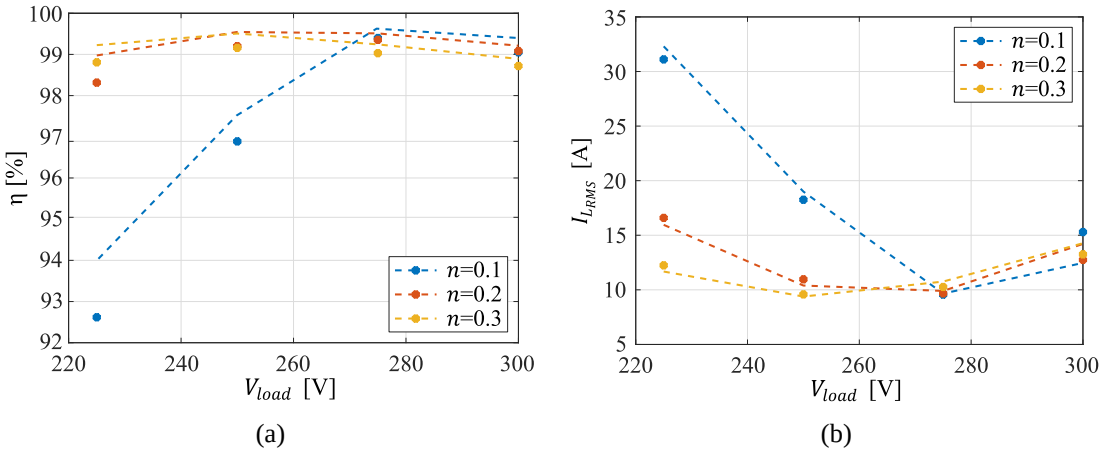


Fig. 4.10. Experimental and simulation results of the DAB-PPC, buck mode. (a) System efficiency. (b) Inductor RMS current.

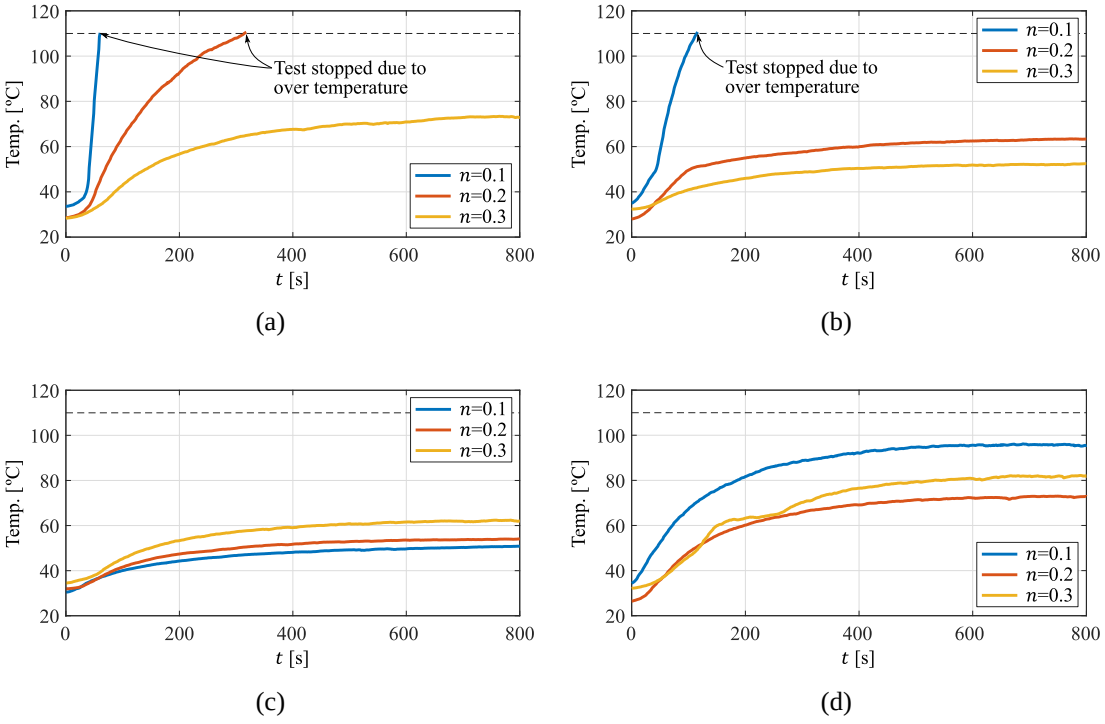


Fig. 4.11. Top-case temperature evolution of the most critical semiconductor of the DAB-PPC, buck mode. (a) Test point 1. (b) Test point 2. (c) Test point 3. (d) Test point 4.

constant results. At lower V_{load} values higher efficiencies are obtained with n=0.3, and at higher V_{load} values, n=0.2 is more efficient.

Fig. 4.11 shows the temperature evolution of the most critical semiconductor at each test point. All of them correspond to the primary side (high current side). As it can be observed, at "Test point 1" and "Test point 2" the test is stopped to protect the semiconductors from over temperature. This occurs with n=0.1 at "Test point 1" and

"Test point 2", and with n=0.2 at "Test point 1". However, in the case of n=0.2, it can take up to 5 minutes. At "Test point 3", the temperature of the semiconductors decreases significantly with the three n designs. Finally, at "Test point 4", the temperature of the semiconductors increases again. This thermal behavior matches completely with the inductor RMS current results from Fig. 4.10. Then, it can be concluded that semiconductors' power losses are mainly due to conduction.

Based on the obtained results, n=0.1 is dismissed as the optimal design. Its low efficiency results when working with low V_{load} values are not competitive. Also, the rapid temperature evolutions at "Test point 1" and "Test point 2" (Fig. 4.11a and Fig. 4.11b) are not acceptable. Comparing n=0.2 and n=0.3, the first presents slightly higher efficiencies than the latter over a larger operation range. On the other hand, during "Test point 1" the test had to be stopped with n=0.2 due to the high temperature of the primary side semiconductors. Nevertheless, 5 minutes are not considered as critical and n=0.2 is selected as the optimal design to compare to the IHB-FPC.

IHB-FPC vs DAB-PPC with n=0.2

For the present comparison, the same test points defined in Table 4.2 are considered except for "Test point 4". In this case, the value of V_{load} is reduced down to 295 V. This value corresponds to the maximum achievable voltage by the IHB-FPC.

In the first place, Fig. 4.12 shows the experimental steady state waveforms. Fig. 4.12a, Fig. 4.12c, Fig. 4.12e and Fig. 4.12g present the waveforms of the IHB-FPC. To be more precise, the current of a single inductor (i_L) and the voltage of the low side semiconductor (v_{Q_2}). Fig. 4.12b, Fig. 4.12d, Fig. 4.12f and Fig. 4.12h present the main current and voltage waveforms of the DAB-PPC, such as: the inductor current (i_L) and the AC voltages (v_{pri} and v_{sec}).

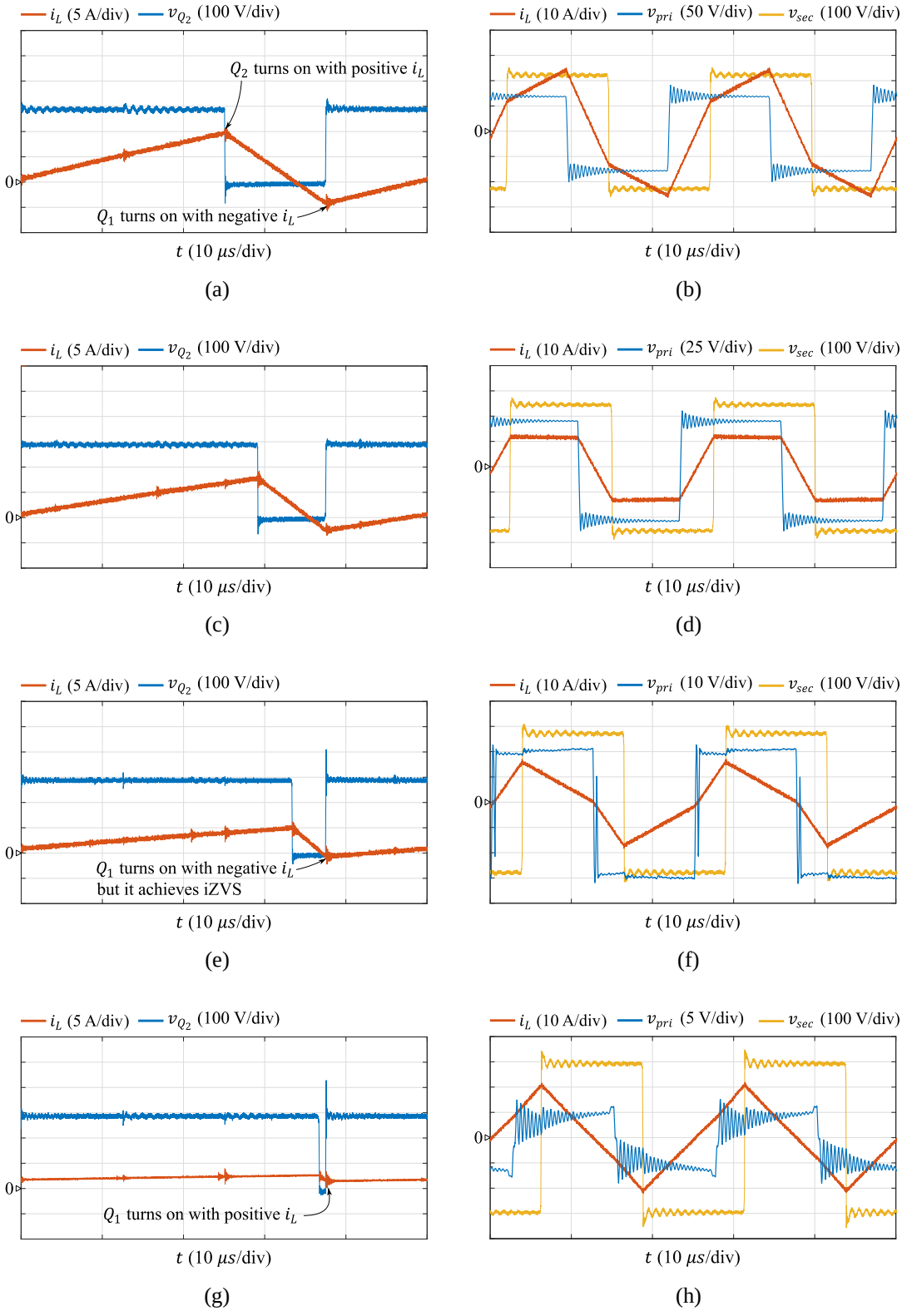


Fig. 4.12. Experimental steady state waveforms, buck mode. "Test point 1" (a) IHB-FPC. (b) DAB-PPC. "Test point 2" (c) IHB-FPC. (d) DAB-PPC. "Test point 3" (e) IHB-FPC. (f) DAB-PPC. "Test point 4" (g) IHB-FPC. (h) DAB-PPC.

Regarding the waveforms from the IHB-FPC, two main observations are obtained. First, its semiconductors always block the maximum voltage of the system (V_{source}=300 V). Second, its semiconductors operate under ZVS at "Test point 1" and at "Test point 2". At "Test point 3" and at "Test point 4" the high-side semiconductors operate under iZVS and hard switching. As it can be observed, at "Test point 1" (Fig. 4.12a) and at "Test point 2" (Fig. 4.12c), Q_2 turns on with a positive inductor current. This means that it turns on with I_{DS}<0. Same thing occurs with Q_1 with a negative inductor current. At "Test point 3" (Fig. 4.12e), Q_1 also turns on with a negative inductor current. Nevertheless, this inductor current is close to zero, which provokes iZVS. At "Test point 4" (Fig. 4.12g), Q_1 turns on with a positive inductor current, thus I_{DS}>0. Due to this, hard switching occurs and the power losses of the semiconductors increase. This is demonstrated later by analyzing the thermal behavior of the semiconductors. Apart from that, a voltage overshoot of more than 100 V appears in v_{Q_2}.

When it comes to the DAB-PPC, a reduction of the voltage blocked by the primary side semiconductors is observed. The maximum blocked voltage appears at "Test point 1" (Fig. 4.12b), more precisely 75 V. However, at "Test point 4" the primary side semiconductors only block up to 5 V (Fig. 4.12h). Apart from that, hard switching of the primary side semiconductors is observed at "Test point 4". $Q_{1,4}$ and $Q_{2,3}$ turn on with a positive and a negative inductor current, respectively. However, at this test point the voltage observed by $Q_{1,2,3,4}$ is only 5 V. Due to this reduced voltage, the switching losses barely increase although hard switching conditions occur.

In the second place, Table 4.7 presents the K_{pr} results of both solutions. The IHB-FPC obtains constant K_{pr} values slightly above 1. This is because P_{in} consists of P_{load} plus the power losses. On the other hand, P_{in} at the DAB-PPC decreases from "Test point 1" to "Test Point 4". This is a direct consequence of the reduction of G_V. As V_{load} gets closer to V_{source}, the power processed by the DAB-PPC decreases up to 0.016. This means that at "Test point 4", the DAB-PPC only processes a 1.6 % of the system power.

In the third place, Fig. 4.13a compares the system efficiency obtained by the IHB-FPC and the DAB-PPC. At "Test point 1" and "Test point 2", the IHB-FPC presents higher efficiency results, especially at "Test point 1", where its efficiency is 1.7 points

Table 4.7. Experimental K_{pr} results, buck mode.

Solution	Parameter	Test point 1	Test point 2	Test point 3	Test point 4
IHB-FPC	P_{in}*	2.526 kW	2.519 kW	2.528 kW	2.534 kW
	P_{load}	2.501 kW	2.501 kW	2.503 kW	2.501 kW
	(K_{pr})	(1.010)	(1.007)	(1.010)	(1.013)
DAB-PPC (n=0.2)	P_{in}	0.635 kW	0.418 kW	0.208 kW	0.040 kW
	P_{load}	2.507 kW	2.503 kW	2.504 kW	2.501 kW
	(K_{pr})	(0.253)	(0.167)	(0.083)	(0.016)

*4 modules

higher. However, at "Test point 3" and "Test point 4", the high side semiconductors of the IHB-FPC commute under hard switching and consequently its efficiency decreases significantly. This is demonstrated in Fig. 4.13b. As it can be observed, the decrement in the efficiency of the IHB-FPC is not due to a higher inductor RMS current. On the other hand, the efficiency of the DAB-PPC remains above 99 %.

Fig. 4.14 presents the top-case temperature evolution of all the semiconductors. At "Test point 1" (Fig. 4.14a and Fig. 4.14b), it can be observed that the semiconductors from the IHB-FPC do barely heat due to the soft-switching conditions. When it comes to the DAB-PPC, its primary side semiconductors present very high temperatures and the test must be stopped to avoid over temperature of devices. This is mainly due to the high inductor RMS current. On the other hand, the secondary side semiconductors do not exceed 40 ºC. At "Test point 2" (Fig. 4.14c and Fig. 4.14d), the IHB-FPC obtains similar results to the previous case. Indeed, due to the reduction of $I_{L_{RMS}}$, the semiconductors obtain lower steady state temperatures. Regarding the DAB-PPC, its primary side

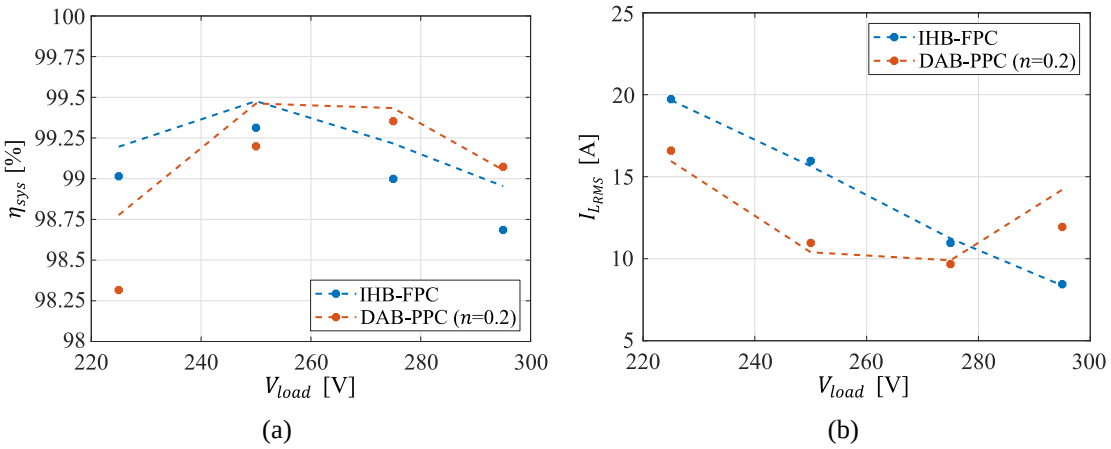


Fig. 4.13. Experimental and simulation results, buck mode. (a) System efficiency. (b) Inductor RMS current. The $I_{L_{RMS}}$ of the IHB-FPC corresponds to the sum of the 4 inductors.

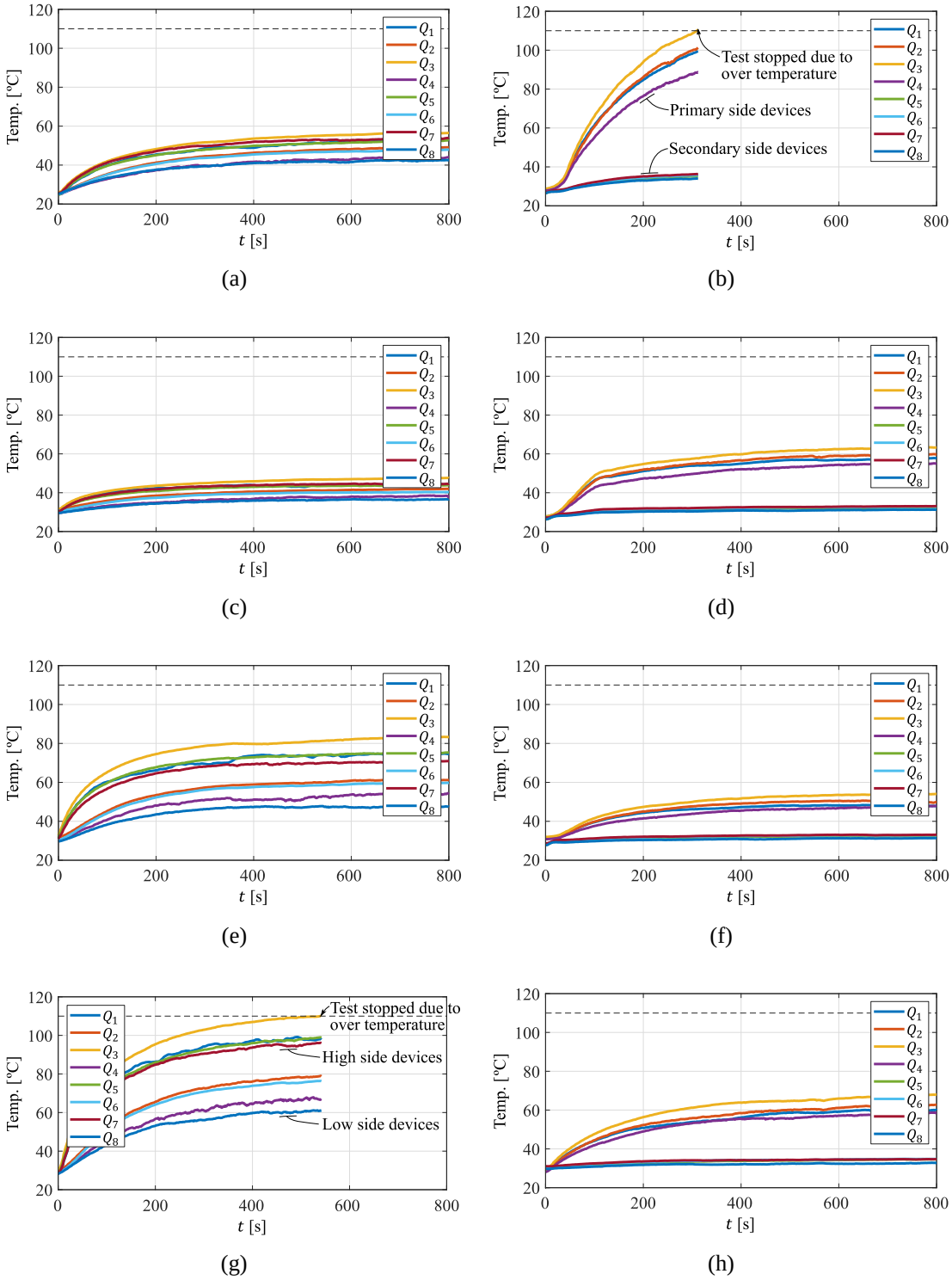


Fig. 4.14. Top-case temperature evolution, buck mode. "Test point 1" (a) IHB-FPC. (b) DAB-PPC. "Test point 2" (c) IHB-FPC. (d) DAB-PPC. "Test point 3" (e) IHB-FPC. (f) DAB-PPC. "Test point 4" (g) IHB-FPC. (h) DAB-PPC.

semiconductors' temperature decreases significantly. This is a direct consequence of the $I_{L_{RMS}}$ reduction in Fig. 4.13b. Still, the secondary side semiconductors do not exceed 40 ºC. At "Test point 3" (Fig. 4.14e and Fig. 4.14f), the high side semiconductors from the IHB-FPC ($Q_{1,3,5,7}$) enter in hard switching conditions. Concerning the DAB-PPC, again the primary side presents higher temperatures than the secondary side. Nevertheless, none of them is bothering. At "Test point 4" (Fig. 4.14g and Fig. 4.14h), the temperature of the high side semiconductors at the IHB-FPC exceeds the 110 ºC limit and the test must be stopped. Indeed, a 15 ºC gap is clearly observed between the high side and the low side devices. On the other side, the highest temperature achieved by semiconductors at the DAB-PPC barely reaches 70 ºC.

4.2.5.2 Boost Mode (P_{load}=−2.5 kW)

The next step is to compare the performance of the IHB-FPC and the DAB-PPC with a reverse power flow. Table 4.8 defines the experimental test points. The main difference compared to the previous analysis is that now V_{load} acts as a source; therefore, P_{load} receives negative values.

IHB-FPC vs DAB-PPC with n=0.2

In the first place, Fig. 4.15 presents the experimental steady state waveforms in boost mode. Fig. 4.15a, Fig. 4.15c, Fig. 4.15e and Fig. 4.15g present the main waveforms of the IHB-FPC: current of a single inductor (i_L) and the voltage of the high side semiconductor (v_{Q_1}). Fig. 4.15b, Fig. 4.15d, Fig. 4.15f and Fig. 4.15h present the inductor current (i_L) and the AC voltages (v_{pri} and v_{sec}) of the DAB-PPC. As it can be observed, now the inductor current is reversed in both cases and regarding the DAB-PPC, the leading AC voltage is v_{sec}.

Table 4.8. Experimental test points, boost mode.

Parameter	Test point 1	Test point 2	Test point 3	Test point 4
P_{load}	−2.5 kW	−2.5 kW	−2.5 kW	−2.5 kW
V_{source}	300 V	300 V	300 V	300 V
V_{load}	225 V	250 V	275 V	295 V

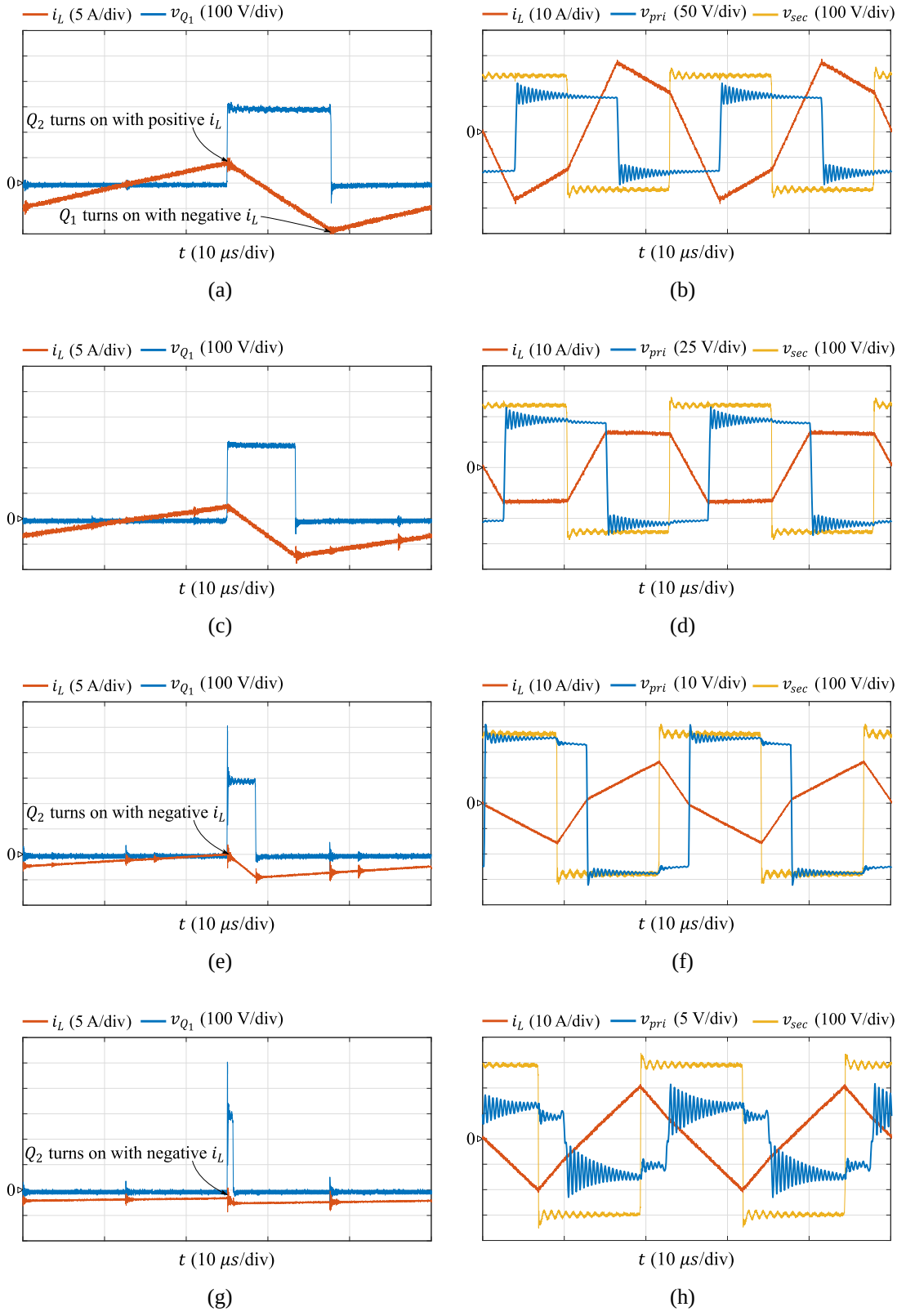


Fig. 4.15. Experimental steady state waveforms, boost mode. "Test point 1" (a) IHB-FPC. (b) DAB-PPC. "Test point 2" (c) IHB-FPC. (d) DAB-PPC. "Test point 3" (e) IHB-FPC. (f) DAB-PPC. "Test point 4" (g) IHB-FPC. (h) DAB-PPC.

Focusing on the results of the IHB-FPC, non-ZVS conditions are observed at "Test point 3" and "Test point 4". In this case, the hard switching occurs when the low side semiconductor (Q_2) turns on. In consequence, a 200 V overvoltage appears at Q_1. Regarding the waveforms of the DAB-PPC, hard switching conditions are also observed at the primary side. To be more precise, at "Test point 4", see Fig. 4.15h. Similar to buck mode, this occurs with very low voltage (around 5 V), which does not endanger the primary side semiconductors.

In the second place, Table 4.9 presents the K_{pr} results. Due to the fact that the system power flow is reversed, the parameters that are used to compute the K_{pr} are P_{out} and P_{source}, which act as the input of the converter and the load of the system, respectively. Compared to the buck mode, similar results are obtained. The IHB-FPC always processes a 100 % of the system power, whereas the DAB-PPC just processes up to a 27.1 % of the system power (Test point 1 case). This percentage decreases down to a 2.5 % at "Test point 4".

In the third place, Fig. 4.16 presents the simulation and experimental system efficiency and $I_{L_{RMS}}$ results. Again, the IHB-FPC presents higher efficiencies than the DAB-PPC at low V_{load} values. However, as V_{load} increases the power processed by the DAB-PPC decreases, and its efficiency improves. On the other hand, the low side devices of the IHB-FPC enter in hard switching and its switching losses increase. This causes an efficiency drop at "Test point 3" and "Test point 4".

Fig. 4.17 shows the top-case temperature evolution of all the devices at each test point. At "Test point 1" the semiconductors from IHB-FPC present low temperatures. However, in the case of the DAB-PPC the test must be stopped due to over temperature.

Table 4.9. Experimental K_{pr} results, boost mode.

Solution	Parameter	Test point 1	Test point 2	Test point 3	Test point 4
IHB-FPC	P_{out}*	−2.499 kW	−2.499 kW	−2.498 kW	−2.499 kW
	P_{source}	−2.478 kW	−2.485 kW	−2.474 kW	−2.469 kW
	(K_{pr})	(1.008)	(1.005)	(1.010)	(1.012)
DAB-PPC (n=0.2)	P_{out}	−0.623 kW	−0.434 kW	−0.222 kW	−0.063 kW
	P_{source}	−2.293 kW	−2.473 kW	−2.483 kW	−2.480 kW
	(K_{pr})	(0.271)	(0.175)	(0.089)	(0.025)

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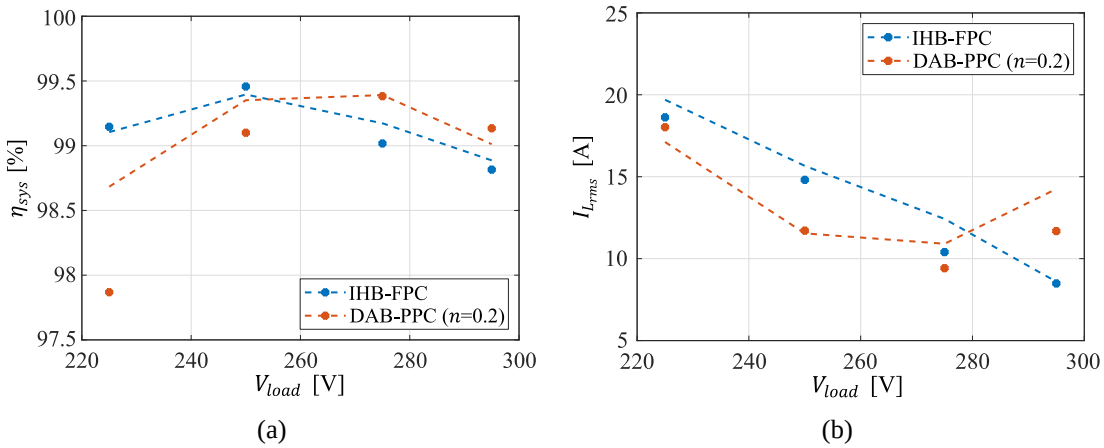


Fig. 4.16. Experimental and simulation results, boost mode. (a) System efficiency. (b) Inductor RMS current.

Again, a clear temperature gap is observed between the primary side and secondary side semiconductors from the DAB-PPC. At "test point 4" contrary results are obtained. In this case, the maximum top-case temperature at the DAB-PPC does not exceed the 70 ºC, whereas in the IHB-FPC temperatures close to 100 ºC are observed.

4.2.6 Discussion

Based on the experimental tests, Table 4.10 summarizes the main results. First, a 1.13 times bigger volume is required for the magnetics of the IHB-FPC. In addition, if the inductor of the DAB-PPC is integrated inside the transformer, a major reduction is achieved. Second, the overall efficiency achieved by the IHB-FPC is slightly higher than the DAB-PPC, specially in boost mode. This is due to the low efficiency of the DAB-PPC at "Test point 1". At this test point, the high value of $I_{L_{RMS}}$ provokes high conduction losses at the primary side. Indeed, the top-case temperature of the primary side semiconductors reaches 110 ºC and the test must be stopped before reaching a thermal steady state. Finally, the electrical stress of different active and passive components is compared. In this case, the main advantage of the IHB-FPC relays on the output capacitor. Due to the 90º phase-shift of the inductor currents, the current filtered by C_{out} is highly reduced. However, the DAB-PPC presents a lower electrical stress on the rest of the components, especially on the inductor (2.16 lower) and the switching devices.

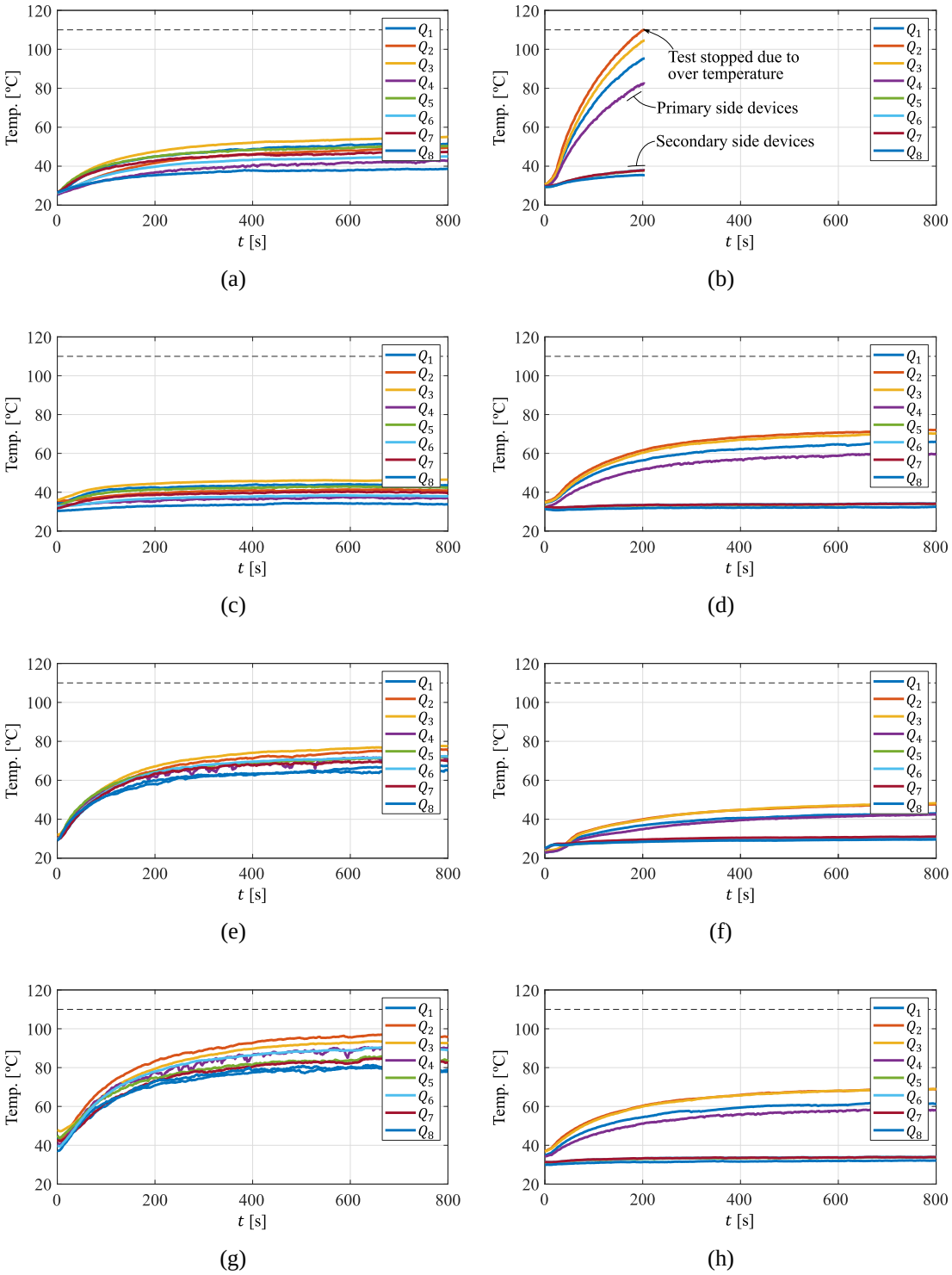


Fig. 4.17. Temperature evolution, boost mode. "Test point 1" (a) IHB-FPC. (b) DAB-PPC. "Test point 2" (c) IHB-FPC. (d) DAB-PPC. "Test point 3" (e) IHB-FPC. (f) DAB-PPC. "Test point 4" (g) IHB-FPC. (h) DAB-PPC.

Table 4.10. Experimental results comparison between the IHB-FPC and the DAB-FPC. Base current (8 A) and base voltage (300 V) are chosen for the electrical stress.

Parameter		IHB-FPC	DAB-PPC
Volume	Inductor	4x126 cm^3	223 cm^3
	Transformer	-	223 cm^3
Overall η_{sys}	Buck mode	99.0 %	98.98 %
	Boost mode	99.1 %	98.87 %
Thermal stress		Distributed in the four HBs	Predominant in the high-current side
Electrical stress	Inductor L	4x0.26 pu	0.48 pu
	Input capacitor C_{in}	0.50 pu	0.42 pu
	Output capacitor C_{out}	0.15 pu	1.76 pu
	Switching devices	0.53 - 0.31 pu (Q_1 - Q_2)	0.35 - 0.28 pu (Q_{1-4} - Q_{5-8})

4.2.7 Conclusion

This case study compares the performance of two DC-DC converters: a IHB-FPC and a DAB-PPC. Both solutions are non-isolated from the system point of view, and they are designed and experimentally tested for the same application. The results show that the DAB-PPC has improved performance than the IHB-FPC in aspects such as: lower volume of magnetics and reduced electrical stress of magnetics and switching devices. Regarding the efficiency, the results show that the DAB-PPC is penalized at a low V_{load} or, in other words, high K_{pr}. As the power processed by the converter is reduced, the efficiency of the DAB-PPC outperforms the IHB-FPC. However, the IHB-FPC presents a higher overall efficiency. The thermal analysis concludes that the power losses of the DAB-PPC are mainly focused on the high current side. Indeed, the maximum top-case temperature achieved at the secondary side is below 40 ºC. On the other hand, the IHB-FPC distributes the heat in the four HBs. This benefits the DAB-PPC in case an external fan is implemented.

4.3 Si-Based PPC vs SiC-Based FPC

Higher energy efficiency and reduced power converter size are the main benefits that WBG devices present as compared to conventional Si based semiconductors [14], [15]. Furthermore, these WBG semiconductors enable devices to operate at much higher voltages/temperatures (typical application of SiC) and higher frequencies (typical application of GaN) than the conventional Si semiconductors [16]. Consequently, the

power converters utilized in applications such as solar, traction, and EV are being enabled with WBG-based devices [17]. On the other hand, Si-based devices are a very mature technology, and so they still dominate the market of power devices due to their reduced cost and ruggedness. However, their performance has reached its theoretical limitations in terms of power density and switching capability [105].

The reduced power processed by the converter and lower voltage/current stress can help conventional Si-based devices to compete with upcoming SiC-based devices. Si-based devices are a very mature technology, and their market offers a large and highly competitive semiconductor variety. So, if these advantages of Si-devices are combined with the benefits of PPP, then a Si-based PPP topology may provide better solutions than a WBG-based FPP solution. This subchapter aims to (i) demonstrate the enhanced performance of Si-based PPCs respect to SiC-based FPCs and (ii) show the benefits that PPP can bring to the life extension of Si-based technology.

4.3.1 System Description

This case study focuses on an on-board charger (OBC) application. Usually, an OBC is divided in two main stages [7]: AC-DC rectification stage and DC-DC stage. The AC-DC stage operates as power factor corrector (PFC) and it also regulates the DC link voltage between both stages. The DC-DC controls the charging current of the battery of the EV. In relation to the normative around EV charging systems, at present, the majority of countries implement isolated DC-DC converters. However, the requirement of galvanic isolation for OBC application is not mandatory, and the application of non-isolated supply equipment is allowed for EV charging [106]. To be more precise, the countries that are included at the corrigendum of the IEC 61851-23 normative are the United States and Canada. Furthermore, the charger examples presented in [7] locate the isolation border at the AC or the DC stage. Therefore, if a PPC architecture is implemented on the DC stage, the AC-DC rectifier could provide galvanic isolation. This work is focused on the design of the DC-DC converter. Fig. 4.18 shows the schematic of the two topologies which are compared: a dual active bridge full power converter (DAB-FPC) and a dual active bridge partial power converter (DAB-PPC).

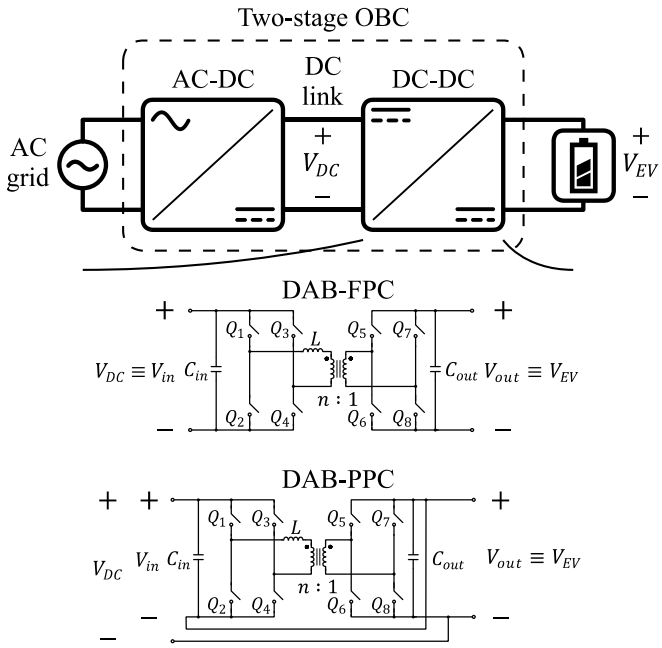


Fig. 4.18. Simplified diagram of the comparison under analysis: DC-DC stage of an OBC.

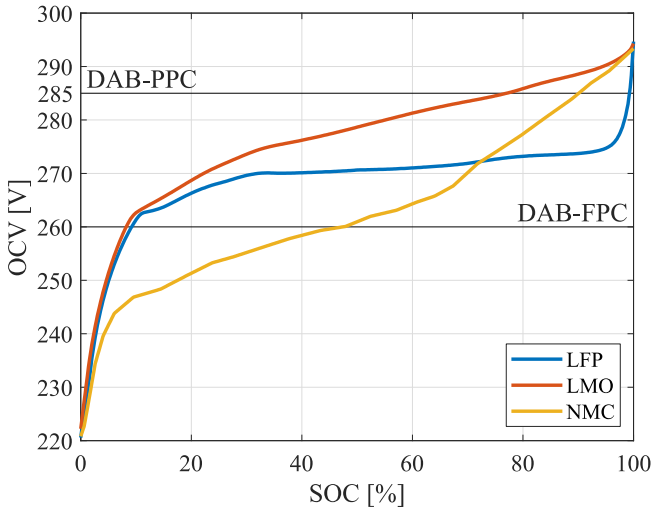


Fig. 4.19. OCV as a function of SOC for three different lithium-ion technologies. Two horizontal lines are highlighted at 260 V (DAB-FPC case) and 285 V (DAB-PPC case). These indicate specific working points that are discussed in detail later.

The concerned application consists of a constant DC source voltage of 300 V (V_{DC}) and the EV's battery voltage (V_{EV}), which is modelled as shown in Fig. 4.19. There, three different open-circuit voltage (OCV) vs. SOC curves are presented. Each of them represents a different lithium-ion technology: lithium-iron-phosphate (LFP), lithium-manganese-oxide (LMO) and nickel-manganese-cobalt (NMC) [107]. The LFP presents a flat profile from 20 % to 95 % SOC. The LMO and the NMC show linear profiles above

10 % SOC values. The aim of considering batteries of three different chemistries is to demonstrate the impact of each of them on the performance of the DAB-FPC and the DAB-PPC.

Regarding the DAB-PPC, since the application consists of a voltage step-down, an ISOP architecture is implemented. This way, reduced voltage level is expected at the primary side ($V_{in} = V_{DC} - V_{EV}$) and reduced current at the secondary side ($I_{out} = I_{EV} - I_{DC}$). The DAB topology is selected for its bi-directionality and zero voltage switching (ZVS) operation. In this work, the DAB is controlled with single PSM due to its ease of implementation [108]. To utilize the benefits of Si-devices, the DAB-PPC is enabled using Si-devices. The DAB-FPC is enabled using state of the art SiC semiconductors. This way, it is expected to observe the benefits that PPP can bring to the life extension of Si based semiconductor.

Table 4.11 defines the electrical design parameters of both converters. The first noticeable difference between the two solutions is V_{in}. In the case of the DAB-PPC a maximum voltage of 80 V is expected, which permits the implementation of lower voltage class and better conducting semiconductors ($R_{DS}{\sim}V_{DS}^{2.5}$ [91]) in the primary side bridge (Q_{1-4}). This will result in lower conduction losses in the primary bridge of the converter. The voltage reduction at the primary side especially benefits Si technology, whose market offers a great variety of semiconductors at a lower cost. Also, a three times lower peak power is expected at the DAB-PPC.

The main drawback of the DAB-PPC is that for certain operating conditions, the converter can operate in non-ZVS regions. This is due to the fact that it has a greater

Table 4.11. Charging unit electrical parameters.

Parameter	Value	
	DAB-FPC	DAB-PPC
V_{DC}	300 V	300 V
V_{EV}	From 220 V to 295 V	From 220 V to 295 V
V_{in}	300 V	From 80 V to 5 V
V_{out}	From 220 V to 295 V	From 220 V to 295 V
$\lvert\widehat{P_{conv}}\rvert$	3 kW	1.05 kW

operation range. As it can be observed in Table 4.11, the DAB-FPC works with a fixed input voltage ($V_{in_{\text{DAB-FPC}}} = V_{DC}$) and a variable output voltage ($V_{out} = V_{EV}$). Whereas, the DAB-PPC contains a variable input voltage ($V_{in_{\text{DAB-PPC}}} = V_{DC} - V_{EV}$) and a variable output voltage ($V_{out} = V_{EV}$). In consequence, the voltage gain observed by the DAB ($M = \frac{V_{out} \cdot n}{V_{in}}$) extends its operation range.

4.3.2 Analytical Modelling

The same DAB model from subchapter 4.2.2.2 and power losses calculus from subchapter 4.2.3 are used for the present analysis. Estimation of switching loss requires identification of the ZVS boundary for DAB-FPC and DAB-PPC architectures. Therefore, as a first step, the boundaries of the ZVS regions of each solution are calculated following the steps described in [109].

Fig. 4.20 presents the ZVS regions of each solution in function of M and the phase-shift (ϕ). The orange areas represent the hard switching region and the grey ones represent the iZVS region. The iZVS is easier to observe in Fig. 4.20a (DAB-FPC case) because of its lower M range. The dashed line represents the trajectory of the operating points of the converter through a complete charging process. As it can be observed, at both solutions, this line keeps a constant ϕ value at 60º (nominal ϕ). This corresponds to an ideal lossless behavior of the converter through the constant-current (CC) charging strategy. In reality, the phase-shift will suffer slight variations that must be corrected by a closed-loop control.

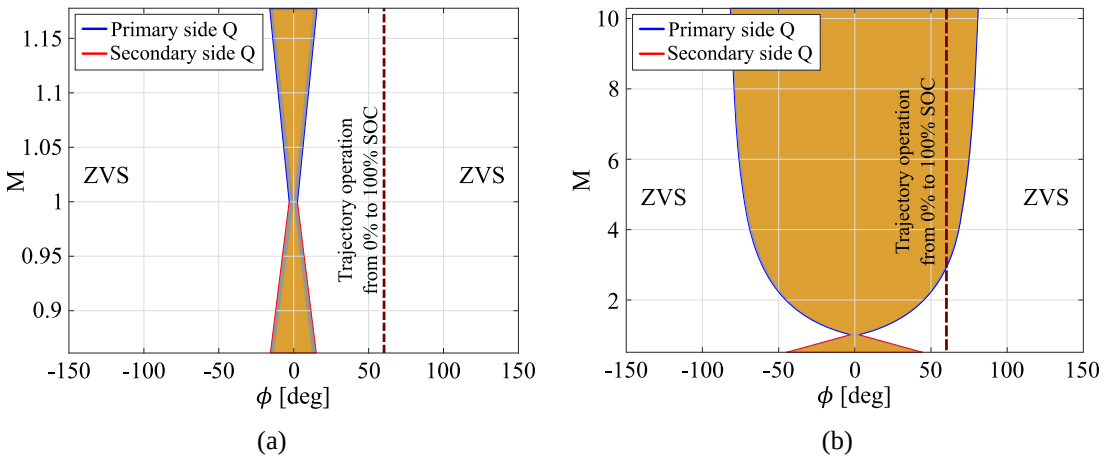


Fig. 4.20. ZVS regions and boundaries for primary and secondary side semiconductors using PSM. (a) DAB-FPC. (b) DAB-PPC.

In the case of the DAB-FPC (Fig. 4.20a), the dashed line never enters in to the orange or grey areas, which means that its semiconductors will always operate under soft switching conditions. However, the DAB-PPC (Fig. 4.20b) does enter inside the non-ZVS areas when M>3. In this condition, the semiconductors from the primary side do not commute under ZVS and their switching losses increase. Nevertheless, during non-ZVS operation (M>3), V_{EV} is at 280 V. Consequently, the voltage switched by the primary side semiconductors will only be 20 V or less. Therefore, a very low increment of the switching losses increment is expected.

4.3.2.1 Control Strategy

A CC charging operation of the battery is considered for comparative evaluation. A closed-loop control strategy is implemented for both solutions and is shown in Fig. 4.21. It is assumed that the DC link (V_{DC}) is externally regulated. I_{ref}^{*} is the reference current during the CC mode and it is chosen based on the battery specifications. The difference between I_{ref}^{*} and the battery current (I_{EV}) is fed to a proportional-integral (PI) type current controller. The PI controller generates the phase shift to control the current output of the converters. Due to the low dynamics of the battery system charging process, the response of the closed-loop control does not require a high bandwidth.

4.3.3 Simulation and Experimental Results

The experimental prototype under analysis is the same presented in the previous case study. Fig. 4.22a and Fig. 4.22b show a real image of the set up for the present analysis. The feature of this prototype is that the selected footprint for the MOSFETs (D^2PAK7) allows implementing SiC and Si technologies. Also, the top-case temperature of the semiconductors is measured using a thermocouple data logger, and an external fan (NMB-MAT 4715FS-12T-B50) is used to cool the devices.

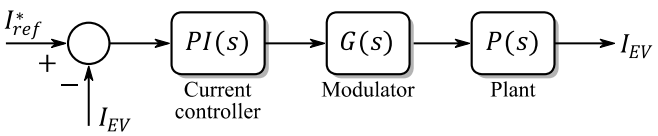


Fig. 4.21. CC closed-loop control strategy.

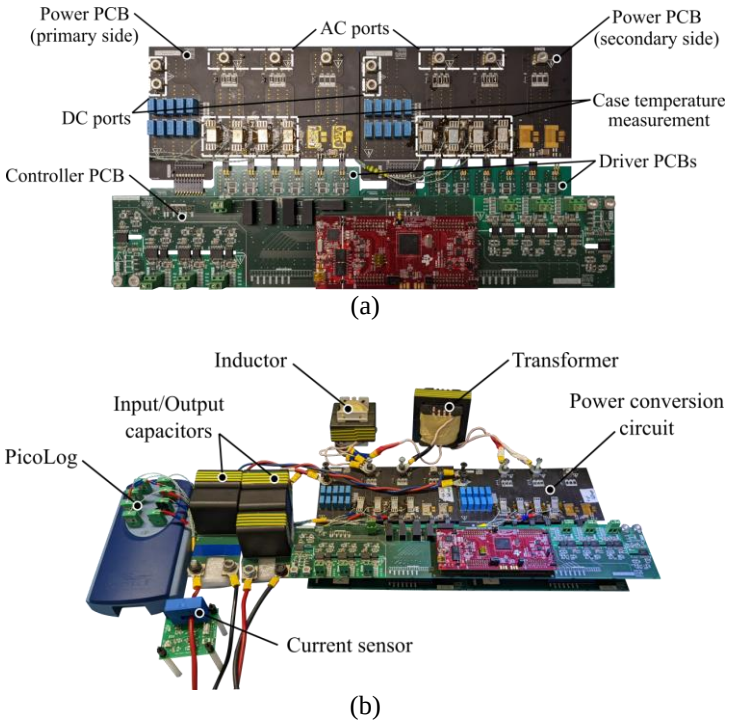


Fig. 4.22. Experimental prototype. (a) Power conversion circuit. (b) Test set-up.

Table 4.12 describes the design parameters and the implemented devices of the SiC-based DAB-FPC and the Si-based DAB-PPC. The Si MOSFETs from Table 4.12 (IRFS4115-7P and IPBE65R075CFD7A) are 2.5 times cheaper than the SiC MOSFET (IMBG65R022M1H). When it comes to SiC, the lower voltage class that can be found in the market is 600 V. Therefore, the advantage of implementing reduced voltage semiconductors is not applicable for SiC devices, at least for the concerned application. GaN technology does offer lower voltage class semiconductors. However, their current capabilities are much lower and their implementation is focused on high frequency applications [15], [110].

The details of the magnetics for both DAB-FPC and DAB-PPC are given in Table 4.13. A transformer with higher volume is needed for the DAB-FPC than the DAB-PPC. The volume is defined as the minimum box which can be put around the active part of the core and windings, which is given by (4.42). The results show that the transformer of the DAB-FPC is 1.64 times bigger than the one required for the DAB-PPC. The litz wire is defined as the number of wires (N_w), times the number of strands (N_{st}), times the

Table 4.12. Design parameters and selected devices of the SiC-based DAB-FPC and the Si-based DAB-PPC.

Parameter	SiC-based DAB-FPC	Si-based DAB-PPC
f_{sw}	40 kHz	40 kHz
C_{in}	MKP1848C71050JY5[14]	MKP1848C71050JY5[14]
C_{out}	MKP1848C71050JY5[14]	MKP1848C71050JY5[14]
n	1.2	0.2
L	100 µH	15 µH
Q_{1-4}	IMBG65R022M1H[15]	IRFS4115-7P[16]
Q_{5-8}	IMBG65R022M1H[15]	IPBE65R075CFD7A[17]

Table 4.13. Magnetics' manufacturing parameters.

Parameter	DAB-FPC		DAB-PPC	
	Inductor	Transformer	Inductor	Transformer
Core	EE6527 (CF 139)	EE8020 (CF 139)	EE6527 (CF 139)	EE6527 (CF 139)
Volume	223 cm^3	367 cm^3	223 cm^3	223 cm^3
Nº of turns	16	36:30	10	6:30
Wire	2x95x200 (9.1 cm^3)	1x630x100 (25.9 cm^3)	1x95x200 (2.8 cm^3)	1x95x200 (10.2 cm^3)

diameter of each strand in µm. The resulting volume of the wire is shown between parentheses, which is given by (4.44).

$$Volume_{wire} = N_w \cdot N_{st} \cdot \pi \cdot r_s^2 \cdot N_t \cdot P_E \quad \textbf{(4.44)}$$

Where r_s is the radius of the strand, N_t is the number of turns and P_E is the perimeter of the inner rectangle of the E core.

The results show that the DAB-PPC requires less wire volume: 3.2 times lower (inductor case) and 2.5 times lower (transformer case). This size reduction in the volume of the magnetics and wire also entails a less costly solution.

[14] 100 µF (C_{in}: 3 parallel connected; C_{out}: 2 parallel connected)
[15] V_{DS}=650 V , R_{DS}=31 mΩ @T_j=175 ºC [SiC]
[16] V_{DS}=150 V , R_{DS}=28.9 mΩ @T_j=175 ºC [Si]
[17] V_{DS}=650 V , R_{DS}=139 mΩ @T_j=150 ºC [Si]

Regarding the experiments, these consist of a full charge of the lithium-ion batteries from Fig. 4.19. A DC power supply is used to act as the DC link and a battery emulator is used to emulate their characteristics. The current reference of the converter is set to 10.2 A and a battery capacity of 2.55 Ah is selected. This configuration ensures a 15 minute charge, time enough to observe the effect of the different OCV vs. SOC curves.

4.3.3.1 Results

In the first place, Fig. 4.23 and Fig. 4.24 present the experimental waveforms of the inductor current (i_L), the primary side semiconductor voltage (v_{Q_1}) and the secondary side semiconductor voltage (v_{Q_5}).

Fig. 4.23 shows the results of the DAB-FPC for three different working points: initial charging point (Fig. 4.23a), midpoint (Fig. 4.23b) and end of charging (Fig. 4.23c). The waveforms of v_{Q_1} and v_{Q_5} show that the maximum voltage blocked by Q_1 and Q_5 is 300 V. This confirms the necessity of implementing 650 V devices. Focusing on the

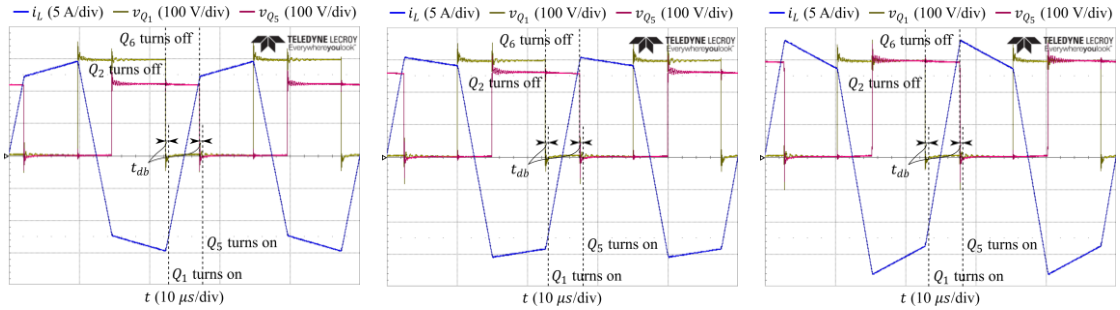


Fig. 4.23. Experimental waveforms of the DAB-FPC with SiC MOSFETs. (a) Initial charging point (V_{EV}=220 V). (b) Midpoint (V_{EV}=260 V). (c) End of charging (V_{EV}=295 V). All semiconductors work under ZVS.

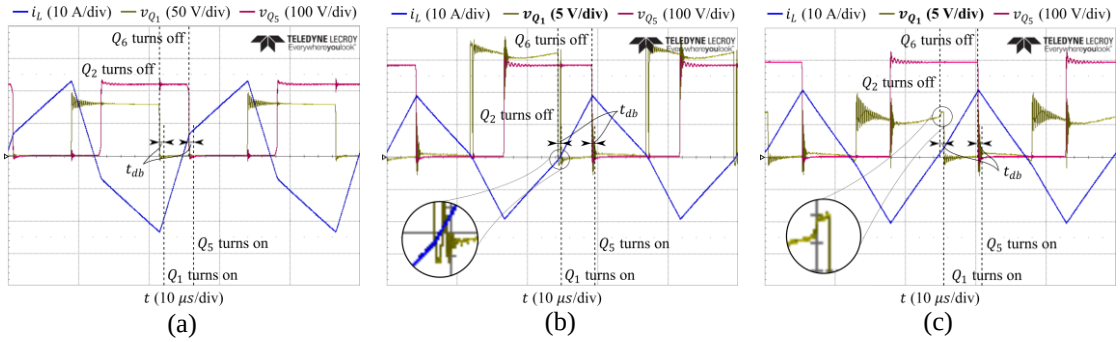


Fig. 4.24. Experimental waveforms of the DAB-PPC with Si MOSFETs. (a) Initial charging point (V_{EV}=220 V). (b) Midpoint where primary side semiconductors get out the ZVS region (V_{EV}=285 V). (c) End of charging. (V_{EV}=295 V).

switching, Fig. 4.23 demonstrates that, from the beginning to the end of the charging process, the DAB-FPC ensures ZVS for all the semiconductors. In the three working points, when Q_2 turns off, a negative i_L helps to charge/discharge the output capacitors. Then, after t_{db} finishes Q_1 turns on with zero voltage. Same thing occurs with $Q_{5,6}$, but with a positive flow of i_L.

Fig. 4.24 presents the experimental waveforms of the DAB-PPC: initial charging point (Fig. 4.24a), midpoint where the primary side semiconductors enter in non-ZVS region (Fig. 4.24b) and end of charging (Fig. 4.24c). Compared to the DAB-FPC, in the DAB-PPC, the waveforms of v_{Q_1} show that the maximum blocked voltage by Q_1 is 80 V (Fig. 4.24a), which demonstrates that the primary side semiconductors only block the voltage difference between the DC source and the battery. This value decreases down to 5 V as the battery charges. This can be seen in Fig. 4.24b and Fig. 4.24c, where the blocking voltage of Q_1 is 15 V and 5 V, respectively. Although an electromagnetic interference (EMI) analysis is out of the scope of this work, it can be concluded that due to this low switching voltage at the primary side, the common-mode and differential-mode voltage is reduced [111]. On the other hand, v_{Q_5} shows that the maximum voltage blocked by Q_5 is 300 V, same as in the DAB-FPC case.

Regarding the switching of the DAB-PPC, its waveforms confirm that soft and hard switching conditions occur at the primary side. Firstly, in Fig. 4.24a, a ZVS operation mode can be observed. Similar to the DAB-FPC, when Q_2 or Q_6 turn off, a negative or positive flow of i_L helps to charge/discharge the output capacitors respectively. Once t_{db} finishes, Q_1 and Q_5 turn on with zero voltage. Secondly, Fig. 4.24b shows the moment in which the primary side semiconductors leave the ZVS region. This occurs when the battery voltage is around 285 V. At this moment, when Q_2 turns off, a negative flow of i_L helps to charge/discharge the output capacitors. However, during t_{db}, the i_L reverses its flow from negative to positive. Please observe the zoomed area from Fig. 4.24b. The positive flow of i_L charges the output capacitor of Q_1, provoking a voltage increment of v_{Q_1}. This increment does not last long, since t_{db} finishes and Q_1 turns on. On the other side, Q_5 continues under ZVS conditions. Thirdly, in Fig. 4.24c, a clear example of hard switching of Q_1 is observed. In this case, when Q_2 turns off, the positive flow of i_L does not help to charge/discharge the output capacitors of Q_1 and Q_2. At this moment, its body

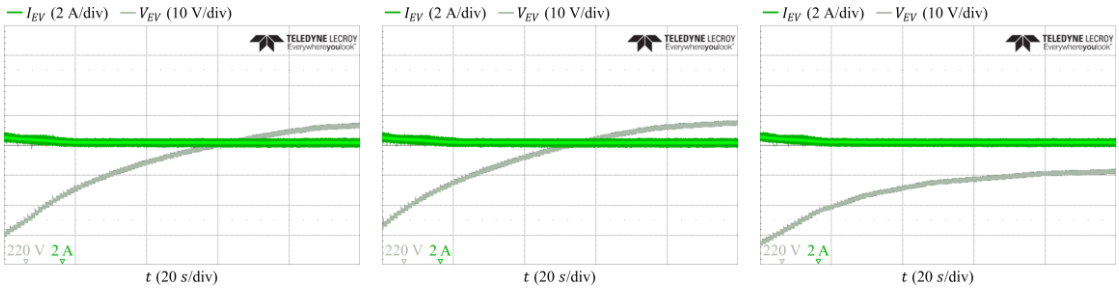


Fig. 4.25. Experimental battery current and voltage. (a) LFP. (b) LMO. (c) NMC.

diode starts conducting, provoking a slight voltage increment, see the zoomed area. Then, Q_1 turns on with all this blocking voltage, which is only 5 V. To sum up, the only semiconductors that commute under hard switching conditions at the DAB-PPC are the ones at the primary side. Nevertheless, they get out from the ZVS region when the battery surpasses the 285 V. At this point, the primary side voltage is only 15 V, so the switching losses barely have an impact in the efficiency. This is discussed in detail later.

To demonstrate the CC control, the battery current (I_{EV}) and voltage (V_{EV}) are shown in Fig. 4.25a (LFP case), Fig. 4.25b (LMO case) and Fig. 4.25c (NMC case). As it can be observed, the current keeps a constant value as the battery voltage increases.

The top-case temperature comparison of the most heated MOSFET is shown in Fig. 4.26. The considered device from the DAB-FPC corresponds to the secondary side and the one from the DAB-PPC corresponds to the primary side. Both devices belong to the high current side. It is interesting to note that the temperature profile of SiC-MOSFETS in DAB-FPC present a similar curve to the OCV profiles from Fig. 4.19. This is because as the voltage increases from 220 V to 295 V, the switching losses for the devices on the secondary side increase proportionally. It should be also noted that among the three different battery chemistries, the NMC chemistry has a lower temperature in initial charging conditions. This behavior of top-case temperature with NMC chemistry is correlated with the OCV vs SOC curve. The NMC chemistry has lower OCV than LFP and LCO chemistries at low SOCs. Thus, the switching losses of the devices for NMC chemistry are lower than with LCO and LFP chemistries. This changes at higher SOC values, where the LFP keeps a lower voltage than the other two technologies. The maximum top-case temperature after considering the three battery chemistries is around 79 ºC.

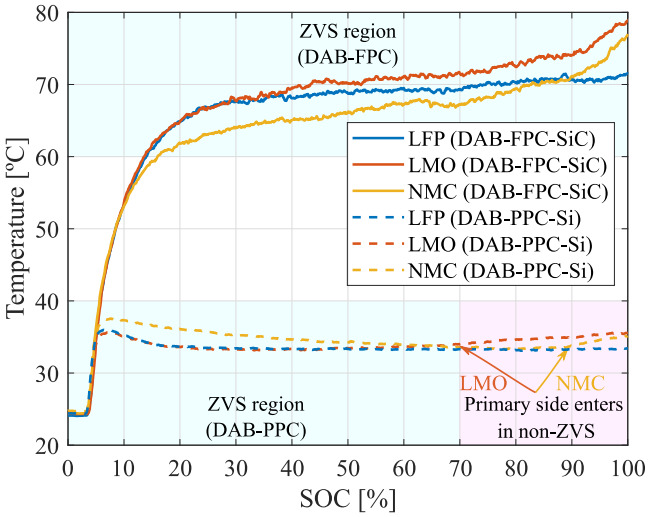


Fig. 4.26. Top-case temperature evolution of the most heated semiconductor.

For the DAB-PPC architecture, the temperature profile is quite different. Apart from the fact that the maximum top-case temperature is much lower (37.6 ºC), its curve decreases as the battery charges. This is strictly related to the K_{pr}. As the battery is charged, its voltage gets closer to the 300 V, which reduces the K_{pr}, thus the power processed by the converter. This is observable at the NMC temperature curve. Since its OCV profile presents lower voltage values than the LMO and LFP, the power processed by the DAB-PPC is higher at a low SOC when charging an NMC. For this reason, the NMC profile presents higher temperatures at the beginning. Above SOC 70 %, the effect of operating in the non-ZVS region can also been seen. At this point, the OCV with LMO chemistry surpasses the 285 V (Fig. 4.19), thus leading to hard switching of devices. This leads to an increment in the switching losses and hence in the temperature of the primary side devices. Similar behaviour is observed with the NMC chemistry when SOC>90 %. For the LFP chemistry, the battery voltage exceeds 285 V when the battery is almost completely charged. Thus, the impact of hard switching events with LFP chemistry is minimal. Due to the temperature dependency of the on-state resistance, the low thermal stress achieved with the DAB-PPC results in better conduction characteristics.

Fig. 4.27 presents the comparison of efficiency of the two architectures using analytical models and experiments. Fig. 4.27a compares the results of the DAB-FPC with SiC. As it can be observed, the analytical and experimental results show that the efficiency slightly reduces as the battery charges. The effect of the OCV-SOC curves is

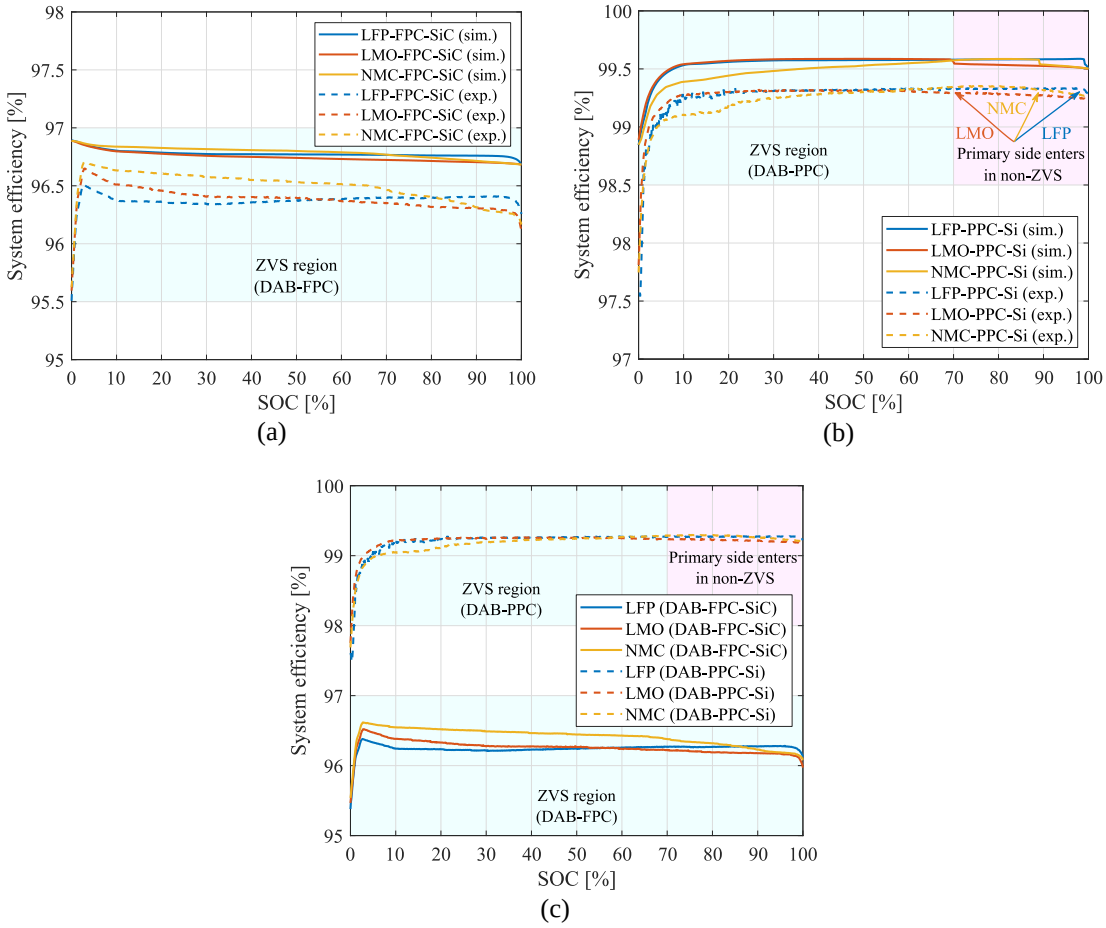


Fig. 4.27. Numerical simulation and experimental efficiency results. (a) DAB-FPC with SiC. (b) DAB-PPC with Si. (c) Only experimental results.

also noticeable, since the NMC obtains higher efficiencies than the other two battery technologies at low SOCs. This is directly related to the temperature curves from Fig. 4.26.

Fig. 4.27b compares the simulation and experimental efficiency results of the DAB-PPC with Si-devices. As it can be observed, both show a lower system efficiency when a NMC battery is charged. Especially at initial charging conditions, when a lower OCV profile causes higher K_{pr} values. Also, the numerical simulations and experimental tests present a slight efficiency drop when the DAB-PPC enters in hard switching conditions. This occurs when the SOC reaches 70 % (LMO case), 90 % (NMC case) and 99 % (LFP case). This is a direct consequence of their OCV curves surpassing 285 V (Fig. 4.19).

The experimental results from both solutions are compared in Fig. 4.27c. It is clear that the DAB-PPC with Si MOSFETs is more efficient than the DAB-FPC with SiC

MOSFETs. Indeed, the DAB-FPC does not reach a 97 % efficiency, while the DAB-PPC presents efficiencies higher than 99 % through nearly all the charging process. Similarly to the temperature curves, the NMC profile has visible differences at the efficiency curves. In the case of the DAB-FPC, the lower voltage of the NMC affects positively to the efficiency. However, in the case of the DAB-PPC the contrary occurs.

Table 4.14 summarizes the total energy losses (based on subchapter 2.3.4) of each solution and its weight in comparison to the total energy charged. Both, numerical solutions and experimental results conclude that the Si-based DAB-PPC is the most efficient. Also, it can be observed how the different OCV-SOC curves of the battery chemistries impact each solution. For example, the DAB-FPC achieves its lowest E_{loss} values when an NMC battery is implemented. However, in the case of the DAB-PPC, the NMC provokes higher E_{loss} than the other two technologies. As discussed before, this is because of the NMC's low OCV at initial charging conditions.

Table 4.14. Total energy losses through the battery charging process.

Parameter		SiC-based DAB-FPC		Si-based DAB-PPC	
		E_{loss} [Wh]	$\frac{E_{loss}}{E_{charged}} \cdot 100$ [%]	E_{loss} [Wh]	$\frac{E_{loss}}{E_{charged}} \cdot 100$ [%]
LFP	Sim.	22.76 Wh	3.33 %	3.06 Wh	0.45 %
	Exp.	26.79 Wh	3.90 %	5.39 Wh	0.78 %
LMO	Sim.	23.69 Wh	3.36 %	3.20 Wh	0.47 %
	Exp.	27.50 Wh	3.89 %	5.59 Wh	0.79 %
NMC	Sim.	22.34 Wh	3.32 %	3.41 Wh	0.51 %
	Exp.	25.15 Wh	3.73 %	5.50 Wh	0.81 %

Table 4.15. Electrical stress comparison at worst case. Base current (10 A) and base voltage (300 V) are chosen based on the maximum battery current and voltage respectively.

Parameter	SiC-based DAB-FPC	Si-based DAB-PPC
VA rating of the inductor L ($V_{rms}I_{rms}$)	2.09 pu	0.43 pu
Stress in C_{in} ($V_{pk}I_{rms}$)	0.99 pu	0.37 pu
Stress in C_{out} ($V_{pk}I_{rms}$)	1.30 pu	1.01 pu
Stress in Q_{1-4} ($V_{pk}I_{rms}$)	1.03 pu	0.30 pu
Stress in Q_{5-8} ($V_{pk}I_{rms}$)	1.22 pu	0.17 pu

Finally, Table 4.15 presents the electrical stress seen by the passive and active devices [40], which is given by (4.45). Due to the reduced power processed by the converter, all the passive and active devices, the inductor, the capacitors and the semiconductors of the DAB-PPC present a lower electrical stress than the ones from the DAB-FPC (from 15 % to 77 %). The magnetics and the semiconductors are the components that benefit the most.

$$Component\ stress = \frac{V_{pk,rms} \cdot I_{rms}}{V_{base} \cdot I_{base}} \tag{4.45}$$

4.3.4 Discussion

With the aim of remarking the benefits and advantages of the Si-based DAB-PPC upon the SiC-based DAB-FPC, Table 4.16 summarizes the main improvements achieved with the PPP-based solution.

Firstly, the maximum top-case temperature of the switching devices is halved in the DAB-PPC. This reduction of the thermal stress improves the conduction characteristics of the semiconductors. In a second optimization process, this could lead to a reduction in the cooling system, which entails a lowered cost and volume. Secondly, the volume results of the DAB-PPC for the transformer and the wire are 1.6 and 2.7 times lower, respectively. This volume reduction can be related with a cost reduction of passive devices. Together with cheaper semiconductors, the Si-based DAB-PPC turns out as a less costly solution. Thirdly, the average energy losses achieved with the DAB-PPC are 3 points lower. Fourth, an electrical stress reduction of the magnetics, the capacitors and

Table 4.16. Main comparison parameters where a Si-based DAB-PPC outperforms a SiC-based DAB-FPC.

Parameter		SiC-based DAB-FPC	Si-based DAB-PPC
Maximum top-case temperature of Q		79 ºC	37.6 ºC
Volume	Inductor	223 cm^3	223 cm^3
	Transformer	367 cm^3	223 cm^3
	Total wire	35 cm^3	13 cm^3
Overall $\frac{E_{loss}}{E_{charged}} \cdot 100$		3.84 %	0.79 %
Electrical stress	Inductor L	2.09 pu	0.43 pu
	Input capacitor C_{in}	0.99 pu	0.37 pu
	Output capacitor C_{out}	1.30 pu	1.01 pu
	Primary side switch Q_{1-4}	1.03 pu	0.30 pu
	Secondary side switch Q_{5-8}	1.22 pu	0.17 pu

the switching devices is achieved with the DAB-PPC (from 15 % to 77 %). The inductor and the secondary side semiconductors are the devices that present a major reduction.

4.3.5 Conclusion

This case study discusses the advantages of Si-based PPCs against SiC-based FPCs. The wide and matured market of Si-devices and their low price makes them an ideal candidate to enable PPC architectures. To quantify the advantages of Si-enabled DAB-PPC architecture, an OBC application is analyzed in this work. Three different battery chemistries are considered to compare both architectures. The different OCV-SOC curves of each chemistry conclude that the same battery technology has a contrary effect on the performance of both solutions. Due to the benefits of PPP, the DAB-PPC architecture utilizes low blocking voltage semiconductors (with low on-state resistance) and its devices suffer a lower electrical stress. It is also shown that even though the PPC solution may lead to non-ZVS of devices in certain operating conditions, the overall efficiency and performance with respect to top-case temperature is much better of Si-based DAB-PPC than SiC-based DAB-FPC. Results using numerical simulations and a 3 kW experimental prototype demonstrate that the Si-based DAB-PPC has improved performance than SiC-based DAB-FPC in all metrics: thermal stress, efficiency, volume and cost.

Chapter 5

IPOS-ISOP ARCHITECTURE APPLICATIONS

This Chapter presents three applications where IPOS-ISOP type PPC architectures are studied for future implementation.

The first application is part of an European project which is focused on developing a hybrid ESS for maritime applications. Regarding the power conversion circuit, this project aims to find an optimal modular solution than can be scalable for further applications and voltage-power levels. Therefore, this case study is focused on the modularity of PPC solutions. The content from this case study corresponds to the article in revision [J5].

The second application consists of a DC-DC converter for hydrogen production. A power converter company showed an interest on the benefits that PPC architectures could bring to the power conversion circuit. This case study presents a design criteria of a PPC architecture based on the load voltage and power curves given by the company.

The third application is focused on the design of a PPC for EV fast charging applications. Via simulations and experimental results, the design of the converter is optimized oriented to energy losses (Wh) and not to power losses (W).

5.1 Description

The benefits of IPOS-ISOP type PPC architectures give reasons to research their viability on different type of applications. This Chapter presents three case studies where the implementation of IPOS-ISOP type architectures has been taken into consideration.

1. **Solutions for largE bAtteries for waterBorne trAnsporT (SEABAT).** This project aims to develop a modular power converter solution for a hybrid energy storage system (HESS). For this purpose, this case study is focused on analyzing the modularity of IPOS-ISOP type PPCs. Special interest is shown to the series connection of modular PPCs.
2. **Hydrogen generation.** A power converter company showed interest on implementing IPOS-ISOP type PPC architectures for hydrogen production. This case study presents a design criteria of a PPC architecture based on the load voltage and power curves given by the company.
3. **EV fast charging application.** This case study proposes a design methodology for a PPC based EV fast charging unit. The design of the converter is optimized oriented to energy losses (Wh) and not to power losses (W).

5.2 SEABAT

This project received funding from the European Union under grant agreement no. 963560 Horizon 2020. Its main goal is to develop a cost-effective HESS architecture for large marine applications that is scalable to at least 1 MWh and validated at a level of 300 kWh. For this purpose, different modular power converter solutions are analyzed to obtain the optimal solution. The solution suggested by Mondragon Unibertsitatea considers IPOS-ISOP type PPC architectures as a promising solution. This subchapter describes the steps to follow for the design of a modular PPC. Special interest is shown to the series connection of the PPC, since entails overvoltage issues that must be considered when sizing the final solution.

5.2.1 System Description

This case study focuses in a HESS design suitable for high energy (HE) and high power (HP) operations in the vessel. Fig. 5.1 shows the HESS configuration. Each DC-

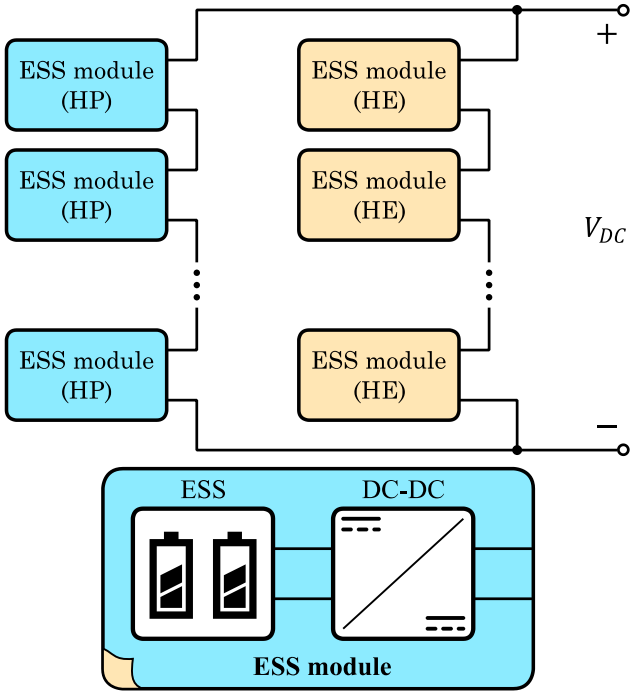


Fig. 5.1. The HESS architecture comprises strings of series-connected HP modules, connected in parallel with strings of series-connected HE modules.

Table 5.1. DC voltage and battery technologies.

Parameter	Description
V_{DC}	1000 V
HP battery technology	Toshiba SCiB 23 Ah LTO @ V_{cell} from 2 V to 2.7 V
HE battery technology	Samsung SDI 94 Ah NMC @ V_{cell} from 3.2 V to 4.13 V

DC converter is in charge of controlling the power flow of a single ESS. The group formed by an ESS and a DC-DC converter will hereinafter be referred as an *ESS module*. Depending on the cell technology used, the ESS modules can be HE or HP modules. The output of the ESS modules are connected in series, forming a string of several HE or HP modules to reach the desired string voltage. Note that the strings are only of one type, HE or HP, and that all the strings have the same voltage. Finally, different strings in parallel form the HESS. Table 5.1 defines the DC bus voltage and the selected battery technologies for the HE and HP ESS modules.

5.2.2 Modular PPC Dimensioning

The aim of this work is to design a modular PPC that can be scalable in series and parallel for different applications and a flexible battery system. This subsection describes

the design procedure to define the number of series connected modules (n_s) and the number of series connected cells per module (n_{cell_m}). Fig. 5.2 shows a simplified electric diagram of a single string. An IPOS type PPC architecture to step-up the ESS voltage to the DC voltage. As it can be observed, each module consists of 4 main voltages: battery cell voltage (V_{cell}), battery module voltage ($V_{bat} = n_{cell_m} \cdot V_{cell}$), converter output voltage (V_{out}) and ESS module output voltage ($V_{mod} = \frac{V_{DC}}{n_s} = V_{bat} + V_{out}$). V_{DC} is the DC bus voltage.

5.2.2.1 Preliminary Considerations

The K_{pr} curve of an IPOS architecture is defined as in (5.1).

$$K_{pr} = \frac{P_{conv}}{P_{mod}} = 1 - \frac{1}{G_V} \tag{5.1}$$

Where, P_{conv} is the power processed by the converter and P_{mod} is the power of a single ESS module. G_V is given by (5.2).

$$G_V = \frac{V_{mod}}{V_{bat}} = \frac{V_{DC}/n_s}{V_{bat}} \tag{5.2}$$

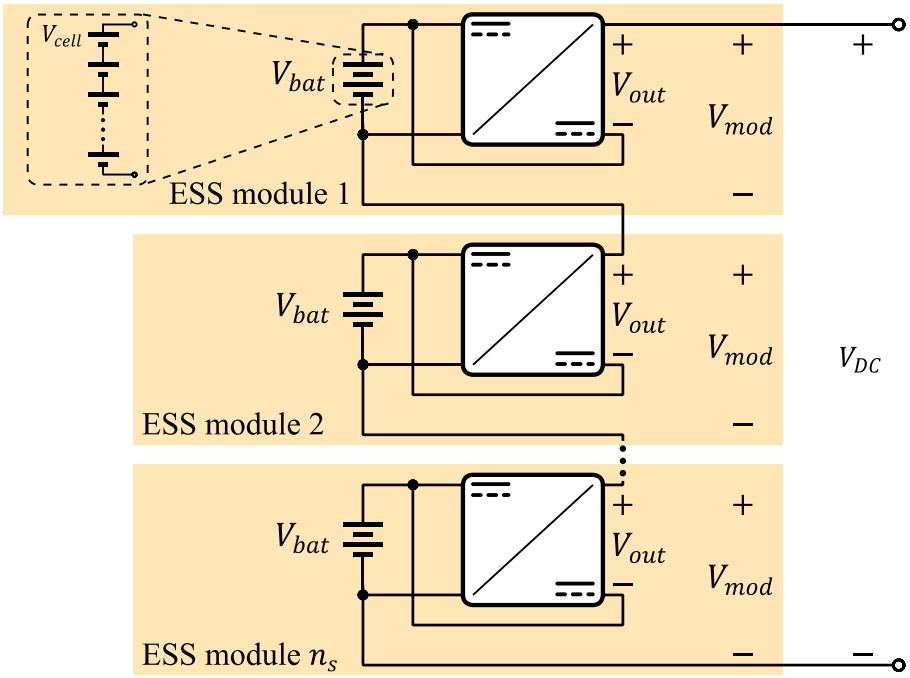


Fig. 5.2. Modular series configuration of the IPOS type PPC topology.

Considering that G_V is in function of a variable voltage (V_{bat}), its minimum and maximum values determine the minimum and maximum K_{pr}. In an ideal case, the minimum G_V is given when the maximum value of the battery ($V_{bat_{max}}$) coincides with V_{mod}. In this case, G_V obtains a value of 1 and the power processed by the converter is 0. However, as the battery discharges, V_{bat} reduces until the battery is totally discharged ($V_{bat_{min}}$). Expression (5.3) defines the maximum G_V range of the battery. Then, expression (5.4) computes the K_{pr}. K_{pr}^* represents the minimum value that can be defined for the design of the converter. If $K_{pr}<K_{pr}^*$, the converter is overloaded when the battery voltage reaches $V_{bat_{min}}$.

$$G_V^* = \frac{V_{mod}}{V_{bat_{min}}} = \frac{V_{bat_{max}}}{V_{bat_{min}}} = \frac{n_{cell_m} \cdot V_{cell_{max}}}{n_{cell_m} \cdot V_{cell_{min}}} = \frac{V_{cell_{max}}}{V_{cell_{min}}} \quad \textbf{(5.3)}$$

$$K_{pr}^* = 1 - \frac{1}{G_V^*} \quad \textbf{(5.4)}$$

Due to the fact that n_{cell_m} needs to be an integer number, it is very rare to make coincide the values of $V_{bat_{max}}$ and V_{mod}. Therefore, K_{pr} (also known as $K_{pr_{MAX}}$) must be defined slightly higher than K_{pr}^* (5.5). Then, the maximum permitted $G_{V_{MAX}}$ is obtained (5.6).

$$K_{pr_{MAX}} > K_{pr}^* \quad \textbf{(5.5)}$$

$$G_{V_{MAX}} = \frac{1}{1 - K_{pr_{MAX}}} \quad \textbf{(5.6)}$$

5.2.2.2 Number of Cells per Module

First, n_s is defined as a vector with integer values from 2 to 20. Second, n_{cell_m} is computed for each n_s, which is given by (5.7),(5.8).

$$V_{bat_{min}} = \frac{V_{mod}}{G_{V_{MAX}}} = \frac{V_{DC}/n_s}{G_{V_{MAX}}} \quad \textbf{(5.7)}$$

$$n_{cell_m} = \left\lceil \frac{V_{bat_{min}}}{V_{cell_{min}}} \right\rceil \quad \textbf{(5.8)}$$

Finally, the minimum and maximum value of V_{bat} is computed for each value of n_{cell_m}, see (5.9),(5.10).

$$V_{bat_{min}} = n_{cell_m} \cdot V_{cell_{min}} \quad \textbf{(5.9)}$$

$$V_{bat_{max}} = n_{cell_m} \cdot V_{cell_{max}} \quad \textbf{(5.10)}$$

Due to the cell operation in (5.8), the resulting $V_{bat_{max}}$ from (5.10) may be higher than V_{mod}. This would suppose a voltage step-down working condition ($G_V < 1$), which implies a bipolar V_{out} and a more complex circuit. For this reason, it must be ensured that G_V gives a value greater than 1 for each n_s. In case the resulting G_V is lower than 1, that n_s is deleted.

5.2.2.3 Number of Modules

The total number of modules of the final solution is the result of the product between the modules connected in series and the number of strings connected in parallel. The number of strings is given by the total maximum power of the application and the power capability of the batteries. However, the number of modules in series is not so evident. This subchapter aims to describe the steps followed to define the necessary number of modules in series.

PPC architectures achieve to reduce the power processed by the converter and they allow implementing lower rated components. Bearing this in mind, this analysis proposes to optimize this reduction by considering that, in case an ESS module fails, the rest of the modules connected in series must assume the resulting overload. The present analysis aims to select the value of n_s that minimizes the overload of K_{pr} and V_{out}.

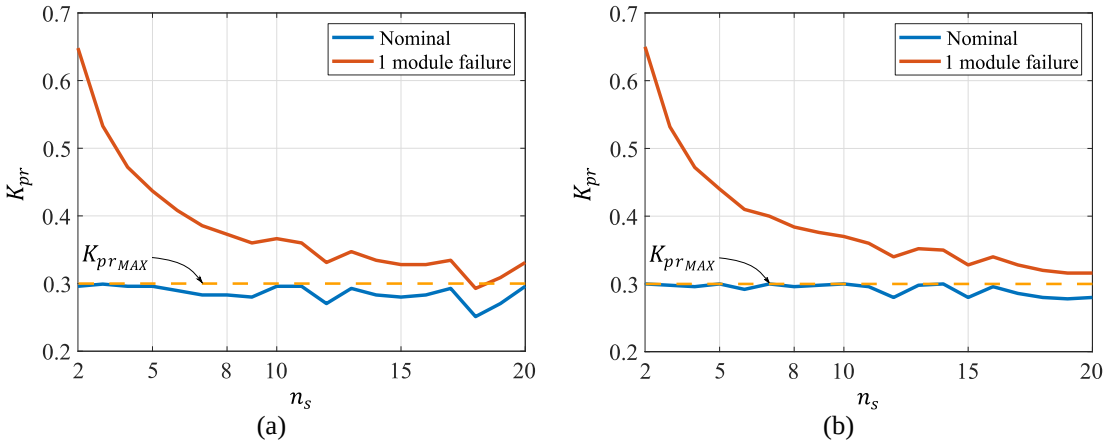


Fig. 5.3. K_{pr} increment for one module failure (a) NMC. (b) LTO.

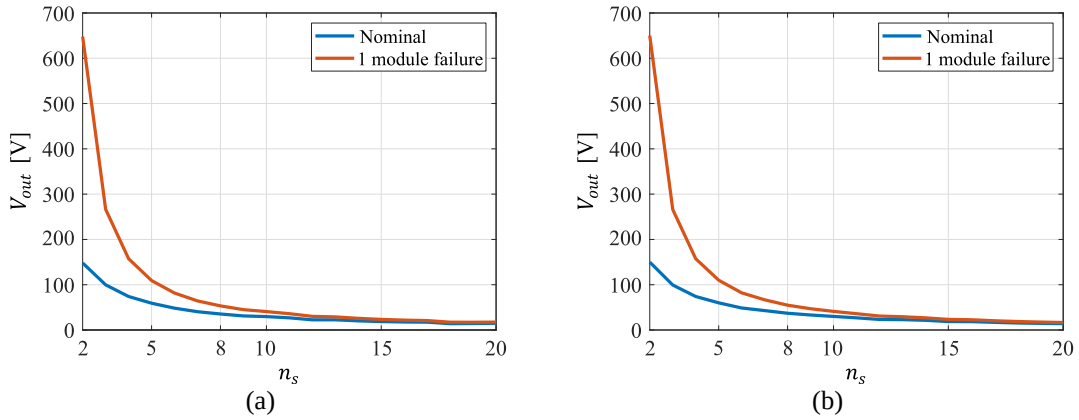


Fig. 5.4. V_{out} increment for one module failure (A) NMC. (B) LTO.

Fig. 5.3 presents the K_{pr} increment of a single ESS module in case another ESS module from the same string fails. As it can be observed, as n_s increases, the K_{pr} increment reduces. This means that the more ESS modules are implemented in series, the less overload exists in case of one of them fails. The results from Fig. 5.3a correspond to the NMC technology and the results from Fig. 5.3b to the LTO technology.

Fig. 5.4 shows the V_{out} increment of a single ESS module in case another ESS module from the same string fails. Similar to the K_{pr}, as the value of n_s increases, a lower overvoltage is expected at the output of the converter in case one of the modules fails. Based on these results, n_s=8 is selected. With this value, the expected overvoltage for both technologies (NMC and LTO) goes from 37 V to 55 V. This way, a 100 V rated switching device can be implemented without taking any risk.

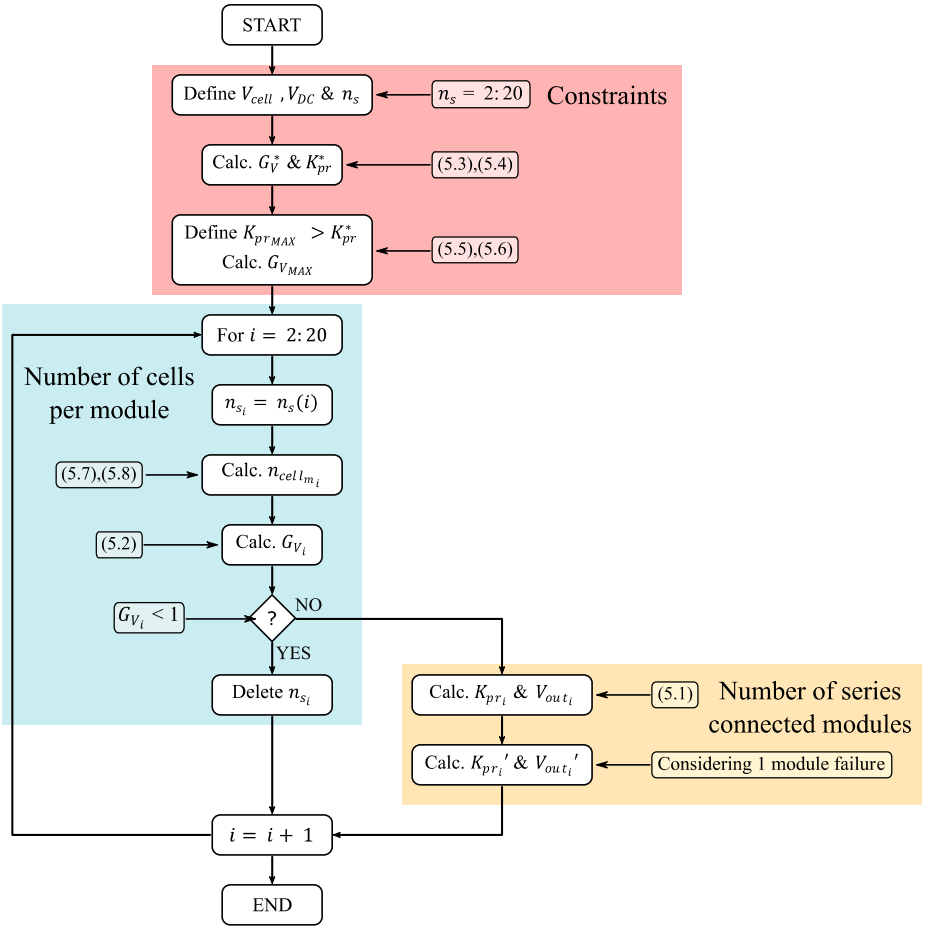


Fig. 5.5. Block diagram of the number of cells (n_{cell_m}) and number of series connected modules (n_s) selection process.

Once n_s=8 is defined, the number of cells per module (n_{cell_m}) is calculated for each battery technology by using (5.7),(5.8): n_{cell_m}=28 (NMC) and n_{cell_m}= 44 (LTO).

To sum up, Fig. 5.5 presents a flowchart of the previously discussed steps.

5.3 Hydrogen Generation

The European Commission confirmed that the role of hydrogen in the European Union's energy and greenhouse gas emission abatement efforts will rapidly increase [112]. This entails economical support for the projects that are focused on the development and implementation of technologies for hydrogen production. For hydrogen to deliver a positive role in the energy transition, it must be produced and delivered to end users in a sustainable manner (energy efficiency, cost, volume…).

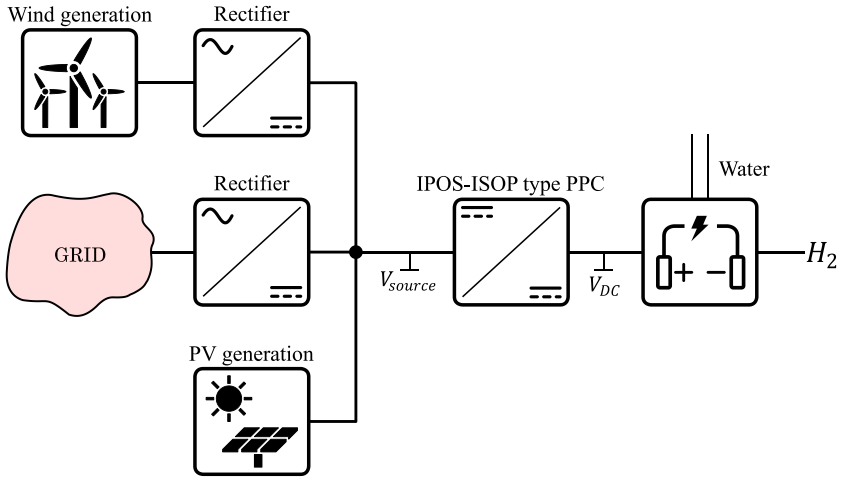


Fig. 5.6. Simplified single-wire diagram of a hydrogen production application.

Fig. 5.6 shows a simplified electric diagram of a hydrogen production application. Typically, an electrolysis process is used to split hydrogen from water using an electric current. The power to produce the electrolysis is obtained from the grid or from renewable energy sources, also known as green hydrogen. This work is focused on the design of the DC-DC converter in charge of supplying the DC voltage between the cathode and the anode. Due to the high power level of this application (MW level), PPC architectures are suggested for analysis. The reduction of the power processed by the converter is considered as a key factor for volume cost and losses reduction.

This case study describes a design criteria of the PPC based on the load voltage and power profiles. This includes the selection of the optimal IPOS or ISOP architecture for the concerned application, the calculus of the DC current/voltage values of the converter and the definition of the switching devices according to the quadrant analysis presented in subchapter 2.1.2.

The electrolyzer is characterized by two operating curves: beginning of life (BOL) and end of life (EOL). The power converter to be designed should feed the electrolyzer from the BOL to the EOL. The data for the electrolyzer under study is given in Table 5.2. Due to conflicts of interest, the data is given in per-unit. As it can be observed, a current increment of about 20 % is considered. The critical factor is the high current consumed by these electrolyzers, which can reach up to thousands of amperes. Fig. 5.7 plots the data from Table 5.2.

Table 5.2. Specifications of the case study for PPC design in electrolyzer.

Load level	I_{DC}	V_{DC}	
		BOL	EOL
120 %	1.2 pu	0.936 pu	1.035 pu
110 %	1.1 pu	0.917 pu	1.018 pu
100 %	1.0 pu	0.898 pu	1.000 pu
90 %	0.9 pu	0.878 pu	0.982 pu
80 %	0.8 pu	0.859 pu	0.965 pu
70 %	0.7 pu	0.839 pu	0.947 pu
60 %	0.6 pu	0.819 pu	0.928 pu
50 %	0.5 pu	0.800 pu	0.911 pu
40 %	0.4 pu	0.781 pu	0.893 pu
30 %	0.3 pu	0.760 pu	0.875 pu
20 %	0.2 pu	0.741 pu	0.858 pu
10 %	0.1 pu	0.722 pu	0.840 pu
0 %	0 pu	0.702 pu	0.822 pu

5.3.1 IPOS-ISOP Architecture Selection and Switching Devices

Analyzing the profiles from Fig. 5.7, BOL and EOL curves have the same characteristics. As the load increases, the voltage rises. The relationship between the load voltage and load current is linear.

Considering that the voltage gain between V_{source} and V_{DC} (see Fig. 5.6) is key to reduce the power processed by the PPC, the first important step is to define the value of V_{source}. In this case, V_{DC} has a minimum value of 0.702 pu (BOL curve) and a maximum value of 1.035 pu (EOL curve). Therefore, for the following analysis, 3 different values of V_{source} are considered: 0.632 pu (90 % of 0.702 pu), 0.966 pu (value between 0.702 pu and 1.035 pu) and 1.139 pu (110 % of 1.035 pu). The value of 0.632 pu ensures buck operation, the value of 1.139 pu ensures boost operation and the value of 0.966 pu requires buck-boost operation. The purpose of defining these 3 V_{source} values is to compare the results of a boost solution, a buck-boost solution and a buck solution.

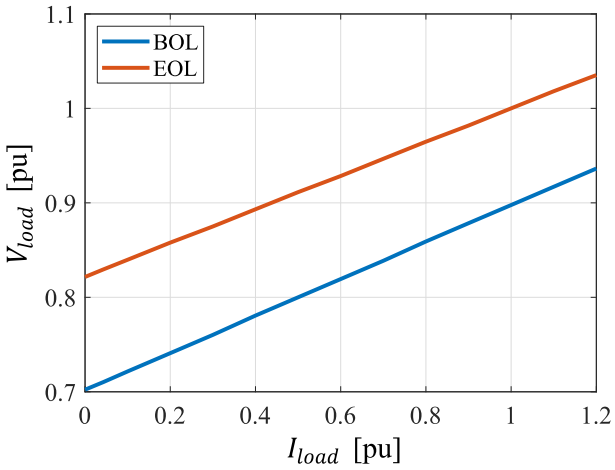


Fig. 5.7. BOL and EOL voltage and current curves of the electrolyzer.

Regarding the V_{source} 0.966 pu, it is a value closer to 1.035 pu than to 0.702 pu. This voltage level is obtained from an optimization process based on the maximum power to be processed by the converter ($|P_{conv_{max}}|$). Fig. 5.8 shows the results of the maximum power processed by the converter for different values of V_{source} between 0.702 pu and 1.035 pu. The blue lines correspond to the results obtained with the IPOS architecture, and the red lines to the ISOP architecture. The continuous lines are obtained from the BOL profile and the dashed lines from the EOL profile. It is concluded that V_{source}=0.966 pu with an ISOP architecture achieves the minimum $|P_{conv_{max}}|$, 0.089 pu. Any other value of V_{source} causes a higher power to be processed by the converter in BOL or EOL conditions.

Once the 3 V_{source} values have been defined, the next step is to compare the power to be processed by the converter (P_{conv}). Fig. 5.9a shows the results obtained with an IPOS architecture and Fig. 5.9b shows the results with an ISOP architecture. The results obtained with each V_{source} are represented by a color and 2 curves, a solid line (BOL) and a dashed line (EOL). The first conclusion is that working in boost mode (V_{source}=0.632 pu) is the solution that obtains the highest P_{conv} values, regardless of the architecture: $|P_{conv_{max}}|$=0.484 pu (IPOS case) and $|P_{conv_{max}}|$=0.792 pu (ISOP case). This occurs because the high power consumption points occur with high voltage. This provokes a higher K_{pr} at a high load power. Comparing the results of the architectures, the power to

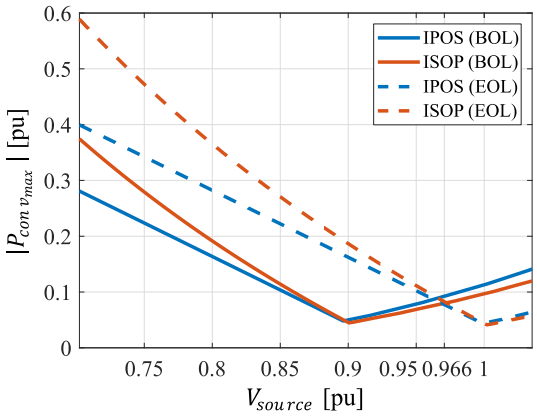


Fig. 5.8. Maximum power processed by the converter for different values of V_{source}.

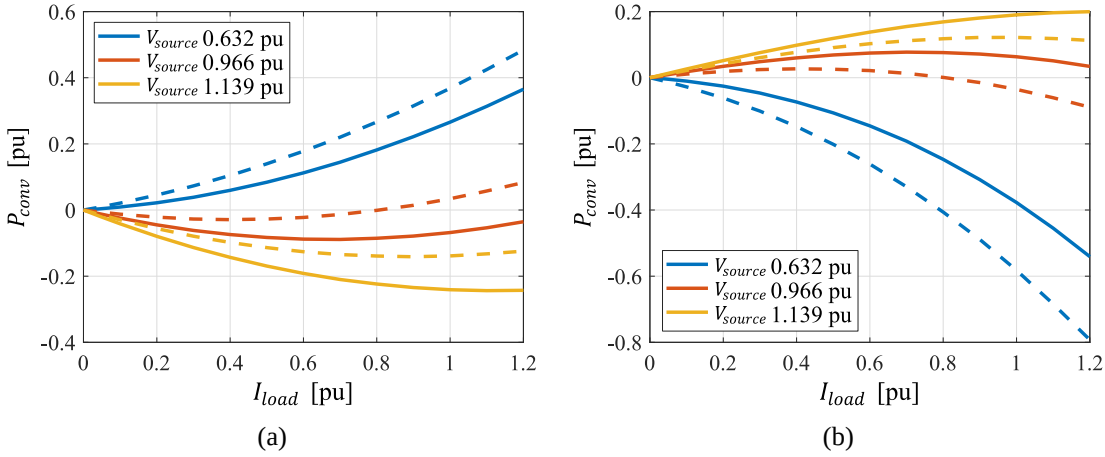


Fig. 5.9. Power curves processed by the converter for BOL (continuous line) and EOL (discontinuous line). (A) IPOS architecture. (B) ISOP architecture.

be processed by the converter is lower in an IPOS architecture. This is because its K_{pr} values in boost mode are always better than those of an ISOP architecture.

The second best solution in terms of reduced P_{conv} is to work in buck mode (V_{source}=1.39 pu). In this case, the fact that the high power consumption points occur with high voltage benefits the buck operation mode. At high power consumptions, the K_{pr} is minimized. This way, the maximum power processed by the converter is considerably decreased: $|P_{conv_{max}}|$=0.244 pu (IPOS case) and $|P_{conv_{max}}|$=0.199 pu (ISOP case). The power to be processed by the converter is lower with an ISOP architecture because it performs better than the IPOS in buck mode.

The solution that achieves the minimum $P_{conv_{max}}$ is the buck-boost mode (V_{source}=0.966 pu). This solution is the one that reduces G_V the most by locating V_{source}

Table 5.3. Maximum DC values for IPOS and ISOP architectures in boost mode, buck-boost mode and buck mode.

Parameter	Boost		Buck-boost		Buck	
	IPOS	ISOP	IPOS	ISOP	IPOS	ISOP
$\lvert P_{conv}\rvert$	0.484 pu	0.792 pu	0.089 pu	0.089 pu	0.244 pu	0.199 pu
V_{in}	0.632 pu	0.403 pu	0.966 pu	0.263 pu	1.389 pu	0.436 pu
V_{out}	0.403 pu	1.035 pu	0.263 pu	1.035 pu	0.436 pu	1.035 pu
I_{in}	0.765 pu	1.965 pu	0.092 pu	1.286 pu	0.214 pu	1.091 pu
I_{out}	1.200 pu	0.765 pu	1.200 pu	0.092 pu	1.200 pu	0.214 pu

between the minimum and maximum voltage values of the load. In this case, $\left|P_{conv_{max}}\right|$=0.089 pu. In order to carry out a fair comparison between the IPOS and ISOP architectures, it would be necessary to know the time elapsed by the application at each of the points in Fig. 5.7, and thus approach the analysis from an energy point of view rather than a power point of view.

Table 5.3 summarizes the maximum DC values of the power converter for each architecture in boost mode, buck-boost mode and buck mode. It is concluded that, in terms of power processed by the converter, working in boost mode is the least promising solution. On the other hand, working in buck-boost mode is the solution that minimizes the power processed by the converter, followed by buck mode.

Based on the semiconductor's 4 quadrant analysis from subchapter 2.1.2 (see Table 2.3 and Table 2.4), Table 5.4 specifies the required type of semiconductor at the primary side and at secondary side: (S) is for active switch, (D) is for diode and (B2B) is for back-to-back. These results are useful for the selection of the topology to implement. First, it is concluded that the Boost-IPOS solution is the one that requires the lowest DC current

Table 5.4. Maximum DC voltage and current parameters for the semiconductors inside the converter.

Parameter		Boost		Buck-boost		Buck	
		IPOS	ISOP	IPOS	ISOP	IPOS	ISOP
Primary	Switch tech.	(S)	(D)	(S)	(B2B)	(D)	(S)
	Voltage class	0.632 pu	0.403 pu	0.966 pu	0.263 pu	1.389 pu	0.436 pu
	Current class	0.765 pu	1.965 pu	0.092 pu	1.286 pu	0.214 pu	1.091 pu
Secondary	Switch tech.	(D)	(S)	(B2B)	(S)	(S)	(D)
	Voltage class	0.403 pu	1.035 pu	0.263 pu	1.035 pu	0.436 pu	1.035 pu
	Current class	1.200 pu	0.765 pu	1.200 pu	0.092 pu	1.200 pu	0.214 pu

for active switches (S or B2B). This is interesting from the company point of view, since the market of these type of devices is more limited than for diodes (D).

Second, it is concluded that in order to work in buck-boost mode, it is necessary to implement back-to-back active switches. Depending on whether it is an IPOS or ISOP architecture, this back-to-back solution is located in the primary or the secondary of the transformer. Although the buck-boost solution achieves the lowest P_{conv}, it is discarded for further analysis due to its circuit complexity and number of components.

Finally, the buck-ISOP solution is selected as the optimal solution. Compared to the buck-boost solution achieves a slightly higher P_{conv}, but it requires a less complex topology: actives switches (S) at the primary side and diodes (D) at the secondary side.

5.4 EV Fast Charging DC-DC

There is no doubt that the emergence of the EV is imminent [3] and in order to make it more attractive to consumer, it is essential to build an extensive and solid EV charging stations grid. Regarding extreme fast charging stations, Fig. 5.10 shows the different structure solutions that exist [6]. All of them are divided in two main stages (a rectification stage and a DC-DC charging unit). However, each solution stablishes the isolation border on a different point. For example, Fig. 5.10a proposes an isolated DC-DC charging unit,

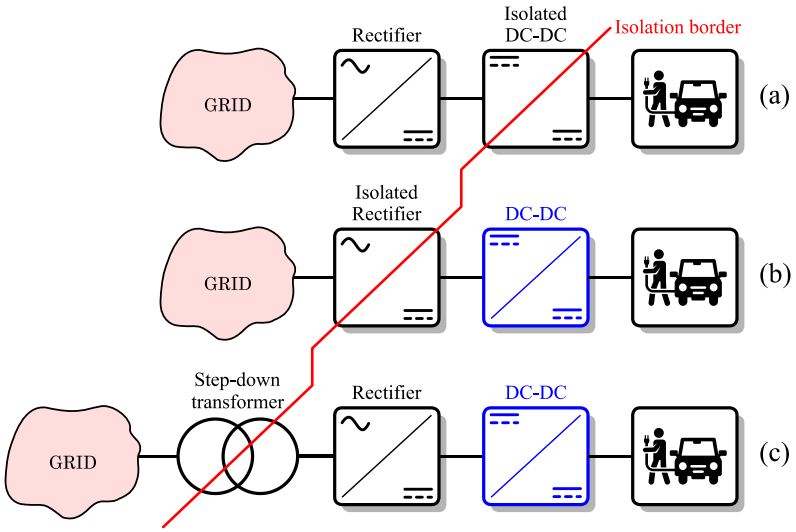


Fig. 5.10. Simplified single-wire diagram of different EV fast charging stations. In blue, the converters under analysis in this case study.

whereas, Fig. 5.10b establishes the isolation border at the power rectifier. Also, in some cases, a line frequency transformer is implemented before the rectification stage, see Fig. 5.10c. This case study is focused on the design of the DC-DC converter. To be more precise, this work contributes by describing a design methodology of a PPP based DC-DC charging unit. This design selects the appropriate transformer turn ratio in function of the converter's performance through the entire charging process of the EV. Since the DC-DC converter under analysis consists of a PPC, the final solution can be considered as the one shown in Fig. 5.10b or Fig. 5.10c.

5.4.1 System Description

The power converter under analysis is connected between a constant DC bus (after the rectifier) and a variable load (EV's ESS). Concerning the DC bus, according to the SAE J1772 standard, its voltage value can vary from 200 V to 600 V in applications with power levels higher than 90 kW [113]. For this case, the DC bus is stablished at 600 V. On the other hand, regarding the ESS of the EV, its voltage, power and SOC curves are presented in Fig. 5.11. The modelled curves represent a fast charging process of an EV (up to a SOC value of 80 %). Regarding the voltage curve, it varies from 350 V to 500 V, whereas the peak power value is defined around 150 kW.

Bearing in mind the application requires a buck operation, an ISOP architecture is selected. Regarding the topology, a DAB is implemented. Fig. 5.12 shows a simplified electric diagram of the final solution. When it comes to the design parameters of the DAB,

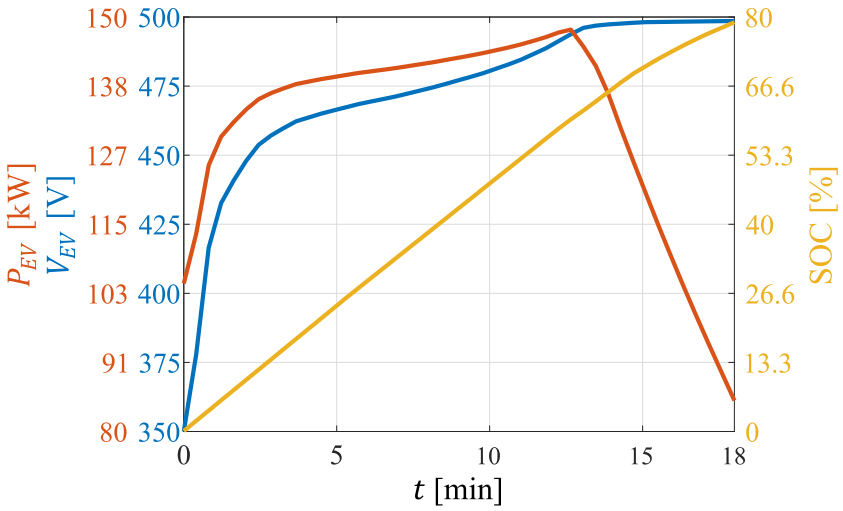


Fig. 5.11. Modelled voltage, power and SOC curves for a fast charging process of an EV.

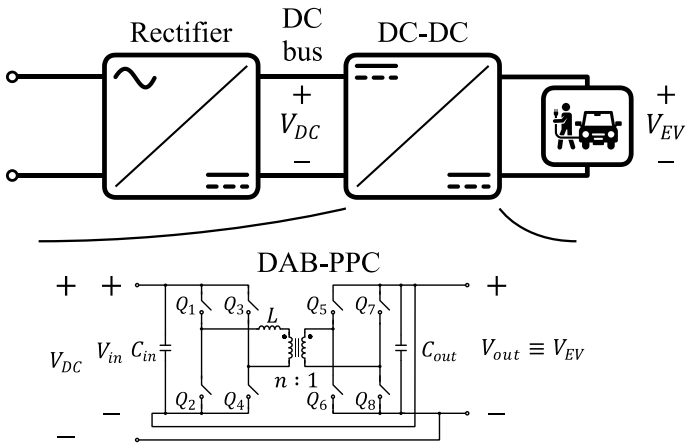


Fig. 5.12. Simplified electric diagram of the DC-DC converter under analysis.

Table 5.5. Design parameters of the DC-DC charging unit.

Parameter	Value		
V_{DC}	600 V		
V_{EV}	From 350 V to 500 V		
$\widehat{P_{EV}}$	150 kW		
V_{in}	From 250 V to 100 V		
V_{out}	From 350 V to 500 V		
P_{in}	44 kW		
f_{sw}	10 kHz		
n	0.7	0.33	0.2
L	17.5 µH	8.25 µH	5 µH

Table 5.5 defines the voltage, power and frequency levels of the system and the converter. As it can be observed, the input voltage consists of the difference between the DC bus and the ESS of the EV. This way, the maximum voltage that the primary side semiconductors will observe is reduced to 250 V. On the other hand, the output voltage contains the same values as V_{EV}, since it is connected in parallel. So, the secondary side semiconductors will be designed for a maximum voltage value of 500 V. The peak power to be processed by the converter is estimated around 44 kW. This occurs at the beginning of the charging process. Although P_{EV} increases as the ESS charges, the power processed by the converter decreases. This is due to the fact that V_{EV} gets closer to V_{DC} as the battery charges, reducing the K_{pr}.

The next step is to define the turn ratio for the transformer (n). This value is crucial when implementing a DAB topology, since it directly affects to the RMS value of the current through the inductor and the rest of the components. Furthermore, bearing in mind that the DAB is implemented on a PPC architecture, it is essential to analyze whether is more intelligent to optimize the value of n: for the beginning of the charge (higher power processed by the converter, but high voltage variability) or for the end of the charge (lower power processed by the converter, but low voltage variability). With this purpose, the present work proposes to carry out an extended comparison with 3 different n values. Each of these values is defined to achieve a maximum performance of the DAB at a specific working point through the charging process: start of charge (V_{EV}=350 V), intermediate point (V_{EV}=450 V) and end of charge (V_{EV}=500 V). Applying equation (4.1), Table 5.5 presents the obtained values for n.

5.4.2 Simulation Results

5.4.2.1 Processed Active and Non-Active Power by the Converter

In the first place, Fig. 5.13 shows the K_{pr} curve of the converter through the charging process for each n value. As it can be observed, all the curves obtain same results, which confirms the fact that the turn ratio of the transformer does not affect to the active power processed by the converter. It is observed that as the EV charges, the K_{pr} is reduced from 0.42 to 0.17.

In the second place, Fig. 5.14a and Fig. 5.14b present the non-active power processed by the inductor and the capacitors, respectively. Regarding the inductor, its critical point occurs at the beginning of the charging process with n=0.2. However, as the EV charges, the N_L curve of n=0.2 decreases, whereas the one of n=0.7 turns into the one with higher N_L. Nevertheless, the peak value achieved with n=0.7 is a 53 % of the one achieved with n=0.2. This is due to the reduction of the K_{pr} through the charging process. Even if n=0.7 is not optimized to work at the last working conditions, the reduction of the power to be processed by the converter cancels out its bad performance. Therefore, its N_L peak is much lower than the one with n=0.2 and similar to n=0.33. When it comes to the non-active power processed by the capacitors, very similar results are obtained. In fact, n=0.2 obtains the higher peak value of N_C and the higher results through a wider

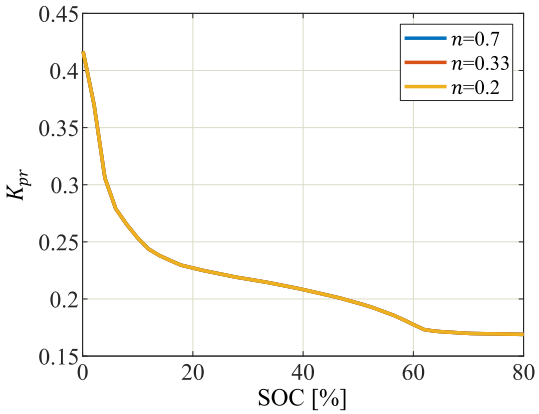


Fig. 5.13. K_{pr} through the battery charging process for each turn ratio.

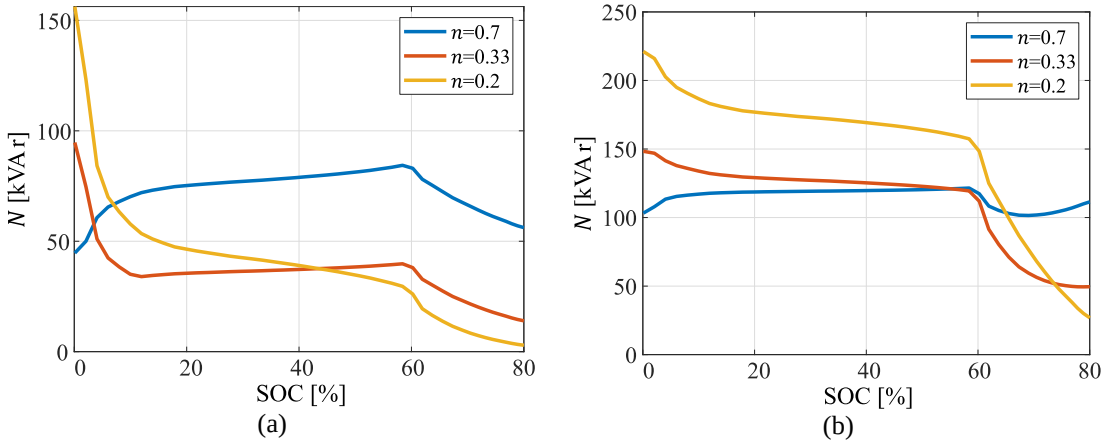


Fig. 5.14. Processed non-active power by the storage elements through the battery charging process for each turn ratio. (a) N_L. (b) N_C.

operation range (up to a SOC of 65 %). When it comes to n=0.7 and n=0.33, the first one presents lower results at the beginning of the charging process. Then, at the constant voltage region (60 % of SOC and above), n=0.33 achieves lower N_C values.

5.4.2.2 Energy Losses

This case study simplifies the calculation of the power losses by only considering the conduction losses of the passive and active devices. Fig. 5.15 shows the computed conduction losses with each value of n. As it can be observed, through great part of the charging process the most efficient results are achieved with n=0.7. On the other hand, n=0.2 is expected to achieve the worst results, since it obtains considerable power losses at the start of the charge. Once entering into the constant voltage region, n=0.33 and n=0.2 obtain the best results. However, at this operation point the power to be processed is very low, so the difference between each solution is relatively small. Then, the total

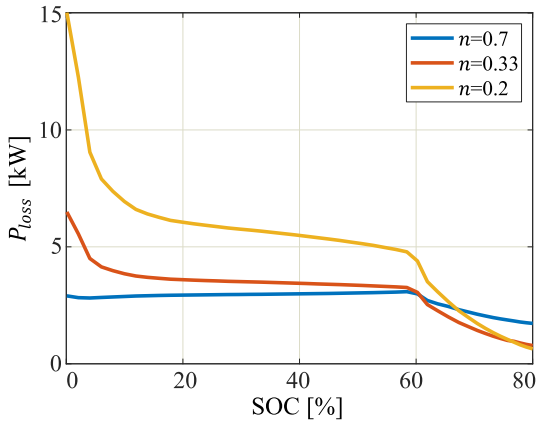


Fig. 5.15. Conduction power losses of the semiconductors and inductor through the battery charging process for each turn ratio.

Table 5.6. Total energy losses through the battery charging process for each turn ratio.

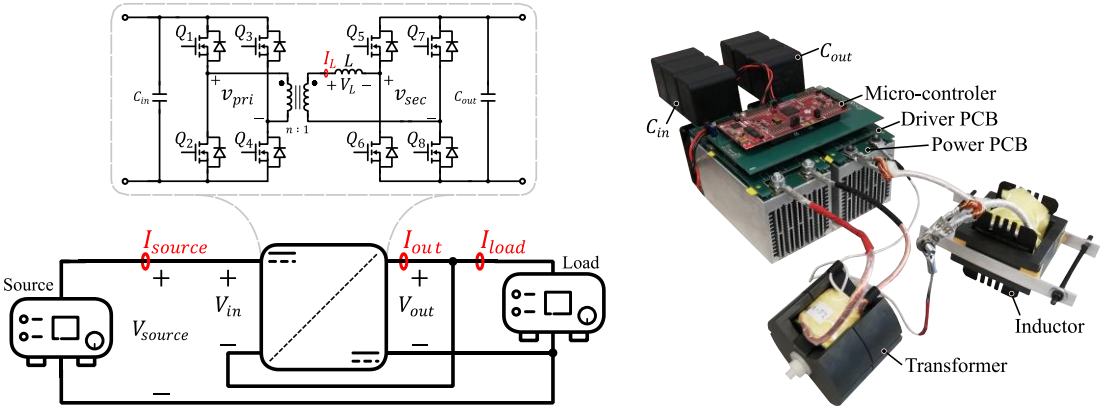
Turn ratio	E_{loss}	$\frac{E_{loss}}{E_{charged}} \cdot 100$	Relative difference
n=0.7	0.81 kWh	2.03 %	54.7 %
n=0.33	0.9 kWh	2.25 %	60.8 %
n=0.2	1.48 kWh	3.7 %	Reference

energy losses are calculated, see Table 5.6. There, it is shown that the most efficient design is with n=0.7, which in comparison to n=0.2, achieves to reduce the energy losses to a 54.7 %. This result concludes that, for the concerned case study, optimizing the design of the DAB for initial working conditions is the most efficient solution.

5.4.3 Experimental Results

5.4.3.1 Test Bench Description

In order to validate the comparison carried out through the simulations, a downscaled test bench as the one presented in Fig. 5.16 is mounted. Fig. 5.16a shows a simplified electric diagram of the implemented DAB-ISOP step-down architecture. Also, the main current and voltage measurements that will be used for the calculation of the comparison parameters are presented. Fig. 5.16b shows the mounted DAB prototype. This prototype reuses the power and driver PCBs presented in Chapter 3.



(a) (b)

Fig. 5.16. Assembled test bench for the analysis of the downscaled EV fast charging unit. (a) Simplified electric diagram of the DAB ISOP step-down with the main current and voltage measures. (b) DAB prototype.

Fig. 5.17 presents the modelled voltage and power curves for the experimental prototype. Compared to the simulation curves from Fig. 5.11, the voltage of the EV (represented as V_{load}) is halved and the peak power value is stablished at 4 kW. Table 5.7 lists the main electrical parameters and components of the experimental test bench. As it can be observed, the turn ratio values remain the same as in the simulations. The inductors are designed to be implemented on the secondary side (less current).

5.4.3.2 Results

In the first place, Fig. 5.18 presents the K_{pr} curve achieved by each solution. Similarly to the simulations, it is observed that the selection of n does not affect to the processed active power ratio of the converter. Apart from that, the three K_{pr} curves present their higher values at the start of the charging process, when V_{load} is in its lowest value. As this value increases and gets closer to V_{source}, the K_{pr} decreases.

In the second place, Fig. 5.19 presents the non-active power processed by the storage elements. Fig. 5.19a shows the processed non-active power by the inductor. As it can be observed, the peak value is obtained at initial charging conditions with n=0.2. Then, as the modelled ESS charges, the curve of n=0.7 obtains the highest values. However, similarly to the simulations, its peak value is still lower than the one with n=0.2 and very similar to n=0.33. On the other hand, there is the non-active power processed by the capacitors, see Fig. 5.19b. In this case, n=0.7 is the design that forces the capacitors

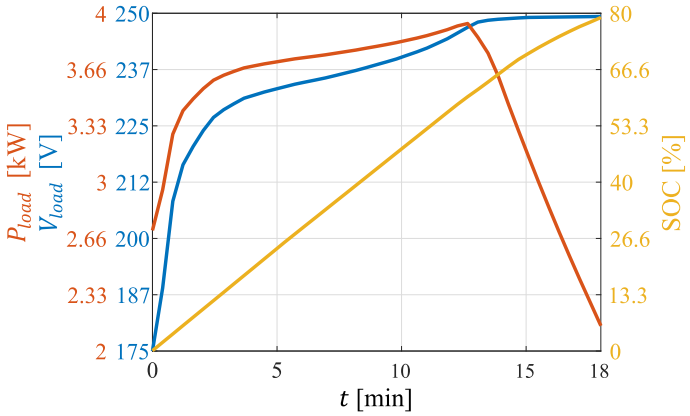


Fig. 5.17. Modelled voltage, power and SOC curves for the experimental prototype.

Table 5.7. Main electrical parameters and components of the experimental test bench.

Parameter	DAB-PPC		
V_{source}	300 V		
V_{load}	From 175 V to 250 V		
$\widehat{P_{load}}$	4 kW		
V_{in}	From 125 V to 50 V		
V_{out}	From 175 V to 250 V		
$\widehat{P_{in}}$	1.2 kW		
f_{sw}	50 kHz		
C_{in}	200 µF		
C_{out}	300 µF		
n	0.7	0.33	0.2
L	62 µH	133 µH	215 µH
Q_{1-4}	IPT111N20NFD[18]		
Q_{5-8}	IPT65R033G7[19]		

to process less power through a wider operation range. In consequence, the capacitor modules implemented at the prototype can be reduced in a future redesign.

[18] V_{DS}=200 V , R_{DS}=30 mΩ @T_j=150 ºC
[19] V_{DS}=650 V, R_{DS}=72 mΩ @T_j=150 ºC

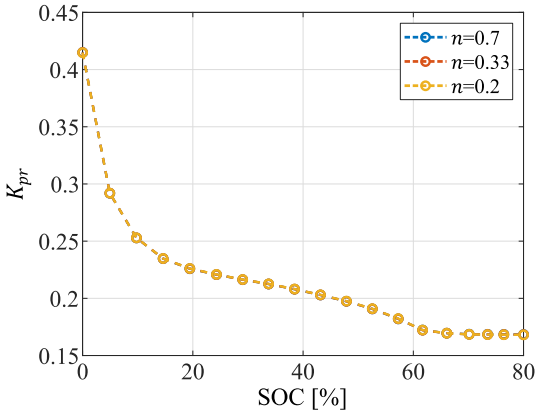


Fig. 5.18. Experimentally obtained K_{pr} through the battery charging process for each turn ratio. The results for n=0.7, n=0.33 and n=0.2 overlap.

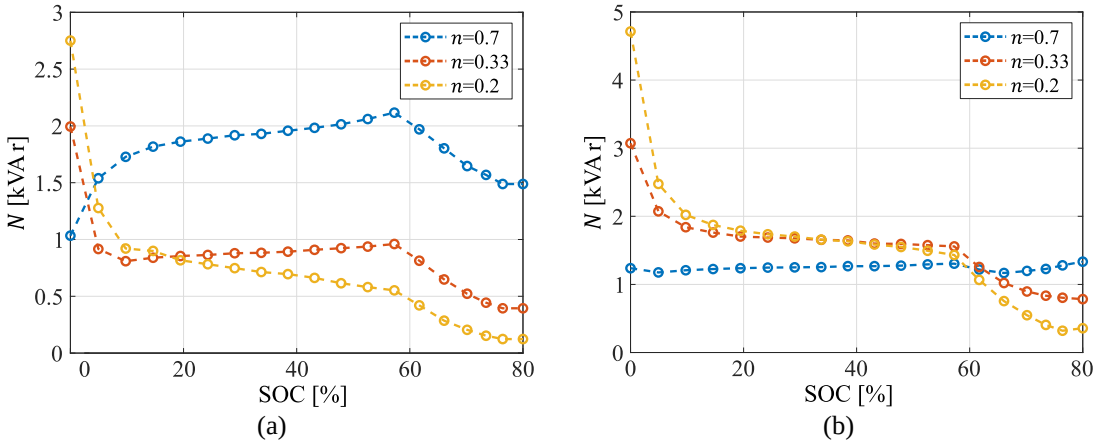


Fig. 5.19. Experimentally obtained processed non-active power by the storage elements through the battery charging process for each turn ratio. (a) N_L. (b) N_C.

In the third place, Fig. 5.20 presents the experimental power losses with each turn ratio. As it can be observed, the DAB design with n=0.7 is the most efficient solution through great part of the charging process, especially at the beginning (when more power is processed by the converter). At the last working conditions, the losses obtained with n=0.7 are higher than with n=0.2 and n=0.33. Nevertheless, due to the low K_{pr}, the P_{loss} difference is negligible. Table 5.8 shows the total energy losses obtained with each turn ratio. It is observed that the most efficient design is with n=0.7, which compared to n=0.2, reduces the energy losses to a 54.35 %. Therefore, it is experimentally concluded that, for the concerned case study, optimizing the design of the DAB for initial working conditions is the most efficient solution. This is because the period in which the converter processes more power is at the start of the charging process. So, optimizing the design for initial working conditions will make up for the bad performance at the last charging period.

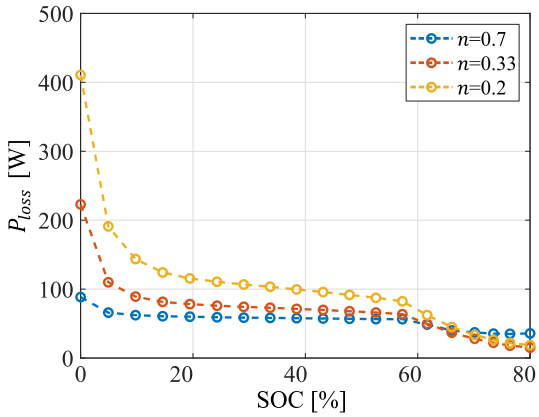


Fig. 5.20. Experimentally obtained power losses through the battery charging process for each turn ratio.

Table 5.8. Experimentally obtained total energy losses through the battery charging process for each turn ratio.

Turn ratio	E_{loss}	$\frac{E_{loss}}{E_{charged}} \cdot 100$	Relative difference
n=0.7	16.11 Wh	1.5 %	54.35
n=0.33	19.77 Wh	1.88 %	68.12
n=0.2	28.99 Wh	2.76 %	Reference

5.4.4 Conclusion

The present work describes a design methodology of a PPC EV fast charging unit. The topology implemented on the PPC architecture consists of a DAB and, with the aim of achieving the most optimal solution, three different transformer turn ratios are compared in terms of processed active and non-active power, and energy losses through the charging process.

The simulations conclude that the turn ratio affects to the non-active power processed by the storage elements and to the power losses of the converter. It is observed that optimizing the design of the converter for working conditions where K_{pr} is higher achieves a more favorable performance. This is experimentally validated with a downscaled 4 kW prototype. The experimental results confirm that an adequate design of the turn ratio can reduce the energy losses to a 54.3 %.

Chapter 6

DESIGN AND ASSEMBLY OF A HIGH-POWER PPC

This Chapter presents the design and assembly of a 50 kW PPC for EV fast charging. First, the main electrical parameters of the application are defined. Then, the size and selection of the active and passive elements are described. Due to the high power level of the application, a test procedure is proposed to validate the converter. Finally, the experimental results are presented for different test conditions.

6.1 Application Selection and Description

The main benefits of IPOS-ISOP type PPC architectures are obtained at low K_{pr} conditions. For example, in Chapter 4, the peak performance is observed at K_{pr}<0.2. However, a great voltage variability of V_{source} and V_{load} affects negatively to their efficiency and thermal stress. Indeed, compared to FPC solutions, one of the main disadvantages of IPOS-ISOP type architectures is the extended operation range of the converter. Concerning this, an ideal application for the high-power PPC must ensure a low K_{pr} and a low voltage variability of the source and the load. In this case, the selected application consists of an EV fast charging DC-DC unit.

Depending on the location of the application, the type of charger (DC or AC, on-board or off-board), and the power level a different standard must be considered [7]. Fig. 6.1 summarizes the main EV charging infrastructures and their corresponding standards. Regarding Europe, IEC 61851 is the one to take into account. Since the converter under analysis consists of a DC-DC unit, it falls into the category Mode 4. Table 6.1 lists the maximum voltage-current-power values defined in this standard. Also, the operation range of the converter is defined. In this case, the high power converter must only operate

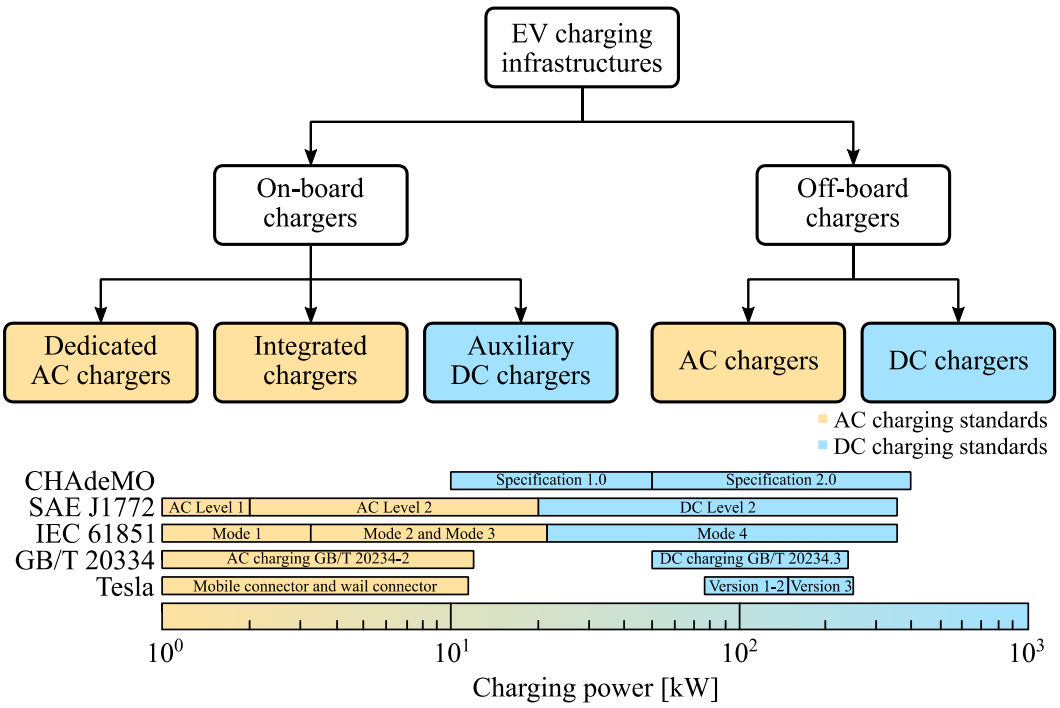


Fig. 6.1. EV charging infrastructures and standards [7].

Table 6.1. Mode 4 (IEC 61851) standard's main points [113].

Parameter	Value
V_{DC}	<1000 V
I_{load}	<400 A
P_{load}	<240 kW
Operation range	Operate only in the CC mode (up to a SOC of 80 % or 90 %)

through the CC region of the battery. Charging the battery in the CC region typically limits the SOC range up to 80 %.

The next step is to define the electrical parameters of the application and select the IPOS-ISOP type architecture. Fig. 6.2 presents the typical configuration of an EV fast charging station. The AC-DC stage is out of scope of this Chapter. Concerning the DC-DC stage, there are two main voltages to be defined: V_{DC} and V_{EV}. The voltage V_{DC} corresponds to the DC link and it is considered as constant. The voltage V_{EV} corresponds to the battery of the EV and, depending on the model of the vehicle, it can vary from 400 V to 800 V, see Table 6.2. At present, 400 V nominal battery EVs are predominant, but there is a trend of elevating this voltage up to 800 V [7], [113]. In order to supply such a wide variety of load voltages, recent fast chargers offer a wide output voltage, see Table 6.3. As it can be observed, most of the chargers in the market are able to achieve an output voltage that goes from 100 V to 1000 V. This is a great advantage compared to PPCs, which present a bad performance with a high G_V. However, there is the case of the V3 Supercharger from Tesla. This charger is designed to charge only Tesla vehicles, which

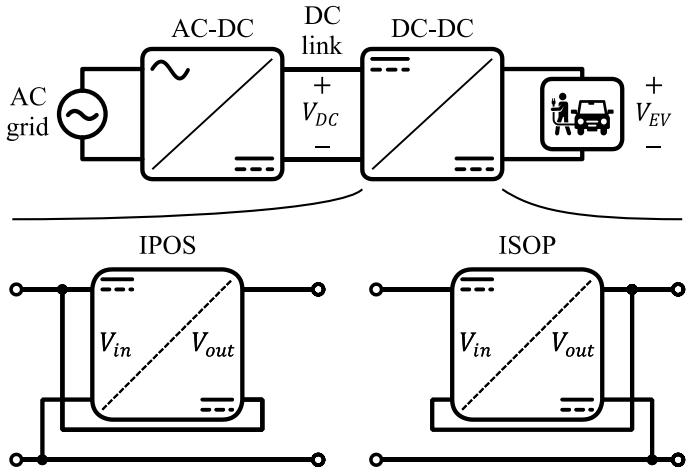


Fig. 6.2. Simplified electric diagram of the high-power DC-DC charging unit under analysis.

Table 6.2. EV models and corresponding battery voltage [7].

Model	Manufacturer	Battery voltage
eCitaro (bus)	Mercedes-Benz	400 V
7900 Electric (bus)	Volvo	600 V
Model S, long range	Tesla	400 V
E-tron 55 Quatro	Audi	396 V
Taycan 4S	Porsche	800 V
Bolt	Chevrolet	350 V
Zoe ZE50	Renault	400 V
Leaf	Nissan	360 V

Table 6.3. EV chargers in the market [7].

Charger	Manufacturer	Output voltage	Output current	Power
Delta Ultra Fast Charger	Delta Electronics	From 50 V to 550 V	125 A	-
Charge Point Express Plus	ChargePoint	From 200 V to 1000 V	390 A	156 kW
ABB Terra HP	ABB	From 150 V to 920 V	500 A	350 kW
ABB Terra GB 184MVZ	ABB	From 200 V to 750 V	300 A	3x60 kW
V3 Supercharger	Tesla	450 V	-	250 kW

simplifies the design of the conversion stage. Since Tesla knows the voltage level of the vehicle to be charged, the output voltage is fixed. This type of applications where the manufacturer must design the conversion circuit for a specific EV are ideal for PPC architectures, for example: a charging station of a fleet of EVs. Turning to the value of V_{EV}, given the trends that are observed on the voltage increment, V_{EV} is defined at 800 V. Therefore, the output voltage that is required for the PPC under analysis is 800 V plus the inherent variability of the battery. Fig. 6.3a shows the modelled voltage curve of V_{EV}, which has a nominal value of 720 V.

Then, the IPOS or ISOP architecture must be selected. As it is shown in Fig. 6.3a, the voltage of a battery varies in function of the energy stored. The higher the SOC, the higher OCV. Bearing in mind that the operation range under analysis just considers a CC charging mode, the power consumed by the EV (P_{EV}) also increases together with the SOC and the V_{EV}. Based on the conclusions from subchapter 5.3, if an IPOS architecture is selected, V_{DC} must be defined below the minimum value of V_{EV} to ensure a boost

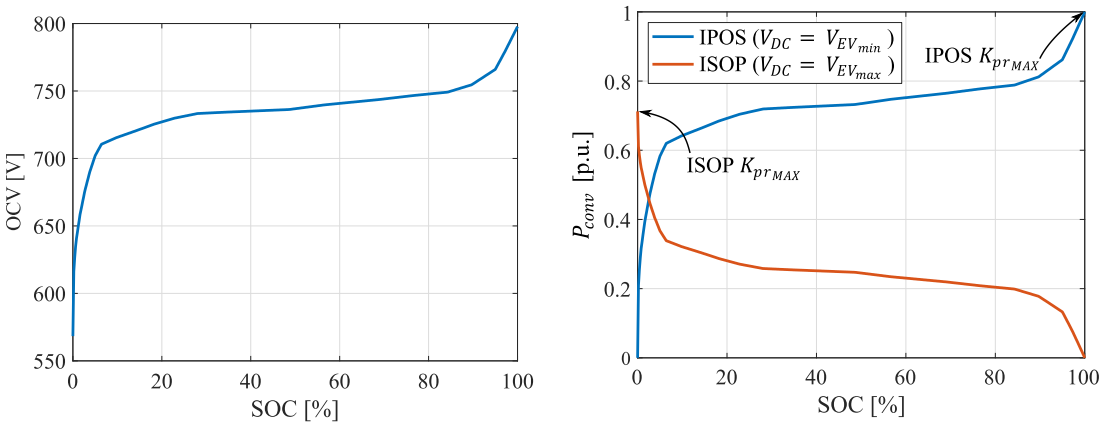


Fig. 6.3. (a) Modelled V_{EV}. Based on the OCV curve of a LiFePo cell [113]. (b) K_{pr} comparison between IPOS and ISOP architectures in function of the V_{cell} from Fig. 6.3a.

operation. If an ISOP architecture is selected, V_{DC} must be defined above the maximum value of V_{EV} to ensure a buck operation. Fig. 6.3b compares the power processed by the converter with these two solutions in per unit. As it can be observed, the maximum K_{pr} obtained with the ISOP occurs at the beginning of the charging process. However, the maximum K_{pr} obtained with the IPOS occurs at the end of the charging process. Since P_{EV} increases through the charging process, the maximum power processed by the converter is higher in the IPOS case. Therefore, the ISOP architecture is selected.

Finally, Table 6.4 and Fig. 6.4 define the main electrical parameters of the system and the modelled EV voltage profile. As it can be observed, the operation range is limited from 10 % SOC to 90 % SOC. The 90 % SOC is defined by the Mode 4 standard, whereas the 10 % SOC is recommended by the battery manufacturers [7]. On the other hand, the peak power value of the application is set to 50 kW.

Table 6.4. Main system electrical parameters.

Parameter	Value
V_{DC}	800 V
V_{EV}	From 715 V to 755 V @ From 10 % to 90 % SOC
$\widehat{P_{EV}}$	50 kW

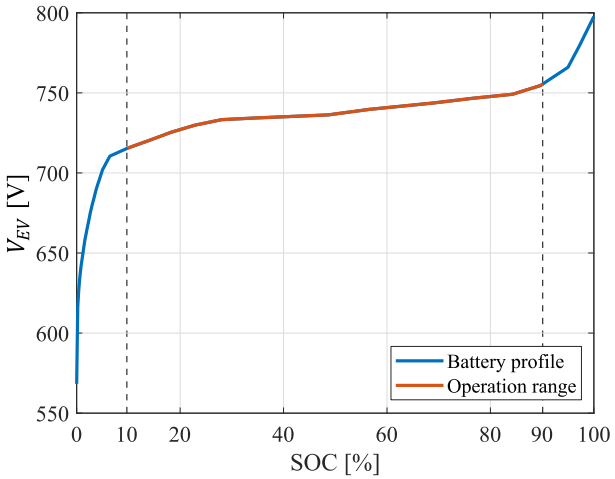


Fig. 6.4. Operation range of the EV fast charging DC-DC under analysis.

6.2 Prototype Design

This subchapter describes the design of the high power PPC and its main purpose is to demonstrate that the benefits observed at low power conditions are also scalable to high power applications: lower current/voltage class devices, reduced cost… It is important to mention that the optimization of the topology and each of its components is out of scope of this Chapter. The selected topology for this analysis is the DAB-PPC. The reason for this is to provide continuity to the designs presented in Chapter 4. Apart from that, the switching frequency is stablished at 20 kHz. This switching frequency is adequate for MOSFET and IGBT devices, which enables the analysis of both technologies.

Fig. 6.5 shows a simplified diagram of the DAB-PPC. As it can be observed, the number of semiconductors is doubled to decrease their thermal stress. This subchapter defines the steps followed for the selection of each component: inductance value, transformation ratio, input-output capacitance, MOSFET or IGBT…

Based on Table 6.4, Table 6.5 shows the main electrical parameters of the converter. The primary side consists of a low-voltage high-current, whereas the secondary side consists of a high-voltage and low-current.

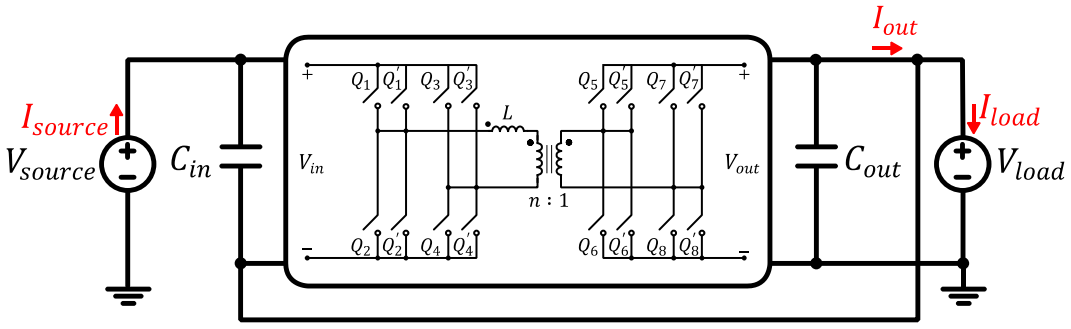


Fig. 6.5. DAB-PPC under analysis.

Table 6.5. Main electrical parameters of the converter, peak values.

Parameter	Value
$\widehat{V_{in}}$	85 V
$\widehat{V_{out}}$	755 V
$\widehat{I_{in}}$	59 A
$\widehat{I_{out}}$	6.62 A
$\widehat{K_{pr}}$	0.105
$\widehat{P_{conv}}$	4.7 kW
f_{sw}	20 kHz

6.2.1 Inductance

The inductance value of the DAB-PPC is a key parameter that directly affects to the performance of the rest of the devices. Its value defines the RMS currents inside the converter and it also decides whether the semiconductors work under ZVS or hard switching conditions.

The first step is to define the transformation ratio (n). The voltage and current values from Table 6.5 show that it exists a 10 times ratio between the primary side and the secondary side. Therefore, n is defined at 0.1, which consists of a round value that simplifies the assembly.

The second step is to calculate an inductance value that ensures ZVS operation through all the CC charging process. Due to the high power level of the application, high voltage and current values are expected, even in low K_{pr} conditions. Therefore, as first step, the boundaries of the ZVS regions are calculated following the steps described in

[109]. Fig. 6.6 shows the ZVS regions for the concerned application. The dashed lines represent the trajectory of the operating points of the converter through a CC charging process. Each dashed line corresponds to an inductor value, which is given by (6.1).

$$L = \frac{n \cdot V_{in} \cdot V_{out} \cdot \phi_{rad} \cdot (\pi - |\phi_{rad}|)}{2 \cdot \pi^2 \cdot f_{sw} \cdot P_{conv}} \quad \textbf{(6.1)}$$

Where, ϕ_{rad} is the phase-shift in radians.

In (6.1), two different values are given to ϕ_{rad}: π/6 (37º), which is the minimum value that ensures ZVS for all the devices, and π/3 (60º) the maximum value that keeps a safe margin to compensate the power losses. ϕ_{rad}= π/6 requires an inductance of 5.2 µH, and ϕ_{rad}=π/3 requires and inductance of 7.1 µH.

Based on the DAB model from subchapter 4.2.2.2, Fig. 6.7 compares the inductor RMS current achieved with each solution. As it can be observed, both solutions present their peak values at initial charging conditions. However, their curves behave differently as the battery charges. The *L*=5.2 µH design shows a convex curve, whereas the *L*=7.1 µH shows a decreasing slope. In overall, it is clear that *L*=5.2 µH presents lower RMS values through all the CC charging process. Therefore, it is concluded that the selection of the inductance value entails a trade-off between low inductor RMS current and ZVS operation. In this case, an intermediate value is selected for the design: *L*=6.3 µH. The required phase-shift for this design is 49º.

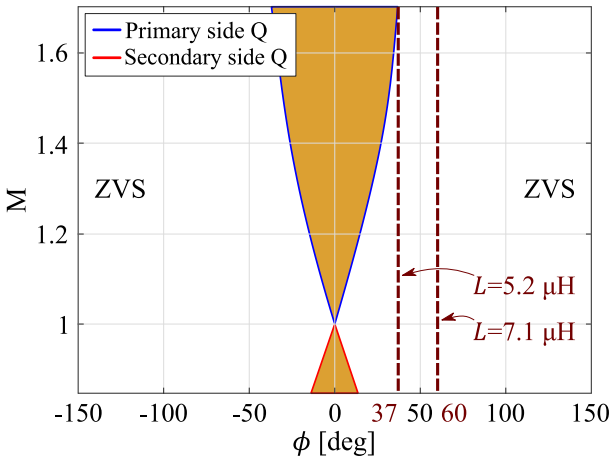


Fig. 6.6. ZVS regions and boundaries for primary and secondary side semiconductors using PSM.

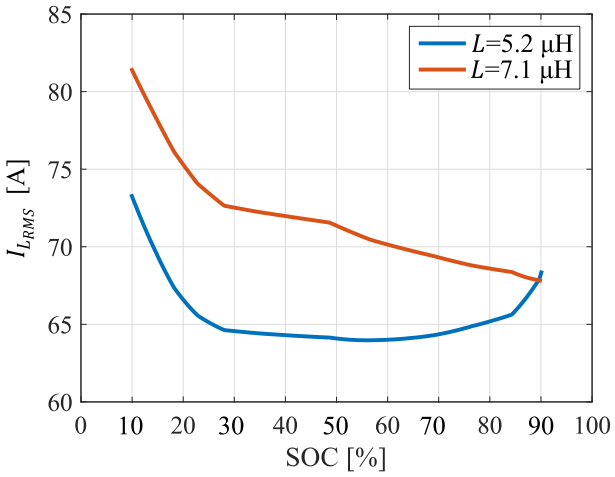


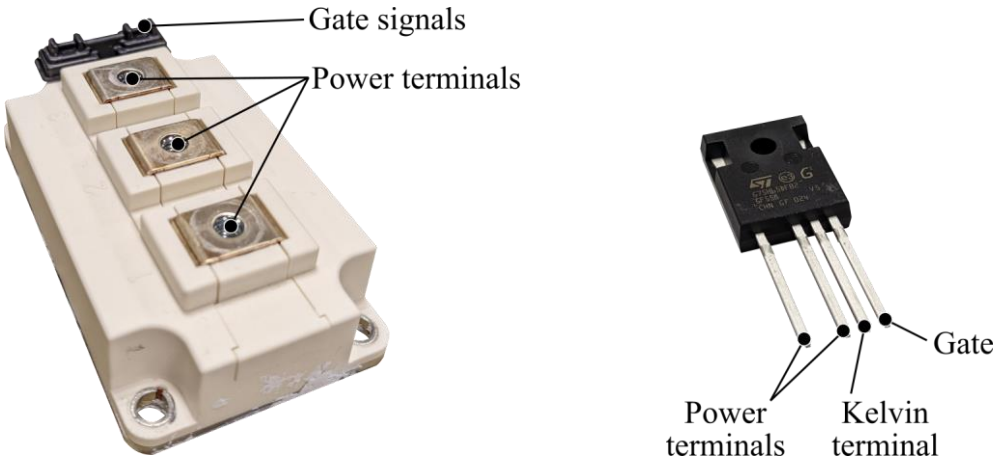
Fig. 6.7. Inductor RMS current for *L*=5.2 µH and *L*=7.1 µH.

6.2.2 Switching Devices

As it can be observed in Table 6.5, the current/voltage requirements from the primary and secondary side are very different: low voltage (80 V) and high current (60 A) at the primary side, and high voltage (800 V) and low current (6 A) at the secondary side. This subchapter selects the appropriate transistor technology for each side. In order to emphasize the benefits of PPC architectures, the search is limited to:

- **TO-247-4 package.** High power converters usually implement module type package for the switching devices, see Fig. 6.8a. This work aims to show that PPC solutions enable the implementation of discrete devices, see Fig. 6.8b. In this case, the TO-247-4 package is selected due to its extra Kelvin emitter connection, which improves the switching characteristics.
- **Silicon technology.** As concluded in subchapter 4.3, Si-based devices and PPC architectures complement each other. The wide and large variety of Si devices is an important advantage against SiC-based devices. The low current/voltage class Si devices in the market boost their implementation in PPC architectures. Furthermore, their reduced cost and maturity turns these devices into ideal solutions for PPC architectures.

Table 6.6 shows the selected devices under analysis. Regarding the primary side, two transistor technologies are compared: IGBT and MOSFET. Although the maximum voltage expected in the primary side is around 80 V, 600 V devices are selected. This is



(a) (b)

Fig. 6.8. (a) Module package. (b) Discrete TO-247-4 package.

Table 6.6. Switching devices under analysis.

Device	Manufacturer ID	Transistor type	Voltage class	Conduction characteristics
Primary side Q_{1-4}	STGW75H65DFB2-4	IGBT	650 V	$V_{CE_{sat}}$=1.9 V @ T_j= 175ºC
	IPZ60R017C7	MOSFET	650 V	R_{DS}=33 mΩ @ T_j= 150ºC
Secondary side Q_{1-4}	IKY40N120CS6	IGBT	1200 V	$V_{CE_{sat}}$=2.25 V @ T_j= 175ºC
	-	MOSFET	-	-

because there is no IGBT for a voltage class lower than 600 V. So, in order to make a fair comparison a 600 V MOSFET is also selected. Regarding the secondary side, a voltage class of 1200 V is defined. No MOSFET is considered for the secondary side bridge. At this voltage level, the on-state resistance of Si-based MOSFETs can reach up to units or tens of ohms.

6.2.2.1 IGBT power losses

The power converter model presented in subchapter 4.2.3 is used to compute the power losses obtained with the MOSFETs. However, in the case of the IGBT, a different procedure is followed. The conduction channel of an IGBT cannot conduct bidirectional current. Therefore, the conduction losses are divided into two: the losses produced by the conduction channel (6.2) and the losses produced by the diode (6.3).

$$P_{cond_{IGBT_{CH}}} = I_{CH} \cdot V_{CE_{sat}} + I_{CH_{RMS}} \cdot R_{CE} \quad \textbf{(6.2)}$$

$$P_{cond_{IGBT_D}} = I_D \cdot V_F + I_{D_{RMS}} \cdot R_D \quad \textbf{(6.3)}$$

Where, I_{CH} and $I_{CH_{RMS}}$ are the average and RMS currents flowing through the transistor channel, I_D and $I_{D_{RMS}}$ are the average and RMS currents flowing through the diode, $V_{CE_{sat}}$ is the collector-emitter saturation voltage, R_{CE} is the collector-emitter resistance, V_F is the forward voltage of the diode, and R_D is the resistance of the diode.

Regarding the switching losses of the IGBT, Fig. 6.9 specifies the switching transients at the primary side. Since the defined inductor ensures ZVS operation through all the CC charging, the switching transients defined in Fig. 6.9 are true through all the operation range. At the beginning of the period, the diodes from $Q_{1,4}$ start conducting until the inductor current (i_L) turns positive. At this moment, the diodes turn-off and the transistors turn-on with zero current and voltage. At T_s/2, the transistors from $Q_{1,4}$ turn-off and the diodes from $Q_{2,3}$ start conducting. When the inductor current turns negative, the diodes turn-off and the transistors turn-on with zero current and voltage. At the end of the period, the transistors from $Q_{2,3}$ turn-off and the diodes from $Q_{1,4}$ start conducting.

The switching losses that occur when the current turns from positive to negative, and vice versa, are neglected. The switching losses due to the turn-on of the diode are also neglected. Therefore, the only switching losses that are considered are the turn-off

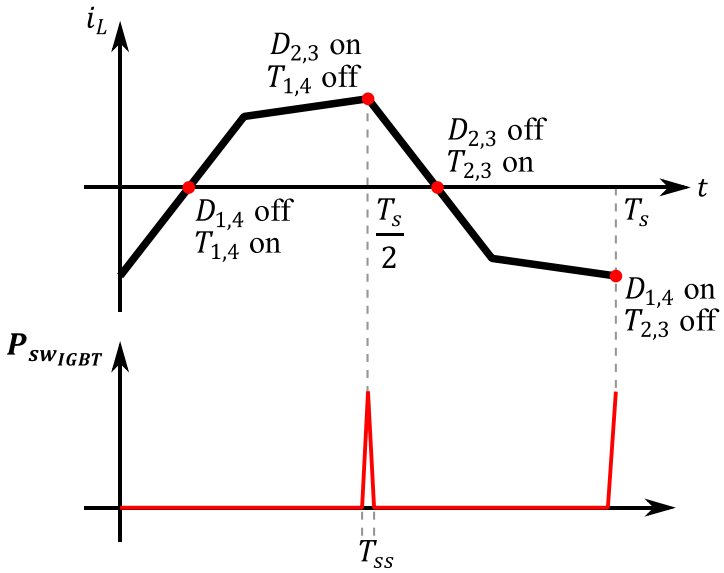


Fig. 6.9. Switching losses of IGBTs at the primary side of the DAB assuming ZVS operation.

of T_{1-4}. These are shown in Fig. 6.9 at $T_s/2$ and T_s. $\boldsymbol{P_{sw_{IGBT}}}$ is a vector that contains the switching losses produced by a single device at each time step (T_{ss}). As it can be observed in Fig. 6.9, $\boldsymbol{P_{sw_{IGBT}}}$ only contains the switching losses that occur at $T_s/2$ and at T_s, which are given by (6.4). Then, the average value of $\boldsymbol{P_{sw_{IGBT}}}$ is computed and multiplied by the number of semiconductors at the primary side (6.5). This is the resulting value for the switching losses of the IGBT devices. Same procedure is followed with the rest of the semiconductors at the secondary side.

$$\boldsymbol{P_{sw_{IGBT}}} = \frac{E_{off}(I_0)}{T_{ss}} \cdot \frac{V_0}{V_{CE_{test}}} \tag{6.4}$$

$$P_{sw} = \overline{\boldsymbol{P_{sw_{IGBT}}}} \cdot 8 \tag{6.5}$$

Where, E_{off} is the turn-off energy losses curve given as a function of collector current. This curve is given by the manufacturer for a specific test voltage ($V_{CE_{test}}$). I_0 and V_0 are the switching current and voltage.

Fig. 6.10 compares obtained results for a single device at the primary side. The solid lines represent the total power losses of each solution and the dashed lines represent the conduction and switching losses. As it can be observed, in both cases the predominant losses are due to the conduction. This is because of the high current at the primary side. The switching losses are minimum due to the ZVS operation and the low blocking voltage. The results demonstrate that the MOSFET devices present a more efficient

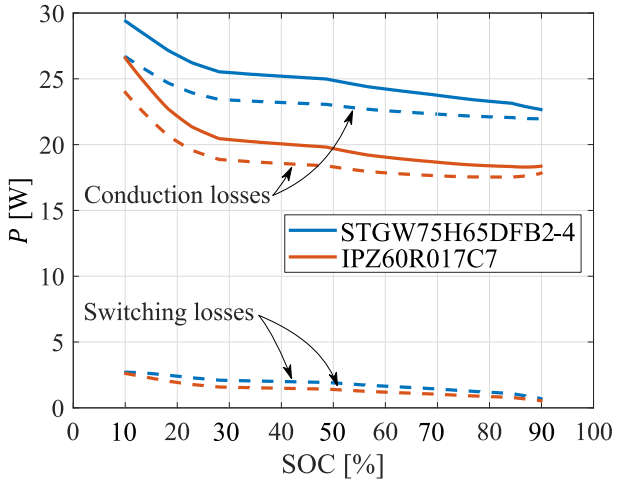


Fig. 6.10. Power losses of a single device at the primary side.

performance. So, they are selected for implementation at the primary side of the prototype. Furthermore, it must be mentioned that the MOSFETs under analysis are designed for a voltage class of 600 V. Selecting lower voltage class devices would decrease the R_{DS} value and improve the efficiency. However, in order to achieve a robust prototype, the IPZ60R017C7 device is kept. At the secondary side, the IKY40N120CS6 device is implemented.

6.2.3 Input-Output Capacitor

In the first place, the output capacitance (C_{out}) is defined to achieve a maximum ripple voltage of 1 %. Based on the power converter model from subchapter 4.2.2.2, an output capacitance of 70 µF ensures a maximum peak-to-peak voltage (V_{pk-pk}) of 8 V through all the operation range. Fig. 6.11a and Fig. 6.11b show the V_{pk-pk} and RMS current of the output capacitor with C_{out}=70 µF.

Regarding the input capacitance (C_{in}), its value is defined to protect the primary side semiconductors. To explain this, Fig. 6.12 presents the overvoltage issue that exists

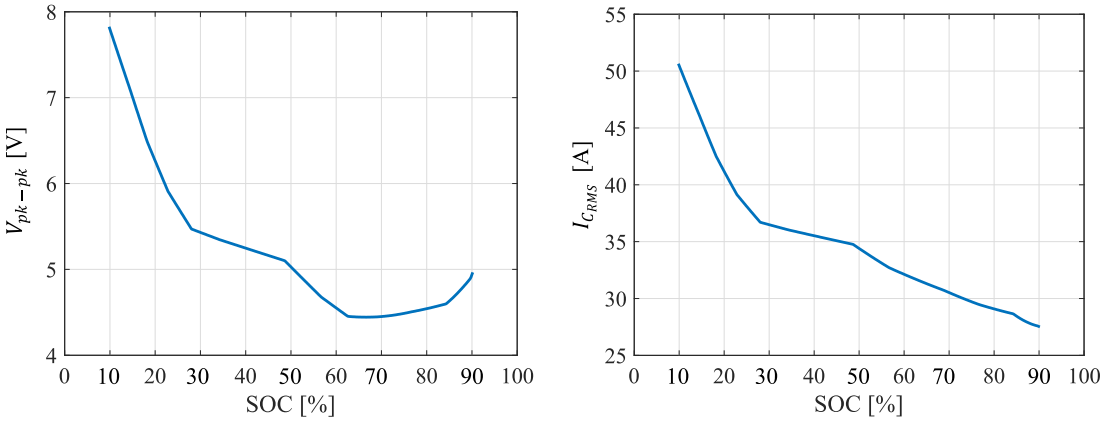


Fig. 6.11. (a) Peak to peak output voltage. (b) Output capacitor RMS current.

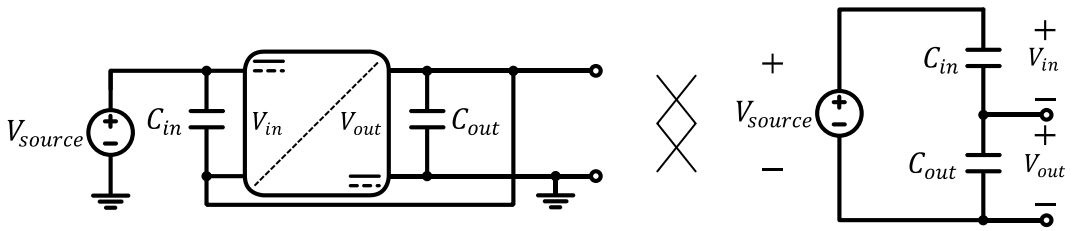


Fig. 6.12. Overvoltage issue with ISOP architectures at no load conditions.

with ISOP architectures at no load conditions. Assuming the case in which the source is connected to the converter, but no load is connected yet, the resulting circuit is simplified to a voltage divisor defined by C_{in} and C_{out}. Thus, the voltages V_{in} and V_{out} are defined by (6.6),(6.7).

$$V_{in} = V_{source} \cdot \frac{C_{out}}{C_{in}} \tag{6.6}$$

$$V_{out} = V_{source} \cdot \frac{C_{in}}{C_{out}} \tag{6.7}$$

Since the primary side semiconductors are designed for a reduced voltage, C_{in} is defined to keep a maximum voltage of 170 V (double of $\widehat{V_{in}}$ from Table 6.5). The result is given by (6.8).

$$C_{in} = V_{source} \cdot \frac{C_{out}}{V_{in}} = 800 \cdot \frac{70\mu}{170} = 330\ \mu\text{F} \tag{6.8}$$

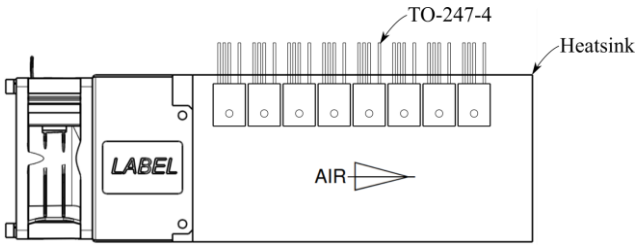
Table 6.7 shows the selected capacitors and their characteristics. In order to achieve the capacitance values of C_{in} and C_{out}, three of these devices are connected in parallel.

6.2.4 Heatsink and Thermal Interface

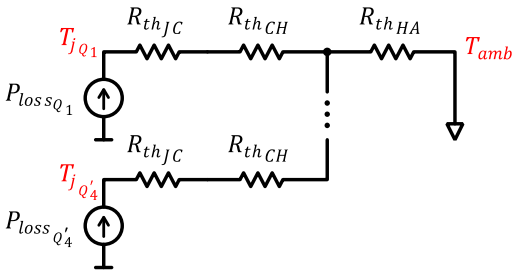
The heatsink, and the thermal interface between the heatsink and the semiconductors are defined based on a thermal resistance circuit. Fig. 6.13a Fig. 6.13b show the selected semiconductor distribution and the thermal resistance model for the primary side, respectively. As it can be observed, it is assumed that the 8 semiconductors from the primary side are attached to the same heat sink. Same thing is assumed for the secondary side devices. Table 6.8 describes each parameter from the circuit.

Table 6.7. Selected input and output capacitors.

Device	Manufacturer ID	Voltage class	Capacitance	I_{RMS}
C_{in}	MKP1848C71050JY5	1200 V	100 µF	20 A
C_{out}	MKP1848H62212JY5	500 V	22 µF	20 A



(a)



(b)

Fig. 6.13. (a) Semiconductor distribution. (b) Thermal resistance circuit model of the primary side.

Table 6.8. Main parameters of the thermal resistance circuit.

Parameter	Description	Value	
		IPZ60R017C7 (Primary side)	IKY40N120CS6 (Secondary side)
P_{loss_Q}	Power losses of the semiconductor	26.7 W	15.9 W
T_{j_Q}	Junction temperature of the semiconductor	<150 ºC	<175 ºC
$R_{th_{JC}}$	Junction to case thermal resistance	0.28 ºC/W	0.3 ºC/W (IGBT) 0.78 ºC/W (diode)
$R_{th_{HA}}$	Heatsink to ambient thermal resistance	0.0691 ºC/W[20]	0.0691 ºC/W[20]
$R_{th_{CH}}$	Case to heatsink thermal resistance	<1.98 ºC/W	<3.39 ºC/W

The first parameter in Table 6.8 is P_{loss_Q}, which is obtained from the power converter model. The results shown in Table 6.8 correspond to the peak power losses. As expected, the primary side presents higher losses due to the high current. The next three parameters (T_{j_Q}, $R_{th_{JC}}$ and $R_{th_{HA}}$) are given by the datasheet of the semiconductors and heatsink. Then, the value of $R_{th_{CH}}$ is obtained by solving the electric circuit from Fig. 6.13b. First, the heatsink temperature (T_H) is computed using (6.9). In this case, a

[20] Heatsink reference: SV-8214JH4-RG42080L12/180FR GUASCH

temperature step is added to the ambient temperature. This temperature step is the division between the sum of the power losses of the 8 semiconductors attached to the heatsink and $R_{th_{HA}}$. It is assumed that the power losses of the 8 semiconductors is the same and the ambient temperature is stablished at 25 ºC. Finally, the maximum value of $R_{th_{CH}}$ is obtained using (6.10). There, the maximum permitted junction temperature limits the value of $R_{th_{CH}}$. In this case, T_{j_Q} is limited to 100 ºC.

$$T_H = T_{amb} + \frac{8 \cdot P_{loss_Q}}{R_{th_{HA}}} \tag{6.9}$$

$$R_{th_{CH}} <= \frac{T_{j_Q} - T_H}{P_{loss_Q}} - R_{th_{JC}} \tag{6.10}$$

The result from (6.10) is used to select an appropriate thermal interface material (TIM). The TIM is the component located between the case of the semiconductor and the heatsink. Its purpose is to improve the thermal conductance between the semiconductor and the heatsink while it electrically insulates them. Table 6.9 describes the selected TIMs. The thermal conductivity is a heat flow through a unit area of a homogeneous material and it is given by the manufacturer. However, it does not take into account the thickness and area of the device. Therefore, the thermal resistance (R_{th}) is calculated using (6.11). As it can be observed, the TIM selected for the primary side presents a lower thermal resistance, but worse electrical insulation. This matches with the electrical characteristics of the converter.

$$R_{th_{TIM}} = \frac{1}{k} \cdot \frac{l}{A} \tag{6.11}$$

Where, k is the thermal conductivity, l is the thickness in meters, and A is the contact area of a TO-247-4 device (0.328 mm^2).

Table 6.9. Selected TIM for the semiconductors.

Device	Manufacturer ID	Thermal conductivity	Thickness	R_{th} (TO-247-4)	Voltage breakdown
Primary side	T-WORK9000	20 W/m·K	0.508 mm	0.16 ºC/W	3000 V
Secondary side	SIL-PAD 2000	3.5 W/m·K	0.38 mm	0.33 ºC/W	4000 V

The thermal resistance values from Table 6.9 are far from the ones required in Table 6.8. This safe-margin is assumed because the smoothness of the heatsink surface and the contact pressure of the semiconductors are not ideal. The expected maximum T_{j_Q} is 51 ºC and it corresponds to the primary side semiconductors. This occurs at initial charging conditions.

6.3 Prototype Assembly

Apart from the design of a 50 kW prototype, one of the main objectives of this work is to assemble it inside a standardized enclosure. This type of solutions are highly implemented in the industry due to their ease of assembly and modularization. Therefore, in order to get closer to a real case scenario, this work aims to fit the 50 kW converter inside a 19 inch (482.6 mm) 4U front panel rack.

Fig. 6.14 shows a real image of the assembled 19 inch rack. Originally, the front panel was completely smooth. However, several holes were added to include power connectors, manual switches and communication ports. More detailed information about each of these connectors is given later in this Chapter.

6.3.1 Transformer with Integrated Inductor

With the aim of reducing the volume of the magnetic elements, the leakage inductance (L_{lk}) of the transformer is designed to match the required inductance by the DAB-PPC. To achieve this, a magnetic design tool developed in Mondragon Goi Eskola Politeknikoa (MGEP) is used. Table 6.10 describes the input-output parameters of the concerned tool and the experimental results of the assembled transformer.

Fig. 6.14. Image of the assembled 19 inch rack.

Table 6.10. Parameters of the assembled transformer with integrated inductance.

Parameter	Design specifications	Assembly parameters	Experimental results
Current waveform	Fig. 6.15a	-	-
Voltage waveform	Fig. 6.15b	-	-
f_{sw}	20 kHz	-	-
n	0.1	-	0.0999
L_m (magnetizing)	-	324 µH	269.9 µH
L_{lk} (leakage)	6.3 µH	From 3.14 µH to 16.98 µH	From 5.75 µH to 8.89 µH
Core	-	EE8020	EE8020
Wire	-	400x200 (primary side) 200x100 (secondary side)	400x200 (primary side) 200x100 (secondary side)
Turns	-	6 (primary side) 60 (secondary side)	6 (primary side) 60 (secondary side)

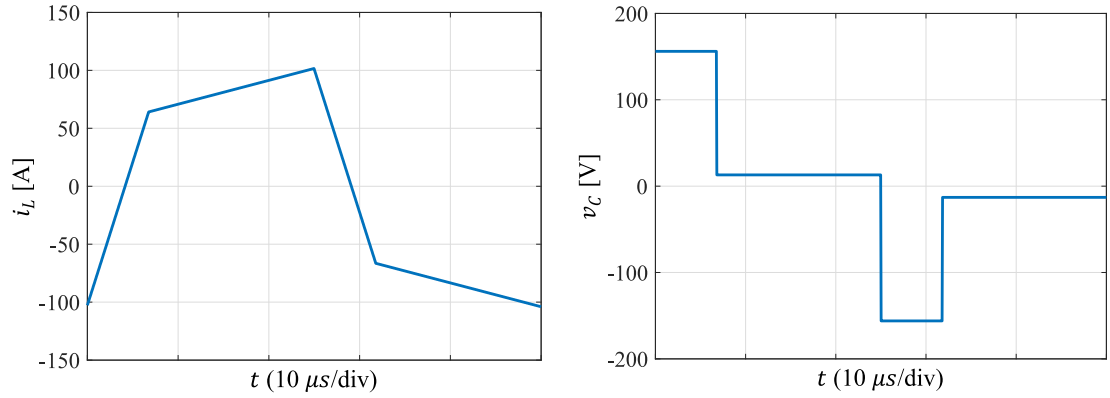


Fig. 6.15. Design specifications for the magnetic design tool. (a) Transformer current waveform at the primary side. (b) Transformer voltage waveform at the primary side.

The inputs or design specifications of the design tool are: the waveform of the most restrictive current and voltage waveforms (see Fig. 6.15), the switching frequency, the transformation ratio and the desired leakage inductance. The outputs or assembly parameters are: the core, the wire and the number of turns. The litz wire is defined as the number of strands (N_{st}) times the diameter of each strand in µm. Also, the expected magnetizing inductance and the leakage inductance range is defined. Based on the assembly parameters, the transformer shown in Fig. 6.16 is assembled. The difference between Fig. 6.16a and Fig. 6.16b is the distance between the primary and secondary windings. The closer they are (Fig. 6.16a case), the less flux leakage exists. Thus, the

(a) (b)

Fig. 6.16. Images of the assembled transformer. (a) Configuration for minimum leakage inductance. (b) Configuration for maximum leakage inductance.

minimum leakage inductance is achieved: L_{min}=5.75 μH. The further they are (Fig. 6.16b case), the higher the flux leakage. Hence, the maximum leakage inductance is achieved: L_{max}=8.89 μH. By adjusting the gap, the leakage inductance is set to 6.3 μH.

6.3.2 Rack assembly

Fig. 6.17a shows the front view design of the rack. As it can be observed, there are 2 positive-negative source connectors and 2 positive-negative load connectors. Then, there is the 230 V connector, which supplies the DSP and the fans. In this regard, there are two switches: Supply (coloured in red) and Enable (coloured in green). The "Supply" switch connects the 230 V to the auxiliary circuit (DSP, fans…). The "Enable" switch activates the power flow by enabling the PWM signals. Also, 3 communication ports are available to communicate with the DSP: 2 input-output ports for controller area communication (CAN) communication and 1 for A-type universal serial bus (USB). Additionally, two holes are added to allow the fans' intake of air.

In Fig. 6.17b, the top view of the arrangement of the different components is shown. Great part of the volume is occupied by the primary side and secondary side power blocks (including the heatsinks and fans). The DSP is located on the top-left corner and the power supply is attached to the back-side panel. The transformer is highlighted to observe its volume. Finally, the top-case temperature measurements are taken out in case this information is required. The design of the PCBs is explained at Appendix A in detail.

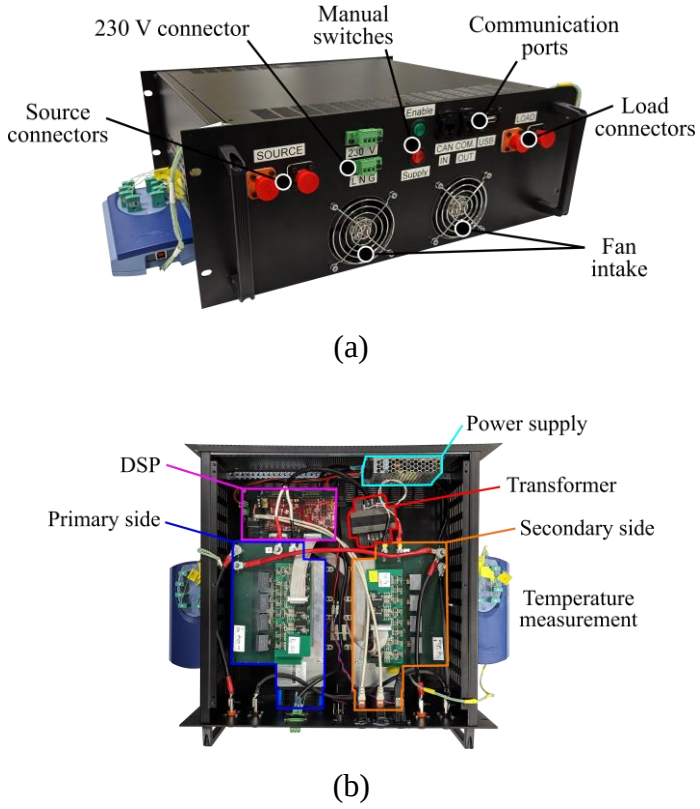


Fig. 6.17. Final image of the assembled rack. (a) Front view. (b) Arrangement of the components.

6.4 Test Modes

Testing a power converter at 800 V and 50 kW entails a challenge equipment-wise. It is difficult and expensive to find power supplies and power loads that can work at these conditions. Therefore, in order to test the designed 50 kW PPC, three different tests are carried out (see Fig. 6.18):

1. **FPC mode.** Due to the PPC configuration, the power processed by the converter is limited to less than 5 kW. In fact, its maximum input voltage-current are 85 V and 60 A, and its maximum output voltage-current are 800 V and 7 A. So, by implementing the FPC configuration presented in Fig. 6.18a, the nominal working conditions of the converter can be tested with no need of high power equipment.
2. **PPC mode at low power conditions.** Fig. 6.18b shows the typical ISOP type PPC configuration. In order to test this configuration, high-voltage (800 V) and high-current (60 A) equipment is required. The available equipment in the lab is limited to 1500 V, 40 A, 18 kW. Therefore, the power that is transferred from the source

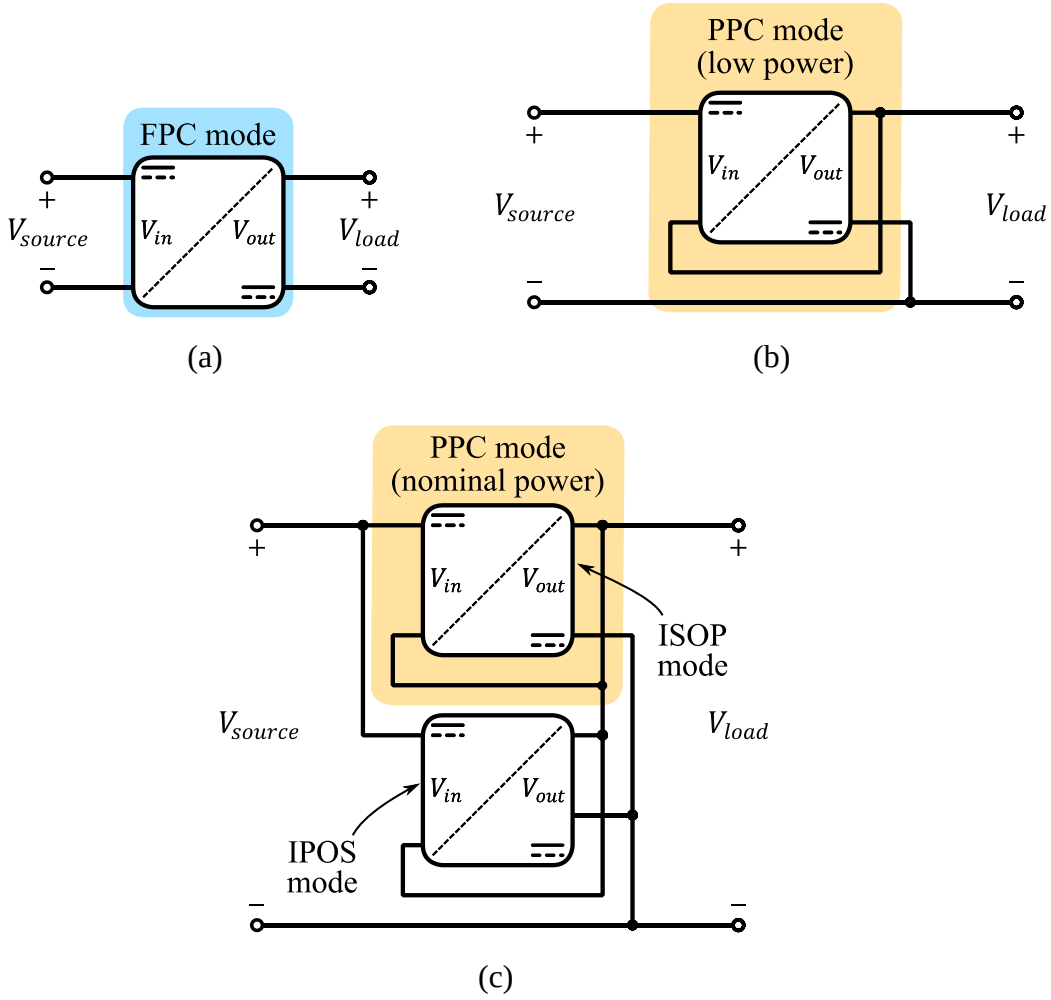


Fig. 6.18. Test modes for the experimental validation. The shaded area defines the converter under test. (a) FPC mode. (b) PPC mode at low power conditions. (c) PPC mode at nominal power conditions.

to the load is limited by the equipment. This configuration mode is useful to test the converter under low power conditions before moving to nominal conditions.

3. **PPC mode at nominal power conditions.** In order to decrease the power observed by the equipment, a second converter is built and connected in parallel, see Fig. 6.18c. Then, one of the converters forces a power flow from V_{source} to V_{load} (ISOP mode) and the second one does the opposite (IPOS mode). This way, the power observed by the equipment is just the sum of the power losses of both converters.

Table 6.11. Selected TIM for the semiconductors.

Test condition		Description	Voltage	Current	Power
FPC mode	Source	IT6015C-80-360	80 V	360 A	15 kW
	Load	IT6012C-800-40	800 V	40 A	12 kW
PPC mode (low power)	Source	ITECH IT6018C-1500-40	1500 V	40 A	18 kW
	Load	ITECH IT6018C-1500-40	1500 V	40 A	18 kW
PPC mode (nominal power)	Source	ITECH IT6018C-1500-40	1500 V	40 A	18 kW
	Load	ITECH IT6018C-1500-40	1500 V	40 A	18 kW

Table 6.11 lists the equipment used at each test condition. As it can be observed, the required equipment at FPC mode consists of a low-voltage high-current source and a high-voltage low-current load. On the other hand, at PPC mode two bidirectional ITECH power supplies are implemented. It is necessary to highlight the fact that both supplies are bidirectional, especially when working at nominal power conditions. At these working condition, any mismatch between the two converters must be compensated by both supplies. Therefore, depending on the power transferred by each converter, each power supply must give or absorb power.

6.5 Experimental Results

In the first place, the test conditions must be described. Fig. 6.19 shows the five test conditions that are used to experimentally validate the prototype. These curves are based on the operation range defined in Fig. 6.4 and the points are equally distributed from 10

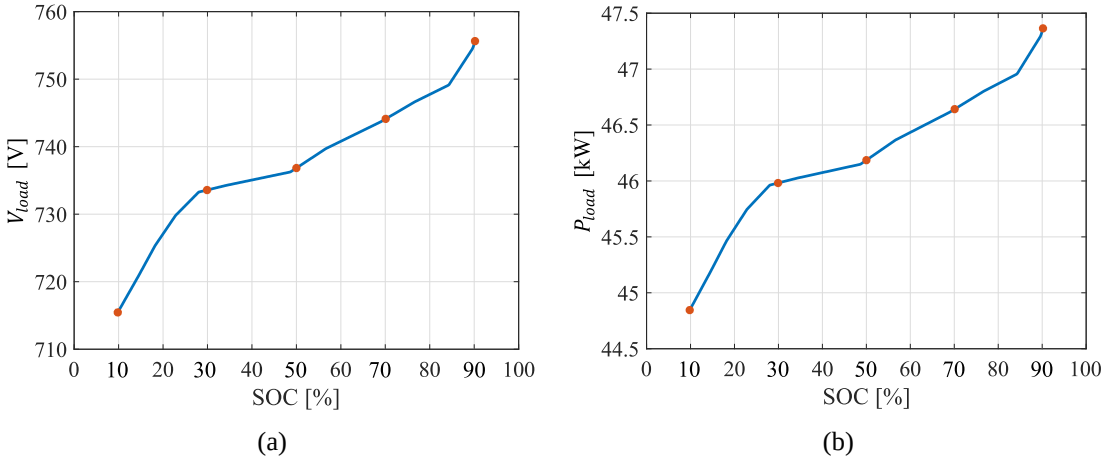


Fig. 6.19. Test conditions with constant V_{source} at 800 V. (a) Load voltage. (b) Load power.

% SOC to 90 % SOC. Appendix B describes in detail how the experimental steady state waveforms, top-case temperatures and efficiencies are obtained.

6.5.1 FPC Mode

The objective of this test is to replicate the working conditions of the converter at FPC mode. Based on the curves from Fig. 6.19 and using (6.12)-(6.14), the test conditions at FPC mode are defined in Fig. 6.20. At FPC mode, the source gets the values of V_{in}, and the load gets the values of V_{out} and P_{out}. As it can be observed in Fig. 6.20, the test point at 10 % SOC is shifted to 14 % SOC. This is because the equipment used as a source is limited to 80 V.

$$V_{source_{FPC}} = V_{in} = V_{source} - V_{load} \tag{6.12}$$

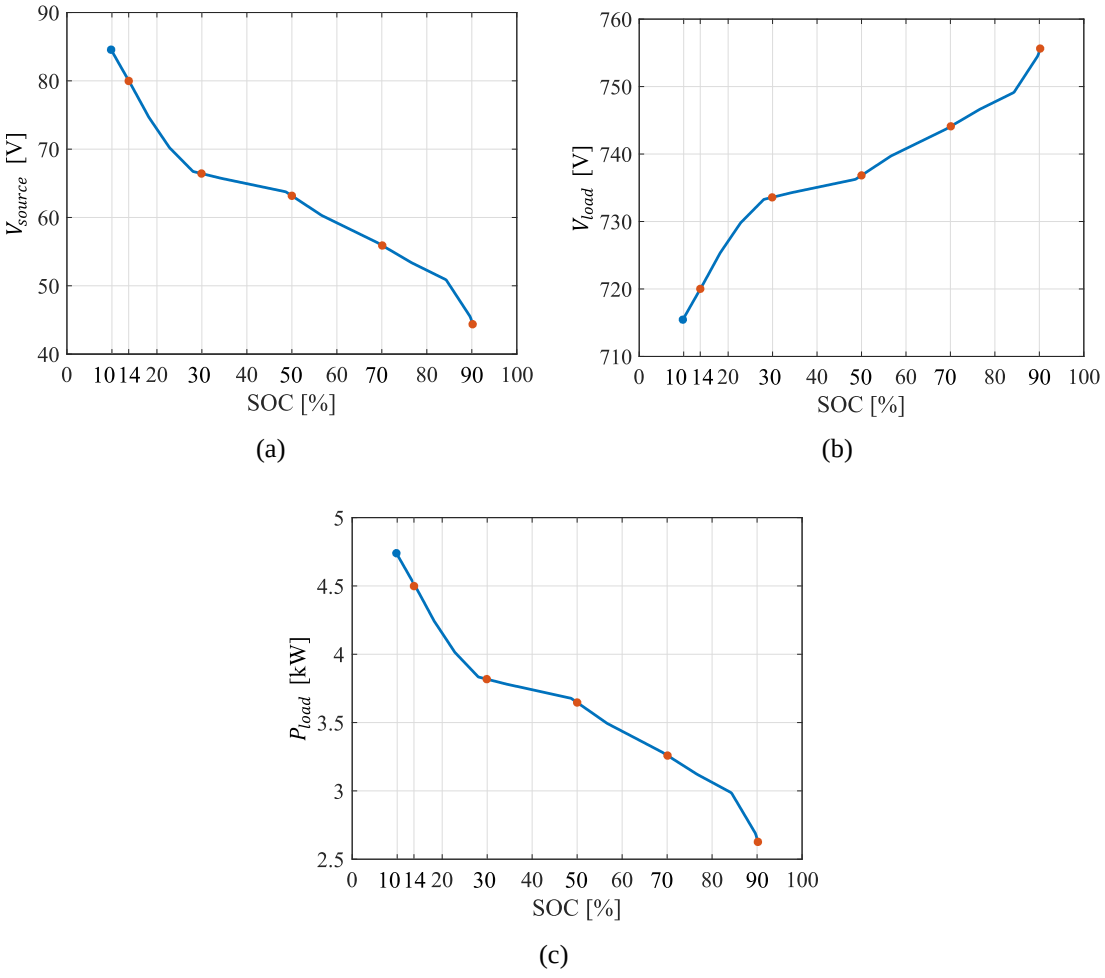


Fig. 6.20. Test conditions at FPC mode. (a) Source voltage. (b) Load voltage. (c) Load power.

$$V_{load_{FPC}} = V_{out} = V_{load} \tag{6.13}$$

$$P_{load_{PPC}} = P_{out} = P_{load} \cdot K_{pr} = P_{load} \cdot (1 - G_V) \tag{6.14}$$

Fig. 6.21a and Fig. 6.21b present the steady state waveforms at the two edge test points: 14 % SOC (initial charging point) and 90 % SOC (end of charging). Both waveforms confirm that ZVS is ensured to all the semiconductors through all the charging process. This is concluded from the inductor waveform (i_L). Fig. 6.21c shows the experimental inductor RMS current at the primary side. The results go from 76.4 A to 72 A and they show a convex behavior similar to the one from Fig. 6.7 with L=5.2 µH.

Then, Fig. 6.22 compares the efficiency results obtained with the devices from Table 6.6. Fig. 6.22a shows the experimental converter efficiency. Since the test is carried out at FPC mode, the efficiency of the converter and the efficiency of the system are the

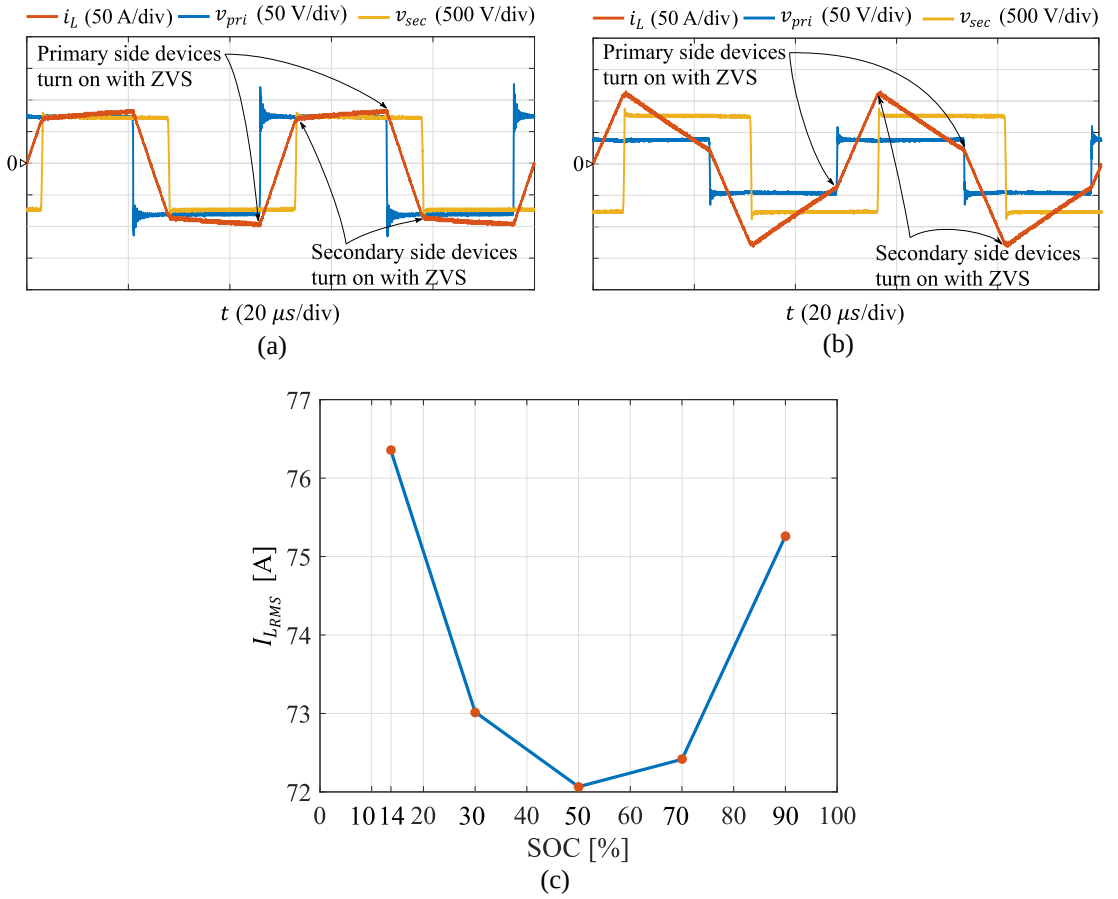


Fig. 6.21. Experimental results at FPC mode. (a) Steady state waveforms at 14 % SOC. (b) Steady state waveforms at 90 % SOC. (c) Inductor RMS current at the primary side.

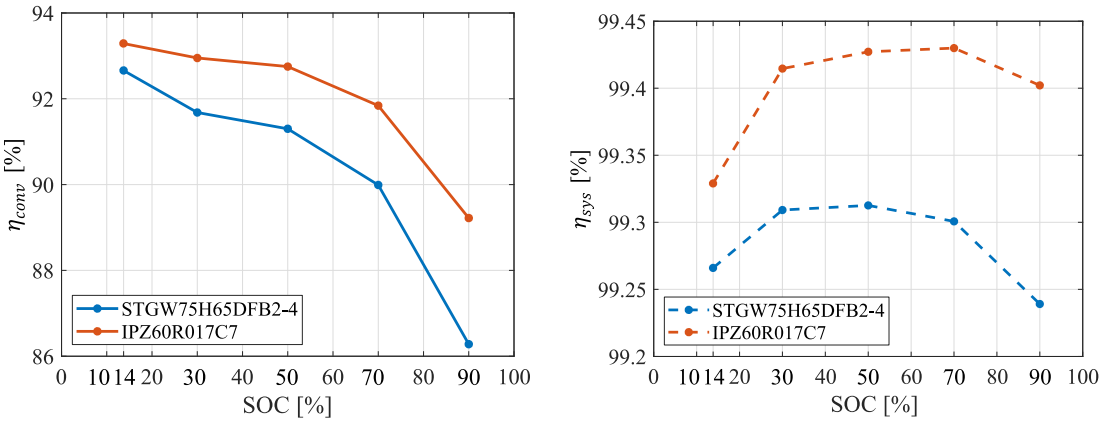


Fig. 6.22. Efficiency results at FPC mode. (a) Experimental converter efficiency. (b) Expected system efficiency at PPC mode.

Table 6.12. Top-case temperature of the most heated semiconductor at FPC mode.

SOC	Temperature	
	Primary side	Secondary side
14 %	44.8 ºC	36.9 ºC
30 %	41.7 ºC	38.4 ºC
50 %	41.5 ºC	38.6 ºC
70 %	40.7 ºC	39.5 ºC
90 %	42.1 ºC	41.6 ºC

same. However, in order to estimate the system efficiency that would exist at PPC mode, Fig. 6.22b shows the expected system efficiency. This value is given by (6.15). As it can be observed, the expected efficiencies are higher than 99 %. The results from Fig. 6.22 confirm that the MOSFET device (IPZ60R017C7) is more efficient.

$$\eta_{sys} = 1 - K_{pr}(1 - \eta_{conv}) \tag{6.15}$$

Table 6.12 shows the top-case temperature of the most critical device at each side of the DAB. The primary side semiconductors decrease their temperature as the battery is charged, except for the last test point. This is directly related to the inductor RMS current from Fig. 6.21c. However, the temperature of the secondary side semiconductors increases with the SOC. This is because of the switching losses, which are dependent on the voltage. As the SOC increases, V_{load} and the voltage blocked by the secondary side devices increase too. The temperature results validate the selected heatsink and TIMs.

6.5.2 PPC Mode at Low Power Conditions

The purpose of this test is to validate the prototype at the ISOP configuration. Since the equipment from the lab is limited to 1500 V, 40 A, 18 kW, this test is limited to the maximum capabilities of the equipment. So, the curves from Fig. 6.19 are downscaled by a ratio of 1.8, see Fig. 6.23. This way, the shape of the steady state waveforms is kept the same and the maximum current observed by the equipment is 40 A.

Fig. 6.24 shows the steady state waveforms at 10 % SOC and at 90 % SOC. Except for the scale, the current and voltage waveforms have a very similar shape to the ones from Fig. 6.21. Apart from that, Fig. 6.25 presents the inductor RMS current and system efficiency results. Both curves are coherent, so the ISOP configuration is validated and the prototype is tested at nominal power conditions.

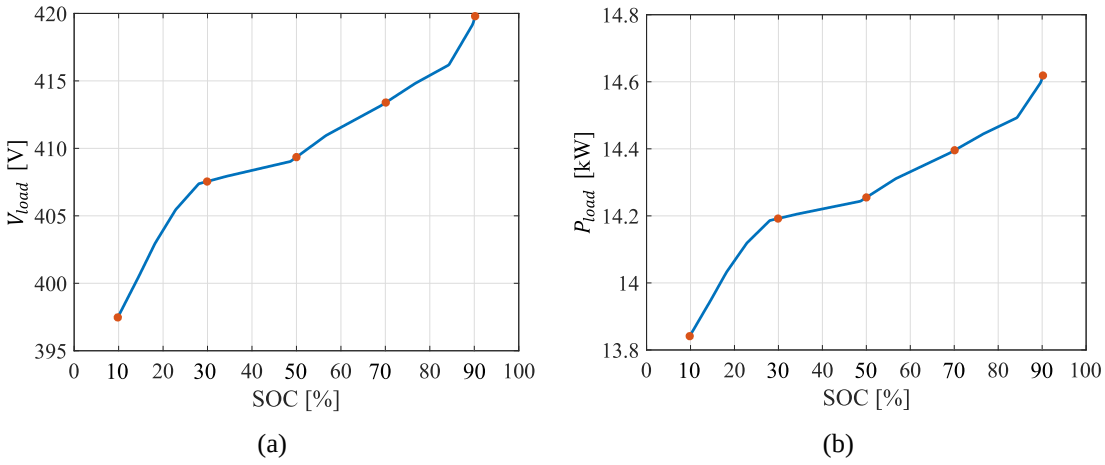


Fig. 6.23. Test conditions at PPC mode and low power conditions. V_{source} is kept constant at 444 V. (a) Load voltage. (b) Load power.

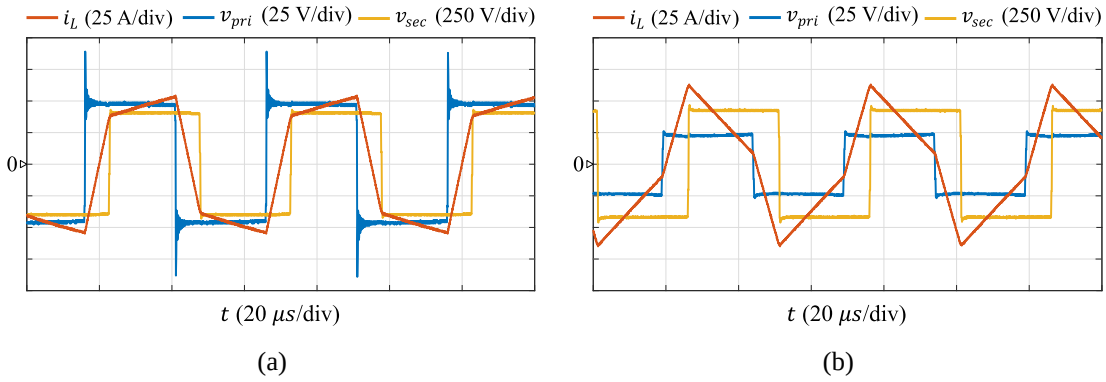


Fig. 6.24. Experimental steady state waveforms at PPC mode with low power conditions. (a) At 10 % SOC. (b) At 90 % SOC.

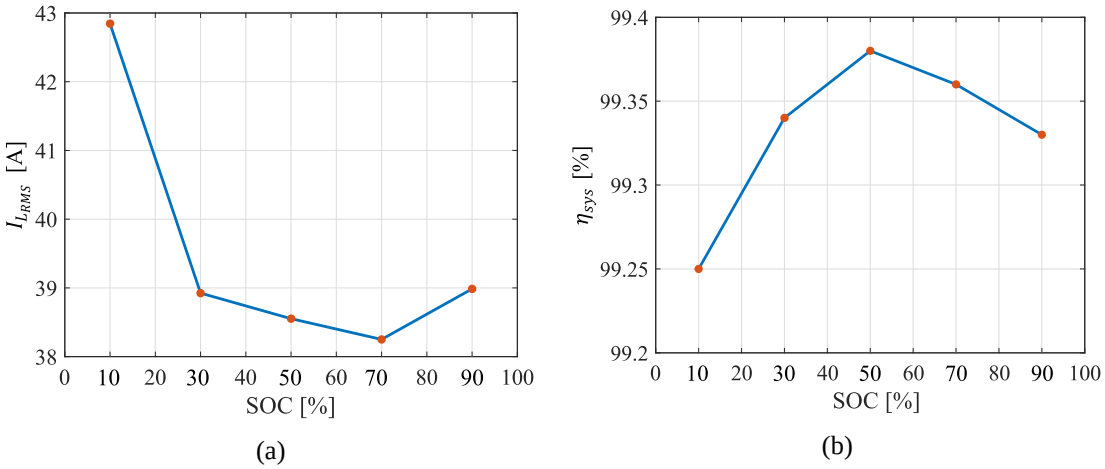


Fig. 6.25. Experimental results at PPC mode with low power conditions. (a) Inductor RMS current. (b) System efficiency.

6.5.3 PPC Mode at Nominal Conditions

The aim of this test is to validate the design of the assembled 50 kW PPC. As shown in Fig. 6.18c, two power converters are assembled, but the one under analysis is the converter working in ISOP mode. In this case, the test conditions are the ones defined in Fig. 6.19.

In the first place, Fig. 6.26 shows the steady state waveforms of both converters. Fig. 6.26a and Fig. 6.26b show the steady state waveforms of the ISOP mode converter at the two edge test points: at 10 % SOC and at 90 % SOC. Fig. 6.26c and Fig. 6.26d show the results of the IPOS mode converter. The main difference between them is the leading AC voltage: v_{pri} (at Fig. 6.26a and Fig. 6.26b) and v_{sec} (at Fig. 6.26c and Fig. 6.26d). The waveforms of the ISOP mode converter conclude that ZVS is ensured through all the charging process. Also, they show very similar shapes to the ones from Fig. 6.21 at FPC mode. This validates the FPC mode as a low-scale solution for PPC architecture testing at nominal conditions.

Fig. 6.27a and Fig. 6.27b present the inductor RMS current at the primary side and the system efficiency results at each test point. The efficiency results confirm the expected efficiencies from Fig. 6.22. As it can be observed, the obtained efficiencies are always higher than 99 %. The peak efficiency is 99.47 % and it occurs at the end of the charging process, when the K_{pr} is at its minimum value.

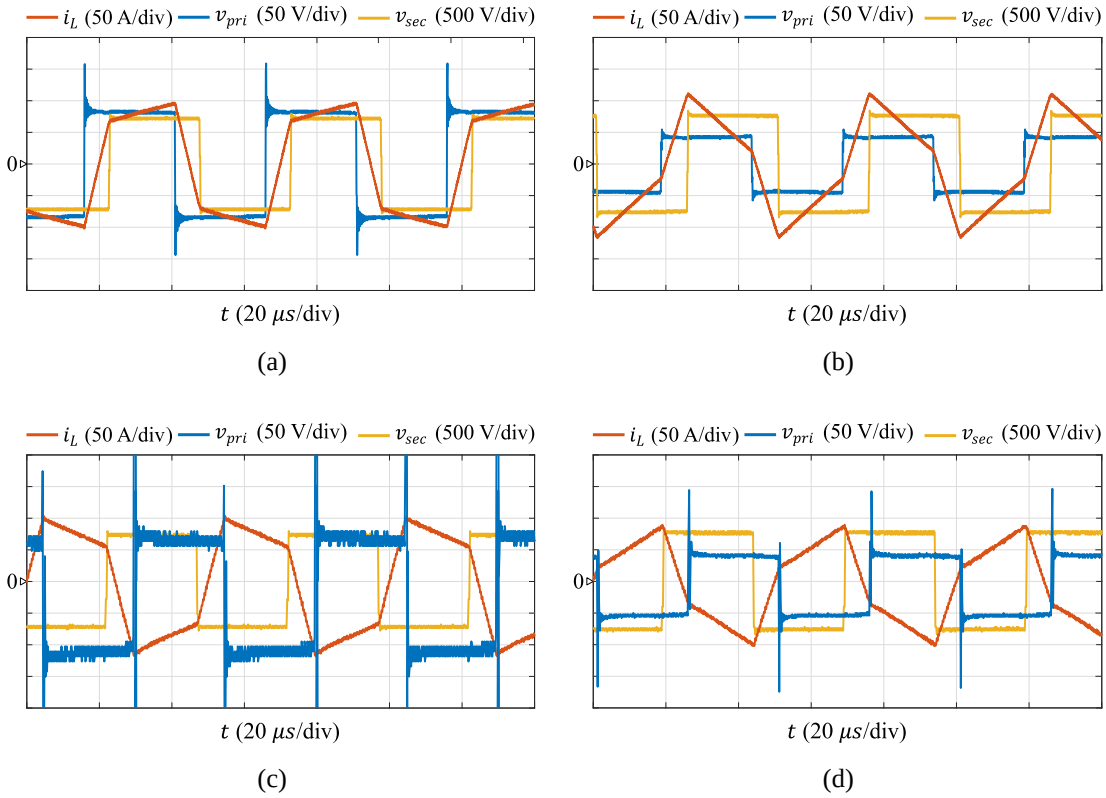


Fig. 6.26. Experimental steady state waveforms at PPC mode with nominal power conditions. ISOP mode converter at (a) 10 % SOC and at (b) 90 % SOC. IPOS mode converter at (c) 10 % SOC and at (d) 90 % SOC.

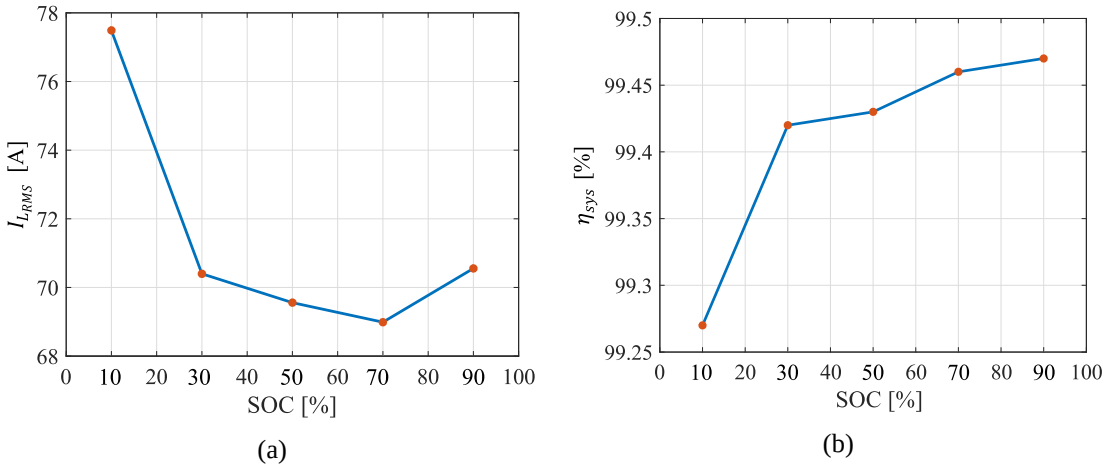


Fig. 6.27. Experimental results at PPC mode with nominal power conditions. (a) Inductor RMS current. (b) System efficiency.

Fig. 6.28 presents the top-case temperature evolution of the most heated semiconductor at each side of the transformer. The dashed lines point out the steady state temperature at each test point. The curves show that the primary side and the secondary

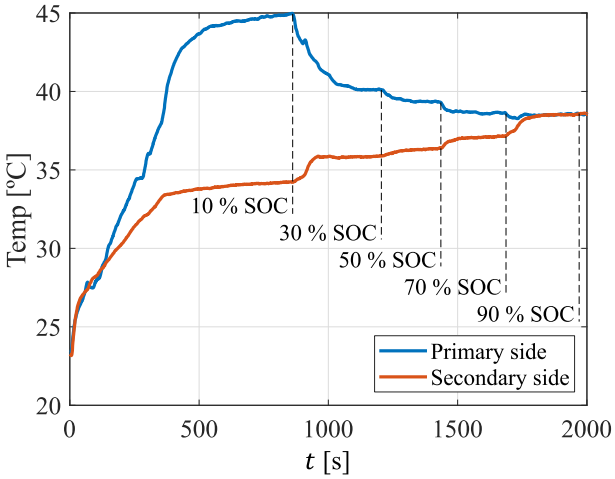


Fig. 6.28. Top-case temperature evolution at PPC mode with nominal power conditions.

side devices present opposite behaviour as the SOC increases. As concluded at FPC mode, the temperature of the primary side semiconductors decreases with the inductor RMS current. On the other hand, the secondary side devices heat up due to the increment of the blocked voltage. Nevertheless, the maximum top-case temperature is 45 ºC (at 10 % SOC case), which thermally validates the design.

Due to the low temperature of the devices, an extra test point is carried out to analyze the maximum power point of the converter. With this purpose, the most efficient test point from Fig. 6.27 is selected (90 % SOC case): V_{source}=800 V and V_{load}=755 V. In this case, the phase-shift is raised from 53.5º (nominal phase-shift) to 90º (maximum power phase-shift). Fig. 6.29 shows the steady state waveforms of the inductor current and the AC voltages. As it can be observed, the phase-shift between the square waveforms is 90º. Table 6.13 presents the main results at this working point. As it can be observed, the load power is increased up to almost 60 kW and the efficiency is kept above 99 %. Apart from that, the top-case temperature of the semiconductors does not surpass the 60 ºC. This is mainly due to the applied safe-margin when selecting the TIMs.

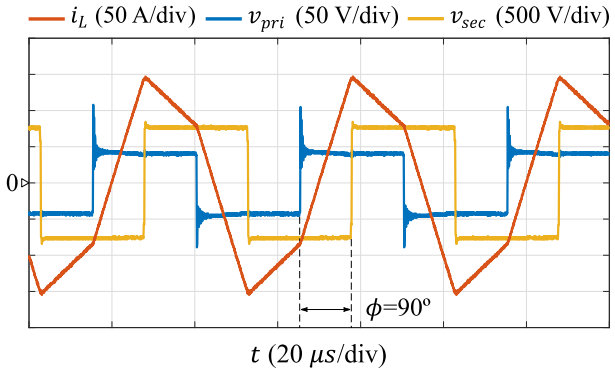


Fig. 6.29. Steady state waveforms at PPC mode and maximum power transferred by the converter.

Table 6.13. Main results at PPC mode and transferring the maximum power.

Parameter	Value
$I_{L_{RMS}}$	101.37 A
P_{load}	59.28 kW
η_{sys}	99.24 %
Top-case temperature	55.6 ºC primary side 42.2 ºC secondary side

6.5.4 Extended Operation Range

The operation range defined in Fig. 6.4 only considers a CC charging from 10 % SOC to 90 % SOC. This subchapter presents the results obtained with the designed converter when working out of the nominal operation range. Fig. 6.30 shows the test conditions. As it can be observed, 2.5 % SOC steps are defined to obtain a mayor

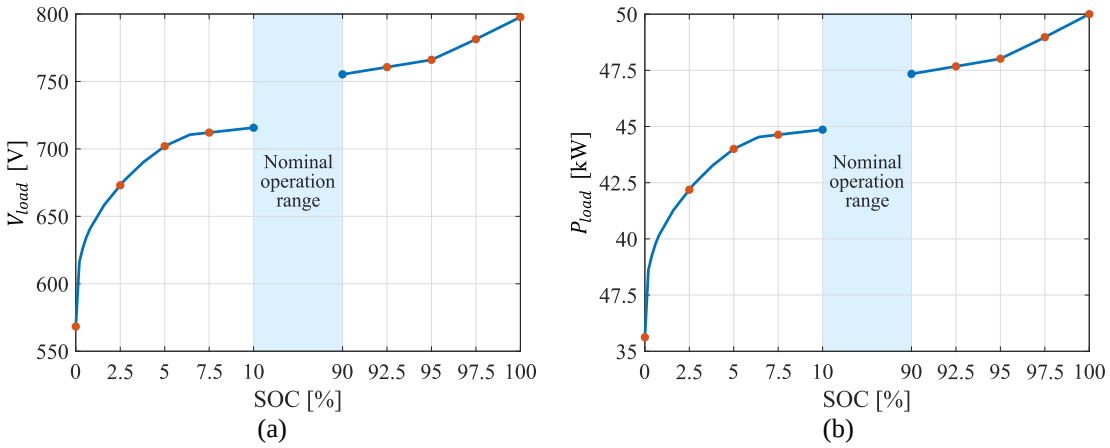


Fig. 6.30. Test conditions at PPC mode and extended operation range. V_{source} is kept constant at 800 V. (a) Load voltage. (b) Load power.

precision of the voltage and power curves. The markers at 10 % SOC and 90 % SOC are colored in blue because they correspond to the nominal operation range.

Fig. 6.31 presents the ZVS boundaries of the semiconductors including the extended operation range. Due to the low value of V_{in} (below 10 V) at the end of the charging process, a high M $\left(\frac{V_{out} \cdot n}{V_{in}}\right)$ is obtained above 90 % SOC. In consequence, Fig. 6.31 is highly distorted and a zoomed area is included. The main conclusion that is obtained from Fig. 6.31 is that the primary side and the secondary side semiconductors leave the ZVS region. The primary side devices enter in hard switching conditions at SOC values above 90 %, and the secondary side semiconductors at SOC values below 10 %.

Fig. 6.32 shows the steady state waveforms at the two edge test conditions: 2.5 % SOC and 100 % SOC. The 0 % SOC test condition is avoided for two reasons: extremely high RMS currents occur and the hard switching conditions at the secondary side disable the communication between equipment.

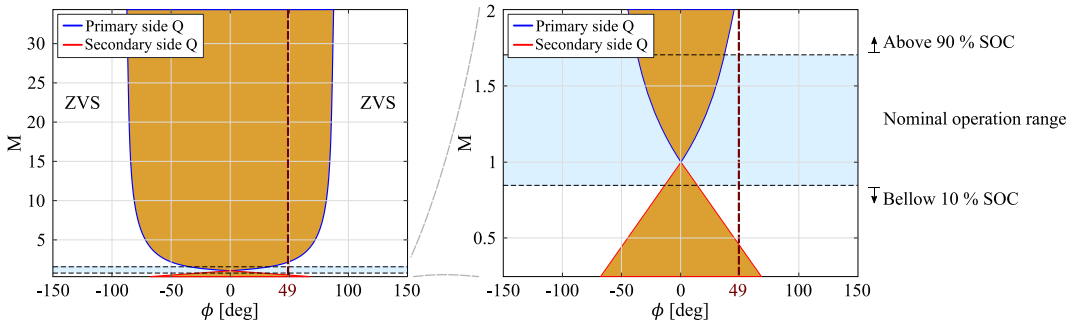


Fig. 6.31. ZVS regions and boundaries for primary and secondary side semiconductors using PSM including the extended operation range.

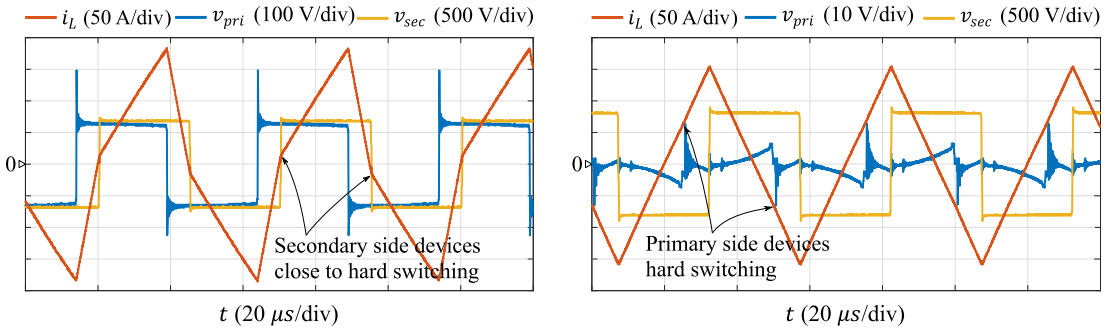


Fig. 6.32. Experimental steady state waveforms at PPC mode and extended operation range. (a) Steady state waveforms at 2.5 % SOC. (b) Steady state waveforms at 100 % SOC.

The results at 2.5 % SOC (Fig. 6.32a) show an inductor peak value of 175 A and the voltage blocked by the primary side devices surpasses 100 V. Although ZVS is ensured for all the semiconductors, it is observed that the secondary side devices are close to hard switching conditions. The waveforms at 100 % SOC (Fig. 6.32b) show more favourable results. The inductor peak current is reduced to 150 A and the voltage blocked by the primary side devices is almost negligible. This is because the voltage difference between the source and the load is only 3 V. At this point, the primary side devices switch under hard switching conditions. However, the blocked voltage is so low that the main losses are still due to the conduction.

Fig. 6.33 presents the experimental inductor RMS current and system efficiency results. As it can be observed, both curves are related to each other. At 2.5 % SOC, due to the high inductor RMS current the efficiency is lower. But, as the RMS current is reduced, the efficiency improves. Although the inductor RMS current above 90 % SOC is similar to the one obtained below 10 % SOC (except for 2.5 % SOC), its efficiency remains higher. This is because above 90 % SOC the K_{pr} is lower, which provokes lower voltage at the primary side; thus, lower switching losses.

Finally, Table 6.14 presents the top-case temperature of the most heated semiconductor at each side of the DAB. As it can be observed, the most critical point for the devices occurs at very low SOC values. However, the maximum steady state temperature is far from the T_j recommended by the manufacturer.

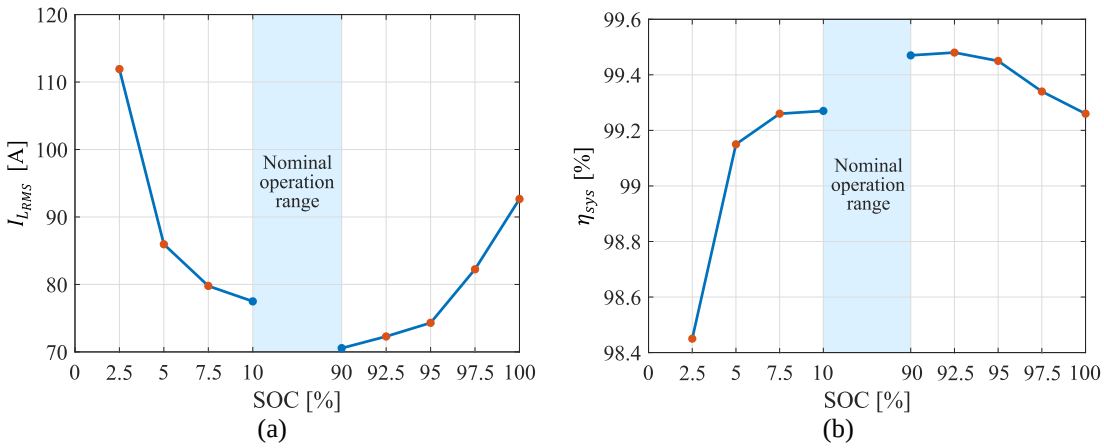


Fig. 6.33. Experimental results at PPC mode and extended operation range. (a) Inductor RMS current. (b) System efficiency.

Table 6.14. Top-case steady state temperature of the most heated semiconductor at PPC mode and extended operation range.

SOC	Temperature	
	Primary side	Secondary side
0 %	-	-
2.5 %	72.4 ºC	46.6 ºC
5 %	50.4 ºC	32.0 ºC
7.5 %	45.5 ºC	32.6 ºC
92.5 %	37.0 ºC	37.0 ºC
95 %	38.7 ºC	37.8 ºC
97.5 %	46.5 ºC	40.0 ºC
100 %	45.7 ºC	42.2 ºC

6.5.5 400 V EV Charging

The prototype under analysis is designed to supply an ESS of 800 V. However, current EV vehicles can also contain a battery voltage of 400 V. Therefore, the designed converter is also tested for charging these group of EVs. In order to keep a low voltage gain between the source and the load, V_{source} is decreased from 800 V to 400 V. This voltage difference should be given by the AC-DC stage. Fig. 6.34 shows the test conditions including the extended operation range. The test condition at 0 % SOC is also avoided in this case.

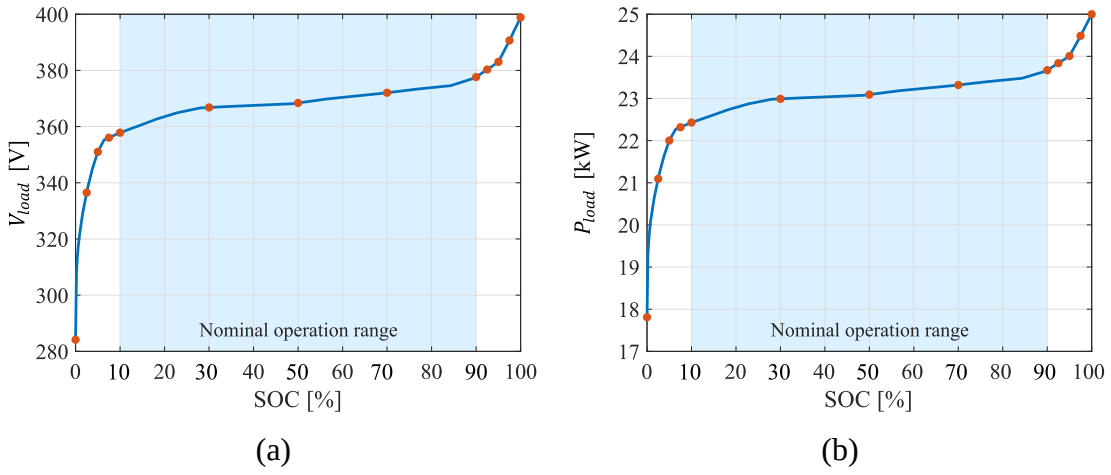


Fig. 6.34. Test conditions at PPC mode for 400 V EV charging. Extended operation range is included. V_{source} is kept constant at 400 V. (a) Load voltage. (b) Load power.

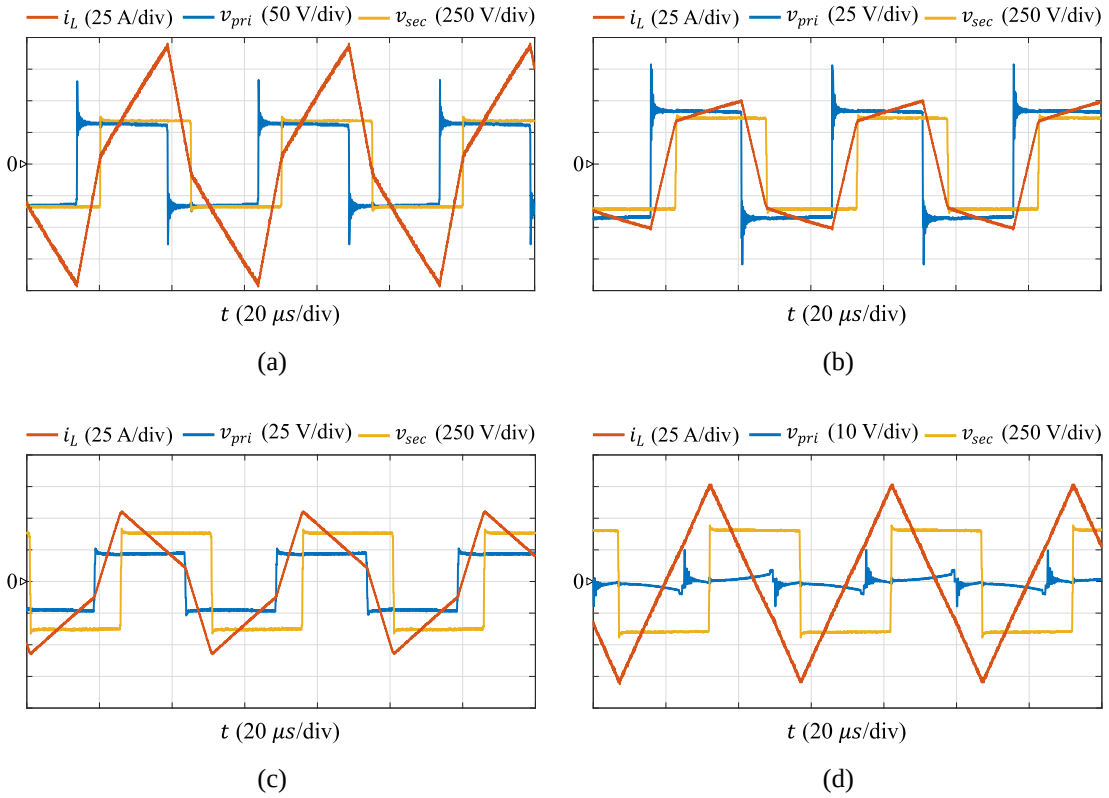


Fig. 6.35. Experimental steady state waveforms at PPC mode for 400 V EV charging. (a) At 2.5 % SOC. (b) At 10 % SOC. (c) At 90 % SOC. (d) At 100 % SOC.

First, Fig. 6.35 presents the steady state waveforms at four different points: 2.5 % SOC, 10 % SOC, 90 % SOC and 100 % SOC. The shape of the waveforms is very similar to the one obtained for 800 V EV charging. At 2.5 % SOC (Fig. 6.35a), secondary side devices are close to hard switching. From 10 % SOC to 90 % SOC (Fig. 6.35b and Fig. 6.35c), ZVS operation is ensured. At 100 % SOC (Fig. 6.35d), the primary side devices work under hard switching conditions. Compared to the 800 V case, the main difference is the scale of the current and voltage waveforms.

Second, Fig. 6.36 shows the inductor RMS current and the system efficiency. The obtained efficiency is higher than 99 % through great part of the charging process. Due to the high inductor RMS current at 2.5 % SOC, the efficiency at this point decreases down to 98.4 %. The maximum top-case temperature is 35.5 ºC and it corresponds to a primary side device at 2.5 % SOC.

Assuming the AC-DC stage is able to regulate the DC bus voltage, it is concluded that the designed converter is also valid to charge a 400 V EV.

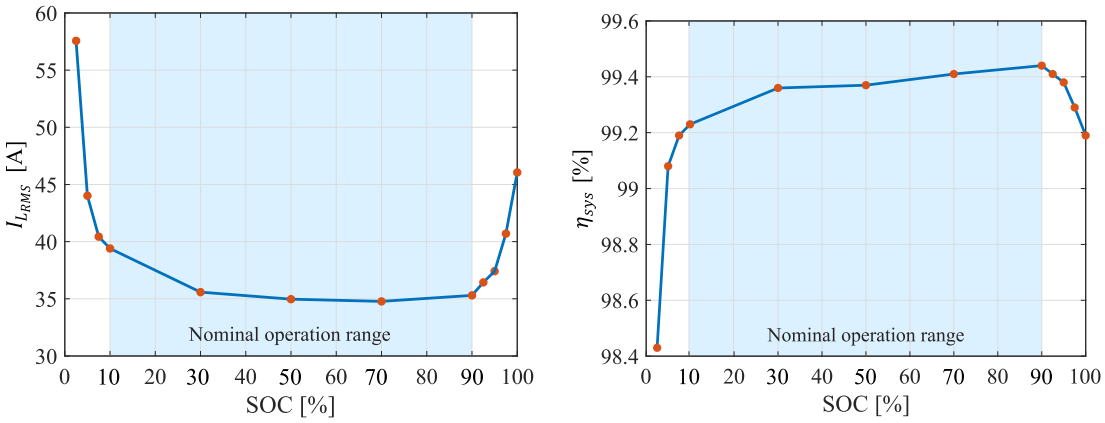


Fig. 6.36. Experimental results for 400 V EV charging. (a) Inductor RMS current. (b) System efficiency.

6.6 Discussion

With the objective of summarizing the goals achieved with the designed 50 kW PPC, Table 6.15 describes the main design parameters and results of the prototype.

First, the volume of the magnetic is highly reduced by matching the leakage inductance of the transformer to the one required by the design. This is achieved by following the design steps given by the magnetic design tool developed in MGEP.

Second, TO-247-4 discrete Si-based devices are validated for a 50 kW application. This is a great achievement since these type of high power applications are assigned for module type packages or SiC-based technology.

Table 6.15. Design and results of the 50 kW PPC.

Parameter	Value	Description
Transformer with integrated inductance	L_{lk}=6.3 µH n=0.1	A single EE8020 core is used. The leakage inductance of the transformer is designed to match the required L.
Primary side semiconductor	IPZ60R017C7	TO-247-4 discrete MOSFET
Secondary side semiconductor	IKY40N120CS6	TO-247-4 discrete IGBT
$\widehat{P_{load}}$	59.28 kW	The maximum power is achieved with a phase-shift value of 90º at 90 % SOC. @ η_{sys}=99.24 %
$\widehat{\eta_{sys}}$	99.47 %	The peak efficiency is achieved with nominal power conditions at 90 % SOC.
Maximum top-case temperature	72.4 ºC	The maximum top-case temperature is measured at the primary side at 2.5 % SOC.

Third, a maximum power of 59.28 kW is transferred to the load at a system efficiency of 99.24 %. However, a peak efficiency of 99.47 % is achieved at nominal conditions. A system efficiency above 99 % at high power applications entails a reduction of hundreds of watts. Also, the maximum top-case temperature is 72.4 ºC, so the prototype is thermally validated.

In conclusion, the assembled PPC prototype is a high power (50 kW nominal power), reduced size (single magnetic and discrete devices), high efficient (above 99 %) and reduced cost (Si-based technology) solution.

Chapter 7

CONCLUSIONS AND OUTLOOK

In this final Chapter the main conclusions of this research work are presented. In this sense, the following steps of the research project will be based on the conclusions presented below.

7.1 Conclusions

In the present work, PPP-based architectures for DC-DC applications are investigated. In Chapter2, three main PPP strategies are identified: DPC, PPC and mixed strategies. Based on the evaluation of their characteristics, PPC-based architectures are selected for further analysis due to their numerous applications and high efficiency. Accordingly, PPC architectures are investigated in detail. The main conclusions and results are summarized in the following list:

- In Chapter 3, PPC architectures that do not require isolated topologies are investigated. This includes the FCC architectures. In this sense, two different topologies are implemented in FPC and PPC architectures, and their performance is compared. The conventional single inductor HB topology performs equally on FPC and PPC architectures. No benefits are observed in terms of lower electrical stress of power losses reduction. On the other hand, the double inductor MSIBC topology improves its performance on a PPC architecture. The experimental results show a lower top-case temperature and a higher efficiency. Nevertheless, the MSIBC-PPC does not present outperform the conventional HB-FPC.
- In Chapter 4, IPOS-ISOP type PPC architectures are investigated through the analysis of two case studies:
    - Isolated topology based PPC vs. non-isolated topology based FPC. The first case study compares the performance of an isolated topology based PPC (DAB-PPC) to a non-isolated topology based FPC (IHB-FPC). It concludes that DAB-PPC has improved performance than the IHB-FPC in aspects such as: lower volume of magnetics and reduced electrical stress of magnetics and switching devices. System efficiency-wise, the DAB-PPC also presents higher results at low K_{pr} (bellow 0.16). However, as the K_{pr} increases, its efficiency is penalized.
    - Si-based PPC vs. SiC-based FPC. The second case study compares the performance of a Si-based DAB-PPC to a SiC-based DAB-FPC for an OBC application. Due to the benefits of PPP, the DAB-PPC architecture requires lower voltage class semiconductors (with low on-state resistance)

and its devices suffer a lower electrical stress. The work concludes that the Si-based DAB-PPC has improved performance than SiC-based DAB-FPC in all metrics: thermal stress, efficiency, volume and cost.

- In Chapter 5, three different applications of IPOS-ISOP type PPC architectures are studied. Each application presents different characteristics, so an adapted design criteria is presented for each application:
    - Electric vessel. This application is focused on a modular power converter solution for a HESS. The series connection of modular PPCs entails significant overvoltage issues and this work presents the design steps that must be considered.
    - Hydrogen generation. This application is focused on the measure and design of the PPC connected to the electrolyzer. Based on the voltage-current curves of the application, a buck mode configuration is concluded as the ideal solution to reduce the maximum power processed by the converter without increasing the complexity of the circuit.
    - EV fast charging station. This application is focused on the design of the DC-DC stage of an EV fast charging application. The implemented topology consists of a DAB-PPC and three different transformer turn ratios are compared in terms of processed active and non-active power, and energy losses through the charging process. The results conclude that optimizing the design of the converter for working conditions where K_{pr} is higher achieves a more favorable performance.
- In Chapter 6, the design and assembly of a 50 kW PPC is validated for EV charging. The selected topology is a DAB and its number of semiconductors is doubled to reduce their stress. Due to the PPC configuration, the maximum power processed by the converter is reduced to less than 5 kW, which enables the implementation of Si-based discrete switching devices. The experimental results demonstrate that the assembled PPC is high efficient (above 99 %). Also, the prototype is thermally validated as the maximum top-case temperature is 72.4 ºC.

7.2 Outlook

Future research on PPC architectures may be related to FCC type and IPOS-ISOP type PPC architectures.

7.2.1 FCC Type Architectures

Chapter 3 ends by suggesting two future research lines related to FCC architectures. On the one hand, it is proposed to research for additional non-isolated topologies that, similar to the MSIBC, improve their performance on PPC architectures. This could include alternative double inductor topologies such us the Cuk converter. On the other hand, the most promising solution should be compared to the conventional HB-FPC and outperform it.

7.2.2 IPOS-ISOP Type Architectures

IPOS-ISOP type architectures seem to be the most promising PPC architectures. However, the next future research lines are proposed to have the big picture:

- Comparison between different isolated topologies. The only isolated topology analyzed and tested trough the work is the DAB. Therefore, it is suggested to compare the performance of different isolated topologies, such as: PSFB, ISFB and resonant converters.
- Short-circuit faults on PPCs. Although IPOS-ISOP type architectures require isolated topologies, they cannot be considered as galvanically isolated. This could suppose a disadvantage against DAB-FPC solutions in case of short-circuit fault. Thus, an analysis of the behavior of IPOS-ISOP type architectures to short-circuit faults is proposed.
- EMI analysis. Due to the reduction of the power processed by the converter, the semiconductors switch with lower voltage and current. In consequence, the EMI emissions are expected to be reduced. An EMI comparison between FPC and PPC solutions could benefit the latter.

-

Appendix A

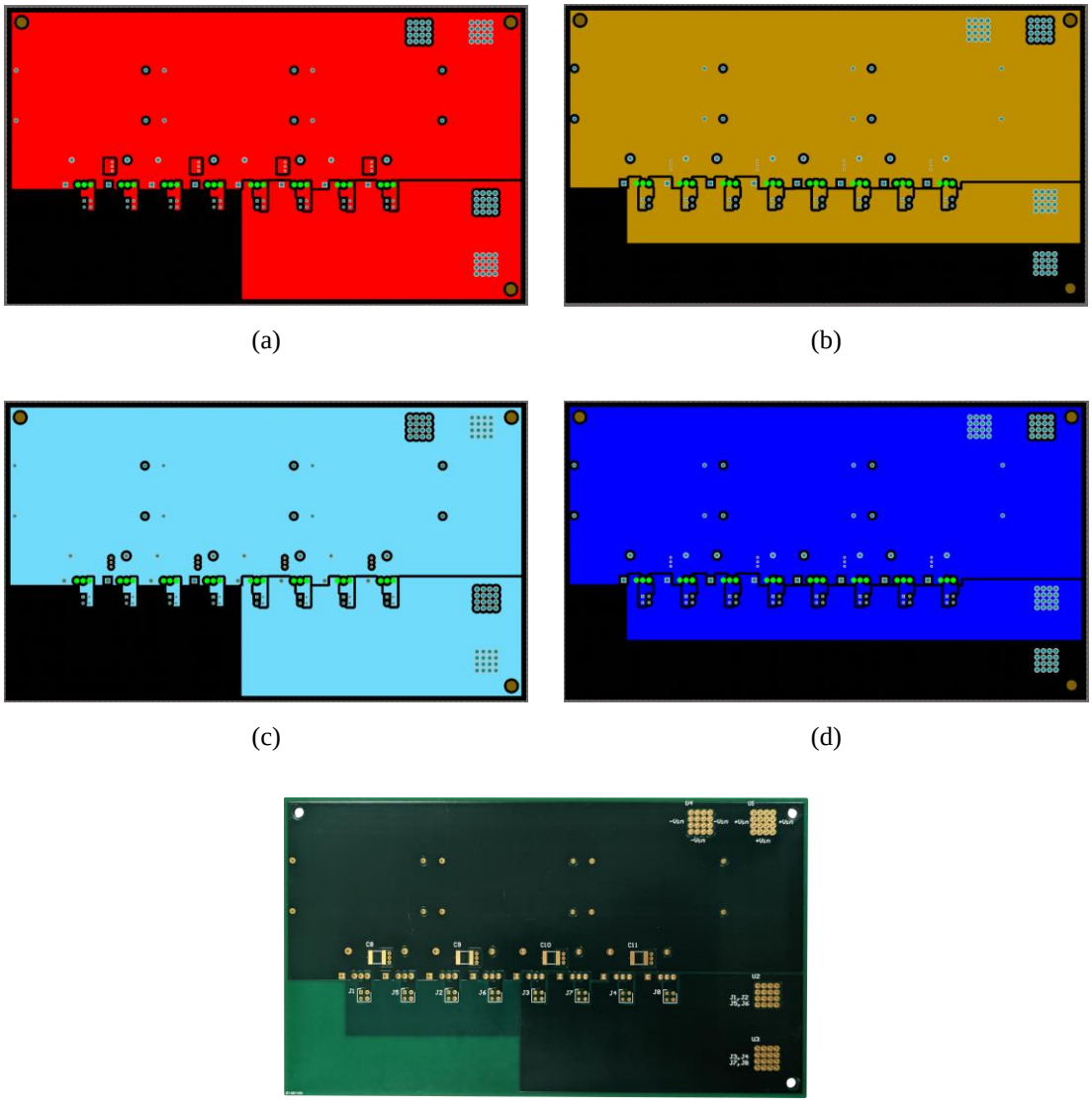
PCB DESIGN OF THE HIGH-POWER PCB

Primary side and secondary side power PCBs

The power stage of the DAB-PPC consists of two full-bridges: primary side (Fig. A.1) and secondary side (Fig. A.2). Both PCBs have 4 layers that can be divided into two groups:

- The top layer and the bottom-middle layer, which have the same shape.
- The bottom layer and the top-middle layer, which have the same shape.

Each PCB contains the DC and AC terminals, the input-output capacitors, the switching devices, and the gate signals connectors.

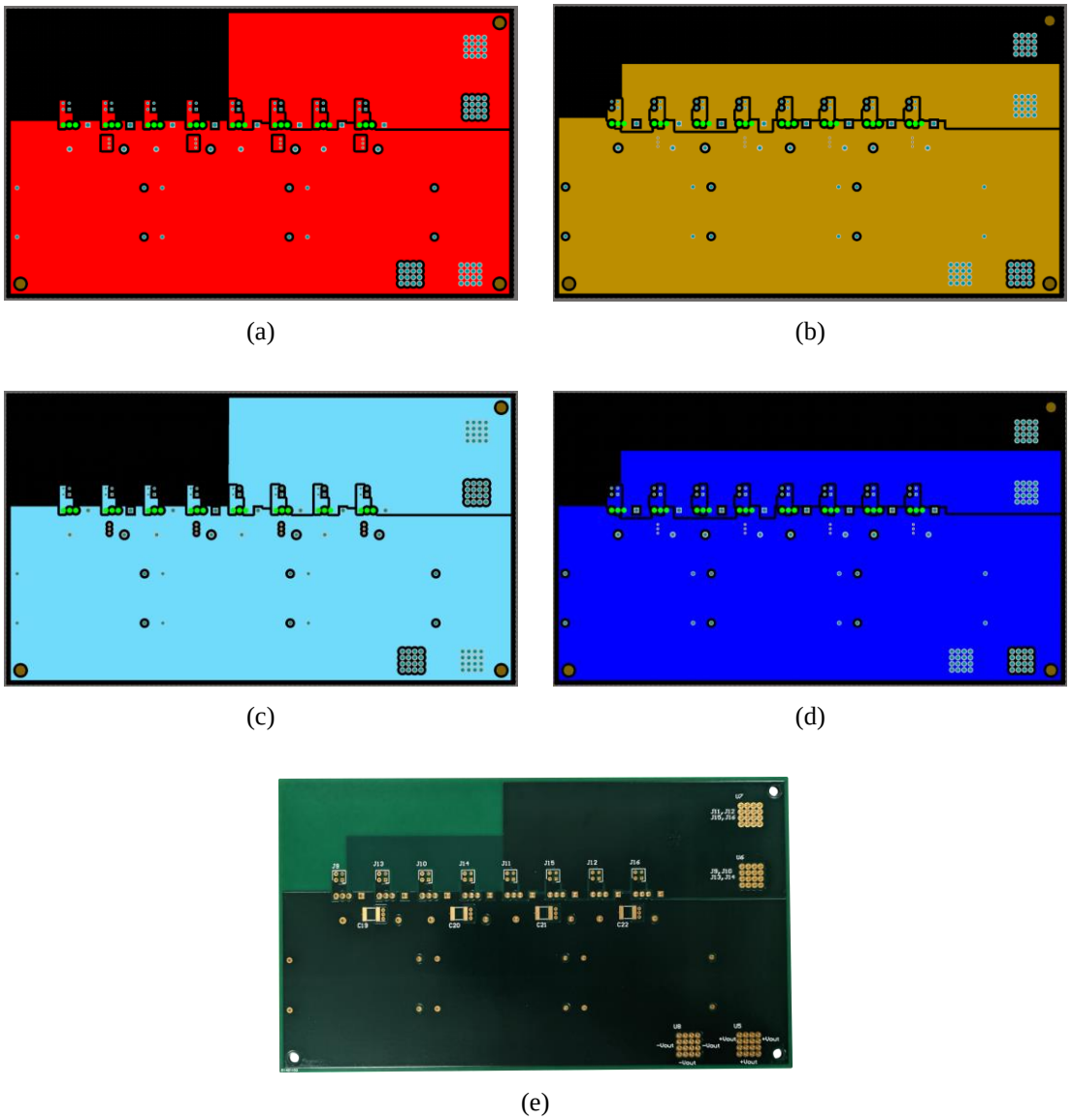


(a) (b)

(c) (d)

(e)

Fig. A.1. PCB layout of the primary side. (a) Top layer. (b) Top-middle layer. (c) Bottom-middle layer. (d) Bottom layer. (e) Image of the primary side PCB.



(a) (b)

(c) (d)

(e)

Fig. A.2. PCB layout of the secondary side. (a) Top layer. (b) Top-middle layer. (c) Bottom-middle layer. (d) Bottom layer. (e) Image of the secondary side PCB.

Driver PCB

Fig. A.3 shows the PCB design of the driver PCB. This PCB adapts the PWM signals to the gate of the switching device. The shame driver PCB design is used for the primary side and the secondary side PCB. Similar to the power PCBs, the design consists of 4 PCB layers.

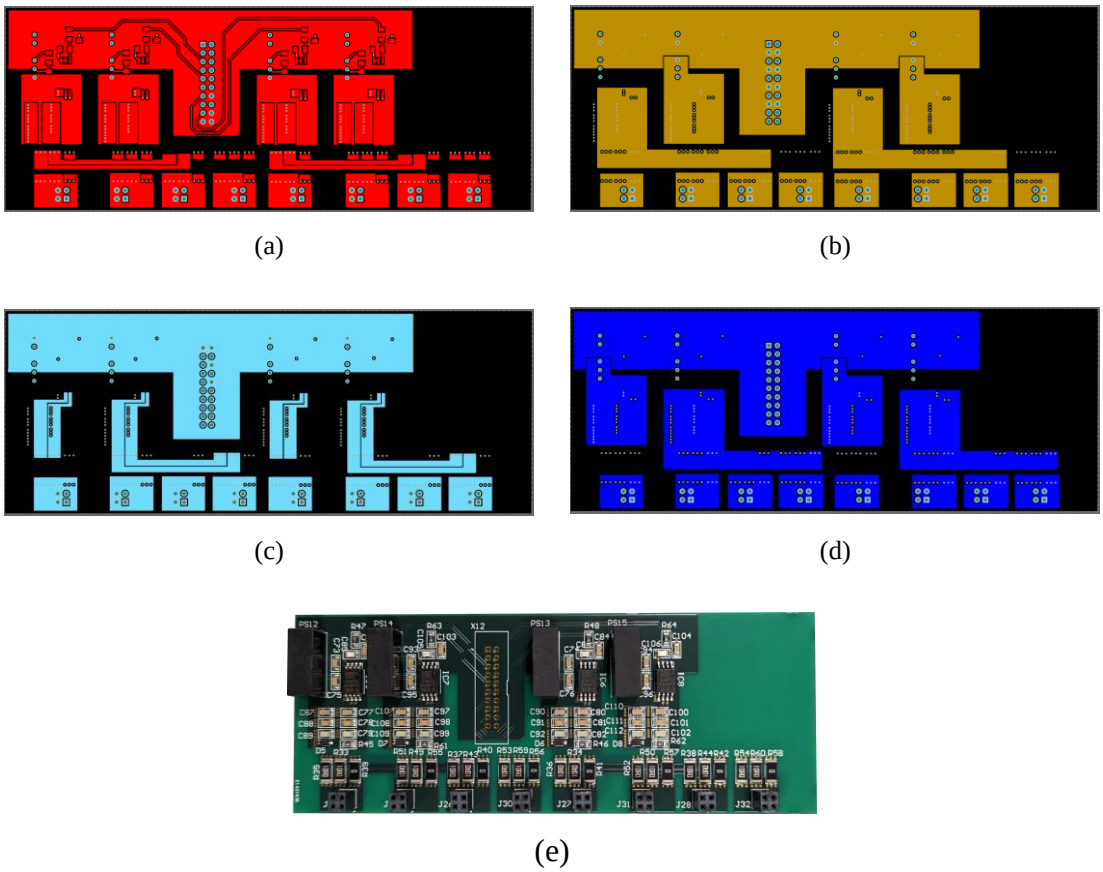
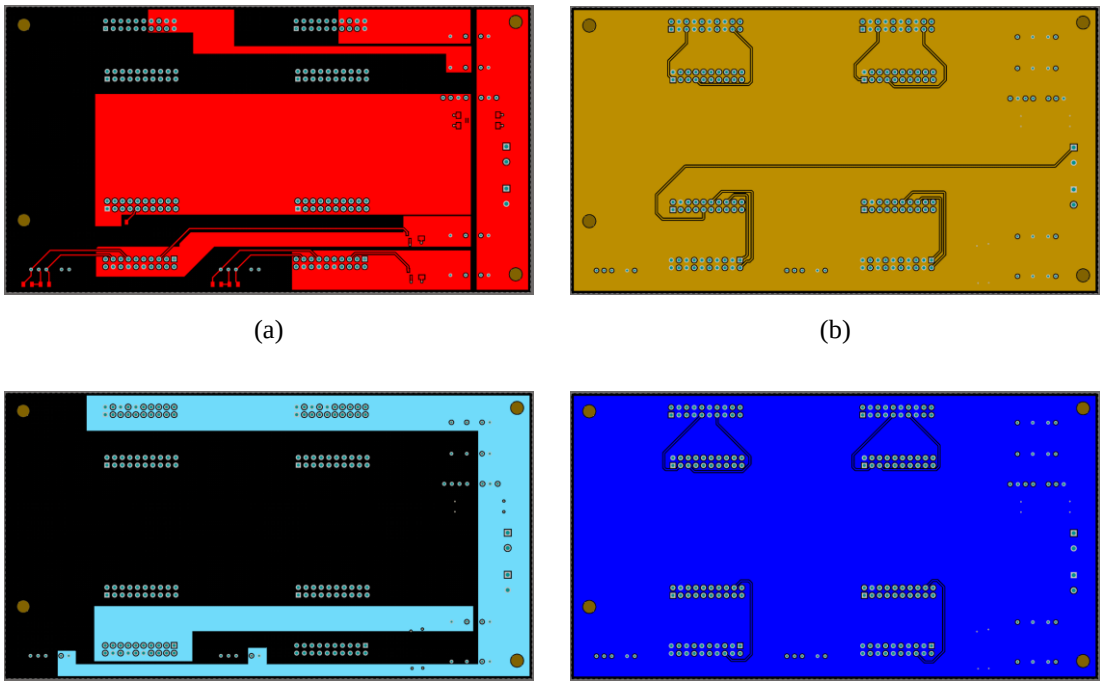


Fig. A.3. PCB layout of the driver. (a) Top layer. (b) Top-middle layer. (c) Bottom-middle layer. (d) Bottom layer. (e) Image of the driver PCB.

Digital signal processor PCB

Fig. A.4 shows the PCB design of the digital signal processor (DSP) PCB. This PCB connects the micro-controller (LAUNCHXL-F28379D) to the rest of the converter.



(a) (b)

(c) (d)

(e)

Fig. A.4. PCB layout of the DSP. (a) Top layer. (b) Top-middle layer. (c) Bottom-middle layer. (d) Bottom layer. (e) Image of the DSP PCB.

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Appendix B

EXPERIMENTAL RESULTS OF THE HIGH POWER PPC

Steady state waveforms

Fig. B.1 shows an image of the transformer primary side current and AC voltages measurement. Then, the voltage and current probes are connected to the oscilloscope to visualize the steady state waveforms. As example, Fig. B.2 shows an oscilloscope screen image at PPC mode and nominal power conditions (at 10 % SOC). Apart from the screen image, the waveform data is extracted in a ".csv" file. This way, the RMS current is computed.

Top-case temperature

Fig. B.3 shows an image of the top-case temperature measurement. As it can be observed, a thermocouple is attached to each switching device. In order to attach the thermocouple, superglue and a Kapton tape is used. Then, a PicoLog 6 data logger is used to acquire all the data in real time. As example, Fig. B.4 shows the temperature evolution of the most heated semiconductors at PPC mode and nominal power conditions.

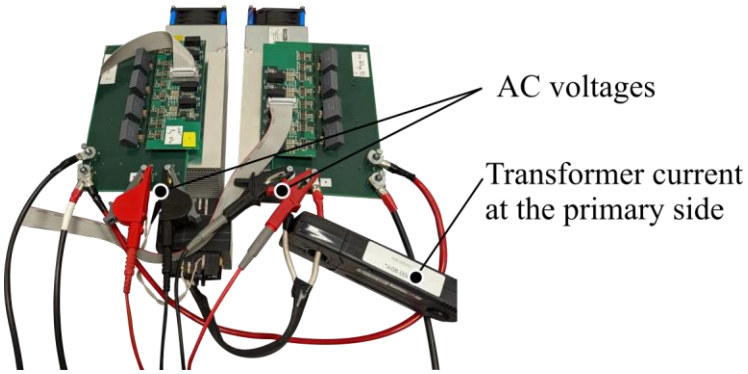

Fig. B.1. Image of the transformer current and AC voltages measurement.

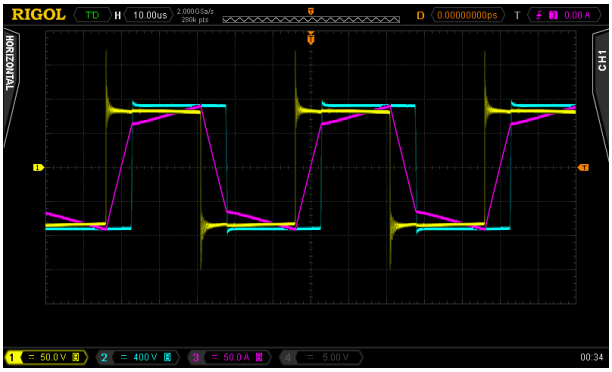

Fig. B.2. Oscilloscope screen image at PPC mode and nominal power conditions (10 % SOC).

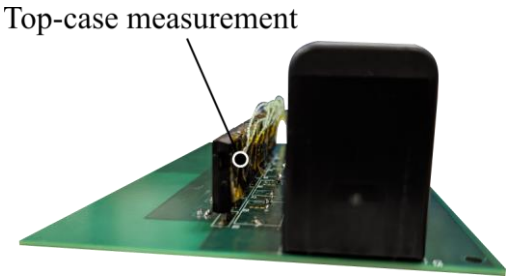

Fig. B.3. Image of the top-case temperature measurement.

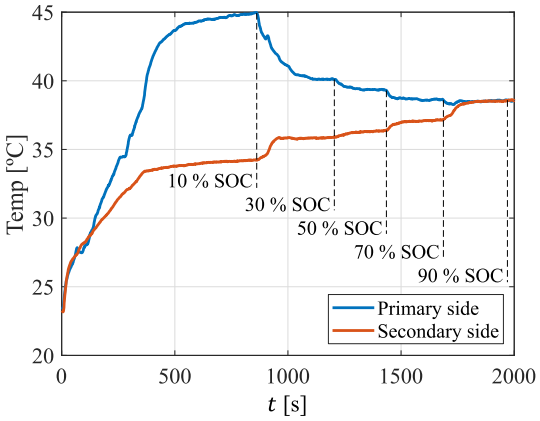

Fig. B.4. Top-case temperature evolution at PPC mode and nominal power conditions.

System efficiency

In order to explain the system efficiency measurement, the PPC mode with nominal power conditions is taken as example. Fig. B.5 shows a simplified electric diagram of the test-bench and Fig. B.6 presents an image of the equipment. The main voltage and currents from Fig. B.5 are:

- V_{source}, I_{source}: they are the voltage and current of the power supply that acts as the source. Both values, together with P_{source}, are shown in the display of the equipment.
- V_{load}, I_{load}: they are the voltage and current of the power supply that acts as the load. Both values, together with P_{load}, are shown in the display of the equipment.
- I_{source_1} is the source current of the converter under test. Since the wattmeter is limited to 40 A, an external current probe is connected to the wattmeter.
- I_{load_1} is the load current of the converter under test. This value is measured by connecting a current probe to the wattmeter.

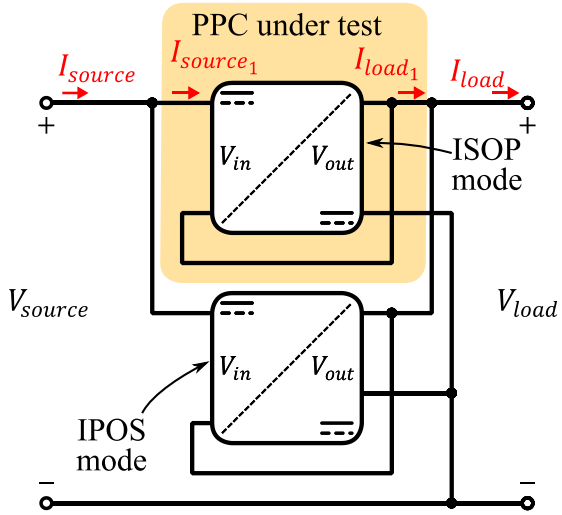

Fig. B.5. Test-bench at PPC mode and nominal conditions.

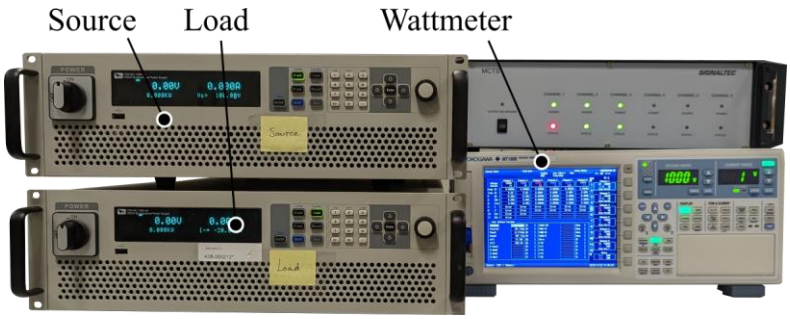

Fig. B.6. Equipment for efficiency measurement.

One way of measuring the power losses is by summing the power given by both power supplies. Due to the power ring configuration from Fig. B.5, the power supplies that act as source and load only observe the power losses of both converters. This value is given by (B.1). Depending on the power transferred by each converter, each power supply must give or absorb power. That is the reason for using bidirectional power supplies.

$$P_{loss} = \frac{P_{source} + P_{load}}{2} \tag{B.1}$$

Another alternative is to compute source power (P_{source_1}) and the load power (P_{load_1}) of the converter under test. This is done by the wattmeter using (B.2)-(B.4).

$$P_{source_1} = V_{source} \cdot I_{source_1} \tag{B.2}$$

-

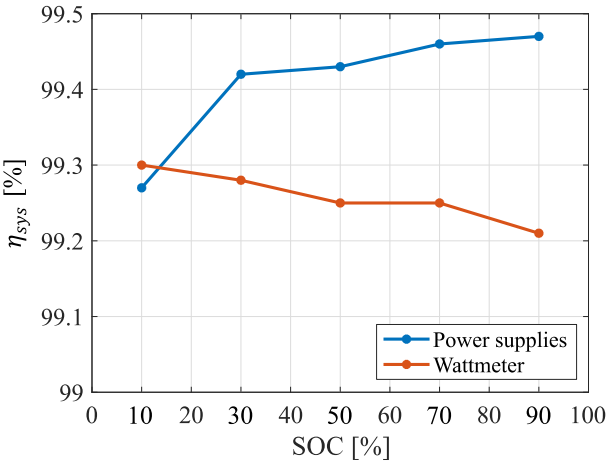

Fig. B.7. Experimental system efficiency comparison at PPC mode and nominal power conditions.

$$P_{load_1} = V_{load} \cdot I_{load_1} \quad \textbf{(B.3)}$$

$$P_{loss} = P_{source_1} - P_{load_1} \quad \textbf{(B.4)}$$

Fig. B.7 compares the system efficiency achieved with the two methods. Both solutions present high efficiency results (above 99 %). However, their curves show a different behaviour. The efficiency obtained with the power supplies increases together with the SOC. On the other hand, the results obtained with the wattmeter decrease. Bearing in mind that the K_{pr} decreases from 10 % SOC to 90 % SOC, it is concluded that the efficiencies obtained with the power supplies are closer to reality. Therefore, the power losses of the high power PPC are defined by the results given by the power supplies.

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