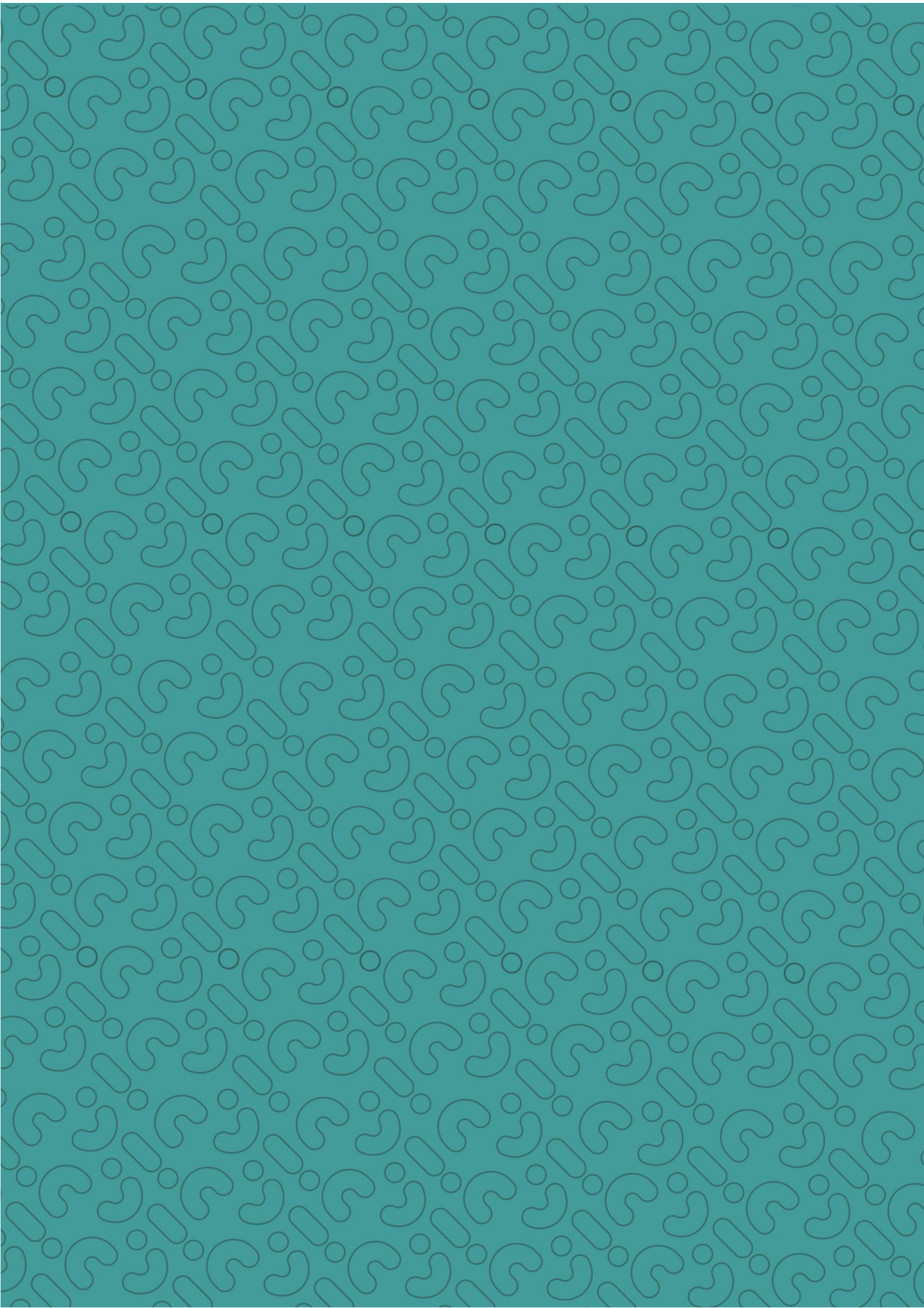


## DOCTORAL THESIS

# Wide Bandgap Technologies for Medium Voltage Applications.

ANTXON ARRIZABALAGA ETXEZARRETA



# Partners



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Thesis directed to obtain the title of DOCTOR  
by MONDRAGON UNIBERTSITATEA

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# Abstract

Renewable energies are experiencing a significant growth in the recent years. Due to their characteristics, power electronics are necessary for their massive integration into the grid. In this context, high power silicon carbide (SiC) modules are identified as possible candidates to improve the features of currently used silicon (Si) insulated gate bipolar transistors (IGBT) in the wind energy, given their improved characteristics. The main goal of this thesis is to analyze their impact in wind energy systems, and to identify the challenges high power SiC modules bring when compared to Si IGBTs.

The levelized cost of energy (LCoE) is the main market competitiveness indicator for the energy sources. This is why a LCoE calculation tool is developed to analyze the theoretical impact of SiC semiconductors in several wind energy systems' power electronics configurations. The results show SiC semiconductors are not able to improve the LCoE of the current configuration because of their high cost, if the semiconductors are replaced one to one. However, if the whole system is optimized, increasing the switching frequency, the SiC semiconductors become competitive. In addition, if their cost is reduced, as expected for the future years, their benefits are increased. The good switching characteristics and the high cost of three level (3L) topologies favour the two level (2L) topology over 3L topologies for the use of SiC semiconductors.

Four laboratory prototypes are built to experimentally verify the LCoE calculation tool results. 2L and 3L topologies are used, with Si and SiC semiconductors. The levelized cost of conversion energy (LCoCE) is used as an indicator to compare the configurations, because the available economical data in the laboratory prototypes is limited. The major conclusions obtained in the theoretical analysis by the LCoE calculation tool are confirmed experimentally.

Finally, the main challenges of the application of high power SiC modules are presented. Several issues that do not affect the designs with slow Si IGBTs need to be considered when using fast switching SiC devices. Issues with the false turn on, the overshoot, the overcurrent protection and the measurements are explained, analyzed and prevention techniques listed. The laboratory prototype is used to validate design techniques to prevent overshoot issues by designing an optimized busbar for the fast switching of SiC modules in 3L converters. The optimization techniques are validated by inductance measurement with an impedance analyzer and switching waveform analysis.

**Keywords:** *Renewable energy, Wind energy, Power electronics, LCoE, High power, SiC, Topologies, Three level, Fast switching, Busbar design.*



# Laburpena

Energia berriztagarriak gorakada nabaria izaten ari dira azken urteetan. Beraien ezaugarriak direla eta, potentzia elektronika beharrezkoa da sarean integrazio masiboa egin ahal izateko. Kontestu honetan, eta beraien ezaugarri tekniko hobeengatik, potentzia altuko silizio karburozko (SiC) moduluak hautagai interesgarriak dira gaur egun erabiltzen diren silizozko (Si) insulated gate bipolar transistors (IGBT-en ingelesez) prestazioak hobetzeko energia eolikoan. Tesi honen helburu nagusia SiC moduluek energia eolikoan duten inpaktua aztertzea da, beraien integrazioak dakartzan erronka nagusiekin.

Energiaren kostu normalizatua (LCoE ingelesez) da energia iturrien lehiakortasuna neurtzen duen adierazle nagusia. Horregatik, LCoE-a kalkulatzeko duen erreminta garatu da, SiC moduluek energia eolikoan erabiltzen diren potentzia elektronika konfigurazio ezberdinetan eduki dezaketen inpaktu teorikoa aztertzeko. Emaitzek, beraien kostu altuagatik SiC erdieroaleak gaur egungo LCoE-a hobetzeko gai ez direla erakusten dute, banan-banako aldaketa egin ezker. Sistema guztia optimizatu ezker ordea, konmutazio frekuentzia handituz, SiC erdieroaleak lehiakorak izan daitezke. Hurrengo urteetan beraien kostua espero den bezala murriztuko balitz gainera, are eta interesgarriagoak lirateke. SiC-aren kostu altua eta konmutazio ezaugarri onak direla eta, 2 tentsio mailako (2L) topologiak hiru mailakoak (3L) baino egokiagoak dira SiC erdieroaleak erabiltzeko.

Lau laborategiko prototipo eraiki dira esperimentalki LCoE kalkulu erremintak emandako emaitzak frogatzeko. 2 eta 3 mailako topologiak erabili dira, baita Si eta SiC erdieroaleak ere. Energiaren bihurteta kostu normalizatua (LCoE ingelesez) erabili da konfigurazioen arteko konparaketa egiteko adierazle bezala, laborategiko prototipoen datu ekonomikoak mugatuak direlako. LCoE kalkulu erremintan lorturiko ondorio nagusiak berretsi dira esperimentalki.

Azkenik, potentzia altuko SiC moduluen aplikazioak dakartzan erronka nagusiak aurkezten dira. Si IGBT motelekin eraginik ez duten fenomeno batzuk kontuz aztertu behar dira SiC erdieroale azkarrak erabiltzean. Pizketa faltsuekin, gaintentsioarekin, gainkorronte babesarekin edo neurketekin izan daitezkeen arazoak azaldu, aztertu eta prebentzio neurriak zerrendatzen dira. Laborategi prototipoa erabiltzen da gaintentsioa konpontzeko aurkezten diren diseinu teknikak balioztatzeko, 3L bihurtailuetan SiC erdieroaleen konmutazio azkarrarekin. Optimizazio teknikak inдукtantzia neurketekin eta konmutazio seinaleen azterketarekin balioztatu dira.

**Hitz klabeak:** *Energia berriztagarria, Energia eolikoa, Potentzia elektronika, LCoE, Potentzia altua, SiC, Topologiak, Hiru maila, Konmutazio azkarra, Busbar diseinua.*

# Resumen

Las energías renovables están experimentando un gran incremento en los últimos años. Debido a sus singularidades, la electrónica de potencia es necesaria para su integración masiva en la red. En este contexto, los módulos de alta potencia de carburo de silicio (SiC) se identifican como posibles candidatos para mejorar las características de los semiconductores insulated gate bipolar transistor (IGBT) de silicio (Si) que se utilizan actualmente en la energía eólica, dadas sus mejores propiedades. El objetivo principal de esta tesis es analizar el impacto de los semiconductores de SiC en la energía eólica, e identificar los principales retos que conlleva su uso en comparación con los módulos de Si. El coste normalizado de la energía (LCoE en inglés) es el indicador principal para evaluar las fuentes de energía. Por ello se ha desarrollado una herramienta de cálculo de LCoE, para analizar el impacto teórico de los semiconductores de SiC en diferentes configuraciones de electrónica de potencia en la energía eólica. Los resultados muestran que los semiconductores de SiC no pueden mejorar el LCoE del sistema actual debido a su alto coste, si se reemplazan los semiconductores uno a uno. En cambio, si se optimiza el sistema completo, aumentando la frecuencia de conmutación, los módulos de SiC pasan a ser competitivos. Además, si como se prevé, el precio del SiC se reduce en los próximos años, sus beneficios serían todavía mayores. Por alto coste del SiC, y sus buenas características de conmutación, la topología de dos niveles (2L) obtiene mayores beneficios que la de tres niveles (3L) con el uso del SiC.

Se han fabricado cuatro prototipos de laboratorio para verificar experimentalmente los resultados de la herramienta de cálculo de LCoE. Se han utilizado las topologías de 2 y 3 niveles, y los semiconductores de Si y de SiC. Se ha utilizado el coste normalizado de la conversión de la energía (LCoCE en inglés) como indicador para comparar las configuraciones, dado que los datos económicos de los prototipos de laboratorio son limitados. Las conclusiones principales de la herramienta de cálculo de LCoE son confirmadas experimentalmente.

Finalmente se presentan los principales retos que conlleva utilizar los módulos de SiC en alta potencia. Fenómenos que apenas son relevantes con los lentos módulos de Si pasan a ser de vital importancia con los rápidos semiconductores de SiC. Se explican, analizan y enumeran técnicas preventivas para el falso encendido, la sobretensión, la protección de sobrecorriente y los sistemas de medidas. Se utiliza el prototipo de laboratorio para validar las técnicas de diseño para prevenir la sobretensión, diseñando un busbar optimizado para su uso con conmutaciones rápidas de módulos de SiC en convertidores de tres niveles. Las técnicas de optimización se verifican mediante medidas de inductancia con un analizador de impedancias y el análisis de las formas de onda de la conmutación.

**Palabras clave:** *Energía renovable, Energía eólica, Electrónica de potencia, LCoE, Alta potencia, SiC, Topologías, Tres niveles, Conmutación rápida, Diseño de busbar.*

# INDEX

	II
Partners	I
Copyright	II
Statement of originality	III
Acknowledgments	IV
Abstract	VI
Laburpena	VII
Resumen	VIII
LIST OF FIGURES	XIV
LIST OF TABLES	XIX
GLOSSARY	XXI
1. Introduction	2
1.1. Background	2
1.2. Renewable energies	2
1.2.1. Renewable energies worldwide	3
1.2.2. Renewable energies economy	5
1.2.3. Levelized cost of energy	6
1.3. Wind energy	7
1.3.1. Wind energy configurations	8
1.3.2. Power electronics of wind energy	10
1.3.3. Levelized cost of energy for wind energy	13
1.4. Silicon carbide semiconductors	14
1.4.1. Physical characteristics of silicon carbide	14
1.4.2. High power silicon carbide semiconductors	17
1.4.3. High power silicon carbide applications	22
1.5. Objectives	30
1.6. Outline of the thesis	30
1.7. Scientific contributions	31
1.8. Publications	31
1.8.1. Conference papers	31
2. LCoE calculation tool	34
2.1. Objective and approach	34

2.1.1.	Objective	34
2.1.2.	Approach	34
2.2.	LCoE calculation equation	34
2.3.	Calculation algorithm	35
2.3.1.	Input parameters	36
2.3.2.	Algorithm models	42
2.3.3.	Cost function	48
2.3.4.	AEP function	51
2.3.5.	LCoE function	51
2.4.	Tool optimization	52
2.4.1.	Computational cost	52
2.4.2.	Vectorization	52
2.5.	Results	52
2.5.1.	Baseline	52
2.5.2.	Current cost	52
2.5.3.	Future scenario	55
2.5.4.	Commercial indicators	57
2.5.5.	Business case selection	58
3.	Hardware implementation	60
3.1.	Test bench objectives and approach	60
3.1.1.	Objective of the test bench	60
3.1.2.	Approach	60
3.2.	Component selection	61
3.2.1.	Modules	62
3.2.2.	Drivers	63
3.2.3.	Capacitors	63
3.2.4.	Cooling systems	65
3.2.5.	DC-link discharge resistors	67
3.2.6.	Sensors	68
3.2.7.	Control board	69
3.3.	Optimal busbar design for 3 level busbar converters	72
3.3.1.	Switching loop evaluation	74
3.3.2.	Busbar design	77
3.3.3.	Design evaluation by impedance analyzer	80
3.3.4.	Design evaluation by switching	85
3.4.	2 level busbar design	91
3.4.1.	Switching loop evaluation	91

3.4.2.	Module placement	92
3.4.3.	Capacitor placement	93
3.4.4.	Busbar assembly	94
3.5.	Hardware validation	94
3.5.1.	3L converter switching validation	95
3.5.2.	2L converter switching validation	96
3.5.3.	3L continuous test	97
3.5.4.	2L continuous test	98
3.6.	Conclusion	99
4.	Experimental testing of the business case	102
4.1.	Conditions of the analysis	102
4.1.1.	Efficiency test conditions	102
4.1.2.	Theoretical converter optimization	103
4.1.3.	LCoCE calculation method	108
4.2.	2 level with Si, baseline configuration	109
4.2.1.	Efficiency tests	109
4.2.2.	Converter optimization	111
4.2.3.	System cost	111
4.2.4.	LCoCE	112
4.3.	2 level with SiC	113
4.3.1.	Efficiency tests	113
4.3.2.	Converter optimization	114
4.3.3.	System cost	114
4.3.4.	LCoCE	115
4.4.	3 level with Si	116
4.4.1.	Efficiency tests	116
4.4.2.	Converter optimization	117
4.4.3.	System cost	118
4.4.4.	LCoCE	118
4.5.	3 level with SiC	119
4.5.1.	Efficiency tests	119
4.5.2.	Converter optimization	120
4.5.3.	System cost	121
4.5.4.	LCoCE	122
4.6.	Configuration comparison	122
4.6.1.	Efficiency	122
4.6.2.	System cost	122

4.6.3.	LCoCE	123
4.6.4.	Future scenario	123
4.6.5.	Conclusion	124
4.7.	Verification of the LCoE calculation tool results	124
4.7.1.	Methodology	124
4.7.2.	Configurations by the LCoE calculation tool	125
4.7.3.	Laboratory prototypes	126
4.7.4.	Analysis	127
5.	Challenges of silicon carbide in high power applications	130
5.1.	False turn on	130
5.1.1.	Phenomenon	130
5.1.2.	Analytical modelling	131
5.1.3.	Critical variable identification	132
5.1.4.	Comparison with silicon	133
5.1.5.	Prevention techniques	133
5.2.	Overshoot	134
5.2.1.	Phenomenon	134
5.2.2.	Analytical modelling	134
5.2.3.	Critical variable identification	134
5.2.4.	Comparison with silicon	135
5.2.5.	Prevention techniques	136
5.2.6.	Experimental verification	136
5.3.	Overcurrent protection	137
5.3.1.	Desat sensing	137
5.3.2.	False Desat triggering	137
5.3.3.	Comparison with silicon	138
5.3.4.	Considerations and recommendations	139
5.4.	Measurements	139
5.4.1.	Equipment selection	139
5.4.2.	Hardware set up	143
5.4.3.	Voltage and current alignment	147
5.4.4.	Alternative measurement techniques	148
5.5.	Conclusion	149
6.	Conclusion and future work	153
6.1.	Conclusion	153
6.2.	Future research lines	155



# List of figures

FIGURE 1. 1. ....	3
WORLDWIDE ENERGY CONSUMPTION EVOLUTION IN DIFFERENT GEOGRAPHICAL REGIONS.	
FIGURE 1. 2. ....	4
WORLDWIDE RENEWABLE ENERGY SHARE FOR 2018 AND 2019 IN DIFFERENT GEOGRAPHICAL REGIONS.	
FIGURE 1. 3. ....	5
GENERATED ENERGY BY SOURCE AND YEAR.	
FIGURE 1. 4. ....	6
EVOLUTION OF THE WORLDWIDE INVESTMENT IN SOLAR PV AND WIND ENERGY.	
FIGURE 1. 5. ....	6
EVOLUTION OF THE COST OF SOLAR PV MODULES AND WIND ENERGY PROJECTS.	
FIGURE 1. 6. ....	7
LCoE EVOLUTION OF SOLAR PV, WIND ENERGY AND COAL.	
FIGURE 1. 7. ....	8
ANNUAL GROWTH FOR RENEWABLE ELECTRICITY GENERATION BY SOURCE, 2018-2020.	
FIGURE 1. 8. ....	9
VARIABLE SPEED WIND TURBINE SYSTEM, DFIG CONFIGURATION.	
FIGURE 1. 9. ....	10
VARIABLE SPEED WIND TURBINE SYSTEM, FULL CONVERTER CONFIGURATION.	
FIGURE 1. 10. ....	11
2 LEVEL BTB TOPOLOGY.	
FIGURE 1. 11. ....	12
MULTI CELL 2 LEVEL BTB TOPOLOGY.	
FIGURE 1. 12. ....	13
3 LEVEL ANPC BTB TOPOLOGY.	
FIGURE 1. 13. ....	13
3 LEVEL ANPC BTB TOPOLOGY.	
FIGURE 1. 14. ....	14
HIGH POWER APPLICATIONS FOR SiC.	
FIGURE 1. 15. ....	15
KEY PHYSICAL CHARACTERISTICS OF SILICON CARBIDE AND GALLIUM NITRIDE, NORMALIZED TO SILICON.	
FIGURE 1. 16. ....	16
SILICON AND SILICON CARBIDE DRIFT LAYER THICKNESS COMPARISON FOR THE SAME BLOCKING VOLTAGE.	
FIGURE 1. 17. ....	16
SILICON AND SILICON CARBIDE SPECIFIC ON RESISTANCE COMPARISON FOR DIFFERENT BREAKDOWN VOLTAGES.	
FIGURE 1. 18. ....	18
Si AND SiC HIGH POWER MODULES FORWARD CHARACTERISTICS COMPARISON.	
FIGURE 1. 19. ....	19
Si AND SiC HIGH POWER MODULES SWITCHING CHARACTERISTICS COMPARISON.	
FIGURE 1. 20. ....	20
COMMERCIAL SiC MOSFET HALF BRIDGE MODULES, IN PRODUCTION (DOTS) AND UNDER DEVELOPMENT (TRIANGLES).	
FIGURE 1. 21. ....	23
SST CONFIGURATION.	
FIGURE 1. 22. ....	24
ELECTRIC DRIVE SYSTEMS' MAIN COMPONENTS.	
FIGURE 1. 23. ....	26
RAILWAY ELECTRIC SYSTEMS' MAIN COMPONENTS.	
FIGURE 1. 24. ....	28
POWER CONSUMPTION RATE OF HOME APPLIANCES.	
FIGURE 1. 25. ....	29
AEP GAIN DEPENDING ON THE ANNUAL AVERAGE WIND SPEED OF THE LOCATION FOR SiC TECHNOLOGY.	
FIGURE 1. 26. ....	29
AEP GAIN PERCENTAGE DEPENDING ON THE AVERAGE ANNUAL WIND SPEED OF THE LOCATION FOR SiC, USING AS REFERENCE THE CURRENTLY USED Si IGBTs.	
FIGURE 2. 1. ....	35
LCoE CALCULATION ALGORITHM.	
FIGURE 2. 2. ....	37
2L TOPOLOGY, (A) PHASE BRANCH DIAGRAM, (B) GATE ORDERS ( $G_{T1}, G_{T2}$ ) AND PHASE VOLTAGE ( $V_{PH-O}$ ) WAVEFORMS.	
FIGURE 2. 3. ....	38



3L NPC TOPOLOGY, (A) DIAGRAM, (B) WAVEFORMS.	
FIGURE 2. 4. ....	39
3L ANPC TOPOLOGY, (A) DIAGRAM, (B) WAVEFORMS.	
FIGURE 2. 5. ....	40
3L NPP TOPOLOGY, (A) DIAGRAM, (B) WAVEFORMS.	
FIGURE 2. 6. ....	43
MODELED FORWARD CHARACTERISTICS OF THE BASELINE SEMICONDUCTOR.	
FIGURE 2. 7. ....	44
MODELED SWITCHING CHARACTERISTICS OF THE BASELINE SEMICONDUCTOR.	
FIGURE 2. 8. ....	53
POWER OF THE CONFIGURATIONS IMPROVING THE LCoE OF THE BASELINE WITH THE CURRENT COST OF THE SEMICONDUCTORS.	
FIGURE 2. 9. ....	53
VOLTAGE OF THE CONFIGURATIONS IMPROVING THE LCoE OF THE BASELINE WITH THE CURRENT COST OF THE SEMICONDUCTORS.	
FIGURE 2. 10. ....	54
TOPOLOGY OF THE CONFIGURATIONS IMPROVING THE LCoE OF THE BASELINE WITH THE CURRENT COST OF THE SEMICONDUCTORS.	
FIGURE 2. 11. ....	54
SEMICONDUCTORS OF THE CONFIGURATIONS IMPROVING THE LCoE OF THE BASELINE WITH THE CURRENT COST OF THE SEMICONDUCTORS.	
FIGURE 2. 12. ....	55
TOPOLOGIES OF THE CONFIGURATIONS WITH SiC SEMICONDUCTORS IMPROVING THE LCoE OF THE BASELINE, WITH HALF OF THE CURRENT COST OF THE SiC SEMICONDUCTORS.	
FIGURE 2. 13. ....	56
SEMICONDUCTOR VOLTAGE LEVELS OF THE CONFIGURATIONS WITH SiC IMPROVING THE LCoE OF THE BASELINE, WITH HALF OF THE CURRENT COST OF THE SiC SEMICONDUCTORS.	
FIGURE 2. 14. ....	56
LCoE DIFFERENCE FOR THE MOST INTERESTING CONFIGURATIONS, CONSIDERING COST REDUCTION IN SiC SEMICONDUCTORS AND THE EFFECT OF SWITCHING FREQUENCY.	
FIGURE 3. 1. ....	61
DESIGNED TEST BENCH CONFIGURATION WITH REGENERATIVE DC LINK REGULATOR AND REPLACEABLE MODULES, (A) 3 LEVEL CONVERTER, (B) 2 LEVEL CONVERTER AND (C) GENERAL DIAGRAM WITH THE MAIN MEASURED POWER VARIABLES.	
FIGURE 3. 2. ....	63
AGILESWITCH 2ASC-12A1HP/17A1HP DRIVER WITH THE ADAPTER BOARD FOR 62 MM MODULES.	
FIGURE 3. 3. ....	66
EFFECTIVE COOLING AREA OCCUPATION REPRESENTATION DIAGRAM FOR, (A) TWO LEVEL CONVERTER AND (B) THREE LEVEL CONVERTER.	
FIGURE 3. 4. ....	67
SELECTED COOLING SYSTEMS FOR, (A) TWO LEVEL CONVERTER AND (B) THREE LEVEL CONVERTER.	
FIGURE 3. 5. ....	71
POWER MODULES DRIVING SCHEME.	
FIGURE 3. 6. ....	72
DESIGNED CONTROL BOARD.	
FIGURE 3. 7. ....	73
SIMULATED TURN OFF VOLTAGE COMPARING DIFFERENT POWER LOOP INDUCTANCES.	
FIGURE 3. 8. ....	74
HIGH POWER SiC MODULES PACKAGES DETAILED PINOUT COMPARISON, (A) HT-3000 SERIES, (B) 62 MM.	
FIGURE 3. 9. ....	75
SINGLE-PHASE 3L ANPC, (A) TOPOLOGY WITH LOW SIDE SWITCHING LOOPS, (B) MODULATION AND PHASE VOLTAGE.	
FIGURE 3. 10. ....	76
TWO-LAYER BUSBAR STRUCTURE WITH OPPOSITE CURRENTS.	
FIGURE 3. 11. ....	76
NORMALIZED INDUCTANCE DEPENDING ON THE ANGLE BETWEEN CURRENTS $\phi$ .	
FIGURE 3. 12. ....	77
3-LEVEL ANPC PHASE LEG FORMATION OPTIONS CONSIDERING PARASITIC INDUCTANCES, (A) NON-OPTIMIZED PHASE LEG, (B) OPTIMIZED PHASE LEG.	
FIGURE 3. 13. ....	78
62 MM MODULE PLACEMENT OPTIONS CONSIDERING CURRENT PATHS IN BUSBAR LAYERS, (A) VERTICAL PLACEMENT, (B) ROTATED MODULE PLACEMENT, (C) ROTATED AND SHIFTED MODULE.	

FIGURE 3. 14. ....	79
CAPACITOR PLACEMENT OPTIONS, (A) SINGLE CAPACITOR, (B) PARALLEL CAPACITORS, (C) OPTIMIZED PARALLEL CAPACITORS.	
FIGURE 3. 15. ....	80
NEUTRAL LAYER DESIGN OPTIONS WITH THE EXPECTED CURRENT PATHS OF THE LOW LONG SWITCHING LOOP, (A) NON-OPTIMIZED NEUTRAL LAYER, (B) OPTIMIZED NEUTRAL LAYER	
FIGURE 3. 16. ....	81
MANUFACTURED BUSBAR WITH ITS LAYERS, (A) TOP VIEW, (B) BOTTOM VIEW.	
FIGURE 3. 17. ....	82
BUSBAR IMPEDANCE TESTING, (A) HIGH SIDE SHORT LOOP, (B) LOW SIDE LONG LOOP.	
FIGURE 3. 18. ....	83
SINGLE CAPACITOR PARASITIC INDUCTANCE MEASUREMENT.	
FIGURE 3. 19. ....	84
NON-OPTIMIZED NEUTRAL LAYER INDUCTANCE MEASUREMENT WITH BYPASS CABLE.	
FIGURE 3. 20. ....	86
DOUBLE PULSE TEST DIAGRAM, (A) THE SETUP, (B) WAVEFORMS OF THE DIFFERENT ELEMENTS.	
FIGURE 3. 21. ....	87
PHYSICAL CONFIGURATION OF THE CURRENT MEASUREMENT ON 62 MM MODULES.	
FIGURE 3. 22. ....	87
DATA ACQUISITION FROM THE TURN OFF WAVEFORM IN A DPT TO CALCULATE THE LOOP INDUCTANCE.	
FIGURE 3. 23. ....	88
THE TURN OFF OF THE SHORT LOOP FOR DIFFERENT CURRENTS.	
FIGURE 3. 24. ....	89
THE TURN OFF OF THE LONG LOOP FOR DIFFERENT CURRENTS.	
FIGURE 3. 25. ....	90
THE TURN OFF OF THE SHORT LOOP WITH THE OPTIMIZED CAPACITORS, AND THE SINGLE CAPACITOR FOR DIFFERENT CURRENTS.	
FIGURE 3. 26. ....	92
2 LEVEL CONVERTERS SWITCHING LOOPS.	
FIGURE 3. 27. ....	92
2 LEVEL CONVERTER MODULE PLACEMENT.	
FIGURE 3. 28. ....	93
CAPACITOR PLACEMENT IN THE 2L CONVERTER.	
FIGURE 3. 29. ....	94
2L CONVERTER RECEPTION, (A) THE BUSBAR WITH THE CAPACITORS AND (B) THE 62 MM MODULES READY TO ASSEMBLE.	
FIGURE 3. 30. ....	95
2L CONVERTER PROTOTYPE.	
FIGURE 3. 31. ....	95
3L CONVERTER PROTOTYPE.	
FIGURE 3. 32. ....	96
MEASURED TURN OFF TRANSIENT $V_{DS}$ WAVEFORM UNDER 750 V DC VOLTAGE IN THE TWO LEVEL CONVERTER FOR DIFFERENT CURRENTS.	
FIGURE 3. 33. ....	98
3L CONVERTER CONTINUOUS TEST AT MAXIMUM POWER, A) AT 2.5 KHZ AND B) AT 10 KHZ SWITCHING FREQUENCY.	
FIGURE 3. 34. ....	98
MEASURED VOLTAGE UNBALANCE PER UNIT, DEPENDING ON THE FUNDAMENTAL FREQUENCY AND SWITCHING FREQUENCY RATIO.	
FIGURE 3. 35. ....	99
2L CONVERTER CONTINUOUS TEST AT MAXIMUM POWER, A) AT 2.5 KHZ AND B) AT 10 KHZ SWITCHING FREQUENCY.	
FIGURE 4. 1. ....	104
COOLING SYSTEM MODELS, (A) FOR THE 2L CONVERTER AND (B) FOR THE 3L CONVERTER.	
FIGURE 4. 2. ....	105
COST OF COMMERCIAL COOLING SYSTEMS DEPENDING ON THEIR THERMAL RESISTANCE.	
FIGURE 4. 3. ....	106
REQUIRED VOLUME OF THE THREE INDUCTORS, DEPENDING ON THE SWITCHING FREQUENCY AND CONVERTER LEVEL.	
FIGURE 4. 4. ....	106
COST OF SINGLE COMMERCIAL INDUCTORS DEPENDING ON THEIR VOLUME.	
FIGURE 4. 5. ....	107
COST OF SINGLE COMMERCIAL CAPACITORS DEPENDING ON THE CAPACITANCE.	
FIGURE 4. 6. ....	107
COST OF THE OUTPUT FILTER DEPENDING ON THE SWITCHING FREQUENCY AND CONVERTER TOPOLOGY.	

FIGURE 4. 7. ....	109
WEIBULL WIND SPEED DISTRIBUTIONS USED FOR AEP CALCULATIONS.	
FIGURE 4. 8. ....	110
EFFICIENCY TESTS OF THE BASELINE (2L Si) CONFIGURATION, (A) FOR DIFFERENT OUTPUT POWERS AT 2.5 KHz SWITCHING FREQUENCY AND (B) FOR DIFFERENT SWITCHING FREQUENCIES AT MAXIMUM OUTPUT POWER.	
FIGURE 4. 9. ....	110
EFFICIENCY TESTS OF THE BASELINE CONFIGURATION FOR DIFFERENT OUTPUT POWERS AND SWITCHING FREQUENCIES.	
FIGURE 4. 10. ....	113
EFFICIENCY TESTS OF THE 2L WITH SiC CONFIGURATION, (A) FOR DIFFERENT OUTPUT POWERS AT 2.5 KHz SWITCHING FREQUENCY AND (B) FOR DIFFERENT SWITCHING FREQUENCIES AT MAXIMUM OUTPUT POWER.	
FIGURE 4. 11. ....	114
EFFICIENCY TESTS OF THE 2L CONFIGURATION WITH SiC FOR DIFFERENT OUTPUT POWERS AND SWITCHING FREQUENCIES.	
FIGURE 4. 12. ....	116
EFFICIENCY TESTS OF THE 3L WITH Si CONFIGURATION, (A) FOR DIFFERENT OUTPUT POWERS AT 2.5 KHz SWITCHING FREQUENCY AND (B) FOR DIFFERENT SWITCHING FREQUENCIES AT MAXIMUM OUTPUT POWER.	
FIGURE 4. 13. ....	117
EFFICIENCY TESTS OF THE 3L CONFIGURATION WITH Si FOR DIFFERENT OUTPUT POWERS AND SWITCHING FREQUENCIES.	
FIGURE 4. 14. ....	119
EFFICIENCY TESTS OF THE 3L WITH SiC CONFIGURATION, (A) FOR DIFFERENT OUTPUT POWERS AT 2.5 KHz SWITCHING FREQUENCY AND (B) FOR DIFFERENT SWITCHING FREQUENCIES AT MAXIMUM OUTPUT POWER.	
FIGURE 4. 15. ....	120
EFFICIENCY TESTS OF THE 3L CONFIGURATION WITH SiC FOR DIFFERENT OUTPUT POWERS AND SWITCHING FREQUENCIES.	
FIGURE 4. 16. ....	123
THE EVOLUTION OF THE LCoCE DIFFERENCE DEPENDING ON THE COST OF THE SiC.	
FIGURE 4. 17. ....	126
LCoCE DIFFERENCE RESPECT TO THE BASELINE OF THE CONFIGURATIONS FROM THE LCoE CALCULATION TOOL, FOR DIFFERENT COSTS OF THE SiC SEMICONDUCTORS.	
FIGURE 4. 18. ....	127
LCoCE DIFFERENCE RESPECT TO THE BASELINE OF THE LABORATORY PROTOTYPES, FOR DIFFERENT COSTS OF THE SiC SEMICONDUCTORS.	
FIGURE 5. 1. ....	131
CIRCUIT SCHEMATIC USED TO EXPLAIN THE FALSE TURN ON PHENOMENON, WITH THE CONSIDERED PARASITICS AND PARAMETERS.	
FIGURE 5. 2. ....	137
DESAT DETECTION CIRCUIT.	
FIGURE 5. 3. ....	138
DESAT DETECTION CIRCUIT UNDER A TURN OFF OF THE SiC MOSFET, WITH THE DISPLACEMENT CURRENT THROUGH THE JUNCTION CAPACITANCE.	
FIGURE 5. 4. ....	143
PERTURBATION IN THE MEASURED CIRCUIT DUE TO THE INTRODUCTION OF (A) VOLTAGE AND (B) CURRENT PROBES.	
FIGURE 5. 5. ....	144
DISTORTION OF THE ORIGINAL SIGNAL DUE TO THE MEASUREMENT SYSTEM.	
FIGURE 5. 6. ....	144
SIMULATED EFFECT OF THE INPUT CAPACITANCE OF THE VOLTAGE PROBE WHEN MEASURING THE V <sub>DS</sub> OF A FF6MR12KM1 SiC MODULE.	
FIGURE 5. 7. ....	145
SIMULATED EFFECT OF THE STRAY INDUCTANCE OF THE CURRENT PROBE WHEN MEASURING THE V <sub>DS</sub> OF A FF6MR12KM1 SiC MODULE.	
FIGURE 5. 8. ....	145
PERTURBATION IN THE MEASURED CIRCUIT DUE TO THE REFERENCE CONNECTION LOOP, (A) ALLIGATOR CLIP WITH LARGE INDUCTANCE, (B) SPRING CLIP WITH LOW INDUCTANCE AND (C) THE EQUIVALENT CIRCUIT OF A VOLTAGE PROBE CONSIDERING THE REFERENCE CONNECTION LOOP.	
FIGURE 5. 9. ....	146
SIMULATED EFFECT OF THE INPUT CAPACITANCE OF THE VOLTAGE PROBE WHEN MEASURING THE V <sub>CE</sub> OF A FF200R12KT4 Si IGBT MODULE.	
FIGURE 5. 10. ....	146
SIMULATED EFFECT OF THE STRAY INDUCTANCE OF THE CURRENT PROBE WHEN MEASURING THE V <sub>CE</sub> OF A FF200R12KT4 Si IGBT MODULE.	
FIGURE 5. 11. ....	148
PROPOSED RC DIVIDER FOR THE USE OF PASSIVE PROBES.	

FIGURE 5. 12. .... 149  
THE HYBRID ELECTRIC AND CALORIMETRIC POWER LOSS CALCULATION SYSTEM, (A) FIRST STAGE WITH THE DUT OFF, AND (B)  
SECOND STAGE WITH THE DUT ON.

# List of tables

TABLE I.....	17
SELECTED SI AND SIC HIGH POWER MODULES FOR COMPARISON.	
TABLE II.....	21
COMMERCIAL HIGH POWER SIC MOSFET HALF BRIDGE MODULE PACKAGES.	
TABLE III.....	36
REQUIRED DC VOLTAGE FOR EACH GRID VOLTAGE.	
TABLE IV.....	37
2L TOPOLOGY SWITCHING STATES.	
TABLE V.....	38
3L NPC TOPOLOGY SWITCHING STATES.	
TABLE VI.....	39
3L ANPC TOPOLOGY SWITCHING STATES.	
TABLE VII.....	40
3L NPP TOPOLOGY SWITCHING STATES.	
TABLE VIII.....	41
CONSIDERED SEMICONDUCTORS.	
TABLE IX.....	41
CONSIDERED 100FIT AND AMBITIOUS 100FIT VALUES FOR EACH SEMICONDUCTOR VOLTAGE STANDARD.	
TABLE X.....	41
REQUIRED NUMBER OF SEMICONDUCTORS IN SERIES FOR EACH GRID VOLTAGE.	
TABLE XI.....	48
CONSIDERED SEMICONDUCTOR COST NORMALIZED TO THE RATED CURRENT.	
TABLE XII.....	57
EFFECT OF THE ANALYZED CONFIGURATIONS ON THE COMMERCIAL INDICATORS, COMPARED TO THE BASELINE.	
TABLE XI.....	62
SELECTED 62 MM MODULES.	
TABLE XII.....	64
DC-LINK CAPACITOR REQUIREMENTS FOR A 1 MF CAPACITANCE.	
TABLE XIII.....	65
SELECTED CAPACITORS FOR THE TEST BENCH.	
TABLE XIV.....	65
MAXIMUM POWER LOSSES AND THE REQUIRED THERMAL RESISTANCE PER CONVERTER.	
TABLE XV.....	66
MAXIMUM POWER LOSSES AND THE REQUIRED THERMAL RESISTANCE PER CONVERTER.	
TABLE XVI.....	67
CALCULATED REQUIRED MAXIMUM DC-LINK DISCHARGE RESISTANCE FOR BOTH CONVERTERS.	
TABLE XVII.....	68
SELECTED DC-LINK DISCHARGE RESISTORS AND THE CHARACTERISTICS OF THE SYSTEM.	
TABLE XVIII.....	68
SELECTED VOLTAGE SENSOR TO MEASURE THE OUTPUT VOLTAGE.	
TABLE XIX.....	68
SELECTED VOLTAGE SENSOR TO MEASURE THE DC-LINK VOLTAGE.	
TABLE XX.....	69
SELECTED CURRENT SENSOR TO MEASURE THE OUTPUT PHASE CURRENT.	
TABLE XXI.....	70
SELECTED CURRENT SENSOR TO MEASURE THE OUTPUT PHASE CURRENT.	
TABLE XXII.....	75
SINGLE-PHASE 3L ANPC, (A) TOPOLOGY WITH LOW SIDE SWITCHING LOOPS, (B) MODULATION AND PHASE VOLTAGE.	
TABLE XXIII.....	77
RESULTING TOTAL INDUCTANCE FOR CONSIDERED PHASE LEG OPTIONS.	
TABLE XXIV.....	82
SYMMETRY TEST RESULTS AND ASYMMETRY COMPARISON.	
TABLE XXV.....	83
CAPACITOR PLACEMENT TEST RESULTS.	
TABLE XXVI.....	84
NEUTRAL LAYER OPTIMIZATION TEST RESULTS.	
TABLE XXVII.....	85
LOOP INDUCTANCE COMPARISON CONSIDERING MODULES.	

TABLE XXX.....	86
SELECTED VOLTAGE AND CURRENT PROBES.	
TABLE XXXI.....	88
THE SHORT LOOP CALCULATED INDUCTANCE BY SWITCHING EVALUATION FOR DIFFERENT CURRENTS.	
TABLE XXXII.....	89
THE LONG LOOP CALCULATED INDUCTANCE BY SWITCHING EVALUATION FOR DIFFERENT CURRENTS.	
TABLE XXXII.....	91
THE SHORT LOOP CALCULATED INDUCTANCE BY SWITCHING EVALUATION FOR DIFFERENT CURRENTS WITH A SINGLE CAPACITOR.	
TABLE XXXIV.....	102
TEST OPERATION POINTS FOR ALL THE STUDIED CONFIGURATIONS.	
TABLE XXXV.....	111
BASELINE CONFIGURATION CONVERTER OPTIMIZATION SUMMARY.	
TABLE XXXVI.....	112
BASELINE CONFIGURATION COST BREAKDOWN AT 2.5 KHZ AND 10 KHZ SWITCHING FREQUENCY.	
TABLE XXXVII.....	112
LCOCE OF THE BASELINE CONFIGURATION.	
TABLE XXXVIII.....	114
2L CONFIGURATION WITH SiC CONVERTER OPTIMIZATION SUMMARY.	
TABLE XXXIX.....	115
2L CONFIGURATIONS WITH SiC COST BREAKDOWN, AT 2.5 KHZ AND 10 KHZ SWITCHING FREQUENCIES.	
TABLE XL.....	116
LCOCE OF THE 2L CONFIGURATION WITH SiC.	
TABLE XLI.....	117
3L CONFIGURATION WITH Si CONVERTER OPTIMIZATION SUMMARY.	
TABLE XLII.....	118
3L CONFIGURATIONS WITH Si COST BREAKDOWN, AT 2.5 KHZ AND 10 KHZ SWITCHING FREQUENCIES.	
TABLE XLIII.....	119
LCOCE OF THE 3L CONFIGURATION WITH Si.	
TABLE XLIV.....	120
3L CONFIGURATION WITH SiC CONVERTER OPTIMIZATION SUMMARY.	
TABLE XLV.....	121
3L CONFIGURATIONS WITH SiC COST BREAKDOWN, AT 2.5 KHZ AND 10 KHZ SWITCHING FREQUENCIES.	
TABLE XLVI.....	122
LCOCE OF THE 3L CONFIGURATION WITH SiC.	
TABLE XLVII.....	125
THE FORCED AND CONSIDERED PARAMETERS IN THE LCOE CALCULATION TOOL.	
TABLE XLVIII.....	132
CRITICAL VARIABLES AFFECTING THE FALSE TURN ON AND ITS CLASSIFICATION.	
TABLE XLIX.....	133
RISE AND FALL TIME COMPARISON BETWEEN EQUIVALENT 1.2 kV SiC MOSFETs AND Si IGBTs, AT MAXIMUM CURRENT AND 600 Vdc..	
TABLE L.....	135
CRITICAL VARIABLES AFFECTING THE OVERSHOOT AND ITS CLASSIFICATION.	
TABLE LI.....	136
Si AND SiC HIGH POWER MODULES $di/dt$ COMPARISON, WITH THE MAXIMUM ALLOWABLE INDUCTANCE IN THE SWITCHING LOOP TO OPERATE AT 50 % OF VOLTAGE DERATING.	
TABLE LII.....	141
Si AND SiC HIGH POWER MODULES RISE TIME COMPARISON, WITH THE REQUIRED VOLTAGE PROBE BANDWIDTH. DATA OBTAINED FROM DATASHEETS.	
TABLE LIII.....	141
Si AND SiC HIGH POWER MODULES $di/dt$ COMPARISON, WITH THE REQUIRED CURRENT PROBE USEABLE RISE TIME. DATA OBTAINED FROM DATASHEETS AND LABORATORY TESTS.	
TABLE LIV.....	142
SEVERAL VOLTAGE PROBES AVAILABLE IN THE MARKET.	
TABLE LV.....	143
SEVERAL CURRENT PROBES AVAILABLE IN THE MARKET.	

# GLOSSARY

## LIST OF ABBREVIATIONS

<b>2L</b>	Two level
<b>3L</b>	Three level
<b>3L ANPC</b>	Three level active neutral point clamped
<b>3L NPC</b>	Three level neutral point clamped
<b>3L NPP</b>	Three level neutral point piloted
<b>AC</b>	Alternating current
<b>AEP</b>	Annual energy production
<b>BC</b>	Business case
<b>BoM</b>	Bill of materials
<b>BTB</b>	Back to back
<b>Capex</b>	Capital expenditure
<b>DC</b>	Direct current
<b>Desat</b>	Desaturation
<b>DFIG</b>	Doubly fed induction generator
<b>DPT</b>	Double pulse test
<b>DSP</b>	Digital signal processor
<b>DUT</b>	Device under test
<b>EMC</b>	Electromagnetic compatibility
<b>EMI</b>	Electromagnetic interference
<b>ESL</b>	Equivalent series inductance
<b>ESS</b>	Energy storage system
<b>FC</b>	Full converter
<b>GaN</b>	Gallium nitride
<b>IGBT</b>	Insulated gate bipolar transistor
<b>LCoCE</b>	Levelized cost of conversion energy
<b>LCoE</b>	Levelized cost of energy
<b>LED</b>	Light emitting diodes
<b>LFT</b>	Low frequency transformer
<b>LuT</b>	Lookup table
<b>LV</b>	Low voltage
<b>MEA</b>	More electric aircraft
<b>MFT</b>	Medium frequency transformer
<b>MOSFET</b>	Metal oxide semiconductor field effect transistor
<b>MV</b>	Medium voltage
<b>Opex</b>	Operation expenditure
<b>PFC</b>	Power factor correction
<b>PM</b>	Permanent magnet
<b>PV</b>	Photovoltaic
<b>PWM</b>	Pulse width modulation
<b>R&amp;D</b>	Research and development
<b>rms</b>	Root mean square
<b>Si</b>	Silicon
<b>SiC</b>	Silicon carbide
<b>SOA</b>	Safe operation area
<b>SST</b>	Solid state transformer
<b>WBG</b>	Wide bandgap
<b>WES</b>	Wind energy system
<b>WT</b>	Wind turbine



CHAPTER 1  
**Introduction**



# 1.Introduction

## 1.1. Background

Humanity is looking for a world where human habitants are safe and sustainable, and where there is universal access to affordable, reliable and sustainable energy, according to Agenda 2030 [1]. In addition, technological and scientific innovation in medicine and energy is considered key to develop knowledge in societies.

The power grid was called “the largest, most complex machine ever devised by man” by Charles Steinmetz in the early 1900s, and its complexity has been increasing since then [2]. The systems basic characteristics since the early days have been 3-phase AC constant voltage, using AC synchronous machines, running at constant frequency, transmitting power over significant distances [3]. However, even if today the power system is expected to integrate a variety of AC and DC sources, together with micro grids and distributed consumption and generation, the grid still requires the bulky power back up of AC synchronous generators.

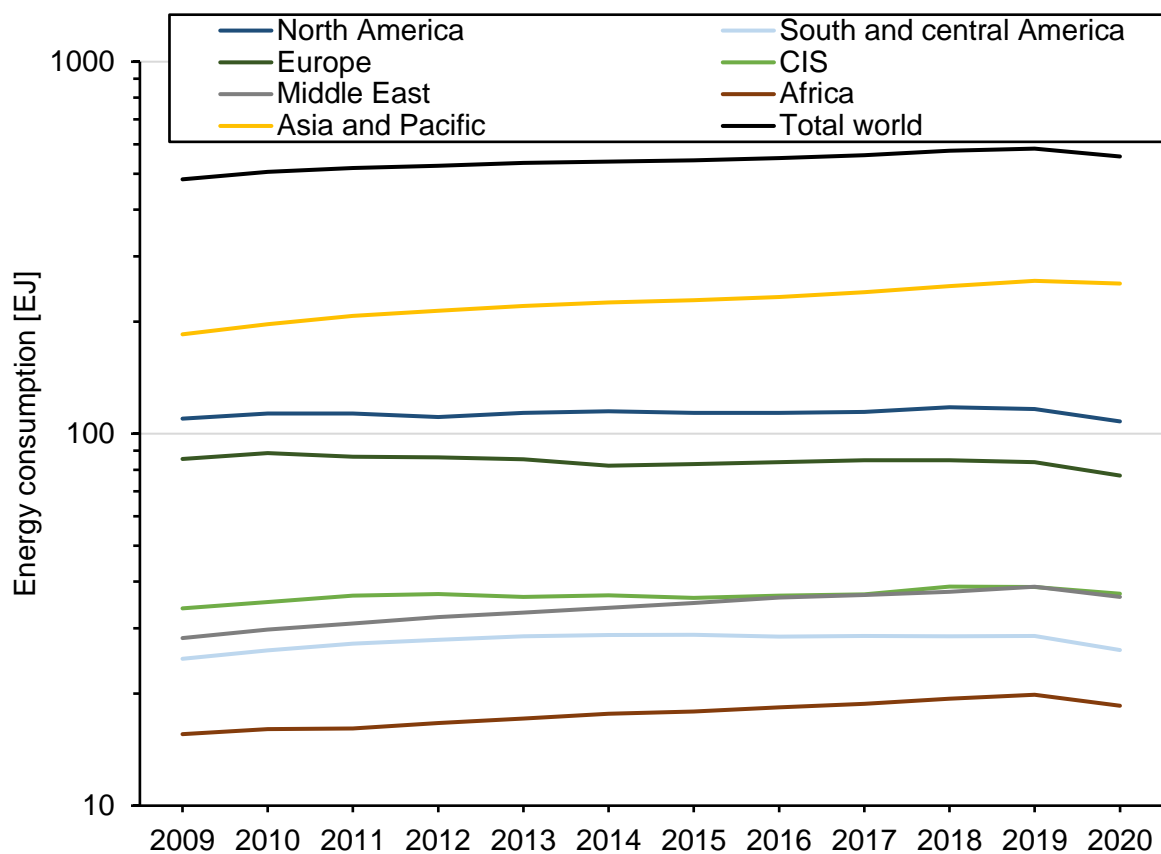
With the increasing concern about environmental issues, such as carbon emissions, the global climate change and energy security, the before mentioned change is accelerated. Based on stated policies, various initiatives are to be considered in order to achieve a reduction in carbon emissions, such as avoiding the increasing energy demand, using bio energy, electrification of remote or rural areas and increasing the performance of energy consuming devices [4].

This work collaborates on the technological transition our society will face in the following years. Improving renewable energy systems is the way this author has found to make a contribution to the world.

## 1.2. Renewable energies

The energy consumption in the world is increasing constantly, and it has grown more than 17% in the last decade [5]. Although some regions like Europe are taking measures to control the consumption growth, the worldwide overall consumption is increasing, as can be seen in Figure 1. 1. Due to the worldwide pandemic in 2020, the energy consumption around the world has decreased, but is expected to increase again in the year 2021 [6]. For this reason, this analysis will focus on the previous years' trend.

Renewable energies are vital to satisfy the energy demand. By 2030 in particular, United Nations want to increase substantially the share of renewable energy in the global energy mix, while doubling the global rate of improvement in energy efficiency [1]. To do so, it is understood the need to enhance international cooperation, promoting investment in energy infrastructure and research in energy technology.

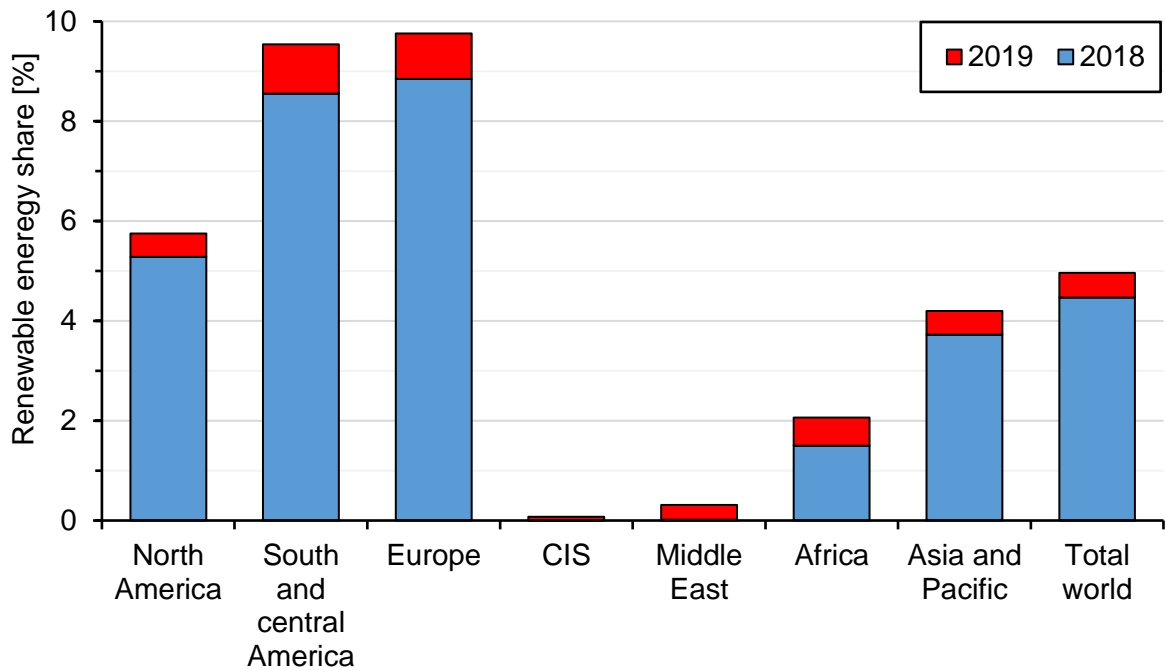


**Figure 1. 1.**

Worldwide energy consumption evolution in different geographical regions [6].

### 1.2.1. Renewable energies worldwide

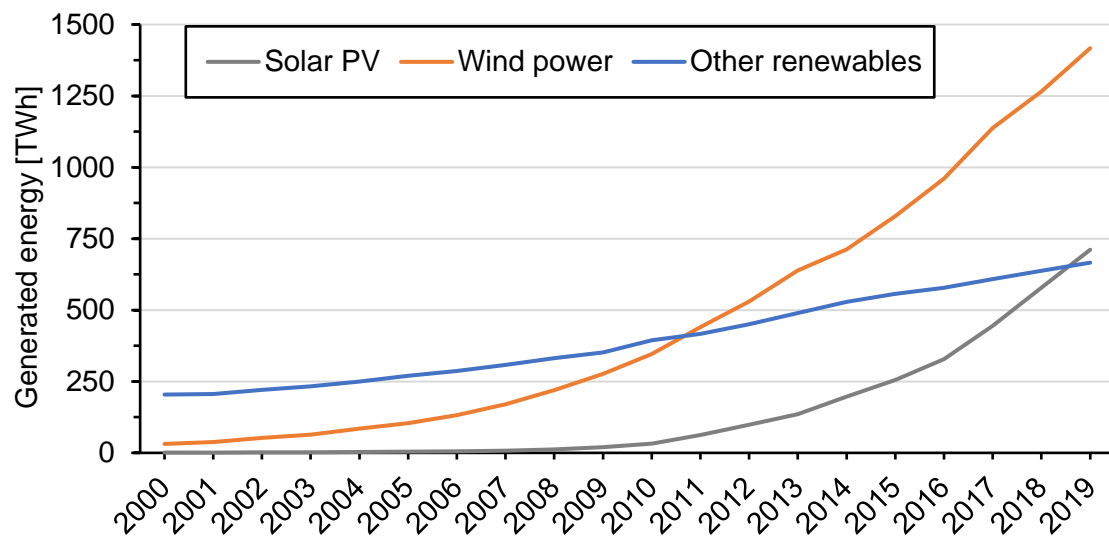
Even if it is increasing, as shown in Figure 1. 2, the share of renewable energy production in the world is still below 5 %. With the current structure, sectors like transport cannot be supplied by renewable means, increasing the dependency on oil. If biofuels are not considered, the contribution of renewable energies in this sector is negligible at 0.3 %. Another example is heating, which is responsible for the 51 % of the energy consumption in the world. Renewable energy only contributes with 2.9 % toward the total [7].



**Figure 1. 2.**

Worldwide renewable energy share for 2018 and 2019 in different geographical regions [5].

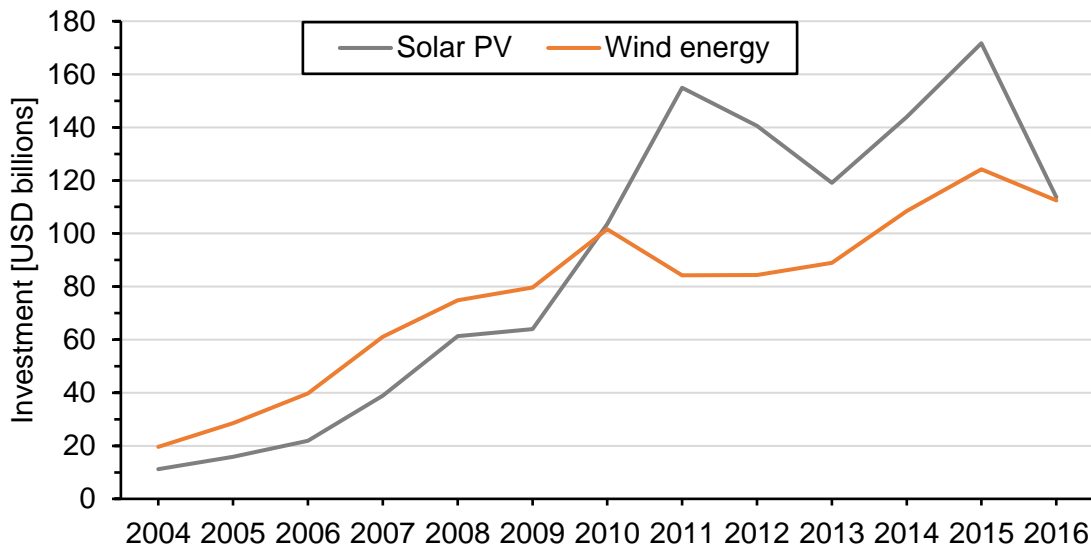
Electricity production is the sector with the highest renewable energy integration. The renewable production share in electricity production was 27.3 % in 2019 [7]. This percentage means an increment of 1.1 % with respect to 2018 [8]. Figure 1. 3 shows the dominance of wind and solar photovoltaic (PV) power (excluding hydro power) among the renewable energies. Both wind and solar PV energy generation are increasing since the 2000s, with growth especially significant since 2010. Both energy sources generated more energy than the rest of renewable energies together [9], which shows that these technologies are the most promising ones for the near future.



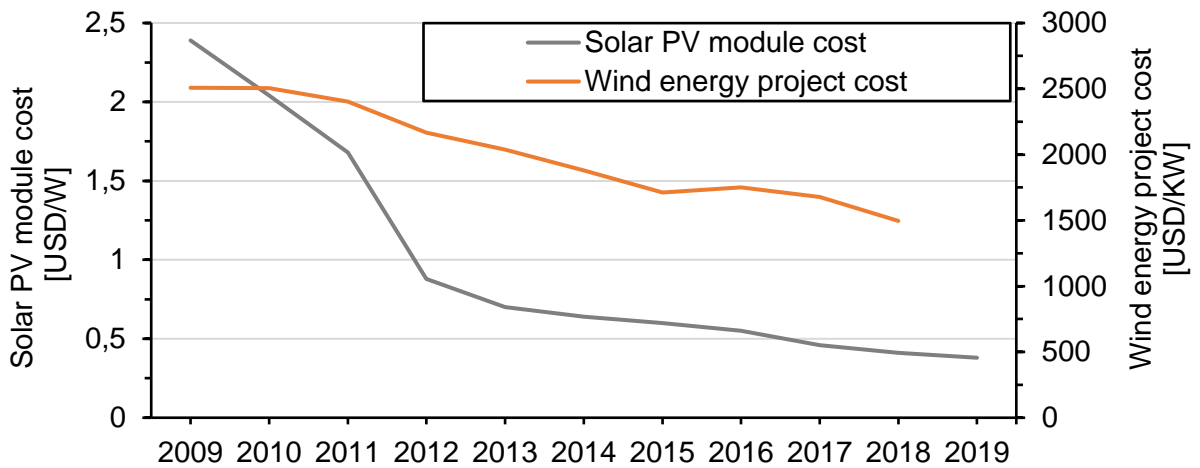
**Figure 1. 3.**  
Generated energy by source and year [9].

## 1.2.2. Renewable energies economy

Worldwide investment in solar PV and wind energy has been also growing during the last decade, shown in Figure 1. 4. The higher investment leads to a reduction in the cost of solar PV modules per watt. The same effect can be seen in Figure 1. 5 with wind energy project costs per kW in the United States. This makes solar PV and wind energy more competitive with respect to other energy sources.



**Figure 1. 4.**  
Evolution of the worldwide investment in solar PV and wind energy [9].



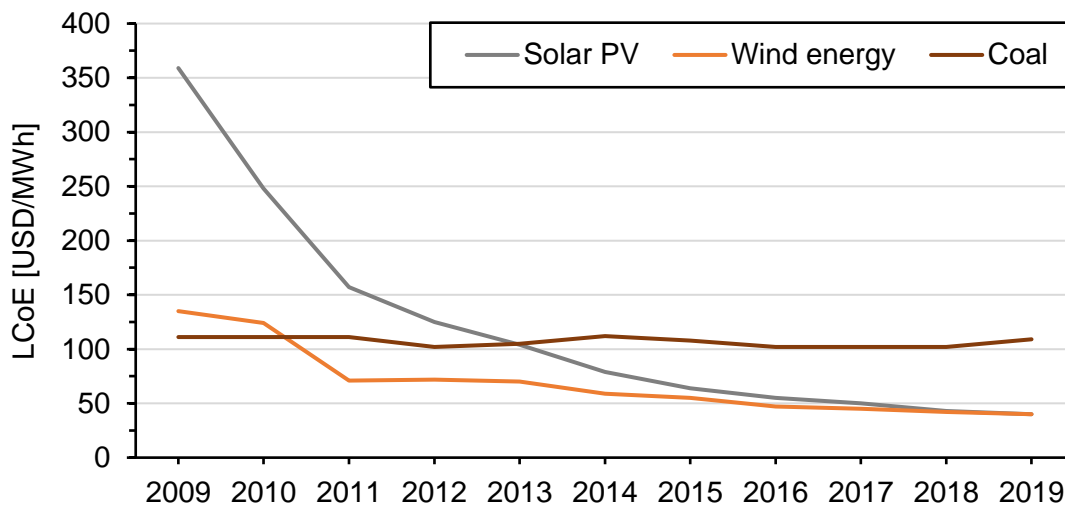
**Figure 1. 5.**  
Evolution of the cost of solar PV modules and wind energy projects [9].

### 1.2.3. Levelized cost of energy

The market competitiveness of an energy source can be evaluated by using the levelized cost of energy (LCoE) metric. The LCoE is defined by the ratio of the total cost of an energy system and the total energy generated over the lifetime of the system [10]. The estimation of the LCoE requires combined efforts from economists and engineers, exchanging technical and economic data between them.

Due to the complexity of the calculation, together with the multiple factors affecting the metric, the estimation ends up being a broad list of assumptions. This is why LCoE calculations are done in a best-worst scenario, obtaining a value band instead of a single value. According to the latest estimations carried out in 2019 [11], the renewable energies can already compete with conventional energy sources.

Utility scale renewable energies, like solar PV and wind already outperform most of the conventional generation systems in the whole LCoE band, as shown in Figure 1. 6. However, low annual energy production (AEP) penalizes rooftop residential and community scale PV.



**Figure 1. 6.**  
LCoE evolution of solar PV, wind energy and coal [11].

Governments and organizations are offering subsidies to support renewable energies, as demanded in the 2030 Agenda [1] or Horizon Europe [12] initiatives. These economic plans and subsidy policies can further reduce the LCoE of renewable energies, when compared to conventional generation systems. These last ones do not receive any economic help, due to the world's need to reduce carbon emissions and revert global climate change. Because of its high initial cost, in installation and construction, offshore wind generation is the renewable energy that could benefit the most from subsidies.

In addition, conventional generation systems' LCoE calculation is sensitive to fuel price. This effect can vary the profitability of conventional generation, increasing the risk of a certain investment. Renewable energies do not suffer from this effect. The fuel price variations are common, and can be caused by various factors [13]. Some of those factors are the irregular or random events occurring in the world [14], like the COVID pandemic suffered in 2020. Some others are speculation activities [15], global economic activities [16], or social and political behaviors of countries and nations [17]. All these factors contribute to the uncertainty about the price of the fuel, making conventional generation LCoE and profitability variable and unpredictable in some cases.

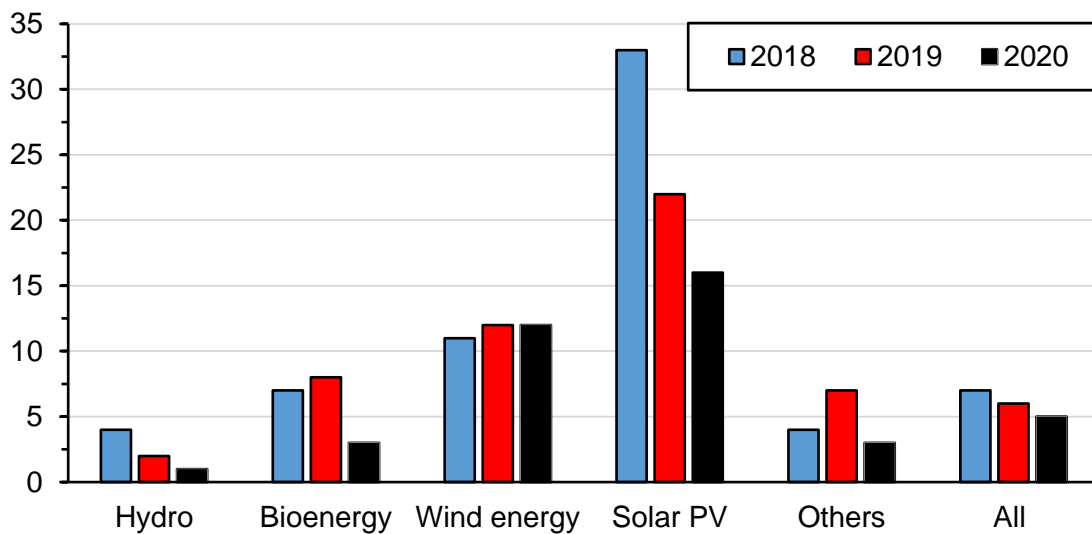
Depending on the technological maturity of a certain energy generation system and its particular characteristics, the LCoE evolution in time is different. Two main trends can be identified. Those which are nearly stable in time, due to their technological maturity, such as conventional energy generation sources. Others are decreasing in time, like wind and solar PV. The decreasing rate of wind power is smaller due to the maturity of the technology, already developed in the 1970s. However, improvements in the system decrease the LCoE year by year. In the case of solar PV, the decrement rate was very fast in the early 2010s, and is reaching more steady rates nowadays. Wind energy and solar PV are competing at the present moment to become the most profitable energy generation system.

### 1.3. Wind energy

In 2008, the U.S. Department of Energy said it is feasible to generate 20 % of the energy in the United States using wind by 2030 [18]. This statement is based on the exponential growth the wind energy is experiencing, together with the rapid pace of its integration into

the energy mix. This goes together with the increased single turbine capacity. When wind power began in the 1970s, wind turbines were rated in tens of kilowatts [2]. However, the rated power is increasing, arriving to the highly anticipated 15-20 megawatt power wind turbines in 2020 [19].

Figure 1. 7 shows wind energy is the most promising renewable energy source, because it is experiencing a regular growth every year. In addition, and unlike solar PV, wind energy can be available during the whole day, even at night. It also allows to still use the land under the wind towers, for agriculture for example. However, the variability of wind makes it highly unpredictable. Offshore wind farms have been developed looking for a more constant wind profile.



**Figure 1. 7.**

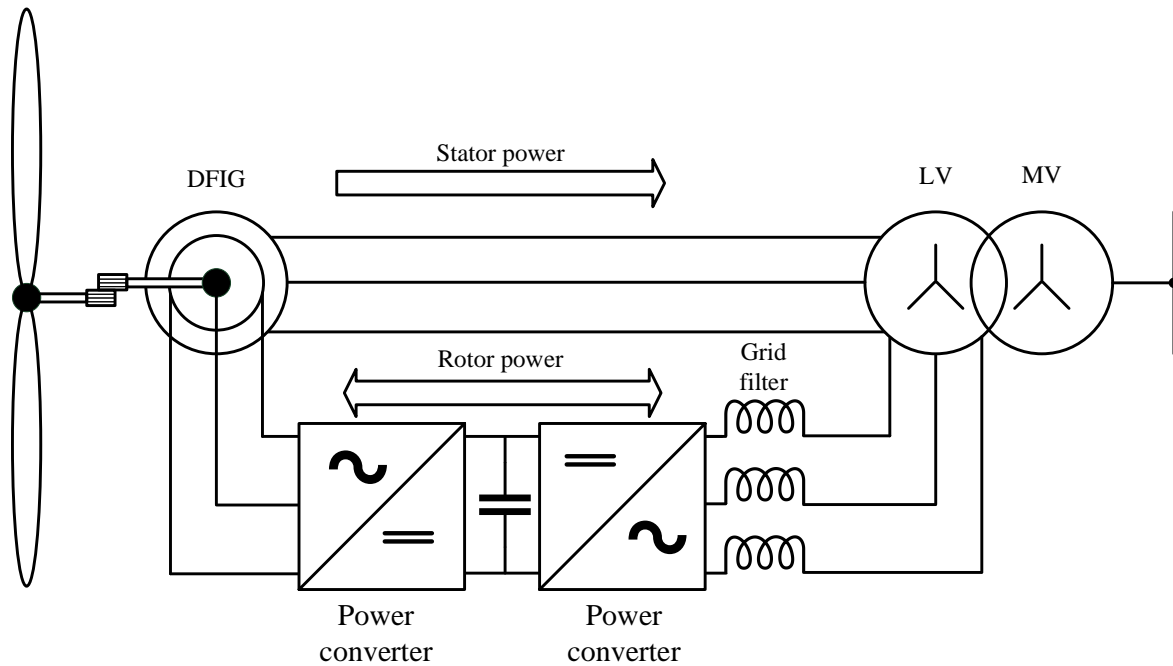
Annual growth for renewable electricity generation by source, 2018-2020 [20].

### 1.3.1. Wind energy configurations

The wind turbines market is dominated by variable speed wind turbines in more than 75 % installations since the 2000s [21]. These wind turbines require power converters to control the power flow inserted in the grid [21]. The power converter is also needed to decouple the wind turbine from the electric grid. Current variable speed wind turbines configurations are mainly divided between full converter (FC) and doubly fed induction generators (DFIG) [22], [23].

#### 1.3.1.1. DFIG

Currently the DFIG is the most adopted configuration, and has been used since the 2000s [24]. As shown in Figure 1. 8, the converter processes only the current and power of the rotor, so the speed of the blades can be controlled in the optimum speed. By doing so, the energy output of the system is maximized [22]. The stator is directly connected to the grid, so the power converter is only rated for the 25-30 % of the total power of the system.



**Figure 1. 8.**  
Variable speed wind turbine system, DFIG configuration.

The reduced power rating of the converter makes this configuration cost effective. In addition, the direct connection of the stator to the grid means the stator power is transferred to the grid without losses. The DFIG configuration has high total system efficiency. Due to the lower cost and better efficiency, this configuration has the best LCoE [22].

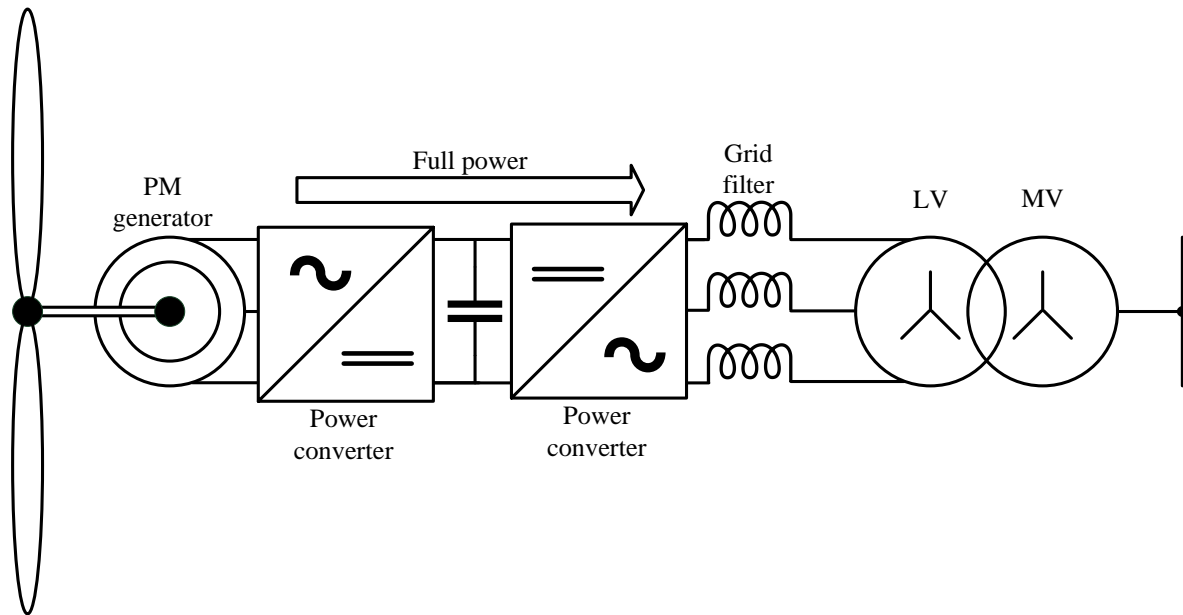
However, as the stator is linked to the grid, a mechanical gearbox is needed to increase the mechanical axis frequency to the grid electrical frequency. In addition, slip rings must be used to make electrical contact between the power converter and the rotor. These slip rings reduce the high voltage capability of the system. The additional mechanical parts reduce the reliability of this configuration, increasing the maintenance cost. The system is not fully decoupled from the grid, so the control of the DFIG configuration is limited.

This configuration is preferred in onshore wind energy. This is due to the high maintenance needs. The DFIG wind turbines need to be installed in locations with easy access. The better LCoE compensates the high maintenance costs in these type of locations.

### 1.3.1.2. Full converter

In the full converter configuration, the permanent magnet (PM) synchronous generator is the most commonly used one. As seen in Figure 1. 9, the power converter needs to process the full power of the system.





**Figure 1. 9.**  
Variable speed wind turbine system, full converter configuration.

The full converter system is totally decoupled from the electric grid, meaning it provides full controllability with the best grid support [24]. It does not require any mechanical part or slip ring, so the reliability is better than in the DFIG. This lowers the maintenance costs. In addition, the lack of slip rings allows to operate at high voltage.

In FC configuration, the permanent magnet (PM) synchronous generator is the most commonly used one. The FC configuration with PM generators provide high reliability, no need of a gearbox, no slip rings and full controllability with best grid support [24]. All these characteristics make FC configuration best for offshore wind energy, due to its low maintenance. However, the configuration suffers from more stress in the power converter, high losses and high cost due to the full power rating of the converter so this configuration is not preferred in onshore [24].

However, this configuration has lower overall system efficiency because the power converter has to process the power of the whole system. The components also suffer from high stress. In addition, the cost of the system is higher due to the high power rating of the converter. The higher cost and lower efficiency lead to a worse LCoE when compared to the DFIG configuration.

The full converter configuration is preferred in locations with difficult accessibility, due to the low maintenance needs. High power systems also take advantage of the high voltage capability of the configuration. The before mentioned makes full converter configuration ideal for offshore wind energy. The low maintenance cost and high reliability compensate the lower LCoE in offshore.

## 1.3.2. Power electronics of wind energy

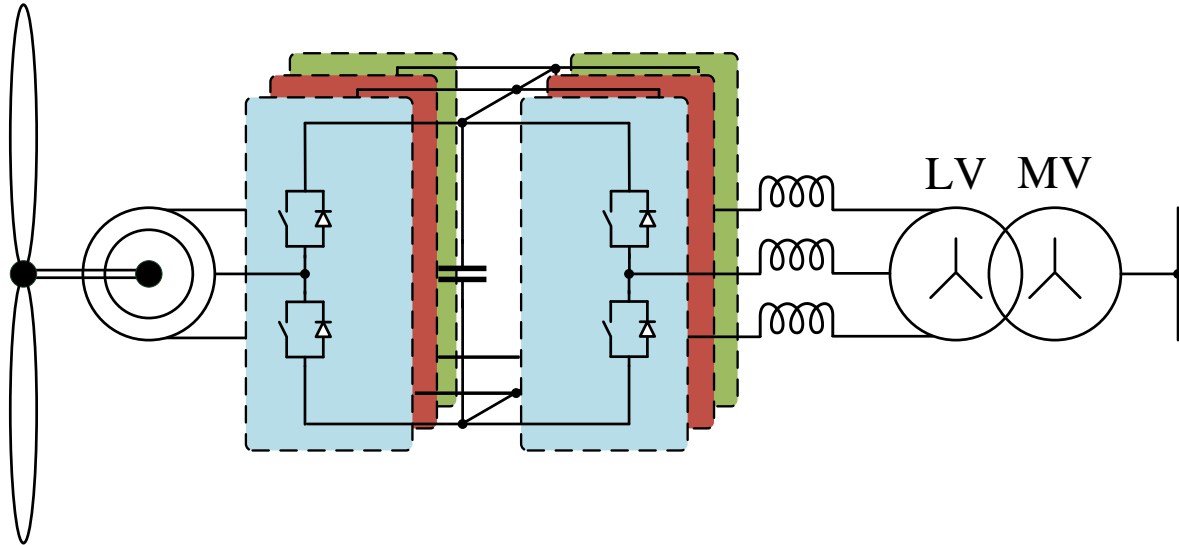
### 1.3.2.1. Back to back converters

The back to back (BTB) converters are symmetric converters with a capacitor bank in the middle. They perform AC-AC conversion with a DC stage in the middle, so the input and the output are decoupled. While one half performs rectification, the other performs inversion. They have a certain amount of energy storage in the DC link that can be used to

add extra features, like fault ride through. Both DFIG and FC configurations use this topology, because the main function in both systems is to decouple the grid from the wind turbine in some way. The only change is the power rating and the control of the converter.

### 1.3.2.2. Two level BTB

In large scale wind energy systems, for both FC or DFIG configurations, the 2 level BTB topology, shown in Figure 1. 10 is the most used one [25]. It consists on a half bridge on each side of the DC link. This converter can synthesize two voltage levels in the output, being those the positive and negative voltages of the DC link.



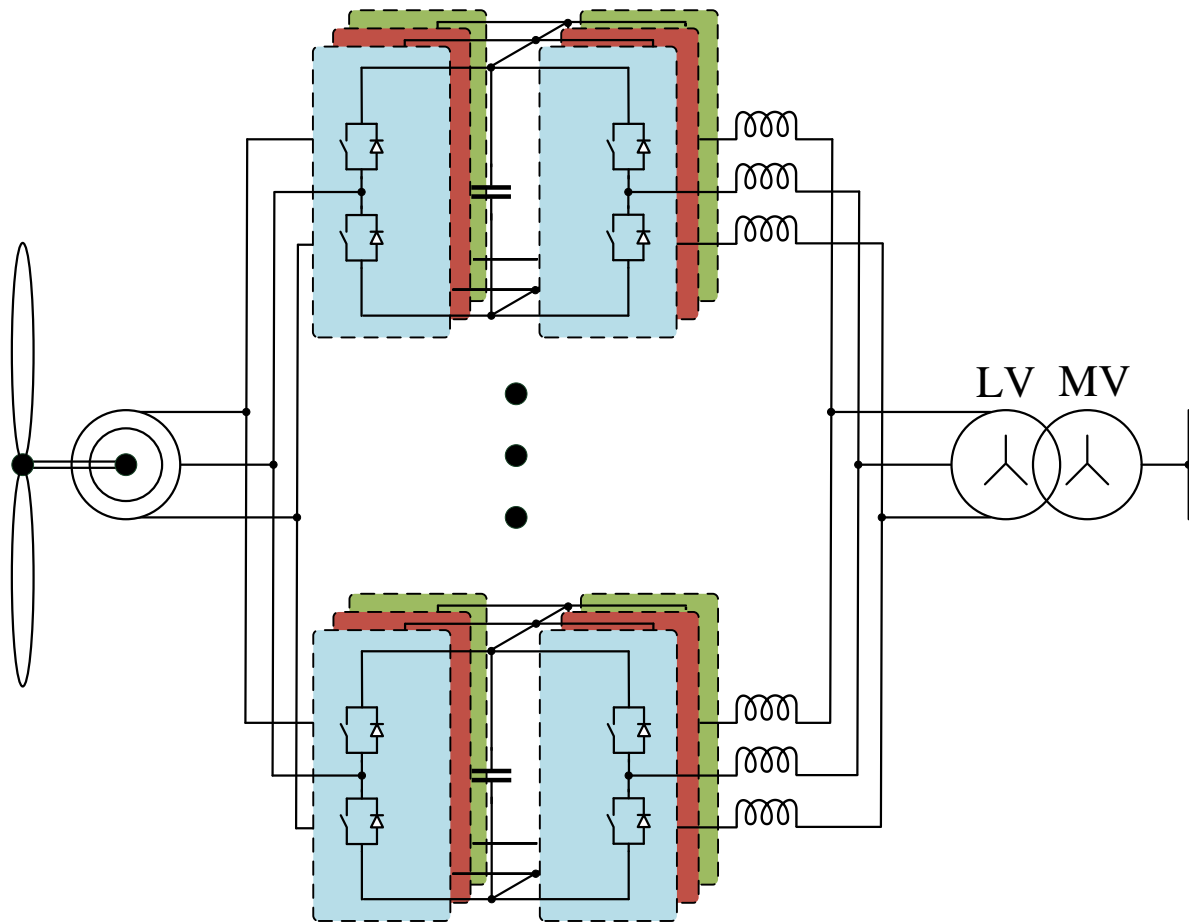
**Figure 1. 10.**  
2 level BTB topology.

Its main advantage is its simplicity. In addition, the low component count makes it a cost effective solution. Finally, and as it only has one switch in the conduction path of the current, the conduction losses of this topology are low.

However, the components suffer high stress so higher semiconductor ratings are needed. Also, the topology generates high  $dV/dt$  because it can only synthesize two voltage levels. As the semiconductors are switching the full DC voltage, the switching losses are high. All the before mentioned makes the 2 level BTB converter a low efficiency solution in high power.

### 1.3.2.3. Improved two level BTB

Modular strategy, using the multi cell topology shown in Figure 1. 11 is used to improve the 2 level BTB performance in high power. This strategy allows to reduce the power rating of each cell [19], [26].



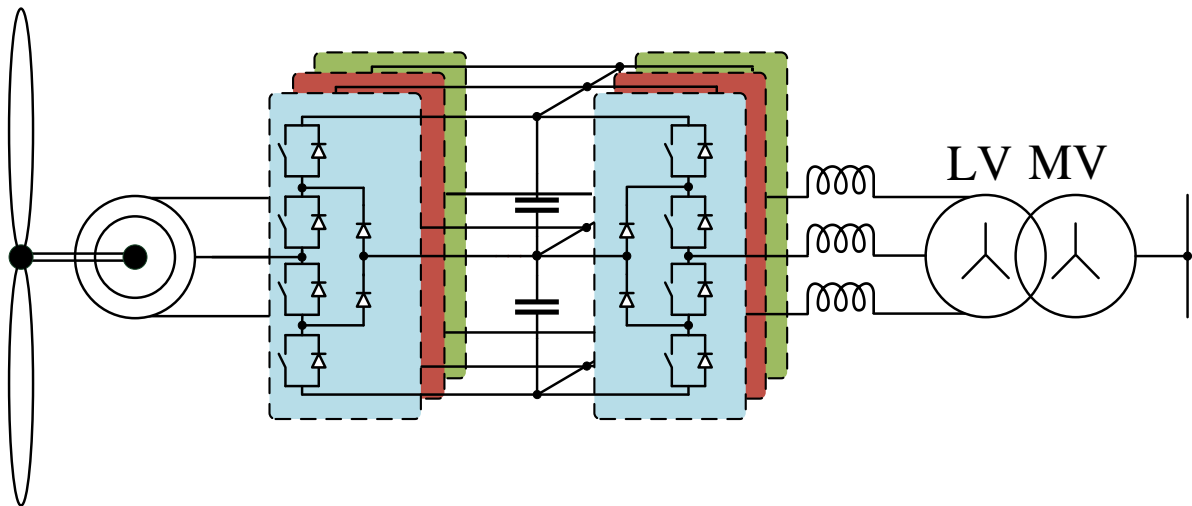
**Figure 1. 11.**  
Multi cell 2 level BTB topology.

The multi cell strategy allows to have optimum performance by each module, and it is a widely used strategy in wind energy. In addition, system level benefits are obtained if special switching patterns are used to interleave the output voltage levels [27]. These benefits can bring reductions in the output filter.

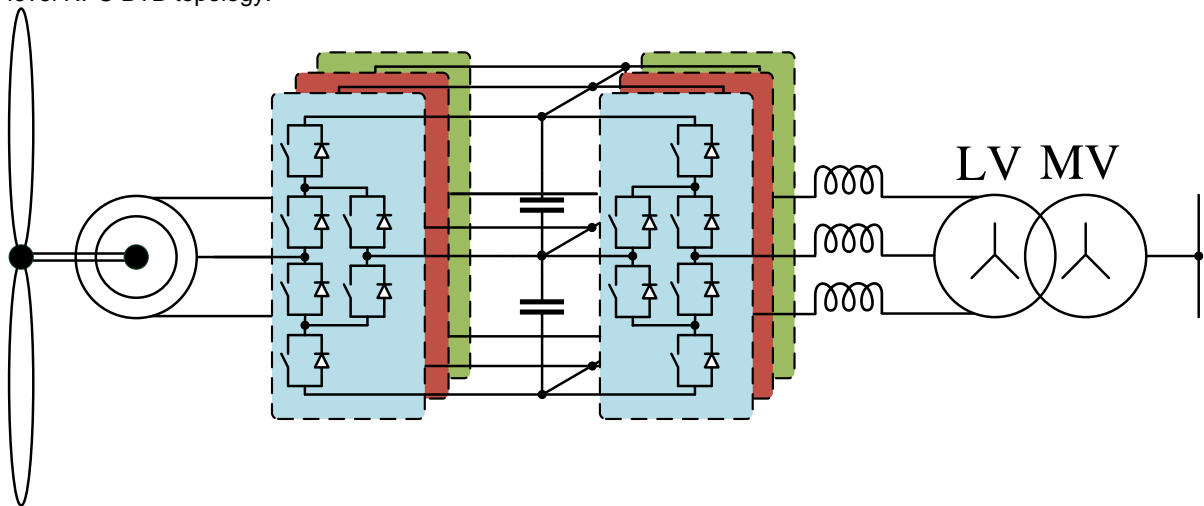
Although the multi cell strategy improves the performance of the 2 level BTB converter, it also increases its complexity. In addition, the cost of the system is higher because the component count is increased. Finally, unwanted circulating current can occur between cells so large coupling inductors are required to suppress them [28].

#### 1.3.2.4. Multilevel BTB

Due to the before mentioned problems of the 2 level BTB converter in large scale wind turbines, multilevel topologies could become the preferred option in these applications [29]–[32]. These topologies can synthesize three voltage levels in the output, including the 0 V level. Even if several level topologies can be used, the most common ones are three level topologies, to keep simplicity and component count low. Among these, the 3 level neutral point clamped (3L NPC) in Figure 1. 12 and its evolution, the 3 level active neutral point clamped (3L ANPC) in Figure 1. 13 are the most common ones [24], [25]. Both topologies need a 3 level branch in each side of the DC link, in order to create the BTB converter.



**Figure 1. 12.**  
3 level NPC BTB topology.



**Figure 1. 13.**  
3 level ANPC BTB topology.

Each semiconductor is switching only half of the DC voltage, so the switching losses are reduced. Moreover, the multilevel topologies have lower  $dV/dt$  and voltage stress for components. This allows to use lower rating components, which are cheaper and have better performance. Finally, output filters can be reduced due to the better harmonic content of the output voltage. These topologies are used in high voltage applications, dividing the voltage of the application between several semiconductors.

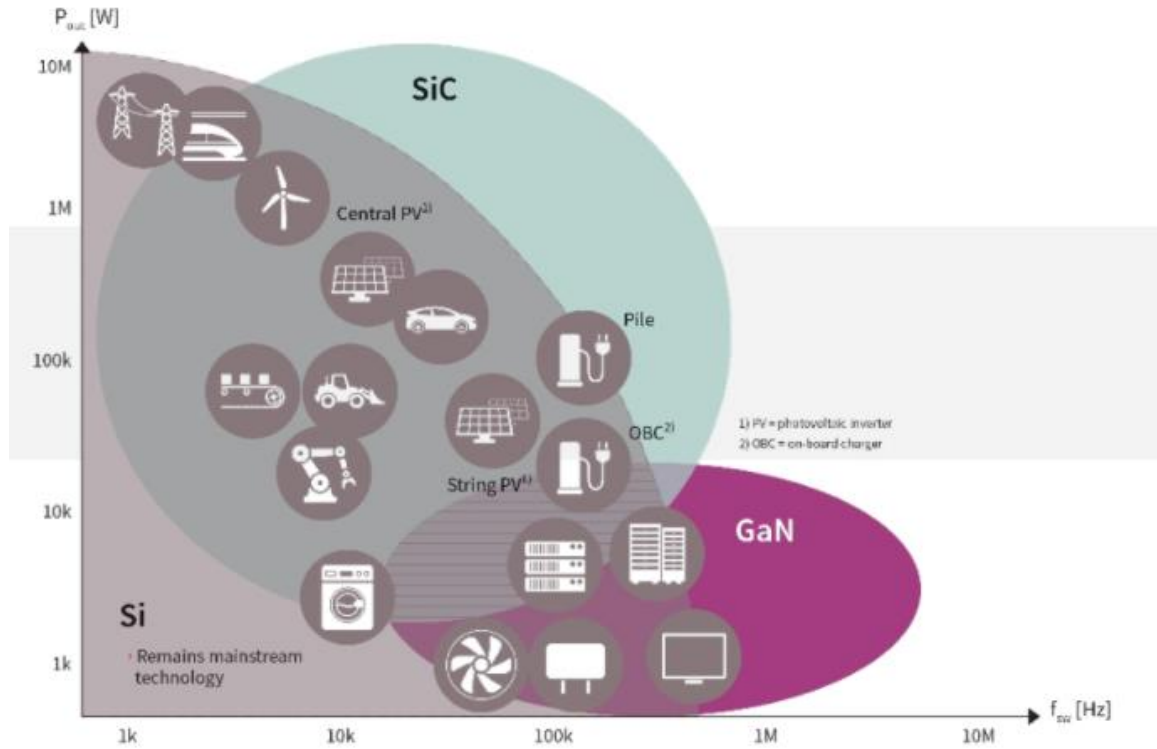
However, each branch needs more components, increasing the cost of the system. The complexity and the switching patterns are also higher. As the DC link is divided, DC link voltage balancing strategies are required and need to be considered in the switching pattern, further adding to the complexity [33]–[36].

### 1.3.3. Levelized cost of energy for wind energy

As the renewable energy industry is a very competitive market, manufacturers want to improve LCoE of their products. Even a slight change in the LCoE can make a big difference in the profitability of their products. The main strategy to date has been to increase the power of the wind turbines, introducing modular strategies. Another successful strategy is

to improve the reliability, reduce maintenance costs or even introduce extra features to improve LCoE.

Finally, a new trend is to investigate the introduction of new technologies or semiconductors. In the new generation of semiconductors, the most promising wide bandgap (WBG) semiconductor for high power applications such as wind energy are the silicon carbide (SiC) ones, as shown in Figure 1. 14.



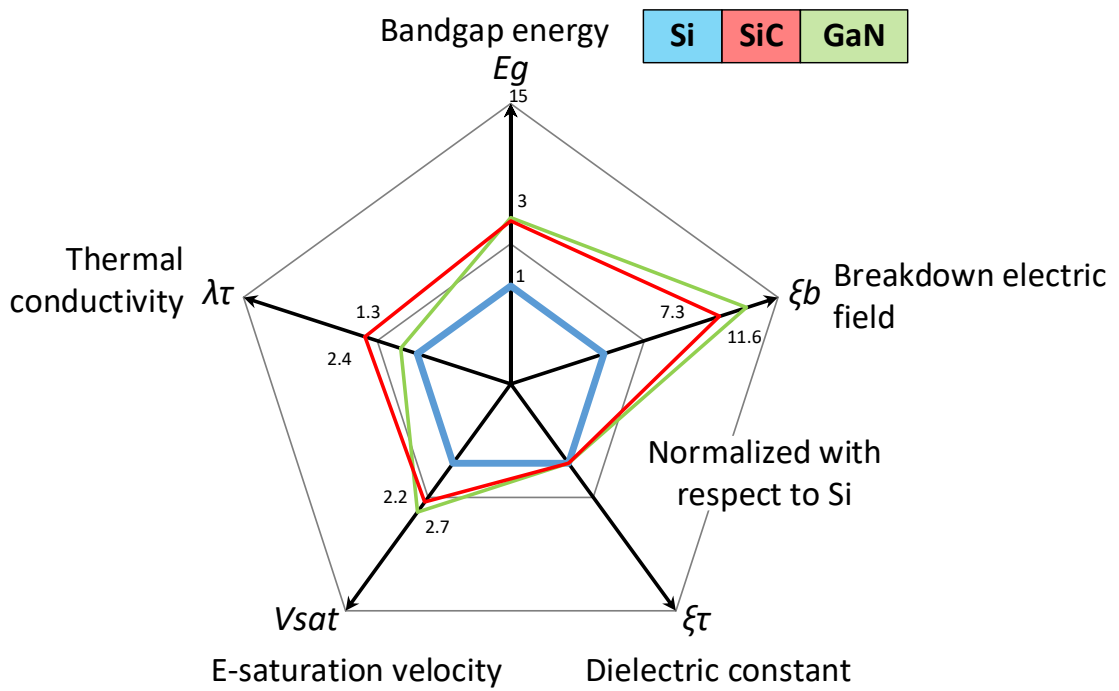
**Figure 1. 14**  
High power applications for SiC [37].

## 1.4. Silicon carbide semiconductors

Silicon carbide has better physical characteristics than silicon (Si) for its use in power electronics [38]. Different polytypes exist, and their physical characteristics differ widely between one another [38], [39]. 4H and 6H polytypes are most used in power electronics because they are the cheapest [36]. SiC is a strong candidate to replace silicon in high voltage and high power applications.

### 1.4.1. Physical characteristics of silicon carbide

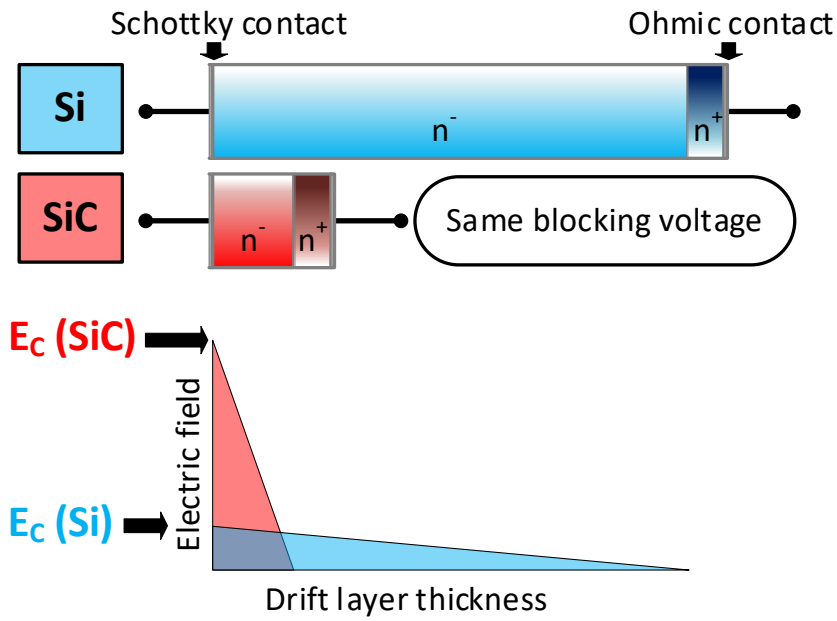
Figure 1. 15 show the physical characteristics of silicon carbide and gallium nitride (GaN), normalized to silicon. These characteristics allow SiC to overcome the limits of power electronics with silicon.



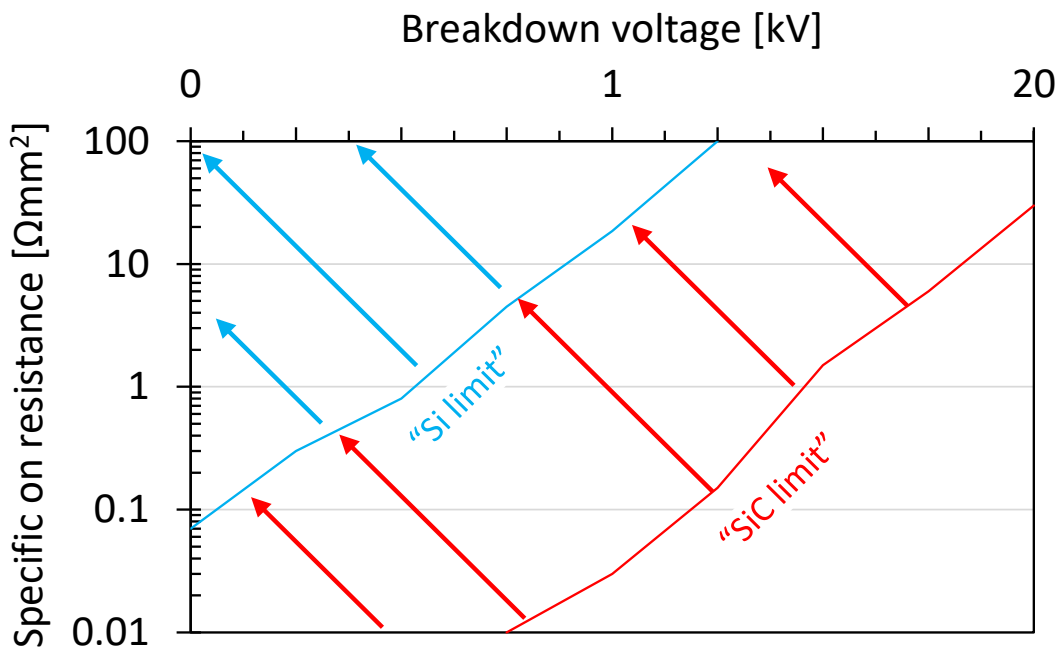
**Figure 1. 15.** Key physical characteristics of silicon carbide and gallium nitride, normalized to silicon [38].

**1.4.1.1. Higher breakdown electric field**

Higher breakdown electric field means it is possible to build semiconductors with higher blocking voltage with thinner drift layers, as shown in Figure 1. 16. This reduces the conduction resistance and losses, changing the silicon limits as seen in Figure 1. 17. The arrows show the design are that can be achieved with both technologies, extending the Si limits with SiC.



**Figure 1. 16.** Silicon and silicon carbide drift layer thickness comparison for the same blocking voltage [40].



**Figure 1. 17.** Silicon and silicon carbide specific on resistance comparison for different breakdown voltages [40].

**1.4.1.2. Higher bandgap energy**

Having higher bandgap energy than Si allows SiC to operate at higher temperature. Ideally, the temperature can increase up to 300 °C, without changing its physical characteristics. This will reduce the cooling needs of the converter, and is a key factor in some applications that need to work in harsh environments.

### 1.4.1.3. Higher thermal conductivity

This characteristic means SiC has better capability to evacuate heat than Si. Again, this can reduce the cooling needs of the SiC converters. However, nowadays the thermal conductivity of SiC semiconductors is limited by the packaging. Currently the packaging materials are the same as for Si, limiting the thermal conductivity and not being designed for high temperature operation.

### 1.4.1.4. Higher electron saturation velocity and smaller chip area

Having high electron saturation velocity allows SiC semiconductors to switch conduction states faster. The less time is spent in the switching, the lower the switching losses are. To operate at higher switching frequency with SiC semiconductors is possible because the energy wasted in each switching is lower than with Si. High switching frequency brings system level benefits in power electronics. Reducing the total harmonic distortion of the synthesized output voltage and reducing the passive components size are the most significant ones.

## 1.4.2. High power silicon carbide semiconductors

The better physical characteristics of SiC allow to develop metal oxide semiconductor field effect transistors (MOSFET) with voltage and current rating of Si insulated gate bipolar transistors (IGBT). Manufacturers are developing full SiC modules equivalent in breakdown voltage and nominal current for high power applications, using Si traditional packages. Regarding diodes, Si fast recovery diodes will be replaced by SiC schottky diodes, with improved switching performance. Equivalent high power modules are analyzed and compared next, regarding their forward and switching characteristics. The selected modules and diodes are shown in Table I, with avt Si fast recovery diode the freewheeling diode in the Si IGBT modules.

**Table I.**

Selected Si and SiC high power modules for comparison.

Technology	Manufacturer	Part number	Voltage [V]	Maximum DC current [A]	Maximum pulsed current [A]
Si IGBT	Infineon	FF200R12KT4	1200	200	400
SiC MOSFET	Infineon	FF6MR12KM1	1200	250	500
Si fast recovery diode	Infineon	FF200R12KT4 freewheeling diode	1200	200	400
SiC Schottky diode	Microsemi	MSCDC200A120D 1PAG	1200	200	400



### 1.4.2.1. SiC vs Si comparison in forward conduction

Figure 1. 18 compares the forward characteristics of the selected high power Si and SiC modules. The MOSFET structure of SiC does not suffer from direct voltage drop, so has low loss in conduction at low currents. However, at high current the performance is similar. The Si fast recovery diode is better in conduction, but the bidirectional capability of the SiC MOSFET limits the use of SiC schottky diode only to dead times.

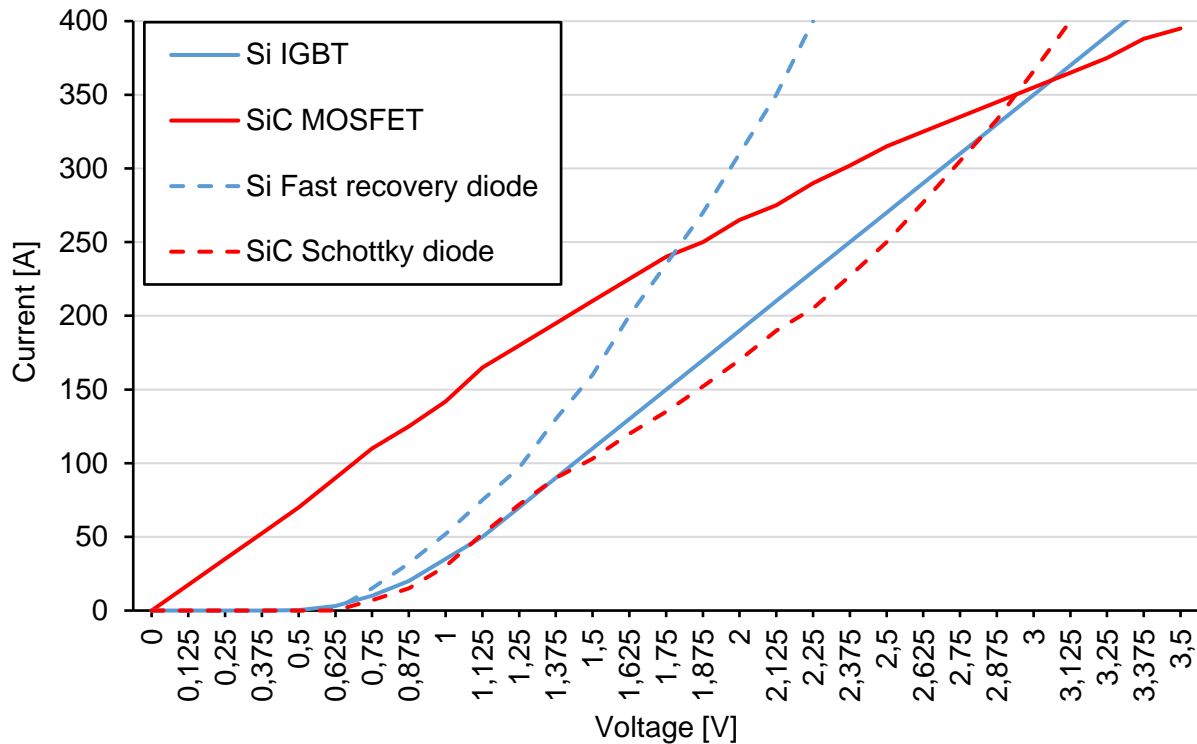


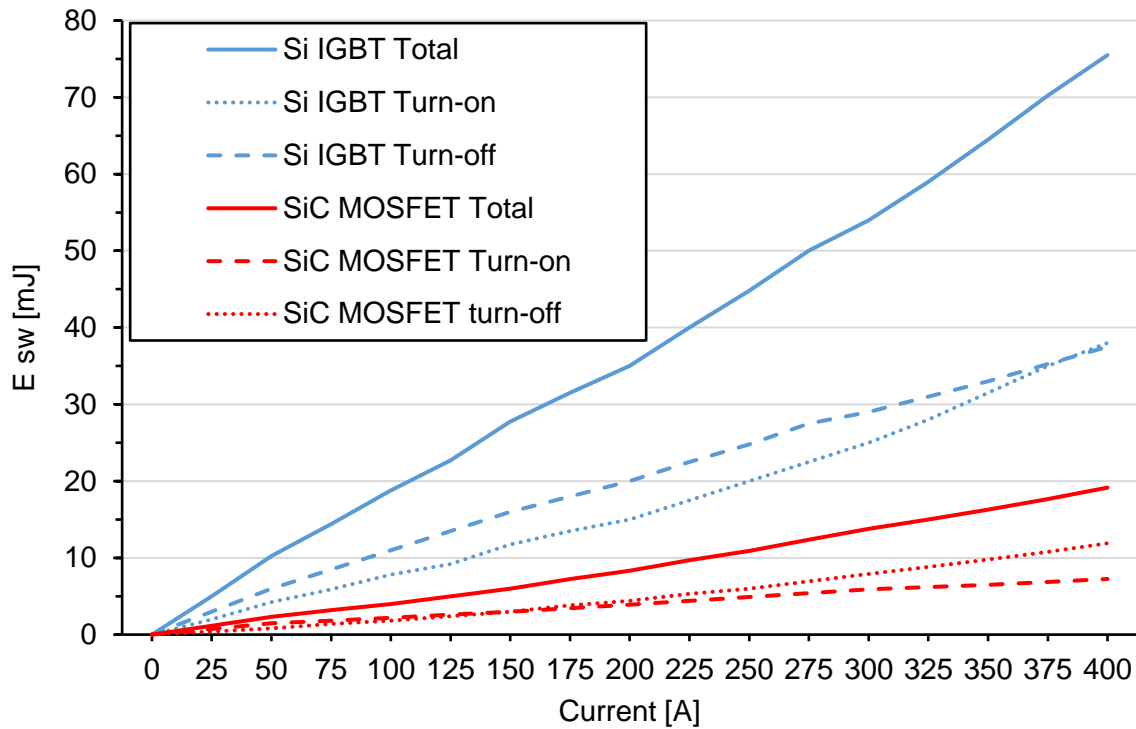
Figure 1. 18.

Si and SiC high power modules forward characteristics comparison.

### 1.4.2.2. SiC vs Si comparison in switching

Figure 1. 19 compares the forward characteristics of the selected high power Si and SiC modules. The main difference is the turn off, in where the SiC MOSFET does not suffer from any tail current. In the Si IGBT, the recombination of carriers results in a turn off 3.5 times slower. In addition, the gate charge is also 3.6 times higher for the Si IGBT. This characteristic makes the whole module slower.

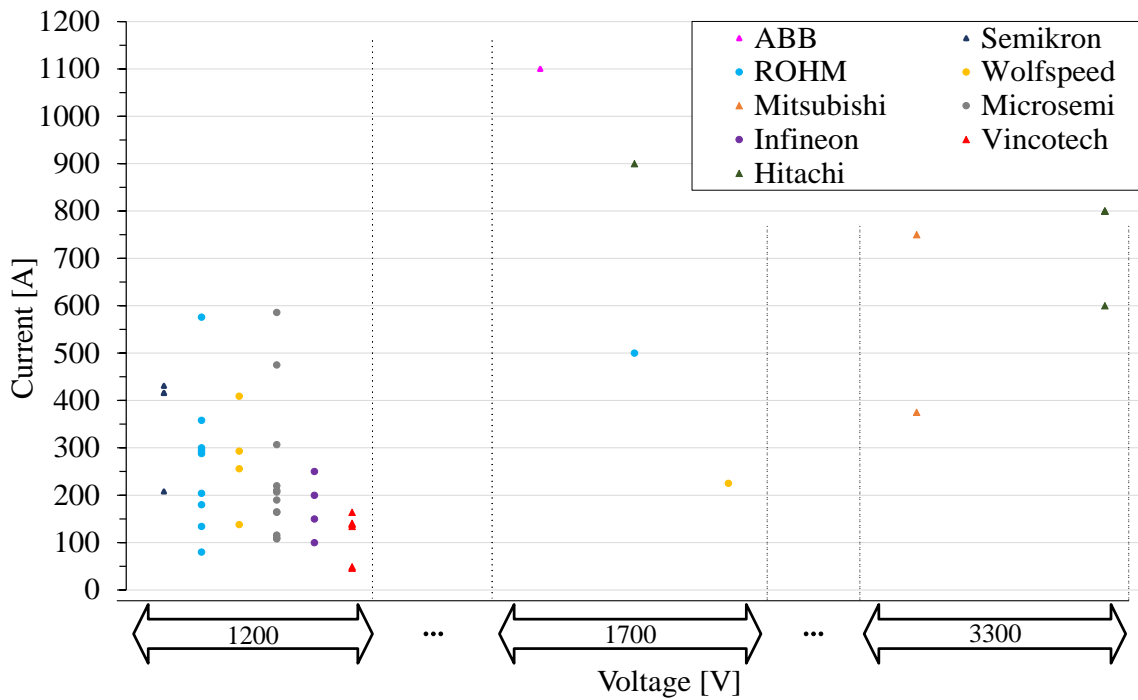
In addition, the Si fast recovery diode has a 32  $\mu\text{C}$  recovery charge while the SiC schottky diodes' total capacitive charge is 0.89  $\mu\text{C}$ . This allows the SiC schottky diode to switch faster and in a more efficient way than its Si counterpart. As a result, the SiC MOSFET is 4 times better in switching than the Si IGBT. Bringing high switching efficiency to high power applications is the most relevant contribution of high power SiC MOSFETs.



**Figure 1. 19.** Si and SiC high power modules switching characteristics comparison.

**1.4.2.3. Commercial high power SiC modules**

SiC high power modules market grew 28 % between 2016 and 2020, and is expected to grow 40 % during 2021 and 2022 [41]. In addition, SiC device manufacturers have doubled in the last years [42]. The SiC MOSFET is identified as the most promising transistor technology regarding active switches [41]. The half bridge modules, consisting of two MOSFETs are the most interesting modules to be used in renewable energies. Figure 1. 20 shows the available high power SiC MOSFET half bridge modules, highlighting the different manufacturers. Dots represent the product is in production, already available for industry, while triangles mean the product is still under development but is expected to be available soon.



**Figure 1. 20.** Commercial SiC MOSFET half bridge modules, in production (dots) and under development (triangles).

There are already various manufacturers involved in the SiC market. In addition, most of the products are available, or expected to be in production soon. Three voltage standards have been developed, based on the ones used for the Si IGBT technology. 1200 V is the one with the fastest development and the highest industrial demand.

The supply chain is very important for industry in order to have replaceable products. Equivalent modules with same package, developed by different manufacturers are specially interesting. Table II shows the package used by the commercialized high power half bridge modules, using SiC MOSFET technology. The manufacturers, together with voltage and current rating are also presented.

**Table II.**  
Commercial high power SiC MOSFET half bridge module packages.

Package	Voltage [V]	Current [A]		Manufacturer	
		From	To		
Easy Dual 1B	1200	100	100	Infineon	
SP1	1200	152	152	Microsemi	
Easy Dual 2B Flow Dual E2	1200	150	240	Infineon Vincotech	
C	1200	113	254	ROHM	
SP3F	1200	311	311	Microsemi	
HM	1200	362	362	Wolfspeed	
SP6	1200	242	828	Microsemi	
62 mm D3 Semitrans	1200 1700 2000	190	485	Wolfspeed Infineon Semikron Microsemi	
E G	1200 1700	300	600	ROHM	
LinPak LV-100 nHOD <sup>2</sup> or M-15 XHP2	1700 3300	375	1100	ABB Mitsubishi Hitachi Infineon	

Most of the packages are only commercialized by one manufacturer. The exception is the 62 mm package, which is used by several manufacturers. This makes it perfect for industrial applications. The same package is used for 1200 V and 1700 V, with current ratings up to 485 A. For high power, the LinPak package is presented. It is also used by several manufacturers but it is still under development and can only be found on demand. The target application of this module is railway traction drives.

### 1.4.3. High power silicon carbide applications

The market of SiC semiconductors is increasing exponentially since the early 2010s. However, this technology's massive adoption in industry is coming through the main market drivers [41]. These are expected to be solar PV, railway, motor drives and power supplies. Other applications like aerospace, which require high power density should also be mentioned.

#### 1.4.3.1. Distribution applications

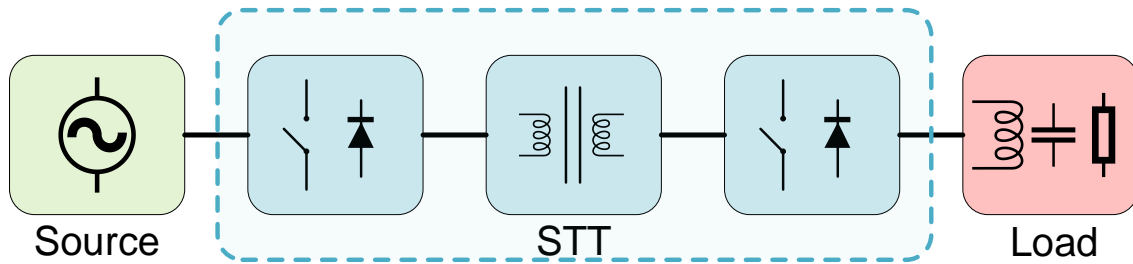
Power distribution nowadays is based on low frequency transformers (LFT) for voltage conversion [43]. Their operation frequency is 50 or 60 Hz, transforming the voltage from medium voltage (MV) levels (6-35 kV) to low voltage (LV) public grid (400 V). These LFTs are operated in fixed voltage and power conditions, making easy to optimize their designs [44].

The LFT technology is mature and well settled. This makes it relatively inexpensive, highly robust and reliable [44]. In addition, the efficiency levels of LFTs are extremely high, up to 99.5 %, mainly because no switched devices are used [45].

However, their performance is highly affected when operated outside their optimum operation point. Voltage drops can occur under heavy loads, and they suffer high power losses in no load operation. They are sensitive to load imbalances, and do not provide overload protection. Due to the oil used for insulation, overheating can lead to fire hazards, and environmental concerns arise with its use [44].

The power distribution model is expected to change in the near future. Renewable energies need to be integrated, together with energy storage systems. Intelligent loads will be introduced, with distributed generation and consumption, needing local autonomous controls. These new features will need bidirectional power flow, with high bandwidth controls and communications. This new concept is called "Energy Internet" [44]. The LFT is not suitable for all the new functionalities, so the solid state transformer (SST) is proposed to integrate the future power distribution system [44], [45].

The SST is the electronic system that replaces the voltage conversion of LFT by medium frequency transformers (MFT), with the use of switched power electronics, as seen in Figure 1. 21. It can also bring additional functionalities due to its extended features like controllability. It has received various names through history, depending on its functions [44].



**Figure 1. 21.**  
SST configuration [45].

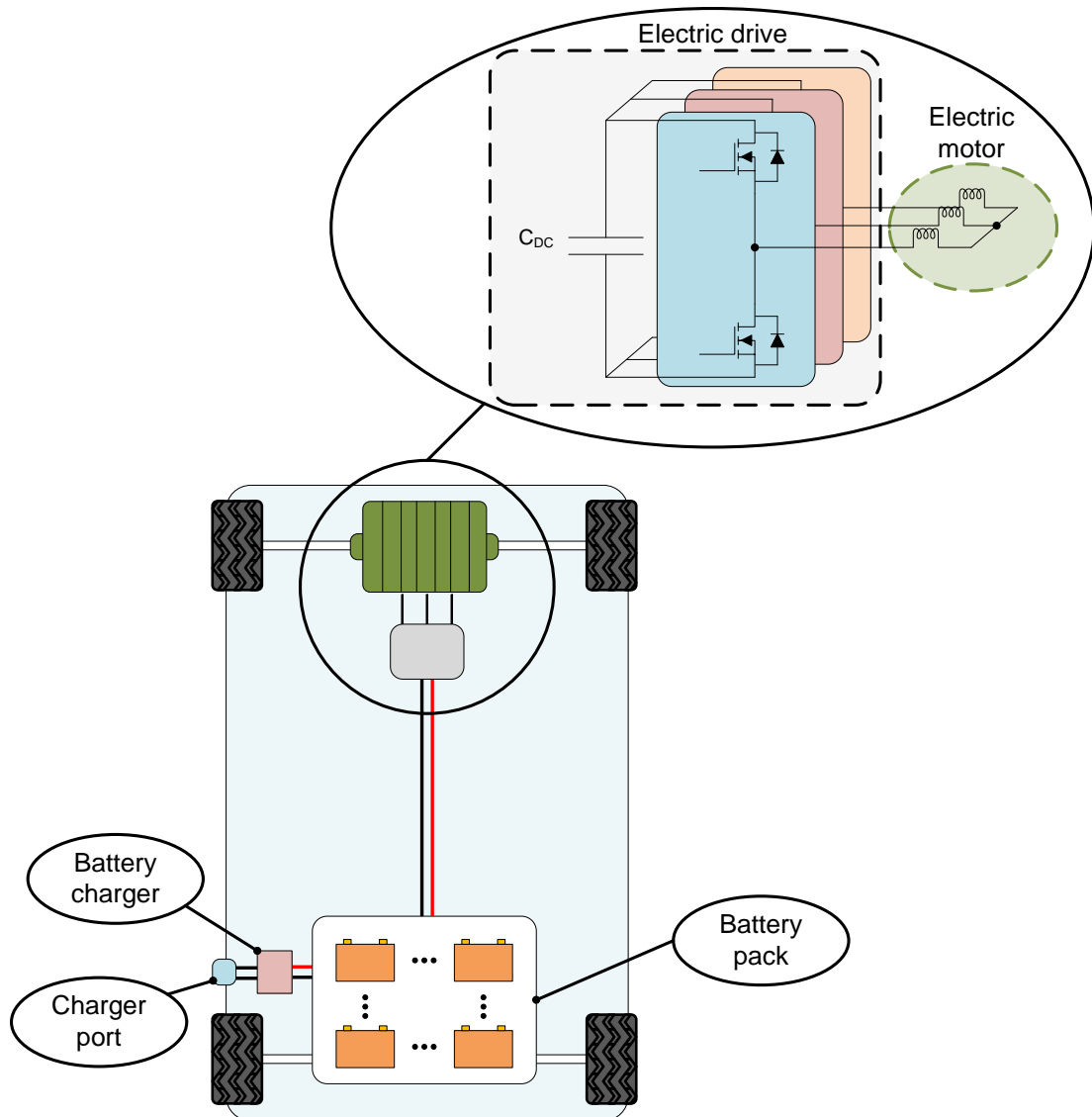
However, the use of switched devices increases the losses of the system, not being able to match the high efficiency of the LFT. Due to high component count, the reliability and the cost of the system is also a major concern [46]. Finally, the thermal stress can also cause a reduced operational life of the SST.

The use of SiC devices is considered to reduce the losses of the system [43]–[45], [47]–[51]. Hybrid Si and SiC SST configurations are also considered, using only SiC in the MV side, making the most of the voltage blocking capability of SiC [43]. SiC seems the perfect technology to overcome the challenges the SST is facing nowadays, and is going to be an enabling technology for the power distribution system transformation in the future.

There are already SiC based distribution system prototypes. For example, GE designed a SST for substation services in 2011. It is a 1 MVA three-stage configuration. It has a 13.8 kV rated voltage and is operated at 20 kHz switching frequency with a MFT. High 97 % efficiency is achieved without the need of oil, [45]. To do so, 10 kV and 120 A SiC MOSFETs are used. 25 % weight and 50 % volume reduction are achieved with respect to the current LFT based solution. The MFT is designed with Nano-crystalline core, obtaining a reduction of 75 % in weight and 50 % in volume. Even if no oil is used, the device is efficiently running at only few degrees more than the conventional system, [52].

#### 1.4.3.2. Electric vehicle

Current and future R&D in electric vehicle field should focus on the development and optimization of the electric drive, shown in Figure 1. 22, [53]. This statement is done based on the highly ambitious technological targets proposed by Horizon 2020, USCAR, DOE and UN ESCAP, which target an increase in power density, reduction in power losses, cost reduction, thermal management simplification together with size and weight reduction.



**Figure 1. 22**  
Electric drive systems' main components [53].

Battery voltage will not exceed 1.5 kV in the near future, varying around 300 and 870 V typically. This is because operational security requirements would change in higher voltages. It is clear that two level topology will be predominant due to its simplicity and cost effectiveness in the presented voltage levels. In addition, and due to weight and size requirements, high speed electric machines will be introduced in the automotive industry. This will lead to an increased switching frequency demand. This makes the reduction of switching losses mandatory in power electronics. Current Si semiconductors cannot achieve these figures, so SiC devices are introduced in the system [53]. The current development scenario is perfect for the introduction of SiC semiconductors in the automotive industry.

The significant benefits presented before will introduce some new and demanding challenges for engineers. Efforts should be made on mechanical designs, to ensure the thermal cycling can be supported by all the components surrounding the electric power train. In addition, the fast switching of SiC semiconductors can increase electromagnetic compatibility issues. This will force to make a layout revision and optimization. Concepts like symmetric designs, for modularity and scalable solutions will be convenient.

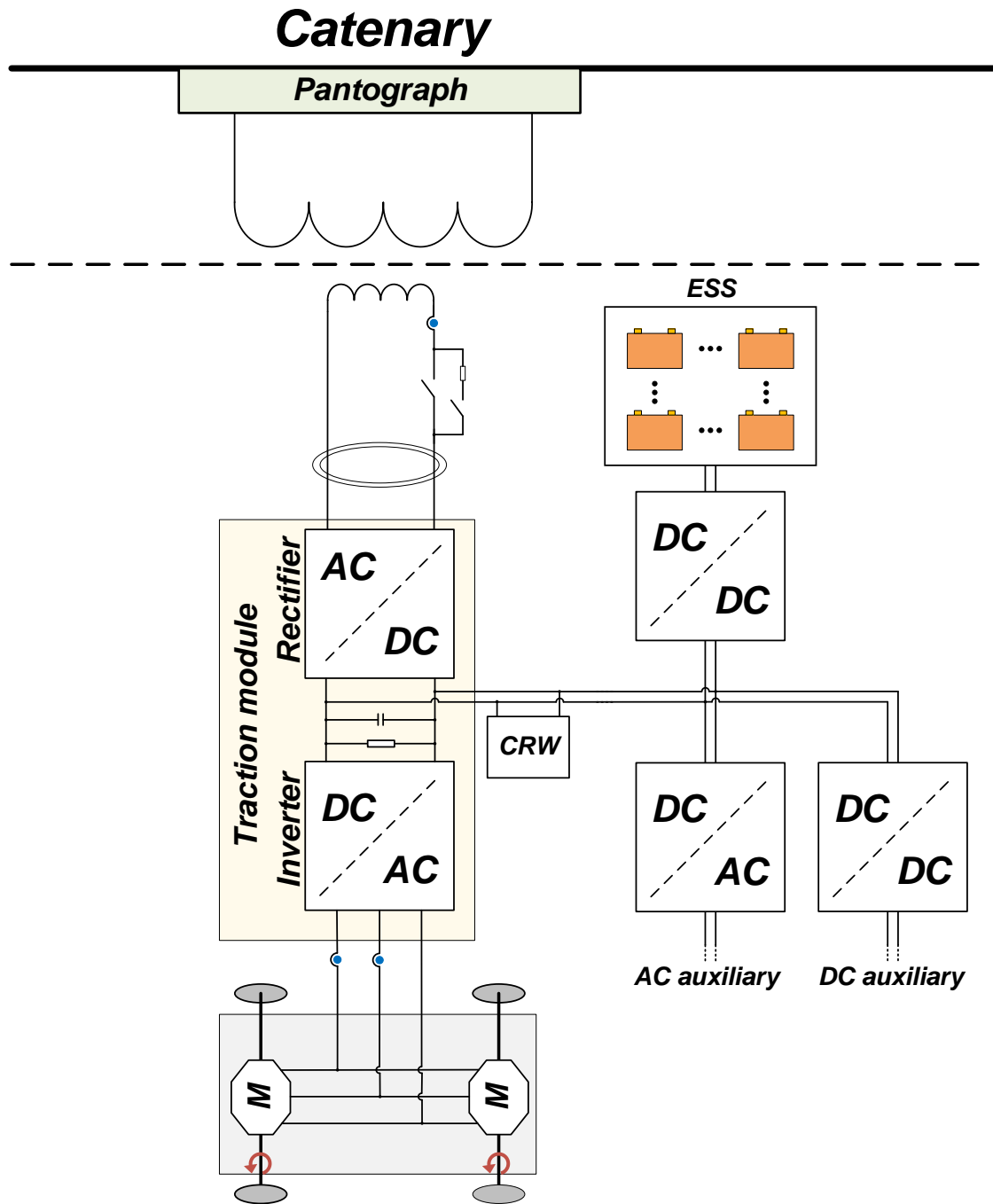
There are several automotive inverters with SiC already in the market. [54] presents a SiC based inverter for automotive applications. Its focus is to achieve high power density, reaching the value of  $34 \text{ kW/dm}^3$ . The switching frequency is 40 kHz. Fraunhofer Institute has also developed a full SiC inverter for automotive application [55]. The selected semiconductors are Cree's Gen2 1.2 kV SiC MOSFETs, switched at 100 kHz, achieving a power density of  $160 \text{ kW/dm}^3$ . In [56] a high efficiency SiC inverter for electric vehicle applications is presented. 99.5 % efficiency is achieved, with the use of 1.2 kV Cree SiC MOSFETs. The size is reduced by half, the peak loss to one third, and the average losses to one half, tested in an urban driving environment.

Finally, it is important to emphasize the fact that Tesla Model 3 is already using SiC MOSFETs for its main inverter [57]. ST Microelectronics was selected as the main supplier, thanks to its 650 V SiC MOSFETs. Tesla Model 3 manufacturing prediction reaches 38000 total units, and considering each Tesla Model 3 uses 24 SiC MOSFET modules, the demand is guaranteed. Indeed, Infineon is also expected to catch-up and become a second supplier for Tesla. This is a clear sign that electric vehicles will be one of the main driving industrial applications in the SiC semiconductor market. As mass production of electric vehicles adopt SiC semiconductor technology, the manufacturers will have to innovate and develop competitive SiC products to keep-up with the market competitiveness.

#### **1.4.3.3. Railway traction**

The load in railway traction can be single phase, with a variable consumption profile. In addition, AC and DC systems are combined, integrating energy storage systems, as shown in Figure 1. 23. The energy storage system (ESS) is typically based on on-board batteries, so a DC charger system is included. This converter must be bidirectional for regenerative operation modes. In addition, the railway electric system is a low voltage high current configuration, managing high power [58].





**Figure 1. 23.**  
Railway electric systems' main components.

The main challenge is to reduce the size and weight of traction inverters in railway [59]. This can be done replacing complex multi-level converters with simple 2 level topologies, reducing the power stage. Reducing the losses can also minimize the volume of the cooling system. Finally, reducing peripherals is also considered.

High voltage and current ratings are the principal characteristics SiC modules should have for their adoption in railway application [60]. 3.3 kV SiC modules should be used for 1.5 kV railway applications, while 6.5 kV SiC modules should be used in 3 kV catenaries [61]. Finally, manufacturers are selecting the 100x140 mm<sup>2</sup> package to develop Si IGBTs, hybrid SiC and full SiC MOSFETs.

Even if the same package is used for the three different technologies, the switching

characteristics are completely different, so each technology should be designed accordingly [61]. In addition, SiC modules need paralleling to reach high current [62]. The power circuits, capacitors, busbars, gate drivers, cooling systems and layouts must be optimized.

Several power converters have been implemented with SiC for railway application to date. There are three different approaches. The first option is to incorporate it in the auxiliary inverter. The second one is to use it in the DC-DC converter that controls the energy storage system (ESS). The third is to incorporate it in the traction inverter.

Mitsubishi delivered the first SiC auxiliary power supply for traction, and is operated in the Tokyo metro [63]. It achieves 30 % loss reduction, together with 20 % size and 15 % weight reduction. ALSTOM also designed a SiC auxiliary inverter that operates in the Milan metro [64]. 1.2 kV Cree SiC MOSFETs are used, switching at 15 kHz and using only air cooling. The DC-DC converter managing the ESS in a tram without catenary is designed with CREE's 1.7 kV SiC MOSFETs in [65]. 70 % inductor, 40 % cooling system and 30 % total volume reduction is achieved.

CAF improved the efficiency of the main inverter 4 %, reducing the weight 15.7 % with the use of SiC [61]. The design uses 3.3 kV and 450 A Hitachi hybrid SiC modules. 3.3 kV and 1200 A hybrid SiC Hitachi modules are also used in [66]. The converter achieves 35 % loss reduction as well as 60 % weight reduction. Mitsubishi used full SiC MOSFETs to obtain 65 % total weight reduction in their propulsion system [67]. Finally, Bombardier tested a full SiC inverter in Stockholm between 2017 and 2018 [68]. They reported 35 % energy reduction with 19 dB noise reduction. The full SiC inverter is 51 % smaller and weighs 22 % less than the reference Si inverter. SiC application is already a reality in railway traction.

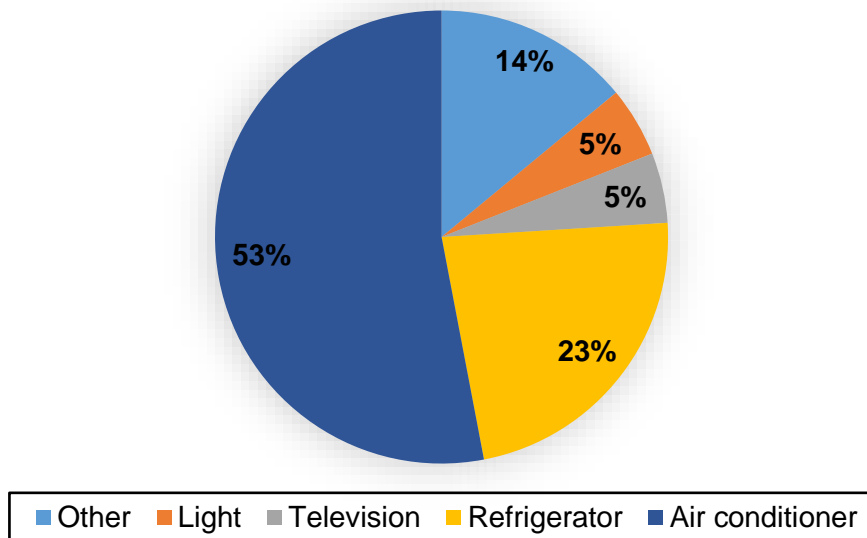
#### 1.4.3.4. Aerospace

The more electric aircraft (MEA) is a wide research field related to aerospace [69]. It is based on changing the mechanic and hydraulic actuators around the airplanes by electric drives. MEA improves fuel efficiency, as well as reducing the maintenance costs of the previous systems [70]. Most of the introduced electric systems are DC-AC converters with power ranges around several kW. Fundamental output frequency of these systems is usually 400 Hz. Their main requirement is to obtain a minimized size and weight, achieving high efficiency to reduce fuel burn [69]. Another particular characteristic is the physical envelope requirements for the converters. This is due to the obligation to insert the converters in a fixed space inside the aircraft [71]. The reduced losses and cooling needs, together with the capability to operate at high switching frequencies make SiC a good candidate to use in aerospace [69].

There are several operating products such as the 50 kW 3 phase 2 level inverter designed for power density [72]. It achieves 97.8 % efficiency switching at 100 kHz. A 50 kW SiC active rectifier is also used to generate the DC distribution line in the MEA [73]. It achieves 2.6 % higher efficiency than Si, switching at 30 kHz. Finally, a 13 kW 2 level inverter is presented using SiC to optimize power density [71]. It achieves 17.5 kW/dm<sup>3</sup> power density with 97.6 % efficiency. This converter is introduced inside a restricted envelope.

#### 1.4.3.5. Home appliances

Power factor correction (PFC) circuits are in the input of most home appliances, and suffer from high losses [42]. Reducing the losses in this stage is key to improve the electronics in home appliances. In addition, Figure 1. 24 shows the air conditioner is the biggest consumption element in homes.



**Figure 1. 24.**  
Power consumption rate of home appliances [74]

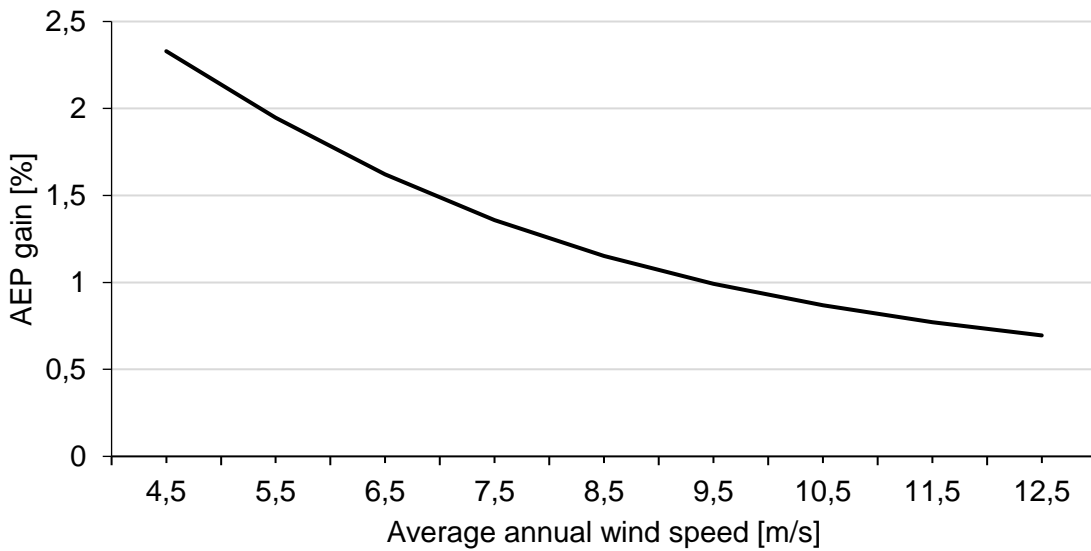
SiC can reduce the losses in PFC circuits, as well as in the compressor inverter of the air conditioning [74]. However, the high  $dV/dt$  of SiC MOSFETs can affect the electromagnetic compatibility (EMC) of the systems [75]. Layouts must be optimized to prevent this issue. In addition, the cost difference with Si IGBTs in the 600 V range is a major concern for SiC application [76].

Some products are already using SiC MOSFETs in the PFC stage. 50 % loss reduction is reported in [75]. [77] reduces turn off losses from 31 to 8 W switching from Si to SiC. In [74], 60 % of the total losses are reduced in the air conditioning using hybrid SiC. Mitsubishi presented a full SiC module for air conditioning applications in 2014 [78]. 45 % loss reduction is reported in the PFC stage. The use of SiC in the induction heating is also studied in [77], [79], [80]. Finally, light emitting diodes (LED) lighting application is studied achieving 94 % efficiency with SiC MOSFETs [81].

#### 1.4.3.6. Wind energy

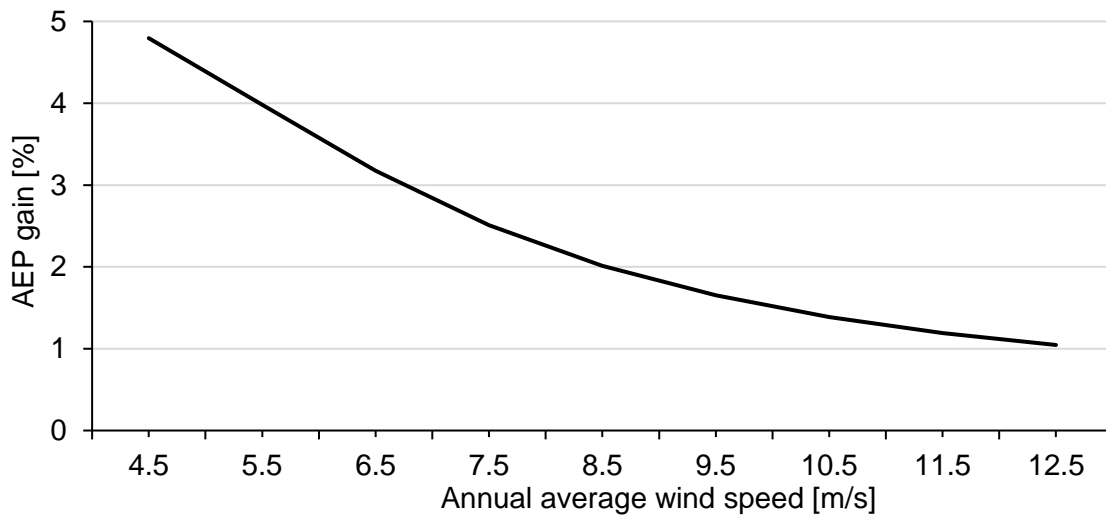
The study in wind energy is only based on simulation work. The characteristics of wind energy systems are presented in Section 1.3. The main parameter to optimize is the LCoE, but other variables can also have a positive impact in the system. The most important one is the cost of the system. Another one is increasing the annual energy production (AEP) by improving the efficiency of the system. Finally, reducing weight or volume can also improve the current solution.

By using SiC MOSFETs in a DFIG system the converter volume is reduced 48 % [82]. The efficiency is increased 1.6 % even if the switching frequency is also increased. As seen in Figure 1. 25, AEP is increased 0.99 % in ideal locations for wind energy systems (9.5 m/s average annual wind speed) [83].



**Figure 1. 25.**  
AEP gain depending on the annual average wind speed of the location for SiC technology [83].

16 % total volume reduction is achieved in a 1.12 MW FC by using SiC diodes [84]. The switching frequency is increased from 1.5 to 3 kHz. Higher efficiency is also achieved with SiC MOSFETs in a 1.5 MW FC [85], [86]. The efficiency is improved 0.6 % with hybrid SiC modules in a 2.3 MW FC [87], [88]. The selected topology for this study is 3 level NPC. Figure 1. 26 shows the AEP improvement that can be achieved using SiC MOSFETs in a 5 MW FC. The gain can be as high as 1.65 % in ideal locations (9.5 m/s average annual wind speed).



**Figure 1. 26.**  
AEP gain percentage depending on the average annual wind speed of the location for SiC, using as reference the currently used Si IGBTs [89].

However, the effect of the cost difference between SiC and Si on the LCoE is negative. If the before mentioned benefits overcome the cost difference is still to be defined. Vestas makes an analysis of LCOE of wind energy, depending on the cost difference between Si and SiC semiconductors, for different power levels [90]. This analysis is done representing value bands, according to possible variations data can suffer [91]. Three scenarios are considered. The first one is making SiC semiconductors cost equal to Si IGBTs. The second

one is to consider the SiC cost is three times higher than the Si IGBTs. The last and worst case scenario is to consider the SiC cost is five times higher than Si. This scenario is the closest one to reality nowadays.

Vestas concludes limited gain can be achieved if SiC semiconductors are introduced in a low voltage system. If the Si and SiC prices are made equal, maximum 1 % LCoE gain can be achieved, improving the current LCoE in every power level. A break-even point in power is found at 5 MW if the SiC cost is three times higher than Si. Considering the SiC cost is five times higher than Si, no power level improves the current LCoE. However, this study is limited to one product. Not enough information about topologies or the overall system is given. Individualized study should be done for different companies and products, also considering several converter topologies.

## 1.5. Objectives

The main goal of the thesis is to achieve performance improvement of the state of the art power electronics of wind energy. To this end, the use of silicon carbide semiconductors, optimized voltage levels and multilevel topologies have been considered promising options. The proposed solution should improve the LCoE, or another technical parameter. However, a tradeoff between key parameters can be found. For this, the following objective is proposed to carry out this thesis.

**Find, design, implement and test a semiconductor, voltage level or topology power electronics converter configuration to improve wind energy systems.**

To achieve the final main objective, the following sub objectives are defined.

- Develop a tool that calculates the LCoE of different converter configurations of wind energy.
- Select the most promising configurations for wind energy business, for further analysis.
- Design and implement a scale test bench for wind energy converters.
- Compare experimentally the selected business cases.
- Identify the restrictions and main challenges of high power SiC modules.

## 1.6. Outline of the thesis

**Chapter 1:** The first chapter presents an overview of renewable energies worldwide, with economic details. It shows wind energy configurations and the power electronics that are actually used. Next, it introduces the LCoE concept. Silicon carbide semiconductors, are presented, showing their physical characteristics, high power SiC semiconductors, the commercial modules and their applications are also shown. Finally, the objectives, the scientific contributions and the achieved publications are listed.

**Chapter 2:** The second chapter presents the developed LCoE calculation tool with the models used in the algorithm. Next the technique used to optimize the algorithm is presented. The results with current and future scenarios are shown, together with the business case selection considering commercial indicators.

**Chapter 3:** The third chapter shows the test bench designed for the business case validation. It presents the specific designs, including 2 and 3 level busbars.

**Chapter 4:** Next, the different business cases are tested in the laboratory prototype, and using the experimental results, the LCoE calculation tool results are validated.

**Chapter 5:** The fifth chapter present the challenges of SiC in high power. Different limiting phenomenon are analyzed and modeled. Solutions are offered to overcome the challenges.

**Chapter 6:** The last chapter presents the conclusion and the future research lines.

## 1.7. Scientific contributions

- **Analysis of the impact of high power SiC modules in the wind energy systems' LCoE:**

First the analysis is done theoretically using the self-programmed LCoE calculation tool. This analysis considers several configuration parameters, provided by the industrial partner, combining technical and economical data. Next, the theoretical results are validated comparing them to the results in the laboratory prototype. Only the converter cost is used for this analysis.

- **Identification, analysis and prevention techniques of the main challenges of the application of high power SiC modules:**

This work identifies the major challenges high power engineers will face when starting to develop their first designs with high power SiC modules. The presented simple models help the understanding of the undesired issues, and the prevention techniques proposed in the work will save the engineers time when addressing the issues, showing the correct direction to solve them.

- **Design process and validation by impedance measurement and switching waveform analysis of an optimized busbar for the fast switching of 3L converters with high power SiC modules:**

An experimental example of how to solve one of the above mentioned challenges (the overshoot) is given in this work. The design techniques are tested with inductance measurement using an impedance analyzer, as well as analyzing the switching waveforms. This design should be a reference design for engineers, and validates the prevention techniques proposed in this work.

## 1.8. Publications

### 1.8.1. Conference papers

Antxon Arrizabalaga; Aitor Idarreta; Mikel Mazuela; Iosu Aizpuru; Unai Iraola; José Luis Rodriguez; Daniel Labiano; Ibrahim Alişar; "Impact of silicon carbide devices in 2 MW DFIG based wind energy system".

In 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), 2020.

Antxon Arrizabalaga; Mikel Mazuela; Aitor Idarreta; Unai Iraola; Iosu Aizpuru; José Luis Rodriguez; Daniel Labiano Andueza; İbrahim Alişar; "Integration of Silicon Carbide devices to increase the AEP (Annual Energy Production) in a PM based wind generation system".

In 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2020.

Antxon Arrizabalaga; Mikel Mazuela; Aitor Idarreta; Unai Iraola; Iosu Aizpuru; “System Level Optimization of 5 MW Wind Converter using 3L-NPC Topology in Medium Voltage with 1.7 kV IGBT”.

In IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, 2020.

Antxon Arrizabalaga; Mikel Mazuela; Aitor Idarreta; Unai Iraola; Iosu Aizpuru; José Luis Rodriguez; Daniel Labiano Andueza; İbrahim Alişar; “Integración de Carburo de silicio para aumentar el AEP de sistemas de generación eólica basados en DFIG”.

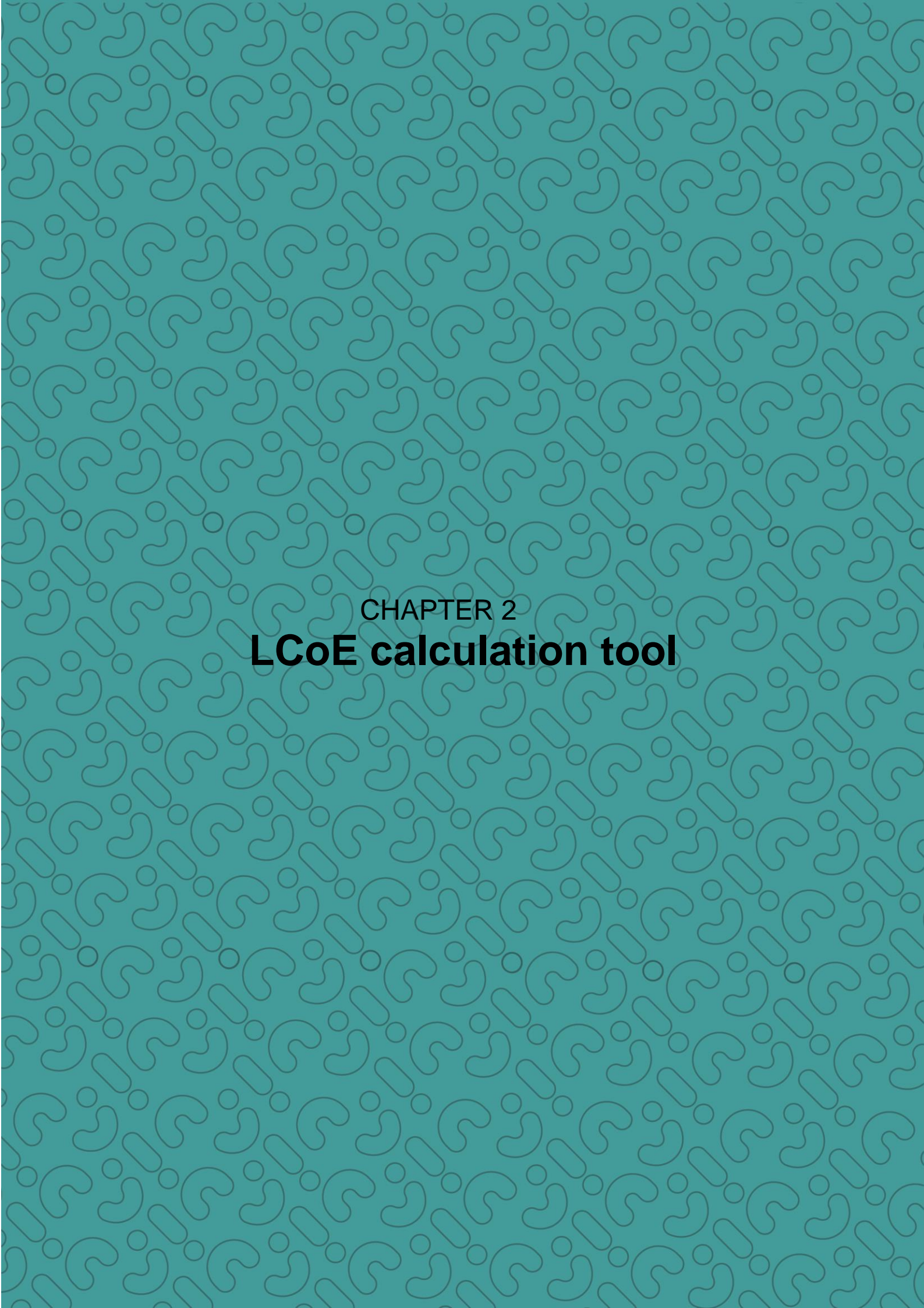
In 27th Annual Seminar on Automation, Industrial Electronics and Instrumentation (SAAEI), 2020.

Antxon Arrizabalaga; Mikel Mazuela; June Urkizu; Jon Aztiria; “SiC erdieroaleak energia eolikoan LCoEa hobetzeko”.

In IV. Ikergazte. Nazioarteko ikerketa euskaraz, 2021.

Antxon Arrizabalaga; Mikel Mazuela; Iosu Aizpuru; June Urkizu; Jon Aztiria; “Benefits of switching from Si to SiC modules with further converter optimization”.

In 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), 2022.



CHAPTER 2  
**LCoE calculation tool**



## 2.LCoE calculation tool

This chapter presents the LCoE calculation tool developed to analyze the impact of SiC semiconductors in wind energy. First, the objective and approach of the tool are presented. Next, The LCoE equation, and the algorithm itself are shown. Finally, the chapter is concluded by showing the optimization performed to the tool, and the obtained results.

### 2.1. Objective and approach

#### 2.1.1. Objective

One of the main indicators that provides a good representation of the optimization of a renewable energy source is the LCoE, since it takes into account both its performance and the capital and operation costs.

In order to understand the variables and parameters involved in the LCoE and to find the best wind energy system (WES) configurations, an LCoE calculation tool is programmed in Matlab. The objective of the tool is to calculate and compare the LCoE of different wind energy systems configurations. The most promising configurations are identified to later test in the laboratory. Wind energy configurations, power converter topologies and semiconductor technologies, as well as voltage ratings are compared.

#### 2.1.2. Approach

Different models and databases are developed to calculate all the required information. In addition, the models must be accessible to the user. By doing so, a fast change can be easily applied, in case the cost of a given component has notoriously changed, for example. This allows easy evaluation of the effect of a certain change. Finally, databases must be adaptable, in case a new semiconductor comes to the market, for example. The algorithm runs iteratively with the LCoE equation its heart, while calculation models and functions feed the needed data.

## 2.2. LCoE calculation equation

The LCoE calculation equation varies from one company to another. In addition, depending on the region or the goal of the analysis, different expressions can be used, considering the most appropriate data in each case. However, the same equation needs to be used in the tool for each configuration, in order to perform a fair comparison.

The equation used in this work is provided by our industrial partners. The current product of the company is considered the baseline, and is used to check the accuracy of the calculations. In addition, the tested configurations are compared to the baseline, in order to evaluate them.

$$\frac{[(WTG_{cost} + BOP) * FCR + Opex] * 1000 * (1 + Comp_{margin})}{Weighted AEP * (1 - Losses)} \quad (1)$$

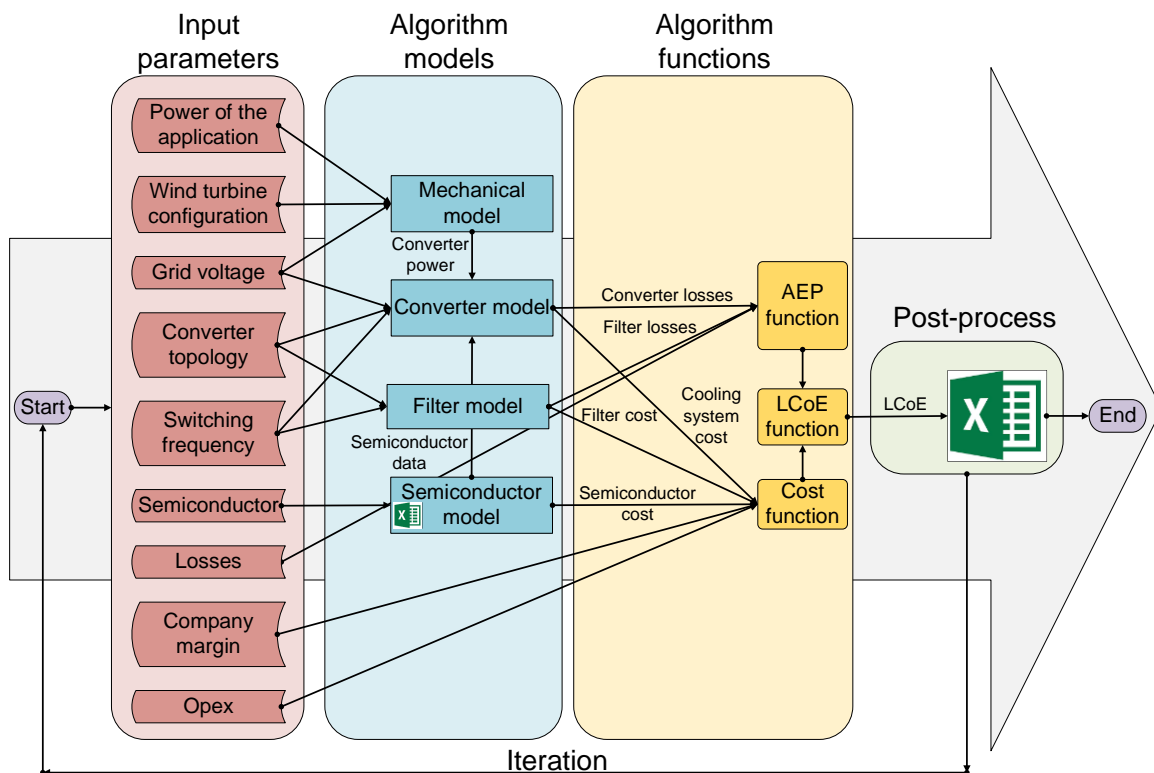
Being the parameters in (1) the following:

- $WTG_{cost}$ : Wind turbine and generator cost.
- $BOP$  (Balance of plant): Civil engineering cost.
- $FCR$  (Fraction of capital cost per year): Annual cost related to taxes.
- $Opex$  (Operation expenditure): Annual maintenance cost. Including unexpected failures.
- $Comp_{margin}$ : Expected benefit percentage per wind turbine for the company.
- $Weighted\ AEP$  (Annual energy production): Averaged ratio of AEP depending on the wind distribution of the location.
- $Losses$ : Losses related to unexpected operation stoppages due to failures. Expressed in a percentage of the AEP.

The economic data in this analysis are provided by the industrial partner. They are adapted to fit the calculated value to the baseline's LCoE.

### 2.3. Calculation algorithm

The designed LCoE algorithm is programmed in MatLab and shown in Figure 2. 1. In order to calculate several configurations' LCoE, the tool is designed to be iterative. A single input variable is changed each iteration. The results are stored in an Excel file to post process.



**Figure 2. 1.**  
LCoE calculation algorithm.

The start and end of the algorithm in Figure 2. 1 are represented in purple. The input parameters are represented in red. The boxes represent calculations, functions or models. Arrows show connection between blocks, and the flow of the algorithm. The main calculation is done in the LCoE calculation function, which is fed by the weighted AEP and the system total cost.

### 2.3.1. Input parameters

The input parameters are considered those that can be selected by the user, and not calculated by the algorithm. Depending on the selected input parameters, a configuration is formed. The algorithm goes through the models, calculating the characteristics of the configuration, getting the LCoE of it. Then, an input parameter is changed, and a second iteration starts. The variation of a single input parameter defines a new configuration, which will be analyzed by the tool.

#### 2.3.1.1. Power of the application

5, 8 and 10 MW applications are analyzed. This affects the power of the converter, and consequently the number of required semiconductors. All the components should be rated according to the selected power. Even if the baseline is 5 MW the effect of increasing the power of the application is also studied.

#### 2.3.1.2. Wind turbine configuration

DFIG and FC configurations are considered. Depending on the configuration, the power converter is rated accordingly. The cost of the generator is also affected by the configuration.

#### 2.3.1.3. Grid voltage

690, 900, 1375, 2850 and 3300 V<sub>AC</sub> grid voltages are considered. The voltages over 1000 V<sub>AC</sub> are high voltages, which cannot be used with DFIG configuration. The voltage levels are selected according to existing standards in industry, but also considering semiconductor voltage limits. The calculation is further explained in this section, together with the semiconductor technology and voltage rating.

Each grid voltage requires a certain DC-link voltage. This is determined by (2), in where  $m_a$  is the modulation index (3).

$$V_{DC} = \frac{V_{grid,ll,rms} \cdot \sqrt{2}}{m_a} \quad (2)$$

$$m_a = \frac{V_{conv,ph,max}}{V_{DC}/2} \quad (3)$$

For safety and voltage margin purposes, the maximum modulation index is set to 0.9, resulting in the DC voltages shown in Table III, assuming conventional inverters.

**Table III.**

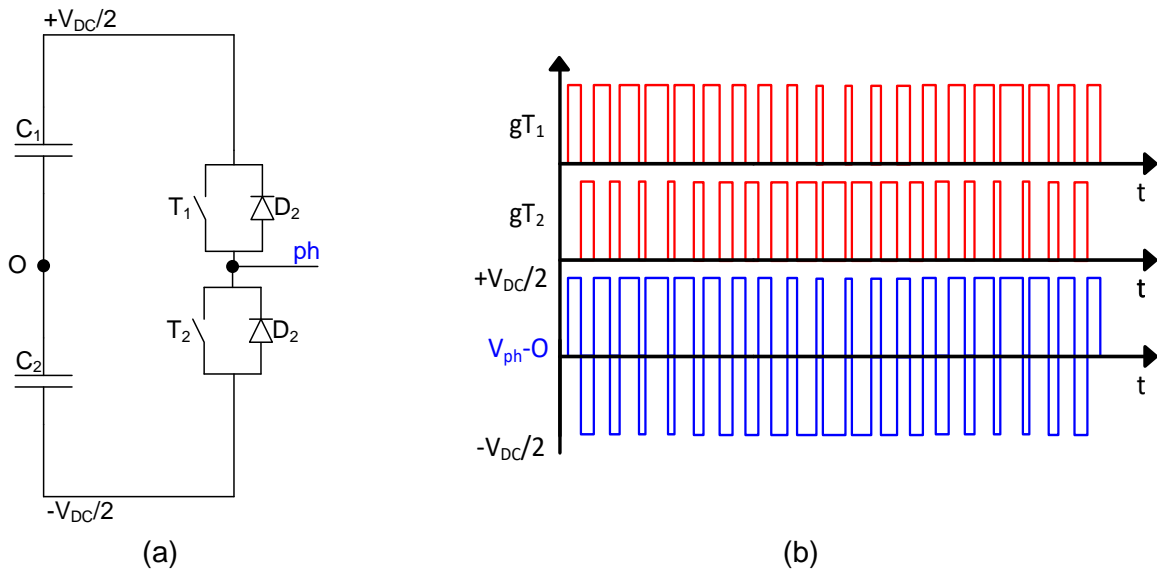
Required DC voltage for each grid voltage.

Grid voltage [V <sub>AC</sub> ]	Required DC-link voltage [V <sub>DC</sub> ]
<b>690</b>	1085
<b>900</b>	1415
<b>1375</b>	2160
<b>2850</b>	4480
<b>3300</b>	5185

**2.3.1.4. Converter topology**

The selected topology highly influences the semiconductor number and voltage rating, together with the losses and required filters. This work considers two (2L) and three level (3L) topologies. A review of the considered topologies is done next.

The 2L topology shown in Figure 2. 2 is the simplest DC-AC converter topology. It uses two semiconductors so there is only one switch in the current path. This achieves low conduction losses. However, each switch needs to block the whole DC voltage. This results in higher voltage stress and switching losses compared to more complex multilevel topologies. The switching states of the topology are shown in Table IV.

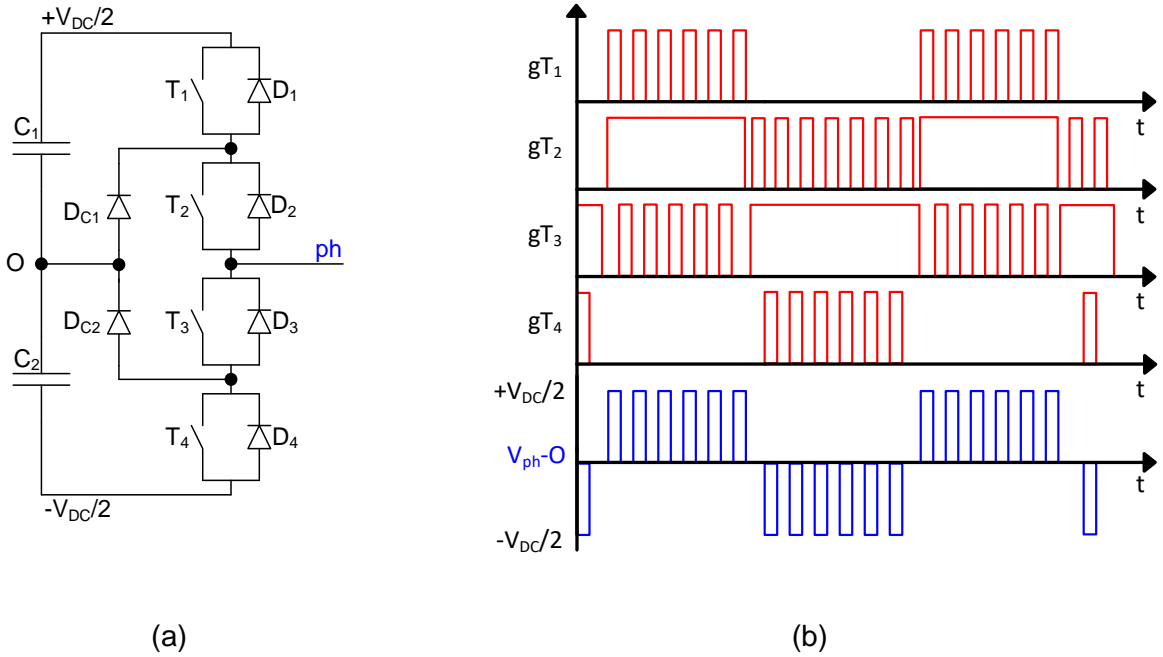


**Figure 2. 2.** 2L topology, (a) phase branch diagram, (b) gate orders ( $g_{T1}, g_{T2}$ ) and phase voltage ( $V_{ph-o}$ ) waveforms.

**Table IV.** 2L topology switching states.

State	$V_{PH-O}$	$T_1$	$T_2$
1	$+V_{DC}/2$	1	0
2	$-V_{DC}/2$	0	1

The 3L topology in Figure 2. 3 is the well-known three level neutral point clamped (3L NPC). An additional output voltage level is obtained with the clamping diodes. Each semiconductor blocks half of the DC voltage ( $V_{DC}/2$ ), so the switching performance is improved. In addition, the voltage rating of the semiconductors can be reduced compared to an equivalent 2L converter. Table V shows the switching states of the 3L NPC topology. In this configuration, there will always be two semiconductors in the main current path, penalizing the conduction losses.

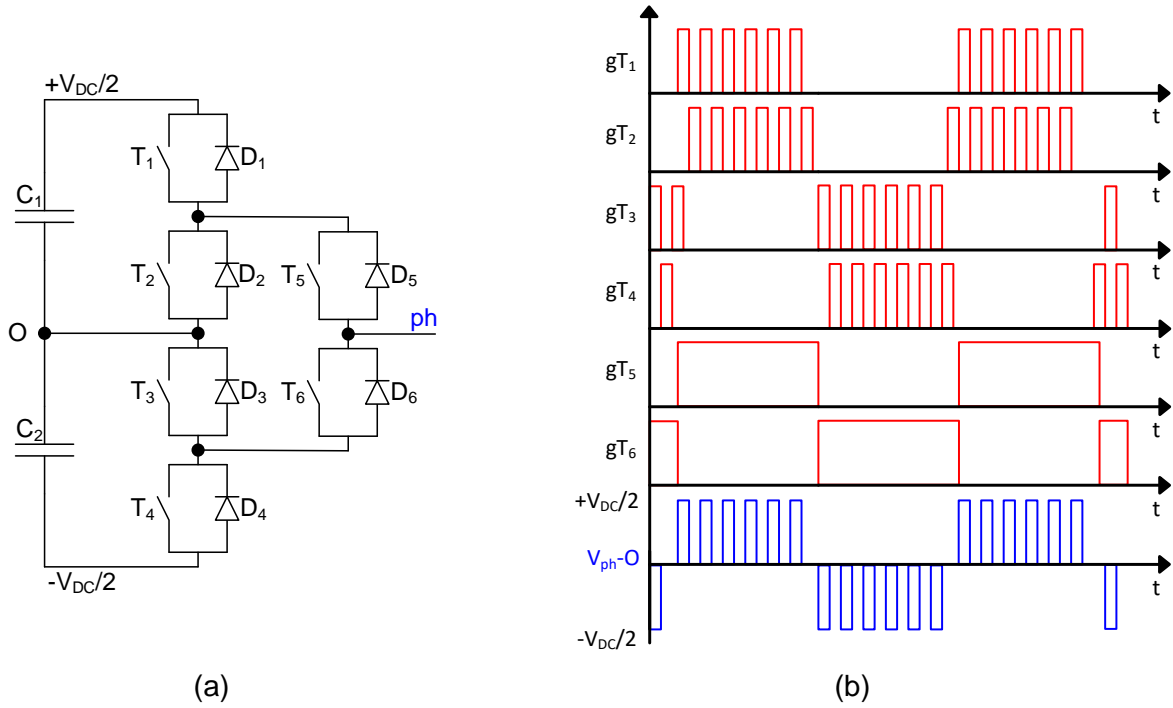


**Figure 2. 3.**  
3L NPC topology, (a) diagram, (b) waveforms.

**Table V.**  
3L NPC topology switching states.

State	$V_{PH-O}$	$T_1$	$T_2$	$T_3$	$T_4$
1	$+V_{DC}/2$	1	1	0	0
2	0	0	1	1	0
3	$-V_{DC}/2$	0	0	1	1

The natural evolution of the 3L NPC topology is the active NPC (ANPC), shown in Figure 2. 4. The clamping diodes are replaced by active switches, which provide extra switching states. In addition, the forward voltage drop in the conduction of the diodes is avoided. Table VI presents the switching states of the 3L ANPC topology, with the redundant states that give a degree of freedom. Using the redundant switching states, an improved switching pattern can be generated, which controls the power losses distribution among semiconductors, for example. In addition, with the appropriate switching pattern, two switches are only commutated at fundamental frequency, reducing the total switching losses of the topology. Each switch blocks only half of the DC voltage ( $V_{DC}/2$ ), achieving the same benefits as the 3L NPC.



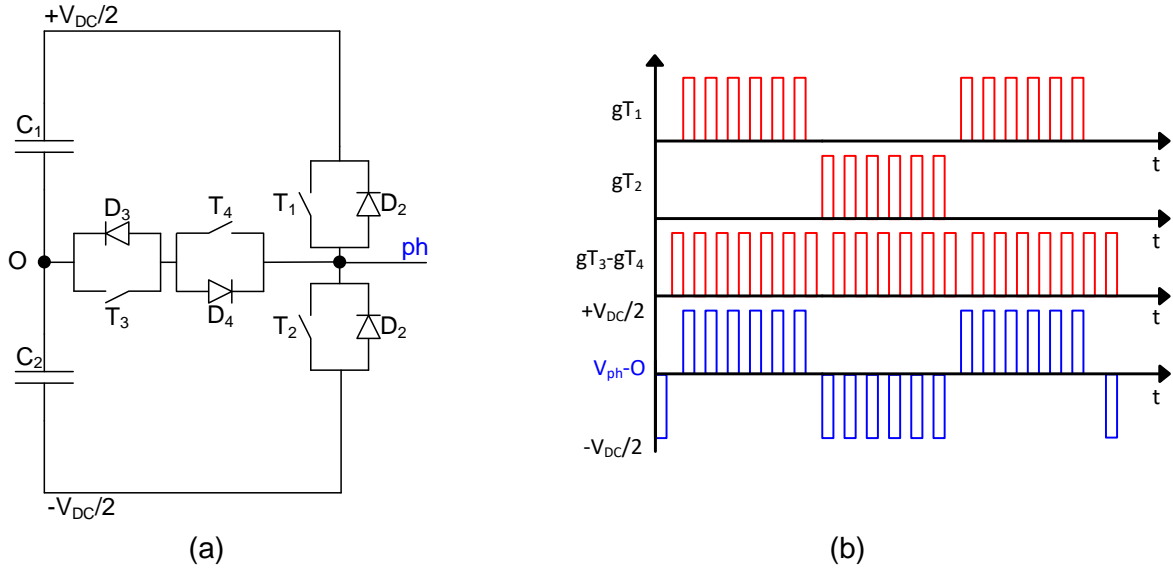
**Figure 2. 4.**  
3L ANPC topology, (a) diagram, (b) waveforms.

**Table VI.**  
3L ANPC topology switching states.

State	$V_{PH-O}$	$T_1$	$T_2$	$T_3$	$T_4$	$T_5$	$T_6$
1	$+V_{DC}/2$	1	0	0*	0	1	0
2	0	0	1*	1*	0	1*	1*
3	$-V_{DC}/2$	0	0*	0	1	0	1

\*Degree of freedom to select switching strategy

The final topology considered is the three level neutral point piloted (3L NPP), shown in Figure 2. 5. It is also called T-type topology. The 3L NPP replaces the clamping diodes in the NPC with a bidirectional switch, still achieving three voltage levels in the output. At a glance, the required number of semiconductors (4 active switches) is reduced compared to the 3L-NPC (4 active switches and 2 diodes). Nevertheless, in a fairer comparison, the same number of semiconductors is needed (6 active switches) if the same voltage rating devices are considered, because  $T_1$  and  $T_2$  have to block the total DC-link voltage ( $V_{DC}$ ). The switching states of this topology are shown in Table VII.



**Figure 2.5.**  
3L NPP topology, (a) diagram, (b) waveforms.

**Table VII.**  
3L NPP topology switching states.

State	$V_{PH-O}$	$T_1$	$T_2$	$T_3^*$	$T_4^*$
1	$+V_{DC}/2$	1	0	0	0
2	0	0	0	1	1
3	$-V_{DC}/2$	0	1	0	0

\*Degree of freedom to select the switching strategy

The baseline solution is based on 2L topology. It is the cheapest, but the efficiency of the system is penalized in high power. 3L topologies are interesting because the filtering requirements are reduced due to the extra output voltage level. This brings a cost reduction in the output filter. Whether the extra semiconductor cost is compensated by the system benefits in efficiency and improved output waveform with three level topologies is a relevant investigation.

Higher level topologies are not considered for this work, as the increased complexity and semiconductor number does not fit the wind energy application. More complex 3L topologies such as the flying capacitor are not considered for the same reason.

**2.3.1.5. Semiconductor**

Silicon (Si) and silicon carbide (SiC) semiconductors are considered. Even if initially hybrid Si-SiC modules were also considered, they were discarded due to the limited availability in the market. The selected modules are half bridge modules, shown in Table VIII. The voltage standards are 1.2, 1.7 and 3.3 kV. The baseline configuration uses 1.7 kV Si IGBTs. In order to guarantee the supply chain, two manufacturers have been considered when possible.

**Table VIII.**

Considered semiconductors.

		1.2 kV	1.7 kV	3.3 kV	
Si IGBT	Ref	SKM1400 GB12P4	SKiiP2414GB1 7E4DUW V2*	MBM1000F S17G	SKM450G B33F
	Manufacturer	Semikron	Semikron	Hitachi	Semikron
	Current rating	1400 A	2400 A	1000 A	450 A
SiC MOSFET	Ref	FMF600D X2-24A	MSM900FS17 ALT	CAS300M1 7BM2	MSM600F S33ALT
	Manufacturer	Mitsubishi	Hitachi	Cree	Hitachi
	Current rating	600 A	900 A	300 A	600 A

\*Reference used by the baseline

The number of semiconductors used in each configuration depends on the power of the application, the grid voltage, the converter topology and the selected semiconductors voltage and current ratings. Manufacturers recommend using semiconductors at a switching voltage below the rated voltage. A good reference is the  $100_{FIT}$  parameter, which represents the voltage level at which the semiconductor will fail 100 times in  $10^9$  hours [92]. Table XIII shows the  $100_{FIT}$  parameter for each semiconductor voltage standard. However, the baseline is operated at what it has been referred as *Ambitious  $100_{FIT}$* , which exploits the switching voltage capability of semiconductors beyond the typical  $100_{FIT}$ . An ambitious  $100_{FIT}$  is estimated and presented in Table IX for each voltage standard.

**Table IX.**Considered  $100_{FIT}$  and ambitious  $100_{FIT}$  values for each semiconductor voltage standard.

	1.2 kV	1.7 kV	3.3 kV
<b><math>100_{FIT}</math> [V<sub>DC</sub>]</b>	600	900	1800
<b>Ambitious <math>100_{FIT}</math> [V<sub>DC</sub>]</b>	800	1200	2500

Semiconductors in 2L and 3L NPP topologies need to block the whole DC-link. In 3L NPC and 3L ANPC, they only need to block half of it. If the DC-link voltage is higher than the ambitious  $100_{FIT}$  several semiconductors need to be put in series, increasing the cost and complexity of the configuration. Table X shows the required number of series semiconductors for each grid voltage and topology.

**Table X.**

Required number of semiconductors in series for each grid voltage.

Grid voltage [V <sub>AC</sub> ]	Topology	1.2 kV	1.7 kV	3.3 kV
690	2L / 3L NPP	2	1	1
	3L NPC / 3L ANPC	1	1	1
900	2L / 3L NPP	2	2	1
	3L NPC / 3L ANPC	1	1	1
1375	2L / 3L NPP	3	2	1
	3L NPC / 3L ANPC	2	1	1
2850	2L / 3L NPP	6	4	2
	3L NPC / 3L ANPC	3	2	1
3300	2L / 3L NPP	7	5	3
	3L NPC / 3L ANPC	4	3	2



The number of semiconductors in parallel is defined by the current rating of the semiconductor. If the current rating is not enough for a certain application, semiconductors need to be added in parallel. This is a more common and easier task than adding semiconductors in series.

### 2.3.1.6. Switching frequency

Three switching frequencies are considered in this work, 2.5, 5 and 10 kHz. The baseline operates at 2.5 kHz. Increasing the switching frequency directly affects the quality of the output waveform, reducing the filtering requirements. However, the switching losses also increase proportionally. Due to the better performance of SiC in switching, analyzed in Section 1.4, 10 kHz is considered. Si IGBTs are kept at a maximum 5 kHz switching frequency.

## 2.3.2. Algorithm models

Each part of the wind energy system is modeled to introduce it in the LCoE calculation tool. After the configuration is defined by the input parameters, the algorithm goes through these models to calculate the required parameters and variables to compute the LCoE. The models can be based on lookup-tables (LuT) or in analytical equations. In addition, the models must keep a reasonable tradeoff between accuracy and computational cost.

### 2.3.2.1. Mechanical model

The mechanical model converts the mechanical power of the wind into electrical power. This is done by LuTs provided by the industrial partner. These LuTs model the behavior of the blades, the mechanical components in the shaft as well as the generator. Different LuTs are provided for different application powers, configurations and grid voltages. The output of this model is the electrical power processed by the converter. In addition, the annual hours working at each power are also computed.

### 2.3.2.2. Semiconductor model

A database is created in Excel with the information of all the semiconductors considered for the tool. In addition, a methodology to add new semiconductors to the database is designed. The objective is to gather the characteristics of each semiconductor so the algorithm can use them in the converter model.

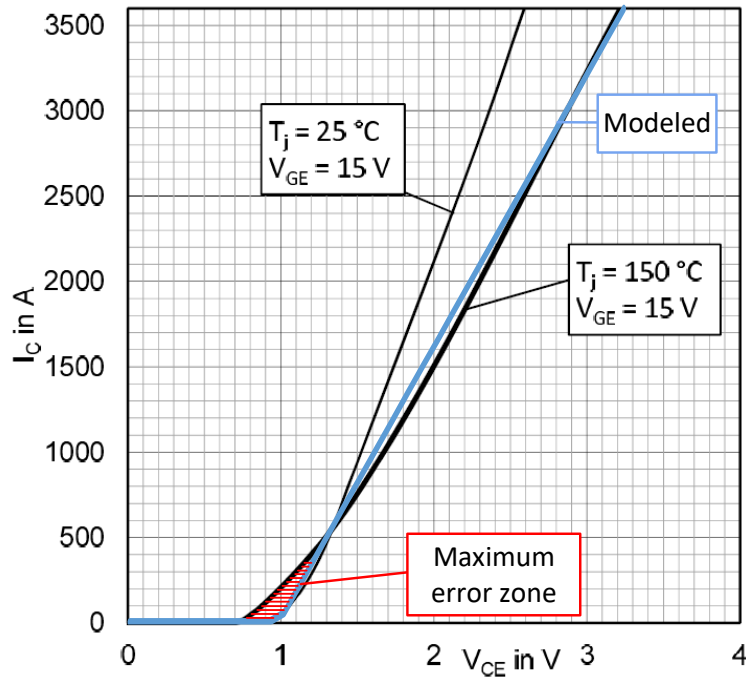
First, the semiconductor model gathers the ambitious  $100_{FIT}$  and the rated maximum current of each semiconductor. With this information the required number of semiconductors in series and in parallel is calculated. This depends on the power of the application, the wind turbine configuration, the grid voltage, the topology of the converter and the semiconductor data.

The next modeled characteristic is the forward conduction of the semiconductor. With this information, the converter model calculates the conduction losses of each configuration. The Si 1.7 kV IGBT used by the baseline is used as an example to illustrate the forward conduction modeling.

The semiconductor is modeled at 150 °C. This is the closest data to the operation point the manufacturers provide. Assuming the semiconductor will operate at 25 °C is unrealistic. As Figure 2. 6 shows, the model consists in a direct voltage drop ( $V_{th}$ ) followed by a first order linear approximation ( $r_d$ ), which models the resistive behavior of the semiconductor, (4).

$$V_{drop}(i) = V_{th} + r_d \cdot i \quad (4)$$

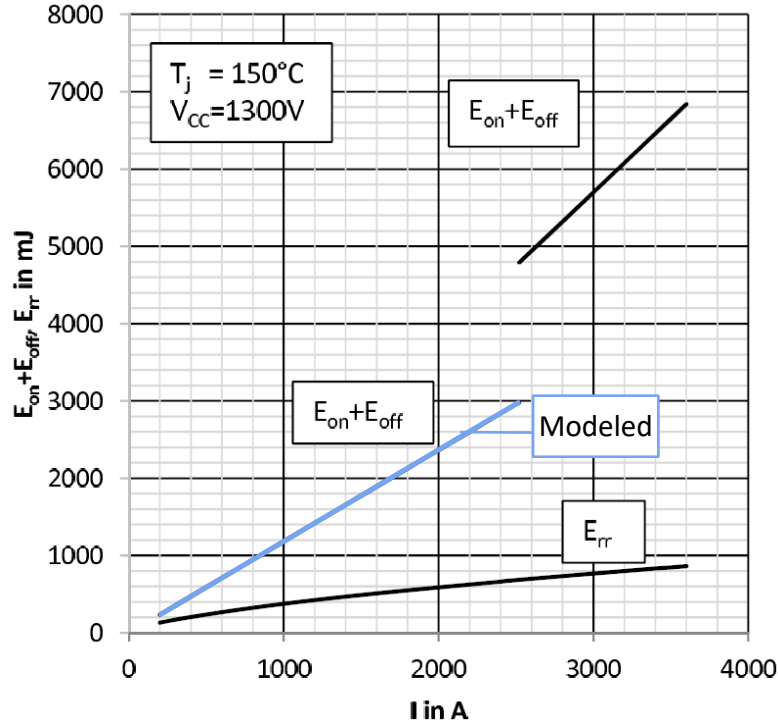
Observing Figure 2. 6, the maximum error occurs for low currents. However, the direct voltage drop ( $V_{th}$ ) in SiC MOSFETs is 0 V, so they are modeled as purely resistive elements ( $r_d \equiv R_{ds,on}$ ). The same modeling technique is used for the diodes.



**Figure 2. 6.**  
Modeled forward characteristics of the baseline semiconductor.

The same curve fitting technique is used for modelling the switching energy losses, as seen in Figure 2. 7. A second order polynomial approximation is used in this case. Both on and off energies are added. The switching energy in the Si diodes is approached similarly, as it is represented in Figure 2. 7. Parameters  $a$ ,  $b$  and  $c$  in (5) are assigned to each semiconductor. In the case of SiC diodes, the switching energy is considered negligible.

$$E_{sw}(i) = a + b \cdot i + c \cdot i^2 \quad (5)$$



**Figure 2.7.**  
Modeled switching characteristics of the baseline semiconductor.

Finally, the semiconductor model also assigns a cost to each semiconductor, which has been approximated thanks to information provided by the industrial partner. The cost of each semiconductor, together with the number of semiconductors is used by the cost function later to calculate the cost of the converter.

### 2.3.2.3. Converter model

The converter model is based on analytical calculations. It calculates the power losses in the converter, using the information given by the semiconductor model, the power of the application, and the switching frequency. These losses are divided between the conduction and switching losses.

The conduction losses are calculated by the product of the voltage drop in the semiconductor, and the current through it, shown in (6).

$$P_c(t) = V_{th}(t) \cdot i_Q(t) + r_d \cdot i_Q^2(t) \quad (6)$$

The average conduction losses during a given  $n$  switching period are obtained by equation (7), where  $\delta_{Q,n} \cdot T_{sw}$  represents the conduction time of Q semiconductor during  $T_{sw}$  switching period.

$$\bar{P}_{cond,n} = \frac{1}{T_{sw}} \int_0^{\delta_{Q,n} \cdot T_{sw}} V_{th} \cdot i_Q(t) + r_d \cdot i_Q^2(t) dt \quad (7)$$

However, the duty-cycle  $\delta_n$  and conducted current shape will vary along a fundamental period  $T_0$  in a sinusoidal waveform application, so each  $n$  periods' power losses need to be computed individually. The sum of all  $N$  periods' conduction losses will result in the total average conduction power losses, (9).

$$N = \frac{T_o}{T_{sw}} = \frac{f_{sw}}{f_o} \quad (8)$$

$$\bar{P}_{cond} = \frac{1}{N} \sum_{n=0}^{N-1} \bar{P}_{cond,n} = \frac{1}{N} \sum_{n=0}^{N-1} \left( \frac{1}{T_{sw}} \int_0^{\delta_{Q,n} T_{sw}} V_{th} \cdot i_Q(t) + r_d \cdot i_Q^2(t) dt \right) \quad (9)$$

Assuming constant  $V_{th}$  and  $r_d$  along the fundamental period, the power losses expression is simplified to (10),

$$\bar{P}_{cond} = V_{th} \cdot i_{Q,ave} + r_d \cdot i_{Q,rms}^2 \quad (10)$$

Where,

$$i_{Q,ave} = \frac{1}{N} \cdot \sum_{n=0}^{N-1} i_{Q,n} \cdot \delta_{Q,n} \quad (11)$$

$$i_{Q,rms} = \sqrt{\frac{1}{N} \cdot \sum_{n=0}^{N-1} i_{Q,n}^2 \cdot \delta_{Q,n}} \quad (12)$$

The duty-cycle or relative conduction  $\delta_{Q,n}$  time of each Q semiconductor in a converter varies along the fundamental period, but also depending on the converter topology, the semiconductors' position within the converter and the working conditions (modulation index,  $m_a$  and power factor  $\phi$  mainly). Thus, the  $i_{Q,ave}$  and  $i_{Q,rms}$  expressions will be different for each Q semiconductor.

In a common PWM application, in which the  $f_{sw}$  is much higher than the fundamental  $f_o$  frequency ( $N \gg 1$ ), and assuming a sinusoidal phase current waveform, these expressions can be simplified obtaining simple integrals [93].

With these assumptions, the average and rms currents of any semiconductor can be derived. For example, (13) and (14) show the average and rms current expressions of a controlled switch of the 2L converter (either  $T_1$  or  $T_2$ , in Figure 2. 2).

$$i_{T1,ave} = \frac{\hat{I}_{ph}}{8\pi} (4 + \pi \cdot m_a \cdot \cos \phi) \quad (13)$$

$$i_{T1,rms} = \hat{I}_{ph} \sqrt{\left( \frac{1}{8} + \frac{1}{3\pi} \cdot m_a \cdot \cos \phi \right)} \quad (14)$$

The conduction losses expressions for all the rest of topologies and semiconductors (either controlled switches or diodes) have been obtained by using the same procedure.

Regarding the switching losses, an equivalent process has been followed. The switching energy is calculated using the second order polynomial approximation in Figure 2. 7. However, the semiconductor model gives the switching energy for a certain DC voltage, usually the  $100_{FIT}$ . (15) assumes the switching energy changes proportionally to the switched voltage  $V_{sw}$ .

$$E_{sw}(t) = \frac{V_{sw}(t)}{V_{100FIT}} (a + b \cdot i(t) + c \cdot i(t)^2) \quad (15)$$

The total power loss due to switching energy in the  $n^{\text{th}}$  switching period is the integral of the energy loss divided by the  $T_{sw}$ , (16).

$$\bar{P}_{sw,n} = \frac{1}{T_{sw}} \int_0^{\delta_{Q,n} \cdot T_{sw}} \frac{V_{sw}(t)}{V_{100FIT}} (a + b \cdot i_Q(t) + c \cdot i_Q(t)^2) dt \quad (16)$$

As well as in conduction losses, the duty-cycle  $\delta_{Q,n}$  and the  $i_Q$  current shape vary along the fundamental period, so each switching periods' switching losses need to be computed individually, to finally sum up all the power losses (17).

$$\bar{P}_{sw} = \frac{1}{N} \sum_{n=0}^{N-1} \left( \frac{1}{T_{sw}} \int_0^{\delta_{Q,n} \cdot T_{sw}} \frac{V_{sw}(t)}{V_{100FIT}} (a + b \cdot i_Q(t) + c \cdot i_Q(t)^2) dt \right) \quad (17)$$

Assuming the switched voltage  $V_{sw}$  and switching frequency  $f_{sw}$  are constant, switching losses are finally calculated as (18).

$$P_{sw} = \frac{f_{sw}}{T_o} \cdot \frac{V_{sw}}{V_{100FIT}} \int_{t_{Q,0}}^{t_{Q,1}} (a + b \cdot i(t) + c \cdot i(t)^2) dt \quad (18)$$

where  $t_{Q,0}$ ,  $t_{Q,1}$  are the conduction period of a given Q semiconductor. Once again, this conduction period will depend on the converter topology, the semiconductor's position within the converter, the modulation index and the power factor, so different switching losses expressions will be obtained for each semiconductor.

For example, (19) and (20) show the switching losses expression of a controlled switch of the 2L converter (either  $T_1$  or  $T_2$ , Figure 2. 2) assuming, for the sake of simplicity, a sinusoidal waveform.

$$\bar{P}_{T1,sw} = \frac{f_{sw} \cdot V_{sw}}{4\pi \cdot V_{100FIT}} (c \cdot \pi \hat{I}_{ph}^2 + 4b \hat{I}_{ph} + 2a \cdot \pi) \quad (19)$$

$$i_{T1,rms} = \hat{I}_{ph} \sqrt{\left( \frac{1}{8} + \frac{1}{3\pi} \cdot m_a \cdot \cos \phi \right)} \quad (20)$$

If the switching frequency is at least 10 times higher than the fundamental frequency, the maximum error produced due to the neglected voltage and current ripple is lower than the 7 % [94].

The analysis explained in this section is done for every topology considered in the LCoE calculation tool, and listed in Section 2.3.1.4. Finally, the converter model also gathers the DC-link voltage. This depends on the grid voltage, and is shown in Table III. With this information the DC-link capacitor cost is calculated by the cost function.

#### 2.3.2.4. Filter model

This model calculates the losses in the inductive filters of the system. The loss modeling technique is the same for the four magnetic components existing in the system. These are:

- Rotor side filter.
- Sharing inductances.
- Grid side filter.
- Harmonic filter.

The industrial partner provides reference loss values for each filter. This work adapts those reference values to the new studied configurations. The losses are divided between the copper losses and the core losses.

The copper losses occur due to the resistance of the conductor  $R$ , see (21).

$$P_{cu} = R \cdot I_{RMS}^2 \quad (21)$$

As seen in (22), the resistance of the conductor is proportional to its length,  $l_{cu}$ , with the length proportional to the number of turns  $N$  (23). So, the copper losses are proportional to the number of turns (24).

$$R = \rho_{cu} \frac{l_{cu}}{A_{cu}} \quad (22)$$

$$l_{cu} \propto N \quad (23)$$

$$P_{cu} \propto N \cdot I_{RMS}^2 \quad (24)$$

The inductance  $L$  of an inductor is proportional to the square of the number of turns (25). So the number of turns, are proportional to the square root of the inductance (26).

$$L = \frac{N^2}{\mathfrak{R}} \quad (25)$$

$$N \propto \sqrt{L} \quad (26)$$

At the same time, the inductance is inversely proportional to the switching frequency (27) and (28).

$$V_L = L \frac{di}{dt} \approx L \frac{di \cdot f_{sw}}{D} \quad (27)$$

$$L \propto \frac{1}{f_{sw}} \quad (28)$$

Following deductions in (24), (26) and (28), the relation in (29) is defined.

$$P_{cu} \propto \sqrt{\frac{1}{f_{sw}}} \cdot I_{RMS}^2 \quad (29)$$

Finally, the equation used by the filter model to calculate the copper losses is derived (30). The reference values are the ones of the baseline, and are provided by the industrial partner.

$$P_{cu,new} = P_{cu,ref} \sqrt{\frac{f_{sw,ref}}{f_{sw,new}}} \cdot \left( \frac{I_{RMS,new}}{I_{RMS,ref}} \right)^2 \quad (30)$$

The losses in the magnetic core in general power electronics applications are calculated by the improved generalized Steinmetz equation. However, the industrial partner of this project proposes a relation dependent on the switching frequency (31). This relation is obtained by experience. The complexity of the calculation of the core losses is highly reduced with the use of this equation.

$$P_{co,new} = P_{co,ref} \sqrt[4]{\left(\frac{f_{sw,new}}{f_{sw,ref}}\right)^5} \quad (31)$$

### 2.3.3. Cost function

The cost of the analyzed configurations is calculated by the cost function. To do so, the output of each of the models referring the cost are used. The effect that the selected input parameters have on the cost of the system is studied. The industrial partner provides the reference costs of the baseline. In addition, the cost of the civil engineering, as well as the generator and turbine are also provided by them for each power of the application and wind turbine configuration.

#### 2.3.3.1. Cost of the semiconductors

The semiconductor model calculates the required number of semiconductors in each configuration. In addition, the generated semiconductor database assigns a cost to each semiconductor  $C_{semi}$ . So the total cost of the semiconductors is calculated with (32).

$$Cost_{semi} = N_{semi} \cdot C_{semi} \quad (32)$$

The cost of the database is assigned after checking with different manufacturers and commercial distributors. Each technology and voltage rating has a different cost. In addition, the cost is given in €/A. The cost of every semiconductor is calculated depending on the technology, voltage and current ratings. Table XI shows the considered costs for the semiconductors.

**Table XI.**

Considered semiconductor cost normalized to the rated current.

	1.2 kV	1.7 kV	3.3 kV	Unit
Si	0.1002	0.1729	0.5294	€/A
SiC	0.3192	0.5188	3.8701	€/A

#### 2.3.3.2. Cost of the drivers

The cost of the drivers is calculated multiplying the cost of the reference driver by the number of semiconductors in the configuration, shown in (33). The cost of the reference driver  $C_{Driver,ref}$  is given by the industrial partner.

$$Cost_{Drivers} = N_{semi} \cdot C_{Driver,ref} \quad (33)$$

### 2.3.3.3. Cost of the control unit

The cost of the control unit is proportional to the power of the application and is shown in (34). The power of the baseline is the reference, so the  $P_{ref}$  is 5 MW.

$$Cost_{CCU} = Cost_{CCU,ref} \cdot \frac{P}{P_{ref}} \quad (34)$$

### 2.3.3.4. Cost of the DC-link capacitors

The required holdup time of the DC-link voltage is the same for different powers of the application. This means the energy required in the capacitors of the DC-link is directly proportional to the power of the application (35).

$$E_{DC-link} = E_{DC-link,ref} \cdot \frac{P}{P_{ref}} \quad (35)$$

However, the energy of a capacitor is defined by its voltage, represented in (36). So the DC voltage is proportional to the square root of the energy in the DC-link (37).

$$E_{DC-link} = C \cdot \frac{V_{DC-link}^2}{2} \quad (36)$$

$$V_{DC-link} \propto \sqrt{E_{DC-link}} \quad (37)$$

(38) is defined to consider the effect of the power and the DC voltage of the application in the cost of the DC-link capacitors.

$$Cost_{DC-link} = Cost_{DC-link,ref} \cdot \frac{P}{P_{ref}} \cdot \sqrt{\frac{V_{DC-link}}{V_{DC-link,ref}}} \quad (38)$$

### 2.3.3.5. Cost of the heatsink

The cost of the heatsink is proportional to the losses of the converter. These losses are calculated by the converter model and presented in Section 2.3.2 of this work. (39) calculates the cost of the heatsink. The reference converter losses  $P_{Loss,conv,ref}$  are taken from the baseline configuration. The reference cost is given by the industrial partner.

$$Cost_{Heatsink} = Cost_{Heatsink,ref} \cdot \frac{P_{Loss,conv}}{P_{Loss,conv,ref}} \quad (39)$$

### 2.3.3.6. Cost of the water pump

The cost of the water pump is considered constant for all the configurations. The cost is given by the industrial partner.

### 2.3.3.7. Cost of the cabinet

The cost of the cabinet is proportional to the power of the application and shown in (40). The power of the baseline is the reference, so the  $P_{ref}$  is 5 MW.

$$Cost_{cabinet} = Cost_{cabinet,ref} \cdot \frac{P}{P_{ref}} \quad (40)$$



### 2.3.3.8. Cost of the grid filters

The required filters power ratings are proportional to the power of the application. However, as shown in (28), the required inductance  $L$  is inversely proportional to the switching frequency  $f_{sw}$ . In addition, the number of turns is proportional to the square root of the inductance (25).

It is considered the cost of the inductor changes at the same rate as the turn number. So the cost of the grid filter is calculated using equation (41). This equation considers the effect of the power and the switching frequency in the cost of the grid inductor. The reference switching frequency is the one in the baseline, 2.5 kHz.

$$Cost_{Lgrid} = Cost_{Lgrid,ref} \cdot \frac{P}{P_{ref}} \cdot \sqrt{\frac{f_{sw,ref}}{f_{sw}}} \quad (41)$$

### 2.3.3.9. Cost of the generator inductor

The calculation of the cost of the generator inductor is done the same way as for the grid inductor. (42) also considers the effect of the power and the switching frequency.

$$Cost_{Lgen} = Cost_{Lgen,ref} \cdot \frac{P}{P_{ref}} \cdot \sqrt{\frac{f_{sw,ref}}{f_{sw}}} \quad (42)$$

### 2.3.3.10. Cost of the brake chopper

The cost of the brake chopper is proportional to the power of the application and is shown in (43). The power of the baseline is the reference, so the  $P_{ref}$  is 5 MW.

$$Cost_{chopper} = Cost_{chopper,ref} \cdot \frac{P}{P_{ref}} \quad (43)$$

### 2.3.3.11. Cost of the circuit breakers and contactors

The cost of the circuit breakers and contactors is proportional to the power of the application and shown in (44). The power of the baseline is the reference, so the  $P_{ref}$  is 5 MW.

$$Cost_{Breaker/contactor} = Cost_{Breaker/contactor,ref} \cdot \frac{P}{P_{ref}} \quad (44)$$

### 2.3.3.12. Cost of the cabling

The cost of the cabling is proportional to the power of the application and is shown in (45). The power of the baseline is the reference, so the  $P_{ref}$  is 5 MW.

$$Cost_{cable} = Cost_{cable,ref} \cdot \frac{P}{P_{ref}} \quad (45)$$

### 2.3.3.13. Total cost of the converter

Finally, all the components' cost is added to calculate the total cost of the converter (46).

$$\begin{aligned}
 Cost_{Converter} = & Cost_{Semi} + Cost_{Drivers} + Cost_{CCU} \\
 & + Cost_{DC-link} + Cost_{Heatsink} + Cost_{Pump} \\
 & + Cost_{Cabinet} + Cost_{Lgrid} + Cost_{Lgen} \\
 & + Cost_{Chopper} + Cost_{Breaker/contactor} \\
 & + Cost_{Cable}
 \end{aligned} \tag{46}$$

### 2.3.4. AEP function

This function calculates the annual energy production of the analyzed configurations. Two wind profiles defining the annual hours at each wind speed are provided by the industrial partner. One for locations with annual average wind speeds of  $n = 7 \text{ m/s}$  and the other for  $n = 8,5 \text{ m/s}$ . The calculation is done by equation (47) for both locations. The power sent to the grid  $P_{Grid}$  at every wind speed is multiplied by the hours spent at that wind speed in a year. Wind speeds superior to 25 m/s are not considered because the wind turbine is forced to parking mode for safety.

$$AEP_{n \text{ avg } v_{wind}} = \sum_{V_{Wind}=0 \text{ m/s}}^{25} P_{Grid}(V_{Wind}) \cdot Annual \text{ Hours } (V_{Wind}) \tag{47}$$

To calculate  $P_{Grid}$ , equation (48) is used.

$$P_{Grid}(V_{Wind}) = P_{Elec}(V_{Wind}) - Loss_{Conv}(V_{Wind}) \tag{48}$$

$P_{Elec}$  refers to the electrical power calculated by the mechanical model for each wind speed. This value is given by a lookup table provided by the industrial partner for every configuration. Then, the converter losses  $Loss_{Conv}$  are subtracted from the electrical power. These are calculated by the converter model for each configuration and wind speed. Finally, to obtain the parameter *Weighted AEP* in equation (1) the equation (49) is used. It is calculated by averaging the annual energy production in locations with 7 m/s and 8.5 m/s annual wind speeds, according to the standards of the industrial partners.

$$Weighted \ AEP = 0,6 \ AEP_{7 \text{ m/s avg } v_{wind}} + 0,4 \ AEP_{8,5 \text{ m/s avg } v_{wind}} \tag{49}$$

### 2.3.5. LCoE function

Finally the LCoE function computes equation (1) to obtain the LCoE of the analyzed configuration. The cost values are provided by the industrial partner, except the converter cost. These are calculated by the cost function. The *Losses* in equation (1) relate to the time the wind turbine is not working due to maintenance or unexpected failures. They are provided by the industrial partner for each configuration. Finally, the civil work cost *BOP*, the tax related cost *FCR* as well as the company margin are also set by the industrial partner.

The calculated LCoE is stored in an Excel file together with the details of the analyzed configuration.

## 2.4. Tool optimization

### 2.4.1. Computational cost

Sweeping the input parameters, the tool analyzes up to 67500 different configurations. The program structure is iterative at first. Configurations are calculated individually, running the whole algorithm for every configuration. Then, a single input parameter is changed, to create a new configuration, and the whole algorithm is run again. With this program strategy it takes several hours to analyze all the configurations.

### 2.4.2. Vectorization

The computational cost of the tool is too high to fulfill the objectives set in Section 2.1. The high capability of MatLab to perform matrix operations is used to optimize the computational cost of the tool.

The input variables are compressed into vectors. The functions use these vectors only once to perform the operations. The computational cost is reduced 70 % with this strategy. This optimization allows to use the tool with the previously defined approach, comparing different scenarios, including variations in cost, new components or different calculation methods. Some input variables cannot be turned into vectors. Semiconductors for example need to access a database with their characteristics, so the iterative process is kept for them. The use of vectors in several functions creates matrixes, which need to be decompressed in order to store them in the results Excel file. This is done using indexing techniques in MatLab.

## 2.5. Results

The LCoE shown in the results is the difference with respect to the LCoE of the baseline. Only the configurations improving or close to improve the baseline are considered. As the baseline is a DFIG based configuration, all the FC configurations are far from the reference LCoE. Only DFIG configurations are then considered in the results analysis.

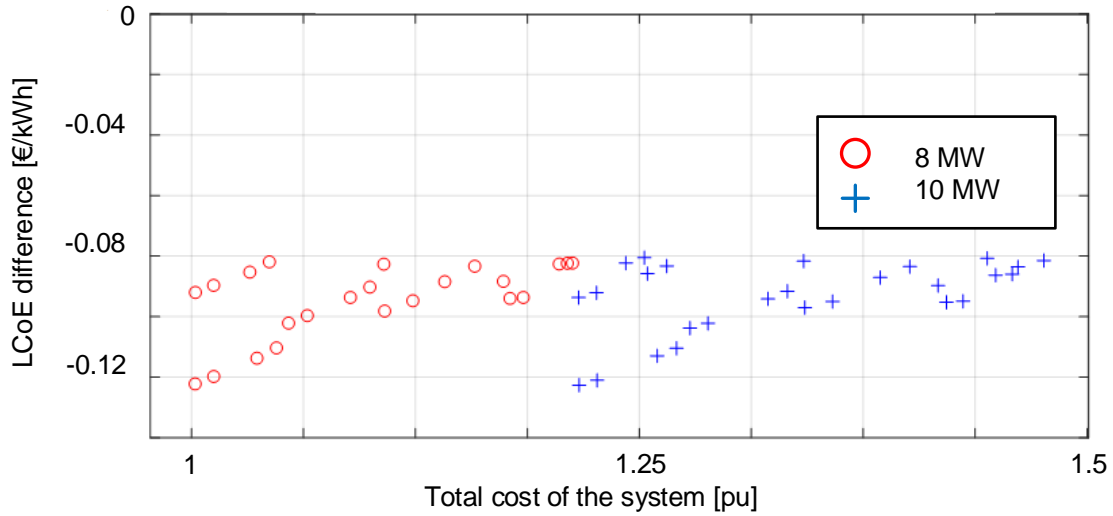
### 2.5.1. Baseline

The tool has been tuned in order to match the LCoE of the baseline accurately, thanks to the specific LCoE data provided by the industrial partner. The baseline is a 5 MW DFIG which uses 1.7 kV Si IGBTs, switching at 2.5 kHz with a 690 V<sub>AC</sub> grid.

### 2.5.2. Current cost

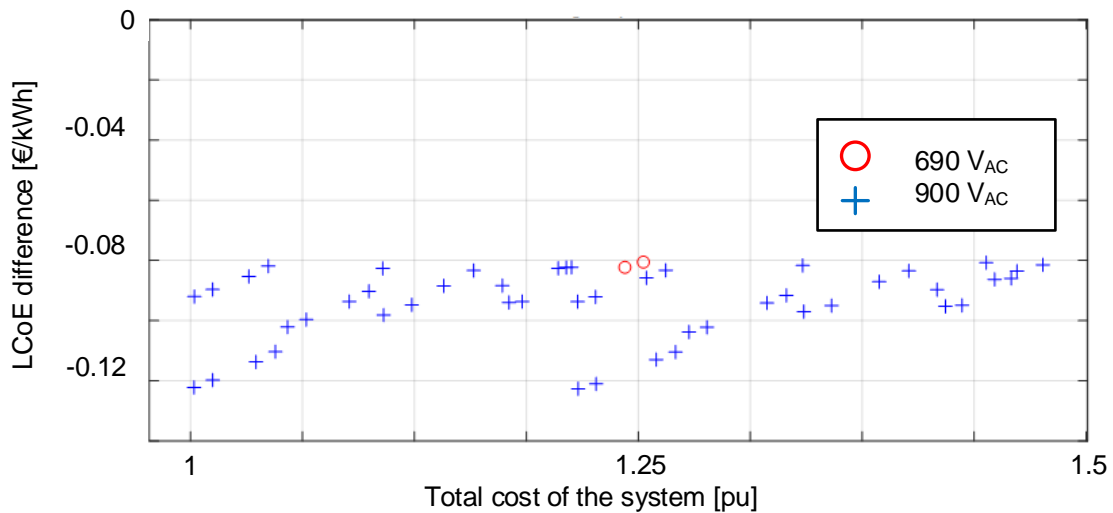
The first analysis is done considering the current cost of the semiconductors. Figure 2. 8 depicts in red and blue, the wind turbine (WT) configurations of 8 MW and 10 MW that would improve the baselines' LCoE (see y axis). The x axis represents the total cost of each WT with respect to the baseline in p.u.. As it can be observed in these results, there are several

configurations that improve the baselines' LCoE, with all of them 8 and 10 MW DFIG solutions. Among these improved solutions, the total cost of the 8 MW configurations is lower than 10 MW ones.



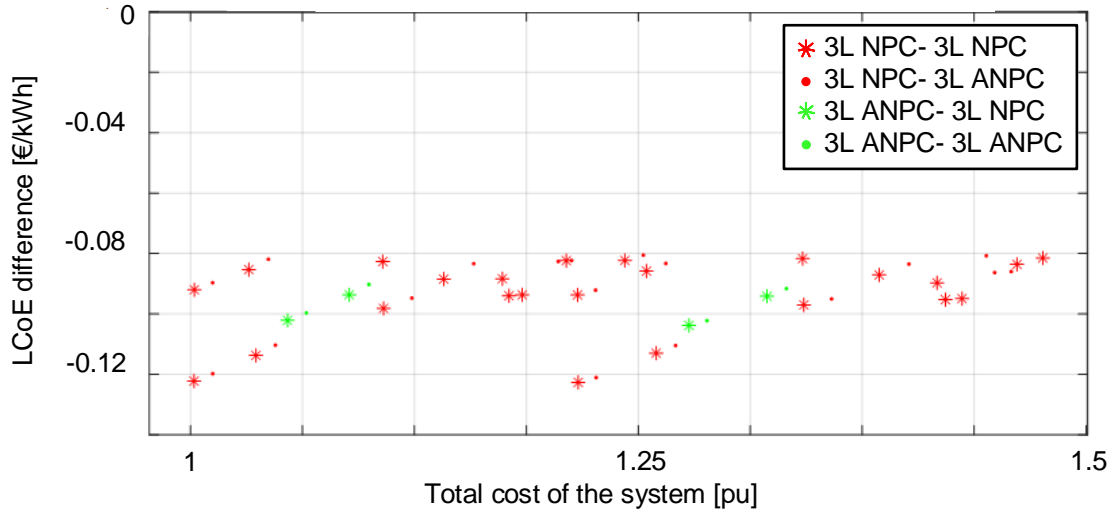
**Figure 2. 8.** Power of the configurations improving the LCoE of the baseline with the current cost of the semiconductors.

Because DFIG cannot work at high voltage, all the configurations that improve the LCoE are low voltage configurations, as shown in Figure 2. 9. Among these low voltage DFIG configurations, 900 V<sub>AC</sub> are preferred over 690 V<sub>AC</sub>, mostly because the current of the application is reduced. This allows to use less semiconductors in parallel, minimizing the total cost of semiconductors. It also shows the advantage of using ambitious 100<sub>FIT</sub>, allowing to increase the voltage of the application until the limit of the semiconductor is met. Doing so, the current of the application is reduced, reducing the number of required parallel semiconductor in each case.



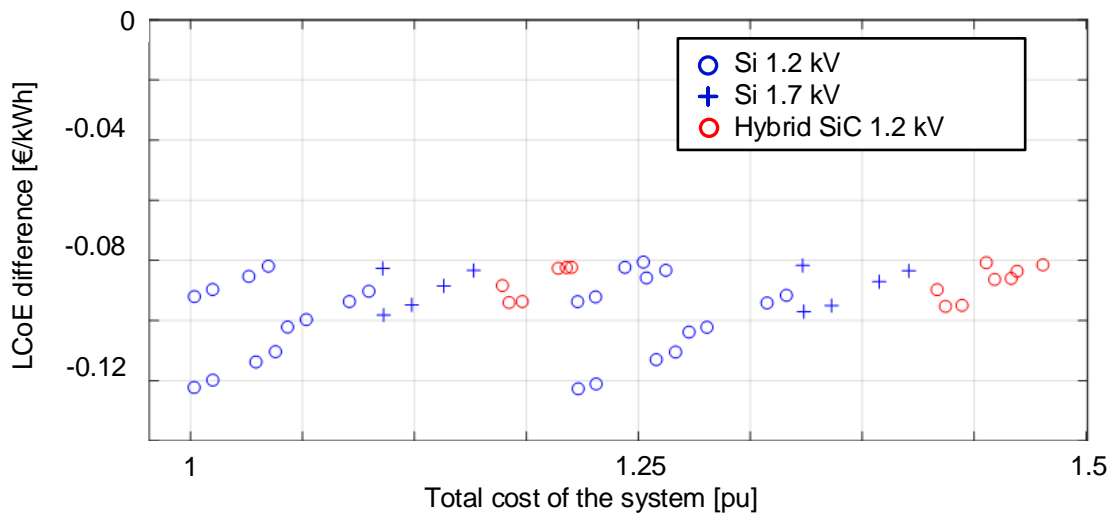
**Figure 2. 9.** Voltage of the configurations improving the LCoE of the baseline with the current cost of the semiconductors.

Figure 2. 10 shows that all the improved configurations use 3L converter topologies. Both 3L NPC and 3L ANPC can be used in both sides of the back-to-back converter. This is an important result, because in the current wind energy market the 2L topology is the most used one. This analysis shows the LCoE of wind energy could be improved by adopting 3L topologies.



**Figure 2. 10.** Topology of the configurations improving the LCoE of the baseline with the current cost of the semiconductors.

Figure 2. 11 shows the semiconductors used in the configurations improving the LCoE of the baseline. All the configurations use Si semiconductors, except some 1.2. kV hybrid semiconductors based configurations. However, these latter configurations are not considered because no commercial products exist, and the only ones manufactured are for specific 3.3 kV applications and certain customers.

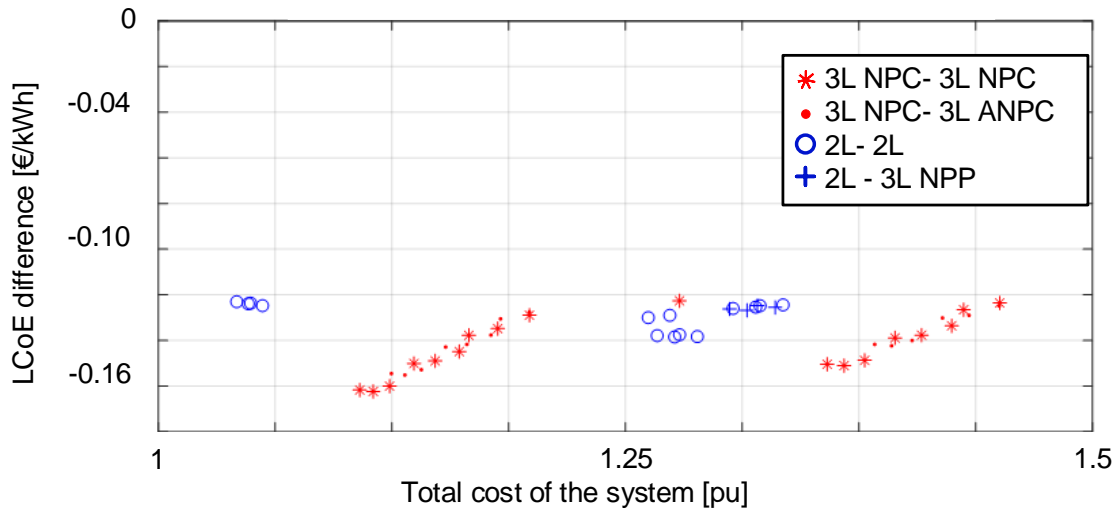


**Figure 2. 11.** Semiconductors of the configurations improving the LCoE of the baseline with the current cost of the semiconductors.

This analysis shows the most promising configurations are those of 8 and 10 MW, with grid voltages of 690 and 900 V<sub>AC</sub>. Higher voltages require semiconductors with higher voltage rating, or putting several devices in series. The increased number of components penalizes the LCoE of high voltage configurations. Regarding the topologies, it is seen 3L topologies improve the LCoE of the baseline. However, all the promising configurations are based on Si semiconductors. With the current cost of the SiC devices, the configurations including this technology cannot compete in cost with the baseline, obtaining higher LCoEs.

### 2.5.3. Future scenario

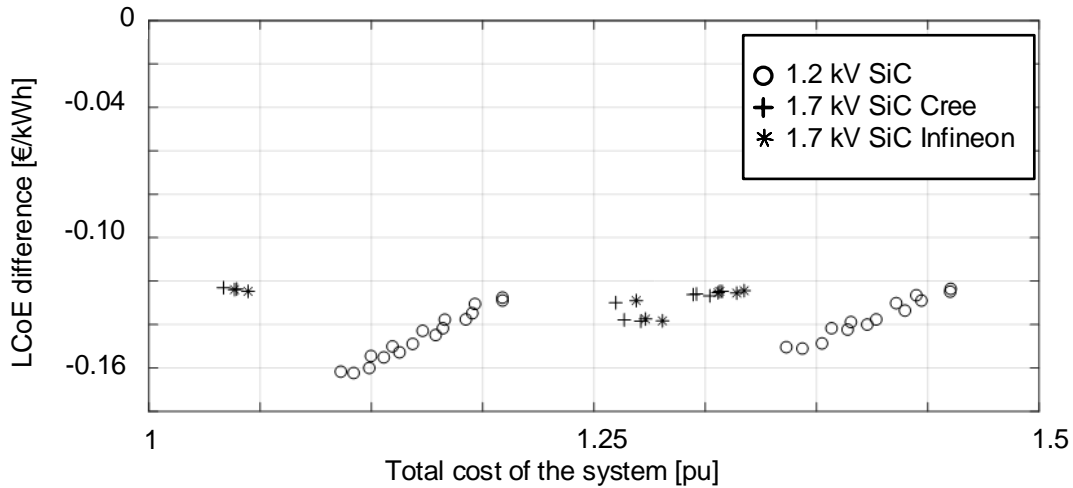
With the objective of analyzing the effect of SiC semiconductors in the LCoE, their cost is reduced. This is done because the prevision says the cost will decrease due to the market increase and technology maturity [95]. With 50 % cost reduction, there are configurations using SiC semiconductors improving the LCoE of the baseline, as seen in Figure 2. 12. For the sake of simplicity, this figure focuses only on the configurations with SiC semiconductors. In comparison with Si based solutions shown in previous section 2.5.2, solutions with major improvements in LCoE (around -0.15 €/kWh reduction) would be obtained with SiC.



**Figure 2. 12.**

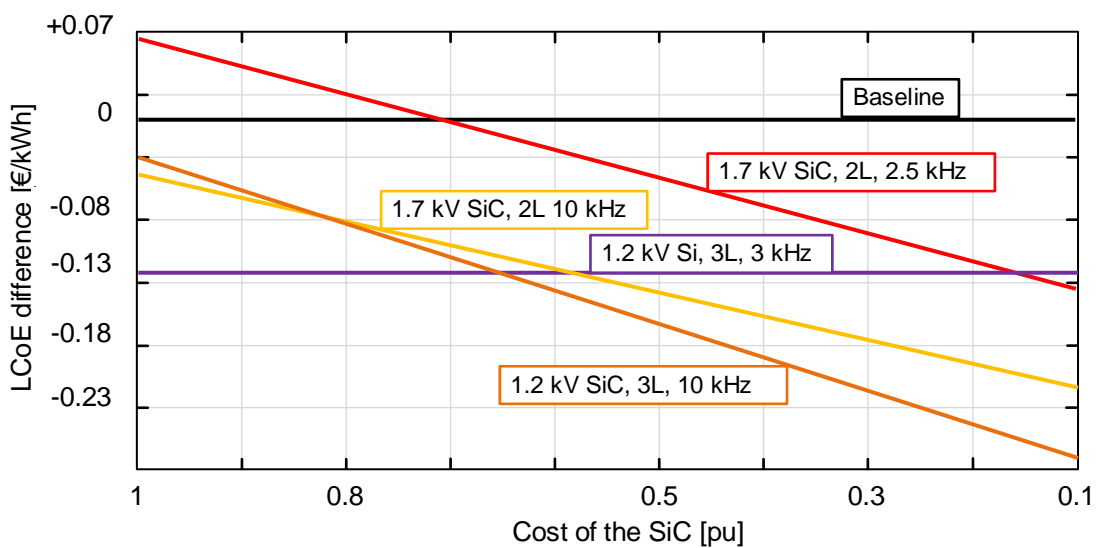
Topologies of the configurations with SiC semiconductors improving the LCoE of the baseline, with half of the current cost of the SiC semiconductors.

As observed in Figure 2. 12, the configurations include 2L and 3L topologies because the cost is lower with 2 level topologies. This occurs because the cost is still the main driver in the LCoE with SiC semiconductors and increasing the number of semiconductors with 3L topologies is not always beneficial. However, and due to the better switching characteristics of SiC, the efficiency of 2L topologies is high enough to have high AEP. Both the high cost of the semiconductors, and the better switching characteristics of SiC make 2L configurations competitive with SiC, when compared to 3L. The used semiconductors are 1.7 kV for 2L and 1.2 kV for 3L, see Figure 2. 13.



**Figure 2. 13.** Semiconductor voltage levels of the configurations with SiC improving the LCoE of the baseline, with half of the current cost of the SiC semiconductors.

Figure 2. 14 analyzes the most promising configurations, considering the cost reduction of SiC semiconductors as well as the effect of the selected switching frequency. Unlike Figure 2. 12, which only shows a 50 % cost reduction, Figure 2. 14 shows the whole evolution of the LCoE for different cost reduction rates. The results show the configurations with SiC can benefit from a higher switching frequency, due to the better switching characteristics. Both 2L and 3L configurations improve the LCoE of the baseline due to the cost reduction of the filters. In addition, the 3L configuration with SiC benefits the most from the expected cost reduction, outperforming the 2L configuration if the cost is reduced more than 20 %. Finally, the analysis shows the 3L configuration with Si is the most competitive one. The cost reduction of SiC needs to be higher than 35 % and 42 % respectively for the 3L and 2L configurations to be competitive when compared to the 3L with Si.



**Figure 2. 14.** LCoE difference for the most interesting configurations, considering cost reduction in SiC semiconductors and the effect of switching frequency.

## 2.5.4. Commercial indicators

Commercial indicators are parameters not included in the LCoE analysis that are still important for companies. The commercial indicators are most of the time related to commercial strategies, company agreements, manufacturing processes or geographical location. If two configurations have similar LCoE, the commercial indicators are key to choose the best product. In addition, some indicators are limiting, meaning that if a configuration gets a low score, it is automatically not considered. This is the case of hybrid SiC technology. Due to its limited production, the supply chain of the semiconductors is not guaranteed, so configurations using hybrid semiconductors are not considered.

The commercial indicators considered in this project are listed in Table XII. The time to market defines the time needed by the company to create a product using a certain configuration. The lower the time to market is, the more interesting the configuration is for the company. The technical risk refers to possibility to fail while developing a product based on a certain configuration. In this case, the failure comes due to technical challenges of the configuration. The lower the technical risk is, the more interesting the configuration is for the company. This benefits simple configurations, with well-known topologies and components. It is most of the times a major drawback for innovation. The development effort indicates the effort in time, money and resources the company needs to assume in order to develop a product using a certain configuration. The lower the development effort is, the more attractive the configuration will be for the company. Finally, the supply chain analyzes if the availability of every component needed to develop the product is guaranteed. If not, the mass production is affected, or the delivery times will not be good enough. If the supply chain is not assured, the configuration is not considered by the company.

The commercial indicators are analyzed comparing the features offered by the new configurations to the baseline. As there is already a developed product with the baseline, it has the best scores in the commercial indicators. Table XII shows how severely the commercial indicators are affected for different configurations. Low indicates the configuration is nearly not affected negatively by the commercial indicator. Medium shows a relative negative effect on the configuration, while high indicates severe negative effect.

**Table XII.**

Effect of the analyzed configurations on the commercial indicators, compared to the baseline.

Indicator	Baseline	3L NPC Si	2L SiC	3L NPC SiC
<b>Time to market</b>	/	Low	Medium	Medium
<b>Technical risk</b>	/	Low	Medium	High
<b>Development effort</b>	/	Low	Medium	High
<b>Supply chain availability</b>	/	Low	Medium	Low

The 3L configuration using Si does not severely affect the commercial indicators. It is a well-known topology, using reliable and available semiconductors. However, as the 3L topology is yet to be used by the industrial partner, it requires some effort and has a certain amount of risk.

The 2L configuration using SiC uses a new semiconductor technology, so the whole system needs to be redesigned accordingly. It requires a higher effort than the previous configuration and involves a higher risk. In addition, the component supply chain is not fully ensured. The required 1.7 kV SiC MOSFETs are being developed rapidly, but there is still a lack of wide offer in the market, with several suppliers.



In the case of the 3L configuration with SiC semiconductors, the commercial indicators are highly affected. This is because the challenge of using a new semiconductor technology is added to the one of using a new topology. However, the supply chain of the semiconductors is ensured, because the required 1.2 kV MOSFETs are widely offered in the market.

### 2.5.5. Business case selection

A business case (BC) is a configuration which, if turned into a product, can be beneficial for the company business wise. Both LCoE and the commercial indicators need to be considered in order to identify the most interesting BC. If a BC is identified, the company studies if the BC is interesting right now, or in a medium-term period. According to the results of the analysis, the company starts to develop a product immediately or following a several year plan. Doing so, they can take advantage of a technological novelty, or a business gap, getting ahead of the competitors.

According to the analysis developed with the LCoE tool and shown in Section 2.5.2, the 3L configuration using Si is the only one improving the LCoE with current semiconductor costs. In addition, the commercial indicators analyzed in Section 2.5.4 support these results. This is why the selected BC with the current situation is the 3L configuration with Si semiconductors.

However, anticipating the cost reduction of the SiC semiconductors gives the chance of getting ahead of the competitors, by preparing a BC based on SiC. The LCoE of 2L and 3L topologies is similar with increased switching frequency and reduced semiconductor cost. However, the commercial indicators identify the 2L topology as the most reasonable one. Even if the 3L topology is going to be preferred in the long term future with SiC, the semiconductor technology transition needs to start with the 2L topology. The evolution is the same that occurred with Si. First, the simple 2L topology is used to introduce the technology. After the semiconductors are known and the product is mature, 3L topology becomes interesting.

The current and future business case selection is based on SiC semiconductor cost reduction prediction. If this does not occur, the performed analysis is not valid. However, anticipating the selection of a BC, and developing a product gives an important advantage to the company with respect to its competitors. This is why the theoretical analysis performed in this chapter will be further studied with laboratory prototypes in the next ones.



CHAPTER 3  
**Hardware implementation**

## 3. Hardware implementation

This chapter presents the test bench used to validate the LCoE analysis performed in the previous chapter. The design of the hardware is shown in detail. First, the objective and the approach of the test bench are given. Next, the process of selecting the different components is explained. The chapter also includes the design of the power stage for both the three level and two level converters, with the corresponding switching loops' validation. Finally, the chapter is concluded by presenting the most relevant results.

### 3.1. Test bench objectives and approach

#### 3.1.1. Objective of the test bench

The main objective is to test the models analyzed in the LCoE calculation tool. With this, the results obtained in the LCoE calculation tool will be validated. The tests will help to compare the business case candidates between them.

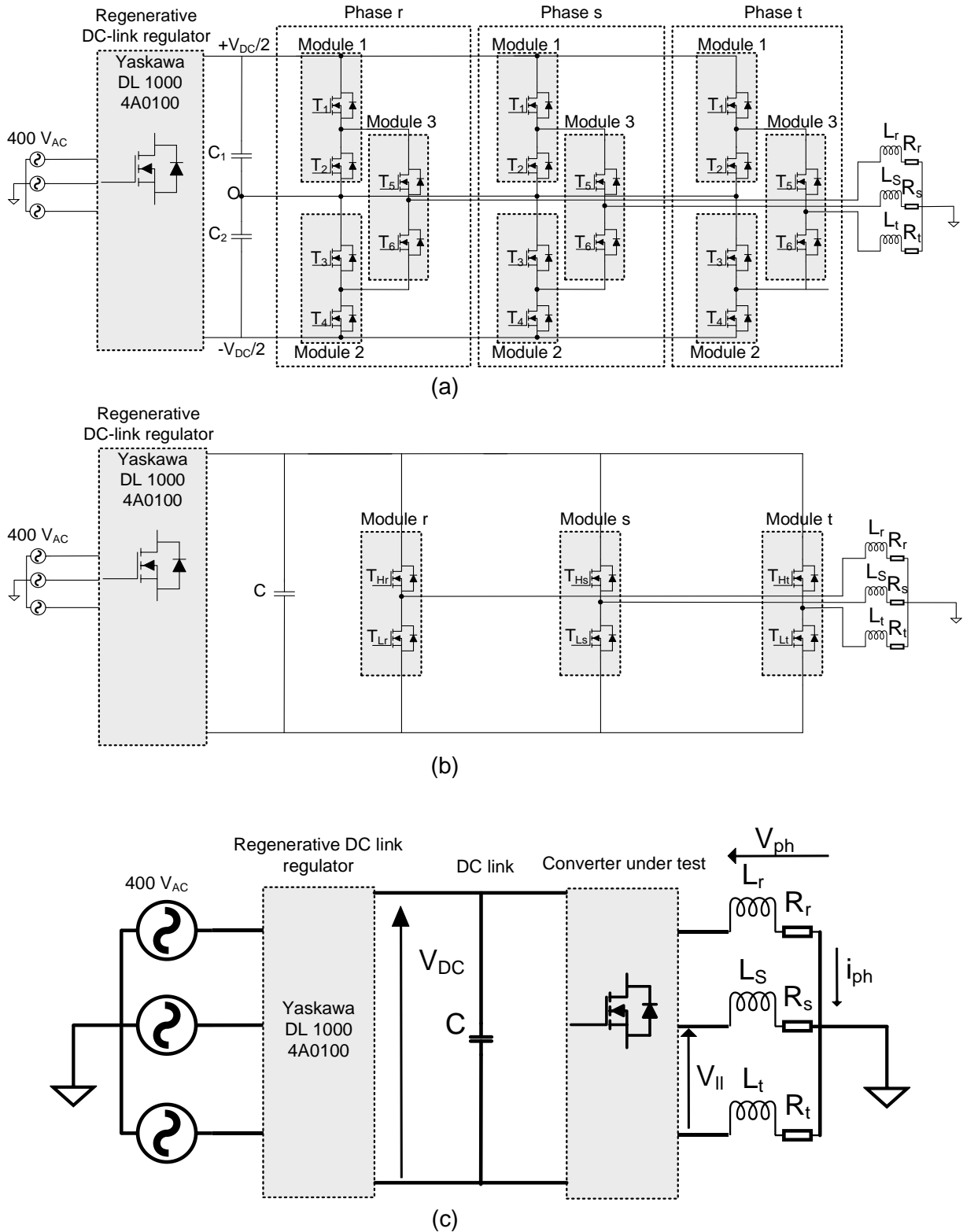
In addition, a second objective is to learn about the application of high power SiC modules. Their performance is being analyzed, specially the switching of high power SiC modules. The objective is to identify the limits and possible adverse effects of high power SiC modules, and then, study how to solve them and make a contribution for the high power electronic designers' community.

#### 3.1.2. Approach

To simplify the test bench, a commercial regenerative DC-link regulator has been used for the input AC-DC stage of the back-to-back (BTB) converter. The analysis is only focused on the DC-AC inverter stage. The selected converter is the 400 V Yaskawa DL 1000 series [96]. To fulfill the objectives, both Si and SiC technologies are tested. In addition, converters with 2 level (2L) and 3 level (3L) topologies are designed. A flexible test bench is needed to keep simplify.

The first decision is to use the same power stage for both semiconductor technologies. By doing so, only one power stage for each topology has to be designed. However, as the requirements of SiC are harder to meet, the power stage is designed for silicon carbide, and validated accordingly.

To use the same power stage, replaceable modules are used. This means the same module package needs to be selected for silicon and silicon carbide. Thus, it is possible to use the same control board for both technologies and topologies. As the three level topology needs to control some extra parameters, the control board will be designed to meet these requirements. Figure 3. 1 shows the designed configuration for the 2L and 3L converters. The main measured power variables are also shown in Figure 3. 1(c), which are common for both converters.



**Figure 3. 1.** Designed test bench configuration with regenerative DC link regulator and replaceable modules, (a) 3 level converter, (b) 2 level converter and (c) general diagram with the main measured power variables.

### 3.2. Component selection

The low scale test bench implemented will be tested at Mondragon Unibertsitatea facilities. The available grid is of 400 V<sub>AC</sub> and 64 A, which limits the power of the tests to 44 kVA. However, a test bench suitable for working at rated voltages of 690V<sub>AC</sub> for 2L and 900 V<sub>AC</sub>

for 3L, as well as power levels up to 125 kVA is built. The selected voltage levels require 1.7 kV modules for the 2L converter and 1.2 kV modules for the 3L.

The selected regenerative DC-link regulator is the Yaskawa 400 V DL 1000 series 4A0100 model. Its output power capability is 100 kW. The DC-link can vary between 600 V and 730 V with the Yaskawa 400 V DL 1000. Additional DC power sources are available to perform certain low power higher voltage tests (up to 1.5 kV).

### 3.2.1. Modules

The market study developed in Section 1.4.2 showed that manufacturers are moving towards common packaging for high power SiC modules. As defined in the test bench approach, the modules need to be replaceable, so the same package is used for Si and SiC. The only suitable package that fills these criteria is the 62mm, see Table II. It is available among different manufacturers, in different semiconductor technologies Si and SiC and the available voltage ratings vary from 1.2 kV and 1.7 kV, up to 2 kV.

Thus, it is proposed to build the converters with real scale modules in terms of voltage rating. The 2L converter will be based on 1.7 kV modules which allow a 1200 V DC-link voltage and 690 V<sub>AC</sub> output voltage. The 3L will be composed of 1.2 kV modules which allow a 1600 V DC-link voltage and 900 V<sub>AC</sub> output voltage. These are considered ambitious 100FIT conditions, and mean pushing the modules voltage rating to the limit [97]. According to these requirements, Table XIII shows the selected 62mm modules.

**Table XIII.**

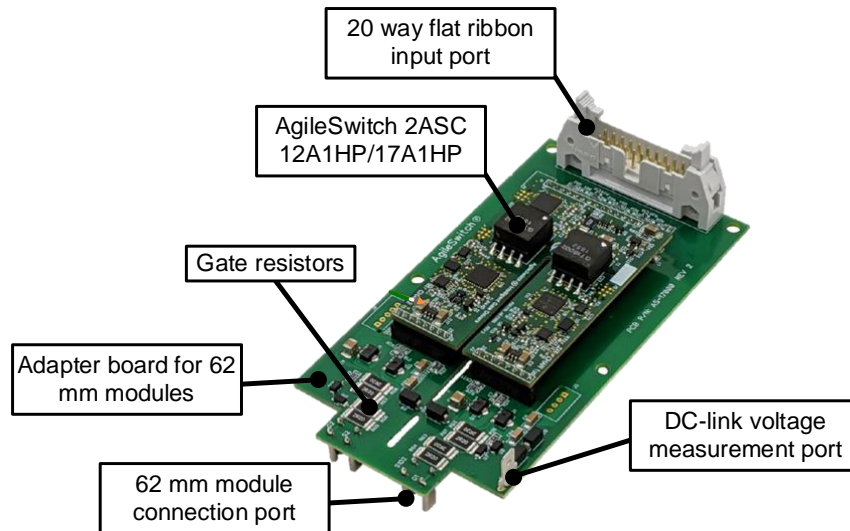
Selected 62 mm modules.

Converter	Technology	Reference	Manufacturer	V <sub>max</sub> [V]	I <sub>max</sub> [A]	Qty	
3 level	Si IGBT	FF200R12K T4	Infineon	1200	20 0	9	[98]
	SiC MOSFET	FF6MR12K M1	Infineon	1200	25 0	9	[99]
2 level	Si IGBT	FF300R17K E4	Infineon	1700	30 0	3	[100]
	SiC MOSFET	CAS300M1 7BM	Cree	1700	32 5	3	[101]
		*FF4MR20 KM1	Infineon	2000	37 0	3	[102]
<p style="color: red;">Out of stock until 2022.</p> <p>*Under development, preliminary samples.</p>							

However, there was no availability in the market for the Cree 1.7 kV SiC MOSFET during the hardware implementation stage due to the high demand. Although equivalent references are checked among other manufacturers, no equivalent solution is found for running the tests during 2021. Finally, the out of production 2 kV (still under development stage) has been provided by Infineon and implemented in the prototype to replace 1.7kV SiC devices.

### 3.2.2. Drivers

The AgileSwitch 2ASC-12A1HP and 2ASC-17A1HP drivers are used to drive the 1.2 kV and 1.7 kV SiC modules respectively. Each of them requires its own specific adapter board, 62CA1-1200 V 62 MM, and 62CA4-12700 V 62 MM, respectively, which serve as a Plug & Play combination, shown in Figure 3. 2. These drivers are specially designed to drive SiC technology, being robust and with high noise immunity. In addition, they are capable of monitoring the temperature and the DC link voltage.



**Figure 3. 2.** AgileSwitch 2ASC-12A1HP/17A1HP driver with the adapter board for 62 mm modules.

Moreover, the drivers are highly programmable using a specially designed interface. A kit box containing the Intelligent Configuration Tool software and the hardware interface for programming all the drivers is acquired. The driver allows to program several fault thresholds. This makes possible to define different overvoltage and overcurrent limits. In addition, this programmable nature makes possible to adapt the features for silicon devices too. This is why the same driver is used for the Si based converters.

### 3.2.3. Capacitors

The capacitors in the DC-link act as energy storage in back to back converters. They are the element that allows the decoupling between the input and output. In wind energy systems it is what allows the generator to operate at a different frequency compared to the grid. The capacitance in the DC-link can be selected using different criteria.

#### 3.2.3.1. Holdup energy

The DC-link capacitor is usually dimensioned according to the holdup energy required under a blackout situation. The criteria is to keep the voltage drop in the DC-link within a controlled range. The required capacitance depends on the allowable voltage drop, during the worst working scenario and the largest allowable blackout time (50).

$$\Delta V_{DC} = \frac{1}{C_{DC}} \cdot I_{DC} \cdot \Delta T \quad (50)$$

Assuming that the DC-link current  $I_{DC}$  is directly proportional to the power delivered by the converter  $P_{out}$ , (51) and (52), the worst DC-link voltage drop under a blackout will be produced working at rated active output power. The test bench is designed for 125 kW rated power.

$$P_{out} \approx P_{DC} = \Delta V_{DC} = \frac{1}{C_{DC}} \cdot I_{DC} \cdot \Delta T \quad (51)$$

$$I_{DC} = \frac{P_{DC}}{V_{DC}} \approx \frac{P_{out}}{V_{DC}} \quad (52)$$

The typical criterion is to keep the voltage for half a grid cycle. In a 50 Hz grid the  $\Delta T$  is 10 ms.

$$\Delta T = \frac{T_o}{2} = \frac{1}{2 \cdot f_o} \quad (53)$$

Combining (51)-(53), for a maximum voltage drop of 20% of the DC-link, the required total DC-link capacitance is calculated. The required capacitance is 4.3 mF and 2.4 mF for the 2L and 3L converters, respectively.

### 3.2.3.2. Test bench approach

However, the blackout hold time criteria is not considered for the test bench. This is because the test bench is designed for a laboratory application, so the holdup energy concept is not important. In addition, the actual test bench DC-link comprises both the selected capacitors and the DC power supply connected to the same DC-link. In this specific test scenario, in which the DC power supply regulates the DC-link voltage to the given reference, the specific calculation of the test bench DC-AC capacitors losses importance, at least in terms of capacitance.

In any case, the capacitance is selected big enough to keep voltage ripple in a reasonable margin. The behavior of the DC-link is checked by simulation to ensure the correct functioning with the selected capacitance.

The first test is done with 1mF. The same capacitance is selected for 2L and 3Lconverters. Every operation condition that is expected to be tested regarding  $P$  and  $Q$  is tested, and the worst conditions are identified. The DC-link capacitor requirements are calculated according to the worst operation points, and are shown in Table XIV. When the DC-link regulator device is added these requirements will be softer.

**Table XIV.**

DC-link capacitor requirements for a 1 mF capacitance.

Converter	$I_{C,rms, max}$ [A]	$V_{C,max}$ [V]
3 level	111	870
2 level	103	1220

According to those requirements, the capacitors available in the market are checked. The film capacitors are the most suitable for these DC-link applications due to their high current capacity. The total DC-link must fulfil the requirements in Table XIV, but multiple capacitors are selected to create the required DC-link. The capacitor placement and capacitor number are explained further in this chapter in Sections 3.3 and 3.4. Table XV shows the selected capacitors for both converters.

**Table XV.**

Selected capacitors for the test bench.

Converter	Single capacitor				
	Ref	C [mF]	I <sub>RMS</sub> [A]	V <sub>max</sub> [V]	
3 level	Cornell Dubilier 947D271K112AEGSN	1	58	1100	
2 level	Cornell Dubilier 947D102K901CJRSN	0.270	78	900	
Converter	Total DC-link				
	Qty	Connection	C [mF]	I <sub>RMS</sub> [A]	V <sub>max</sub> [V]
3 level	12	2P(each DC-link half per phase)	0.810	348	2200
2 level	8	4P2S	2	312	1800

### 3.2.4. Cooling systems

Each power stack is placed on a metallic heatsink that is air-cooled. The heatsink is specified according to the required dissipation capability and the required dimensions to place the different modules. This is why 2L and 3L converters have separated cooling systems. However, Si and SiC converters use the same cooling system.

Firstly, a simulation sweep is launched with MatLab Simulink® using the models in Section 2.3.2.3, in order to identify the most critical operation points, which are shown in Table XVI. The worst case is identified at maximum current, 110.14 A and 84.44 A for the two and three level converters respectively. The power factor in the worst cases is 0.95. The simulation is done at 125 kVA and maximum switching frequency, 10 kHz for SiC and Si technologies.

The maximum junction temperature of the semiconductors is set at 125 °C, and the required heatsink thermal resistance calculated using Foster thermal networks tuned with values provided by the manufacturers for each semiconductor. The silicon converters suffer the maximum losses and have the most restrictive thermal resistances. Thus, in both cases (2L and 3L), the Si configurations have determined the required heatsinks. According to the simulation results, a single heatsink has been designed for the three phases of the 2L converter, whereas one independent heatsink has been designed for each phase of the 3L converter. The critical losses and the required thermal resistances are gathered in Table XVI. The data shown for the three level converter is for one phase.

**Table XVI.**

Maximum power losses and the required thermal resistance per converter.

Converter	Maximum power loss [W]	Required thermal resistance [k/W]
2L	3360	0.0122
3L	1480 (493 per phase)	0.1 (per phase)

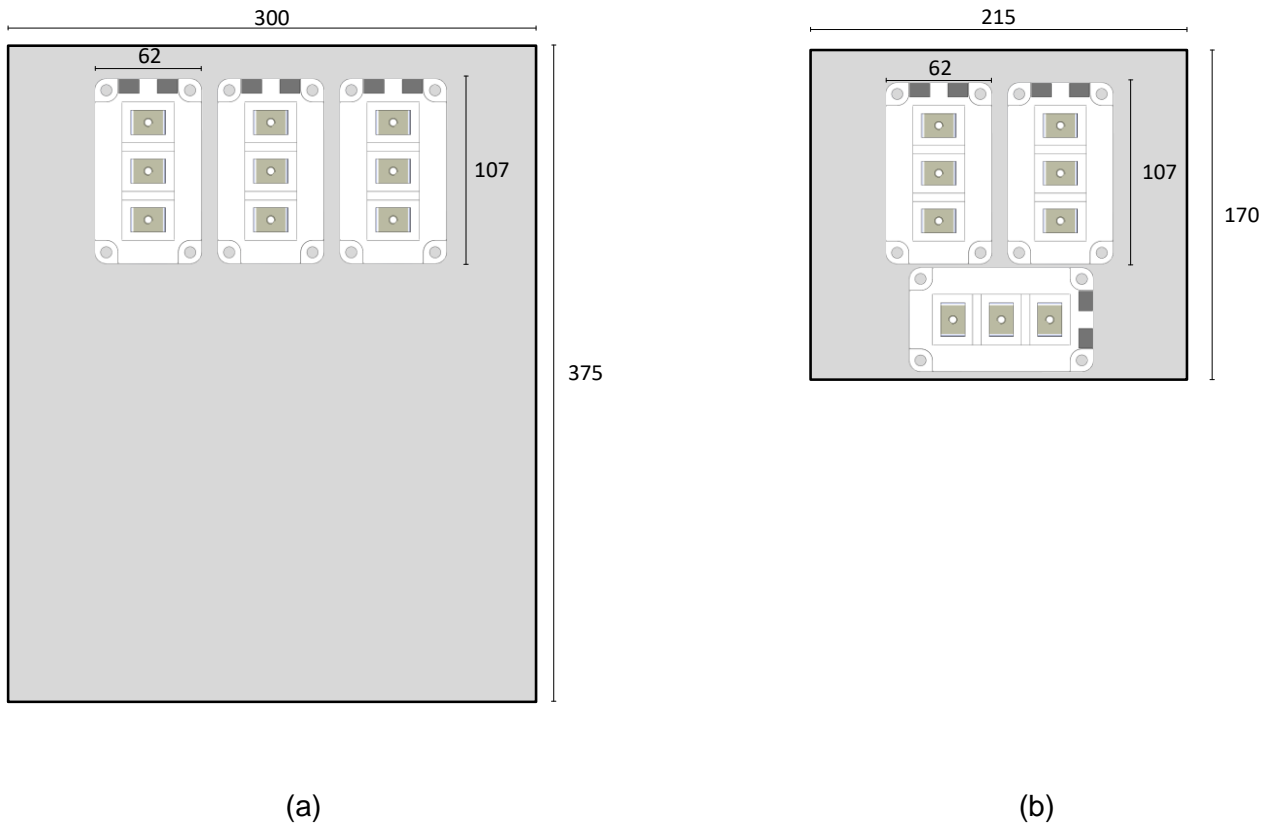


The power electronics component manufacturer GUASCH has provided the required heatsink for each case, which fulfill the thermal resistance requirements, as shown in Table XVII. However, the effective cooling area needs to be studied. This is the area in where the modules are in contact with the cooling system. Both two and three level cooling systems effective areas need to fit three modules.

**Table XVII.**  
Maximum power losses and the required thermal resistance per converter.

Converter	Reference	Thermal resistance [k/W]	Qty
2L	SV-C300B-RG14369/400	0.0122	1
3L	SV-C215A-RG14230/200	0.0249	3

As seen in Figure 3. 3, the dimensions of the cooling systems fit properly with the required three modules of the 2L converter and each of the 3L phases. The layout and module placement details are given further in this work, in Section 3.3. Both the thermal resistance, as well as the effective cooling area occupation requirements are met. The GUASCH offer is accepted and both cooling systems are sent to mechanize. The mechanical adjustments to hold the electronic components on the cooling system are made by GUASCH. Figure 3. 4 shows the selected cooling systems pictures.



**Figure 3. 3.**  
Effective cooling area occupation representation diagram for, (a) two level converter and (b) three level converter.



**Figure 3. 4.**  
Selected cooling systems for, (a) two level converter and (b) three level converter.

### 3.2.5. DC-link discharge resistors

A discharge resistor has been connected in parallel to each of the DC-link capacitor to ensure the proper discharge once the converter is turned off. A discharge time of 4 minutes is defined for the discharge. After that time, the DC-link must be discharged to ensure the safety of any operator. (54) describes the discharge and defines the required resistance. Results are shown in Table XVIII.

$$T_{disch} = 5 \cdot R_{disch} \cdot C_{DC} \quad (54)$$

**Table XVIII.**  
Calculated required maximum DC-link discharge resistance for both converters.

Converter	Resistance [kΩ]
2L	24
3L	59

The resistors are constantly connected to the DC-link to avoid extra controls and switches for shutdown protocol. This means they are consuming power during the operation of the converter. The resistors need to withstand the voltage in the DC-link, as well as be able to dissipate the consumed power. They are placed in the effective cooling areas of the cooling systems to help the dissipation.

The DC-link of the 3L level converter is split into two halves. In addition, each phase is also mounted in a separate power stage. Thus, each phase will have two resistors, one for each half of the DC-link, so summing up, 6 resistors are used for the 3L converter. On the other hand, in the 2L converter the whole DC-link is mounted together, so a single resistor is enough in this case.

Table XIX shows the selected discharge resistors and the characteristics of the resulting system for both converters. The discharge times together with the maximum voltage and the dissipated power requirements are met.

**Table XIX.**

Selected DC-link discharge resistors and the characteristics of the system.

Converter	Reference	R [kΩ]	P <sub>max</sub> [W]	V <sub>max</sub> [V]	Qty	P <sub>diss</sub> [W]	T <sub>disch</sub> [s]
2L	ARCOL/Ohmite HS150 18K J	18	150	2500	1	80	180
3L	ARCOL/Ohmite HS50 47K J	47	50	1250	6	14	127

### 3.2.6. Sensors

Both the 2L and 3L converters need to sense the output voltage and current for control. In addition, the DC-link voltage also needs to be sensed. In the DC-link, a single sensor is enough for the 2L converter. However, two sensors are required in the 3L converter, in order to measure each half of the split DC-link. To prevent unbalances between the two DC-link capacitor voltages, a simple control strategy is used [36].

LEM sensors are used, with current output to avoid signal distortion due to noise. The same voltage and current sensors have been kept for both SiC and Si configurations.

#### 3.2.6.1. Voltage sensors

The output AC voltage in the 3L converter is up to 900 V<sub>AC</sub>, while it is 690 V<sub>AC</sub> in the 2L. According to those voltage levels, the selected sensors are shown in Table XX.

**Table XX.**

Selected voltage sensor to measure the output voltage.

Converter	Reference	Maximum voltage [V]	Qty
2L	LEM DVL 750	750	3
3L	LEM DVL 1000	1000	3

The maximum DC-link voltage is 1600 V for the 3L converter, which means each half of the DC-link would be charged around 800 V in balanced state under rated conditions. However, the possible unbalances must be considered, being necessary to leave certain transient and ripple margin over that rated voltage. In the case of the 2L converter, its DC-link rated voltage value is 1200 V. According to the rated voltages and the described operational margins, the voltage sensors shown in Table XXI have been selected for the DC-link measurement.

**Table XXI.**

Selected voltage sensor to measure the DC-link voltage.

Converter	Reference	Maximum voltage [V]	Qty
2L	LEM DVL 1500	1500	1
3L	LEM DVL 1000	1000	2

### 3.2.6.2. Current sensors

From the converter control point of view, only the output current of the converters needs to be sensed. To do so LEM current sensors are used. One current sensor has been integrated for each phase. Although the maximum current of the semiconductors is 370 A, the sensors have been rated for a reference power of 125 kVA, due to the limitation of the test bench. Thus, the selected current sensors have 200 A maximum current. The same reference is used for both converters. Table XXII shows the current sensors in both converters.

**Table XXII.**

Selected current sensor to measure the output phase current.

Converter	Reference	Maximum RMS current [A]	Qty
2L	LF 205-S/SP3	200	3
3L	LF 205-S/SP3	200	3

### 3.2.7. Control board

Table XXIII shows the control variables for the operation of both converters. In addition, the supply voltages contained in the control board and the control signals are also presented. Table XXIII defines the input and output requirements for the control board. The same control board is used for 2L and 3L converters, so it is designed for the more demanding 3L converter requirements. The spare measurements are avoided in the 2L converter.

The control is performed by the C2000™ LAUNCHXL-F28379D LaunchPad™, which is a Texas Instruments digital signal processor (DSP). This technology is selected because it enables simple and fast programming based on MatLab-Simulink and Code Composer Studio. The C2000 LaunchPad compresses a DSP and several peripherals which allow to measure the required inputs and generate up to 18 PWM signals.

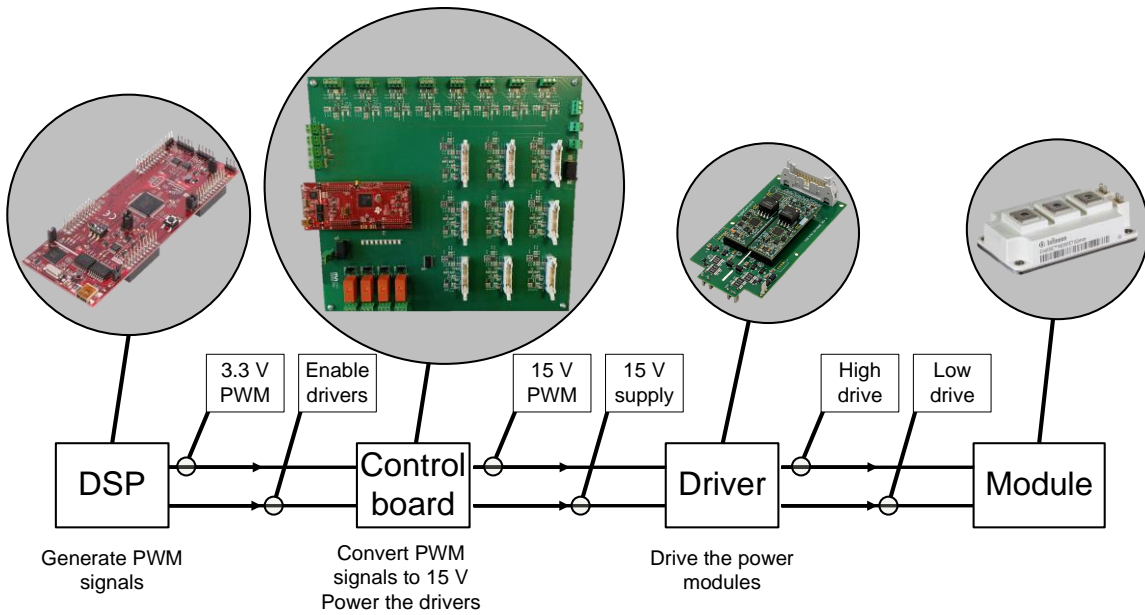
**Table XXIII.**

Selected current sensor to measure the output phase current.

Converter	Variable name	Input/output	Qty	Type
2L	Phase voltage	Input	3	75 mA max analog
	Phase current	Input	3	200 mA max analog
	DC-link voltage	Input	1	75 mA max analog
	±12 V supply voltage	Input	1	Supply voltage
	+5 V supply voltage	Input	1	Supply voltage
	+15 V supply voltage	Input	1	Supply voltage
	+24 V supply voltage	Input	1	Relay activation voltage
	Relay control	Input	4	3.3 V Digital signal
	Enable drivers	Input	3	3.3 V Digital signal
	ePWMx A/B	Input	6	3.3 V PWM
	±12 V supply voltage	Output	7	LEM supply voltage
	+15 V supply voltage	Output	3	Driver supply voltage
	DSP phase voltage	Output	3	0-3 V analog
	DSP phase current	Output	3	0-3 V analog
	DSP DC-link voltage	Output	1	0-3 V analog
High/Low Driver	Output	6	15 V PWM	
3L	Phase voltage	Input	3	75 mA max analog
	Phase current	Input	3	200 mA max analog
	DC-link voltage	Input	2	75 mA max analog
	±12 V supply voltage	Input	1	Supply voltage
	+5 V supply voltage	Input	1	Supply voltage
	+15 V supply voltage	Input	1	Supply voltage
	+24 V supply voltage	Input	1	Relay activation voltage
	Relay control	Input	4	3.3 V Digital signal
	Enable drivers	Input	9	3.3 V Digital
	ePWMx A/B	Input	18	3.3 V PWM
	±12 V supply voltage	Output	8	LEM supply voltage
	+15 V supply voltage	Output	9	Driver supply voltage
	DSP phase voltage	Output	3	0-3 V analog
	DSP phase current	Output	3	0-3 V analog
	DSP DC-link voltage	Output	2	0-3 V analog
High/Low Driver	Output	18	15 V PWM	

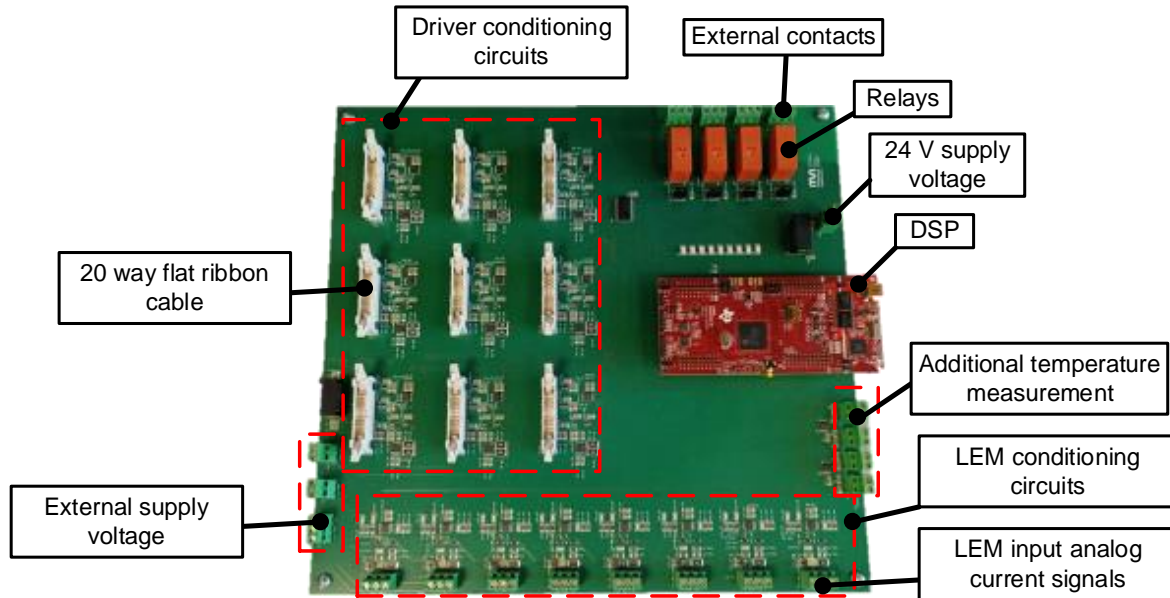
The input control supply voltages are generated by insulated external power supplies. The input analog signals are the output signals of the LEM sensors. Once in the control board and away from any noise source, the analog current signals are converted into 0-3 V output analog signals.

Figure 3. 5 shows the power module driving scheme, starting from the generation of the PWM signals in the DSP. Their ultimate goal is to drive the modules in the converter. The control board converts the input 3.3 V PWM signals coming from the DSP into 15 V PWM signals in the output. However, to activate this conversion the Enable drivers 3.3 V digital input signal must be active. A 20-way flat ribbon cable is used to connect the control board and the drivers. The 62AC1 driver adapter that contains the 2ASC driver core has an equivalent 20 pin input port.



**Figure 3. 5**  
Power modules driving scheme.

The relays are controlled from the DSP with a 3.3 V digital signal. They are activated with the external 24 V supply. They open and close four additional contacts. These are used to control circuit breakers and contactors installed for security in the test bench. Additional temperature measurement ports are available if needed. Figure 3. 6 shows the final designed control board, with the different components and circuits highlighted.



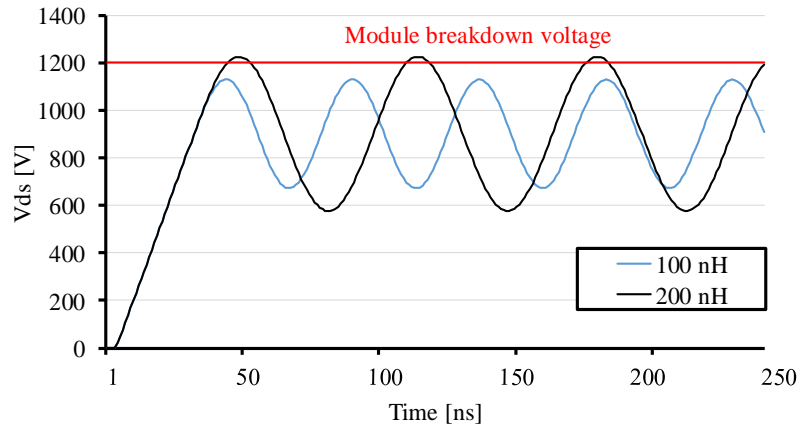
**Figure 3. 6.**  
Designed control board.

### 3.3. Optimal busbar design for 3 level busbar converters

The parasitic components and the layout play a much more important role in converters using SiC because of the high  $dV/dt$  and  $di/dt$  that involves the fast switching. If the designs are not optimized, potentially destructive problems can occur with the use of SiC devices. The most common destructive phenomenon is the voltage overshoot that can occur during the turn off of SiC devices. This overvoltage is produced due to the voltage created in the parasitic inductance of the power loop. This effect is aggravated by SiC semiconductors, since the voltage of an inductor is proportional to the stray inductance  $L_s$  but also to the  $di/dt$  (55). Faster switching with SiC means higher current change rate, and consequently, a higher voltage in the parasitic inductance, which is added to the steady state blocking voltage. As modules become faster, the power loop inductances need to become smaller to prevent this overvoltage phenomena.

$$\Delta V = L_s \frac{di}{dt} \quad (55)$$

For example, the switching of a 1200 V SiC module is simulated in Figure 3. 7, with 100 nH and 200 nH in the power loop. The result represents the importance of a reduced inductance, since the overshoot with 200 nH in the power loop would damage the module in this particular example. In addition, a higher inductance will reduce the resonant frequency and rise the voltage resonance amplitude, increasing the required filter for electromagnetic interference (EMI) compliance.

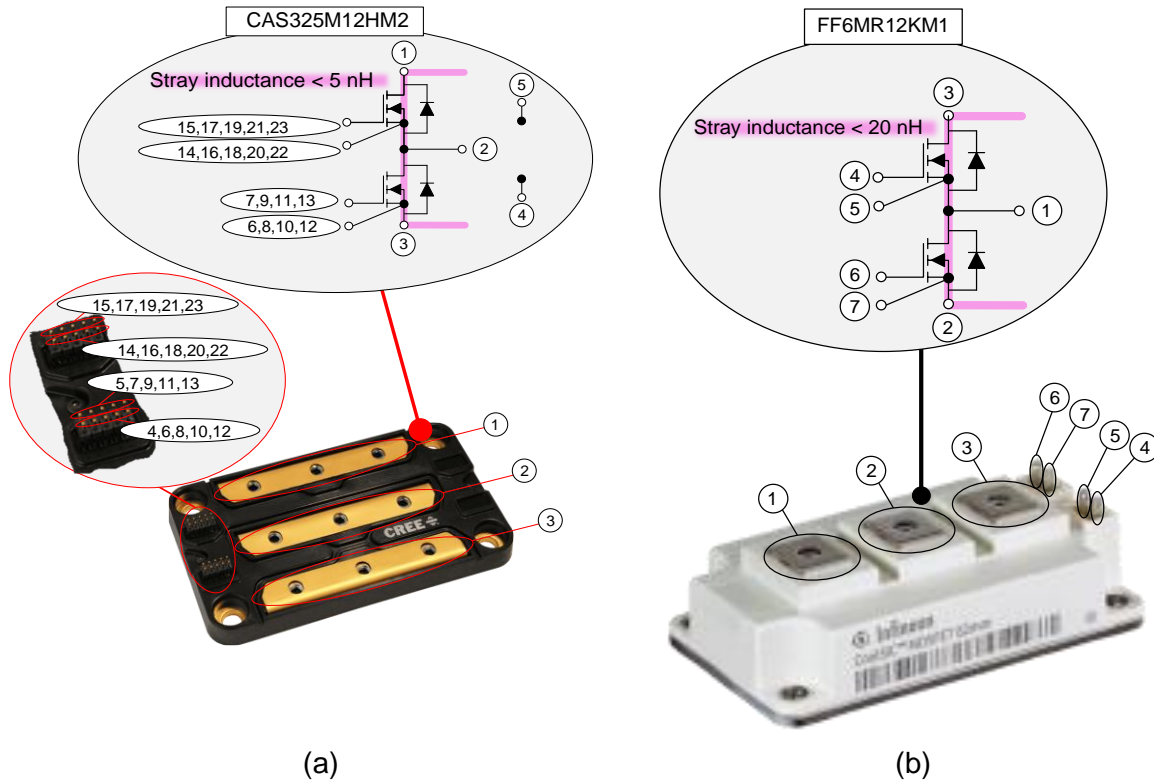


**Figure 3. 7.**  
Simulated turn off voltage comparing different power loop inductances.

The electronic components in the power loop of a power converter are connected by means of a busbar. The current and thus the power is conducted through the busbar, as well as any high frequency disturbances produced during switching transfers, which can produce undesired effects in the semiconductors. That is why the proper design of the busbar is necessary to minimize the resulting parasitic inductance in the power loop. In 3L converter topologies, this task is more complex because multiple switching loops exist [103], [104] and need to be considered in the design. Without careful consideration in the design process to reduce stray inductance, the  $di/dt$  of the switches would have to be reduced to control the overshoot, but with the burden of increasing the switching losses. Another technique to mitigate the overvoltage is to implement snubbers, with similar increment of the energy loss [105], [106]. Therefore, an optimized busbar design is necessary to fully use the potential of SiC technology.

Layout and busbar design have been discussed in the literature, mostly for 2L converters [107]–[109]. Refs. [110]–[114] present procedures to design busbars for 3L converters, but the best results are obtained in [115], where the loop inductances are reduced significantly. The authors propose a design methodology to optimize the busbar in 3L converters. However, the methodology is only tested with HT-3000 package modules. As Figure 3. 8 shows, the pinout of the HT-3000 package is different from the 62 mm module selected in this research work. This directly affects the layout of the converter and thus the design of the busbar. Ref. [116] uses 62 mm modules to build a 3L converter, optimizing the loop inductance, but the inductance is four times higher than the one obtained in [115]. Due to the 62 mm package pinout, asymmetries are also found between switching loops. These asymmetries lead to unbalanced parasitics and voltage stress in the modules. In addition, uneven transient current due to asymmetric impedance reduce the reliability and increase EMI emissions of the converter [117]. Based on the analysis above, the methodology proposed in [115] is adapted for 62 mm modules. A detailed design is presented and experimentally tested for a 62 mm package. In the design, the asymmetries found in [116] are also addressed.





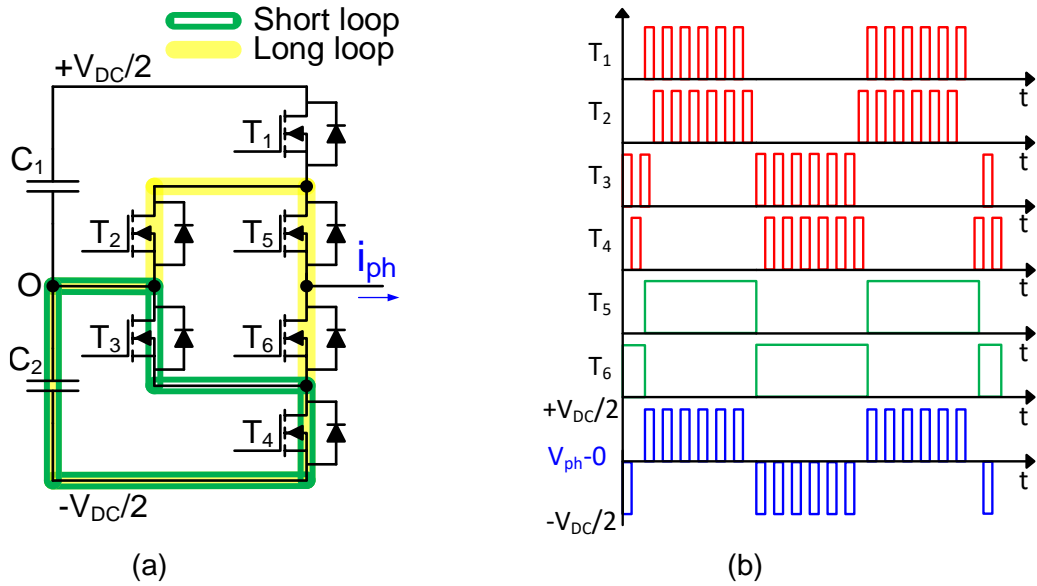
**Figure 3. 8.** High power SiC modules packages detailed pinout comparison, (a) HT-3000 series [118], (b) 62 mm [99].

### 3.3.1. Switching loop evaluation

#### 3.3.1.1. 3 level ANPC topology

To optimize the layout of the converter, it is necessary to understand the operation of the topology and its switching loops. Figure 3. 9 shows a single-phase 3L ANPC, and Table XXIV gathers its switching states. The presence of redundant states (+0 and -0) and the degree of freedom of some switches (for example  $T_3$  in  $+V_{DC}/2$  and  $T_2$  in  $-V_{DC}/2$ ) allows implementing different modulation strategies depending on different objectives. This work considers a modulation in which  $T_1, T_2, T_3$  and  $T_4$  work as high frequency switches, while  $T_5$  and  $T_6$  switch at fundamental frequency, as seen in Figure 3. 9(b). The corresponding output phase voltage  $V_{ph} - 0$  is also shown in Figure 3. 9(b).

The topology has two pairs of symmetrical switching loops. Figure 3. 9(a) illustrates the low pair; the high pair is symmetrical with respect to the neutral point of the DC capacitors. Each of the low pair of loops is closed through the DC link capacitor  $C_2$ . The inductance of each loop resonates with the output capacitance of the respective active device in the loop. To keep the symmetry, the resulting inductance between the high side and low side switching loop pairs should be identical. Thus, it is indispensable to identify the inductances contributing to each switching loop to correctly study them.



**Figure 3. 9.** Single-phase 3L ANPC, (a) topology with low side switching loops, (b) modulation and phase voltage.

**Table XXIV.** Switching states of single phase 3L ANPC converter

State	T <sub>1</sub>	T <sub>2</sub>	T <sub>3</sub>	T <sub>4</sub>	T <sub>5</sub>	T <sub>6</sub>
+V <sub>DC</sub> /2	1	0	0*	0	1	0
+0	0	1	0	0	1	0
-0	0	0	1	0	0	1
-V <sub>DC</sub> /2	0	0*	0	1	0	1

\*T<sub>3</sub> in +V<sub>DC</sub>/2 and T<sub>2</sub> in -V<sub>DC</sub>/2 can be either 1 or 0 depending on the switching strategy.

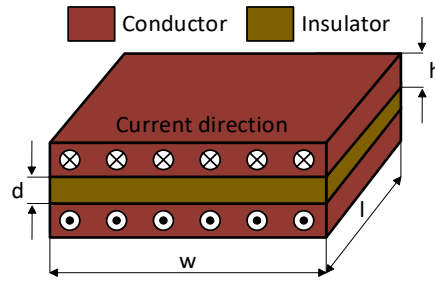
**3.3.1.2. Parasitic inductances and cancelling effects**

Each component in the switching loop has an equivalent series inductance (ESL). Hence, every part should be carefully selected to minimize ESL. Paralleling components is also a simple way to reduce the resulting inductance, at least when mechanical requirements such as weight and volume restrictions allow to do so.

The other parasitic inductance to consider is created by the busbar. The inductance of a single plate is known as self-inductance  $L_s$  and is calculated with (56) [109], [119],

$$L_s = \frac{\mu_0 \mu_r l}{\pi} \left( \frac{1}{8} + \frac{2h}{h+w} \right) \quad (d \ll h || d+h \ll w) \tag{56}$$

where  $\mu_0$  and  $\mu_r$  are the vacuum permeability and the relative permeability of the insulation material;  $l$ ,  $w$  and  $h$  are the length, width and thickness of the plate respectively; and  $d$  is the distance between two adjacent plates, as sketched in Figure 3. 10.



**Figure 3. 10.**  
Two-layer busbar structure with opposite currents.

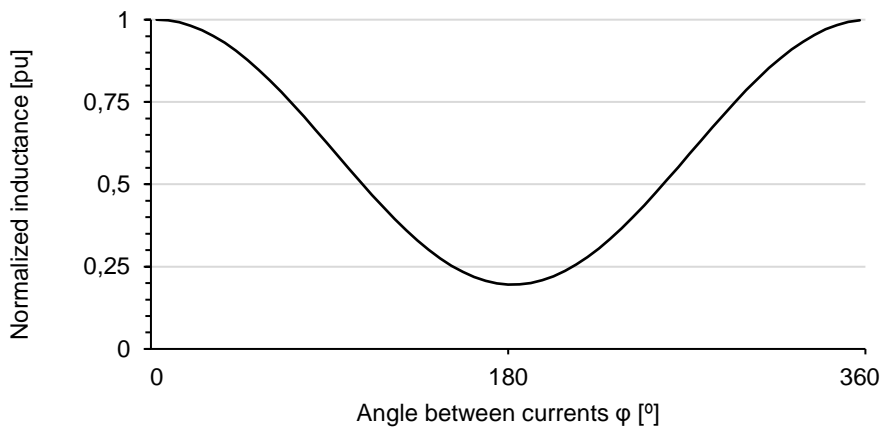
When two plates are overlapped, the mutual inductance  $M$ , has to be added, which is calculated with (57) [120]. The resulting inductance  $L_{tot}$  is (58),

$$M = \frac{\mu_0 \mu_r l h}{\pi \sqrt{4(d+h)^2 + kw^2}} \cos \varphi \tag{57}$$

$$L_{tot} = 2L_s + 2M \tag{58}$$

where  $k$  is the correction factor and  $\varphi$  is the angle between the currents in each plate. Magnetic cancelation can be used to reduce the resulting inductance, forcing opposite currents in adjacent plates [108], as in Figure 3. 10. Doing so,  $\varphi$  is  $180^\circ$  and the resultant  $L_{tot}$  is (59), obtaining the minimum inductance, as shown in Figure 3. 11.

$$L_{tot} = \frac{\mu_0 \mu_r l}{\pi} \left( \frac{1}{4} + \frac{4h}{h+w} - \frac{2h}{\sqrt{4(d+h)^2 + kw^2}} \right) \tag{59}$$



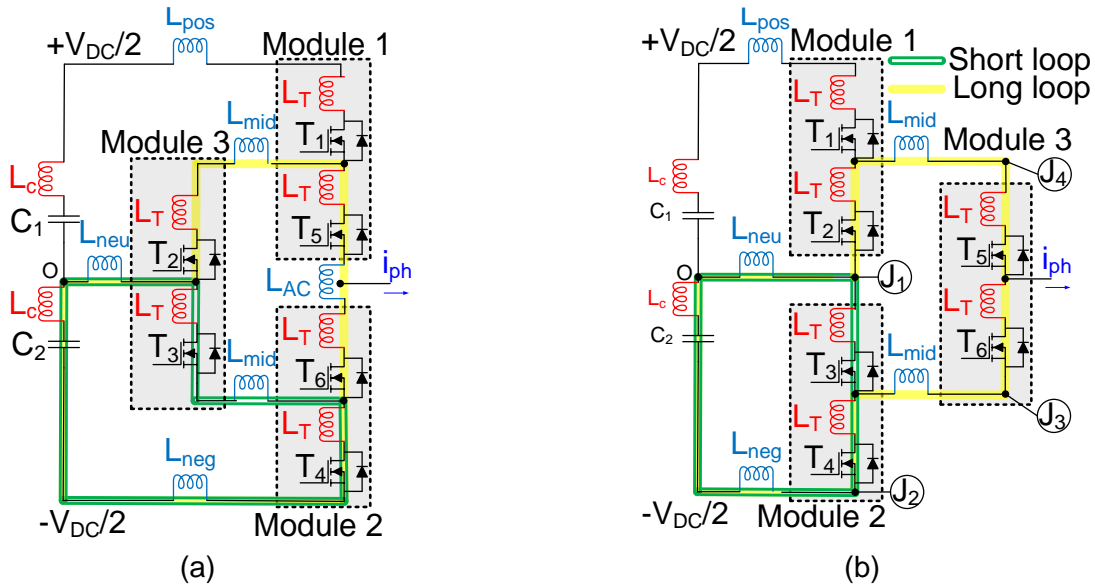
**Figure 3. 11.**  
Normalized inductance depending on the angle between currents  $\varphi$ .

### 3.3.2. Busbar design

#### 3.3.2.1. Phase leg formation

To create a 3L ANPC leg with half-bridge modules, three modules are required. However, as Figure 3. 12 shows, two different options exist. After drawing the modules for both options, the busbar parts required for connection are also drawn for analysis.

Next, all the inductances in the low switching loops for both options are noted in Table XXV. If each busbar part is considered independent, the total parasitic inductance  $L_{tot}$  of each loop is (60)-(63). Comparing the short loops  $L_{tot,sl}$ , one less busbar connection is identified in the optimized phase leg, shown in Figure 3. 12(b). Thus, this second optimized option is selected for the design.



**Figure 3. 12.**

3-level ANPC phase leg formation options considering parasitic inductances, (a) non-optimized phase leg, (b) optimized phase leg.

**Table XXV.**

Resulting total inductance for considered phase leg options.

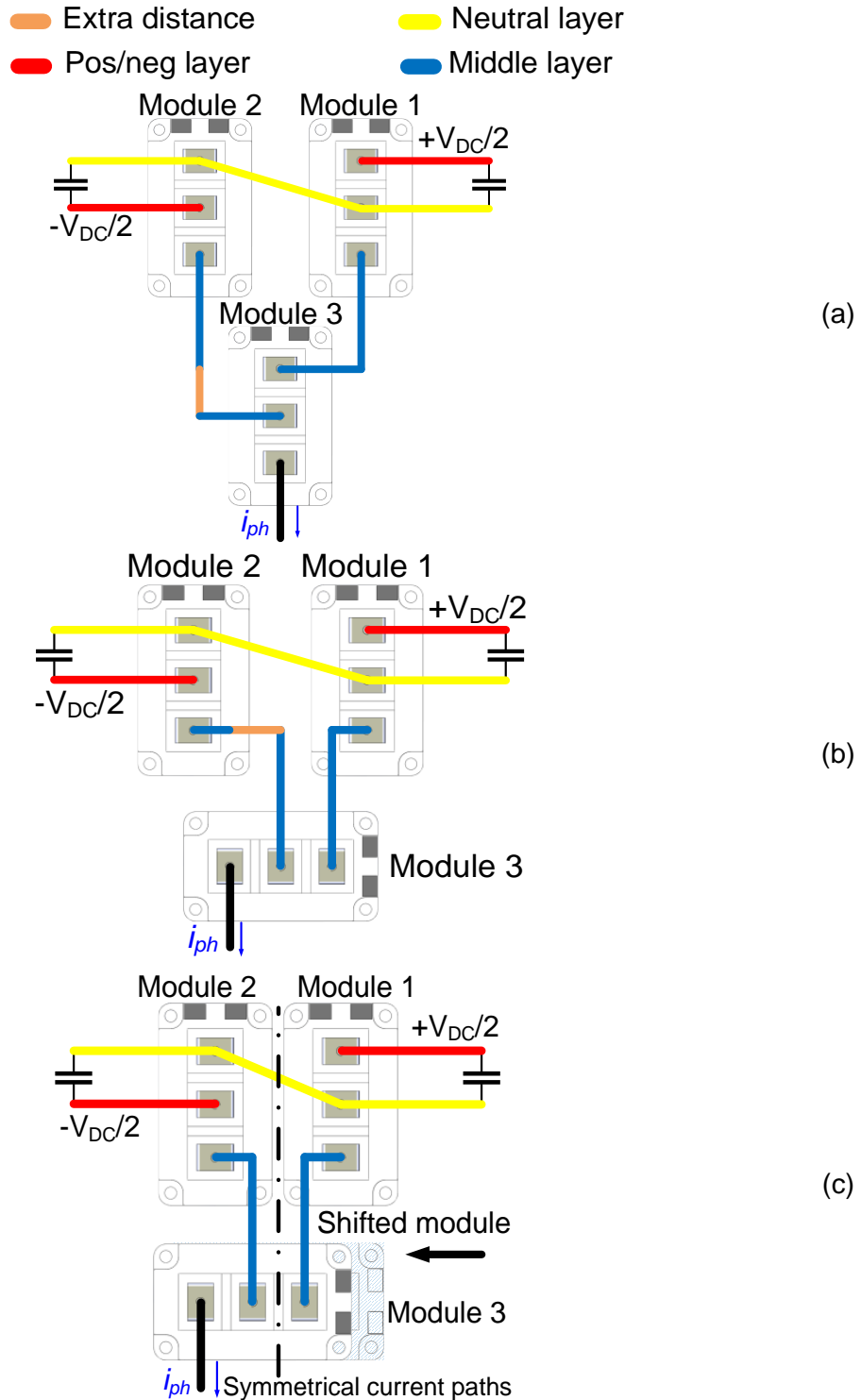
Switching loop	Phase leg option		
Short loop	Non-optimized phase leg	$L_{tot,sl} = L_c + 2L_T + L_{neu} + L_{mid} + L_{neg} *$	(60)
	Optimized phase leg	$L_{tot,sl} = L_c + 2L_T + L_{neu} + L_{neg} *$	(61)
Long loop	Non-optimized phase leg	$L_{tot,ll} = L_c + 4L_T + L_{neu} + L_{mid} + L_{AC} + L_{neg} *$	(62)
	Optimized phase leg	$L_{tot,ll} = L_c + 4L_T + L_{neu} + L_{mid} + L_{mid} + L_{neg} *$	(63)

\* $L_{neg}$  is equivalent to  $L_{pos}$  in upper side loops

#### 3.3.2.2. Module placement

Determining the module placement is the next design step. The challenge is to create symmetrical current paths to reduce parasitic unbalances, while keeping the minimum distance between modules. To do so the busbar layers in Figure 3. 13 are studied. The vertical placement in Figure 3. 13(a) works for the HT-3000 package, but it creates a vertical

asymmetry for the 62 mm package due to the different pinout. As sketched in Figure 3. 13(b), rotating Module 3 solves the vertical asymmetry related to the pinout. But it should not be aligned with the mechanical center, because a horizontal asymmetry is created. With the shift applied to Module 3 in Figure 3. 13(c), symmetrical current paths and switching loops can be achieved in theory. This analysis is conceptually valid, but is subject to manufacturing restrictions.



**Figure 3. 13.** 62 mm module placement options considering current paths in busbar layers, (a) vertical placement, (b) rotated module placement, (c) rotated and shifted module.

### 3.3.2.3. Capacitor placement

The DC-link capacitor is part of both switching loops, so it is a key component of the design. It is important to minimize the parasitic inductance added by this component, even more in high current applications. This is because the contribution of this component to the total inductance of the loop can be significantly high when compared to other parts. The ESL of the capacitor should be a main factor in the part selection. A good option is to use metallized film capacitors, with high current ratings and reduced ESL when compared to electrolytic counterparts. This choice is recommended in [115] and done in this design.

If a single capacitor is used as shown in Figure 3. 14(a), the full ESL will be added to the switching loop inductance. A good technique to reduce the ESL is to parallel many parts, as illustrated in Figure 3. 14(b). However, if parallel capacitors are placed oppositely, as recommended in [121] and shown in Figure 3. 14(c), the magnetic cancellation effects described in Figure 3. 11 can be achieved, reducing the parasitic inductance around 80 %. The proposed design uses this last technique.

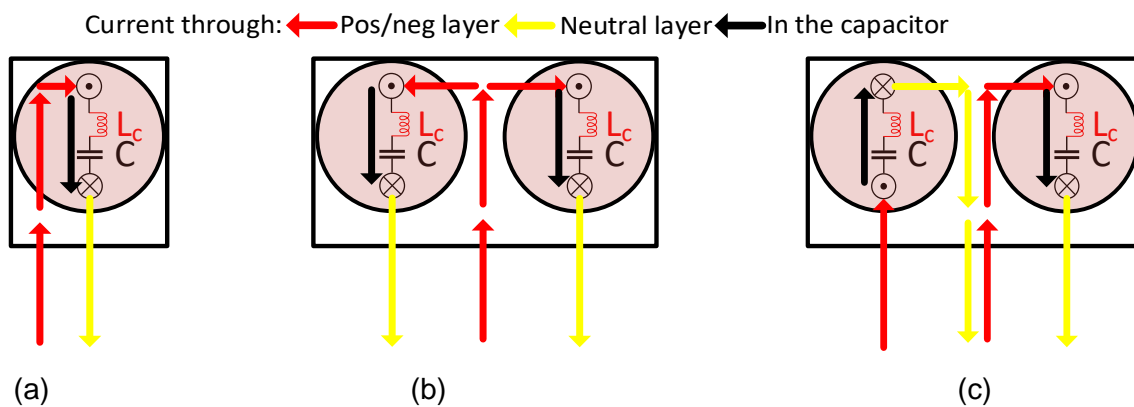


Figure 3. 14.

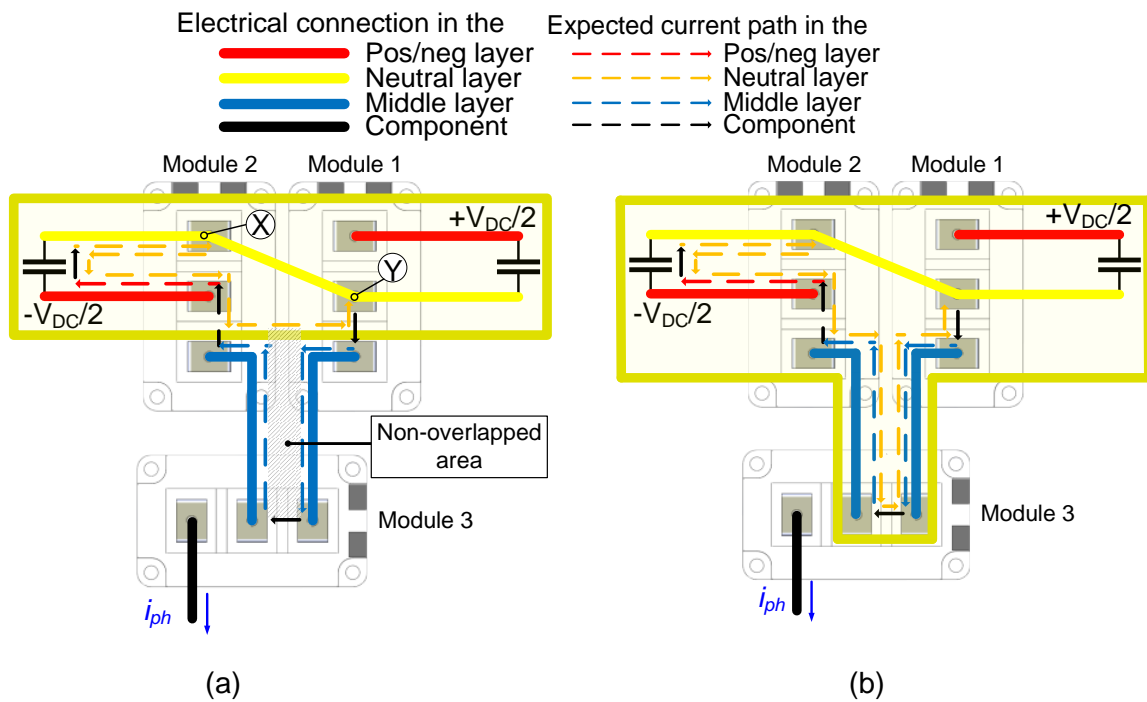
Capacitor placement options, (a) single capacitor, (b) parallel capacitors, (c) optimized parallel capacitors.

### 3.3.2.4. Neutral layer design

The neutral layer design should be analyzed carefully because both pairs of switching loops share it. Based on Figure 3. 13, this layer is not connected to Module 3. Then, a small layer like the one sketched in Figure 3. 15(a) with the yellow area, connecting both capacitors with Modules 1 and 2 is enough for the topology operation. However, and following the methodology proposed in [115], the return path of the current should also be considered. To do so, the long loop is studied.

Figure 3. 12(b) shows that the long loop goes through the three modules. Taking the low long loop as an example, Figure 3. 15(a) represents the expected current path in a small neutral layer, not covering Module 3. As the returning current in the neutral layer does not have the option to overlap to its ongoing opposite current in the middle layer, an area (shaded in black between Module 3 and Modules 1 and 2) is formed. The parasitic inductance of the loop is increased because the cancelling effect in (59) is not applied.

The optimized neutral layer in Figure 3. 15(b), represented with the yellow area, overlaps Module 3, allowing the current in the long loop to flow as illustrated. By doing so, opposite currents are allowed. Ref. [115] simulates this effect using Ansys Q3D, achieving 6.3 times lower parasitic inductance with the optimized neutral layer. This last option is the selected one for the proposed design.



**Figure 3. 15.**

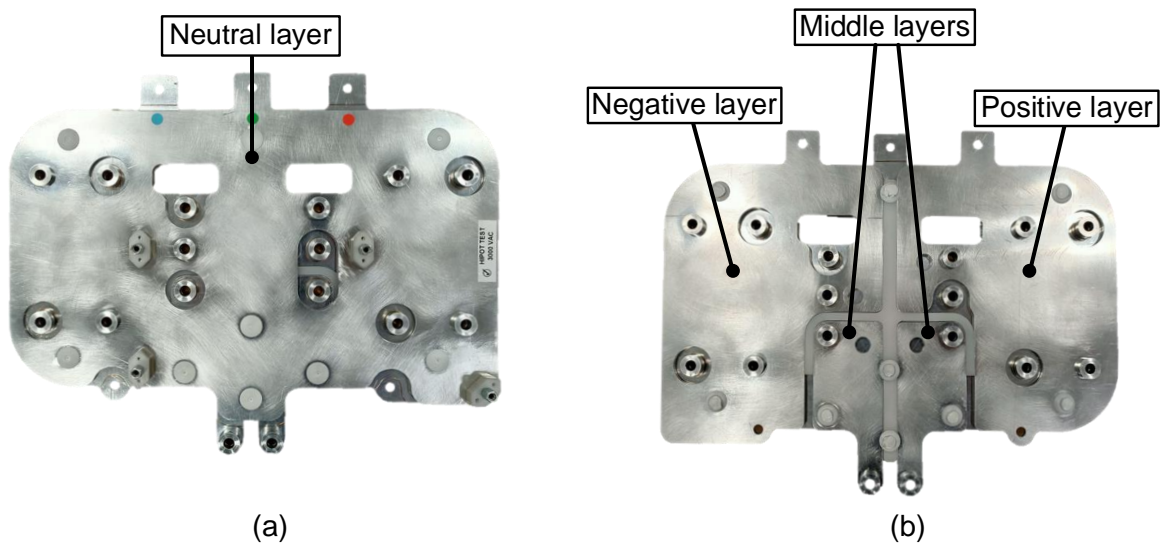
Neutral layer design options with the expected current paths of the low long switching loop, (a) non-optimized neutral layer, (b) optimized neutral layer.

### 3.3.3. Design evaluation by impedance analyzer

#### 3.3.3.1. Evaluation methodology

The 3L ANPC converter busbar that has been designed and manufactured according to the process described in previous stages is shown in Figure 3. 16. Once assembled, the different parasitic inductances are tested using the Bode 100 impedance analyzer and B-WIC impedance adapter. This setup allows to run impedance measurements between 1 Hz and 50 MHz. Based on the rise and fall time [122], shown in the datasheet of the module used in this design [99], the inductance at 25 MHz is analyzed. Following the example provided in the user manual [123], open, short and load calibrations are performed before measuring. The modules are shorted to perform the measurements, but the capacitors are included. Connection points shown in this section match the ones shown in Figure 3. 12(b) and Figure 3. 15(a).

To evaluate the benefits of the proposed design techniques, the dismissed options are created and also tested in the lab. Finally, the results are compared to other designs, considering the package of the modules used in each case.

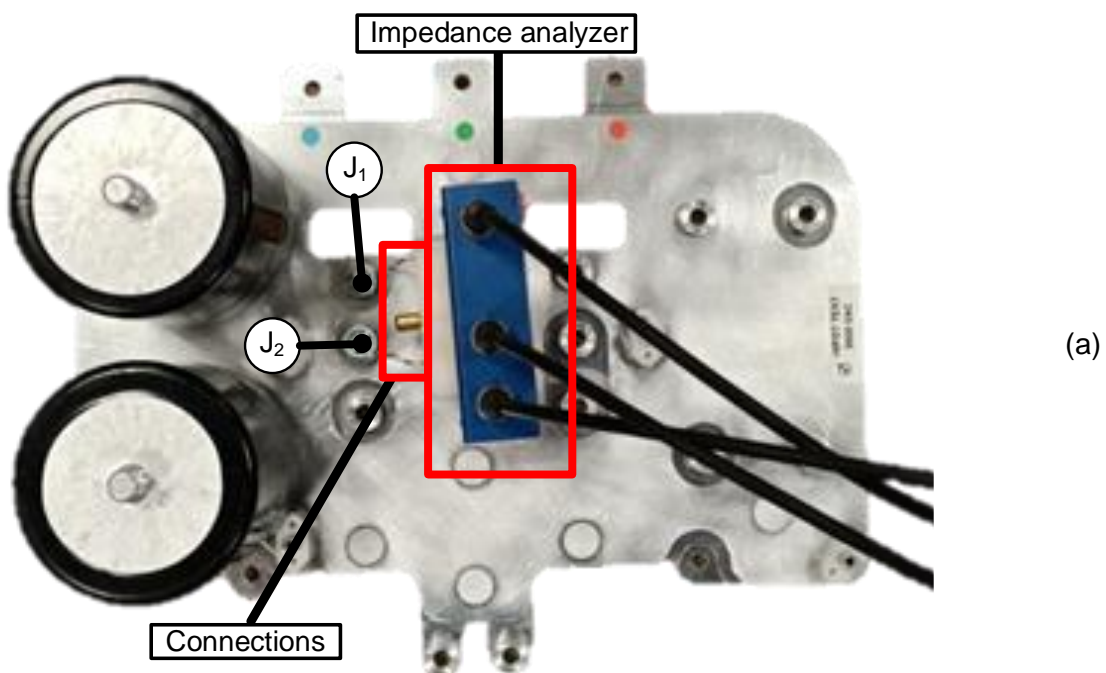


**Figure 3.16.** Manufactured busbar with its layers, (a) top view, (b) bottom view.

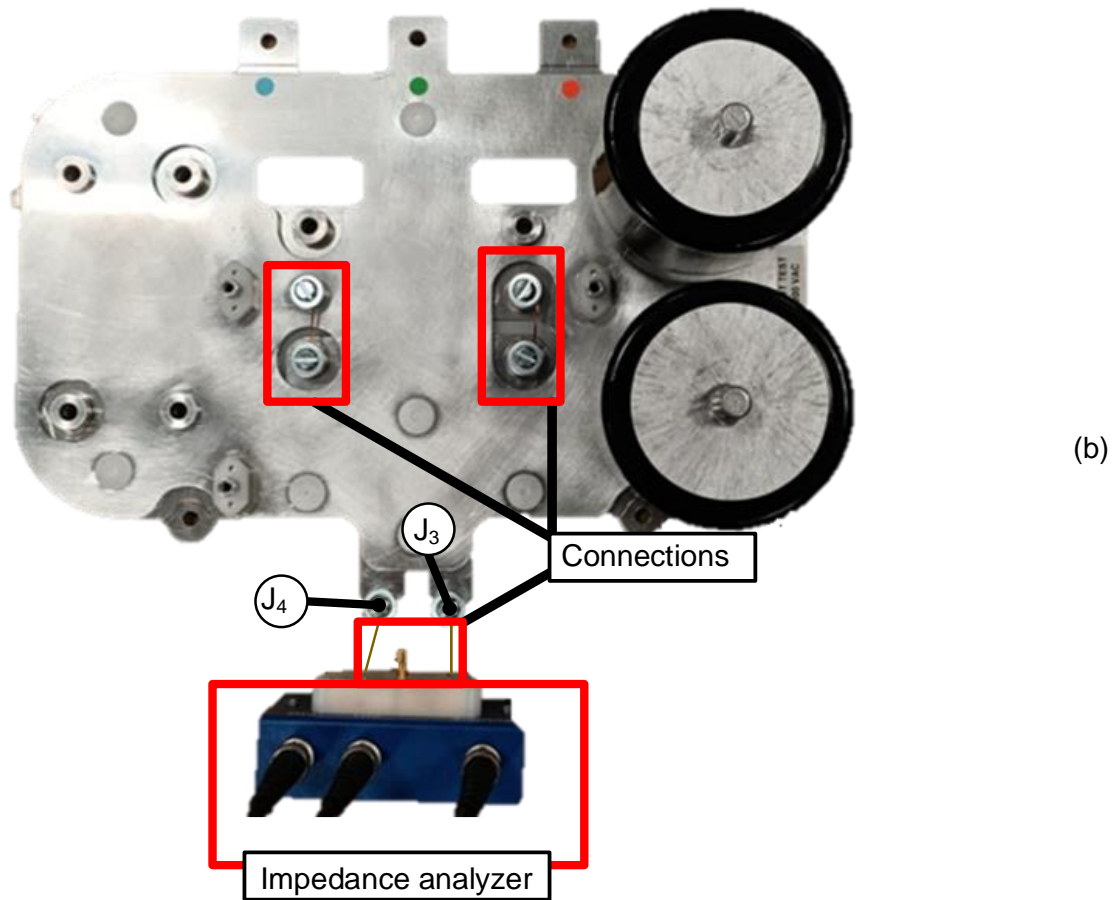
### 3.3.3.2. Commutation symmetry evaluation

The inductance of both pair of switching loops is measured with the impedance analyzer. Figure 3.17(a) shows the testing of the upper side short loop, with the positive side of the DC bus connected. Figure 3.17(b) shows the testing of the lower side long loop, with the negative side of the DC bus connected.

Table XXVI shows the results of the experimental measurements. These results are compared to the ones in [116], where 62 mm modules were used, and the asymmetry in both designs is assessed. The proposed design achieves 91 % and 90 % reduction in the asymmetry for short and long loops respectively. The inductances of the prototype are 4.17 nH for the short loop and 8.41 nH for the long loop. Modules are not considered for these measurements, but the capacitors are included.







**Figure 3. 17.**  
Busbar impedance testing, (a) high side short loop, (b) low side long loop.

**Table XXVI.**  
Symmetry test results and asymmetry comparison.

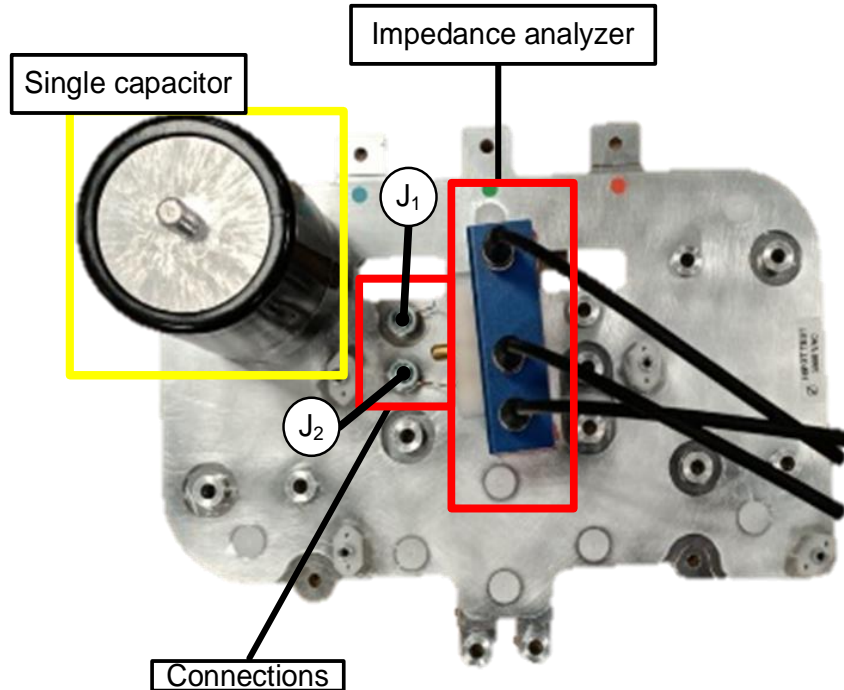
Switching loop	Inductance measured in the proposed design [nH]	Inductance measured in [116] [nH]
High short loop	4.17	15.82
Low short loop	4.19	16.71
Asymmetry [%]	0.48	5.33
High long loop	8.53	27.42
Low long loop	8.41	23.39
Asymmetry [%]	1.37	14.69

### 3.3.3.3. Capacitor placement evaluation

To test the inductance of the single capacitor option, a capacitor is removed from the busbar. The test bench configured for this measurement is shown in Figure 3. 18. The inductance of the parallel capacitors option in Figure 3. 14(b) is estimated to be one half of the measured single capacitor value.

The inductance of the optimized parallel capacitors in Figure 3. 14(c) is the same as the short loop in Figure 3. 17(a) because the modules are not considered for the measurement.

The configuration with optimized parallel capacitors achieves the lowest inductance. Obtaining a reduction of 78.5 % and 57 % compared to a single capacitor and parallel capacitors configurations respectively. Table XXVII summarizes the measurement results, presenting the applied method.



**Figure 3. 18.**  
Single capacitor parasitic inductance measurement.

**Table XXVII.**  
Capacitor placement test results.

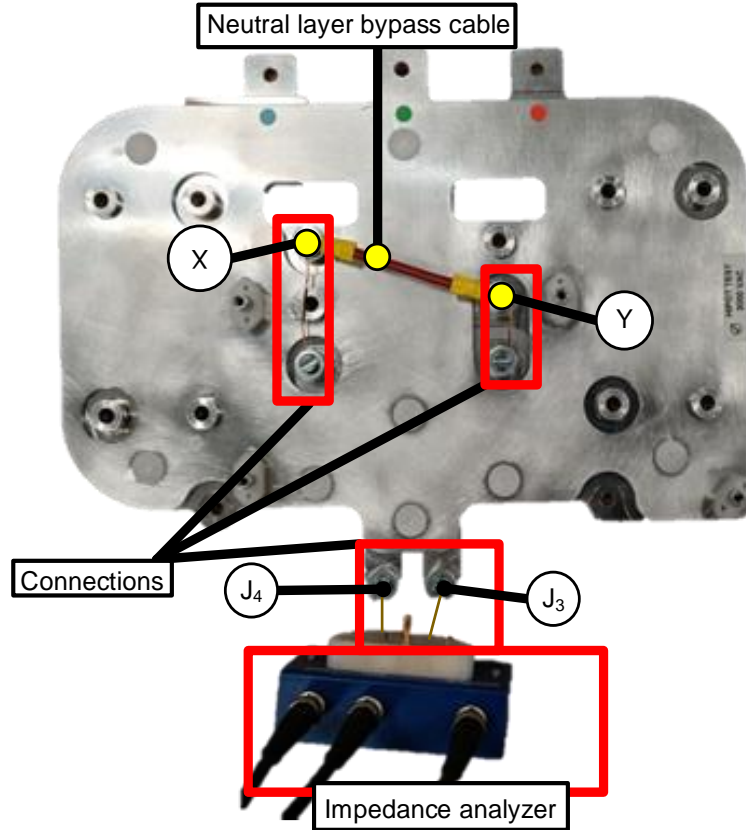
Configuration	Inductance [nH]	Method
Single capacitor	19.41	Measured
Parallel capacitors	9.70	Estimated
Optimized parallel capacitors	4.17	Measured

**3.3.3.4. Neutral layer design evaluation**

To emulate the non-optimized neutral layer in Figure 3. 15(a), a bypass cable is used. As illustrated in Figure 3. 19, this cable connects Modules 1 and 2, omitting the neutral layer in the prototype through insulation. The optimized neutral layer should not be connected to the measured loop for this test, thus capacitors must be removed from the busbar, as they are connected to this layer. The returning current can only flow throw the bypass cable, creating the scenario in Figure 3. 15(a). In addition, points X and Y in Figure 3. 19 match those in Figure 3. 15(a) for clarity. The virtual scenario created for this test is a way of obtaining a measurement of a neutral layer that does not overlap ongoing currents.

The inductance of the created non-optimized neutral layer is measured. According to the analysis in Figure 3. 15, the measured value should be compared to the long loop. However, the long loop goes through the capacitors, so the inductance of the optimized parallel capacitors (4.17 nH) is added to the measured inductance. Thus, the total estimated inductances for neutral layers are shown in Table XXVIII.

The inductance of the long loop with the non-optimized neutral layer is 82.3 % higher. This result shows the importance of actively overlapping layers to allow returning currents to flow in the outgoing path. In addition, the result is consistent with the simulation performed in [115] which shows an increment of 6.3 times in the inductance of the design without the full overlapping neutral layer. The inductance measured in the created non-optimized neutral layer is 5.6 times higher compared to the optimized one, matching both results.



**Figure 3. 19.**  
Non-optimized neutral layer inductance measurement with bypass cable.

**Table XXVIII.**  
Neutral layer optimization test results.

Option	Inductance [nH]
Non optimized middle layer	47.72
Optimized middle layer	8.44

**3.3.3.5. Loop inductance evaluation**

Table XXIX compares loop inductances achieved in the proposed design with other 3L converters. Module inductances are also added to the results for a fair comparison. The package used in each design is noted too. The proposed design achieves significantly lower parasitic inductance than most of the other designs.

Comparison with [116] is especially important as the same package is used, even if the parasitic inductance of the devices are different. In addition, the asymmetry issues found with 62 mm package are addressed. Similar inductances as in the reference design [115] are achieved if the modules are not considered. The results show the possibility to apply the design methodology presented in [115] to other packages. The comparison also validates the design changes done to adapt the methodology to a new pinout.

**Table XXIX.**

Loop inductance comparison considering modules.

Reference	Device package	Single device $L_T$ [nH]	DC bus [kV]	Short loop [nH]	Long loop [nH]
[115]	HT 3000	2	1.0	7	18
[114]	EconoDUAL	10	2.4	n/a	115
[111]	HiPak	24	2.0	78	208
[124]	Semitrans 4	20	1.2	55	135
[125]	n/a	n/a	n/a	96	150
[126]	Semitrans 4	20	n/a	48	76
[112]	PrimePak™2	5	1.1	95	118
[116]	62 mm	7	0.9	30	51
Proposed	62 mm	9	0.8	22	44

### 3.3.4. Design evaluation by switching

#### 3.3.4.1. Evaluation methodology

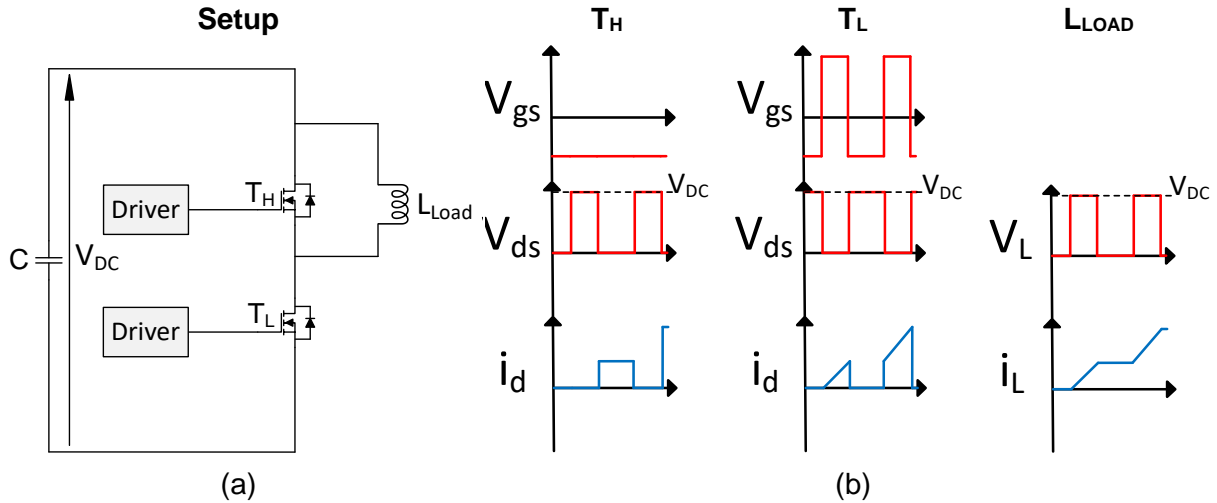
The different parasitic inductances are tested using the switching waveforms obtained in the laboratory. To do so, the double pulse testing (DPT) technique presented in the following section is used. The short loop, the long loop and the short loop with a single capacitor are switched and the waveforms analyzed. The results are then compared to the measurements in the previous section.

#### 3.3.4.2. Double pulse test

The switching validation is done by performing a DPT to the 3L ANPC power stage. This test evaluates the layout and the switching of the converter. With the waveforms obtained in the DPT, the parasitic inductance of the switched loop can be calculated, as explained in Section 3.3.4.4.

Figure 3. 20 (a) shows the setup for the DPT. In this case,  $T_H$  is the non-active switch, and is always OFF acting like a freewheeling diode, while  $T_L$  is the active switch, performing the two pulses. The test can be performed with a single half bridge module.

To test the layout, the device under test (DUT) must switch with current. The activation of  $T_L$  during the first pulse creates a linearly rising current through  $L_{Load}$  inductor. Then, this active switch  $T_L$  is switched-off and the body diode of the non-active switch acts as a freewheeling diode which keeps the inductor current conducting. This transitions allows testing the turn off commutation of the DUT. Later, after a previously calculated time, the DUT is switched-on under the desired load current in the second pulse. Thus, a turn on and a turn off commutation of the DUT are generated and monitored.



**Figure 3. 20.** Double pulse test diagram, (a) the setup, (b) waveforms of the different elements.

Analyzing the voltage and current waveforms of the DUT, the switching energy can be calculated. However, in this specific stage, the DPT has been used to measure the inductance of the switching loop under different conditions. The test is also used to predict possible destructive phenomena, especially regarding the overvoltage during turn off.

**3.3.4.3. Selected voltage and current probes**

The DPT waveforms are captured with voltage and current probes. The voltage probe needs to be rated at least as high as the breakdown voltage of the modules. This is 1200 and 1700 V for the semiconductors in the 3L and 2L converters, respectively. In addition, the probe needs to guarantee a high enough bandwidth to measure the fast transients. Insulated probes are preferred to avoid grounding issues.

Current probes need to be able to measure up to 200 A. The dynamic capability is also important, as high  $di/dt$  is expected in the SiC modules. Finally, the current probe needs to fit in the power circuit, so physical restrictions also exist.

Table XXX shows the selected voltage and current probes. The same probes are used for both 2L and 3L converters, as well as for Si and SiC converters. In addition, Figure 3. 21 shows how the Rogowski coil fits the 62 mm modules terminals for correct measurements. All the measurement requirements are met with the selected voltage and current probes.

**Table XXX.** Selected voltage and current probes.

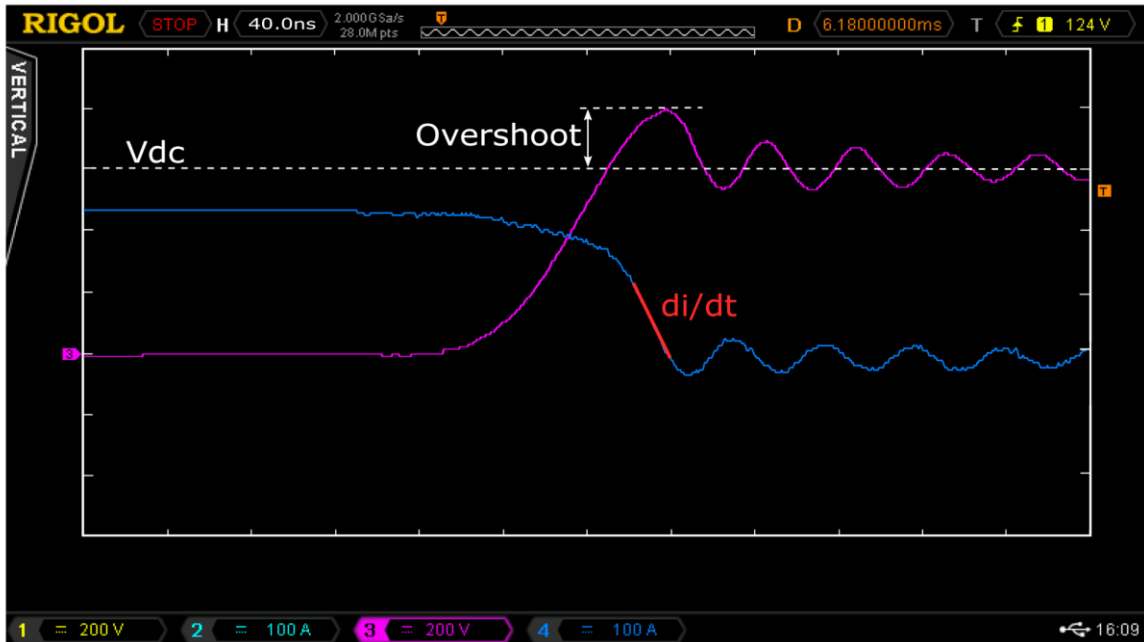
	Reference	Type	Maximum rating	Bandwidth or $di/dt$	Qty
<b>Voltage probe</b>	PMK BumbleBee	Insulated	2000 V	400 MHz	2
<b>Current probe</b>	CWT MiniHF 3/B/4/100/5	Rogowski coil	600 A	100 A/ns	2



**Figure 3. 21.**  
Physical configuration of the current measurement on 62 mm modules.

#### 3.3.4.4. Inductance calculation from the DPT

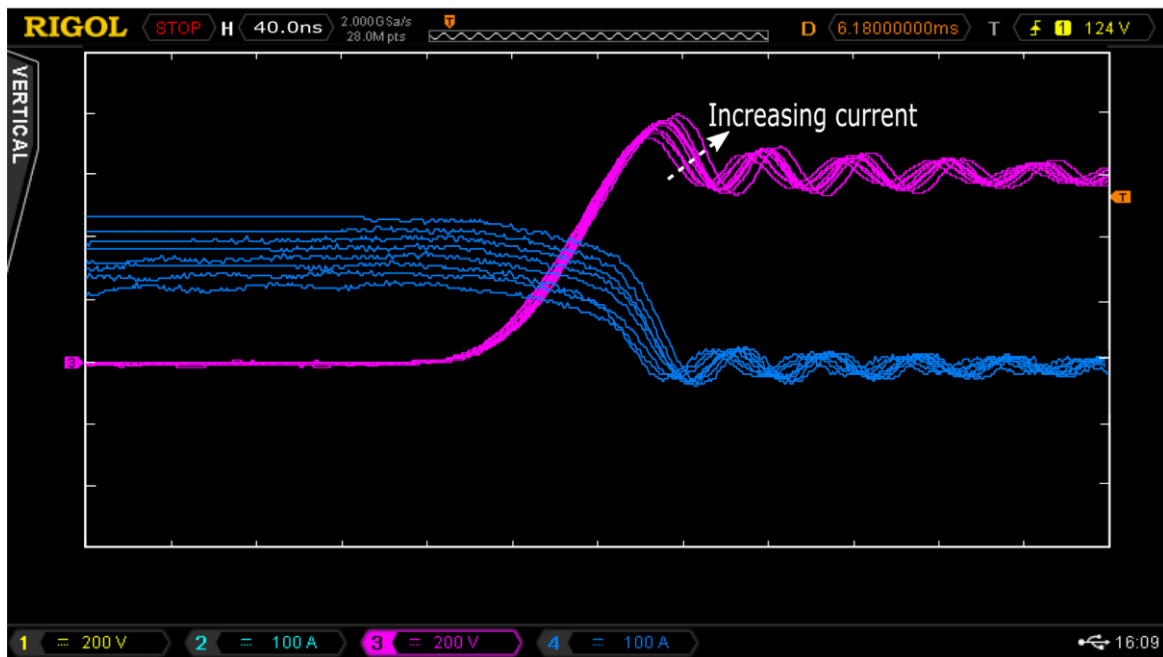
Equation (55) is used to calculate the inductance of the switched loop. The overshoot represents the voltage in the loop inductance, and can be obtained by the difference between the maximum peak voltage and the DC value. The  $di/dt$  is the turn off slope of the current. These information are obtained from the analysis of the switching waveform data, as done in Figure 3. 22.



**Figure 3. 22.**  
Data acquisition from the turn off waveform in a DPT to calculate the loop inductance.

### 3.3.4.5. Short loop

First, the short loop is tested switching 600 V and increasing the current from 125 to 225 A, Figure 3. 23 shows the turn off waveform of the short loop for different currents. The analysis described in the previous section is performed for every switching condition, and summarized in Table XXXI. The maximum overshoot suffered in the switching of the short loop is of 190 V, which is given at maximum current. Also, the  $di/dt$  increases as the switched current is also increased, achieving a maximum of 8.86 A/ns.



**Figure 3. 23.**  
The turn off of the short loop for different currents.

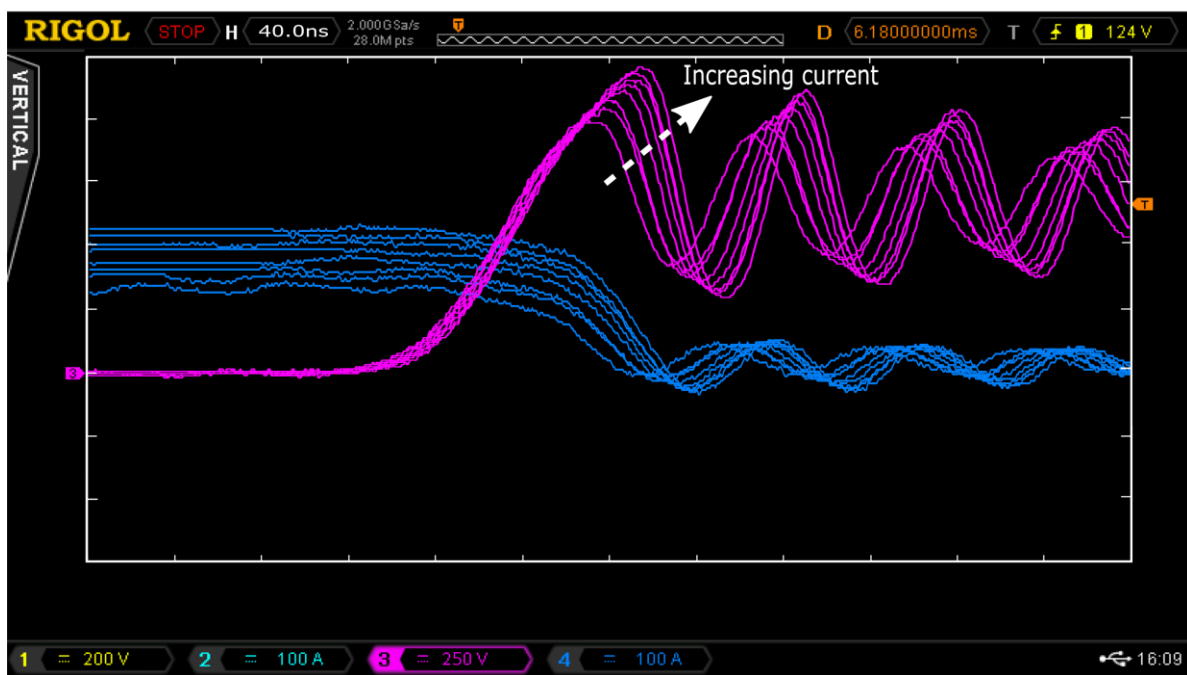
**Table XXXI.**  
The short loop calculated inductance by switching evaluation for different currents.

Current [A]	$di/dt$ [A/ns]	Overshoot [V]	Calculated inductance [nH]
125	4.83	110	22.9
140	5.64	126	22.4
155	6.05	142	23.5
170	6.44	150	23.3
185	7.25	159	21.9
195	7.25	166	22.9
210	8.05	174	21.6
225	8.86	190	21.5

The calculated inductance values are consistent over all the switching currents. In addition, they match well with the busbar inductances measured in Section 3.3.3.5 and shown in Table XXIX. The measured inductance with the impedance analyzer is 22 nH considering the module that is part of the switching loop. The switching test shows close results, validating the impedance analyzer measurements for the short loop.

### 3.3.4.6. Long loop

Next, the long loop is tested in the same way. Figure 3. 24 shows the turn off waveform of the long loop for different switched currents. Table XXXII presents the characteristics of the analyzed waveforms. The maximum overshoot is higher than in the short loop, 502 V at maximum current. The calculated inductances are also consistent for all the switched currents.



**Figure 3. 24.**  
The turn off of the long loop for different currents.

**Table XXXII.**  
The long loop calculated inductance by switching evaluation for different currents.

Current [A]	$di/dt$ [A/ns]	Overshoot [V]	Calculated inductance [nH]
115	4.83	310	64.1
130	5.37	358	66.6
140	5.8	382	65.8
155	6.44	422	65.5
165	7.03	438	62.3
180	7.5	454	60.4
195	7.73	486	62.8
210	7.73	502	64.9



However, the results do not match the measurements in Section 3.3.3.5 and shown in Table XXIX. The main difference with the measurements performed on the short loop is that more modules are part of the long loop. While the measurement of the short loop is direct, and only adding the inductance of a module gives good measurement accuracy, this is not the case in the long loop. All three modules in a single phase of a 3L ANPC converter are part of the long loop, having to use bypass connections for the impedance measurement, as shown in Figure 3. 17. This leads to inaccurate results, as confirmed by the disparity of the results in Table XXIX and Table XXXII.

### 3.3.4.7. Capacitor placement optimization

Finally, the configuration with the single capacitor, shown in Section 3.3.2.3 is also tested with the DPT. Figure 3. 25 shows the turn off of the short loop comparing the waveforms with the optimized capacitors and the single capacitor. The registered values are shown in Table XXXII. The maximum overshoot is 286 V which is higher than the value registered with the optimized cap. Regarding the  $di/dt$ , the maximum value is 7.73 A/ns, achieved at maximum current. The achieved current reduction rate is slower than with the optimized capacitors layout.

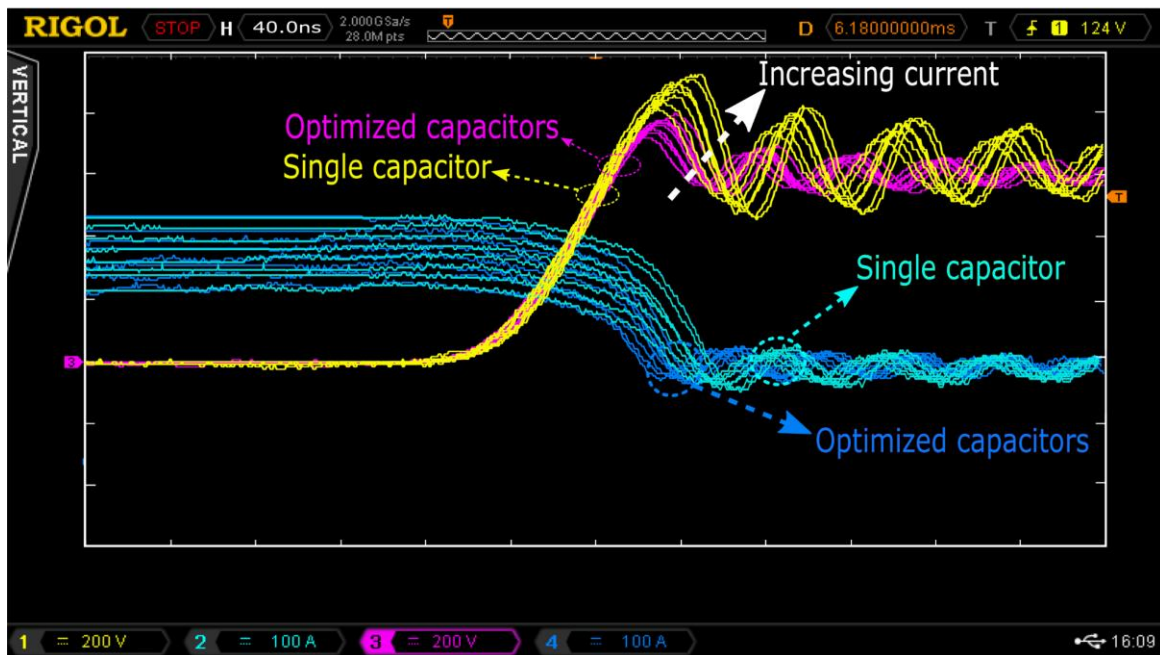


Figure 3. 25.

The turn off of the short loop with the optimized capacitors, and the single capacitor for different currents.

**Table XXXIII.**

The short loop calculated inductance by switching evaluation for different currents with a single capacitor.

Current [A]	$di/dt$ [A/ns]	Overshoot [V]	Calculated inductance [nH]
115	4.83	182	37.7
130	5.27	206	39.1
140	5.95	222	37.4
155	6.44	238	37
165	6.77	254	37.6
180	6.77	262	38.7
195	7.25	270	37.3
210	7.73	286	37

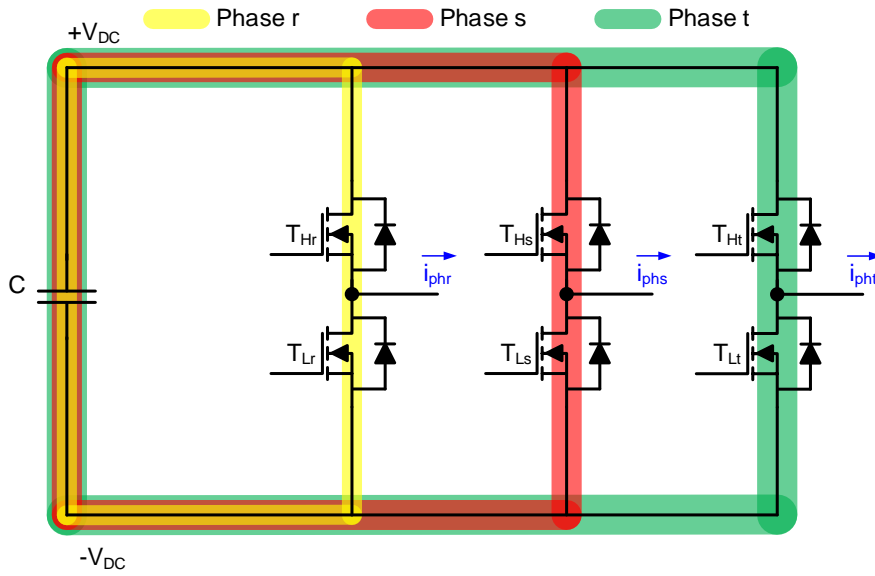
The calculated loop inductance is higher than with the optimized capacitors, shown in Table XXXI, and predicted by the impedance measurement. Also, the results are consistent for all the switched currents. In addition, the results match the measurements in Section 3.3.3.3 and shown in Table XXVII. The measurements by the impedance analyzer are done without the modules, so 18 nH should be added to those results. The final measured inductance with the modules is 37 nH, matching the calculations in the waveforms.

## 3.4. 2 level busbar design

Unlike 3L converters, the 2L topology only has one switching loop. The analysis and design of the busbar is straightforward, focusing only on two requirements. The first is to keep distances as short as possible. The second is to ensure returning currents can flow in the opposite path, applying the magnetic cancellation technique shown in Figure 3. 11. A single module is required to build a phase, so the 3 phases of the converter are built in the same busbar.

### 3.4.1. Switching loop evaluation

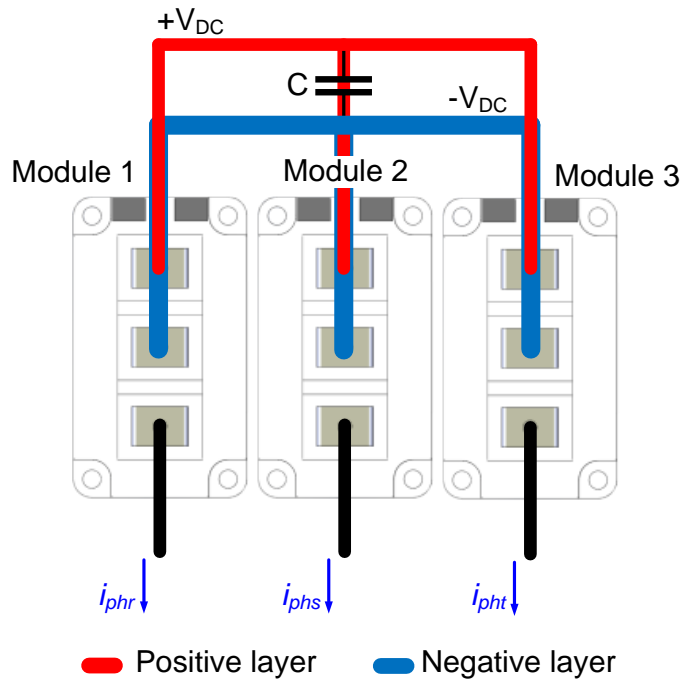
Each phase has its own switching loop, shown in Figure 3. 26. The switching loops individually cannot be optimized because there is only one possible configuration. This is because a single module is used per phase. The modulation is also the simplest. High and low switches in each phase are opposite, while each phase is 120° out of phase.



**Figure 3. 26.**  
2 level converters switching loops.

### 3.4.2. Module placement

There is only one possible module placement, shown in Figure 3. 27. Positive and negative layers connect the respective capacitor terminal to the module. The modules should be as close as possible, while still keeping the required gap for proper mechanical connection and insulation. In addition, both layers should be overlapped in order to allow opposite currents.

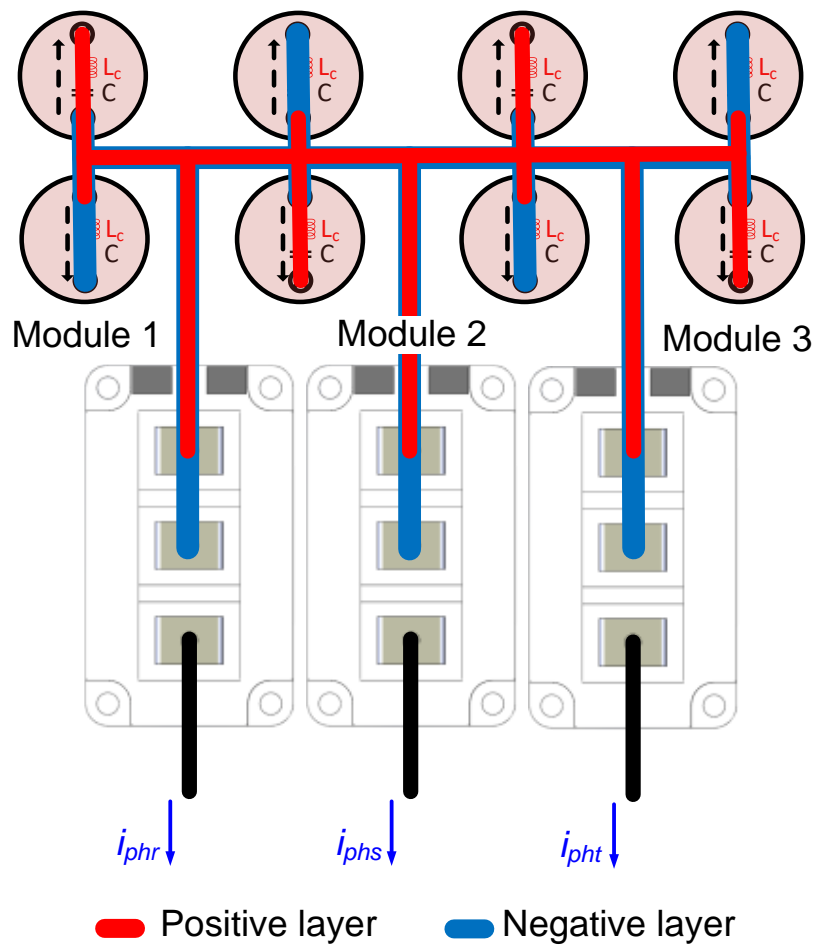


**Figure 3. 27.**  
2 level converter module placement.

### 3.4.3. Capacitor placement

The capacitor is connected to the three phases, and the current path to each one needs to be analyzed. The objective is to keep a symmetric current path for the three phases while the parasitic inductance in the path is minimized. To do so, the same technique as in the 3L converter is used. The capacitors are paralleled to divide the ESL, and opposite direction is given in order to achieve magnetic cancelation.

Figure 3. 28 shows the designed capacitor structure. Each capacitor is opposite to the two closest ones, forcing the opposite currents through all the structure. In addition, the distance between every module and two capacitor pairs is always identical. This last characteristic ensures symmetry between phases.



**Figure 3. 28.**  
Capacitor placement in the 2L converter.

### 3.4.4. Busbar assembly

The designed busbar is built and assembled in the laboratory. Figure 3. 29 shows the laboratory prototype. The negative layer and the modules are located underneath the positive layer and the capacitors.

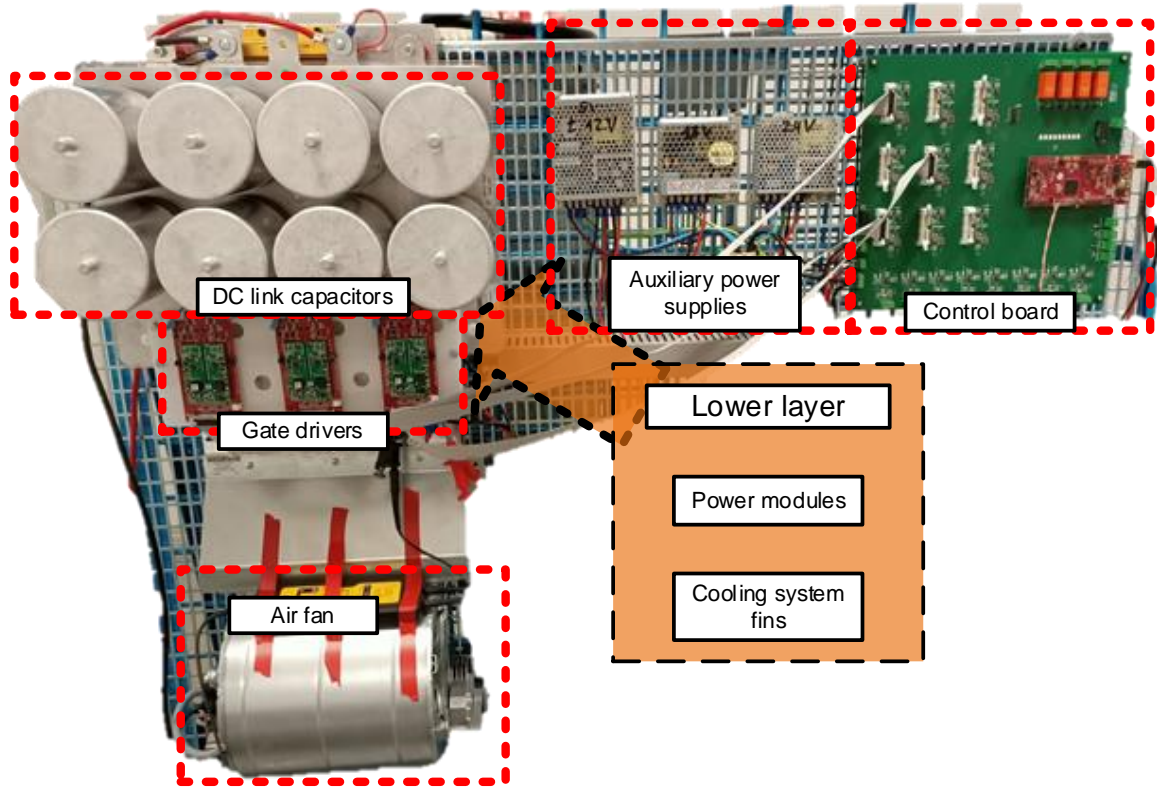


**Figure 3. 29.**

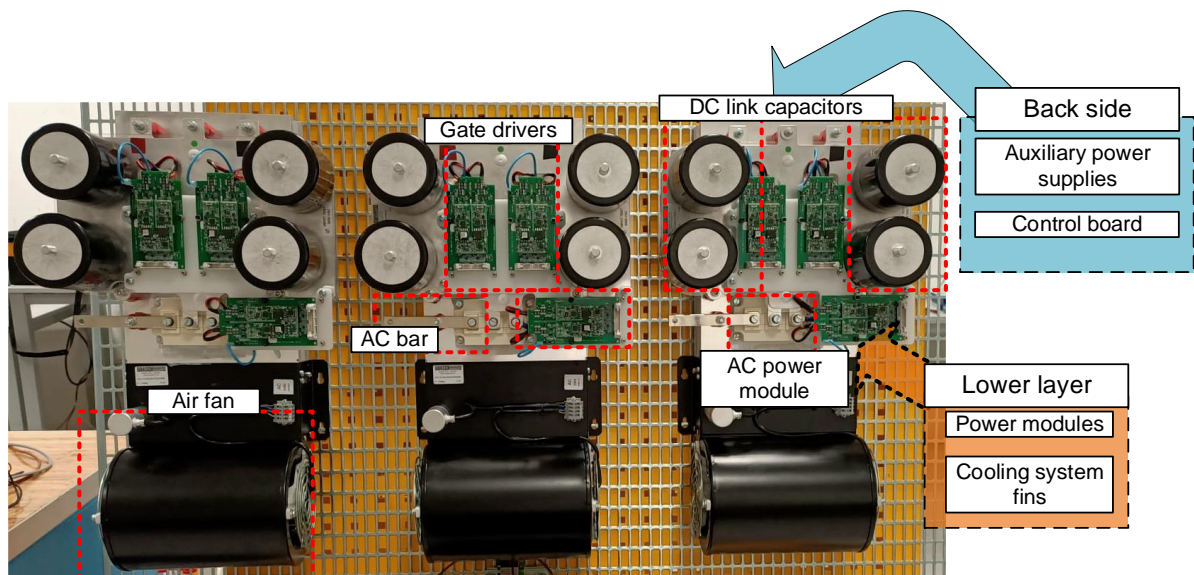
2L converter reception, (a) the busbar with the capacitors and (b) the 62 mm modules ready to assemble.

## 3.5. Hardware validation

The 2L and 3L prototypes have been implemented by fully assembling all the parts. Figure 3. 30 shows the final 2L converter prototype while the 3L prototype is shown in Figure 3. 31. The Yaskawa DC-link regulator is connected to the DC-link separately. The final step before performing any test is to validate the switching of both converters.



**Figure 3.30.**  
2L converter prototype.



**Figure 3.31.**  
3L converter prototype.

### 3.5.1. 3L converter switching validation

Both short and long switching loops are tested to validate the laboratory prototype. Figure 3.22 and Figure 3.23 show the measured drain to source voltage  $V_{ds}$  for a turn-off transient in short and long loops respectively. The test is performed with 600 V, the 100FIT value, in each half of the DC-link, which is a higher value than what the converter will handle in the continuous tests.

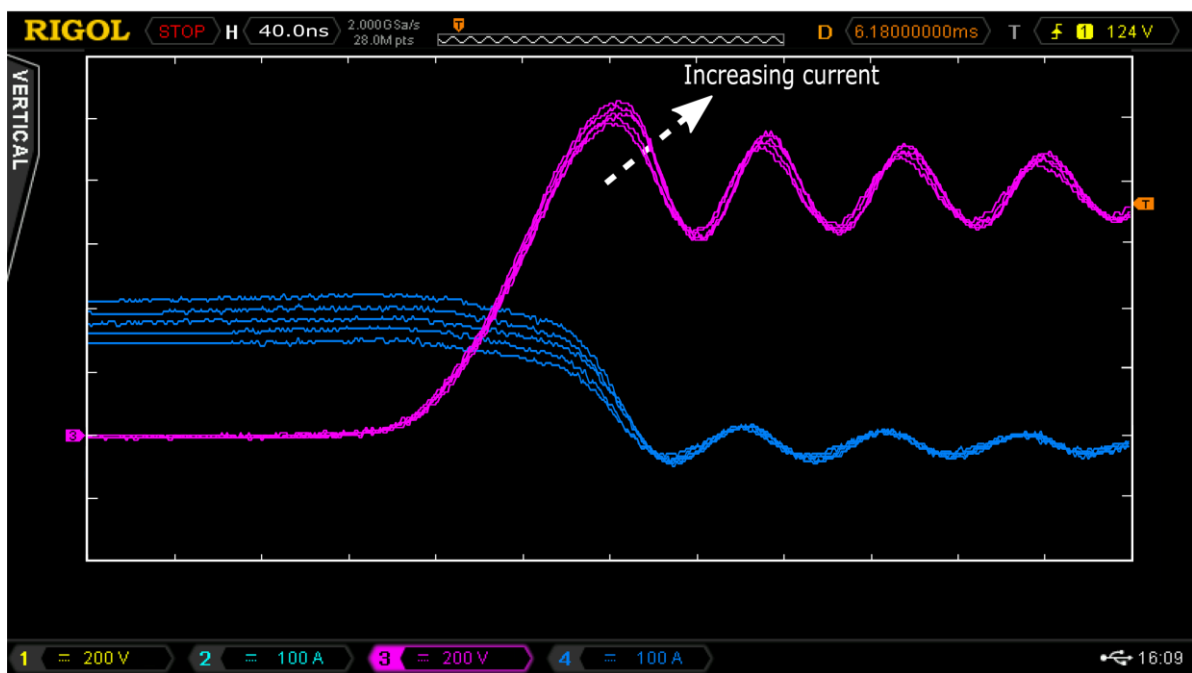
Following the classic definition in electronics, rising time of  $V_{ds}$  is measured from 0.1 to 0.9 of the DC value [127]. The achieved rise time in the short loop is 40 ns, being the fastest  $di/dt$  8.86 A/ns. The maximum measured  $V_{ds}$  voltage is 790 V while switching 225 A, proving safe switching operation in the short loop.

The rise time in the long loop is also 40 ns, being the fastest  $di/dt$  7.73 A/ns. The maximum measured  $V_{ds}$  voltage is 1102 V while switching the maximum current. It is concluded that the 1200 V modules are switched in fast but safe conditions, not suffering any overvoltage in the turn off in either switching loop, see Figure 3. 23 and Figure 3. 24.

### 3.5.2. 2L converter switching validation

Figure 3. 32 shows the measured drain to source voltage  $V_{ds}$  for a turn off transient in the 2L converter. The DC voltage is 750 V, being over the value that will be used in the continuous tests. The rising time of  $V_{ds}$  is measured from 0.1 to 0.9 of the DC value, as done in the 3L converter.

The measured rise time is 46 ns, being the fastest  $di/dt$  8.6 A/ns. The maximum measured  $V_{ds}$  voltage is 1054 V while switching 225 A. The calculated stray inductance of the switching loop is 35 nH. The correct switching of the 2L converter is validated.



**Figure 3. 32.**

Measured turn off transient  $V_{ds}$  waveform under 750 V DC voltage in the two level converter for different currents.

### 3.5.3. 3L continuous test

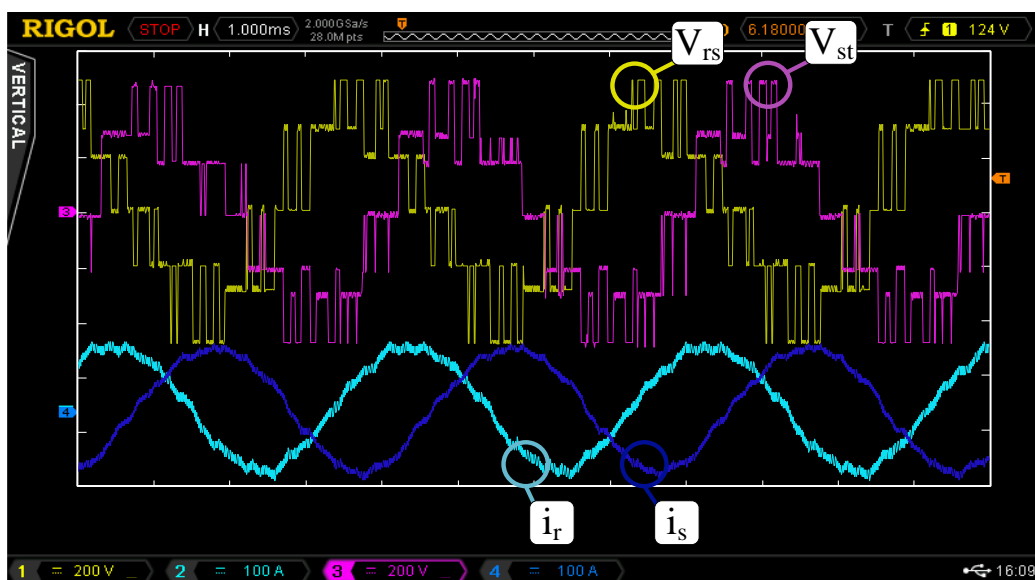
The 3L converter is tested at maximum power to ensure the correct functioning. The output waveforms are shown in Figure 3. 33. The testing conditions are shown in the next chapter in Table XXXIV. The first test is performed at 2.5 kHz switching frequency, Figure 3. 33(a), being the fundamental frequency  $f_0$  of the output sinewave 250 Hz. The switching frequency is only 10 times higher than the fundamental frequency, so the converter struggles to synthesize a proper output current sinewave.

In addition, voltage unbalances are observed in between the two DC link halves. During the design of the 3L converter, the neutral point balancing strategy presented in [36] is applied. However, as the switching frequency and the fundamental frequency are too close, the control strategy cannot operate effectively.

This issue is solved when increasing the switching frequency. Figure 3. 33(b) shows the output waveforms of the 3L converter at 10 kHz switching frequency. The output current sinewave is cleaner, and the voltage unbalances observed at 2.5 kHz are corrected with the neutral point balancing strategy.

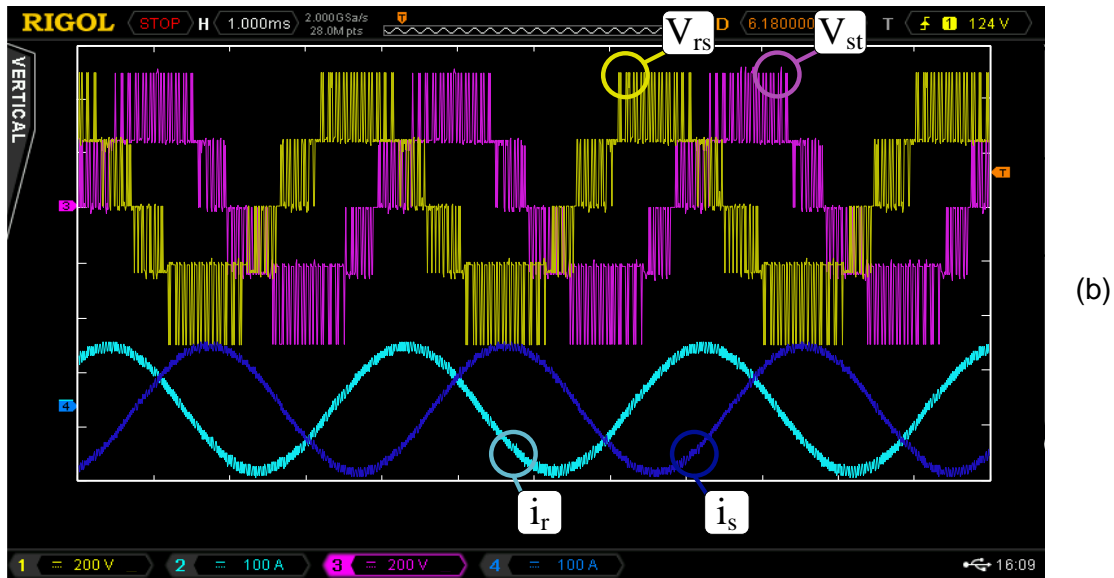
As a neutral point balancing strategy is necessary to ensure the correct operation of 3L converters, a switching frequency at least 30 times higher than the fundamental is recommended at high modulation indexes  $m_a$ , if the voltage unbalance is to be kept under 5 %. This is shown in Figure 3. 34, in which the measured voltage unbalance is presented per unit, depending on the switching frequency and fundamental frequency ratio at  $m_a = 0.9$ . This analysis shows that the aforementioned ratio must be used if an acceptable unbalance below 5 % is to be achieved. The unbalance is reduced as lower  $m_a$  values are used [36].

The performed tests validate the 3L converters correct operation, at maximum power and different switching frequencies, acknowledging the voltage balancing issue.

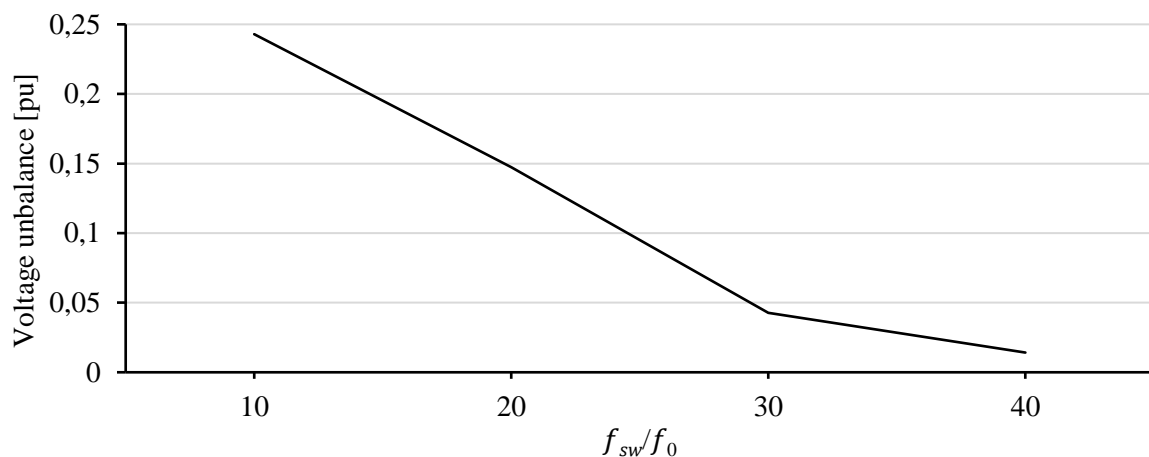


(a)





**Figure 3. 33.**  
3L converter continuous test at maximum power, a) at 2.5 kHz and b) at 10 kHz switching frequency.



**Figure 3. 34.**  
Measured voltage unbalance per unit, depending on the fundamental frequency and switching frequency ratio.

### 3.5.4. 2L continuous test

The 2L converter is tested at maximum power to ensure the correct functioning. The output waveforms are shown in Figure 3. 35. The testing conditions are shown in the next chapter in Table XXXIV. The first test is performed at 2.5 kHz switching frequency, Figure 3. 35 (a), being the fundamental frequency  $f_0$  of the output sinewave 250 Hz. Once again, at low switching frequency, the quality of the output current sinewave is low.

When increasing the switching frequency up to 10 kHz, Figure 3. 35 (b), the quality of the output current sinewave improves considerably. The 2L converter is validated at maximum operation power for different switching frequencies.

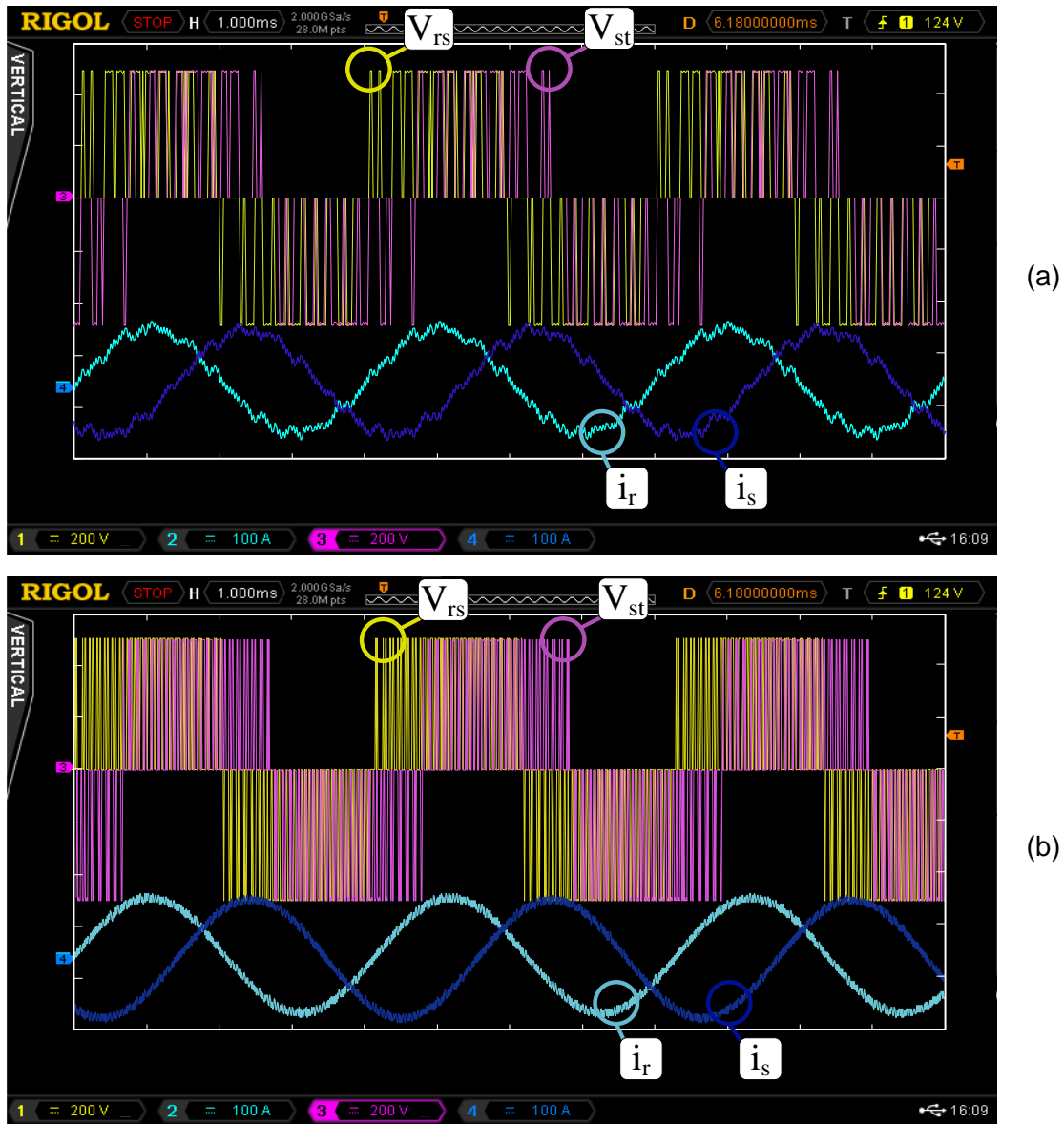


Figure 3.35. 2L converter continuous test at maximum power, a) at 2.5 kHz and b) at 10 kHz switching frequency.

### 3.6. Conclusion

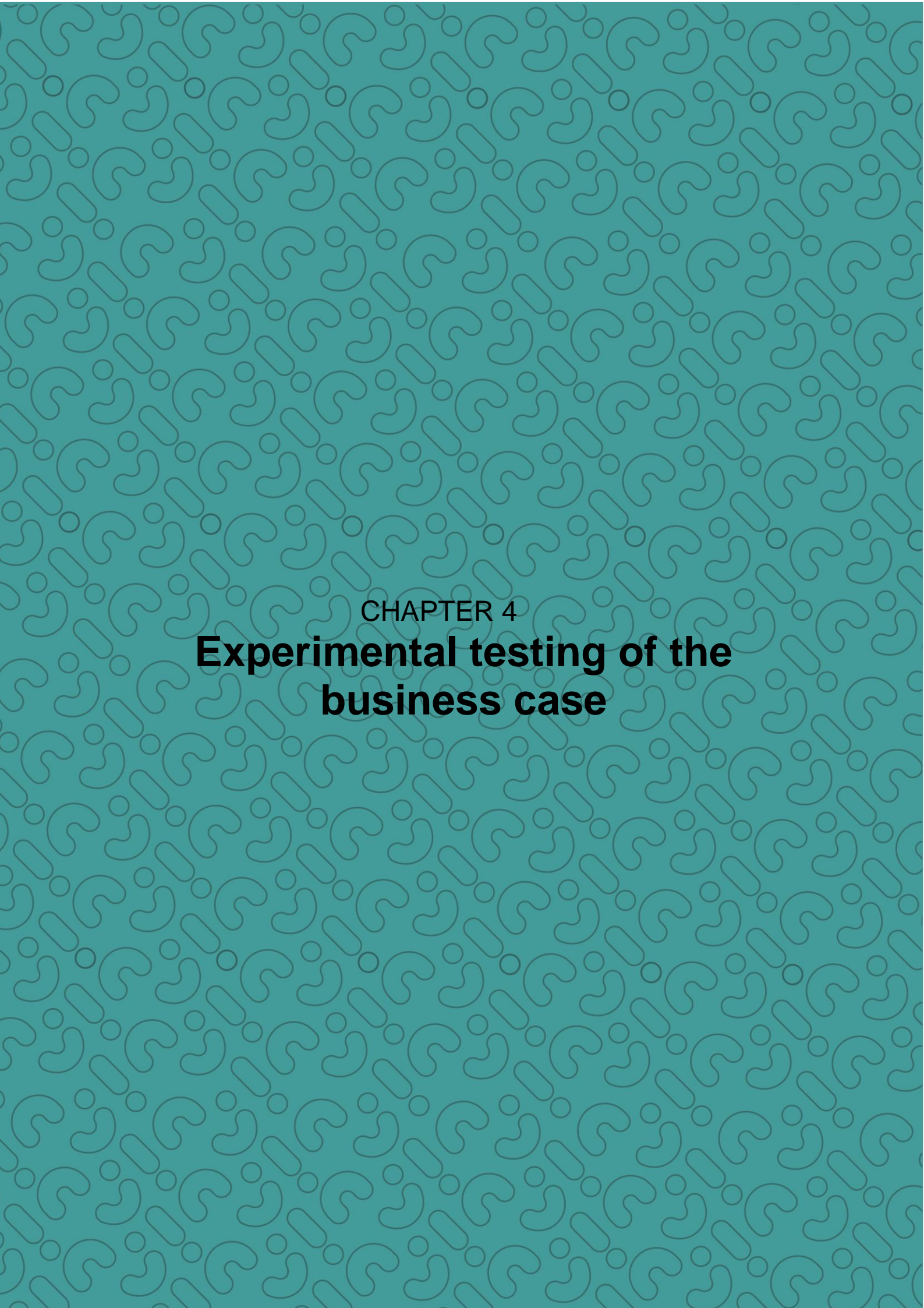
This chapter describes the design of two versatile test benches capable of testing 2L and 3L DC-AC converter configurations, which eases the comparison between different semiconductor technology (Si vs SiC) and voltage (1.2 kV, 1.7 kV, 2 kV) ratings. Careful component selection is presented, together with the power stage design.

For the 3L converter, an optimized busbar design is tested, adapting the successful design methodology in [115] to 62 mm package. Shifted module placement is proposed to ensure switching loop symmetry, parallel capacitors with opposite currents are used, as well as an optimized neutral layer, actively overlapping the ongoing current path. Each design decision is evaluated in detail using impedance analyzer measurements. The proposed design improves the symmetry over 90 % and reduces loop inductance 15 % when compared to existing 3L converters with 62 mm modules. The busbar is tested at 600 V, switching in 40 ns, while having a safe overshoot at 225 A. There is no need to slow down the gate or use snubbers.

For the 2L converter, the module placement is straightforward. However, the capacitor placement is optimized. The switching of the two level converter is also validated with a DPT. The design is tested at 750 V, switching in 46 ns, while having a safe overshoot at maximum current of 225 A. Again, no need to slow down the gate or add any safety measure is observed. High power converters will benefit with improved efficiency and increased power density due to the achieved switching characteristics in this work.

Continuous tests are carried out for both 3L and 2L converters at maximum power. Both converters are also tested at different switching frequency. A voltage unbalance issue is observed and explained at low switching frequency in the 3L converter. There is no remarkable issue in the 2L converter.

The test bench is ready to perform the efficiency tests. In addition, this test bench will allow to compare the selected business cases, fulfilling the proposed objective.



CHAPTER 4  
**Experimental testing of the  
business case**

## 4. Experimental testing of the business case

This chapter presents the tests made in the test bench designed in the previous chapter. The objective is to validate the models used in the LCoE calculation tool of Chapter 2. The business cases (BC) identified in Section 2.5.5 are tested and compared.

First, the baseline configuration, based on Si semiconductors and two level (2L) is analyzed. Then, the same topology is used but with SiC semiconductors. Next, the three level (3L) configuration with Si is introduced. Finally, the 3L topology is studied with SiC semiconductors.

For each configuration, the efficiency and the bill of material (BoM) is analyzed, as they are the two main factors for the LCoE calculation. A theoretical converter optimization is also performed if the configuration allows so, and the efficiency and BoM of the optimized configuration are analyzed again. Finally, the LCoE of each configuration is calculated. The chapter ends with the main conclusions obtained in the tests, comparing the different features provided by each configuration to those offered by the baseline. This chapter adds experimental support to the BC selection in Section 2.5.5.

### 4.1. Conditions of the analysis

This section explains the conditions in which the analysis has been performed. First, the operation points of the laboratory tests are listed. Next, the theoretical converter optimization method is presented. Finally, the mathematical expression as well as the method used to calculate the LCoE of each configuration are shown. In order to make a fair study, the testing points, the converter optimization, as well as the LCoE calculation method are the same for every configuration.

#### 4.1.1. Efficiency test conditions

The tests are performed keeping the same fixed DC link voltage and modulation index  $m_a$ . The active power is increased from 5 to 40 kW, reaching the limit of the testing facility. The load inductors are changed in every testing point, to ensure the power factor  $PF$  is kept between the desired margins. The fundamental frequency  $f_0$  of the synthesized sinewave is fixed in order to get the necessary impedance with the available load inductors. The switching frequency is varied from 2.5 to 10 kHz, to evaluate its effect in both topologies and technologies. Table XXXIV shows the testing conditions and operation points.

**Table XXXIV.**

Test operation points for all the studied configurations.

Parameter	Value	Unit
DC voltages	630	V
Modulation index	0.9	/
Power factor	0.75-0.85	/
Fundamental frequency	250	Hz
Switching frequency	2.5-10	kHz
Active power	5-40	kW

The converters are run in the operation conditions previously described. The obtained line voltage and phase currents are shown in Figure 3. 33 and Figure 3. 35 for the SiC modules at full power. Only two phases are measured because it is a balanced load system. The peak current value in this test is 110 A, corresponding to 40 kW.

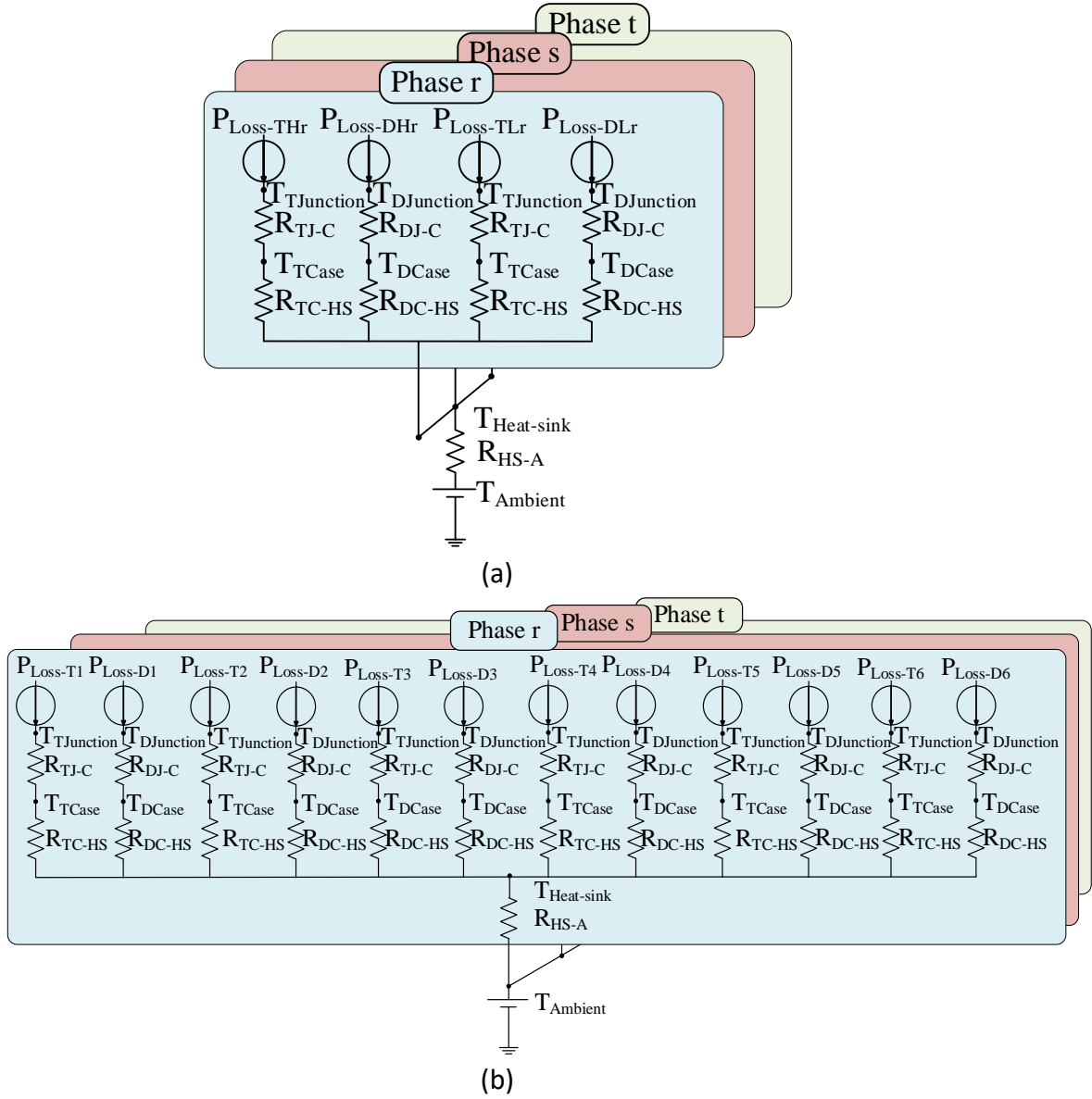
### 4.1.2. Theoretical converter optimization

The laboratory prototypes designed in Chapter 3 are not optimized but designed with sufficient safety margin in order to be able to perform the desired tests without risk. For example, the cooling system could be adjusted to 40 kW, which is the maximum power level tested in the lab. In addition, the output filters are not considered, but are of great importance if the whole system is studied. This section presents the converter optimization method used to adjust the aforementioned components to each converter. The goal is to obtain a more accurate cost for each configuration, in order to perform a fair LCoE analysis later on.

#### 4.1.2.1. Cooling system calculation

The cooling system is calculated separately for the 2L and 3L converters. However, the methodology is the same. Figure 4. 1 shows the thermal models used for both converters. The three phases of the 2L converter are mounted in the same heat sink system, but the 3L converter uses one heat sink per phase in order to optimize the module layout, as explained in Section 3.2.4. Each module is composed of two couples of semiconductors, and each couple is formed by an active switch  $T$  and a diode  $D$  in antiparallel.  $R_{J-C}$  and  $R_{C-HS}$  represent the thermal resistance from the junction to the case of each semiconductor and from the case to the heat sink respectively. These parameters are found in the datasheets of the modules.

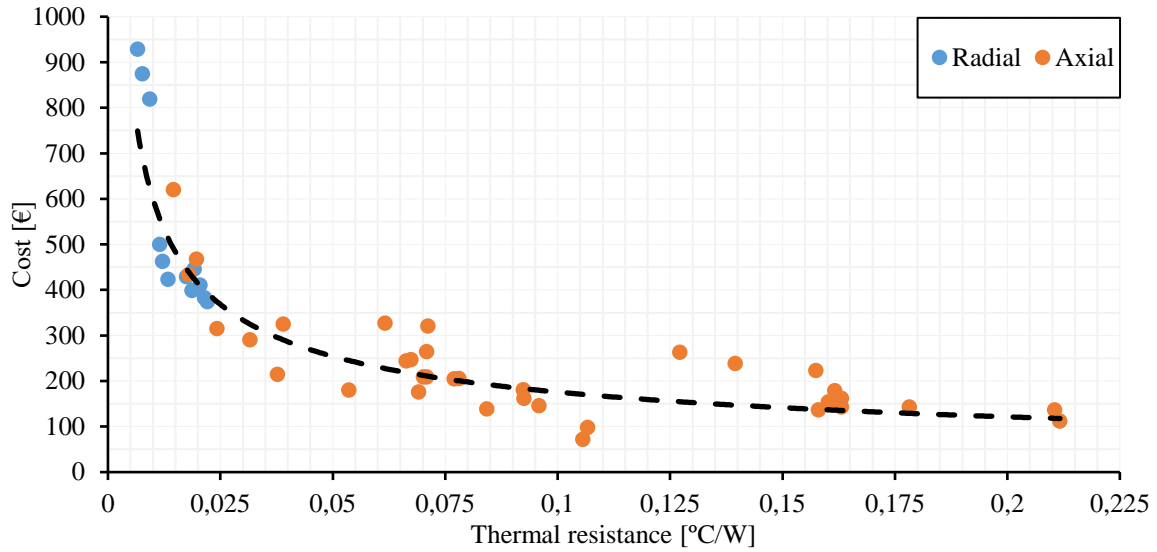
The power losses considered for the sizing are the maximum registered for each configuration in the tests. It is not possible to distinguish the distribution of the losses between the diode and the transistor within a module, so the worst case scenario is analysed. This corresponds to the case in which all the losses are generated in the path with the highest thermal resistance. The maximum allowable thermal resistance of the cooling system  $R_{HS}$  is calculated for each case.



**Figure 4. 1.** Cooling system models, (a) for the 2L converter and (b) for the 3L converter.

Next, a cost is assigned to each required cooling system. This is done by using as a reference several commercial cooling systems available in the market. Figure 4. 2 shows the cost of the analysed commercial cooling systems depending on their thermal resistance. A potential curve that approximates the trend is obtained (64), and used to assign a cost to the required cooling system for each configuration.

$$Cost_{CS} = 51.412 \cdot R_{th}^{-0.534} \tag{64}$$



**Figure 4. 2.**  
Cost of commercial cooling systems depending on their thermal resistance.

#### 4.1.2.2. Output filter calculation

A similar method is used to calculate the output filter and its cost. The selected filter topology is the LC line filter, and each phase is calculated individually. First, the inductance and capacitance values in the filter are calculated using expressions (65) and (66) presented in [128] and [129] respectively.  $V_{DC}$  is 630 V,  $\Delta I_{out}$  is defined as 10 % of the  $I_{out}$  and  $Att_{req}$ , which refers to the required attenuation of the filter, is set to 0.01 in order to have enough damping in the switching frequency [130].  $m$  refers to the converter topology level, 2 or 3 in this case.

$$L_f = \frac{V_{DC}}{6(m-1) \cdot \Delta I_{out} \cdot f_{sw}} \quad (65)$$

$$C_f = \frac{1}{(2\pi \cdot f_{sw})^2 \cdot L_f \cdot Att_{req}} \quad (66)$$

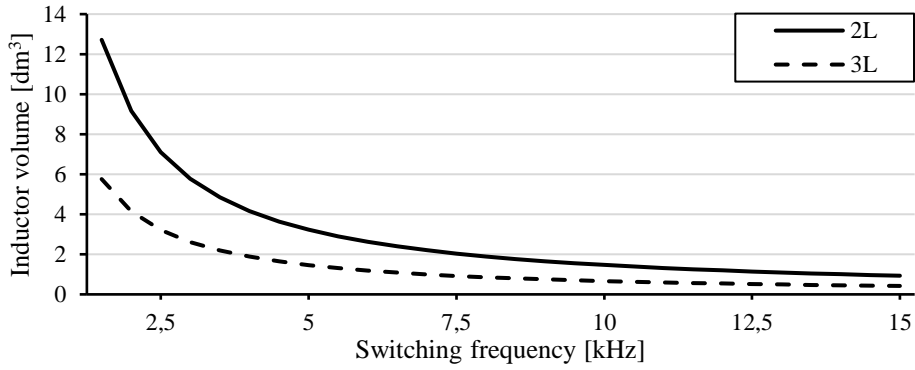
There is not a clear relation between the inductance and the cost of an inductor. However, the trend is clear if the volume of the inductor is calculated. The volume of an inductor not only depends on the inductance, but also considers several parameters of the application, such as the peak current, the maximum magnetic flux, the loss distribution or geometrical constraints. To calculate the volume of the inductor, the area product  $A_p$  technique proposed in [131] is used. (67) uses the factor  $k_L$  to relate the area product and inductor volume. This factor is dependent on the switching frequency, so a polynomial approximation is performed to calculate  $k_L$  in [132], and shown in (68).

$$Vol_{L_f} = k_L \cdot A_p^{\frac{3}{4}} \quad (67)$$

$$k_L = 2.676 \times 10^{-5} \cdot f_{sw} + 19.71 \quad (68)$$

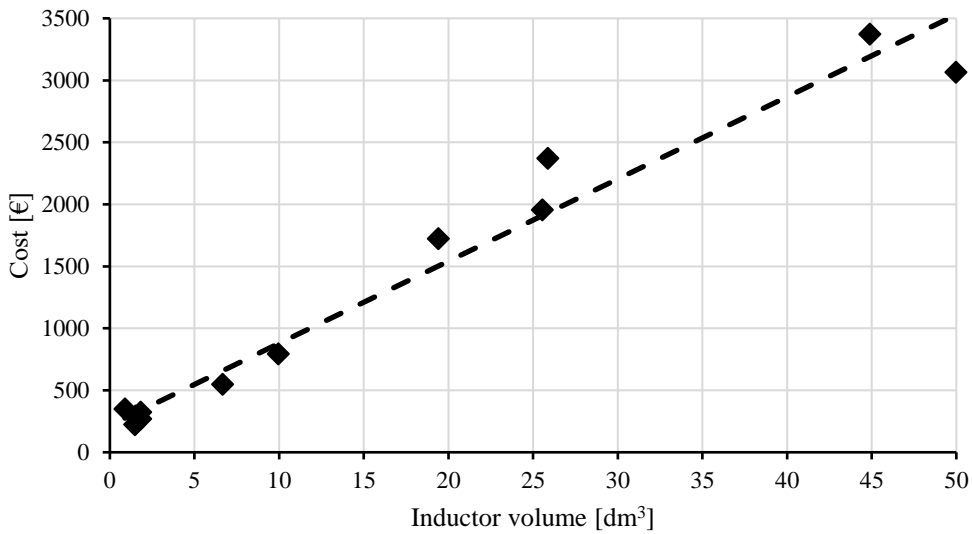


The required volume for the three inductors is shown in Figure 4. 3. As it is observed, the required volume is exponentially reduced with increased switching frequency. In addition, using a three level converter will further reduce the volume of the inductor. The peak output current measured in the laboratory is used for the calculations in (67), shown in Figure 3. 33 and Figure 3. 35.



**Figure 4. 3.** Required volume of the three inductors, depending on the switching frequency and converter level.

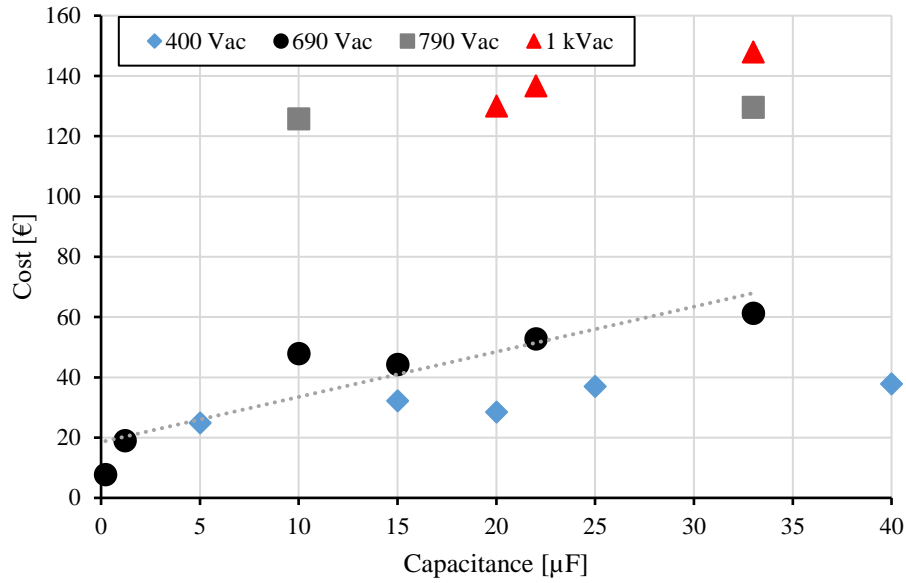
The volume of an inductor is directly related to its cost, as shown in Figure 4. 4. Commercial inductors are plotted depending on their volume and their cost. A linear relation is observed, and expressed in (69).



**Figure 4. 4.** Cost of single commercial inductors depending on their volume.

$$Cost_L = 66.268 \cdot Vol_L + 216.18 \tag{69}$$

Regarding the capacitors, the cost is directly related to the capacitance for each voltage rating. This is again observed after analysing commercial capacitors and plotting them in Figure 4. 5. The selected voltage rating for the converter optimization is the 690 V<sub>AC</sub> product group. The linear relation between the capacitance and the cost for the 690 V<sub>AC</sub> capacitors is (70). The capacitance value should be introduced in μF.

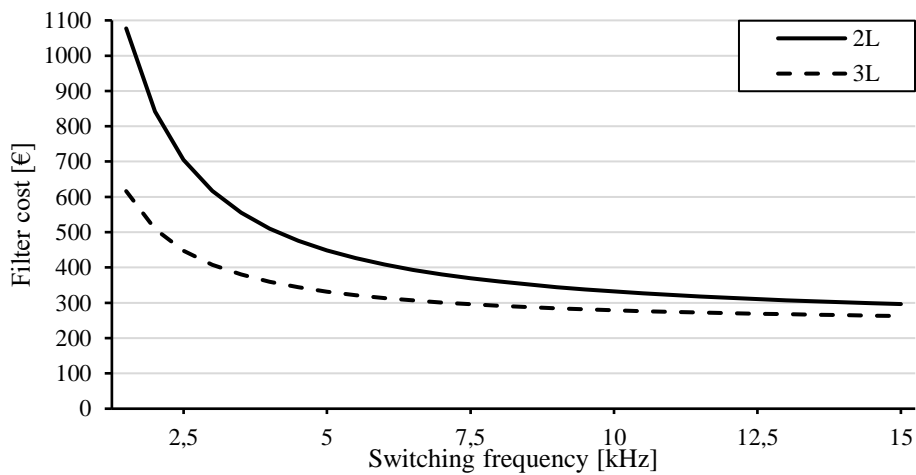


**Figure 4. 5.**  
Cost of single commercial capacitors depending on the capacitance.

$$Cost_C = 1.497 \cdot C[\mu F] + 18.522 \quad (70)$$

The cost of the whole output filter is calculated by adding the cost of all the components (71). Figure 4. 6 shows the total cost of the output filter for different topologies as well as switching frequencies. It is seen that increasing the switching frequency is a good strategy to reduce the cost. In addition, having more voltage levels also leads to a cost reduction.

$$Cost_{Filter} = 3 \cdot Cost_L + 3 \cdot Cost_C \quad (71)$$



**Figure 4. 6.**  
Cost of the output filter depending on the switching frequency and converter topology.

### 4.1.3. LCoCE calculation method

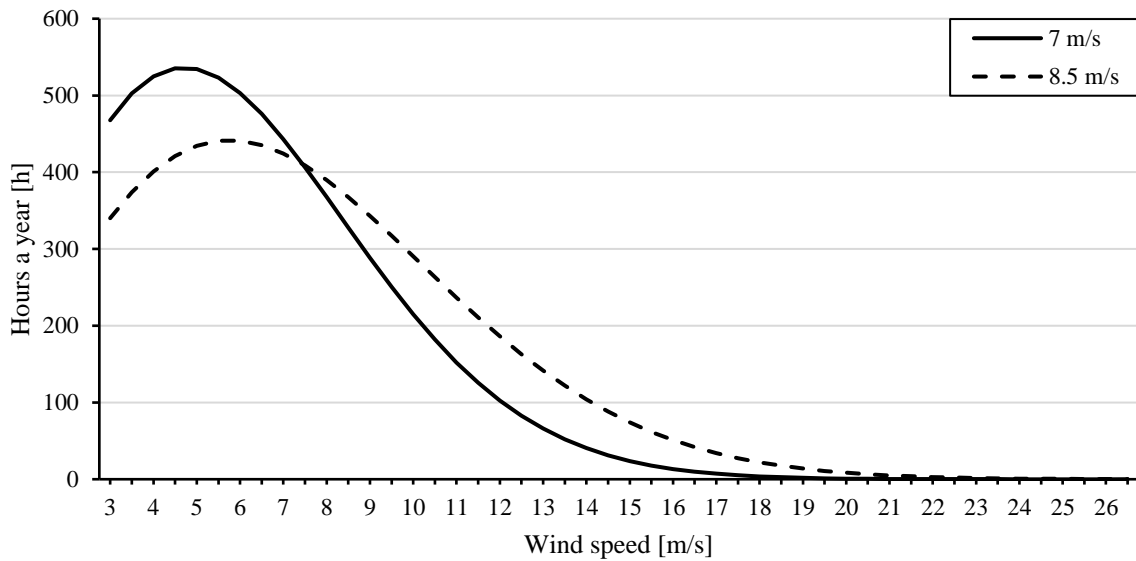
The final goal is to calculate the LCoE of the tested configurations. The calculation of LCoE previously introduced in (1) in Chapter 2 is complex and requires a lot of data provided by industry, as considers certain *Capex* and *Opex* out of reach of this analysis. Due to the complexity of (1), and lack of information in the experimental platform, this expression cannot be used in this case. Instead of that, a simplified version of the LCoE is used, not considering several parameters such as *Opex*, the civil engineering cost, as well as the cost of the mechanical parts. This new parameter has been named in this work as levelized cost of conversion energy (LCoCE) and considers only the cost of the power electronics conversion system. The new parameter gives information about how much it costs to process a certain energy unit in a specific power electronic configuration. The LCoCE of each configuration is calculated with (72), and considers only the available data of the designed laboratory prototypes.

$$LCoCE = \frac{\text{Total cost of the system}}{\text{Weighted AEP}} \quad (72)$$

The *Total cost of the system* is calculated by adding the cost of all the known components in the configuration (73).

$$\begin{aligned} \text{Total cost of the system} &= Cost_{Semiconductors} + Cost_{Drivers} + Cost_{Busbar} \\ &+ Cost_{CS} + Cost_{Dccaps} + Cost_{Control\ board} + Cost_{Sensors} \\ &+ Cost_{Circuit\ breakers} + Cost_{Output\ filter} \\ &+ Cost_{Connections\ and\ envelope} \end{aligned} \quad (73)$$

The *Weighted AEP* is calculated with two wind distributions, as in (49). However, the *AEP* is calculated considering the losses measured in the laboratory tests for each configuration. First, a Weibull probability distribution with the form factor  $k = 2$  is used to calculate the annual hours at each wind speed for two different locations, one with an annual average wind speed of 7 m/s, and the other with an annual average wind speed of 8.5 m/s, Figure 4. 7.



**Figure 4. 7.**

Weibull wind speed distributions used for AEP calculations.

Then, the power curves of the 5 MW turbine of the industrial partner are scaled down to 40 kW, in order to have the same power rating as the laboratory prototypes. The scaled power curves provide information about the power delivered by the wind turbine at each wind speed, but are not shown in this document due to the confidential status of the information. Knowing the power at each wind speed, the losses measured in the laboratory are subtracted at each power point for every configuration. With the information in Figure 4. 7 about the hours in each wind speed, the weighted AEP is calculated for each configuration using (49). Every parameter in (72) is now available to calculate the LCoCE.

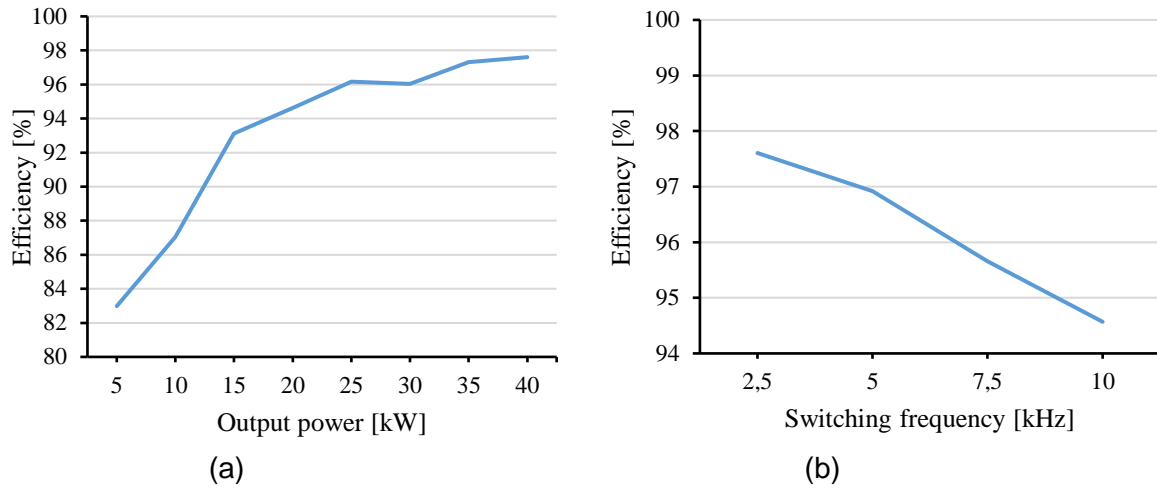
First, the LCoCE of the baseline configuration is calculated. Next, the LCoCE calculated for the other configurations is compared to it, analyzing the variation in percentage.

## 4.2. 2 level with Si, baseline configuration

This section shows the configuration that is going to be considered as baseline. It consists of the 2L topology with Si IGBTs. It is the closest configuration to the real baseline, only scaling the power levels. This configuration is used as a reference to compare LCoCE results of the other configurations.

### 4.2.1. Efficiency tests

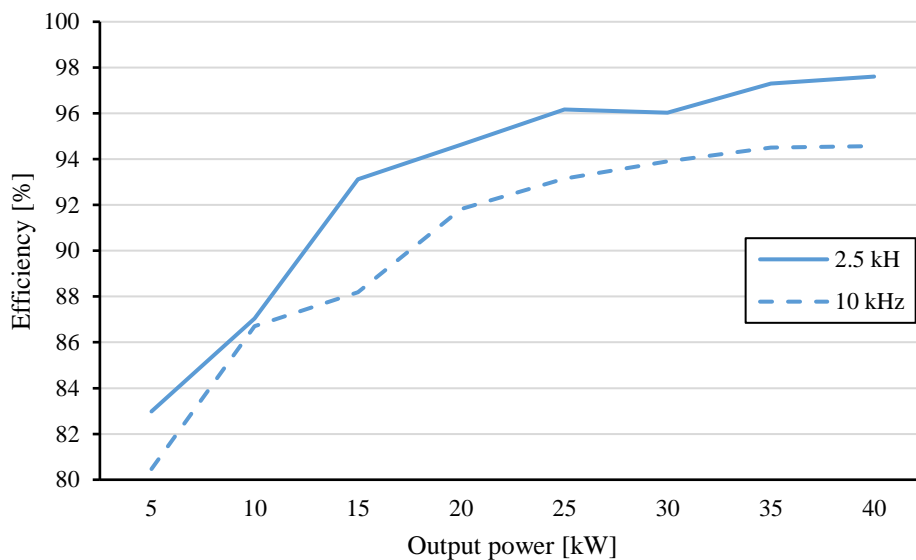
First, the baseline configuration is tested at 2.5 kHz switching frequency and different output powers, Figure 4. 8(a). Then, the switching frequency is increased at maximum output power, and its effect on the efficiency is analyzed in Figure 4. 8(b). It is observed how the poor switching behavior of the Si IGBTs penalize the efficiency of this configuration mostly at low power, where these losses are dominant. In addition, it can be seen that increasing the switching frequency comes with a high efficiency penalty, confirming the poor switching behavior of the Si IGBTs. All the efficiency tests are performed according to the conditions described in Section 4.1.1 and in Table XXXIV.



**Figure 4. 8.**

Efficiency tests of the baseline (2L Si) configuration, (a) for different output powers at 2.5 kHz switching frequency and (b) for different switching frequencies at maximum output power.

The baseline configuration is also tested at different output powers and high switching frequency, 10 kHz, Figure 4. 9. The poor switching characteristics of Si IGBTs are once again confirmed as the high frequency configuration does not reach 95 % efficiency in any operation point. This results show the limited options of increasing the switching frequency with Si IGBTs in a 2L topology.



**Figure 4. 9.**

Efficiency tests of the baseline configuration for different output powers and switching frequencies.

## 4.2.2. Converter optimization

In this section, the cooling system and the output filter of the baseline are optimized according to the methodologies presented in Section 4.1.2. In addition, increasing the switching frequency is also analyzed. Regarding the cooling system, the thermal model in Figure 4. 1(a) is applied to each configuration for the maximum losses registered in the tests shown in Figure 4. 9. Next, the cost of the cooling system is calculated using (64). The filter is calculated for each configuration depending on the topology level, 2 in this case, and the switching frequency, 2.5 and 10 kHz. Figure 4. 6 shows the cost of the output filter in each case. Table XXXV summarizes the obtained results.

**Table XXXV.**

Baseline configuration converter optimization summary.

Configuration	Baseline 2.5 kHz		Baseline 10 kHz	
	Value	Unit	Value	Unit
Maximum $P_{loss}$	1295	W	1922	W
Maximum $R_{th}$	0.0509	°C/W	0.0245	°C/W
Cooling system cost	252.22	€	372.93	€
Filter cost	705.33	€	332.19	€

## 4.2.3. System cost

Table XXXVI shows the cost breakdown of the baseline at 2.5 kHz and 10 kHz switching frequency. The major difference is brought by the cost of the output filter. While increasing the switching frequency increases the cost of the cooling system due to the higher losses, the output filter can be reduced. The total cost of the system is reduced by increasing the switching frequency, because the output filters represent a higher percentage of the total cost than the cooling system.

**Table XXXVI.**

Baseline configuration cost breakdown at 2.5 kHz and 10 kHz switching frequency.

Component	Baseline 2.5 kHz			Baseline 10 kHz		
	Qty	Cost [€]	[%]	Qty	Cost [€]	[%]
<b>Semiconductors</b>	3	387.12	4.65	3	387.12	4.80
<b>Drivers</b>	3	691.74	8.32	3	691.74	8.59
<b>Busbar</b>	1	1410	16.96	1	1410	17.50
<b>Cooling system</b>	1	252.22	3.03	1	372.93	4.63
<b>DC link capacitors</b>	8	947.36	11.40	8	947.36	11.76
<b>Control board</b>	1	599.51	7.21	1	599.51	7.44
<b>Sensors</b>	7	881.32	10.60	7	881.32	10.94
<b>Circuit breakers and security</b>	3	1405.18	16.91	3	1405.18	17.44
<b>Output filter</b>	1	705.33	8.48	1	332.19	4.12
<b>Cables, connectors and mechanical envelope</b>	/	1029.48	12.38	/	1029.48	12.78
<b>Total</b>	8309.26		100	8056.83		100
<b>Difference [€]</b>				<b>-252.43</b>		

#### 4.2.4. LCoCE

The LCoCE of the baseline configuration is calculated using the methodology presented in Section 4.1.3. Table XXXVII summarizes the results. The reduction of the LCoCE by the increment of the switching frequency is negligible, as the difference is below the 0.0015 %.

**Table XXXVII.**

LCoCE of the baseline configuration.

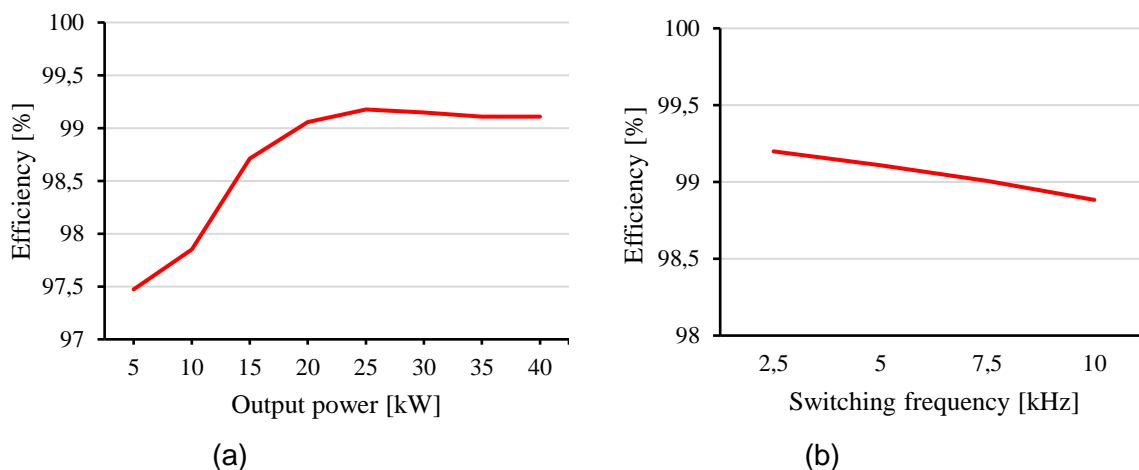
Configuration	Baseline 2.5 kHz		Baseline 10 kHz	
	Value	Unit	Value	Unit
<b>Weighted AEP</b>	115.57	MWh	112.06	MWh
<b>Total cost</b>	8309.26	€	8056.83	€
<b>LCoCE</b>	71.898	€/MWh	71.897	€/MWh
<b>Difference</b>			<b>-0.0013</b>	%

### 4.3. 2 level with SiC

This section analyzes the 2L topology with SiC MOSFETs. The procedure is the same as for the baseline. First, the efficiency tests performed in the lab are shown. Next, the converter optimization is performed, and the system cost calculated. Finally, the LCoCE is analyzed.

#### 4.3.1. Efficiency tests

First, the 2L configuration with SiC is analyzed for different output powers at 2.5 kHz switching frequency in Figure 4. 10(a). Next, the switching frequency is increased up to 10 kHz at maximum output power in Figure 4. 10(b). The results show an efficiency higher than 99 % for the maximum power points. In addition, Figure 4. 10(b) shows the excellent switching performance of SiC, being able to operate at 10 kHz at over 98.8 % efficiency at maximum power. All the efficiency tests are performed according to the conditions described in Section 4.1.1 and in Table XXXIV.

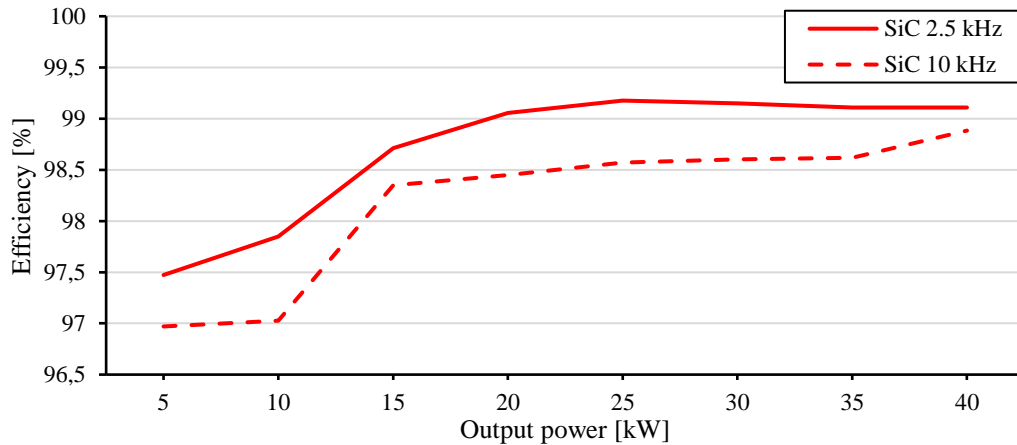


**Figure 4. 10.**

Efficiency tests of the 2L with SiC configuration, (a) for different output powers at 2.5 kHz switching frequency and (b) for different switching frequencies at maximum output power.

The 2L configuration with SiC is also tested at 10 kHz switching frequency for all the output powers, Figure 4. 11. The good switching performance of SiC allows to operate at 10 kHz with efficiencies over the 98 % in most of the operation points.





**Figure 4. 11**

Efficiency tests of the 2L configuration with SiC for different output powers and switching frequencies.

### 4.3.2. Converter optimization

In this section, the cooling system and the output filter of the 2L configuration with SiC are optimized according to the methodologies presented in Section 4.1.2. In addition, increasing the switching frequency is also analyzed. Regarding the cooling system, the thermal model in Figure 4. 1(a) is applied to each configuration for the maximum losses registered in the tests shown in Figure 4. 11. Next, the cost of the cooling system is calculated using (64). The filter is calculated for each configuration depending on the topology level, 2 in this case, and the switching frequency, 2.5 and 10 kHz. Figure 4. 6 shows the cost of the output filter in each case. Table XXXVIII summarizes the obtained results.

**Table XXXVIII.**

2L configuration with SiC converter optimization summary.

Configuration	2L with SiC 2.5 kHz		2L with SiC 10 kHz	
	Value	Unit	Value	Unit
Maximum $P_{loss}$	320	W	483	W
Maximum $R_{th}$	0.293	°C/W	0.18	°C/W
Cooling system cost	99	€	127.55	€
Filter cost	705.33	€	332.19	€

### 4.3.3. System cost

Table XXXIX shows the cost breakdown of the 2L configuration with SiC at 2.5 kHz and 10 kHz switching frequency. The major difference is brought by the cost of the output filter. While increasing the switching frequency increases the cost of the cooling system due to the higher losses, the output filter can be reduced. The total cost of the system is reduced by increasing the switching frequency, because the output filters represent a higher percentage of the total cost than the cooling system. The SiC semiconductors represent the highest cost in these configurations.

**Table XXXIX.**

2L configurations with SiC cost breakdown, at 2.5 kHz and 10 kHz switching frequencies.

Component	2L with SiC 2.5 kHz			2L with SiC 10 kHz		
	Qty	Cost [€]	[%]	Qty	Cost [€]	[%]
<b>Semiconductors</b>	3	1800	18.81	3	1800	19.51
<b>Drivers</b>	3	691.74	7.23	3	691.74	7.50
<b>Busbar</b>	1	1410	14.74	1	1410	15.29
<b>Cooling system</b>	1	99	1.03	1	127.55	1.38
<b>DC link capacitors</b>	8	947.36	9.90	8	947.36	10.27
<b>Control board</b>	1	599.51	6.27	1	599.51	6.50
<b>Sensors</b>	7	881.32	9.21	7	881.32	9.55
<b>Circuit breakers and security</b>	3	1405.18	14.68	3	1405.18	15.23
<b>Output filter</b>	1	705.33	7.37	1	332.19	3.60
<b>Cables, connectors and mechanical envelope</b>	/	1029.48	10.76	/	1029.48	11.16
<b>Total</b>		9568.92	100		9224.33	100
<b>Difference [€]</b>					-344.59	

#### 4.3.4. LCoCE

The LCoCE of the 2L configuration with SiC is calculated using the methodology presented in Section 4.1.3. Table XL summarizes the results. The 2L configuration with SiC takes advantage of the good switching characteristics of SiC, not reducing the AEP significantly with increased switching frequency when compared to the same configuration at 2.5 kHz. With the cost reduction shown in Table XXXIX, it is concluded that increasing the switching frequency is positive in the case of the 2L configuration with SiC, in terms of the LCoCE.

**Table XL.**

LCoCE of the 2L configuration with SiC.

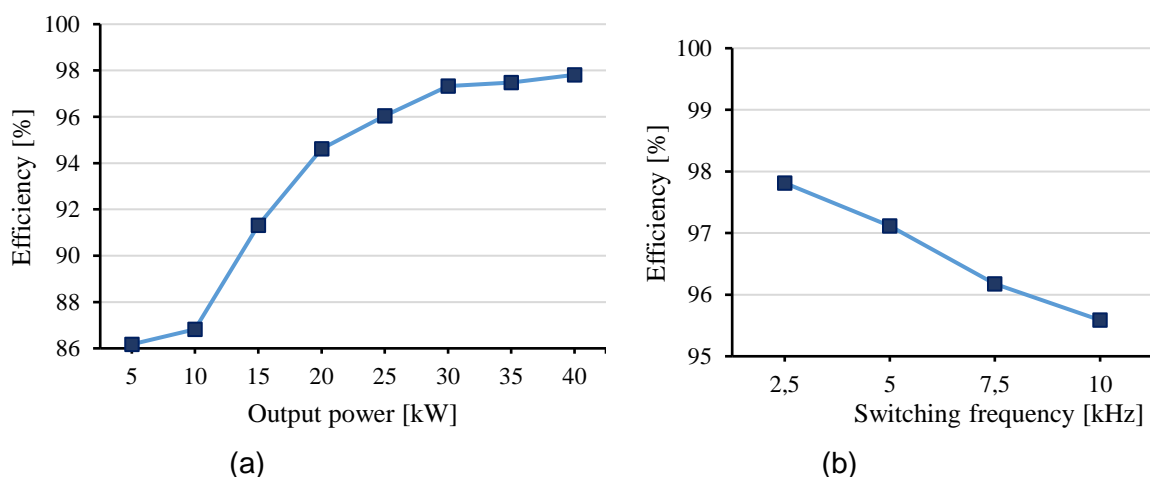
Configuration	2L with SiC 2.5 kHz		2L with SiC 10 kHz	
Parameter	Value	Unit	Value	Unit
Weighted AEP	119.90	MWh	119.36	MWh
Total cost	9568.92	€	9224.33	€
LCoCE	79.807	€/MWh	77.281	€/MWh
Difference			-3.165%	%

## 4.4. 3 level with Si

This section analyzes the 3L topology with Si IGBTs. The procedure is the same as for the baseline. First, the efficiency tests performed in the lab are shown. Next, the converter optimization is performed, and the system cost calculated. Finally, the LCoCE is analyzed.

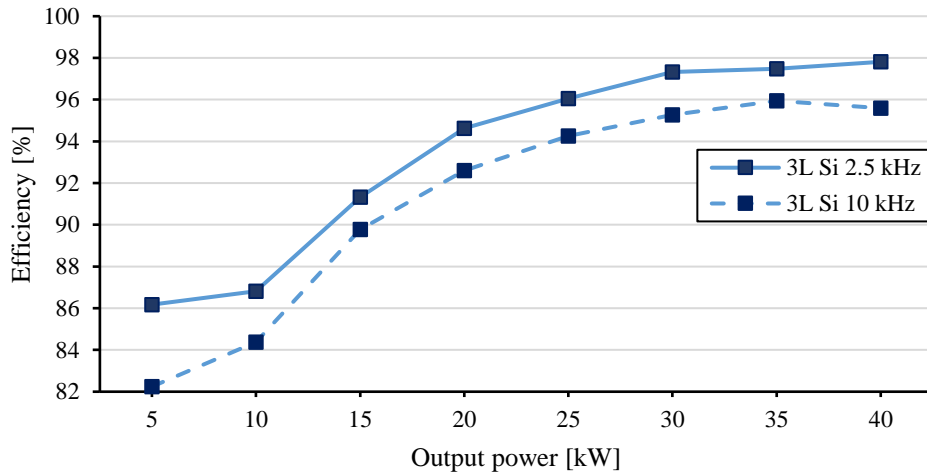
### 4.4.1. Efficiency tests

First, the 3L configuration with Si is analyzed for different output powers at 2.5 kHz switching frequency in Figure 4. 12(a). Next, the switching frequency is increased up to 10 kHz at maximum output power in Figure 4. 12 (b). The results show an improvement on the switching behavior with respect to the 2L configuration with Si. The 3L configuration with Si can work at 10 kHz switching frequency and achieve an efficiency over 95.5 % at maximum power. All the efficiency tests are performed according to the conditions described in Section 4.1.1 and in Table XXXIV.

**Figure 4. 12.**

Efficiency tests of the 3L with Si configuration, (a) for different output powers at 2.5 kHz switching frequency and (b) for different switching frequencies at maximum output power.

The 3L configuration with Si is also tested at 10 kHz switching frequency for all the output powers, Figure 4. 13. The better switching performance of the 3L topology achieves nearly 96 % efficiency even at high switching frequency.



**Figure 4.13**

Efficiency tests of the 3L configuration with Si for different output powers and switching frequencies.

#### 4.4.2. Converter optimization

In this section, the cooling system and the output filter of the 3L configuration with Si are optimized according to the methodologies presented in Section 4.1.2. In addition, increasing the switching frequency is also analyzed. Regarding the cooling system, the thermal model in Figure 4.1(b) is applied to each configuration for the maximum losses registered in the tests shown in Figure 4.13. Next, the cost of the cooling system is calculated using (64). In the case of the 3L configurations, the cooling system is calculated per phase. The filter is calculated for each configuration depending on the topology level, 3 in this case, and the switching frequency, 2.5 kHz and 10 kHz. Figure 4.6 shows the cost of the output filter in each case. Table XLI. summarizes the obtained results.

**Table XLI.**

3L configuration with Si converter optimization summary.

Configuration	3L with Si 2.5 kHz		3L with Si 10 kHz	
	Value	Unit	Value	Unit
Maximum $P_{loss}$	1317	W	1765	W
Maximum $R_{th}$ per phase	0.1975	°C/W	0.1368	°C/W
Cooling system cost (per phase)	122.24	€	148.72	€
Filter cost	447.83	€	278.85	€

### 4.4.3. System cost

Table XLII shows the cost breakdown of the 3L configuration with Si at 2.5 kHz and 10 kHz switching frequency. The major difference is brought by the cost of the output filter. While increasing the switching frequency increases the cost of the cooling system due to the higher losses, the output filter can be reduced. The total cost of the system is slightly reduced by increasing the switching frequency, because the output filter represents a higher percentage of the total cost than the cooling system. The busbar becomes the highest cost of this configuration due to its complexity and the three separated pieces. The drivers also represent a big part of the cost due to the high number of the components.

**Table XLII.**

3L configurations with Si cost breakdown, at 2.5 kHz and 10 kHz switching frequencies.

Component	3L with Si 2.5 kHz			3L with Si 10 kHz		
	Qty	Cost [€]	[%]	Qty	Cost [€]	[%]
<b>Semiconductors</b>	9	753.12	6.96	9	753.12	7.01
<b>Drivers</b>	9	1626.39	15.02	9	1626.39	15.15
<b>Busbar</b>	3	2541	23.47	3	2541	23.67
<b>Cooling system</b>	3	366.72	3.39	3	446.16	4.16
<b>DC link capacitors</b>	12	813.12	7.51	12	813.12	7.57
<b>Control board</b>	1	599.51	5.54	1	599.51	5.58
<b>Sensors</b>	8	1243.8	11.49	8	1243.8	11.58
<b>Circuit breakers and security</b>	3	1405.18	12.98	3	1405.18	13.09
<b>Output filter</b>	1	447.83	4.14	1	278.85	2.60
<b>Cables, connectors and mechanical envelope</b>	/	1029.48	9.51	/	1029.48	9.59
<b>Total</b>		10826.15	100		10736.61	100
<b>Difference [€]</b>					-89.54	

### 4.4.4. LCoCE

The LCoCE of the 3L configuration with Si is calculated using the methodology presented in Section 4.1.3. Table XLIII summarizes the results. In the case of the 3L configuration, the cost reduction by increasing the switching frequency does not justify the AEP loss due to the reduced efficiency. The LCoCE is penalized when the switching frequency is increased.

**Table XLIII.**  
LCoCE of the 3L configuration with Si.

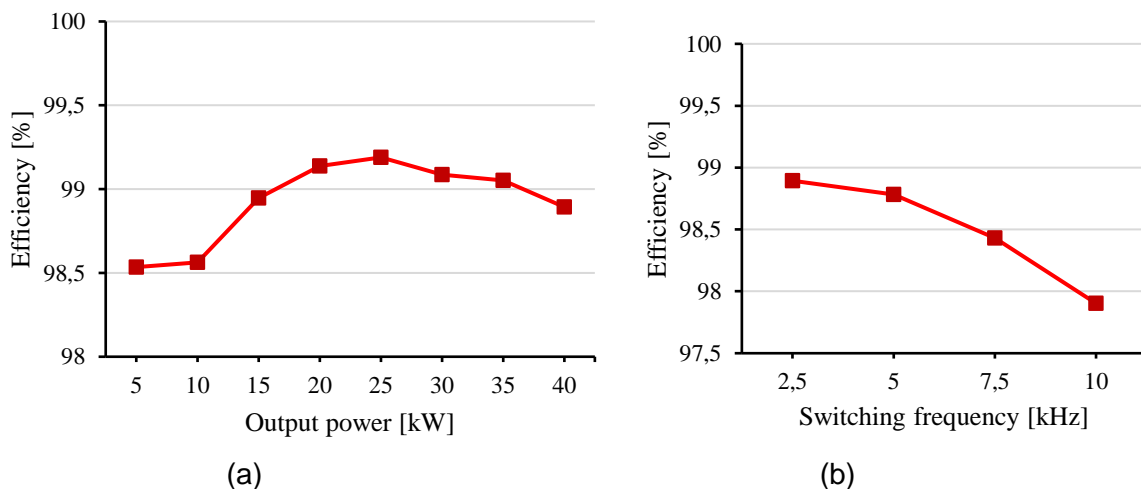
Configuration	3L with Si 2.5 kHz		3L with Si 10 kHz	
Parameter	Value	Unit	Value	Unit
Weighted AEP	115.77	MWh	113.23	MWh
Total cost	10826.15	€	10736.61	€
LCoCE	93.514	€/MWh	94.821	€/MWh
Difference			+1.397	%

## 4.5. 3 level with SiC

This section analyzes the 3L topology with SiC MOSFETs. The procedure is the same as for the baseline. First, the efficiency tests performed in the lab are shown. Next, the converter optimization is performed, and the system cost calculated. Finally, the LCoCE is analyzed.

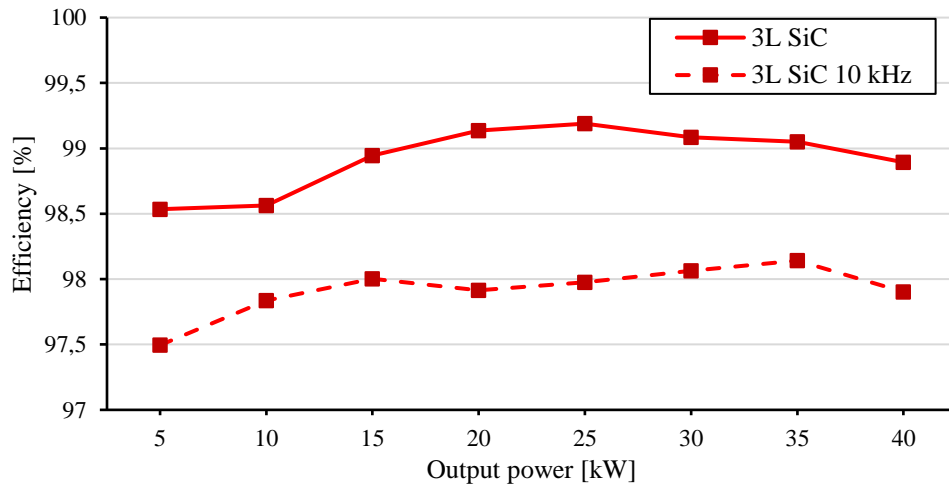
### 4.5.1. Efficiency tests

First, the 3L configuration with SiC is analyzed for different output powers at 2.5 kHz switching frequency in Figure 4. 14(a). Next, the switching frequency is increased up to 10 kHz at maximum output power in Figure 4. 14(b). The results show a high efficiency at low power, up to 98.5 % with 5 kW load. The maximum efficiency is greater than 99.1 %, but decreases below 99 % with increased power. This is because the 3L topology has more semiconductors than the 2L in the current path, so the conduction losses penalize this configuration. All the efficiency tests are performed according to the conditions described in Section 4.1.1 and in Table XXXIV.



**Figure 4. 14.** Efficiency tests of the 3L with SiC configuration, (a) for different output powers at 2.5 kHz switching frequency and (b) for different switching frequencies at maximum output power.

The 3L configuration with SiC is also tested at 10 kHz switching frequency for all the output powers, as shown in Figure 4. 15. The configuration shows a nearly constant efficiency around 98 % at 10 kHz switching frequency for all the operation points, showing better performance compared to the Si based converters.



**Figure 4. 15**

Efficiency tests of the 3L configuration with SiC for different output powers and switching frequencies.

#### 4.5.2. Converter optimization

In this section, the cooling system and the output filter of the 3L configuration with SiC are optimized according to the methodologies presented in Section 4.1.2. In addition, increasing the switching frequency is also analyzed. Regarding the cooling system, the thermal model in Figure 4. 1(b) is applied to each configuration for the maximum losses registered in the tests shown in Figure 4. 15. Next, the cost of the cooling system is calculated using (64). In the case of the 3L configurations, the cooling system is calculated per phase. The filter is calculated for each configuration depending on the topology level, 3 in this case, and the switching frequency, 2.5 kHz and 10 kHz. Figure 4. 6 shows the cost of the output filter in each case. Table XLIV summarizes the obtained results.

**Table XLIV.**

3L configuration with SiC converter optimization summary.

Configuration	3L with SiC 2.5 kHz		3L with SiC 10 kHz	
	Value	Unit	Value	Unit
Maximum $P_{loss}$	442	W	838	W
Maximum $R_{th}$ per phase	0.9527	°C/W	0.6205	°C/W
Cooling system cost (per phase)	52.75	€	66.33	€
Filter cost	447.83	€	278.85	€

### 4.5.3. System cost

Table XLV shows the cost breakdown of the 3L configuration with SiC at 2.5 kHz and 10 kHz switching frequency. The major difference is brought by the cost of the output filter. While increasing the switching frequency increases the cost of the cooling system due to the higher losses, the output filter can be reduced. The total cost of the system is slightly reduced by increasing the switching frequency, because the output filters represent a higher percentage of the total cost than the cooling system. Once again with SiC, the semiconductors are the highest cost of the configuration. In addition, the busbar is also a high cost due to its complexity and the three separated pieces. The drivers also represent a large portion of the cost due to the high number of the components.

**Table XLV.**

3L configurations with SiC cost breakdown, at 2.5 kHz and 10 kHz switching frequencies.

Component	3L with SiC 2.5 kHz			3L with SiC 10 kHz		
	Qty	Cost [€]	[%]	Qty	Cost [€]	[%]
<b>Semiconductors</b>	9	2629.08	21.04	9	2629.08	21.26
<b>Drivers</b>	9	1626.39	13.02	9	1626.39	13.15
<b>Busbar</b>	3	2541	20.34	3	2541	20.55
<b>Cooling system</b>	3	158.27	1.27	3	199	1.61
<b>DC link capacitors</b>	12	813.12	6.51	12	813.12	6.58
<b>Control board</b>	1	599.51	4.80	1	599.51	4.85
<b>Sensors</b>	8	1243.8	9.96	8	1243.8	10.06
<b>Circuit breakers and security</b>	3	1405.18	11.25	3	1405.18	11.36
<b>Output filter</b>	1	447.83	3.58	1	278.85	2.26
<b>Cables, connectors and mechanical envelope</b>	/	1029.48	8.24	/	1029.48	8.33
<b>Total</b>		12493.66	100		12365.41	100
<b>Difference [€]</b>					-128.25	



#### 4.5.4. LCoCE

The LCoCE of the 3L configuration with SiC is calculated next, using the methodology presented in Section 4.1.3. Table XLVI summarizes the results. Once again, the benefits of increasing the switching frequency in the 3L configuration are not clear, being the improvement is less than -0.009 %. The small cost reduction by increasing the switching frequency does not justify the AEP loss brought by the worse efficiency.

**Table XLVI.**  
LCoCE of the 3L configuration with SiC.

Configuration	3L with SiC 2.5 kHz		3L with SiC 10 kHz	
Parameter	Value	Unit	Value	Unit
Weighted AEP	119.87	MWh	118.65	MWh
Total cost	12493.66	€	12365.41	€
LCoCE	104.226	€/MWh	104.217	€/MWh
Difference			-0.0086	%

### 4.6. Configuration comparison

This section compares the analyzed configurations in terms of efficiency and system cost. The most important parameter, the LCoCE, that includes the previous two, is also analyzed.

#### 4.6.1. Efficiency

The configurations using SiC semiconductors show better efficiency than their Si counterparts. In addition, the excellent switching characteristics of SiC, allows to increase the switching frequency without penalizing the efficiency as much.

One of the goals of the 3L configurations is to reduce the switching losses. However, the good switching performance of SiC makes the 2L configuration compete with the 3L in efficiency, so the benefits of selecting a 3L configuration due to efficiency are not clear when using SiC modules.

#### 4.6.2. System cost

The most cost-efficient configuration is the baseline. Regarding the system cost, all the configurations reduce the cost by increasing the switching frequency. This is because the filters are big contributors to the total cost of the system, and can be reduced with increased switching frequency. However, the reduction in the filters is not as significant for 3L configurations as it is for the 2L ones, so the cost reduction with increased switching frequency is lower for 3L than for 2L. In addition, the increased component count such as drivers and semiconductors also penalize the 3L configurations.

The configurations with SiC are penalized due to the high cost of the semiconductors. The cost difference over equivalent Si devices is about 3.5 times in 1.2 kV voltage rating semiconductors, used in the 3L configurations. On the other hand, the cost difference is

nearly 4.7 in higher voltage semiconductors used for 2L configurations, penalizing SiC severely. Although the cost difference in the SiC modules is higher for the 2L configuration, its total cost is lower than the 3L configuration due to the reduced component count.

### 4.6.3. LCoCE

The cost of the system is the main parameter affecting the LCoCE calculation. This is why the baseline gets the best LCoCE. The only real contender is the 2L configuration with SiC. However, it still has 11 % worse LCoCE than the baseline. If the switching frequency is increased, the difference is reduced to 7.48 %, making it an interesting contender. Finally, every 3L configuration is very far in terms of LCoCE due to their high cost.

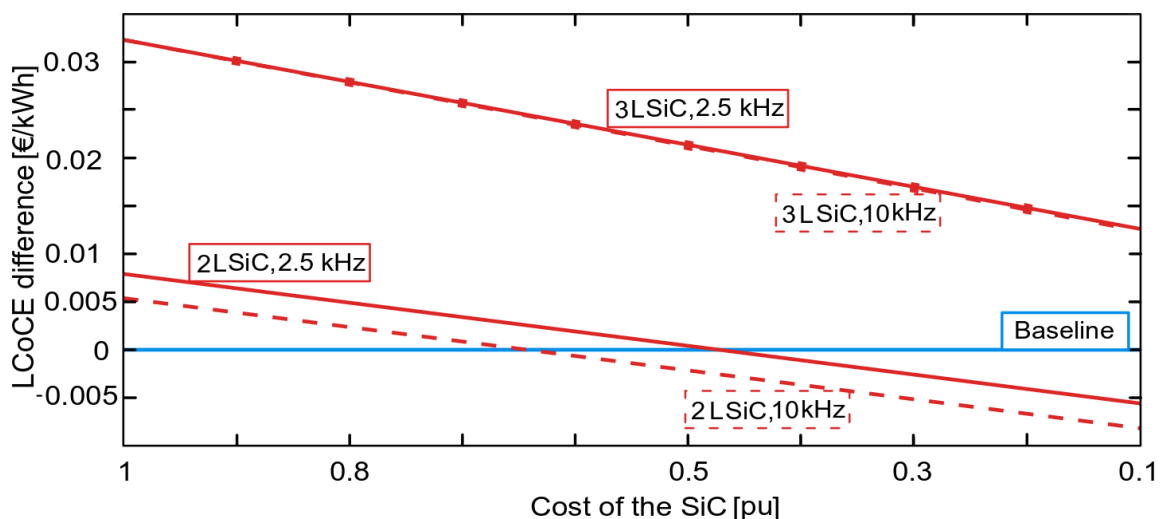
The baseline's LCoCE cannot be improved with today's SiC semiconductor costs.

### 4.6.4. Future scenario

The results in this chapter show the LCoCE of the baseline cannot be improved with the current cost of the semiconductors. In order to extend the analysis to a future scenario, the forthcoming cost reduction of the SiC semiconductors is considered, as done in Section 2.5.3.

Figure 4. 16 shows the LCoCE difference between the studied configurations, depending on the cost of the SiC. 2L configurations with SiC can improve the LCoCE of the baseline if the cost is reduced by half. However, and due to its lower total cost, the 2L configuration with increased switching frequency already improves the LCoCE of the baseline at the 65 % of the current SiC cost.

Regarding the 3L configurations, it is not possible to improve the LCoCE of the baseline in any case due to the high total cost. In addition, increasing the switching frequency only provides a marginal advantage.



**Figure 4. 16.**

The evolution of the LCoCE difference depending on the cost of the SiC.

### 4.6.5. Conclusion

A new parameter named LCoCE is proposed as a methodology to compare the different configurations. This is done as a simplified calculation of the LCoE, to avoid the use of unreachable economical and industrial parameters.

The LCoCE of the laboratory prototypes are compared. The baseline obtains the best LCoCE, as a result of its low cost. Although the high cost of the devices penalize the configurations using SiC, the 2L configuration with SiC is the closest to the baseline. The LCoCE of this configuration can be further improved if the advantages of the increased switching frequency are considered.

Next, a future projection is done reducing the cost of SiC semiconductors. The LCoCE of the baseline is matched with the 65 % of the current cost of the SiC semiconductors with the 2L configuration and an increased switching frequency. The cost should be reduced over 50 % if the switching frequency is not increased in order to match the LCoCE of the baseline.

The 3L configurations are far from the LCoCE of the baseline. In addition, the LCoCE of the baseline cannot be improved with these configurations even if the cost of the SiC is reduced to the maximum. This occurs due to the high total cost of the 3L that are penalized by their high component count.

## 4.7. Verification of the LCoE calculation tool results

This section compares the results obtained by the LCoE calculation tool with the results obtained by the laboratory prototypes. First, the comparison methodology is explained. Next, the results of the comparison are shown and analyzed.

### 4.7.1. Methodology

The LCoE calculation tool analyzes several different configurations, with multiple variables. The power of the application, the configuration of the wind turbine and the grid voltage are some examples of parameters which the LCoE calculation tool considers but the laboratory prototype cannot vary.

In addition, the LCoE calculation tool considers several unknown parameters in the laboratory prototype, such as the *opex* or even civil engineering works. The cost of the mechanical parts like the blades or the tower are also nonexistent in the laboratory prototypes. There is a need to design a methodology to compare both the LCoE calculation tool results and the LCoCE results of the laboratory prototypes. The selected method is to analyze the results comparing them to their own baseline. Then, the variations and trends with respect their own baseline are studied.

The first step to perform a fair analysis between the different systems is to match all the parameters that the laboratory prototype does not consider to the ones of the baseline. The forced parameters are shown in Table XLVII., together with the ones that are considered for the analysis.

**Table XLVII.**

The forced and considered parameters in the LCoE calculation tool.

Parameter	Value	Status
WT configuration	DFIG	Forced
Power of the system	5 MW	Forced
Grid voltage	690 V <sub>AC</sub>	Forced
Topology	2L and 3L	Considered
Technology	Si and SiC	Considered
Switching frequency	2.5 and 10 kHz	Considered

Next, the LCoCE of the configurations obtained in the LCoE calculation tool is calculated using (72). The LCoE calculation tool already calculates the *Weighted AEP* correctly, as shown in Section 2.3.4. But the *Total cost of the system* needs to be readdressed. This parameter is recalculated for the configurations in the LCoE calculation tool, considering only the components in (73).

Having the LCoCE of the configurations in the LCoE calculation tool, the variation with respect to their own baseline is calculated. The results are shown in variation percentage with respect to the baseline (74). The same calculation is performed for the configurations obtained in the laboratory.

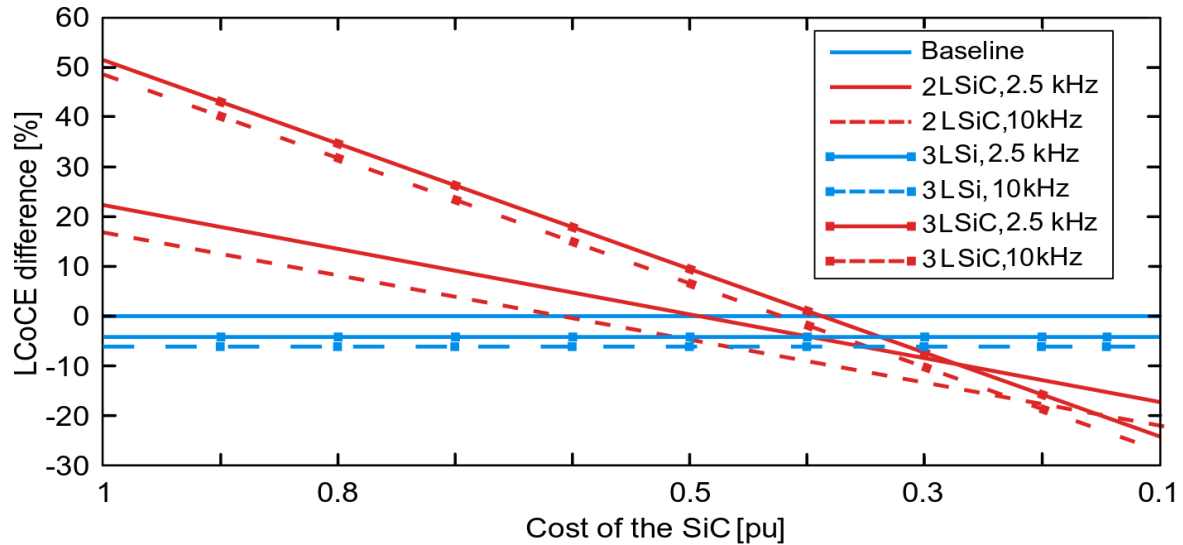
$$\Delta LCoCE [\%] = 100 \cdot \frac{LCoCE_{Configuration} - LCoCE_{Baseline}}{LCoCE_{Baseline}} \quad (74)$$

#### 4.7.2. Configurations by the LCoE calculation tool

Figure 4. 17 shows the evolution of the variation of the LCoCE of the configurations calculated by the LCoE calculation tool depending on the cost of the SiC semiconductors. It is observed that increasing the switching frequency (dashed lines) benefits the LCoCE of every configuration. This benefit is more significant in the 2L configuration with SiC.

However, the configurations with SiC semiconductors do not improve the baseline with the current cost. If the cost of the SiC is reduced 60 %, the 2L with SiC and increased switching frequency improves the LCoCE of the baseline. This occurs at 50 % of the cost if the switching frequency is not increased.

Regarding the 3L configurations with SiC, they have worse LCoCE than the 2L unless the cost is reduced below 30 %. In addition, the cost of the SiC should go below 40 % in order to improve the LCoCE of the baseline. Contrarily, the 3L configuration with Si is favorable. It improves the LCoCE of the baseline over 5 %.



**Figure 4. 17.**

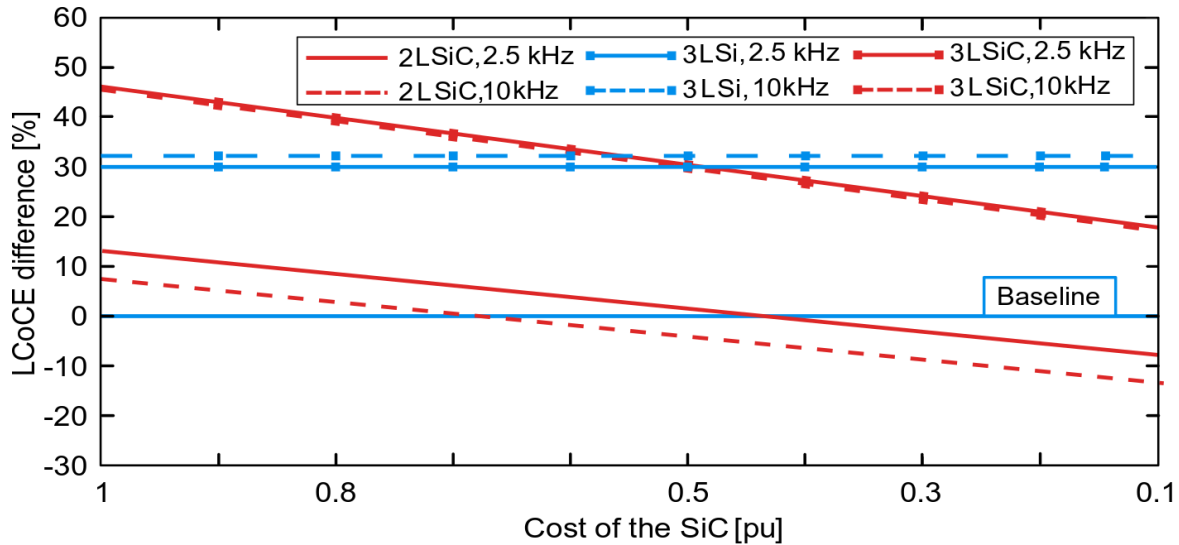
LCoCE difference respect to the baseline of the configurations from the LCoE calculation tool, for different costs of the SiC semiconductors.

### 4.7.3. Laboratory prototypes

Figure 4. 18 shows the evolution of the variation of the LCoCE of the laboratory prototypes depending on the cost of the SiC semiconductors. It shows that increasing the switching frequency benefits the LCoCE of the configurations with SiC semiconductors. However, the benefit is not equal for 2L and 3L configurations. While the LCoCE improvement with increased switching frequency is significant in the 2L configurations, it is negligible in the 3L.

The configurations with SiC semiconductors do not improve the LCoCE of the baseline with the current cost. The 2L configuration with SiC and increased switching frequency improves the LCoCE of the baseline if the cost of the SiC is reduced to be 70 %. The cost should go down until the 45 % in the case of the 2L configuration with low switching frequency.

The 3L configurations with SiC have worse LCoCE than the 2L. In addition, the 3L configuration with SiC will never improve the LCoCE of the baseline, even if the cost of the SiC is reduced to the maximum. Finally, the 3L configuration with Si does not improve the LCoCE of the baseline in the case of the laboratory prototypes, increasing it 30 %.



**Figure 4. 18.**

LCoCE difference respect to the baseline of the laboratory prototypes, for different costs of the SiC semiconductors.

#### 4.7.4. Analysis

This section analyzes the LCoCE results obtained for both cases in the previous section. The first is that in both cases increasing switching frequency improves the LCoCE of the configurations with SiC. Moreover, in both cases the benefit of increased switching frequency is more relevant in the 2L configuration.

Another identical aspect is that in both cases (LCoE tool and laboratory prototypes) the configurations with SiC do not improve the LCoCE with the current cost. However, in both cases the 2L configuration with SiC improves the LCoCE of the baseline with a reduction of the cost of the SiC. In the case of the configurations by the LCoE calculation tool, the break-even point is at 60 % of the current cost, while in the laboratory prototype, this point occurs at 70 % of the cost. Although the exact numbers do not match, similar trends are observed for the 2L configurations with SiC in the LCoE calculation tool and the laboratory prototype. When focusing on the 3L configurations, the trends between the configurations with SiC and with Si are similar in both cases. The configuration with Si has better LCoCE with the current cost, but it is improved by the configuration with SiC when the cost of SiC is reduced. This improvement occurs at 35 % of the current cost in the configurations by the LCoE calculation tool, while in the case of the laboratory prototypes this occurs at 50 % of the cost.

However, the main difference is observed with respect to the baseline. In the configurations by the LCoE calculation tool, the 3L with Si has better LCoCE than the baseline, but it is far from improving it in the laboratory prototypes. In addition, in the case of the configurations by the LCoE calculation tool, the 3L with SiC improves the baseline with a cost reduction, while this does not occur in the laboratory prototype, even with the maximum cost reduction. Even if some trends match, such as in the 2L configuration with SiC, it is not possible to expect similar results in the LCoE calculation tool and the laboratory prototype. While the cost data in the calculation tool is given by the industrial partner, taken from their well established industrialized product, the cost of the laboratory prototype is the one provided by the commercial suppliers. In addition, the laboratory prototypes are not optimized in cost, because the main objective was to design a functional and versatile test bench, see Section 3.1.

For these reasons, the divergences in the LCoCE results between the LCoE calculation tool

configurations and the laboratory prototypes are considered coherent. Finally, the main four conclusions are verified, because both the LCoE calculation tool configurations and the laboratory prototype fulfill them:

1. The configurations with SiC cannot improve the LCoE of the baseline with the actual cost of the SiC semiconductors.
2. The most promising configuration using SiC semiconductors is the 2L, due to the high cost of the 3L because of the high component number.
3. The 2L configuration with SiC can improve the LCoE of the baseline if the cost of the SiC semiconductors is reduced in the future.
4. Increasing the switching frequency improves the LCoE of the configurations with SiC, and is very interesting in the 2L configuration.

CHAPTER 5

**Challenges of silicon carbide in  
high power applications**



## 5.Challenges of silicon carbide in high power applications

This chapter presents the major challenges silicon carbide (SiC) technology faces in high power applications. The objective is to identify the destructive phenomenon, as well as other notable differences with silicon (Si). By modelling these issues, prevention techniques are presented. Experimental verification of the modelling, the prevention techniques and comparison with Si are also presented.

The first destructive phenomenon is the false turn on. This is suffered by the device turning off in a half bridge, while the other is turning on. If the false turn on is severe, and lasts long enough, the resulting short circuit current is damaging.

Another challenge is to control the overshoot on the turn off while keeping switching speed high. This is an overvoltage occurring in the device due to the high current changing rates as well as the inductance in the switching loop. If the overvoltage exceeds the maximum blocking voltage of the device, this is severely damaged.

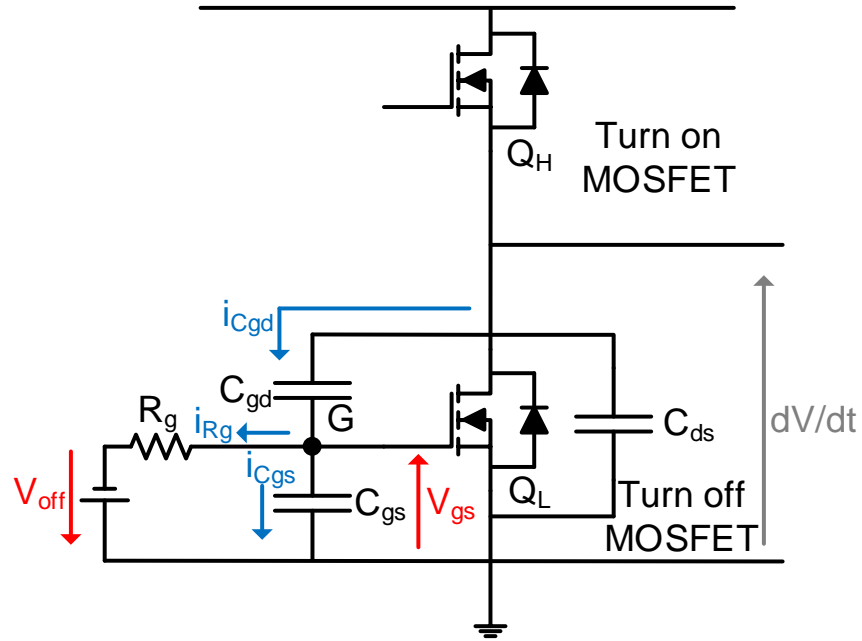
Protections such as the overcurrent protection sensing should also be designed specifically for SiC. Due to the high dynamics of the SiC modules, the sensing circuits might suffer disturbances, never considered with slow Si devices.

Finally, measurement techniques and equipment is also studied for SiC. General measurement issues are presented, together with techniques to correctly perform them. In addition, recommendations to select the correct equipment for each system are given.

### 5.1. False turn on

#### 5.1.1. Phenomenon

The false turn on is a potentially destructive phenomenon occurring in power devices switching at high speed in half bridge structures. The off device turns on unintentionally on the turn on of the opposite device. It can occur during a short period, but it can also extend during a considerable time. Figure 5. 1 shows the circuit which models the turn on issue during the following section.



**Figure 5. 1.**

Circuit schematic used to explain the false turn on phenomenon, with the considered parasitics and parameters.

The consequence of a false turn on is the short circuit of the DC voltage. This happens because both the high and low switches are on during a period of time. The current through both devices increases, and can lead to high degradation or even the failure of the device.

### 5.1.2. Analytical modelling

In this section, a simplistic model of the false turn on is presented, in order to identify the main critical parameters affecting the phenomenon. The objective is to understand the phenomenon better, analysing the circuit in Figure 5. 1. First, the condition to turn on a device is presented (75). If the gate to source voltage  $V_{gs}$  surpasses the threshold voltage  $V_{th}$  of a device, this will start to turn on. In this moment, the device will start conducting current through the drain.

$$V_{gs} \geq V_{th} \quad (75)$$

The  $V_{gs}$  is the instantaneous voltage between the gate and source terminal. Its dynamic depends on the charge of the equivalent gate to source capacitor  $C_{gs}$  (76), thus, on the current flowing through it  $i_{Cgs}$  (77), which is calculated applying Kirchhoff current law in point  $G$  of Figure 5. 1. Therefore, according to Figure 5. 1,  $V_{gs}$  does not only depend on the current  $i_{Rg}$  through the external driving circuit, but also on the current  $i_{Cdg}$  flowing through the  $C_{gd}$  parasitic capacitor.

$$V_{gs} = V_{Cgs} = \frac{1}{C_{gs}} \int_0^t i_{Cgs} dt \quad (76)$$

$$i_{Cgs} = i_{Cdg} - i_{Rg} \quad (77)$$

At the same time,  $i_{Cdg}$  can be expressed as the current through the reverse transfer capacitance  $C_{rSS}$ , better shown in Figure 5. 1 as  $C_{dg}$  (78).

$$i_{cga} = C_{ga} \frac{dV_{dg}}{dt} \quad (78)$$

In addition,  $V_{gs}$  is also a function of the turn off voltage  $V_{off}$  applied by the driver, and the voltage drop in the gate resistance  $R_g$  (79), by applying Kirchhoff voltage law in point  $G$  in Figure 5. 1.

$$V_{gs} = V_{cgs} = i_{Rg}R_g - V_{off} \quad (79)$$

### 5.1.3. Critical variable identification

Using the simple analytical model presented in the previous section, this section identifies the critical variables affecting the false turn on. The variables are listed and classified depending on their nature. Variables that are dependent on the device or the application are considered passive, as the designer cannot change them. The ones that are design selections are considered active, as the designer can act on them, to prevent the false turn on. Table XLVIII shows the variable identification and its classification.

**Table XLVIII.**

Critical variables affecting the false turn on and its classification.

Variable	Classification
$C_{gs}$	Passive
$C_{dg}$	Passive
$\frac{dV_{dg}}{dt}$	Active
$R_g$	Active
$V_{off}$	Active

The passive variables are dependent on the modules that are being used, and will be discussed in the next section. The actives, on the other hand, can be controlled by the designer. Their effect on the false turn on phenomenon is presented next.

Having high  $dV_{dg}/dt$  increases  $i_{cga}$ , as shown in (78). As part of this current will charge  $C_{gs}$  as explained in (76) and (77), having high  $dV_{dg}/dt$  is directly related to the risk of suffering the false turn on phenomenon.

The effect of  $R_g$  should be analyzed carefully. Increasing  $R_g$  increases the risk of suffering a false turn on for the same  $i_{Rg}$  (79). However, having a high gate resistance will slow down the device, reducing the  $dV_{dg}/dt$  that causes the undesired  $i_{cga}$ .

Finally, having a negative turn off voltage  $V_{off}$  reduces the risk of turning on the device accidentally (79).

### 5.1.4. Comparison with silicon

This section compares the false turn on phenomenon between the SiC MOSFETs and the Si IGBTs. Table XLIX compares equivalent 1.2 kV SiC MOSFETs and Si IGBTs, with their expected switching times by the manufacturers.

**Table XLIX.**

Rise and fall time comparison between equivalent 1.2 kV SiC MOSFETs and Si IGBTs, at maximum current and 600 V<sub>DC</sub>.

Variable	SiC MOSFET	Si IGBT	Unit
Reference	FF6MR12KM1	FF200R12KT4	
$t_{rise}$	32.0	45.0	ns
$t_{fall}$	45.2	160	ns

The expected switching times are considerably faster for the SiC. This leads to a higher  $dV_{dg}/dt$  because the same voltage is switched in less time. This increases the risk of suffering a false turn on, as explained in the previous section.

The faster switching times of the SiC makes more likely to suffer a false turn on with this technology than with Si. The rare false turn on phenomenon in high power Si modules should carefully be considered when introducing SiC MOSFET high power modules.

### 5.1.5. Prevention techniques

There are two main design decisions that can be made in order to prevent a false turn on. The first is to slow down the device in order to reduce the  $dV_{dg}/dt$ . This is done by increasing the gate resistance  $R_g$ . However, if the device is not slowed down sufficiently, and  $i_{Rg}$  is not reduced, increasing  $R_g$  can have a negative impact, as explained in Section 5.1.3, and shown in (79). Another negative effect of slowing down the device is the increment of the switching losses.

The other decision that can be made is to supply a negative voltage in the driver during the turn off of the device (79). This will increase the security margin in the gate voltage before the threshold voltage is met, and makes the false turn on more unlikely to happen even if a voltage spike appears in the gate.

This last decision increases the cost and complexity of the driver, and the maximum negative gate voltages of the device should be checked for security. However, it is a good technique to reduce the risk of suffering false turn on phenomenon in SiC high power modules, and most of the driver manufacturers are already considering it in their products. This technique is also recommended in the reference designs of most of the SiC device manufacturers.

## 5.2. Overshoot

### 5.2.1. Phenomenon

The overshoot is an overvoltage occurring on the turning off device. It is caused by the fast current changing rate and the inductance in the switching loop. Due to the high  $di/dt$ , the parasitic inductance of the loop experiences a voltage, which is added to the DC voltage of the system. If the overvoltage is greater than the maximum blocking voltage of the device, a breakdown will occur. This is a fatal error that leads to the destruction of the device. The whole phenomenon is widely explained in Section 3.3, and shown in Figure 3. 7.

### 5.2.2. Analytical modelling

This section presents a simple model to understand the overshoot phenomenon and to identify the main parameters affecting it. However, as each topology needs to be addressed independently, a methodology to analyze them is shown. (80) shows the drain to source voltage in a turning off device, and (81) represents the value of the overshoot.  $L_{StrayTotal}$  refers to the total parasitic inductance in the switching loop that is being turned off. This is why each topology requires an individual analytical model.

$$V_{ds} = V_{dc} + V_{overshoot} \quad (80)$$

$$V_{overshoot} = L_{StrayTotal} \cdot \frac{di}{dt} \quad (81)$$

The first step is to identify the switching loops of the selected topology. While the 2L topology has only one switching loop, the 3L ANPC topology has two pairs of symmetrical switching loops for example. The next step is to identify the parasitic inductances contributing to the  $L_{StrayTotal}$  in each switching loop. Even if each switching loop is different, and should be analyzed individually, there are always three types of parasitic inductances contributing to the total inductance (82). The total stray inductance  $L_{StrayTotal}$  is the sum of the parasitic inductance of the modules that are part of the switching loop  $L_{modules}$ , plus the parasitic inductance of the connections, represented as  $L_{busbars}$  and the parasitic inductance of the capacitors  $L_{capacitors}$ .

$$L_{StrayTotal} = L_{modules} + L_{busbar} + L_{capacitors} \quad (82)$$

A detailed example of this analysis is shown in Section 3.3, for a 3L ANPC topology.

### 5.2.3. Critical variable identification

Using the general analytical model presented in the previous section, this section identifies the critical variables affecting the overshoot. This variables are listed and classified depending on their nature. Variables that are dependent on the device or the application are considered passive, as the designer cannot change them. The ones that are design selections are considered active, as the designer can act on them, to prevent a severe overshoot. Table L shows the variable identification and its classification.

**Table L.**

Critical variables affecting the overshoot and its classification.

Variable	Classification
$L_{modules}$	Passive
$L_{capacitors}$	Passive
$\frac{di}{dt}$	Active
$L_{busbar}$	Active

In the case of an overshoot, having a small  $L_{StrayTotal}$  is essential (81). This is why the component selection is critical, in order to minimize the effect of the so called passive variables. In addition, there are layout and design techniques to further minimize the inductance of the selected components, explained in Section 5.2.5.

As for the active variables, the design of the busbar plays a major role. The most important factor when minimizing  $L_{busbar}$  is the layout of the converter. The physical position of each component highly affects the parasitic inductance of the connections. The design techniques used when designing the busbar are also important. Finally, reducing the  $di/dt$  of the application by increasing the  $R_g$  also reduces the overshoot (81), but with the penalty of increasing the switching losses.

#### 5.2.4. Comparison with silicon

This section compares the overshoot issue between the high power SiC and Si modules. The parasitic inductance of the capacitors is not affected by the technology, as the capacitors used for the converters are the same for SiC and Si. The packages of high power SiC and Si modules determining the parasitic inductance of the module are variable. Some manufacturers, aware of the importance of the stray inductance for fast switching of the SiC, are opting to optimize the stray inductance of their SiC modules, creating specific high power packages for SiC. However, there are several high power SiC modules using traditional packages, such as the 62 mm, looking for a simple transition from Si to SiC.

The main difference is once again in the switching times. Table LI shows a comparison between the expected  $di/dt$  for different Si and SiC high power modules. In addition, the maximum allowable switching loop inductance is calculated using (81), to keep the overshoot under control and use the module with 50 % of voltage derating. This means that if a 1.2 kV module is used, the DC voltage is 600 V, and the maximum allowable overshoot before a breakdown is also 600 V.

**Table LI.**

Si and SiC high power modules  $di/dt$  comparison, with the maximum allowable inductance in the switching loop to operate at 50 % of voltage derating.

Module reference	Technology	$V_{ds}/V_{ce}$ [kV]	$I_d/I_c$ [A]	Maximum $di/dt$ [A/ns]	Maximum allowable inductance in the switching loop [nH]
FF200R12KT4	Si	1.2	200	2	300
FF6MR12KM1	SiC	1.2	250	8.86*	68
FF300R17KE4	Si	1.7	300	3.75	226
FF8MR20KM1	SiC	2	185	8.6*	116
*Data obtained in the laboratory.					

It is shown the allowable inductance in the power loop is several times smaller for high  $di/dt$  values of SiC modules. This means careful design of the busbar and layout of the converter should be done to use the SiC modules at high switching speed. The converter layouts and busbar designs made for Si IGBTs might not be useable with SiC modules anymore, forcing high power engineers to perform an extra effort with novel switching loop designs.

### 5.2.5. Prevention techniques

There are two ways of reducing the overshoot effect, according to (81). The first is to slow down the device, by reducing the  $di/dt$ . However, once again, and as explained in Section 5.1.5, this increases the switching losses of the device.

The preferred option should be to optimize the converter design to minimize the  $L_{StrayTotal}$  of each switching loop. The first step is to select the most suitable components, considering their stray inductance as one of the main selection criteria. The next is physically locating the components in the optimum positions, analyzing the effect this will have in the connections and in the switching loops. Finally, designing the connection busbar is key. Using design techniques to minimize the parasitic inductances, such as paralleling components, considering the returning current paths and using the magnetic cancellation to reduce the mutual inductance are of great importance.

A whole optimized design, considering the aforementioned prevention techniques and explaining each one in detail is presented in Section 3.3.

### 5.2.6. Experimental verification

Each prevention technique is experimentally verified by means of impedance measurement in Section 3.3. The reduction of the parasitic inductance is measured using an impedance analyzer. The importance of the component selection, correct component paralleling, layout and connection by an optimum busbar design is verified. In addition, Section 3.3.4 validates the switching performance of the designed busbar, using double pulse testing. The achieved waveforms are shown in each case.

### 5.3. Overcurrent protection

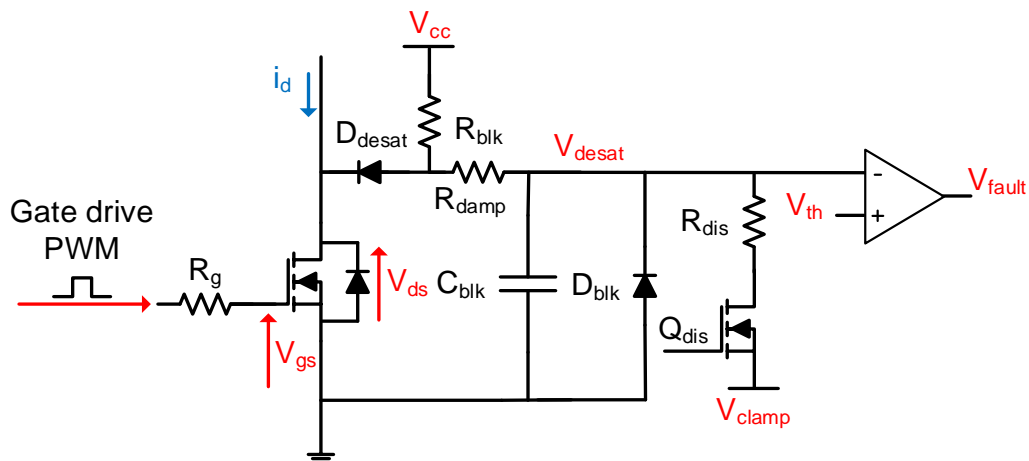
The need of overcurrent protection in high power and high voltage SiC modules is critical, because they have weaker short circuit withstand capability than their low voltage counterparts [133]. In addition, this overcurrent protection needs to be fast (less than 10  $\mu\text{s}$ ) to prevent degradation [134].

The desaturation sensing (Desat) is a faster overcurrent protection than solid state circuit breakers [135], for example, offering a relatively simple detection circuit and reliable performance. This protection is integrated in most of the commercial high power SiC module drivers. However, care should be taken when designing or programming the Desat limits when using high power SiC modules, in order to prevent false Desat triggering.

In this section, first a general overview of the Desat sensing technique and circuit is presented. Next the issue of false Desat triggering is addressed when operating with high power SiC modules. A comparison with silicon is made, to identify the major differences regarding the Desat sensing. Finally, considerations and recommendations are given to prevent this undesired phenomenon.

#### 5.3.1. Desat sensing

Figure 5. 2 shows a general Desat detection circuit. During the normal operation, the  $D_{desat}$  diode is forward biased. During an overcurrent fault,  $I_d$  increases drastically, increasing  $V_{ds}$  and reverse-biasing  $D_{desat}$ .  $C_{blk}$  is then charged through  $V_{cc}$ . When the capacitor voltage reaches the threshold voltage in the comparator  $V_{th}$ ,  $V_{fault}$  flips, triggering the overcurrent detection.  $Q_{dis}$  and  $R_{dis}$  are used to discharge  $C_{blk}$  when the protected SiC MOSFET is off. The  $D_{desat}$  diode is usually a SiC Schottky diode, or more than one in series, because it should have at least the same blocking voltage as the protected SiC MOSFET.

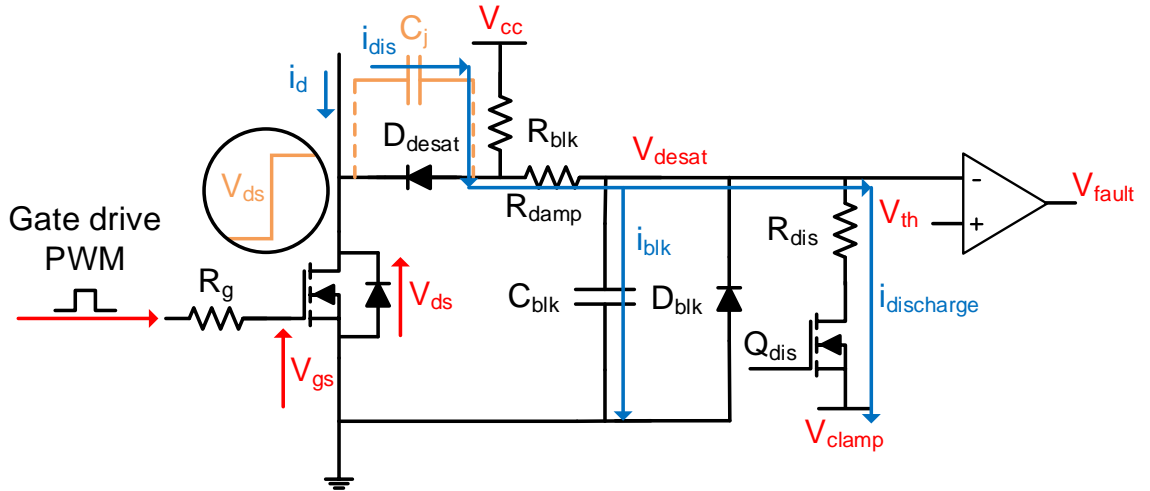


**Figure 5. 2.**  
Desat detection circuit.

#### 5.3.2. False Desat triggering

This section explains the false Desat trigger phenomenon in a simplistic way, with the objective to identify the differences with Si and provide recommendations to overcome the issue. During a regular turn off, the  $dV_{ds}/dt$  of the SiC MOSFET can falsely trigger the Desat detection. Figure 5. 3 shows the Desat detection circuit under a turn off of the SiC MOSFET.





**Figure 5. 3.**

Desat detection circuit under a turn off of the SiC MOSFET, with the displacement current through the junction capacitance.

The high voltage transient induces the displacement current  $i_{dis}$  through the junction capacitance  $C_j$  of the Desat diode  $D_{desat}$ . Even if  $Q_{dis}$  is added to absorb  $i_{dis}$  through  $R_{dis}$  when the SiC MOSFET is off, a positive voltage spike will occur in  $C_{blk}$ , which can falsely trigger the Desat detection if the spike is greater than the reference voltage  $V_{th}$  in the comparator.

A simple model is shown next to present the main variables affecting the voltage spikes falsely triggering the Desat detection.  $i_{dis}$  is dependent on the junction capacitance of the desat diode, and on the  $dV_{ds}/dt$  of the SiC MOSFET (83). Applying Kirchhoff current law,  $i_{blk}$  is calculated (84), which is a function of the displacement current  $i_{dis}$ . Finally, the voltage spike in  $V_{desat}$  is inversely proportional to  $C_{blk}$  and proportional to the current through it during the time the  $dV_{ds}/dt$  lasts in the SiC MOSFET (85).

$$i_{dis} = C_j \frac{dV_{ds}}{dt} \quad (83)$$

$$i_{blk} = i_{dis} - i_{discharge} \quad (84)$$

$$V_{desat} = \frac{1}{C_{blk}} \int_0^t \left( \frac{dV}{dt} \right) (i_{dis} - i_{discharge}) dt \quad (85)$$

It is concluded the junction capacitance of the Desat diode, the  $dV_{ds}/dt$  of the SiC MOSFET, as well as the  $C_{blk}$  capacitor value are key to control the voltage spike. In addition, the time in which  $dV_{ds}/dt$  occurs is also important.

### 5.3.3. Comparison with silicon

As seen in the previous section, the  $dV_{ds}/dt$  of the device is a key parameter when suffering false Desat detection. This has traditionally been low in high power Si IGBTs, but is increased reaching 30 V/ns with the high power SiC MOSFETs. With these high voltage variation rates, the false Desat detection becomes an issue.

In addition, and as observed in (85), the switching time is also key. This is why the higher the voltage the device is switching with the same  $V_{ds}/dt$  the higher the voltage spike will be. [136] demonstrates high voltage SiC MOSFETs are more likely to suffer high voltage spike in  $V_{desat}$  sensing voltage due to the longer times spent at high  $dV_{ds}/dt$ .

### 5.3.4. Considerations and recommendations

[137] presents a design guide for improving the noise immunity of Desat detection circuits. The first recommendation is to reduce  $C_j$  as much as possible. This can be done by implementing several lower voltage SiC Schottky diodes in series as  $D_{desat}$  diode. This technique will reduce the resultant junction capacitance, reducing the risk of a false Desat detection.

Another technique is to increase slightly  $R_{damp}$ . However, this resistor cannot be increased considerably, as it needs to be much smaller than  $R_{blk}$ . Finally, a high  $C_{blk}$  will also reduce the voltage spike in  $V_{desat}$ . However, this results in a significant increase of the blanking time, which can lead to a high current in the SiC MOSFET during this period [135].

## 5.4. Measurements

The need of proper measurements is well known by high power engineers. It is mandatory to capture several voltage and current waveforms during the design steps, in order to predict, and solve the aforementioned issues in the semiconductors.

Although novel techniques are being proposed to measure the switching losses, the traditional and most used methodology is to evaluate the captured voltage and current waveforms. If the measurement is not correctly done, the expected switching losses are miscalculated. This can lead to an incorrect cooling system design, and even to a catastrophic end in some cases.

Knowing the importance of a correct measurement system, the high power engineers have solved this issue by developing specific techniques and equipment for the task. However, these are not always suitable to measure the faster dynamic characteristics of high power SiC modules. This section gives recommendations on how to select proper equipment, set up the measurement system as well as techniques to align correctly the voltage and current measurements, considering different delay times. Finally two alternative methodologies to measure are presented. This section will help the high power engineers to adapt the already used measurement systems to the more restrictive SiC requirements.

### 5.4.1. Equipment selection

The first task is to correctly select the measurement equipment. The major requirement is the minimum bandwidth of the voltage and current probes, together with the selected oscilloscope. Of course, voltage and current ratings also need to be met.

First, the minimum bandwidth concept is explained; next different types of voltage and current probes are presented, and their differences explained. Finally, the SiC requirements are compared with the Si, to illustrate the differences, and available equipment is listed.

#### 5.4.1.1. Minimum bandwidth

In order to measure the fast transients of SiC modules, even faster probes are required. The bandwidth  $BW$  of a signal is calculated using (86) [138], being the rise time  $t_{rise}$  the time required by the signal to rise from its 10 % to the 90 % [127]. The factor 0.35 can be used but up to 0.45 is recommended [138].

$$BW = \frac{0.35 \text{ to } 0.45}{t_{rise}} \quad (86)$$

The voltage and current probes should at least have 3 times the bandwidth of the signal to measure [138]. In addition, the oscilloscope should have even higher bandwidth than the probes, to avoid affecting the measurement [139].

#### 5.4.1.2. Voltage probe

The voltage probes adapt the voltage of the application to the input range of the oscilloscope [139]. They should at least satisfy the maximum voltage limit, the dynamic voltage range, the accuracy, the bandwidth and the isolation requirements of the application. There are two main types, active differential and passive probes.

Active differential probes measure the voltage between two points, neither of which is at ground level. The reference of an active differential probe can be at elevated and floating potential.

Passive probes have no isolation. Their reference is connected to the ground of the oscilloscope. This should be carefully considered when designing a measurement system, to avoid short circuiting different potential points through the passive probes and the ground of the oscilloscope.

#### 5.4.1.3. Current probe

The current probes provide an image of the sensed current and adapt it to the input ranges of the oscilloscope [139]. They should at least satisfy the maximum current limit, the dynamic current range, the accuracy and the bandwidth requirements of the application. In some cases, the usable rise time of the probe is provided by the manufacturer, instead of the bandwidth. This defines the minimum rise time that the current probe can measure with 10 % of error [140]. The rise time of the measured current should be superior to the one of the current probe. Finally, the physical installation of the current probe is also important, because an impedance is added to the loop by doing so. In addition, some current probes require adapting the power loop for their installation, so the physical characteristics of the probe should also be considered.

There are several types of current probes, but the most common ones are the split core probes, the Pearson current transformers, the Rogowski coils and the coaxial shunts. The first three work with magnetic field operation principles, while the coaxial shunts are resistors inserted in the circuit. While the first three current probes provide galvanic isolation, the coaxial shunt does not. In addition, it is the only one that is integrated in the power loop. The added inductance should be considered because of the effect it can have in the overshoot, due to the fast  $di/dt$  of SiC modules, see Section 5.2.

#### 5.4.1.4. Comparison with silicon requirements

Once again, the major difference between the novel high power SiC modules and the state of the art Si IGBTs is the switching speed. As presented in the previous section, the required bandwidth and the usable rise time of voltage and current probes change according to the switching speed of the modules. Table LII shows the comparison between several Si and SiC high power modules rise times and the required voltage probe bandwidths, calculated as shown in 5.4.1.1.

**Table LII.**

Si and SiC high power modules rise time comparison, with the required voltage probe bandwidth. Data obtained from datasheets.

Module reference	Technology	$V_{ds}/V_{ce}$ [kV]	$I_d/I_c$ [A]	Minimum rise time [ns]	Required voltage probe bandwidth [MHz]
FF200R12KT4	Si	1.2	200	45	23.3
FF6MR12KM1	SiC	1.2	250	32	32.8
FF300R17KE4	Si	1.7	300	55	19
FF8MR20KM1	SiC	2	185	46*	22.8

\*Data obtained in the laboratory.

The bandwidth requirements are superior for the SiC modules in both voltage ranges. This means the equipment used to measure Si IGBTs might not be valid to measure SiC MOSFETs. The data for FF8MR20KM1 is obtained in the laboratory as the module is still in development stage and the manufacturer could not provide an official datasheet.

In addition, the maximum  $di/dt$  of each high power module is also shown in Table LIII. The data is obtained from the datasheets in the case of Si, and measured in the laboratory for the SiC, see Section 3.5. The required current probe useable rise time is set to be just enough to be able to measure the according  $di/dt$ .

**Table LIII.**

Si and SiC high power modules  $di/dt$  comparison, with the required current probe useable rise time. Data obtained from datasheets and laboratory tests.

Module reference	Technology	$V_{ds}/V_{ce}$ [kV]	$I_d/I_c$ [A]	Maximum $di/dt$ [A/ns]	Required current probe useable rise time [A/ns]
FF200R12KT4	Si	1.2	200	2	+2
FF6MR12KM1	SiC	1.2	250	8.86*	+8.86
FF300R17KE4	Si	1.7	300	3.75	+3.75
FF8MR20KM1	SiC	2	185	8.6*	+8.6

\*Data obtained in the laboratory.

Again, the required useable rise time is superior for the SiC modules. The current probes used for Si should be double checked and ensure their useable rise time is enough to perform a correct measurement with the fast  $di/dt$  of SiC modules.

### 5.4.1.5. Available voltage probes

Table LIV presents several voltage probes available in the market. They are classified depending on their maximum voltage rating, their bandwidth and their cost. Regarding passive probes, it is seen they are limited in the maximum voltage ratings, not even reaching 1 kV. Even if the cost is overall affordable, and the bandwidth is good enough, the clear limiting factor is the voltage rating.

As for the active differential probes, there are several available options over the 1 kV range. However, if high bandwidth is required at high voltage, the cost increases over 1 k€. Differential probes are preferred to measure the  $V_{ds}$  in high power SiC modules, due to their high voltage rating and sufficient bandwidth. Isolation also is a key factor, to reduce the complexity of their installation.

**Table LIV.**

Several voltage probes available in the market.

Device	Type	$V_{max}$ [kV]	BW [MHz]	Cost [k€]*
<b>Tektronix TPP0051</b>	Pass	0.3	50	0.04
<b>Yokogawa 701938</b>	Pass	0.6	200	0.14
<b>Tektronix P2220</b>	Pass	0.3	200	0.18
<b>Rigol RP3500A</b>	Pass	0.3	500	0.21
<b>Tektronix TPP1000</b>	Pass	0.3	1000	1
<b>Pico TA057</b>	Diff	1.4	25	0.4
<b>Hameg HZ115</b>	Diff	1.4	35	0.5
<b>Pintek DP-08VF</b>	Diff	0.4	150	0.55
<b>Pintek DP-16VF</b>	Diff	8	150	0.6
<b>Pico TA042</b>	Diff	1.4	100	0.6
<b>Pico TA044</b>	Diff	7	70	0.9
<b>Tektronix P5205A</b>	Diff	1	100	2.2
<b>PKM Bumblebee</b>	Diff	2	400	3.25

\*Electronic equipment provider cost per single unit in 2022.

### 5.4.1.6. Available current probes

Table LV shows several available current probes in the market. They are classified depending on their type, maximum current rating, useable minimum rise time or bandwidth and the cost. Pearson and Rogowski coils provide the minimum rise time data, while the split core and coaxial shunt probes provide bandwidth information. The fastest current probe is the coaxial shunt, but its bandwidth will also be limited by the voltage probe used to measure the voltage in its terminals. Although the Pearson current transformer is cost effective, its minimum useable rise time is limited, and its physical installation complex.

**Table LV.**

Several current probes available in the market.

Device	Type	$i_{\max}$ [A]	Minimum useable rise time [A/ns]	BW [MHz]	Cost [k€]*
Iwatsu SS-240A	Split core	30	/	50	2.1
Iwatsu SS-260	Split core	150	/	10	3.3
Hioki 3274	Split core	300	/	50	3.9
CWT Mini HF6	Rogowski coil	1200	80	/	2
Pearson 410	Pearson	5000	20	/	0.38
T&M SDN-015	Coaxial shunt	$E_{\max}$ **	/	1200	0.35

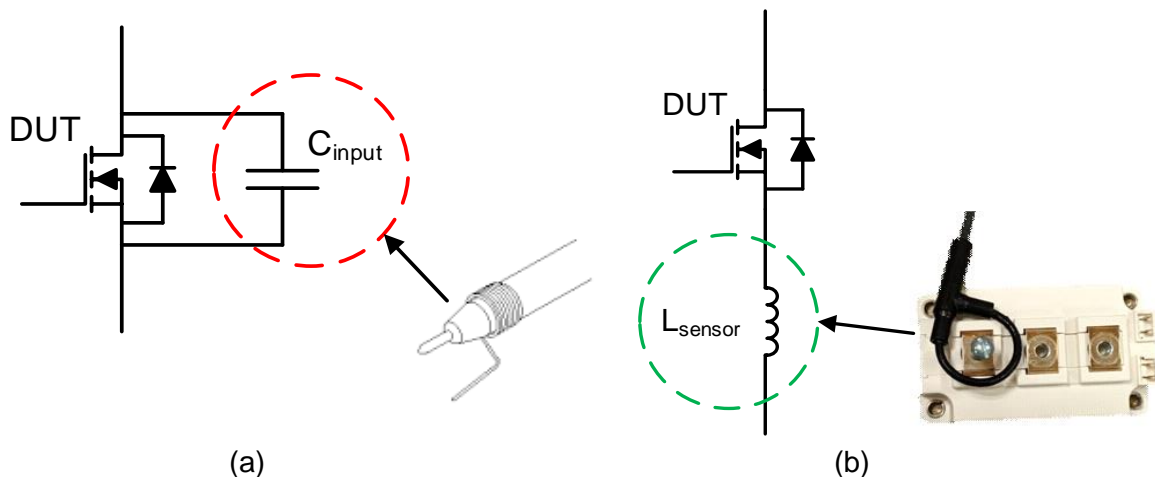
\*Electronic equipment provider cost per single unit in 2022.  
\*\*Dependent on current pulse duration.

## 5.4.2. Hardware set up

This section presents the most common hardware issues when setting up the measurement system. First, the effect of the introduction of voltage and current probes in the in the original circuit is analyzed. Then the grounding loop is specifically analyzed. Finally, the analysis is compared to Si IGBTs.

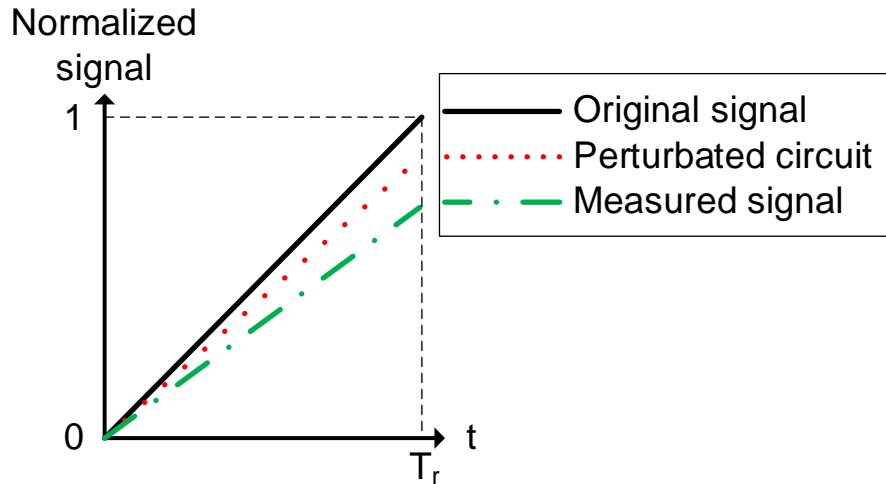
### 5.4.2.1. Circuit perturbation

Voltage and current probes are not ideal, and their input capacitance as well as inductance affect the measured circuit. As shown in Figure 5. 4(a), voltage probes add parallel capacitance to the measured circuit, due to their input capacitance. On the other hand, Figure 5. 4(b) shows current probes add series inductance to the switching loop [141].

**Figure 5. 4.**

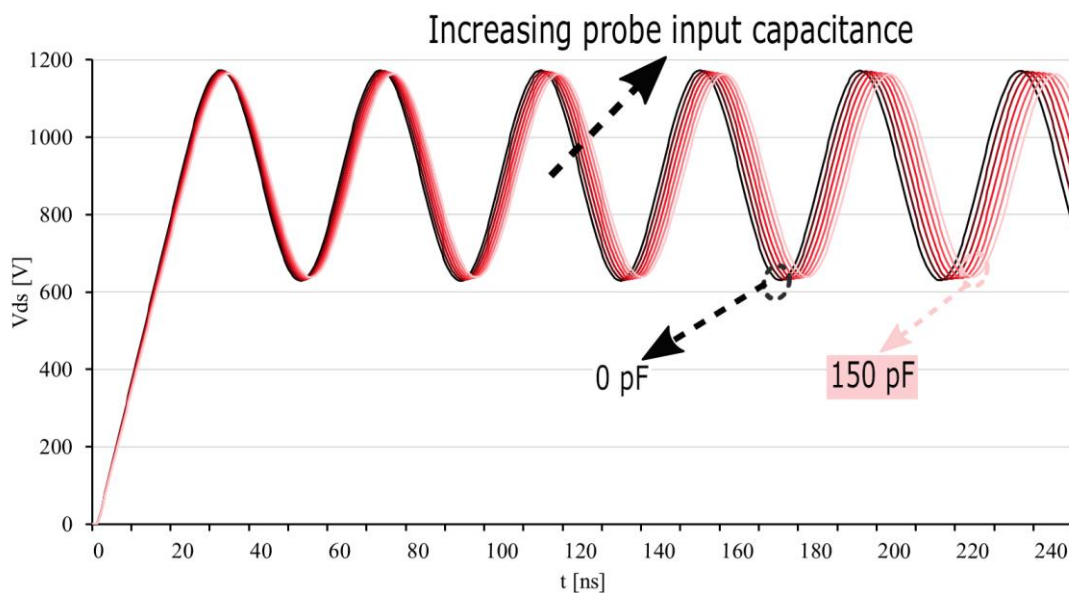
Perturbation in the measured circuit due to the introduction of (a) voltage and (b) current probes.

The perturbations to the circuit already change the original signal, as shown in Figure 5. 5. The original signal is distorted by the sole installation of the measurement circuit due to the perturbation, so the signal entering the voltage or current probe already carries an error. In addition, the probe itself will further distort the original signal, due to the bandwidth limits for example, adding more error to the measured signal. All this phenomenon have low pass filtering effect, attenuating the original signal as shown in Figure 5. 5 [142].



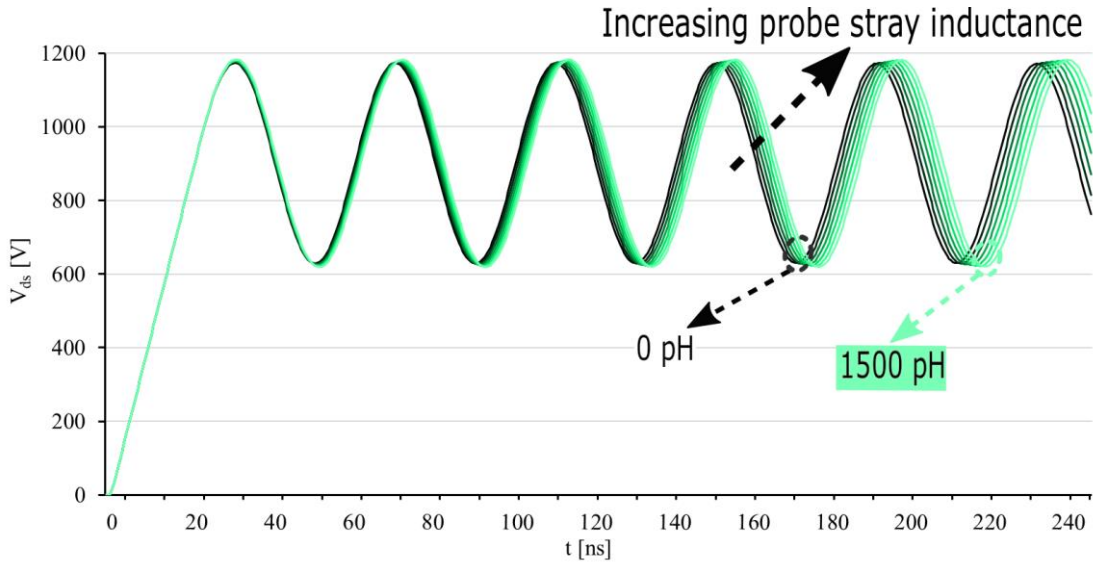
**Figure 5. 5.**  
Distortion of the original signal due to the measurement system.

The effect of the input capacitance of the voltage probe on the  $V_{ds}$  measurement is simulated and shown in Figure 5. 6. The selected SiC module is the FF6MR12KM1, and the input capacitance of the probe is increased from 0 pF until 150 pF. It can be seen the original  $V_{ds}$  (in black) is attenuated, and a delay introduced. This error can affect the switching loss calculation for example, due to the incorrect rise time calculation. In addition, the effect in the SiC module is demonstrated even with small pF input capacitance.



**Figure 5. 6.**  
Simulated effect of the input capacitance of the voltage probe when measuring the  $V_{ds}$  of a FF6MR12KM1 SiC module.

Next, the effect of the stray inductance of the current probe in the  $V_{ds}$  of a FF6MR12KM1 SiC module is simulated, Figure 5. 7. The inductance is increased from 0 to 1500 pH. This time, and due to the added inductance, the signal peak value is increased, see Section 5.2, and a delay is introduced in the measurement. The error can again lead to an incorrect switching loss calculation for example.

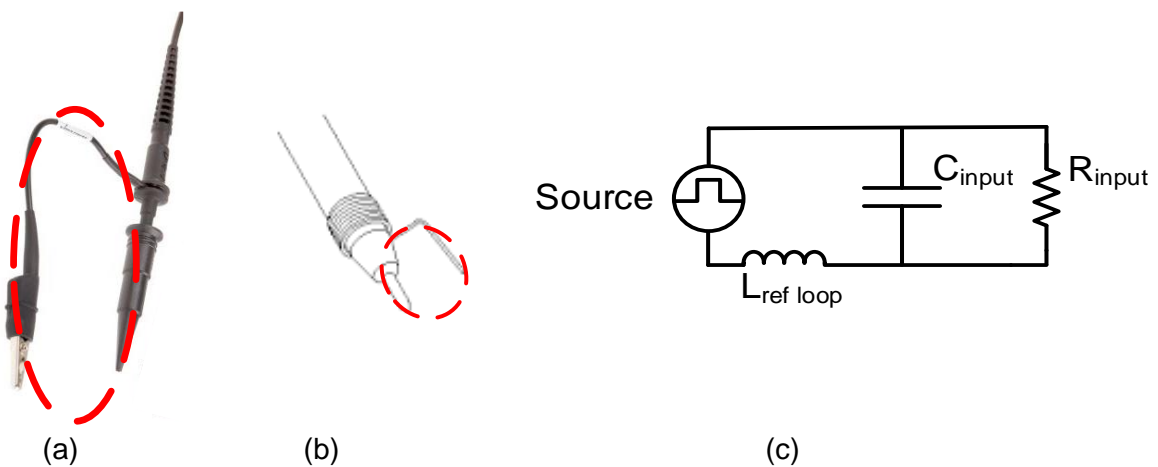


**Figure 5. 7.** Simulated effect of the stray inductance of the current probe when measuring the  $V_{ds}$  of a FF6MR12KM1 SiC module.

**5.4.2.2. Referencing connection loop**

A reference is always connected when using a voltage probe. This connection creates a loop with the positive terminal, shown in Figure 5. 8. The reference loop inductance needs to be minimized when designing the measurement system, in order to avoid resonances in the LC tank created by the reference loop inductance and the input capacitance of the probe [143]. Figure 5. 8 shows two different referencing connections, (a) with a large referencing loop inductance due to the alligator clips and (b) a smaller reference loop inductance with the spring clip. Figure 5. 8(c) shows the equivalent circuit of the voltage probe, considering the reference loop.

As seen in the previous sections, adding extra inductance in the reference loop can alter the original signal, leading to an error in the measurement. The most sensible measurement to this effect in the application of high power SiC modules is the gate circuit. This is because the added inductance can already be superior to the one in the gate driver PCB, totally altering the original circuit.

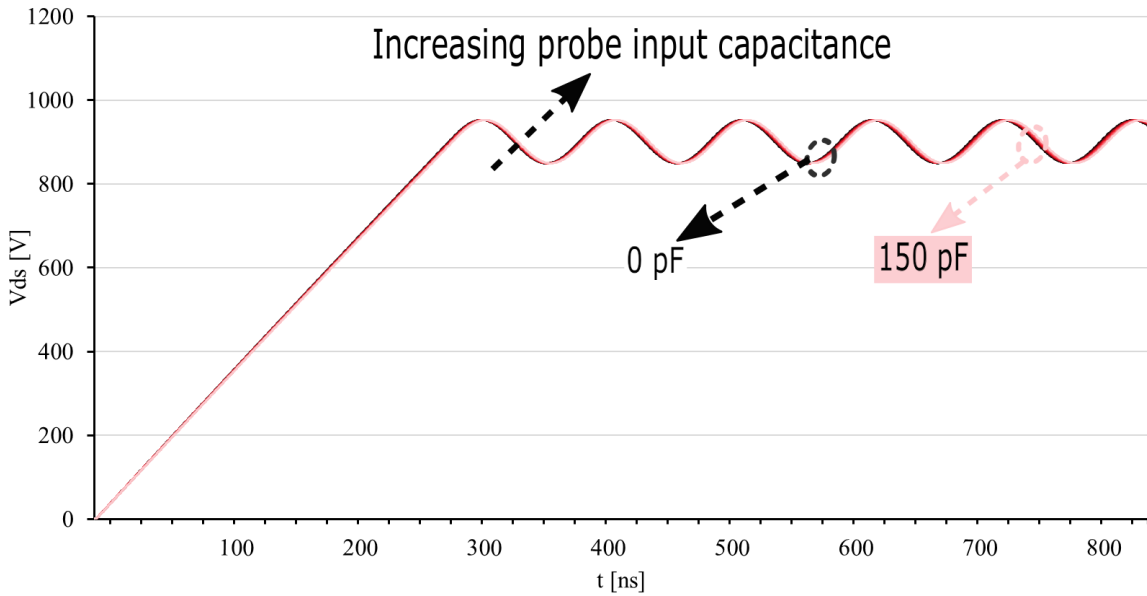


**Figure 5. 8.** Perturbation in the measured circuit due to the reference connection loop, (a) alligator clip with large inductance, (b) spring clip with low inductance and (c) the equivalent circuit of a voltage probe considering the reference connection loop.

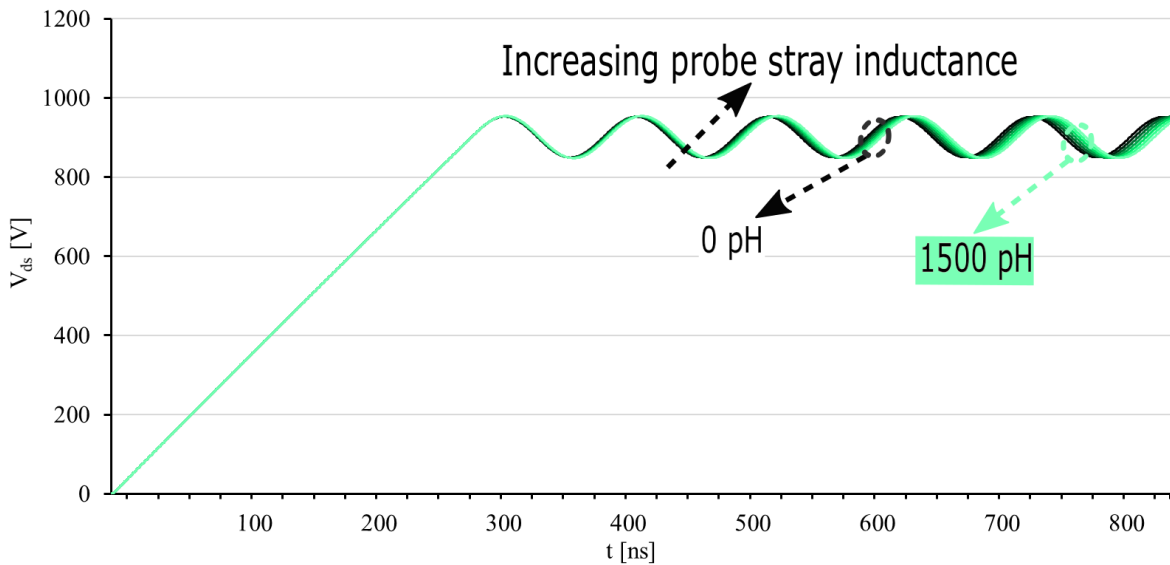


**5.4.2.3. Comparison with silicon**

Due to the lower switching speeds of Si IGBTs, the effect of these circuit perturbations are much lower. Figure 5. 9 and Figure 5. 10 simulate the effect of the voltage and current probes in the FF200R12KT4 Si IGBT module. The perturbation, even if existent, is much lower than the one shown with the FF6MR12KM1 SiC MOSFET analyzed in the previous section.



**Figure 5. 9.** Simulated effect of the input capacitance of the voltage probe when measuring the Vce of a FF200R12KT4 Si IGBT module.



**Figure 5. 10.** Simulated effect of the stray inductance of the current probe when measuring the Vce of a FF200R12KT4 Si IGBT module.

### 5.4.3. Voltage and current alignment

Each voltage and current probe has its own propagation delay characteristic. This means it is very likely to have a timing misalignment between the voltage and current probe in the measurement circuit. The alignment error leads to a miscalculation of the switching losses. Due to the fast dynamics of SiC devices, even a few nanoseconds error can lead to a severe switching loss calculation error [144].

The timing and alignment of the voltage and current probes should be tested before a DPT is performed with SiC. The next section presents the most common and effective alignment techniques.

#### 5.4.3.1. De-skew techniques

The voltage and current alignment is called the de-skew. [143] presents the most common and used techniques. The first one is the self alignment fixture, present in some probes. Even the accuracy is most of the times acceptable, not all the probes are provided with this fixture, so it is not a totally reliable technique.

The second technique is based on the visual inspection. A switching waveform is captured, with high precision, and the voltage and current signals are overlapped. The timing is then adapted manually to match the propagation delays. The execution of this technique is easy and is not time consuming, but its accuracy is very poor. This technique can be acceptable if the switching times of the device are not extremely fast, as in the case of the SiC high power modules, usually switching at tens of nanoseconds. However, if the system is based on discrete components, with just nanoseconds of rise and fall time, this technique is insufficient.

The resistive DPT is a good option for high power SiC modules, if better de-skew is required. This technique is based on the DPT concept, but with a resistive load instead of an inductor. A high resistance (hundreds of ohms) is used, with the lowest possible stray inductance. This ensures the voltage and the current in the switching should be perfectly aligned. This allows a much easier identification of the misalignment, and posterior de-skew. The key factor in this technique is that the resistor should have as low stray inductance as possible, in order to have the highest resistive behavior in the system. In addition, the setup suffers perturbations, so those effects should be minimized.

The final technique is based on the voltage drop in the  $V_{ds}$  of the device during the turn on, due to the stray inductance of the switching loop. This voltage drop can be captured with a high bandwidth voltage probe and high resolution in the oscilloscope. In addition, the same voltage drop can also be calculated with (87).

$$V_{drop} = L_{stray} \frac{di_d}{dt} \quad (87)$$

Capturing several switching waveforms, and calculating the  $di/dt$  point by point by post processing the current measurement data, the  $L_{stray}$  of the circuit can be calculated. Next, the evolution of  $V_{drop}$  is recalculated using (87) and the current measurement data. The voltage drop measured with the voltage probe and the calculated one with the current data and expression (87) should be perfectly aligned, performing a high precision de-skew [145]. This is a high accuracy de-skew technique, but requires several switching waveform data to check the consistency. However, does not require any setup perturbation, so it is relatively easy and fast to perform [143]. If the oscilloscope does not provide additional advanced scope match functions, the data should be post processed with a software such

as MatLab. This technique is especially interesting to use with discrete components or even surface mounted devices such as GaN switches, in which the loop inductances are very small. Any circuit perturbation to introduce a resistor would alter the measurement too much, so the voltage drop evaluation technique is recommended in this case.

#### 5.4.4. Alternative measurement techniques

Regarding the challenges of measuring correctly the waveforms of fast devices, or some of the times the economic cost of the correct equipment, some other techniques have been presented in the literature. Section 5.4.4.1 presents a simple and affordable method to measure the waveforms of the fast SiC devices [139]. However, if the waveforms are not necessary, and the only required information are the switching losses, a methodology to measure them without any waveform acquisition is presented in Section 5.4.4.2.

##### 5.4.4.1. RC attenuator

In [139] a method to measure fast transients with passive probes is presented, as shown in Figure 5. 11. This significantly reduces the cost of the measurement system, as shown in Table LIV. However, the need to attenuate the voltage signal is identified. Using a purely resistive network would present a bad frequency response, so a resistive-capacitive voltage attenuator is proposed to improve the frequency response. [139] shows every design step of the RC network, following three main criteria:

1. High enough bandwidth.
2. Required attenuation to satisfy the passive probe dynamic voltage range.
3. Low equivalent capacitance and high equivalent resistance.

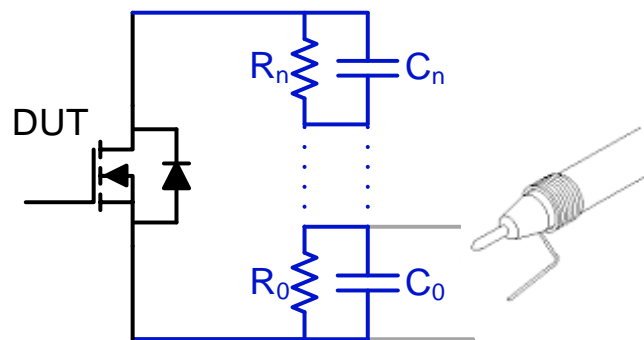


Figure 5. 11.

Proposed RC divider for the use of passive probes [139].

##### 5.4.4.2. Calorimetric measurements

The DPT may be inaccurate to calculate the switching losses of the novel fast switching devices, mostly in soft switching applications [146], due to the errors in the measurements. Calorimetric measurements are considered a better option, because they are based on the temperature increment in the converter to estimate the power losses, without the need to perform fast voltage and current measurements. Although these tests take longer time, because steady state temperatures need to be measured, the precision is better, and they eliminate the need to de-skew the voltage and current probes [146].

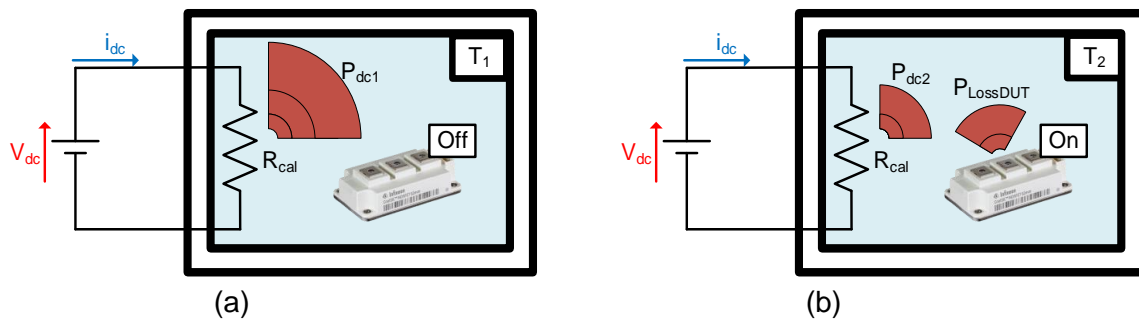
[147] presents and analyzes three methods to perform calorimetric measurements in power converters. The first is based on the temperature difference of the heatsink. The second measures the air flow temperature difference. The third, which is the least accurate and not recommended, measures the increase of the enthalpy of the air flow.

A hybrid electric and calorimetric method is presented in [148], and shown in two stages in Figure 5. 12. The device under test (DUT) is closed in a thermally isolated chamber. First, the chamber is heated with a DC resistor, up to  $T_1$ , with the DUT off, with the power dissipated in the resistor the only heat source. The  $P_{dc1}$  is easily measured in the input of the chamber, using simple DC measurements Figure 5. 12(a).

Next, the device is turned on, so the  $P_{DUT2}$  is added to the resistor power as a heat source. The temperature of the chamber increases, Figure 5. 12(b). The DC power is slowly decreased until the temperature of the chamber is matched with the previous one, being  $T_1 = T_2$ . The DC power is measured again, and it is concluded the power losses in the DUT are the DC power difference (88). The DUT is operated at several switching frequencies to decouple switching and conduction losses. In addition, there is no need to know any thermal characteristic of the module with this technique, and the temperature measurement of the chamber can be done easily.

$$P_{lossDUT} = P_{dc1} - P_{dc2} \quad (88)$$

This method assumes no losses in the system, such as in stray capacitances inductances of PCB tracks [147], so a correct estimation of the switching losses is hard to perform. In fact, the accounted losses are the total losses in the system, not only the ones in the DUT. However, there is no need for fast and complex electrical measurements, so de-skew errors, as well as circuit perturbations are avoided. This is why the hybrid calorimetric technique is considered a good option for very fast discrete SiC devices, or the even faster GaN devices.



**Figure 5. 12.**

The hybrid electric and calorimetric power loss calculation system, (a) first stage with the DUT off, and (b) second stage with the DUT on.

Currently, with the evaluated dynamics in the high power SiC modules, the need to introduce calorimetric measurements is not mandatory. However, with the evolution of SiC modules, faster dynamics might show the need to avoid voltage and current measurements for switching loss calculation, so investing in an isothermal chamber might be interesting for the near future of high power engineers.

## 5.5. Conclusion

This chapter shows several challenges brought by SiC high power modules. Irrelevant issues for high power engineers with Si IGBTs become a key factor in new designs with SiC. Extra care should be taken when switching from Si to SiC modules, and as shown in this chapter, the one to one replacement can lead to a failure. This is why revisiting the already existing designs, and optimizing them for the use of SiC is mandatory for industry

seeking the extra features of SiC devices.

The first challenge to overcome is the false turn on phenomenon. It can be a destructive one, and it limits the switching speed of SiC high power modules. A proper driver design, carefully monitoring the switching characteristics such as the  $dV_{ds}/dt$  is a must. Selecting drivers that allow to turn off the SiC modules with a negative gate voltage is also a recommended prevention technique

Next the overshoot is analyzed. It is also a destructive phenomenon, that can lead to the breakdown of the modules. The overvoltage will limit the high speed switching of the SiC modules if it is not addressed in the design stages. A correct and careful layout and power loop design is key to be able to switch at high  $di/dt$ . The phenomenon is widely analyzed and the main design rules for high power busbars which have been applied in this work in Section 3.3 are presented.

Another important feature in the designs with high power SiC modules is the overcurrent protection. As seen in the literature, it is important for high power modules and has been widely discussed. However, the techniques used with Si need to be adapted in order to avoid issues with the fast switching dynamics of SiC modules. The prevention of false overcurrent detection is a major challenge, making the detection circuit immune to noise. General design recommendations are given in Section 5.3.4, being the most important one the careful selection of the Desat diode  $D_{desat}$  to minimize its junction capacitance  $C_j$ . Installing several diodes in series to increment the blocking voltage capability and reduce the  $C_j$  at the same time is considered favorable. Careful Desat detection voltage threshold  $V_{th}$  selection, as well as considering appropriate Desat times is important when switching high voltage, because long rise times can also falsely trigger the overcurrent protection.

Finally, the challenge of measuring the fast voltage and current transients is presented. This is not problematic with high power Si IGBTs, but can be very challenging with high power SiC modules. The importance of a careful equipment selection and set up design is highlighted. Guidance is provided regarding the voltage and current probe requirements for each system. In addition, the effect of the introduction of measurement equipment is also presented. Correct voltage and current alignment techniques are shown, highlighting the advantages and disadvantages of each one. Finally, the option to consider alternative measurement techniques is introduced, if failing to capture correct waveforms. The calorimetric power loss measurement, and specially the hybrid calorimetric measurement is also introduced, even if it might not be necessary to implement with actual high power SiC modules dynamics.

There is several future work that should be done regarding the challenges of high power SiC modules. For example, the simple modelling of the false turn on phenomenon in high power modules would help engineers to predict this phenomenon, and work with the SiC high power modules in their safe switching speed limit.

Even if the overshoot is well modeled, the coupled effect with the false turn on phenomenon should be analyzed in the future, working with a maximum allowable  $L_{stray}$  in the switching loop as a parameter in the false turn on models. Combining both phenomenon prediction models will determine a safe operation area (SOA) definition methodology for high power SiC modules.

The existing switching models for SiC devices are of high complexity and time consuming. An extremely detailed modelling is necessary when using fast discrete SiC devices, but might be unnecessary with slower high power modules. Investigating the fidelity of simplified switching models is of high interest. By doing so, a simple, fast and reliable methodology to predict the SOA of a certain module and application can be designed. This would help high power engineers to transition safely from Si IGBTs to high power SiC modules, and get the

most benefits out of this technology.

CHAPTER 6

# **Conclusion and future work**

## 6. Conclusion and future work

This last chapter presents the main conclusions of this research project. In addition, the future research lines related to this conclusions are also presented.

### 6.1. Conclusion

Renewable energies are taking over the conventional energy sources, mostly for electricity generation. Solar PV and wind energy specially, are rapidly increasing their production worldwide. Introducing the generated solar and wind power to the grid is a challenge, and power electronics is the enabling technology for this task.

SiC semiconductors offer better technical characteristics than their Si counterparts. High power SiC MOSFETs for example, can be used in applications in which Si IGBTs are commonly used, due to their similar blocking voltage and current ratings. These enhanced technical features include faster switching characteristics, reducing the switching losses. In this context, several high power modules are already available in the market. While some manufacturers are opting to keep the same Si packages for SiC, others are developing their specific packages.

There are already different industrial applications for high power SiC modules, such as distribution grid applications, the electric vehicle, railway traction, aerospace and renewable energies. For this last application, the LCoE is the main techno-economical indicator to evaluate the competitiveness of a certain configuration. It is remarkable that renewable energies are already improving the LCoE of traditional energy sources in the last years, due to their technological advances.

High power SiC semiconductors should be considered to improve the LCoE of wind energy systems due to their voltage and current rating and improved technical characteristics when compared to the same rating Si IGBTs. However, after analyzing wind energy configurations with SiC semiconductors in the designed LCoE calculation tool, it is concluded they are not capable of improving the LCoE of the current system due to their high cost, and if a one to one replacement is applied. Still, if the switching frequency is increased to 10 kHz, configurations with SiC become competitive, improving the LCoE of the current solution 0.04 €/kWh. In addition, the expected cost reduction of SiC MOSFETs will further benefit these configurations. The most promising topology for the introduction of the SiC is the 2L, because of its simplicity and low component count. The 3L topology with SiC is penalized by the high cost due to the high component count, needing a 20 % cost reduction of the SiC semiconductors to improve the LCoE of the 2L configuration with SiC.

The LCoCE should be analyzed instead of the LCoE to validate the LCoE calculation tool results with the laboratory prototype, because only the converter cost data is available for the experimental platform. The implemented laboratory prototypes validates the conclusions obtained by the LCoE calculation tool:

1. Increasing the switching frequency is beneficial for SiC configurations.
2. The 2L topology is the most promising one for the introduction of SiC.
3. A reduction of the cost of SiC semiconductors will further improve their LCoE.
4. The whole system should be redesigned and optimized for the use of SiC, in order to obtain the maximum benefit out of the high power SiC modules.

The laboratory prototypes also show that the good switching characteristics of SiC overcomes the high switching loss penalty of the 2L configuration with Si. This is why high



efficiency, up to 98.88 % can be achieved at the increased switching frequency of 10 kHz with SiC, even with the simple 2L topology.

However, some challenges arise when designing high power converters with SiC. There are several phenomenon that are not relevant with Si IGBTs, but should carefully be studied when redesigning the systems with SiC. The most important ones are the false turn on and the overshoot, which can both be destructive.

In this context, a proper switching characteristic definition is mandatory to prevent the false turn on. In addition, selecting drivers that allow to turn off the SiC device with negative voltage is also recommended. On the other hand, the layout of the converter and the design of the busbar is key to prevent the overshoot. Paralleling components, and using magnetic cancelation techniques reduces the stray inductance of the switching loop, preventing the overshoot issues. An optimized layout and busbar design are mandatory to switch SiC high power modules safely.

The 3L prototype with SiC validates the specific busbar design techniques, achieving 22 nH and 44 nH inductance in the short and long loop respectively. In addition, the inductance reduction is confirmed by measuring it with an impedance analyzer and by switching waveform analysis. The results acquired with both techniques match for the short loop, validating the optimized busbar design for the 3L converter and the overshoot prevention techniques to operated high power SiC modules at high switching speeds. The long loop measurements differ more from the switching analysis due to the need to bypass the modules for the measurements.

The achieved maximum  $di/dt$  is 8.86 A/ns in the short loop. The maximum measured  $V_{ds}$  voltage is 790 V while switching the maximum current, proving safe switching operation in the short loop. The fastest  $di/dt$  in the case of the long loop is 7.73 A/ns. The maximum measured  $V_{ds}$  voltage is 1102 V while switching the maximum current. The rise times are 40 ns for both loops. It is concluded that the 1200 V 250 A modules are switched in fast but safe conditions, not suffering any overvoltage in the turn off in neither switching loop.

Regarding SiC modules protection, the overcurrent detection circuit design is important and should also be redesigned specifically for the SiC. Fast dynamics make the overcurrent detection circuit susceptible to false overcurrent detections. To avoid this issue, reducing the junction capacitance of the Desat diode is key. The threshold detection voltage and the timing should also be redesigned and carefully selected. It is seen both high  $dV_{ds}/dt$  and longer times during the switching penalize the noise immunity of the overcurrent detection circuits. This is why this circuit should be carefully designed for high power SiC modules, which operate at the worst case scenario.

To finish off, it is seen performing reliable voltage and current measurements is more complex with SiC than with Si, due to the fast voltage and current dynamics. Voltage and current probes should satisfy absolute rating values, but also bandwidth requirements. In addition, introducing measurement equipment distorts the measured circuit, perturbing the original signal. Acceptable circuit alterations with Si become unacceptable with SiC due to the high induced error. Besides, the timing misalignment between voltage and current probes can affect severely the switching loss calculation in high power SiC modules. While a few nanoseconds are not relevant in the slow Si IGBTs, they represent a large percentage of the switching time of high power SiC modules. This is why de-skew techniques should be applied before any switching loss evaluation is done using the DPT. Finally, if the measurement system is too complex or becomes too expensive, the hybrid calorimetric power loss measurement can be used to eliminate measurement issues and calculate the switching losses correctly.

This work contributes by analyzing the impact of high power SiC modules in the LCoE of wind energy, both theoretically and experimentally. Not only technical aspects are considered, but economical data is also used to perform the analysis. The conclusions provide a clear roadmap to the industry regarding the introduction of high power SiC modules in their products.

In addition, this work also presents the main technical challenges the industry will face when introducing SiC modules in their designs. A general overview of the possible technical issues as well as indications on how to solve them are given. These recommendations are supported by a reference design for industry, which can be used as a guide to optimize the future products, fully using the enhanced switching characteristics of high power SiC modules.

## 6.2. Future research lines

After analyzing the impact of SiC devices in wind energy, other applications should also be considered. The LCoCE indicator can be extended to other applications, such as the electric vehicle, railway traction, or solar PV for example. By considering the specific needs of each application, and using the specific consumption profiles, the LCoCE of the application with Si and SiC could be calculated.

In addition, and after analyzing several different applications, those which are benefited the most could be classified. The definition of general rules to identify applications that will take the most advantage of high power SiC semiconductors, based on the techno-economical indicator LCoCE could be very helpful for companies making the transition to SiC.

The final research regarding the applications could be to analyze if specific details benefit more Si and others SiC, for the same applications. Analyzing the electric bus application for example, urban buses could benefit more from SiC than long distance buses, or the opposite, due to their different power consumption profile. Knowing this can make companies offer a SiC or a Si product for the same application, but after analyzing and considering the specific consumption profile with their client.

Regarding the SiC high power modules themselves, to define a simple and fast methodology to predict the safe operation area (SOA) of SiC high power modules is important. The actual switching models are focused on very fast discrete components, and are extremely complex and time consuming. To evaluate the fidelity of simpler switching models for high power SiC modules could save time and improve their use in the industry.

In addition, combining false turn on models with overshoot models will help to define the SOA of SiC high power modules. Additionally, there is a need to create simple and safe tests to feed the switching models. The methodology should consist on the following steps:

1. Define the equations.
2. Perform simple and safe tests to the system to feed the parameters in the equations.
3. Solve the equations and calculate the  $dV/dt$  limits for the system and application.

The definition of a simple SOA prediction methodology will allow high power engineers to develop safe designs with SiC in a fast way, but still using the full potential of their fast switching characteristics.

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