

DOCTORAL THESIS

HIGH POWER DENSITY DC-DC CONVERTER FOR MORE ELECTRIC AIRCRAFT



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High-Power Density DC-DC Converter for More Electric Aircraft

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Abstract

Nowadays, the large dependency of the current society of the non-renewable energies is encouraging the acceleration of the climatic change, which is having a considerable impact on the environment. Consequently, an impulse of the renewable energy consumption (photovoltaic, eolic, tidal, etc.) is being produced. This fact does not only affect to the main forms of electric power generation, but also has an impact on the main users of non-renewable energies. In this context, the automotive sector is one of the principals affected, in which the traditional propulsion method based on fossil fuels is being replaced by partially or totally electric thrust vehicles.

Since H2020 started, two new concepts regarding the aeronautic transport where launched: More Electric Aircraft (MEA) and All Electric Aircraft (AEA). In this kind of aircrafts, the Electric Power Distribution System (EPDS) is divided into AC/DC and DC/DC energy conversion. In this work, the DC/DC EPDS proposed for the electric aircraft are analyzed in detail, aiming to deepen into the knowledge of the most employed Power Electronic Converter (PEC) topologies.

In these EPDS, the most utilized PEC according to literature proposals is the Dual-Active-Bridge (DAB) converter. This PEC is formed by two full bridges, interconnected by a power transformer, which can act as inverter and/or rectifier, giving bidirectionality to the system power transfer. As an alternative to DAB converter, Active-Bridge-Active-Clamp (ABAC) has been also proposed, whose primary side is identical to DAB. However, low-voltage side is modified by dividing the full bridge into two half-bridges to include clamp capacitors and output filter DC inductors.

To evaluate the scenarios that encourage the utilization of these topologies, the analytical models that describe the voltage and current behavior of the components that are included in these converters are developed in this work. Furthermore, the operating regions while working with the main modulation methods are presented. Once the analytical models are obtained, a brute force-based optimization algorithm is developed that allows to analyze the utilization of different semiconductor, heatsink, magnetic devices and/or capacitor technologies. Then, the evaluation of the impact of these component technologies on the efficiency and volumetric power density of the converter is performed.

Laburpena

Gaur egun, gizarteak energia ez berriztagarrien kontsumoarekiko duen mendekotasun handiak lagunduta, klima aldaketa bizkortzen ari da, ekosisteman gero eta inpaktu handiagoa edukita. Horren ondorioz, energia berriztagarrien kontsumoa bultzatzen ari da (fotovoltaikoa, eolikoa, mareen energia, etab.). Gertaera horrek energia elektrikoa sortzeko modu nagusiei eragiteaz gain, energia ez berriztagarrien erabiltzaile nagusiei eragiten die. Testuinguru horretan, automobilgintza sektorea da kaltetu nagusietako bat, non erregai fosiletan oinarritutako propultsio metodo tradizionala energia elektrikoaren bidez erabat edo partzialki bultzatutako ibilgailuekin ordezten ari den.

H2020aren hasieratik, garraio aeronautikoaren bi kontzeptu berri kaleratu ziren: hegazkinik elektrikoena (ingelesetik More Electric Aircraft, MEA) eta hegazkin elektriko hutsa (ingelesetik, All Electric Aircraft). Aireontzi mota horietan, potentzia elektrikoa banatzeko sistema AC/DC eta DC/DC energia bihurtzean banatzen da. Lan honetan, hegazkin elektrikorako integratutako eta/edo proposatutako DC/DC banaketa sareak aztertzen dira, normalean enplegatzen diren potentzia bihurgailu elektronikoen topologien ezagutzan sakontzeko.

Banaketa sare horien barruan, DAB da (ingelesetik Dual-Active-Bridge) literaturaren proposamenen arabera gehien erabiltzen den potentzia bihurgailu elektronikoa. Bihurgailu hori bi zubi osok osatzen dute, potentzia transformadore batek interkonektatuta. Zubi horiek, berriz, artezle eta/edo inbertsore gisa jardun dezakete, energia elektrikoaren fluxua noranzko bikoa izatea ahalbidetuta. ABAC da (ingelesetik: Active-Bridge-Active-Clamp) DC/DC banaketa sareetan ere erabiltzen den bihurgailuaren beste alternatiba bat. Bihurgailu horren goi tentsioko aldea DABren berdina da. Hala ere, behe tentsioko aldean zubi osoa bi zubi erditan banatzen da, tarteko bus batean bi kondentsadore eta irteera iragazkiko bi DC induktore sartzeko.

Topologia baten edo bestearen erabilera errazten duten agertokiak ebaluatu ahal izateko, lan honetan bihurgailu horietan sartzen diren osagaien korronteko eta tentsioko portaera deskribatzen duten ekuazio analitikoak garatzen dira, bai eta modulazio metodo nagusiekin lan egiten denean horiek dituzten funtzionatzeko moduak ere. Tentsio eta korronteen ekuazio analitikoak topologia bakoitzean integratzen diren elementuetan lortu ondoren, optimizazio algoritmo bat egiten da, indar gordinean oinarrituta. Algoritmo horrekin, erdieroalearen, disipadorearen, elementu magnetikoen eta/edo kondentsadoreen hainbat teknologiaren erabilera aztertu daiteke, bihurgailuaren efizientzian nahiz haren potentzia bolumetrikoaren dentsitatean duten eragina ebaluatzeko.

Resumen

En la actualidad, la alta dependencia de la sociedad del consumo de energías no renovables esta favoreciendo la aceleración de un cambio climático que tiene cada vez más impacto en el ecosistema. Como consecuencia, se está produciendo un impulso del consumo de energías renovables (fotovoltaica, eólica, mareomotriz, etc). Este hecho no solo afecta a las principales formas de generación de la energía eléctrica, sino que también repercute en los principales usuarios de energías no renovables. En este contexto, el sector automovilístico es uno de los principales afectados, donde el tradicional método de propulsión basado en combustibles fósiles está siendo reemplazado por vehículos impulsados total o parcialmente mediante energía eléctrica.

Desde el comienzo del H2020, dos nuevos conceptos de transporte aeronáutico fueron lanzados: el avión más eléctrico (del inglés, More Electric Aircraft-MEA), y el avión puramente eléctrico (del inglés, All Electric Aircraft-AEA). En este tipo de aeronaves, el sistema de distribución de potencia eléctrica se divide en conversión de energía AC/DC y DC/DC. En este trabajo, se analizan las redes de distribución DC/DC integradas y/o propuestas para el avión eléctrico con el objetivo de profundizar en el conocimiento de las topologías de convertidores electrónicos de potencia comunmente empleados.

Dentro de estas redes distribución, el convertidor electrónico de potencia más empleado de acuerdo con las propuestas de la literatura es el DAB (del inglés Dual-Active-Bridge). Este convertidor está formado por dos puentes completos, interconectados por un transformador de potencia, que pueden actuar de rectificador y/o inversor, otorgando bidireccionalidad al flujo de energía eléctrica. Otra alternativa de convertidor también empleado en redes de distribución DC/DC es el ABAC (del inglés Active-Bridge-Active-Clamp), cuyo lado de alta tensión es idéntico al DAB. Sin embargo, en el lado de baja tensión el puente completo se divide en dos medios puentes para incluir dos condensadores en un bus intermedio y dos inductores de DC de filtro de salida.

Para poder evaluar los escenarios que favorecen la utilización de una topología u otra, en este trabajo se desarrollan las ecuaciones analíticas que describen el comportamiento en corriente y tensión de los componentes que se incluyen en estos convertidores, así como los modos de funcionamiento de estos cuando se trabaja con los principales métodos de modulación. Una vez obtenidas las ecuaciones analíticas de tensiones y corrientes en los diferentes elementos que se integran en cada topología, se realiza un algoritmo de optimización basado en fuerza bruta que permite analizar la utilización de distintas tecnologías de semiconductor, disipador, elementos magnéticos y/o condensadores para evaluar el impacto que estas tienen tanto en la eficiencia del convertidor como en la densidad de potencia volumétrica del mismo.

List of Publications

Journal

A) Alejandro Fernandez-Hernandez, Fernando Gonzalez-Hernando, Asier Garcia-Bediaga, Irma Villar, Gonzalo Abad, "Design Space Analysis of Dual-Active-Bridge Converter for More Electric Aircraft", submitted to *MDPI Energies*, Sep. 2022.

Conference

- A) Alejandro Fernandez-Hernandez, Asier Garcia-Bediaga, Irma Villar, Gonzalo Abad, "Analytical Equations of the Currents in Dual Active Bridge Converter for More Electric Aircraft", *IEEE Vehicle Power and Propulsion Conference (VPPC)*, 2020, pp. 1-6.
- B) Alejandro Fernandez-Hernandez, Asier Garcia-Bediaga, Irma Villar, Gonzalo Abad, "Analytical Model of the Current Stress in Active-Bridge-Active-Clamp Converter for More Electric Aircraft", *IEEE Energy Conversion Congress and Exposition* (ECCE), 2021, pp. 1785-1792.
- C) Alejandro Fernandez-Hernandez, Asier Garcia-Bediaga, Irma Villar, Gonzalo Abad, "Analysis of Interleaved Input-Parallel Output-Parallel Dual-Active-Bridge Converter for More Electric Aircraft", *IEEE Vehicle Power and Propulsion Conference (VPPC)*, 2021, pp. 1-5.
- D) Alejandro Fernandez Hernandez, Fernando Gonzalez-Hernando, Asier Garcia-Bediaga, Irma Villar, Gonzalo Abad, "Exploration of the η-ρ Pareto Optimization of Bidirectional Isolated DC-DC Power Electronic Converters for More Electric Aircraft", *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022. [AC-CEPTED]

Glossary

Acronyms

Active-Bridge-Active-Clamp
neuro Bridge-neuro-Oramp
Alternative Current
All-Electric Aircraft
Auxiliary Power Unit
Average
Cooling System Performance Index
Constant Voltage/Constant Frequency
Constant Voltage/Variable Frequency
Dual-Active-Bridge
Direct Current
Double Phase Shift
Electromagnetic Interference
Electric Power Distribution Systems
Extended Phase Shift
Energy Storage System
Finite Element Analysis
Figure of Merit
Gallium Nitride
High Voltage Alternative Current
High Voltage Direct Current
Insulated Gate Bipolar Transistor
improved Generalized Steinmetz Equation
Input Parallel Output Parallel
Input Series Output Parallel
Low Voltage Alternative Current
Low Voltage Direct Current
More Electric Aircraft

\mathbf{MFT}	Medium Frequency Transformer
MLCC	Multi-layer Ceramic Capacitors
MOO	Multi-Objective Optimization
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
OTM	Optimal Transition Mode
PCB	Printed Circuit Board
PECs	Power Electronic Converters
\mathbf{PSM}	Phase Shift Modulation
\mathbf{PWL}	Piecewise Linear
\mathbf{PWM}	Pulse Width Modulation
\mathbf{RMS}	Root Mean Square
SiC	Silicon Carbide
SPS	Single-Phase Shift
SRC	Series Resonant Converter
SSB	Solid-State Breaker
\mathbf{TPM}	Trapezoidal Modulation
TPS	Triple Phase Shift
TRM	Triangular Modulation
ZVS	Zero Voltage Switching

Symbols

Variable	Description	Unit
$A_{ m c}$	Core area	mm^2
$A_{\rm p}$	Area product	m^4
$B_{ m m}$	Maximum magnetic flux density	Т
$B_{ m m(Lo)}$	Maximum magnetic flux density in the output induc-	Т
	tor of ABAC converter	
$B_{\rm sat}$	Saturation flux density of a magnetic core	Т
C_{11}	Primary stray capacitance of the power transformer	\mathbf{F}
C_{12}	Primary-secondary stray capacitance of the power	\mathbf{F}
	transformer	
C_{22}	Secondary stray capacitance of the power transformer	F
$C_{ m c}$	Clamp capacitance of ABAC converter	F
$C_{\rm oss}$	Output capacitance	\mathbf{F}
$C_{\rm rss}$	Reverse transfer capacitance	F
$E_{\rm off}$	Turn-off energy	J
$E_{\rm on}$	Turn-on energy	J
$f_{ m sw}$	Switching frequency	kHz
$h_{ m cond}$	Conduction heat transfer coefficient	$W/(m^2K)$
$h_{\rm conv}$	Convection heat transfer coefficient	$W/(m^2K)$
$h_{ m cu1}$	Copper thickness in the primary winding	m
$h_{ m cu2}$	Copper thickness in the secondary winding	m
$h_{ m ins1}$	Primary-to-primary insulation distance	m
$h_{ m ins2}$	Secondary-to-Secondary insulation distance	m
$h_{ m ins12}$	Primary-to-secondary insulation distance	m
$h_{ m rad}$	Radiation heat transfer coefficient	$W/(m^2K)$
$i_{\rm CLV}$	Current that flow through the LVDC capacitor	А
$I_{\rm DS,max}$	Drain-to-source maximum current	А
$I_{\rm Lout1}$	Current through output inductor at primary switch-	А
	ing instant (ABAC)	
$I_{\rm Lout2}$	Current through output inductor at primary switch-	А
	ing instant (ABAC)	
$I_{\rm Lout(AVG)}$	AVG current through output inductor (ABAC)	А
$I_{\rm Lout(max)}$	Maximum current through output inductor (ABAC)	А
$I_{\rm Lout(min)}$	Minimum current through output inductor (ABAC)	А

Variable	Description	Unit
$I_{\rm sw1}$	Current value in the primary winding of power trans-	А
	former at switching instant of primary power devices	
$I_{\rm sw2}$	Current value in the primary winding of power trans-	А
	former at switching instant of secondary power devices	
l	Magnetic path length	mm
$l_{ m g}$	Air gap length	mm
L_{k1}	Leakage inductance in the primary side of a power	Н
	transformer	
L_{k2}	Leakage inductance in the secondary side of a power	Н
	transformer	
L_{M}	Magnetizing inductance	Н
L_{out}	Output inductance (ABAC)	Н
L_{σ}	Decoupling inductance	Н
M	Normalized DC gain $(n V_{\rm LV}/V_{\rm HV})$	V/V
$M_{ m s}$	Number of magnetic sections	-
n	Transformer turns ratio	-
n_1	Number of turns in primary winding	-
n_2	Number of turns in secondary winding	-
$N_{\rm p1}$	Number of PCBs set in parallel in the primary wind-	-
	ing	
N_{p2}	Number of PCBs set in parallel in the secondary wind-	-
	ing	
$N_{\rm p(DAB)}$	Number of parallel converters in IPOP DAB	-
$N_{\rm sw}$	Number of power devices connected in parallel	-
P_{cu}	Copper losses in the power transformer	W
P_{cond}	Conduction losses	W
$P_{ m dt}$	Dead-time losses	W
P_{out}	Output power	W
$P_{\rm sw}$	Switching losses	W
$P_{\rm v}$	Core losses density	W/cm^3
r_{I}	AC/DC current ripple ratio in output inductors	_
	(ABAC)	
$R_{ m AC1}$	Primary AC resistance in a power transformer	Ω
$R_{\rm AC2}$	Secondary AC resistance in a power transformer	Ω
R _{DS,on}	Drain-to-source on resistance	Ω
$(R_{\rm DS,on} C_{\rm oss})^{-1}$	FOM of power devices	Hz
,	-	

Variable	Description	Unit
$R_{ m th,ha}$	Heatsink-to-ambient thermal resistance	C/W
$R_{ m th,jc}$	Junction-to-case thermal resistance	C/W
$r_{ m VHV}$	Distortion factor on HVDC side	-
$r_{ m VLV}$	Distortion factor on LVDC side	-
$t_{ m dt}$	Dead time in power devices	\mathbf{S}
$T_{ m j}$	Junction temperature of the power device	\mathbf{C}
$V_{ m AC}$	AC Voltage	V
$V_{\rm Clamp}$	Voltage on the clamp capacitors of ABAC converter	V
$V_{ m DC}$	DC Voltage	V
$V_{ m DS,max}$	Drain-to-source maximum voltage	V
$V_{ m GS}$	Gate-to-source voltage	V
$V_{\rm HV}$	Voltage level on HVDC side	V
$V_{ m LV}$	Voltage level on LVDC side	V
$V_{\rm SD}$	Free-wheeling voltage drop	V
$W_{\mathbf{a}}$	Window area	mm^2
$\Delta I_{\rm Lout(pk-pk)}$	Peak-to-peak current ripple on output inductor (ABAC)	А
$\Delta V_{\rm HV(pk-pk)}$	Peak-to-peak voltage ripple on HVDC side	V
$\Delta V_{\rm Clamp(pk-pk)}$	Peak-to-peak voltage ripple on the clamp capacitors (ABAC)	V
$\Delta V_{\rm LV(pk-pk)}$	Peak-to-peak voltage ripple on LVDC side	V
Δv	Voltage across the decoupling inductance	V
δ	Phase-shift between primary and secondary voltages of the power transformer	rad
δ_{lim}	Maximum δ allowed due to the design considerations	rad
δ_{max}	Maximum δ due to the decoupling inductance obtained in the design	rad
$\delta_{ m TPM}$	δ modulation angle in TPS-TPM	rad
δ_{TRM}	δ modulation angle in TPS-TRM	rad
$\delta_{\rm max,TPM}$	Maximum δ in TPS-TPM	rad
$\delta_{ m min,TPM}$	Minimum δ in TPS-TPM	rad
$\delta_{ m sd}$	Skin depth	m
η	Efficiency of the converter	%
μ	Permeability of the material	H/m
μ_0	Vacuum permeability	H/m
$\mu_{ m r}$	Relative permeability of a magnetic material	H/m
ρ	Power density of the converter	kW/dm^3

Variable	Description	Unit
$ ho_{\mathbf{w}}$	Electrical resistivity of the windings	$\Omega { m m}$
arphi	Interleave phase shift angle	rad
Ω_1	Phase shift between half-bridge branches of the pri-	rad
	mary side	
Ω_2	Phase shift between half-bridge branches of the sec-	rad
	ondary side	
$\Omega_{1,\mathrm{TPM}}$	Ω_1 in TPS-TPM	rad
$\Omega_{2,\mathrm{TPM}}$	Ω_2 in TPS-TPM	rad

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1

Introduction

Summary:

One of the major concerns of the present society is climate change. Due to this fact, the transport industry is developing electric vehicles that are more efficient and less harmful to the environment than traditional non-renewable fuel consumption-based. Therefore, the aircraft industry is increasing the amount of electrical power installed, where power electronics play an important role in facing upcoming challenges. Then, this chapter presents the state of the art of aircraft Electric Power Distribution Systems (EPDS) and DC/DC Power Electronic Converters (PECs).

1.1 Introduction

Since *Horizon2020* started, the different means of transport have experienced an enormous increase in research and development to reduce their environmental impact and improve the security and comfortability of the passengers. According to the European Commission [1], Fig. 1.1 depicts the greenhouse gas emissions of the principal means of transport. Among them, civil aviation represents 13.1% of the total emitted pollution. This fact makes it the second most polluting vehicle.

The last data available from Eurostat [2] reports an increment in the popularity of aircraft transport, up to the amount of 1,043 million passengers per year. Furthermore, the development of new aircraft vehicles inspires us to believe in an air transport network where more agents are also involved [3]. Flightpath 2050 also contemplates an optimistic future for aerospace transportation, which expects to grow in the following years. This positive growth leads the aircraft industry to develop more secure and high-efficient systems by including more electrical power supplies, which exhibit better performance than classical power distribution networks.

As shown in Fig. 1.2(a), classical aircraft have four power sources [4]: hydraulic, pneumatic, mechanical, and electric. However, it results in worst performance systems due to the high amount of power conversions needed compared to all and hybrid electrical systems, which are more versatile and show to be a more efficient power source. Therefore, the aerospace industry is developing airplanes with higher electrical capabilities. To this aim, More Electric Aircraft (MEA) and All-Electric Aircraft (AEA) concepts arose. However, propulsion thrust stills being convectional in commercial airplanes [5]. AEA is a long-term objective where electric sources are included in a whole electric system, obtaining benefits in terms of efficiency and emissions. However, MEA looks to include more electro-hydraulic, electro-pneumatic and electro-mechanic actuators to substitute

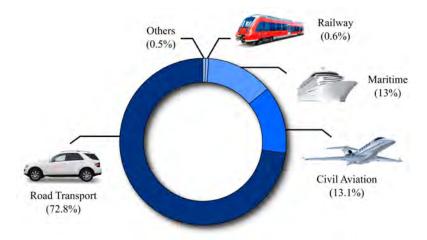


Figure 1.1 Greenhouse gas emissions of different mean of transport.

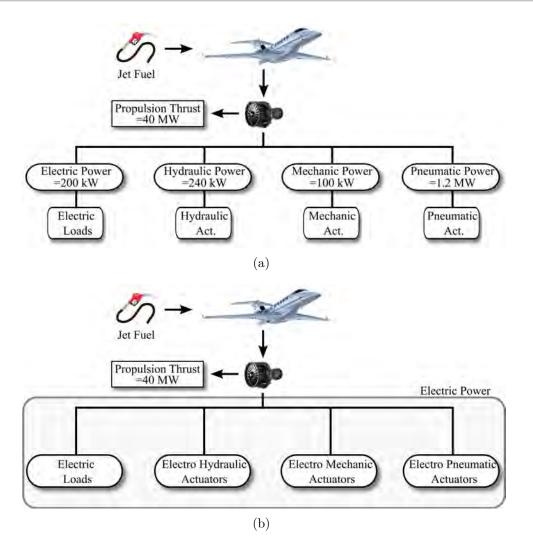


Figure 1.2 Aircraft power distribution: (a) Classical and (b) MEA

conventional hydraulic, pneumatic, or mechanic systems.

Nowadays, we can find aircraft like the Boeing 787 and Airbus A380 in which the increment of electrical power is noticeable. Fig. 1.2(b) shows MEA power distribution, where all the power sources are implemented in an all-electric power network. The increment of aircraft electrical power capability has a positive impact on power electronics developments, which must satisfy all the requirements for every application, such as Energy Storage System (ESS), Wing Ice Protection System (WIPS), and the power supplies of flight-conditioning systems.

In this context, Electric Power Distribution Systems (EPDS) of Direct Current (DC) are acquiring a huge importance. These EPDS are composed of HVDC and LVDC buses interconnected between them and with the different DC loads. Then, bidirectional isolated DC/DC Power Electronic Converters (PECs) are the most common solution to interface HVDC and LVDC distribution networks, especially in ESS and Solid-State Breaker (SSB) applications.

This chapter is structured as follows. Section 1.2 describes in detail different EPDS that are suitable for MEA and AEA concepts, as well as aircraft system requirements. Afterward, section 1.3 presents the state of the art of bidirectional isolated DC/DC PECs and Medium Frequency Transformer (MFT). Then, section 1.4 exposes the motivation and objectives that drive the development of this work. Finally, section 1.5 gathers the structure of the document.

1.2 More Electric Aircraft: EPDS and Requirements

A wide variety of options are available when considering the EPDS for aircraft electrification based on Alternative Current (AC) and DC distribution buses. Among the different alternatives, the distribution buses defined in standards MIL-STD-704F and ISO 1540:2006 for DC/DC power conversion are the objective of this work [6, 7]. Then, this documents aims for application proposals as ESS and power flow regulation between HVDC buses. DC/DC PECs are a hot research topic in aircraft industry to find the best solutions to satisfy MEA specifications, which are focused on high-efficiency and low volume and weight systems, to achieve high-power-density DC/DC converters. Hereafter, EPDS proposed for conventional and future aircrafts are presented [5].

1.2.1 Electric Power Distribution Systems

Fig. 1.3 shows an example of a typical MEA power distribution network, where Constant Voltage/Variable Frequency (CV/VF) 115 V_{AC} bus is directly connected to the electric generators. Then, AC/AC, AC/DC and DC/DC PECs are responsible of the energy conversion to obtain High Voltage (HV) and Low Voltage (LV) AC and DC buses. Moreover,

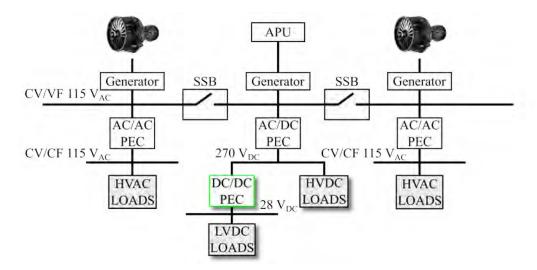


Figure 1.3 Example of EPDS for MEA.

two SSB connects High Voltage Alternative Current (HVAC) buses for fault protection. Also, it is meaningful to think of the aircraft EPDS as an independent grid, in which any variation on AC or DC loads influences the dynamic response of the system.

Considering DC power distribution, 270 $V_{\rm DC}$ is the voltage level established for HVDC bus, while 28 $V_{\rm DC}$ is the present-day choice for LVDC bus. Furthermore, 540 $V_{\rm DC}$ and 128 $V_{\rm DC}$ (when considering ESS application) have been also considered for HVDC and LVDC sides to reduce the current stress on these buses. Nevertheless, the conception of these ideas belongs to a research environment, and its implementation in commercial aircraft is not ready yet. Most of the EPDS presented for MEA are mainly focused on combined AC and DC distribution lines where AC is the leading actor. However, there are many literature proposals since MEA and AEA concepts started [5] - [11]. Moreover, the importance of the DC distribution lies on the reduction of the aircraft weight, as well as the improvement in the performance of the whole system [12]- [14].

Many European projects have proposed multiple EPDS configurations to find diverse solutions for MEA. The first outline comes from More Open Electrical Technologies (MOET) European project. This project studies the best EPDS configuration for MEA, and Fig. 1.4 shows a simplification of the studied EPDS [15]. The two main engines connect to the generators, which supply four HVAC buses. SSB acts as interface between HVAC buses to feed the AC buses when a generator is in failure mode. Then, AC/DC and DC/DC PECs link HVAC, HVDC and LVDC buses to regulate the power transfer. Furthermore, the power flow direction is modified when considering ESS applications as extra security protection. It is essential to note that implementing ESS instead of Auxiliary Power Unit (APU) leads to free-emission aircraft and carries to the utilization of bidirectional isolated PECs, which allow to control both power transfer and power flow direction.

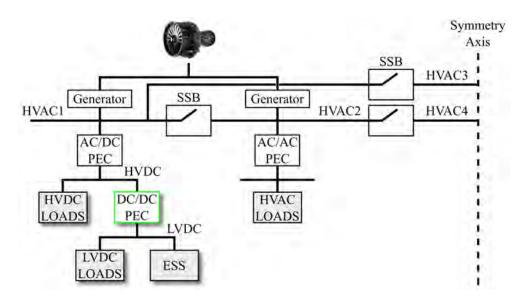


Figure 1.4 Simplification of an EPDS proposed in MOET project.

1. INTRODUCTION

The Integrated, Intelligent Modular Power Electronic Converter (I2MPEC) European project also proposed an EPDS for MEA (see Fig. 1.5), where sources and loads are plugged into matrix contactors [16]. AC/DC and DC/AC PECs play a vital role in this configuration to interconnect AC sources and loads between them and with the DC distribution line. Furthermore, DC/DC PECs are used to interface ESS with the HVDC bus, which makes necessary the utilization of a bidirectional PEC.

The main interest of this EPDS is the modularity achieved, which allows operating when one or more PECs are in failure mode. The utilization of Silicon Carbide (SiC) and Gallium Nitride (GaN) power semiconductors benefits this modular strategy to develop PECs for aircraft EPDS in the I2MPEC project. These technologies enable to improve the power density of the whole system, i.e. higher efficiency with less weight and/or volume. Therefore, the aims of the published research that are result of the I2MPEC project lie in the volume/weight and efficiency analysis of modular PECs as well as the design of power semiconductor modules for MEA applications [17] - [19].

Also, the literature considers Flexible EPDS configurations. In this EPDS, DC/DC power conversion plays the most significant role. As show in Fig. 1.6, DC/DC PECs function is not only focused on the connection of HVDC and LVDC buses. Furthermore, the DC/DC PECs included in this EPDS must interface different buses in case of a failure event of one branch, improving the reliability of the system. Therefore, designers also contemplate ESS even though the system includes an APU.

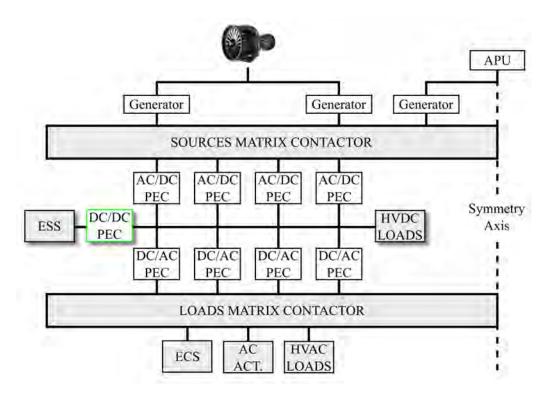


Figure 1.5 Simplification of a modular EPDS proposed in I2MPECT project.

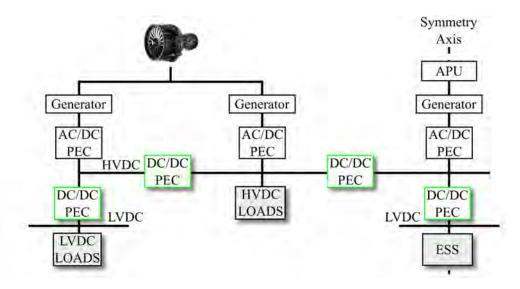


Figure 1.6 Example of flexible EPDS for MEA.

To conclude, this work presents two more DC distributions of the different EPDS configurations for MEA applications. The first one, depicted in Fig. 1.7(a) based on a distributed system where power management is divided in primary and secondary distribution units. On the one hand, ESS connect to primary distribution units through a bidirectional isolated DC/DC PEC. On the other hand, secondary distribution units directly link to the primary power distribution, while a bidirectional isolated DC/DC PEC interface HVDC and LVDC buses inside the secondary distribution units. Secondly, Fig. 1.7(b) illustrates a single bus based EPDS. This configuration consists of a unique 270 $V_{\rm DC}$ distribution line, where HVDC loads hook up, as bidirectional isolated DC/DC PECs to generate multiple LVDC distribution lines. As in previous EPDS, ESS and 28 $V_{\rm DC}$ loads connect to the LVDC side.

This subsection exposes EPDS found in literature for MEA applications, where it is patent an increase of the importance that power electronics takes inside the aircraft. Furthermore, conventional CV/VF and Constant Voltage/Constant Frequency (CV/CF) V_{AC} distribution lines are being replaced by DC-based EPDS. In these EPDS, bidirectional isolated DC/DC PECs allow controlling the power flow direction, which improves the reliability of the system. Therefore, the literature presents numerous research on these converters in the last years, focusing on efficiency, volume and weight when considering MEA. Section 1.3.1 details a comprehensive review of bidirectional isolated DC/DC PECs literature for this application. Before arriving to the bidirectional isolated DC/DC PECs literature review, the next subsection describes the system requirements defined by MEA specifications. Furthermore, the most relevant restrictions when designing the inverter, rectifier or power transformer stages of the DC/DC converters are discussed.

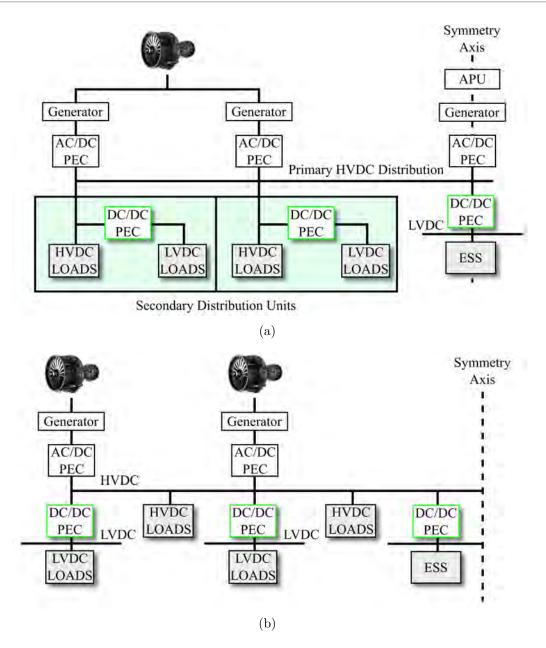


Figure 1.7 DC based EPDS for MEA: (a) Distributed and (b) Single bus.

1.2.2 System Requirements

Power distribution requirements in MEA are established in standard MIL-STD-704F [6]. As presented before, EPDS focus on the following buses: CV/VF and CV/CF for AC distribution, and HVDC and LVDC buses for DC distribution. We find 115/200 $V_{\rm AC}$ power distribution lines depending on the considered aircraft divided in CV/VF or CV/CF. On the one hand, the frequency range of the VF distribution line goes from 360-800 Hz. On the other hand, CF networks work at 400 Hz. Furthermore, AC operation also considers double-voltage 230/400 $V_{\rm AC}$ CF, while DC distribution contemplates two voltage levels, which are 270 $V_{\rm DC}$ and 28 $V_{\rm DC}$ for HVDC and LVDC distributions.

The objective of ISO 1540:2006 is to establish the electrical characteristics that must

be supplied to the utilization equipment [7]. In AC distribution, 26 $V_{\rm AC}$ of CF is described for Low Voltage Alternative Current (LVAC) loads. A wide diversity is available for LVDC distribution buses, which also contemplates the utilization of 14 $V_{\rm DC}$ and 42 $V_{\rm DC}$.

Since bidirectional isolated DC/DC PECs are the objective of this work, Table 1.1 describes the operation limits and distortion factors of the DC buses included in MIL-STD-704F. In the 28 V_{DC} bus, the steady-state voltage lies in the range from 22-29 V when working at normal operation, while 250-280 V is allowed for 270 V_{DC} bus. Furthermore, the maximum permitted distortion factors on HVDC and LVDC sides are 0.015 and 0.035, which corresponds to a peak-to-peak voltage ripples of 6 V and 1.5 V. These requirements have a considerable impact on the bus capacitors, especially in the LVDC side due to the required capacitance to fulfill the standard. Then, the volume and weight of these components are highly determined by the specification and must be studied in detail. Also, the standard impact on the selection of the power devices, since they must withstand the voltage level on HVDC and LVDC sides. Therefore, SiC, GaN and Si technologies can be considered for the HVDC side, while LVDC voltage levels encourage to think on GaN and Si technologies due to the lack of SiC semiconductors at this voltage range.

In addition to the considered specifications that come from the standard, designers must consider the thermal limitations to ensure that the converter works properly in the whole output power range. These limitations are mainly set by the thermal behavior of the switching devices and power transformer, which define the required heatsink. Considering the switching devices, the thermal limit for the analysis included in this work is 80 °C of maximum case temperature. This way, the junction temperature does not overcome the maximum limit of the device. Furthermore, it is fundamental to assure that the temperature on the core of the power transformer does not exceed the Curie temperature, which is close to the 200 °C for most of the ferrite materials utilized in MFT. Therefore, the thermal limit of this component is set to 130 °C, introducing a safety margin of 70 °C.

Parameter	Value	Units
	250-280	V
$V_{\rm LV}$	22-29	V
Dist. Factor $(r_{\rm VHV})$	0.015	-
Dist. Factor $(r_{\rm VLV})$	0.035	-
Peak-to-peak voltage ripple $(\Delta V_{\rm HV(pk-pk)})$	6	V
Peak-to-peak voltage ripple $(\Delta V_{LV(pk-pk)})$	1.5	V

Table 1.1 Normal operation characteristics of DC buses in MIL-STD-704F

1.3 State of the Art

In recent years, power electronics research and development on bidirectional isolated DC/DC PECs for mobility applications have grown up due to the extended popularity of electric means of transport. Therefore, it is possible to find in the literature a wide variety of topology proposals depending on the considered vehicle and the application requirements. In the case of MEA, bidirectionality and isolation are required for ESS and power flow regulation between HVDC and LVDC buses [20]. Then, the most promising bidirectional isolated DC/DC PECs proposed for MEA and a technology review of MFT are detailed in following sections.

1.3.1 Bidirectional Isolated DC/DC PECs in MEA

As previously mentioned, DC/DC applications for MEA are the aim of this work. The literature studies of this area are focused on bidirectional-isolated DC/DC converters, more especially when aiming to interface an ESS with the HVDC. In this context, the Airbus company has developed a buck-boost converter unit (BBCU) through two different projects [21]. The first one is to manufacture a bidirectional-isolated DC/DC PEC to interface ± 270 and 28 $V_{\rm DC}$ buses. Then, the optimization of the converter looks to improve, among others, the industrial production of the PEC.

New wide bandgap semiconductor technologies, i.e. SiC and GaN, have been also studied in detail. A comparison between SiC Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) over Si Insulated Gate Bipolar Transistor (IGBT) in terms of performance and reliability for motor drive application in MEA is addressed in [22]. These technologies have been evaluated for harsh environment applications, analyzing the feasibility and the optimization of the PEC [23, 24]. To this aim, Dual-Active-Bridge (DAB) converter is the selected topology, comparing the benefits and drawbacks of the Triple Phase Shift (TPS)-Trapezoidal Modulation (TPM) and Single-Phase Shift (SPS) Rectangular modulation. Also, DAB converter has been researched with HVDC and LVDC inverter and/or rectifier stages formed by SiC and Si semiconductor technologies in aircraft applications [25]. Furthermore, the evaluation of multiple topologies based on DAB converter is carried out when using wide bandgap semiconductors to analyze which configuration provides higher efficiency and lower volume of the cooling system [26].

Alternatively, the DAB converter has been compared with resonant-based DC/DC converter topologies, as the CLLC Series Resonant Converter (SRC) [27]. This converter topology is composed by a resonant tank connected to the primary and secondary stages of the power transformer, preserving the symmetry of the circuit. The non-symmetrical configuration of the resonant tank has been designed and verified experimentally [28].

The main advantage over DAB is its inherent Zero Voltage Switching (ZVS) behavior in whole working points when the switching frequency of the converter is set above the resonant frequency.

One of the main advantages of the DAB converter is the ease of implementation regarding resonant tank-based power converters when multiport configurations are considered [29, 30]. For these configurations, impedance models and transfer function for multiport DAB converter have been proposed [31, 32]. Moreover, the control algorithm for these kinds of architectures, as well as the optimal design for efficiency versus cost trade-off are presented in [33, 34]. Also, the power flow management of these systems is studied in [35]. These multiport configurations are commonly presented to interconnect DC buses of the same voltage levels, reducing the drawbacks of these architectures.

Nevertheless, the major drawback of DAB is the bulky LVDC capacitor needed to fulfill the voltage ripple requirements set in MEA standards. Therefore, Active-Bridge-Active-Clamp (ABAC) converter has been proposed to solve this issue [36]. In this PEC, the LVDC side configuration is modified to add clamp capacitors and output inductors [37]. Furthermore, the utilization of advanced modulation methods, such as TPS-TPM and TPS-Triangular Modulation (TRM) have been considered in [38, 39]. The main handicap of this topology lies on the high number of passive devices included, which cause current sharing and ripple cancellation issues [40]. Finally, the global picture of bidirectional isolated DC/DC PECs proposed for MEA is gathered in Table 1.2, where the main characteristics of the presented literature proposals are summarized.

1.3.2 Medium Frequency Transformers: Technology Review

In past decades, the contributions to the knowledge of power transformer technology have been focused on MFT, which exhibits lower volume than classical low-frequency transformers. This fact is because the required area product (A_p) of the application is lower as higher is the switching frequency for a considered losses density (P_v) according

Ref.	Topology	Tech.	$V_{\rm in}/V_{\rm out}$ [V]	Rated power [kW]	Freq. [kHz]	Eff. [%]
[21]	BBCU	SiC	540/28	12	100	85
[23]	DAB	SiC	270/28	6.5	40	94
[24]	DAB	SiC	270/28	4	40	96
[25]	DAB	Si	270/28	1	100	90
[26]	DAB	GaN	270/28	5	100	97
[27]	SRC	Si	270/28	3	80-220	96.5
[28]	SRC	-	270/28	2	250	94
[29] - [34]	QAB	SiC	28/28 & 270/270	2.5 & 3	20	96.5
[35]	DAB	-	270/270	2	20	-
[36] - [40]	ABAC	SiC/Si	270/28	10	100	97

Table 1.2 Literature proposals for bidirectional-isolated DC/DC PEC

to the Steinmetz equation (see Chapter 3) [41, 42]. The emergence of wide bandgap semiconductors has facilitated the increment of the switching frequency of bidirectional isolated DC/DC PECs. In consequence, these stages are built with smaller magnetic cores.

Modeling and design of power transformers have been widely characterized in the literature. First, the model of transformer electric and magnetic equivalent circuits is detailed in [43]. Moreover, many design methodologies have been proposed for MFT of DAB topology [44] - [49]. To develop these methodologies, the accurate estimation of power losses under non-sinusoidal excitation has been analyzed in [50] - [55]. As well as the determination of the power losses, the computation of the leakage inductance is of great interest when considering the design of DAB converter [56] - [58]. The importance of the leakage inductance when designing a MFT is noticeable since it can act as decoupling inductance, also known as power transfer inductance. This way, a series inductor typically connected in the HVDC side is avoided. Furthermore, the thermal behavior of power transformers has been widely discussed in literature [59, 60]. Thus, the high number of parameters that impact on the design of magnetic components and need to be considered leads to the proposal of optimal multi-objective design methodologies based on genetic algorithms and neuronal networks [61, 62]. As a result of these researches, the following dissertations have been published [63] - [66]. Although the presented studies can be easily adapted to any core geometry, they are focused on conventional magnetic cores.

Nevertheless, most of the power transformers proposed for MEA applications are planar [67]. Planar core geometries are characterized by a low profile, good thermal behavior, and high-power density [68]. Moreover, planar magnetic components are easy to manufacture and facilitate the implementation of interleaved winding configurations. However, there is a trade-off in these components between the leakage inductance and the interwinding parasitic capacitance when an interleaving strategy is considered. Therefore, the optimal design and trade-offs of planar magnetic components have been addressed in [69]. Also, the determination of the leakage inductance in these structures is studied in [70] - [72]. Hereafter, the literature proposals for the power transformer stage in isolated DC-DC PECs based on planar technology are presented. Considering the power range of the DC-DC converters gathered in the previous section that are proposed for MEA applications, 1-10 kW power transformers are selected.

A power versus frequency map of planar transformers for isolated DC/DC PECs is represented in Fig. 1.8. The researches that developed these power transformers are gathered in Table 1.3. Among the presented transformers, those that are made for 270/28 V have been specifically designed for MEA applications. Furthermore, there are proposals for electric vehicle applications [74]. To exploit the benefits of planar technology, some works that are focused on the configuration of the primary and secondary windings [73,

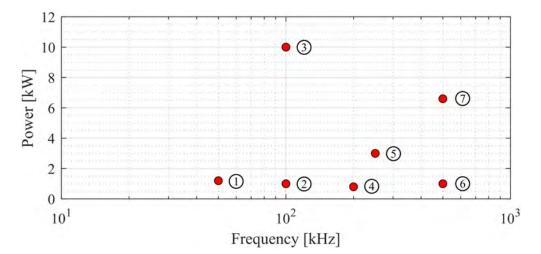


Figure 1.8 Power versus frequency map of planar transformers in isolated DC/DC PECs.

No.	Ref.	$V_{\rm in}/V_{\rm out}$ [V]	Rated power [kW]	Freq. [kHz]
1	[69]	50/25	1.2	50
2	[25]	270/28	1	100
3	[36] - [40]	270/28	10	100
4	[73]	400/100	0.8	200
5	[74]	170-267/235-431	3	250
6	[75]	750/600	1	500
7	[76]	85-265/250-450	6.6	500

Table 1.3 Planar MFT in isolated DC/DC PECs.

75, 76]. Nevertheless, it is important to note that there are no thermal models considering planar core geometries, which makes necessary the adaptation of the available models for conventional core geometries.

At this point, it is marked that the planar technology readiness is high enough to face the challenges to develop isolated bidirectional DC/DC PECs for MEA applications. This technology allows to design and manufacture PECs with higher power density than those based on conventional power transformers. Therefore, the volume and weight of the future PECs for aircraft applications are optimized, which are two of the most important parameters in MEA applications. Moreover, the efficiency of the power transformer is a key parameter to achieve a high-power density converter. Then, multi-objective optimization must be considered to find the best tradeoff between these parameters.

1.3.3 Dual-Active-Bridge and Active-Bridge-Active-Clamp

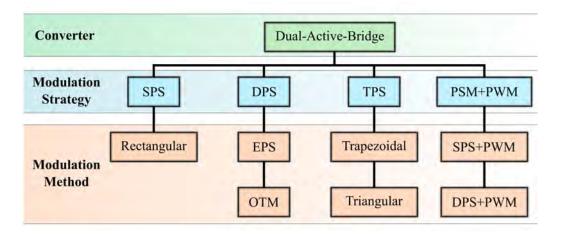
Through section 1.3.1, different literature proposals for the DC/DC PEC of aircraft EPDS have been presented. Among the available options, DAB has been identified as the most promising DC/DC PEC topology. However, the main drawback of this topology is found

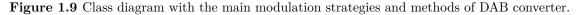
in the bulky output capacitor required to satisfy MEA requirements. Therefore, the ABAC converter has been also considered as an appropriate topology for MEA due to its inherent elimination of the voltage ripple in this component, which considerably decreases the required capacitance. DAB and ABAC converters have been widely studied in literature since they can be utilized in many application proposals, e.g. traction, electric vehicle, and photovoltaic. In order to analyze the gaps of knowledge in both cases, a deep literature review of these converters is done in this section regardless of the application proposal.

Dual-Active-Bridge

The first research study of DAB is found in [77]. It is a bidirectional isolated DC/DC PEC formed by two full-bridge inverter and/or rectifier stages interconnected by a power transformer. A class diagram of the different modulations with which the DAB converter can operate is depicted in Fig. 1.9. In this work, two distinction levels are established: the modulation strategies define the number of angles shifted and/or the presence of a combined Phase Shift Modulation (PSM) plus Pulse Width Modulation (PWM), while the modulation method determines how the different modulation angles are shifted. It is important to note that the PWM can be applied in primary and/or secondary power devices when PSM plus PWM is considered. The most popular modulation methods of DAB converter are SPS Rectangular modulation, TPS-TPM, and TPS-TRM [78] - [80]. These modulation methods, which received their name from the shape of the current waveform obtained in transformer windings, are described in depth in Chapter 2.

SPS Rectangular modulation is the simplest and easiest to implement [81]. In this modulation, the phase shift between the positive terminals of primary and secondary windings of the power transformer is set to manage the power transfer level and the power flow direction. However, the main drawback of this modulation method is the





loss of ZVS when working outside unity DC gain at medium and/or low power transfer. Alternatively, TPS-TPM and TPS-TRM have been proposed to solve this issue [82]. These modulations methods are commonly proposed in a combined modulation method. Nevertheless, there is no continuity in the phase shift angles when the switch between SPS and TPS modulations is produced. Therefore, Optimal Transition Mode (OTM) is proposed to allow the swap while the converter is operating [83]. The scopes of the OTM modulation are to allow the continuity between SPS and TPS as well as to minimize the conduction loss during this transition. As a result, high-efficiency converters are achieved when LVDC buses are expected due to the application requirements [84].

The loss of ZVS operation in DAB has been solved through different modulation methods, among which Extended Phase Shift (EPS) is one of the most popular [85]. Furthermore, modifications to the EPS have been reported to facilitate the implementation of the modulation algorithm while maintaining the benefits of the ZVS operating region [86]. As reported in the literature, DC currents may appear through the transformer depending on the modulation method, which causes saturation on this component. Thus, different controls have been developed to avoid DC currents in the transformer windings [87] - [89]. The large number of modulations available for DAB leads to the proposal of a generic model which can be utilized regardless of the selected modulation method [90]. On the other hand, lower popularity is given to PSM plus PWM which are proposed to reduce the circulating reactive power when working at light load conditions [91].

Alternative modulation methods have been studied to improve the converter efficiency by reducing switching and/or conduction losses compared to the conventional modulations. Considering SPS Rectangular modulation, an optimal modulation method considering frequency variation to increase the efficiency of the converter in the worst operating point is aimed in [92]. The increment of the converter efficiency is done by enhancing the switching and/or conduction behavior. Regarding conduction losses, the circulating reactive power in DAB is a huge handicap when working with a low voltage and highcurrent DC bus. Therefore, Double Phase Shift (DPS) and TPS modulation strategies have been proposed to minimize the reactive power in DAB converter [93] - [96]. Instead, the ZVS behavior of DAB working with SPS Rectangular modulation is improved by the aforementioned TPS-TPM and TPS-TRM. An analysis of the ZVS behavior in the DAB converter is performed in [97, 98]. Also, control algorithms have been developed to reduce the switching losses when working at high frequencies [99]. Nevertheless, it is possible to enhance the ZVS operating region without changing the modulation method by employing auxiliary circuits [100] - [102]. In fact, a variable decoupling inductor has been also considered to extend the ZVS area of the DAB converter [103].

A wide research of DAB converter is focused on design methodologies and strategies to enhance the efficiency of the converter considering different modulation methods [104, 105]. Nonetheless, the most interesting when considering MEA applications are those that look for a multi-objective optimization [106]. Then, different parameters, e.g. cost, efficiency, weight and/or volume, are aimed during the design stage of the converter. As previously stated, the bulky output capacitor is the main drawback of DAB when considering this converter to interconnect HVDC and LVDC sides in the EPDS of an aircraft. This circumstance impact on both volume and weight, penalizing the volumetric and gravimetric power density of the resulting converter. Therefore, interleaved DAB structures have been also considered in the literature for ESS to solve this issue [107] - [109]. The configuration of these structures is set in Input Series Output Parallel (ISOP) and Input Parallel Output Parallel (IPOP), where the parallel connection is always done in the side that requires a reduction of the voltage ripple.

A comprehensive review of the state of the art of DAB converter is performed in this section. A summary of the presented literature works is gathered in Table 1.4, where they are sorted by contribution.

Active-Bridge-Active-Clamp

ABAC converter, also known as current-fed DAB, has been presented for hybrid ESS applications in [110]. The configuration of this converter is identical to the DAB on the HVDC side, while the LVDC side is modified by including clamp capacitors and output

Table 1.4 Summary of literature contributions for DAB converter.
--

Ref.	Contribution	Application
[77]	Characterization of DAB converter for high-power and high-power density DC/DC conversion	Aerospace
[78] - [80]	Modeling, design and optimization of DAB converter considering different modulation methods	Traction and Electric Vehicle
[81]	Analytical modeling of SPS Rectangular modulation	Aerospace (MEA)
[82], [97] - [99]	Modulation methods to extend the ZVS operating region of DAB	Traction
[83, 84]	Alternative modulation method (OTM) to increase the efficiency of DAB in the transition between SPS Rectangular and combined TPS-TPM and TPS-TRM	Electric Vehicle
[85, 86]	Characterization of EPS modulation to improve the ZVS behavior. Modifications to EPS modulation.	Aerospace (MEA)
[87] - [89]	Control methods to avoid DC currents flowing through the transformer windings	Electric Vehicle
[90]	Generic and unified model of DAB converter that is applicable to any considered modulation method	-
[91]	Control strategy based on the combination of PSM+PWM modulation strategies	Electric Vehicle
[92]	Optimal modulation method considering frequency variations to SPS Rectangular modulation	Traction
[93] - [96]	Control methods to minimize the circulating reactive power in DAB converter with DPS and TPS modulation strategies	-
[100] - [103]	Auxiliary circuits and variable inductor to enhance ZVS behavior.	Wide Voltage/Load Operation
[104] - [106]	Design optimization of DAB converter	Wide Voltage/Load Operation
[107] - [109]	ISOP and IPOP structures to reduce voltage ripple in LVDC ca- pacitors	ESS

inductors. The modulation strategies and methods are similar to DAB, which are exposed in Fig. 1.9.

Although the literature on ABAC converter is not as extensive as on DAB, there are also proposals of this converter for photovoltaic applications [111]. Furthermore, the optimized operation of ABAC converter has been studied to increase the efficiency in photovoltaic systems [112]. As previously commented, the main advantage of this topology is the voltage ripple cancelation on the LVDC side due to the phase opposition of the current ripple that flows through the output inductors (see Chapter 2). Nevertheless, the same ZVS and conduction losses issues that those reported on DAB topology are found. Therefore, optimized switching patterns have been proposed for ABAC converter based on SPS Rectangular modulation to increase the efficiency when working at high switching frequencies [113]. Advanced modulation methods have been researched to extend the ZVS area of the converter in the whole operating points [114]. In MEA applications, the main contribution to the power losses comes from the switching and/or conduction losses of the power devices that are placed on the LVDC side. Thus, DPS modulation control the phase shift between the positive terminals of the power transformer and between the midpoints of the half-bridge branched that compose the secondary side is proposed in [115]. As well as in DAB, the reduction of the conduction losses is also aimed in ABAC [116]. Then, split secondary configurations have been considered to reduce the conduction losses on the LVDC side in MEA applications [36] - [40]. Variations to the configuration of the ABAC converter have been studied to reduce the low-frequency input current ripple when the converter is connected to a single-phase inverter load [117].

Comparative evaluation between current-fed and voltage-fed DAB-based converters is performed in detail in [118]. Moreover, different configurations of current-fed DAB converters are compared in [119]. Finally, DPS plus PWM modulation methods are applied to ABAC when aiming to reduce the circulating current that flows through the different stages of the converter [120]. A wide revision of the work presented at international conferences and/or journals for ABAC and current-fed DAB-based topologies is developed in this section. A summary of the literature review that is done along this section for ABAC converter is gathered in Table 1.5.

1.4 Motivation and Objectives

The motivation of this work lies in the need for new tools and methods that aid in the design procedure of high-power bidirectional isolated DC/DC PECs for electric aircraft applications. The sizing of passive components, power devices and cooling systems must be aimed in detail to reach high-power density values. To achieve this goal, different con-

Ref.	Contribution	Application
[110, 111]	Multiport soft-switched bidirectional isolated DC/DC converter	ESS and Photovoltaic
[112, 113]	Optimized operation of ABAC converter to improve the efficiency of the system	ESS and Photovoltaic
[114, 115]	Alternative modulation methods to extend the ZVS operating area of ABAC converter	-
[116]	Minimization of conduction losses in ABAC converter	LVDC applications
[117]	Reduction of input current ripple	Photovoltaic
[118, 119] $[120]$	Comparative evaluation an review of current-fed and voltage-fed DAB based topologies DPS plus PWM modulation method to increase the efficiency of ABAC converter	LV and HC applications Photovoltaic

 Table 1.5 Summary of literature contributions for ABAC converter.

verter topologies and modulation methods presented in the literature have been exposed in this chapter. Among the considered topologies for MEA applications, DAB is the most commonly used. Alternatively, ABAC converter has been also proposed to reduce the bulky output capacitor required in DAB to fulfill the strict voltage ripple requirement in the LVDC bus.

These power converters have been studied in depth in the literature considering different application proposals. Nevertheless, the impact of each converter in aircraft EPDS has not been characterized in detail, where different design axis must be considered. The most important design variables when considering MEA applications are volume, weight, cost per kilowatt, Mean Time Between Failures (MTBF) of power devices, and power losses. To optimize these parameters, semiconductor technologies and modulation methods are the main degrees of freedom. Switching, RMS and Average (AVG) currents stress in the whole working region must be computed to size the cooling system of the power converter.

The wide number of parameters that impact on the design of these power converters leads to the proposal of this work, which is launched to examine how the aforementioned design variables impact on DAB and ABAC topologies. Through this work, analytical evaluation of DAB has been developed considering SPS Rectangular, TPS-TPM and TPS-TRM modulation methods to obtain the values of switching, RMS and AVG currents. These analytical models have been verified with a simulation model developed in PLECS. The verification of these models aids to determine switching and conduction losses in primary and secondary power devices. Moreover, the same mathematical development and characterization have been done for ABAC converter when working with SPS Rectangular modulation.

The objective of these models is to develop new optimization routines that aid the designers of these PECs by reducing the computational cost of the design stage, enabling

a comprehensive evaluation of each design variable. Furthermore, the roadmaps of the semiconductor technologies, cooling system, magnetic core shapes (planar or conventional) and materials, and capacitor technologies that are considered in this work are given. These roadmaps are based on analytical component models that are detailed in the appendices of this thesis, which are extracted based on LTSpice simulation models (semiconductors) and datasheet and/or manufacturer data (cooling system, magnetic core, and DC bus capacitors).

The mentioned contributions are related to the following lines of research:

- Comparison of the proposed topologies with the presented analytical models, identifying the benefits and drawbacks of each power converter.
- Characterization of the power losses distribution in the whole operating region, determining the critical working point.
- Determine the tradeoff between the volume and/or weight of the transformer and output capacitor when considering IPOP structures in the DAB converter.
- Obtain a roadmap of the application to determine the scenarios that encourage the utilization of the considered PECs in MEA applications.

To sum up, the present work aims to deal with the issues that must be faced to fulfill the requirements of MEA applications when bidirectional isolated DC/DC PECs are required. Therefore, a wide understanding of the behavior of DAB and ABAC converters is obtained, which can be also extrapolated to any considered application.

1.5 Structure of the Document

The outline of this dissertation is gathered in this section. A descriptive diagram of the contents that are covered in this work is presented in Fig. 1.10. In this diagram, the contents of the present work are distributed as follows:

• In Chapter 1, the current trends in the EPDS of an aircraft are shown together with the proposals for future electric aircraft. Furthermore, an exhaustive review of the existing state of the art of bidirectional isolated DC/DC PECs for MEA applications is carried out. Through this analysis, DAB and ABAC converters are identified as the most promising topologies for MEA. Therefore, the literature contributions of these converters are studied regardless of the application proposal, detailing the principal gaps of knowledge found.

1. INTRODUCTION

	Ch. 1: Introduction Exhaustive review of the current state of the art of bidirectional isolated DC/DC PECs for MEA applications.	
	Ch. 2: Bidirectional Isolated DC/DC PECs Comprehensive analysis and characterization of DAB and ABAC converters. Development of the theoretical description and simulation models of these converters.	
Lul	Ch. 3: Design of Magnetic Components Design of the power transformer and output inductors that are placed in DAB and ABAC topologies.	
	Ch. 4: Optimal Design Methodology for MEA Optimization of the gravimetric and/or volumetric power density of the DAB and ABAC converters with brute force algorithms.	
	Ch. 5: Conclusions and Future Work Main conclusions and future lines of research that are obtained from the development this work.	

Figure 1.10 Descriptive diagram of the structure of this dissertation.

- In Chapter 2, DAB and ABAC converters are characterized in detail. To this aim, SPS Rectangular and combined TPS-TPM and TPS-TRM are considered, which are the most popular modulation methods of these converters. Then, the analytical models that describe the behavior of these converters are gathered in this chapter. Furthermore, the states when working with the different modulation methods are depicted. To obtain the RMS and AVG currents, the Piecewise Linear (PWL) models that define the shape of the current waveform that flows through the transformer windings are given. Furthermore, the analysis of DAB and ABAC converters based on the analytical models developed in PLECS. Also, the design space analysis of DAB converter is done, as well as the experimental validation of the analytical models in this converter.
- In Chapter 3, the design of the magnetic components that conform to both converters is aimed. Then, the analytical models that are useful for the design of the power transformer stage (DAB and ABAC) and output inductors (ABAC) are detailed based on literature works. Then, the analytical design of these components is validated with Finite Element Analysis (FEA) tools to characterize in-depth the parasitic capacitances and inductances that inherently appear due to the component behavior.

- In Chapter 4, the optimization of the bidirectional isolated DC/DC PECs that are studied in this work is focused on. To optimize the power density of the result-ing converter, a brute force algorithm is developed based on the analytical models developed in this work.
- In **Chapter 5**, the conclusions extracted from this work are gathered with the resulting contributions. Furthermore, the future lines of research that are open after this investigation are pointed out.

2

Bidirectional Isolated DC/DC PECs

Summary:

Along this chapter, the most promising DC/DC PECs are described in detail. To this aim, the analytical models that govern the behavior of DAB and ABAC converters when working with the main modulation methods are presented. Furthermore, the switching states of both converters are depicted, as well as the ZVS operating areas. Also, the analytical models to determine the RMS and AVG currents that flow through the different components and the minimum dead time required to achieve ZVS in the power devices of these converters are given. An evaluation of IPOP DAB structures is done in this section to analyze the impact of the output capacitor in this converter topology. Finally, an analysis of the power losses in the switching devices of these converters is done.

2.1 Introduction

Bidirectional isolated DC/DC PECs are commonly utilized to interface ESS with DC grids and/or loads. These converters are typically found in traction, marine, electric vehicle and/or aircraft applications. The main interests of these converter topologies, lies in the bidirectional capability and the isolation stage included.

The device that provide isolation between both sides of the converter is a power transformer, whose size is lower than classical low-frequency power transformers. Since the emergence of wide bandgap SiC and GaN semiconductors, the operating frequency of the PECs is constantly increasing, which directly affects to the sizing of the magnetic devices (see Chapter 3).

As reviewed along Chapter 1, the principal proposals of bidirectional isolated DC/DC PECs are focused on DAB converter. This converter topology is the most popular in MEA applications. Nevertheless, the strict LVDC voltage ripple requirement becomes a disadvantage for this topology, appearing new converter proposals as ABAC.

In the MEA literature of these PECs (see Table 1.2), the contributions are mainly focused on the design of these converters under different modulation methods to achieve high-power density DC/DC conversion. Nevertheless, there is a lack of analytical models that describe the behavior of these PECs.

In this context, the analytical models of the power devices considering the main modulation methods of these converters are developed in this work. These models provide an insightful knowledge to the system designer, allowing a fast evaluation of different semiconductor and capacitor technologies.

Therefore, the equations provided in this chapter aids in the design steps of DAB and ABAC power converters, avoiding the large time consumption derived from simulation methods. This fact enable the contribution of a brute-force based Multi-Objective Optimization (MOO) which helps to determine which converter provides the best efficiency to power density trade-off (see Chapter 4).

Along this chapter, the behavior of DAB and ABAC converters considering the classical SPS Rectangular modulation is detailed. Furthermore, alternative modulation methods as TPS-TPM and TPS-TRM are also analyzed for DAB converter, as well as the evaluation of IPOP configurations based on the Fourier series equations.

In order to characterize the required dead-time in these topologies, the minimum value to achieve a complete ZVS behavior is given. Finally, the evaluation of the power losses in the HVDC and LVDC switching devices of DAB and ABAC converter is done to study the impact of the LVDC differences between both converters.

2.2 Dual-Active-Bridge

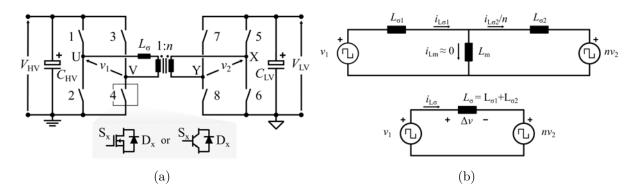
The schematic of DAB converter is shown in Fig. 2.1(a). It is formed by two full-bridge inverter and/or rectifier stages interconnected by a power transformer. Semiconductors S_1 - S_4 connect the primary side of the transformer to the HVDC side, while the secondary side is connected through S_5 - S_8 to the LVDC side. Moreover, the AC equivalent circuit of DAB converter is presented in Fig. 2.1(b) referred to the primary side. Considering that the magnetizing inductance (L_M) of the power transformer is noticeable larger than the decoupling inductance (L_{σ}), the equivalent circuit is simplified to the bottom picture.

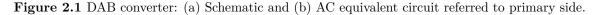
Three different control angles can be distringuished, which are the phase shift between nodes U-X, U-V and X-Y. The shifting of these angles is reflected in transformer primary and secondary waveforms as δ , Ω_1 and Ω_2 respectively. In Fig. 2.2, the corresponding angles are represented on the transformer voltage waveforms with TPS-TPM modulation.

A wide diversity of modulation methods are available in DAB converter due to the large quantity of active power devices that are utilized in this converter. Nevertheless, this work is focused in the most popular modulation methods of DAB, which are SPS Rectangular, TPS-TPM and TPS-TRM. Hereinafter, the operating modes of each modulation method are presented along with the analytical models that describe its behavior.

2.2.1 SPS Rectangular Modulation

SPS Rectangular Modulation is the main modulation method of DAB converter, which only modifies the modulation angle δ between $-\pi/2$ and $\pi/2$ to manage power flow direction and power transfer level. In this modulation, the phase shift between the mid-points of primary and secondary half-bridge branches (Ω_1 and Ω_2) are set to zero. Furthermore, the maximum power transfer is only achieved with this modulation when considering a specific design, i.e. for a given output power (P_{out}), switching frequency and decoupling





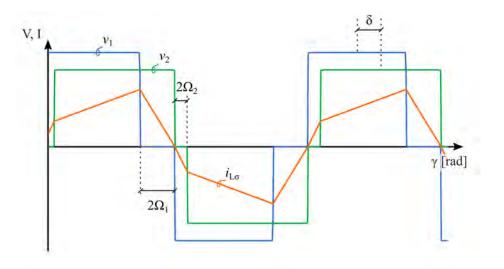


Figure 2.2 Voltage waveforms in primary (v_1) and secondary (v_2) windings of the power transformer together with the current waveform that flows through the decoupling inductor.

inductance. Mathematical development to obtain switching currents in primary and secondary power devices is described in [78, 79], resulting in (2.1) for the primary and secondary switching currents (I_{sw1} and I_{sw2}) referred to the primary side of the transformer with this modulation:

$$I_{\rm sw1} = \frac{V_{\rm HV} \pi + n \, V_{\rm LV} \, (2 \, |\delta| - \pi)}{4 \, \pi \, f_{\rm sw} \, L_{\sigma}} \, , \quad I_{\rm sw2} = \frac{V_{\rm HV} \, (2 \, |\delta| - \pi) + n \, V_{\rm LV} \, \pi}{4 \, \pi \, f_{\rm sw} \, L_{\sigma}} \, , \qquad (2.1)$$

where *n* is the transformer turns ratio, $V_{\rm HV}$ and $V_{\rm LV}$ are the voltages of the HVDC and LVDC sides respectively, δ is the modulation angle, $f_{\rm sw}$ is the switching frequency and L_{σ} is the decoupling inductance.

As previously menctioned, there are three degrees of freedom when the design of a DAB converter is aimed, i.e. P_{out} , f_{sw} and L_{σ} . This is due to the fact that given two of these three parameters, the remaining parameter is easily determined from (2.2):

$$P_{\rm out} = \frac{V_{\rm HV} \, n \, V_{\rm LV} \, \delta \, \left(\pi - |\delta|\right)}{2 \, \pi^2 \, f_{\rm sw} \, L_{\sigma}} \quad . \tag{2.2}$$

Moreover, the equation to determine the required δ to transfer the desired P_{out} is obtained by rearranging this equation, which is shown in (2.3):

$$\delta = \frac{\pi}{2} \left(1 - \sqrt{1 - 8 f_{\rm sw} L_{\sigma} P_{\rm out} \left(\frac{1}{V_{\rm HV}^2 M}\right)} \right)$$
(2.3)

being important to note that there is not possible to transfer the desired output power at the specified working point if the solution of this equation is complex.

The voltage waveforms in primary and secondary windings of the power transformer

and the current waveform through the decoupling inductor when working with SPS Rectangular modulation are shown in Fig. 2.3. There are two operating modes, which depends on the DC gain ($M = nV_{\rm LV}/V_{\rm HV}$) of the corresponding working point:

- Case I: In this case, hard switching turn-on and turn-off transitions are expected in primary or secondary power devices. The conditions to work in these operating region are to reach negative values in the primary or secondary switching currents $(I_{sw1} < 0 \text{ or } I_{sw2} < 0)$, as represented in Fig. 2.3(a).
- Case II: This operating mode is also known as the ZVS working area of DAB converter. Actually, this converter is typically designed to operate in this region at nominal conditions, which is found at high-power transfer and/or normalized DC gain $(n V_{\rm LV}/V_{\rm HV})$ close and/or equal to unity.

The states of the DAB converter are differenciated in Fig. 2.3, which are pictured in Fig. 2.4. There are eight different states, whose nomenclature goes from a-h [78, 80]. Hereinafter, these states are described in detail:

- State a: This state is present when the primary and secondary voltages are positive and negative respectively, being negative the value of the current that flows through the transformer. Then, primary and secondary diodes D_1 and D_4 , and D_6 and D_7 are conducting current [see Fig. 2.4(a)]. This state leads to states b and/or c when the sign of the secondary voltage waveform turns positive (case I) or the current value reaches zero (case II).
- State b: The state b appears in case I when the voltage in the secondary winding of the transformer shift to positive while the current stills being negative. Thus, there is

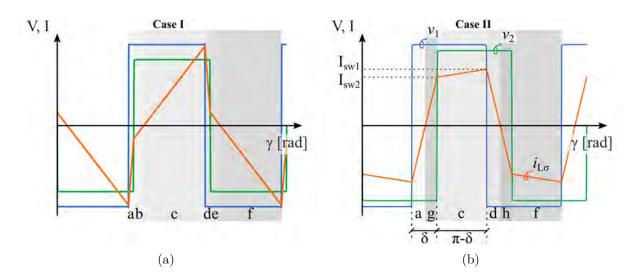


Figure 2.3 Voltage and current waveforms in transformer windings in the different operating modes of DAB converter: a) case I and b) case II.

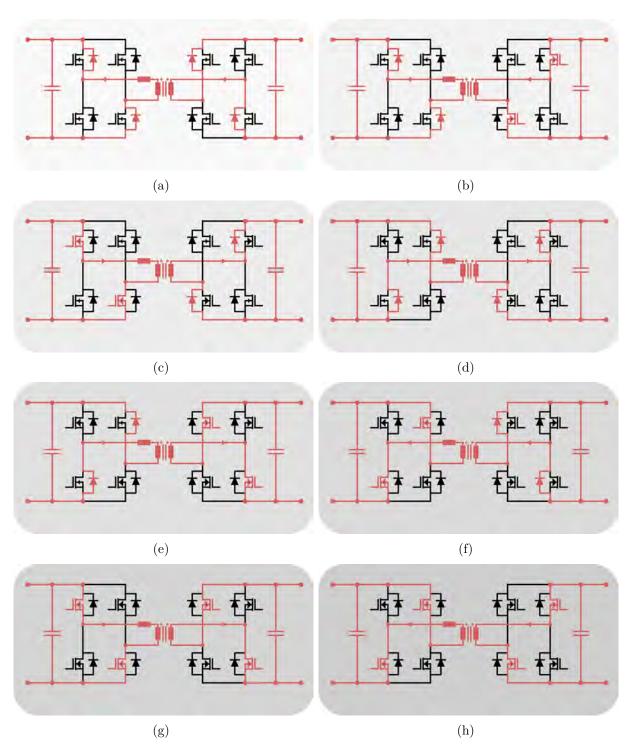


Figure 2.4 States of DAB converter when working with SPS Rectangular modulation.

no change in the primary side regarding state a, while the secondary semiconductors M_5 and M_8 turn-on to start the conduction mode [see Fig. 2.4(b)]. Since this switching takes place with the corresponding circulating current, there are turn-on losses associated with the transition between states a and b.

• State c: The state c is common to both cases, which begins when the voltages and current values are positive. In this state, semiconductors M_1 and M_4 , and D_5 and

 D_8 are in conduction mode [see Fig. 2.4(c)]. The transition to this state is lossless in both cases for primary semiconductors, while there is a current flowing through secondary power devices in the turn-off of M_6 and M_7 in case II.

- State d: This state, which is also present in both cases, is preceded by state c. There is no change in secondary power devices, while turn-off transition with the losses associated to the corresponding switching current are in the primary side, where D_2 and D_3 are conducting current [see Fig. 2.4(d)].
- State e: This state only takes place in case I. There are no changes in primary side, since the difference regarding state d is the change in the sign of the value of the secondary voltage. Then, secondary semiconductors M₆ and M₇ turn-on with the corresponding switching losses [see Fig. 2.4(e)].
- State f: Also present in both cases, states e and h are prior to state f. The transition to this state is lossless in primary side. However, turn-off losses are related to M_5 and M_8 in case II.
- States g and h: These states are in case II. In both states, the associated switching losses are related to the turn-off switching of secondary semiconductors M₅ and M₈, and M₆ and M₇ when shifting from states g and h to c and f respectively.

The transition between cases I and II is found at the condition of negative primary and/or secondary switching currents. Therefore, the analytical model of the boundary between ZVS and hard-switching operating regions are obtained by equating (2.1) and (2.2) to zero, which results in:

$$M_{\text{DAB1}} = \frac{\pi}{n \left(\pi - 2 \ |\delta|\right)} \ , \ M_{\text{DAB2}} = \frac{(\pi - 2 \ |\delta|)}{n \pi} \ , \tag{2.4}$$

where M_{DAB1} and M_{DAB2} are the normalized DC gain $(n V_{\text{LV}}/V_{\text{HV}})$ of DAB that establish the boundaries between ZVS (case II) and hard-switching (case I) in primary and secondary power devices respectively. In Fig. 2.5, these functions are plotted versus the normalized output power for δ modulation angle in the range $[-\pi/2,\pi/2]$. The relationship between M_{DAB1} and M_{DAB2} with the output power is obtained by rearranging in function of the normalized DC gain (M) (2.3):

$$P_{\rm out} = \frac{(V_{\rm HV})^2 \, M \, \delta \, (\pi - |\delta|)}{2 \, \pi^2 \, f_{\rm sw} \, L_{\sigma}} \quad . \tag{2.5}$$

In this work, the following nomenclature is adopted: forward and backward modes refer to power flow direction, while buck and boost modes distinguish the relationship between $V_{\rm HV}$ and $V_{\rm LV}$. Then, the operating area is divided in four quadrants, which are

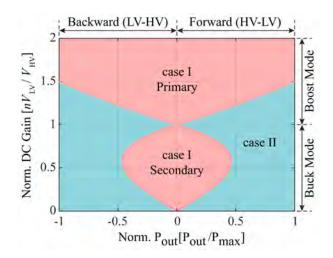


Figure 2.5 Operating areas of case II and case I in DAB converter

backward-buck, backward-boost, forward-buck and forward-boost. Furthermore, primary and secondary sides are considered HVDC and LVDC sides regardless the power flow direction, resulting in a symmetrical operating regions with respect to y-axis. The characterization of these areas is of huge interest in order to determine the switching losses in power devices in each working point.

On the other hand, the ability to determine the conduction losses in power devices is also important. To address this issue, the PWL functions of the transformer current waveform presented in (2.6) for case II are utilized afterwards to obtain the RMS and AVG currents that flows through every component of the converter:

$$i_{\mathrm{L}\sigma}(t) = \begin{cases} -I_{\mathrm{sw1}} + \frac{I_{\mathrm{sw1}}}{T_{1}}t & 0 \le t \le T_{1} \\ \frac{I_{\mathrm{sw2}}}{(T_{2} - T_{1})}(t - T_{1}) & T_{1} \le t \le (T_{1} + T_{2}) \\ I_{\mathrm{sw2}} + \frac{(I_{\mathrm{sw1}} - I_{\mathrm{sw2}})}{T_{3}}(t - (T_{1} + T_{2})) & (T_{1} + T_{2}) \le t \le T_{\mathrm{sw}}/2 \end{cases}$$
(2.6)

where T_1 , T_2 and T_3 are the times that define the intervals of the current waveform. Considering the AC equivalent circuit presented in Fig. 2.1(b), these characteristic times are obtained utilizing the equation of the voltage across the decoupling inductance (Δv):

$$\Delta v = L_{\sigma} \, \frac{di_{L\sigma}}{dt} \quad , \tag{2.7}$$

$$T_1 = \frac{L_{\sigma}}{V_{\rm HV} + n \, V_{\rm LV}} \, I_{\rm sw1} \, , \ T_2 = \frac{L_{\sigma}}{V_{\rm HV} + n \, V_{\rm LV}} \, I_{\rm sw2} \, , \ T_3 = \frac{T_{\rm sw}}{2} - (T_1 + T_2) \, , \qquad (2.8)$$

which only can be utilized for forward power transfer in the case II. The analytical models to determine RMS and AVG currents in power devices are gathered in Table 2.1 for forward mode in case II. These models are really useful to accurately calculate the conduction power losses in the semiconductors. The nomenclature adopted in these equations for the switching devices (S or D) is utilized to differentiate the sign of the current, being possible to determine hindsight the power losses regardless the selected device (IGBT or MOSFET). In Fig. 2.6, the provided times and devices nomenclature are represented in order to clarify the assumptions taken.

In this subsection, the theoretical description of the SPS Rectangular modulation has been analyzed. Hereinafter, alternative modulation methods to improve the switching behavior of the converter when working at high-switching frequencies are described and discussed.

Table 2.1 Analytical models of the RMS and AVG currents in power devices referred to the primary side in the case II of SPS Rectangular modulation. Forward power transfer (HVDC to LVDC).

Switch	RMS	AVG
S ₁₋₄	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \cdot \left(\frac{I_{\rm sw2}^2}{3} \cdot T_2 + \frac{I_{\rm sw1}^2 + I_{\rm sw2}^2 + I_{\rm sw1} \cdot I_{\rm sw2}}{3} \cdot T_3\right)}$	$\left \left(\frac{1}{T_{\rm sw}} \right) \cdot \left(\frac{I_{\rm sw2}}{2} \cdot T_2 + \frac{I_{\rm sw1} + I_{\rm sw2}}{2} \cdot T_3 \right) \right $
S ₅₋₈	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\cdot\left(\frac{{I_{\rm sw2}}^2}{3}\cdot T_2\right)}$	$\left(\frac{1}{T_{\rm sw}}\right)\cdot\left(\frac{I_{\rm sw2}}{2}\cdot T_2\right)$
D ₁₋₄	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\cdot\left(\frac{{I_{\rm sw1}}^2}{3}\cdot T_1\right)}$	$\left(\frac{1}{T_{\rm sw}}\right)\cdot\left(\frac{I_{\rm sw1}}{2}\cdot T_1\right)$
D ₅₋₈	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \cdot \left(\frac{I_{\rm sw1}^2}{3} \cdot T_1 + \frac{I_{\rm sw1}^2 + I_{\rm sw2}^2 + I_{\rm sw1} \cdot I_{\rm sw2}}{3} \cdot T_3\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \cdot \left(\frac{I_{\rm sw1}}{2} \cdot T_1 + \frac{I_{\rm sw1} + I_{\rm sw2}}{2} \cdot T_3\right)$

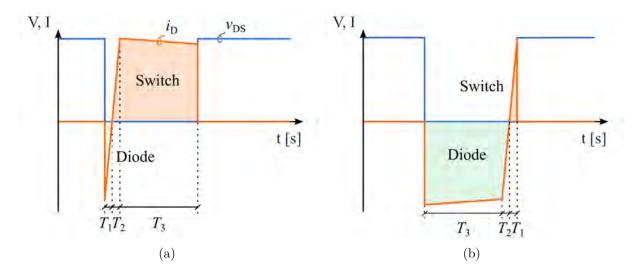


Figure 2.6 Drain to source voltage and drain current waveforms in DAB power devices when working in case II (forward power transfer): a) primary and b) secondary devices.

2.2.2 TPS Trapezoidal and Triangular Modulations

Alternatively to SPS Rectangular modulation, combined TPS - TPM and TPS - TRM are utilized to extend the ZVS operating area of the converter when the converter operates at medium and/or high switching frequencies. Then, the efficiency of the converter is increased when working at medium and low power transfer considering that the converter is designed to transmit the maximum power transfer working with SPS Rectangular modulation at δ equal to $\pi/2$. In these modulation methods, δ , Ω_1 and Ω_2 are modified at the same time to get trapezoidal and/or triangular current waveforms through the transformer windings. In Fig. 2.7, voltage and current waveforms in transformer windings are presented for both modulation methods. As well as in SPS Rectangular modulation, eight states are differenciated [78, 80]:

- State a: This state occurs in TPS-TPM, and also in TPS-TRM when working in the condition $V_{\rm HV} < n V_{\rm LV}$. The voltage across primary side is positive and zero in the secondary winding, which makes that the current has a growing trend. The beginning of this state is at zero current level, while the transition from state a to b results in the turn-off losses of the secondary power devices.
- State b: It is common to both modulations independently the operating condition. The shifting between states b and c results in the turn-off losses of semiconductor M_4 , while b to d transition is lossless since the current level is zero.
- State c: In this state, voltage at primary terminals of the power transformer is zero, while the secondary voltage is positive. Furthermore, no power losses when shifting from state c to d or e are found due to the zero current level.

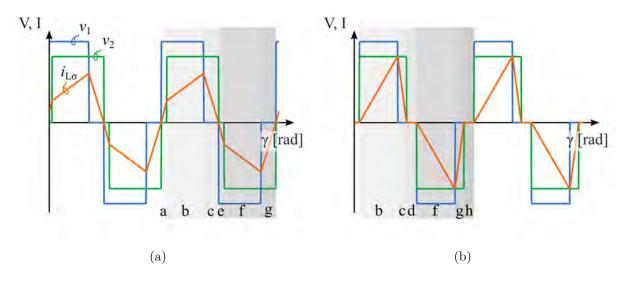


Figure 2.7 Voltage and current waveforms in TPS modulation methods of DAB converter: a) TPM and b) TRM ($V_{\rm HV} > n V_{\rm LV}$)

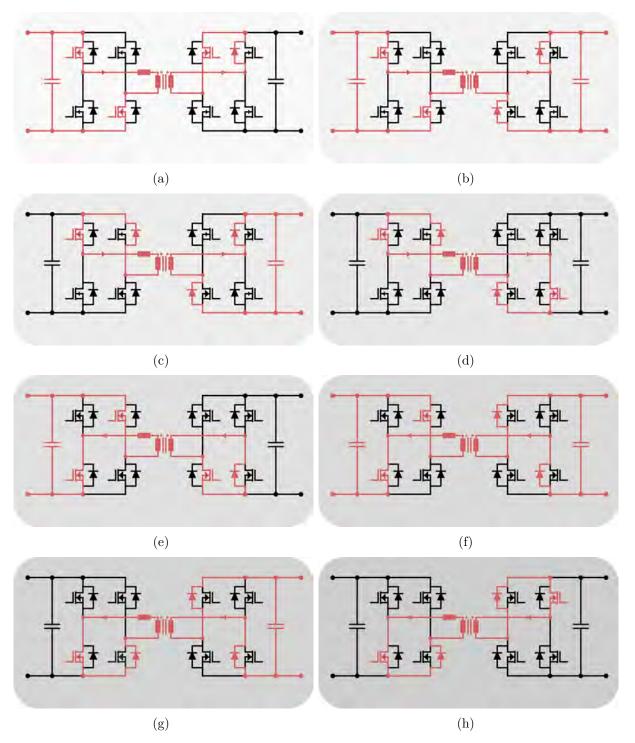


Figure 2.8 States of DAB converter when working with TPS-TPM and TPS-TRM modulation.

- States d and h: These states represent the two possibilities for the circulation of the remaining current in both primary and secondary sides in the interval in which primary and secondary voltages are set to zero.
- State e: This state is characterized by the turn-off switching losses of the semiconductor M_8 in the e-f transition. The voltage in the primary side is positive, while the secondary voltage changes from zero to a negative value in e-f shift causing the

described losses.

- State f: The transition between states f and g in TPS-TPM and TPS-TRM $(v_1 > n v_2)$ generates losses in the semiconductor of the primary side M_3 . However, there are no switching losses due to the f-h transition.
- State g: There are not losses associated with the shifting between states g and h, which is due to the zero circulating current. In this state, primary voltage is zero while both secondary voltage and circulating current are negative, which cause that semiconductors M_1 , D_4 , D_6 and D_8 are in conduction.

From the description of these states, it is clear that the switching behavior of these modulation methods is inherently better than in SPS Rectangular modulation, since the hard switching losses from turn-on and off commutations are clearly reduced. This fact improves the efficiency of the converter when working with TPS - TPM and TPS - TRM. In order to profundize in the analytical models that describe the behavior of these modulation methods, a detailed characterization is presented down below. To simplify the operating conditions and thus the resulting equations, the t_{dt} in the power devices is neglected in these modulation methods. However, the analytical models that consider this parameter have been previously reported in [78] - [80].

The analytical models that describe the behavior of the converter when working with this modulation method are more complex than with SPS Rectangular modulation. First, the P_{out} transferred by the converter with TPS-TPM is defined in (2.9):

$$P_{\rm out} = sgn(\delta) V_{\rm HV}^{2} \frac{(\pi - |\delta| - \Omega_{1} - \Omega_{2}) \left[M^{2} \left(|\delta| - \Omega_{2} + \Omega_{1}\right) + M \left(|\delta| - \Omega_{1} + \Omega_{2}\right)\right] + M^{2} \left(|\delta| - \Omega_{2} + \Omega_{1}\right)^{2}}{4 \pi^{2} f_{\rm sw} L_{\sigma}} .$$
(2.9)

DAB converter is able to work with TPS-TPM when the modulation angle δ_{TPM} is comprised between certain values ($\delta_{\min,\text{TPM}}$ and $\delta_{\max,\text{TPM}}$). The boundaries of the modulation angle δ are established in (2.10) in function of M:

$$\delta_{\min,\text{TPM}} = \begin{cases} \frac{\pi}{2} (1 - M) & \text{if } M < 1\\ \frac{\pi}{2} \left(1 - \frac{1}{M}\right) & \text{if } M \ge 1 \end{cases}$$
(2.10)

$$\delta_{\max,\text{TPM}} = \frac{\pi}{2} \left(\frac{1+M^2}{1+M+M^2} \right) \quad . \tag{2.11}$$

In Fig. 2.9, the operating area of combined TPS-TPM and TPS-TRM is presented

considering that the converter is designed to transfer the maximum output power in SPS Rectangular modulation at $\delta = \pi/2$ and M = 1. The maximum $I_{\rm LV}$ of this modulation method is achieved at $\delta = \pi/3$, which match with the condition $V_{\rm HV} = n V_{\rm LV}$, i.e. M = 1. However, the maximum extractable output power is higher if the normalized DC Gain is increased when $V_{\rm HV}$ is fixed and $V_{\rm LV}$ is raised. This is due to the fact that the output power results from the product of $I_{\rm LV}$ and $V_{\rm LV}$. There is also another way to modify the normalized DC gain by decreasing $V_{\rm HV}$ while $V_{\rm LV}$ is set to a certain value. If the normalized DC gain is increased by reducing the value of the $V_{\rm HV}$, the operating area described in Fig. 2.9 is narrowed, and thus the maximum P_{out} and I_{LV} are lower. For the operating conditions presented in Fig. 2.9, i.e. constant $V_{\rm HV}$ and variable $V_{\rm LV}$, the maximum $P_{\rm out}$ is asymptotic at twice of the nominal output power (red dashed line), although this are not commonly used operating conditions for DAB. In this case where the primary referred LVDC is much larger than the HVDC $(n V_{LV} \gg V_{HV})$, the operating area of the TPS - TPM is not relevant, being this region characterized by the wide area in which TPS-TRM is able to work. In order to determine the modulation angle δ_{TPM} to transfer the desired $P_{\rm out}$, the following equation is utilized:

$$\delta_{\text{TPM}} = sgn\left(P_{\text{out}}\right) \frac{\pi}{2\left(1 + M + M^2\right)} \\ \left(\left(1 + M^2\right) - \left(1 + M\right)\sqrt{M - \frac{4f_{\text{sw}}L_{\sigma} |P_{\text{out}}| \left(1 + M + M^2\right)}{V_{\text{HV}}^2 M}}\right) , \quad (2.12)$$

which impacts on the resulting $\Omega_{1,\text{TPM}}$ and $\Omega_{2,\text{TPM}}$. Depending on the normalized DC gain of the converter, the equations to determine $\Omega_{1,\text{TPM}}$ and $\Omega_{2,\text{TPM}}$ are defined in (2.13):

$$\Omega_{1,\text{TPM}} = \begin{cases}
\left| \delta_{\text{TPM}} \right| - \Omega_{2,\text{TPM}} \\
\frac{\pi (1 - M) + 2M |\delta_{\text{TPM}}|}{2 (1 + M)} & \Omega_{2,\text{TPM}} = \begin{cases}
\frac{\pi (M - 1) + 2 |\delta_{\text{TPM}}|}{2 (1 + M)} & \text{if } M < 1 \\
|\delta_{\text{TPM}} - \Omega_{1,\text{TPM}} & \text{if } M \ge 1
\end{cases}$$
(2.13)

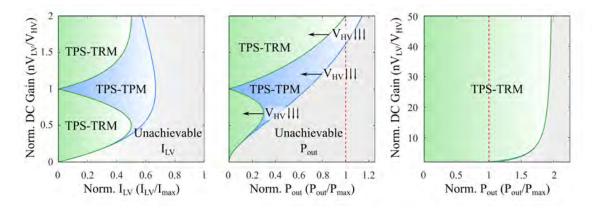


Figure 2.9 Operating area of combined TPS-TPM and TPS-TRM considering: a) the LVDC current, b) the output power and d) the asymptotic behavior at high DC gain values.

2. BIDIRECTIONAL ISOLATED DC/DC PECS

Regarding TPS-TRM, the upper boundary of this modulation coincides with the lower boundary of TPS-TPM set in (2.10). Both modulation methods are a continuation of each other for low and medium/high power transfer. Then, the analytical models that define the behavior of TPS-TRM differ above and below M = 1, as the output power defined in (2.14):

$$P_{\rm out} = \begin{cases} \frac{V_{\rm HV} \, M \, \delta_{\rm TRM} \, (\pi - 2 \, \Omega_{2,\rm TRM})}{2 \, \pi^2 \, L_{\sigma} \, f_{\rm sw}} & \text{if } M < 1 \\ \frac{V_{\rm HV} \, M \, \delta_{\rm TRM} \, (\pi - 2 \, \Omega_{1,\rm TRM})}{2 \, \pi^2 \, L_{\sigma} \, f_{\rm sw}} & \text{if } M > 1 \end{cases}$$
(2.14)

The equations required to compute the modulation angle δ_{TRM} are defined in (2.15):

$$\delta_{\text{TRM}} = \begin{cases} sgn(P_{\text{out}}) \frac{\pi \sqrt{|P_{\text{out}}| \ L_{\sigma} f_{\text{sw}} (1-M)}}{V_{\text{HV}} M} & \text{if } M < 1\\ sgn(P_{\text{out}}) \frac{\pi \sqrt{|P_{\text{out}}| \ L_{\sigma} f_{\text{sw}} (1-1/M)}}{V_{\text{HV}}} & \text{if } M > 1 \end{cases}$$
(2.15)

which also define the $\Omega_{1,\text{TRM}}$ and $\Omega_{2,\text{TRM}}$ needed as:

$$\Omega_{1,\text{TRM}} = \begin{cases} |\delta_{\text{TRM}}| + \Omega_{2,\text{TRM}} \\ \frac{\pi}{2} - \frac{M |\delta_{\text{TRM}}|}{M - 1} & \Omega_{2,\text{TRM}} = \begin{cases} \frac{\pi}{2} + \frac{|\delta_{\text{TRM}}|}{M - 1} & \text{if } M < 1 \\ |\delta_{\text{TRM}}| + \Omega_{1,\text{TRM}} & \text{if } M > 1 \end{cases}$$
(2.16)

The value of the modulation angles δ , Ω_1 and Ω_2 in both modulation methods is represented in Fig. 2.10 along with the boundaries previously established. The aforementioned combined TPS-TPM and TRM strategy is possible thanks to the continuity in the values

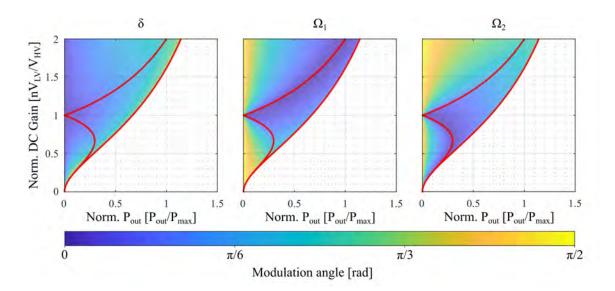


Figure 2.10 Modulation angles δ , Ω_1 and Ω_2 in combined TPS-TPM and TRM

of δ , Ω_1 and Ω_2 that exists in the transition between these modulation methods. Furthermore, the values presented for Ω_1 and Ω_2 are quasi-symmetrical between them in the intervals [0,1] and $[1,\infty]$ of y-axis. Therefore, it is possible to observe that Ω_1 is higher when the converter is working at $V_{\rm HV} > n V_{\rm LV}$, i.e. M<1, while the oposite trend describe the behavior of Ω_2 . However, the largest values of δ are found at TPS-TPM, and it is constantly reduced as soon as it approaches to TPS-TRM.

Finally, the PWL functions that describe the current waveform that flow through the power transformer in both TPS-TPM and TPS-TRM (for M>1) are presented in (2.17) and (2.18) respectively:

$$i_{L\sigma}(t) = \begin{cases} \frac{I_{sw2}}{T_1}t & 0 \le t \le T_1\\ I_{sw2} + \frac{I_{sw1} - I_{sw2}}{T_2}(t - T_1) & T_1 \le t \le (T_1 + T_2)\\ I_{sw1} - \frac{I_{sw1}}{T_3}(t - (T_1 + T_2)) & (T_1 + T_2) \le t \le T_{sw}/2 \end{cases}$$
(2.17)

$$i_{L\sigma}(t) = \begin{cases} \frac{I_{sw2}}{T_1} t & 0 \le t \le T_1 \\ I_{sw2} - \frac{I_{sw2}}{T_2} (t - T_1) & T_1 \le t \le (T_1 + T_2) \end{cases}$$
(2.18)

As well as in SPS Rectangular modulation, T_1 , T_2 and T_3 are the time intervals of each modulation, which are presented in Fig. 2.11 for these TPS modulation methods. In this case, the drain-source voltage and drain current waveforms are depicted for each halfbridge, since the current distribution is not equal in the half-bridge branches of primary and secondary side. As presented in the states of these modulation methods, two of these branches turn-off in hard switching (S_{3-4} and S_{5-6}), while the switching losses due to voltage-current crossover are zero in the remaining devices (S_{1-2} and S_{7-8}) when considering TPS - TPM in forward mode power transfer. In the case of TPS - TRM, there is only one hard switch turn-off transition in S_{5-6} when working in forward-boost mode, while this losses occur in S_{3-4} when working in forward-buck mode.

The equations to determine the time intervals in TPS-TPM in forward mode power transfer are given in (2.19):

$$T_1 = \frac{L_{\sigma}}{V_{\rm HV}} I_{\rm sw2} \ , \ T_2 = \frac{T_{\rm sw}}{2} - 2 T_{\Omega_1} - 2 T_{\Omega_2} \ , \ T_3 = \frac{L_{\sigma}}{n V_{\rm LV}} I_{\rm sw1} \ , \tag{2.19}$$

being the switching currents $(I_{sw1} \text{ and } I_{sw2})$ defined by (2.20):

$$I_{\rm sw1} = \frac{n \, V_{\rm LV} \, (|\delta| - \Omega_2 + \Omega_1)}{2 \, \pi \, f_{\rm sw} \, L_{\sigma}} \, , \quad I_{\rm sw2} = \frac{V_{\rm HV} \, (|\delta| - \Omega_1 + \Omega_2)}{2 \, \pi \, f_{\rm sw} \, L_{\sigma}} \, . \tag{2.20}$$

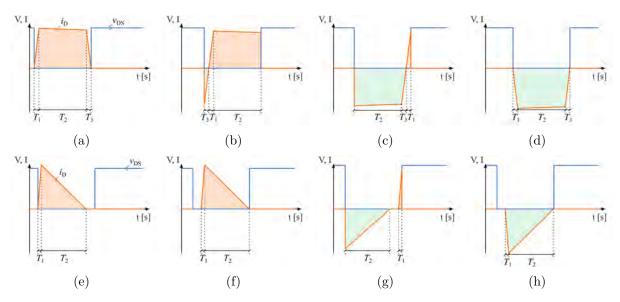


Figure 2.11 Drain to source voltage and drain current waveforms in DAB power devices in TPS modulations (forward power transfer): a) S_{1-2} and D_{1-2} , b) S_{3-4} and D_{3-4} , c) S_{5-6} and D_{5-6} , and d) S_{7-8} and D_{7-8} (TPS-TPM), e) S_{1-2} and D_{1-2} , f) S_{3-4} and D_{3-4} , g) S_{5-6} and D_{5-6} , and h) S_{7-8} and D_{7-8} (TPS-TRM, M>1).

Furthermore, the corresponding times to the modulation angles δ , Ω_1 and Ω_2 in both TPS-TPM and TPS-TRM are:

$$T_{\delta} = \frac{|\delta|}{2\pi f_{\rm sw}} , \quad T_{\Omega_1} = \frac{\Omega_1}{2\pi f_{\rm sw}} , \quad T_{\Omega_2} = \frac{\Omega_2}{2\pi f_{\rm sw}} .$$
 (2.21)

The time intervals are different for buck and boost modes when considering TPS-TRM in forward and/or backward power transfer. In (2.22) and (2.23) the equations to compute these times in forward-boost and forward-buck modes respectively:

$$T_{1} = \frac{L_{\sigma}}{V_{\rm HV}} I_{\rm sw2} , \quad T_{2} = \frac{L_{\sigma}}{|V_{\rm HV} - n \cdot V_{\rm LV}|} I_{\rm sw2} , \qquad (2.22)$$

$$T_1 = \frac{L_{\sigma}}{|V_{\rm HV} - n \, V_{\rm LV}|} \, I_{\rm sw1} \ , \ T_2 = \frac{L_{\sigma}}{n \, V_{\rm LV}} \, I_{\rm sw1} \ . \tag{2.23}$$

where the corresponding switching currents I_{sw1} (buck mode) and I_{sw2} (boost mode) are calculated with (2.24):

$$I_{\rm sw1} = \frac{n V_{\rm LV} |\delta|}{\pi f_{\rm sw} L_{\sigma}} , \quad I_{\rm sw2} = \frac{V_{\rm HV} |\delta|}{\pi f_{\rm sw} L_{\sigma}} . \qquad (2.24)$$

Finally, the analytical models to determine the RMS and AVG currents in power devices while working in these combined TPS-TPM and TRM are gathered in Table 2.2 and Table 2.3.

Switch	RMS	AVG
S ₁₋₂	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\frac{I_{\rm sw2}^2}{3}T_1 + \frac{I_{\rm sw1}^2 + I_{\rm sw2}^2 + I_{\rm sw1}I_{\rm sw2}}{3}T_2 + \frac{I_{\rm sw1}^2}{3}T_3\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{I_{\rm sw2}}{2} T_1 + \frac{I_{\rm sw1} + I_{\rm sw2}}{2} T_2 + \frac{I_{\rm sw1}}{2} T_3\right)$
S_{3-4}	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{I_{\rm sw2}^2}{3} T_1 + \frac{I_{\rm sw1}^2 + I_{\rm sw2}^2 + I_{\rm sw1} I_{\rm sw2}}{3} T_2\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{I_{\rm sw2}}{2} T_1 + \frac{I_{\rm sw1} + I_{\rm sw2}}{2} T_2\right)$
S_{5-6}	$\sqrt{\left(rac{1}{T_{ m sw}} ight) rac{{I_{ m sw2}}^2}{3}T_1}$	$\left(rac{1}{T_{ m sw}} ight) rac{I_{ m sw2}}{2} T_1$
D ₃₋₄	$\sqrt{\left(rac{1}{T_{ m sw}} ight) rac{{I_{ m sw1}}^2}{3}T_3}$	$\left(rac{1}{T_{ m sw}} ight) rac{I_{ m sw1}}{2} T_3$
D_{5-6}	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{I_{\rm sw1}^2 + I_{\rm sw2}^2 + I_{\rm sw1} I_{\rm sw2}}{3} T_2 + \frac{I_{\rm sw1}^2}{3} T_3\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{I_{\rm sw1} + I_{\rm sw2}}{2} T_2 + \frac{I_{\rm sw1}}{2} T_3\right)$
D ₇₋₈	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\frac{I_{\rm sw2}^2}{3}T_1 + \frac{I_{\rm sw1}^2 + I_{\rm sw2}^2 + I_{\rm sw1}I_{\rm sw2}}{3}T_2 + \frac{I_{\rm sw1}^2}{3}T_3\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{I_{\rm sw2}}{2} T_1 + \frac{I_{\rm sw1} + I_{\rm sw2}}{2} T_2 + \frac{I_{\rm sw1}}{2} T_3\right)$

Table 2.2 Analytical models of the RMS and AVG currents referred to primary side in TPS-TPM. Forward power transfer (HVDC to LVDC).

Table 2.3 RMS and AVG current equations referred to primary in TPS-TRM. Forward power transfer (HVDC to LVDC).

	Switch	RMS	AVG
	S_{1-4}	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\frac{I_{\rm sw2}^2}{3}T_1 + \frac{I_{\rm sw2}^2}{3}T_2\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{I_{\rm sw2}}{2} T_1 + \frac{I_{\rm sw2}}{2} T_2\right)$
	S_{5-6}	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \frac{I_{\rm sw2}^2}{3} T_1}$	$\left(\frac{1}{T_{\rm sw}}\right) \frac{I_{\rm sw2}}{2} T_1$
M > 1	D_{5-6}	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \frac{I_{\rm sw2}^2}{3} T_2}$	$\left(\frac{1}{T_{\rm sw}}\right)\frac{I_{\rm sw2}}{2}T_2$
	D ₇₋₈	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\frac{I_{\rm sw2}^2}{3}T_1 + \frac{I_{\rm sw2}^2}{3}T_2\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{I_{\rm sw2}}{2} T_1 + \frac{I_{\rm sw2}}{2} T_2\right)$
M < 1	S ₁₋₂	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\frac{I_{\rm sw1}^2}{3}T_1 + \frac{I_{\rm sw1}^2}{3}T_2\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{I_{\rm sw1}}{2} T_1 + \frac{I_{\rm sw1}}{2} T_2\right)$
	S ₃₋₄	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \frac{I_{\rm sw1}^2}{3} T_1}$	$\left(\frac{1}{T_{\rm sw}}\right) \frac{I_{\rm sw1}}{2} T_1$
	D ₃₋₄	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \frac{I_{\rm sw1}^2}{3} T_2}$	$\left(\frac{1}{T_{\rm sw}}\right) \frac{I_{\rm sw1}}{2} T_2$
	D ₅₋₈	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\frac{I_{\rm sw1}^2}{3}T_1+\frac{I_{\rm sw1}^2}{3}T_2\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{I_{\rm sw1}}{2} T_1 + \frac{I_{\rm sw1}}{2} T_2\right)$

2.2.3 Analytical Models for DC-bus Capacitors

During this thesis, the analytical models that describe the RMS and AVG currents that flow through the power devices have been presented for SPS Rectangular modulation, TPS-TPM and TPS-TRM. In this section, the analytical models of the RMS currents and peak-to-peak voltage ripple in HVDC and LVDC capacitors are presented.

2. BIDIRECTIONAL ISOLATED DC/DC PECS

To determine the analytical models of RMS current and voltage ripple in input and output capacitors, Kirchhoff current law is applied in the positive terminal of these components. Considering HVDC to LVDC power transfer, full-bridge inverter and rectifier stages input (i_{in}) and output (i_{out}) currents can be defined as in Fig. 2.12. Then, the corresponding definition of RMS current and voltage ripple in the input DC-link capacitor are presented in (2.25) and (2.26):

$$I_{C_{HV(RMS)}} = \sqrt{\int_{0}^{T_{\delta}} (I_{HV} - i_{in})^2 dt} + \int_{T_{\delta}}^{T_{SW}/2} (I_{HV} - i_{in})^2 dt , \qquad (2.25)$$

$$\Delta V_{\mathcal{C}_{\mathrm{HV}(\mathrm{pk-pk})}} = \frac{\int_{0}^{T_{\mathrm{Charge}}} (I_{\mathrm{HV}} - i_{\mathrm{in}}) dt}{C_{\mathrm{HV}}} .$$
(2.26)

In (2.26), the definite integral of the current during the charging time (T_{Charge}) is the charge stored in the capacitor, commonly defined as the product between voltage across capacitor and capacitance. By solving these integrals, the analytical models presented in this section are obtained for input capacitor. Furthermore, the input and/or output rectifier currents can be defined with piece-wise linear functions, resulting on the current waveforms depicted in Fig. 2.13. This procedure is also carried out for output capacitor.

Depending on the modulation method, the cases to define the RMS current and peakto-peak voltage ripple are defined as:

• SPS Rectangular modulation:

Case 1: $I_{SW1} > I_{HV}$ and $I_{SW2} > I_{HV}$ for input capacitor, $n I_{SW1} > I_{LV}$ and $n I_{SW2} > I_{LV}$ for output capacitor.

Case 2: $I_{SW1} < I_{HV}$, $I_{SW2} > I_{HV}$ and $|I_{SW1}| > I_{HV}$ for input capacitor, $n I_{SW1} < I_{LV}$ and $n I_{SW2} > I_{LV}$ for output capacitor.

Case 3: $I_{SW1} < 0$ and $|I_{SW1}| > I_{HV}$ for input capacitor, $n I_{SW1} > I_{LV}$ and $n I_{SW2} < I_{LV}$ for output capacitor.

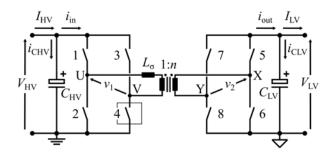


Figure 2.12 DAB schematic with the currents of interest for the mathematical modeling.

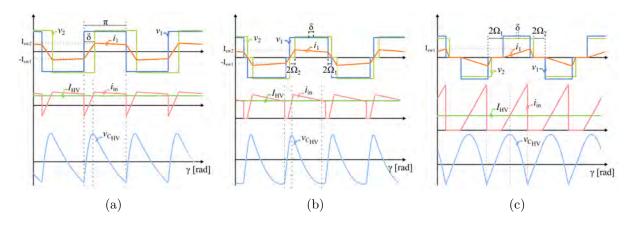


Figure 2.13 Main current and voltage waveforms of DAB converter: a), b) and c) are the primary and secondary voltage $(v_1 \& v_2)$ and primary current (i_1) in SPS Rectangular, TPS-TPM and TPS-TRM respectively, together with the input currents $(I_{\rm HV} \& i_{\rm in})$ and voltage ripple $(v_{C_{\rm HV}})$ in these modulation methods. Forward mode power transfer (from HV to LV).

Case 4: $I_{SW1} > I_{HV}$ and $I_{SW2} < I_{HV}$, for input capacitor, and no distinction on output capacitor.

• Combined TPS-TPM and TPS-TRM:

Case 1: $I_{SW1} > I_{HV}$ and $I_{SW2} > I_{HV}$ for input capacitors, $n I_{SW1} > I_{LV}$ and $n I_{SW2} > I_{LV}$ for output capacitors.

Case 2: $I_{SW1} < I_{HV}$ and $n I_{SW2} > I_{HV}$ for input capacitors, $n I_{SW1} < I_{LV}$ and $n I_{SW2} > I_{LV}$ for output capacitors.

Case 3: $I_{SW1} > I_{HV}$ and $I_{SW2} < I_{HV}$ for input capacitors, $n I_{SW1} > I_{LV}$ and $n I_{SW2} < I_{LV}$ for output capacitors.

In order to simplify the equations presented in this section, the parameters defined in Table 2.4 are presented. Then, these results show a good matching between analytical and simulation values.

Finally, the analytical models of the RMS current and peak-to-peak voltage ripple in HVDC and LVDC capacitors are summarized in Table 2.5, 2.6 and 2.7 for the modulation methods considered in this work.

Table 2.4 Definition of key parameters for the simplification of the analytical models of the RMS current and peak-to-peak voltage ripple in input and output capacitors.

Parameter	Value	Parameter	Value
A_1	$I_{\rm SW1} + I_{\rm HV}$	A_2	$n I_{\rm SW2} + I_{\rm LV}$
B_1	$I_{\rm SW1} + I_{\rm SW2}$	B_2	$n I_{\rm SW1} + n I_{\rm SW2}$
C_1	$I_{\rm SW1} - I_{\rm HV}$	C_2	$n I_{\rm SW1} - I_{\rm LV}$
D_1	$I_{\rm SW2} - I_{\rm HV}$	D_2	$n I_{\rm SW2} - I_{\rm LV}$
E_1	$I_{\rm SW1} - I_{\rm SW2}$	E_2	$n I_{\rm SW1} - n I_{\rm SW2}$

Modulation	Case	$\Delta V_{ m C_{HV(pk-pk)}}$	$\Delta V_{ m C_{LV(pk-pk)}}$
	1	$\frac{0.5{A_1}^2L_\sigma}{C_{\rm HV}\left(V_{\rm HV}+nV_{\rm LV}\right)}$	$rac{0.5{A_2}^2\left(L_{\sigma}/n^2 ight)}{C_{ m LV}\left(V_{ m HV}/n+V_{ m LV} ight)}$
SPS	2	$\frac{D_1{}^2 L_\sigma n V_{\rm LV}}{C_{\rm HV} \left(\left(n V_{\rm LV} \right)^2 - V_{\rm HV}{}^2 \right)}$	$rac{0.5{D_2}^2\left(L_\sigma/n^2 ight)}{C_{ m LV}\left(V_{ m LV}-V_{ m HV}/n ight)}$
	3	$rac{0.5 \mid A_1 \mid^2 L_{\sigma}}{C_{ m HV} \; (n V_{ m LV} - V_{ m HV})}$	$\frac{0.5 C_2^2 (L_{\sigma}/n^2) (2 V_{\rm HV}/n)}{C_{\rm LV} ((V_{\rm HV}/n)^2 - V_{\rm LV}^2)}$
	4	$\frac{0.5 C_1{}^2 L_\sigma}{C_{\rm HV} (V_{\rm HV} - n V_{\rm LV})}$	
	1	$\frac{0.5 D_1{}^2 (L_{\sigma}/V_{\rm HV}) + (0.5 E_1 + C_1) T_2}{C_{\rm HV}}$	$\frac{(0.5 E_2 + C_2) T_2 + C_2^2 (L_{\sigma}/V_{\rm LV})}{C_{\rm LV}}$
TPS-TPM	2	$rac{0.5{D_1}^2L_{\sigma}nV_{ m LV}}{C_{ m HV}V_{ m HV}(nV_{ m LV}-V_{ m HV})}$	$rac{0.5{D_2}^2\left(L_\sigma/n^2 ight)}{C_{ m LV}\left(V_{ m LV}-V_{ m HV}/n ight)}$
	3	$rac{0.5{C_1}^2L_\sigma}{\overline{C_{ m HV}\left(V_{ m HV}-nV_{ m LV} ight)}}$	$\frac{0.5 {C_2}^2 \left(L_\sigma/n^2\right) (V_{\rm HV}/n)}{C_{\rm LV} V_{\rm LV} (V_{\rm HV}/n-V_{\rm LV})}$
TPS-TRM	1	$\frac{0.5 {D_1}^2 L_\sigma n V_{\rm LV}}{C_{\rm HV} V_{\rm HV} \left(n V_{\rm LV} - V_{\rm HV} \right)}$	$\frac{0.5 {D_2}^2 \left(L_\sigma/n^2\right)}{C_{\rm LV} \left(V_{\rm LV}-V_{\rm HV}/n\right)}$
	2	$\frac{0.5 C_1{}^2 L_{\sigma}}{C_{\rm HV} (V_{\rm HV} - n V_{\rm LV})}$	$\frac{0.5 C_2^2 (L_{\sigma}/n^2) (V_{\rm HV}/n)}{C_{\rm LV} V_{\rm LV} (V_{\rm HV}/n - V_{\rm LV})}$

 ${\bf Table \ 2.5 \ Voltage \ ripple \ in \ input \ and \ output \ capacitor \ (power \ transfer \ from \ HVDC \ to \ LVDC)}$

Modulation	Case	$I_{ m RMS}$
	ZVS	$\sqrt{(2 f_{sw}) \left((A_1^2 + B_1^2/3 - A_1 B_1) (T_1 + T_2) + (D_1^2 + E_1^2/3 + D_1 E_1) T_3 \right)}$
SPS	$I_{\rm SW1} < 0$	$\sqrt{(2 f_{sw}) \left((A_1^2 + B_1^2/3 - A_1B_1) T_1 + (D_1^2 + E_1^2/3 + D_1E_1) (T_2 + T_3) \right)}$
	$I_{\rm SW2} < 0$	V(25sw)((11 + 21 / 0 - 1121)(11 + (21 + 21 / 0 + 2121)(12 + 13))
TPS-TPM	-	$\sqrt{\left(2f_{\rm sw}\right)\left(\left(I_{\rm SW2}^2/3 - I_{\rm HV}D_1\right)T_1 + \left(D_1{}^2 + E_1{}^2/3 + D_1E_1\right)T_2 + I_{\rm HV}{}^2T_3\right)}$
TPS-TRM	$V_{\rm HV} < n V_{\rm LV}$	$\sqrt{(2 f_{\rm sw}) \left((I_{\rm SW2}^2/3 - I_{\rm HV} D_1) T_1 + (D_1^2 + I_{\rm SW2}^2/3 + D_1 I_{\rm SW2}) T_2 + I_{\rm HV}^2 T_3 \right)}$
	$V_{\rm HV} > n V_{\rm LV}$	$\sqrt{\left(2 f_{\rm sw}\right) \left(\left(I_{\rm HV}^2 + I_{\rm SW1}^2/3 - I_{\rm HV} I_{\rm SW1}\right) T_1 + \left(I_{\rm HV}\right)^2 \left(T_2 + T_3\right)\right)}$

Table 2.7 RMS Current in output capacitor (power transfer from HVDC to LVDC))
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Modulation	Case	$I_{ m RMS}$
	ZVS	$\sqrt{(2 f_{sw})((C_2{}^2 + B_2{}^2/3 - C_2 B_2)(T_1 + T_2) + (D_2{}^2 + E_2{}^2/3 + D_2 E_2)T_3)}$
SPS	$I_{\rm SW1} < 0$	$\sqrt{\left(2f_{\rm sw}\right)\left(\left(C_2{}^2+B_2{}^2/3-C_2B_2\right)T_1+\left(D_2{}^2+E_2{}^2/3+D_2E_2\right)\left(T_2+T_3\right)\right)}$
	$I_{\rm SW2} < 0$	$\bigvee (2 j_{SW}) ((02 + D_2 / 0 + 02 D_2) 11 + (D_2 + D_2 / 0 + D_2 D_2) (12 + 13))$
TPS-TPM	-	$\sqrt{(2 f_{\rm sw}) \left(I_{\rm LV}^2 T_1 + \left(D_2^2 + E_2^2 / 3 - D_2 E_2 \right) T_2 + \left(C_2^2 + \left(n I_{\rm SW1} \right)^2 / 3 - C_2 n I_{\rm SW1} \right) T_3 \right)}$
TPS-TRM	$V_{\rm HV} < n V_{\rm LV}$	$\sqrt{(2 f_{\rm sw}) \left(I_{\rm LV}^2 (T_1 + T_3) + \left(D_2^2 + (n I_{\rm SW2})^2 / 3 - D_2 n I_{\rm SW2} \right) T_2 \right)}$
	$V_{\rm HV} > n V_{\rm LV}$	$\sqrt{\left(2 f_{\rm sw}\right) \left(\left(\left(n I_{\rm SW1}\right)^2 / 3 - I_{\rm LV} C_2\right) T_1 + \left(C_2{}^2 + \left(n I_{\rm SW1}\right)^2 / 3 - C_2 n I_{\rm SW1}\right) T_2 + I_{\rm LV}{}^2 T_3\right)}$

2.2.4 Time Domain Analysis for IPOP DAB

To conclude with the analytical modeling of DAB converter, the time domain equations that describe the voltage and current waveforms through the different components are presented in this section for IPOP DAB configurations working in interleaving based on the models gathered in [50]. A schematic of IPOP DAB is depicted in Fig. 2.14(a). These structures are formed by multiple DAB whose input and output ports are connected in parallel. The power processed by each converter is the nominal power that is specified by the application divided by the number of parallel converters ($N_{\rm p(DAB)}$).

The main benefit of IPOP DAB configurations in MEA applications lies in the ability to work by interleaving the operation of these converters, reducing the resulting current and voltage ripple on the LVDC capacitor. As shown in Fig. 2.14(b), the interleaving operation is done by applying an interleave phase shift angle (φ) between the modulation angle δ of the gate signals of each converter. The gate signals in each full-bridge are presented for a couple of power devices whose on state is synchrounous (S₁ and S₄ in HVDC side, S₅ and S₈ in the LVDC side). The degrees of freedom to set the interleaving angle

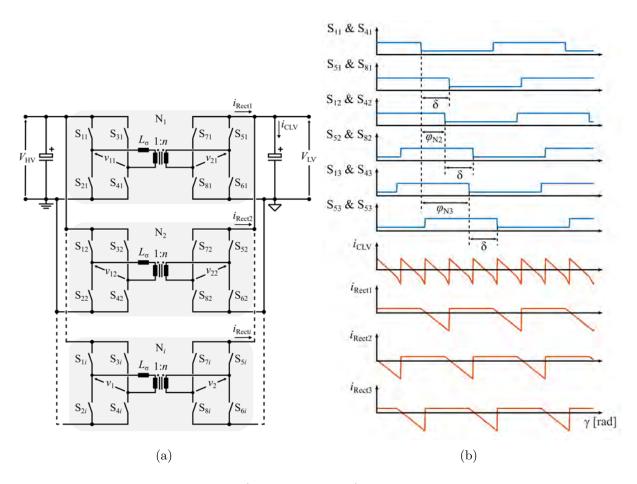


Figure 2.14 IPOP DAB converter: a) schematic and b) gate signals, output capacitor current, and rectifier output currents when working with SPS Rectangular modulation and considering $N_{p(DAB)} = 3$.

 (φ) , which increase with the number of power converters considered, are high. Therefore, in this work the interleaving angle in each paralleled converter (φ_{Ni}) is determined with (2.27):

$$\varphi_{\mathrm{N}i} = N_{i-1} \varphi \quad . \tag{2.27}$$

This assumption leads in most cases to non-rectangular, trapezoidal or triangular (depending on the modulation method) current waveforms flowing through the output capacitor, in which the resulting current and/or voltage ripples are reduced. Nevertheless, at certain values of the interleaving angle, i.e. $\varphi = \pi/N_{\rm p(DAB)}$ and its multiples, the frequency of the capacitor current waveform is increased in a factor equal to the number of paralleled converters [109]. This phenomena is represented in Fig. 2.15 for $N_{\rm p(DAB)} = 3$, where the frequency of the LVDC capacitor current ($i_{\rm CLV}$) is three times the frequency of the output current in the rectifier stages ($i_{\rm Rect1}$, $i_{\rm Rect2}$ and $i_{\rm Rect3}$). Hereinafter, the analytical model IPOP DAB for *i* converters working in parallel is detailed. This model helps to analyze the impact of the interleaving angle on the resulting RMS current in all components of the converter in different modulation methods, likewise to aid in the design procedure.

Fourier Analysis

Using the AC equivalent circuit of the *i*th DAB and the phasor diagram that define its behavior exposed in Fig. 2.15, the voltages on primary and secondary sides of the power transformer of the *i*th converter are defined as:

$$v_1^i(t) = \sum_{h=1}^{\infty} V_1^h \sin\left(h(\omega t + \delta - \varphi_{\mathrm{N}i})\right) \quad , \tag{2.28}$$

$$v_2^i(t) = \sum_{h=1}^{\infty} V_2^h \sin(h(\omega t - \varphi_{Ni}))$$
, (2.29)

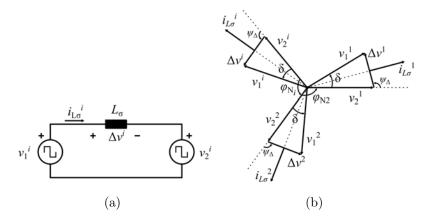


Figure 2.15 (a) AC equivalent circuit of the ith DAB converter and (b) phasor diagram.

where V_1^h and V_2^h are the amplitudes of the *h*th harmonic, which are computed with (2.30) and (2.31):

$$V_1^h = V_{\rm HV} \frac{2}{h\pi} \cos(h\,\Omega_1) \left(1 - \cos(h\pi)\right) \quad , \tag{2.30}$$

$$V_2^h = V_{\rm LV} \, \frac{2}{h \, \pi} \cos \left(h \, \Omega_2\right) \left(1 - \cos \left(h \, \pi\right)\right) \quad . \tag{2.31}$$

Then, the voltage difference in the AC link of the hth harmonic in the ith converter the voltage drop in the decoupling inductance is determined:

$$\Delta v^{i}(t) = \sum_{h=1}^{\infty} \Delta V^{h} \cos\left(h\left(\omega t - \varphi_{\mathrm{Ni}}\right) + \psi_{\Delta}\right) \quad , \qquad (2.32)$$

where the amplitude of the *h*th harmonic and the phase (ψ_{Δ}) are defined as:

$$\Delta V^{h} = \sqrt{\left(V_{1}^{h}\right)^{2} + \left(V_{2}^{h}\right)^{2} - 2V_{1}^{h}V_{2}^{h}\cos\left(h\,\delta\right)} \quad , \tag{2.33}$$

$$\psi_{\Delta} = \arctan\left(\frac{V_1^h \sin\left(h\,\delta\right)}{V_1^h \cos\left(h\,\delta\right) - V_2^h}\right) - \frac{\pi}{2}\operatorname{sign}\left(V_1^h \cos\left(h\,\delta\right) - V_2^h\right) \quad . \tag{2.34}$$

Finally, the current waveform of the *i*th converter that flows through the L_{σ} is:

$$i_{L\sigma}^{i}(t) = \sum_{h=1}^{\infty} I_{L\sigma}^{h} \sin\left(h\left(\omega t - \varphi_{Ni}\right) + \psi_{\Delta}\right) \quad , \tag{2.35}$$

where the amplitude of the hth harmonic is computed with (2.34):

$$I_{L\sigma}^{h} = \frac{\Delta V^{h}}{2 \pi h f_{\rm sw} L_{\sigma}} \quad . \tag{2.36}$$

With the presented analytical model, voltage and current waveforms in transformer windings can be determined. Moreover, it is possible to establish the current and voltage waveforms in the power devices and input/output capacitors based on these models.

Since volume and weight of output capacitors are the main disadvantage when considering MEA applications, its analytical model is presented below based on the voltage and current waveforms in transformer windings. Therefore, the piece-wise functions of the current waveform in output capacitors are presented for the considered modulation methods.

In SPS rectangular modulation, the voltage in the secondary winding of the power transformer is positive or negative. Therefore, the piece wise function of the rectifier output current waveform in the *i*th converter is determined with (2.37):

$$i_{\text{Rect}}^{i}(t) = \begin{cases} i_{L\sigma}^{i} & \text{if } V_{2}^{i}(t) > 0\\ -i_{L\sigma}^{i} & \text{if } V_{2}^{i}(t) < 0 \end{cases}$$
(2.37)

Then, the current waveform in the output capacitor is defined as:

$$i_{\rm CLV} = \sum_{i=1}^{N_{\rm p}} i_{\rm Rect}^i - \frac{P}{V_{\rm LV}}.$$
 (2.38)

It is important to note that (2.38) is obtained under the assumption of relatively large output capacitor. Thus, the current ripple in the LVDC bus is neglected.

In TPS-TPM and TPS-TRM, the voltage waveform in the secondary side is positive, negative or zero. Thus, the resulting output current waveform of the rectifier stage in the ith converter is computed with (2.39):

$$i_{\text{Rect}}^{i}(t) = \begin{cases} i_{L\sigma}^{i} & \text{if } V_{2}^{i}(t) > 0\\ 0 & \text{if } V_{2}^{i} = 0\\ -i_{L\sigma}^{i} & \text{if } V_{2}^{i}(t) < 0 \end{cases}$$
(2.39)

As in SPS rectangular modulation, the current waveform in the output capacitor is determined by using (2.38). In section 2.4, the validation of the exposed equations based on a simulation model is presented together with the scenarios that enable the utilization of these configurations.

2.3 Active-Bridge-Active-Clamp

As stated along the Chapter 1 of this work, the main disadvantage of DAB converter in MEA applications is the required large capacitance in LVDC bus to satisfy the low voltage ripple requirement [36]. As an alternative to DAB, ABAC converter has been proposed in [36, 37]. With this topology, the large required LVDC capacitance in DAB is reduced due to the inclusion of two output filter inductors working in phase oposition. Moreover, as well as in DAB converter, advanced modulation methods based on TPM and TRM current shapes in transformer windings have been studied in ABAC converter [38, 39]. These modulation methods improve the efficiency of the power converter when working outside unity normalized DC Gain at low power transfer. Furthermore, the influence of the passive components over different output characteristics as current sharing, output voltage ripple and/or output voltage ripple cancellation has been characterized [40].

The schematic of ABAC converter is shown in Fig. 2.16. It is formed by a full-bridge

in the primary stage and two half-bridge branches in the secondary side, which can act as inverter and/or rectifier connected through an isolation transformer. Semiconductors $S_1 - S_4$ and $D_1 - D_4$ connect the primary side of the transformer with the HVDC bus, while the secondary side is connected through $S_5 - S_8$ and $D_5 - D_8$ to the clamp capacitors and the output inductors. These output inductors act as interface between the secondary half-bridges and the LVDC bus.

Nevertheless, one of the main gaps found in literature is the lack of analytical models that aid in the design and understanding of this PEC. Therefore, the equations that describe the behavior while working with SPS Rectangular modulation are presented in this work.

2.3.1 SPS Rectangular Modulation

As in DAB converter, SPS rectangular modulation is the simplest and the most commonly used modulation method among those that can be implemented on this topology. Therefore, its analytical modeling is widely analyzed through this section. In Fig. 2.17, voltage waveforms in primary (v_1) and secondary (v_2) windings of the power transformer are presented togheter with the current waveform flowing through the decoupling inductor $(i_{L\sigma})$. Furthermore, the current through one of the output inductors (i_{Lout}) is exposed, being its phase-opposed current circulating over the other inductor. Therefore, the resulting current ripple before the LVDC bus is canceled.

Looking at the configuration of the secondary side in ABAC converter, RMS and AVG currents in secondary switching devices depend on the currents that flow through the secondary winding of the power transformer and through the output inductors. After applying Kirchhoff current law in nodes X and Y (see Fig. 2.16), the current distribution in the power devices of this stage is obtained. Moreover, the current through topside $(S_{5-7} \text{ and } D_{5-7})$ and bottomside $(S_{6-8} \text{ and } D_{6-8})$ semiconductors is not the same, as it is shown in Fig. 2.15. In order to characterize the RMS and AVG current stress in these

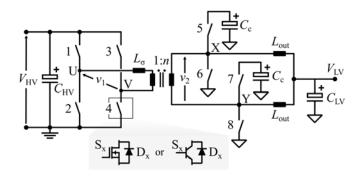


Figure 2.16 Schematic of ABAC converter.

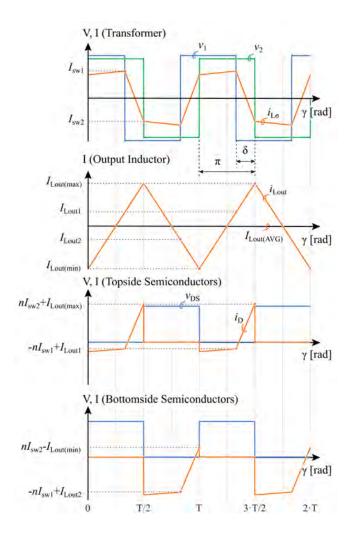


Figure 2.17 Main waveforms in secondary side of ABAC converter under SPS rectangular modulation. From top to bottom: Voltage in primary (v_1) and secondary (v_2) windings of the power transformer and current through decoupling inductor $(i_{L\sigma})$, current through output inductor (i_{Lout}) , and blocking voltage (v_{DS}) and drain current (i_D) in topside $(S_{5-7} \text{ and } D_{5-7})$, and in bottomside $(S_{6-8} \text{ and } D_{6-8})$ semiconductors.

devices, the current levels at $(\pi - \delta)$ and switching instants are defined as A,B,C,D in (2.40) nd (2.41) to simplify the mathematical development of this work:

$$A = (I_{\text{Lout(max)}} + n I_{\text{sw2}}) , B = (I_{\text{Lout(min)}} - n I_{\text{sw2}}) , \qquad (2.40)$$

$$C = (I_{\text{Lout1}} - n I_{sw1}), D = (I_{\text{Lout2}} + n I_{sw1}), \qquad (2.41)$$

where $I_{\text{Lout(max)}}$ and $I_{\text{Lout(min)}}$ are the maximum and minimum current values in the output inductance, and I_{Lout1} and I_{Lout2} are the current in the output inductance at switching instant in primary side. The equations to determine these currents, as well as I_{sw1} and I_{sw2} , are presented from (2.42)-(2.46):

$$I_{\rm sw1} = \frac{V_{\rm HV} \pi + n \, V_{\rm Clamp} \, (2 \, |\delta| - \pi)}{4 \, \pi \, f_{\rm sw} \, L_{\sigma}}, \quad I_{\rm sw2} = \frac{V_{\rm HV} \, (2 \, |\delta| - \pi) + n \, V_{\rm Clamp} \, \pi}{4 \, \pi \, f_{\rm sw} \, L_{\sigma}}, \tag{2.42}$$

$$I_{\text{Lout(max)}} = I_{\text{Lout(AVG)}} + 0.5 \,\Delta I_{\text{Lout(pk-pk)}} \quad , \tag{2.43}$$

$$I_{\text{Lout(min)}} = I_{\text{Lout(AVG)}} - 0.5 \,\Delta I_{\text{Lout(pk-pk)}} \quad , \tag{2.44}$$

$$I_{\text{Lout1}} = I_{\text{Lout(min)}} + \frac{\left(I_{\text{Lout(max)}} - I_{\text{Lout(min)}}\right)}{\pi} (\pi - \delta), \qquad (2.45)$$

$$I_{\text{Lout2}} = I_{\text{Lout(max)}} + \frac{\left(I_{\text{Lout(min)}} - I_{\text{Lout(max)}}\right)}{\pi} (\pi - \delta), \qquad (2.46)$$

being V_{Clamp} the voltage on the clamp capacitors ($V_{\text{Clamp}} = 2 V_{\text{LV}}$). Furthermore, current ripple ratio (r_{I}), peak-to-peak current ripple ($\Delta I_{\text{Lout}(\text{pk}-\text{pk})}$) and AVG current ($I_{\text{Lout}(\text{AVG})}$) in the output inductor are defined regarding the output inductance (L_{out}) in (2.47) and (2.48):

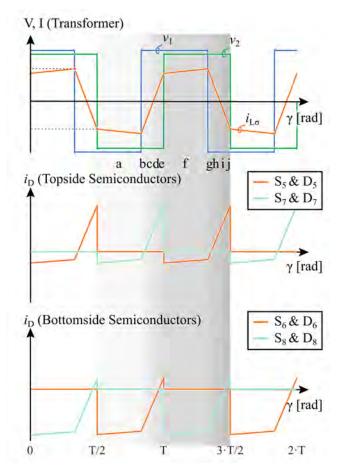
$$I_{\text{Lout}(\text{AVG})} = \frac{P_{\text{out}}}{V_{\text{Clamp}}}, \quad \Delta I_{\text{Lout}(\text{pk-pk})} = \frac{V_{\text{LV}}}{2L_{\text{out}}f_{\text{sw}}}, \quad (2.47)$$

$$r_{\rm I} = \frac{\Delta I_{\rm Lout(pk-pk)}}{I_{\rm Lout(AVG)}} = \frac{(V_{\rm LV})^2}{L_{\rm out} f_{\rm sw} P_{\rm out}}.$$
(2.48)

Since the differences between DAB and ABAC converters are in the rectifier stage, the operating modes defined hereinafter for ABAC converter reveal whether the current is flowing through switch or diode in the secondary side, i.e. positive or negative, at π and $(\pi - \delta)$ instants respectively in topside and bottomside power devices. Therefore, these operating modes describe hard-switching (case I) and ZVS (case II) regions, divided in case I a, case I b, case II a, case II b and case II c.

Considering case II a, the blocking voltage and current waveforms in secondary power devices of the rectifier stage are depicted in Fig. 2.18 together with the voltage and current waveforms in the transformer. These states differ from DAB in the secondary side, where the current through power devices is the result of the Kirchhoff current law on the midpoint of each half-bridge branch. Therefore, the states of the ABAC converter when working with SPS Rectangular modulation are detailed below (see Fig. 2.19):

- State a: In this state primary and secondary voltages are negative, as well as the current flowing through topside and bottomside power devices. The transition from state j to this state produce losses in the turn-off of S₅ and S₈.
- State b: The voltage on primary side of the power transformer becomes positive in this state. Then, turn-off switching losses between states a and b are due to semiconductors S_2 and S_3 .



 $\label{eq:Figure 2.18} {\rm Description \ of \ the \ states \ in \ ABAC \ converter \ when \ working \ with \ SPS \ Rectangular \ modulation.}$

- State c: In this case, the current through the semiconductors connected to the negative terminal of the power transformer becomes positive, which turn-on S₇ without losses.
- State d: Once the current through the transformer turns positive, S₁ and S₂ turn-on switching is lossless.
- State e: Finally, the current that flows through bottomside semiconductor S_6 turns to positive. The turn-on transition of this semiconductor between states d and e is lossless, while turn-off switching losses from state e to state f are due to semiconductors S_6 and S_7 .
- States f-j: The transitions throughout these states is similar to the above described. However, the combination of voltages and current values, positive or negative, in the power transformer is the oposite to the previous states.

The corresponding boundary conditions are presented in Table 2.8 together with the blocking voltage and drain current waveform in power devices of each operating mode.

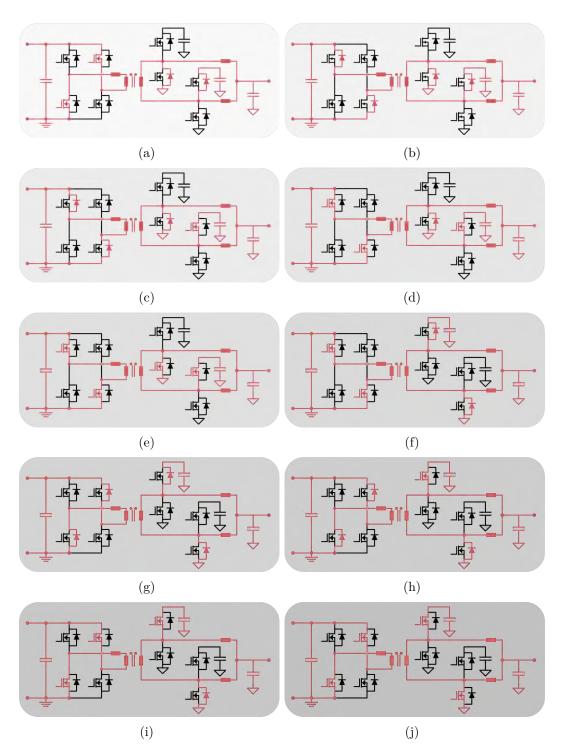


Figure 2.19 States of ABAC converter when working with SPS rectangular modulation.

By equating these boundary conditions to zero and rearranging from above equations the boundaries between the defined cases II and I are gathered below:

$$M_{\rm ABAC1} = \frac{\pi^2 - 2\,\delta^2}{2\,\pi^2 \left(n + \frac{1}{2\,n\,\left(L_{\rm out}/L_{\sigma}\right)}\right)} \quad , \tag{2.49}$$

$$M_{\rm ABAC2} = \frac{\pi (\pi - 2 |\delta|) - 2 |\delta| (\pi - |\delta|)}{2 \pi^2 \left(n + \frac{1}{2 n (L_{\rm out}/L_{\sigma})} \right)} , \qquad (2.50)$$

$$M_{\text{ABAC3}} = \frac{2 |\delta| (\pi - |\delta|) - \pi^2}{2 \pi \left(n (2 |\delta| - \pi) + \frac{\pi - 2 (\pi - |\delta|)}{2 n (L_{\text{out}}/L_{\sigma})} \right)} , \qquad (2.51)$$

$$M_{\text{ABAC4}} = \frac{2 |\delta| (|\delta| - \pi) - \pi^2}{2 \pi \left(n (2 |\delta| - \pi) + \frac{|\delta| - \pi/2}{n (L_{\text{out}}/L_{\sigma})} \right)}$$
(2.52)

Once the corresponding DC gain functions of the ZVS boundaries have been obtained, it is possible to define the operating areas as well as to evaluate the influence of the output inductance over the ZVS boundaries in ABAC. Fig. 2.20 presents the DC gain boundaries of the different cases for ABAC versus the normalized output power. The ZVS area for primary side is the same than the depicted in Fig. 2.5 for DAB, and it is not indicated for clarity. To obtain the ZVS boundaries of the secondary side, an ideal case of infinite output inductance (and thus, $\Delta I_{\text{Lout}(pk-pk)} = 0$) is considered in Fig. 2.20(a), defining the operating area of each case.

However, operating modes of ABAC are modified when a finite output inductance is considered. In Fig. 2.20(b), two different scenarios have been considered. An ideal case, where the output inductance tend to infinite and a finite inductance ($L_{out} = 1 \mu H$). This evaluation exhibits how ZVS boundaries in secondary power devices of ABAC converter vary when the output inductance is decreased. It can be seen that ZVS operating modes appear in buck and boost modes, while hard-switching regions affects on buck mode. Moreover, the influence of hard-switching cases on buck mode is reduced when a finite

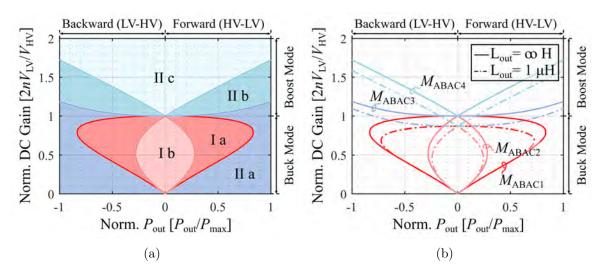


Figure 2.20 (a) Operating modes in the secondary side of ABAC converter. The influence of output inductances (L_{out}) is exposed in (b). To analyze the results regardless the application, output power and DC gain are normalized.

Case	Boundary condition	$v_{DS} \ \& \ i_D \ { m waveforms}$		
I a.	$n I_{\rm sw2} - I_{\rm Lout(min)} \le 0$	$S_{5-7} \& D_{5-7}$ $S_{6-8} \& D_{6-8}$		
I b.	$n I_{\rm sw2} + I_{\rm Lout(max)} \le 0$	V, I t [s] v_{DS} t_{D} t_{D}		
II a.	$\begin{split} -n I_{\mathrm{sw1}} + I_{\mathrm{Lout1}} &\geq 0 \ \& \\ -n I_{\mathrm{sw1}} - I_{\mathrm{Lout2}} &\geq 0 \end{split}$	V, I V, I t [s] V, I v _{DS} v _{DS}		
II b.	$-n I_{\rm sw1} + I_{\rm Lout1} \ge 0$	V, I V, I V, I V, I V, I V DS V DS		
II c.	$-n I_{\rm sw1} - I_{\rm Lout2} \ge 0$	V, I t [s] V, I in t [s]		

Table 2.8 Summary of ZVS and hard-switching cases, boundary conditions, and voltage and currentwaveforms in power devices (Forward mode).

inductance is set. This behavior is symmetric about Y axis. This reduction on the hardswitching operating area is concentrated in the operating points where the normalized DC gain is close to unity. This phenomena is explained by the influence of $V_{\rm LV}$ on the current ripple ($\Delta I_{\rm Lout(pk-pk)}$). The main objective when decreasing the output inductance is to increase the current ripple, which impacts on the switching currents in the power devices of the secondary side. However, this increment is reduced when LVDC starts to decrease, up to the point in which ZVS boundaries are the same for both inductances, and thus no improvements in decreasing its value are found.

Likewise in DAB converter, RMS and AVG currents in power devices have been characterized for ABAC converter. Since the current distribution in the primary side is the same in both converters, the analytical models presented in this work aid to determine the conduction and switching currents stress in the secondary side. In Table 2.9, 2.10, 2.11 and 2.12 the equations of the RMS and AVG currents are summarized. Each case correspond to an operating mode of ABAC, which are described in Table 2.8. Case II b. is not found in tables since the equations that describe its behavior are obtained from cases II a (for bottomside semiconductors) and II c (for topside semiconductors).

Furthermore, the presented models can be utilized for forward (HVDC to LVDC power transfer) and backward (LVDC to HVDC power transfer) operating modes. However, some adaptations must be done in order to adapt these models to backward operation. When the converter works in backward mode, the sign of the current waveform is the opposite of the forward mode. Therefore, the RMS and AVG current stress are calculated by swapping the equations of S_{5-7} with D_{5-7} , and S_{6-8} with D_{6-8} in each operating mode.

Then, the equations gathered in this work aid in the determination of the current stress in the LVDC side power devices of ABAC in both forward and backward operating modes

Switch	RMS	AVG
S_{5-7}	$\sqrt{\left(rac{1}{T_{ m sw}} ight)\left(rac{A^3}{3\;(A-C)} ight)T_{\delta}}$	$\left(rac{1}{T_{ m sw}} ight) rac{A^2}{2 \; (A-C)} T_{\delta}$
S_{6-8}	$\sqrt{\left(rac{1}{T_{ m sw}} ight)\left(rac{B^3}{3\;(B-D)} ight)\;T_\delta}$	$\left(rac{1}{T_{ m sw}} ight) rac{B^2}{2\left(B-D ight)} T_{\delta}$
D ₅₋₇	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\left(\frac{(C-B)^2}{3}+BC\right)\left(\frac{T_{\rm sw}}{2}-T_{\delta}\right)+\frac{C^3}{3\left(C-A\right)}T_{\delta}\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{-\left(C+B\right)}{2} \left(\frac{T_{\rm sw}}{2} - T_{\delta}\right) + \frac{C^2}{2\left(A-C\right)} T_{\delta}\right)$
D ₆₋₈	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\left(\frac{(D-A)^2}{3} + AD\right)\left(\frac{T_{\rm sw}}{2} - T_{\delta}\right) + \frac{D^3}{3(D-B)}T_{\delta}\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{D+A}{2} \left(\frac{T_{\rm sw}}{2} - T_{\delta}\right) + \frac{D^2}{2 \left(D-B\right)} T_{\delta}\right)$

Table 2.9 RMS and AVG current equations in case II a. Forward power transfer (HVDC to LVDC).

Table 2.10 RMS and AVG current equations in case II c. Forward power transfer (HVDC to LVDC).

Switch	RMS	AVG
	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\frac{C^3}{3\ (C-B)}\ \left(\frac{T_{sw}}{2}-T_{\delta}\right)+\left(\frac{(A-C)^2}{3}+A\ C\right)\ T_{\delta}\right)}$	
S_{6-8}	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\frac{D^3}{3\left(D-A\right)}\left(\frac{T_{sw}}{2}-T_{\delta}\right)+\left(\frac{\left(B+D\right)^2}{3}-BD\right)T_{\delta}\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{D^2}{2 \ (A-D)} \ \left(\frac{T_{\rm sw}}{2} - T_{\delta}\right) + \frac{-(B+D)}{2} \ T_{\delta}\right)$
D ₅₋₇	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{B^3}{3 (B-C)}\right) \left(\frac{T_{sw}}{2} - T_{\delta}\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \frac{B^2}{2 \ (C-B)} \left(\frac{T_{sw}}{2} - T_{\delta}\right)$
D ₆₋₈	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\frac{A^3}{3\left(A-D\right)}\right)\left(\frac{T_{sw}}{2}-T_{\delta}\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \frac{A^2}{2 (A-D)} \left(\frac{T_{\rm sw}}{2} - T_{\delta}\right)$

Switch	RMS	AVG
S_{5-7}	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{B^3}{3 \left(B-C\right)} \left(\frac{T_{sw}}{2}-T_{\delta}\right)+\frac{A^3}{3 \left(A-C\right)} T_{\delta}\right)}$	$\left \left(\frac{1}{T_{\rm sw}} \right) \left(\frac{B^2}{2 \left(B - C \right)} \left(\frac{T_{\rm sw}}{2} - T_{\delta} \right) + \frac{A^2}{2 \left(A - C \right)} T_{\delta} \right) \right $
S ₆₋₈	0	0
D ₅₋₇	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{C^3}{3 \ (C-B)} \ \left(\frac{T_{sw}}{2} - T_{\delta}\right) + \frac{C^3}{3 \ (C-A)} \ T_{\delta}\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{C^2}{2 \left(B-C\right)} \left(\frac{T_{\rm sw}}{2} - T_{\delta}\right) + \frac{C^2}{2 \left(A-C\right)} T_{\delta}\right)$
D ₆₋₈	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\left(\left(\frac{(D-A)^2}{3}+DA\right)\left(\frac{T_{sw}}{2}-T_{\delta}\right)+\left(\frac{(B-D)^2}{3}+BD\right)T_{\delta}\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \left(\frac{(A+D)}{2} \left(\frac{T_{sw}}{2} - T_{\delta}\right) + \frac{(B+D)}{2} T_{\delta}\right)$

Table 2.11 RMS and AVG current equations in case I a. Forward power transfer (HVDC to LVDC).

Table 2.12 RMS and AVG current equations in case I b. Forward power transfer (HVDC to LVDC).

Switch	RMS	AVG
S ₅₋₇	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\cdot\left(\frac{B^3}{3\cdot(B-C)}\right)\cdot\left(\frac{T_{sw}}{2}-T_{\delta}\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \cdot \frac{B^2}{2 \cdot (B-C)} \cdot \left(\frac{T_{sw}}{2} - T_{\delta}\right)$
S_{6-8}	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right)\cdot\left(\frac{A^3}{3\cdot(A-D)}\right)\cdot\left(\frac{T_{sw}}{2}-T_{\delta}\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \cdot \frac{A^2}{2 \cdot (D-A)} \cdot \left(\frac{T_{sw}}{2} - T_{\delta}\right)$
D ₅₋₇	$\sqrt{\left(\frac{1}{T_{\rm sw}}\right) \cdot \left(\frac{C^3}{3 \cdot (C-B)} \cdot \left(\frac{T_{sw}}{2} - T_{\delta}\right) + \left(\frac{\left(A-C\right)^2}{3} + A \cdot C\right) \cdot T_{\delta}\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \cdot \left(\frac{C^2}{2 \cdot (B-C)} \cdot \left(\frac{T_{sw}}{2} - T_{\delta}\right) - \frac{A+C}{2} \cdot T_{\delta}\right)$
D ₆₋₈	$\sqrt{\left(\frac{1}{T_{sw}}\right) \cdot \left(\frac{D^3}{3 \cdot (D-A)} \cdot \left(\frac{T_{sw}}{2} - T_{\delta}\right) + \left(\frac{(B-D)^2}{3} + B \cdot D\right) \cdot T_{\delta}\right)}$	$\left(\frac{1}{T_{\rm sw}}\right) \cdot \left(\frac{D^2}{2 \cdot (D-A)} \cdot \left(\frac{T_{sw}}{2} - T_{\delta}\right) + \frac{D+B}{2} \cdot T_{\delta}\right)$

considering all the hard-switching and ZVS cases. Hereafter, these analytical models are utilized to determine the power losses in the inverter and/or rectifier stages, as well as to compare ABAC and DAB converter in different scenarios.

2.4 Simulation Validation

To validate the analytical models presented in this work, a simulation model is developed in PLECS. The design values considered to validate the analytical models are gathered in Table 2.13 for a MEA case study. In order to simplify the validation procedure, the following assumptions are taken. To idealize the simulation model, dead time in switching devices and conduction losses in passive devices are neglected. Furthermore, clamp capacitances are modeled as ideal voltage sources in ABAC converter.

Power Devices

First, input and output voltages are set to the nominal operating point of MEA, i.e. 270 V and 28 V. To transmit 1 kW at 100 kHz of switching frequency, the decoupling inductance is 75.6 μ H when δ_{lim} is set to $\pi/2$. The converters are set to work in all possible operating modes by establishing two different voltages in LVDC side, which are 22 V and 29 V.

In Fig. 2.21, the theoretical and simulation values of the RMS current that flows through the power devices is presented for DAB converter referred to primary side. Two case studies have been considered for the LVDC bus: 29 V [Fig. 2.21(a)] and 22 V [Fig. 2.21(b)]. At high and medium-power transfer, the resulting currents are lower in primary and secondary switches in SPS Rectangular modulation compared with TPS-TPM. However, some exceptions are found in $D_1\&D_2$ and $S_7\&S_8$. At low power transfer, TPS-TRM shows lower current level in all the switching devices, excluding $D_1\&D_2$ and $D_3\&D_4$ in 270/22 case. Furthermore, simulation and analytical values are presented together to evaluate the accuracy of the analytical models extracted in this work. The results show a good correlation between analytical and simulation values, validating the equations presented in this work for DAB converter.

In Fig. 2.22, the theoretical and simulation values of the RMS, AVG and switching currents that flow through the secondary power devices are presented together with the maximum and minimum values of the output inductors. For the operating conditions employed in this work, the RMS and AVG values of the current that flow through the secondary semiconductors are higher in almost all the power range for 270/29 case. This behavior is explained by the low output to decoupling inductance ratio (L_{out}/L_{σ}) . Under the specifications listed in Table 2.13, the difference between the current ripple [see (2.43) and (2.44)] in 270/22 and 270/29 due to the output voltage is considerable, as shown in Fig. 2.22. Furthermore, the switching currents in topside and bottomside semiconductors are also larger at 270/29. Therefore, although this conditions are good to evaluate the precision of the analytical models developed in this work, it is not worthy to operate the converter due to the huge conduction and switching losses that would be originated close to the nominal operating point of MEA applications, i.e. 270/27.

To finalize the validation based on PLECS simulation model, the impact of $t_{\rm dt}$ and $C_{\rm c}$ is analyzed in Fig. 2.23 for ABAC. To this aim, the relative error is presented for different values of these two variables. First, the relative error when $t_{\rm dt}$ is modified from its ideal

Parameter	Symbol	Val	ue	Units
Voltage on HVDC bus	$ $ $V_{\rm HV}$	270)	V
Voltage on LVDC bus	$V_{\rm LV}$	28		V
Switching frequency	$f_{\rm sw}$	100	C	kHz
Limit of the modulation angle	δ_{lim}	$\pi/2$		rad.
Output power	$P_{\rm out}$	1		kW
Decoupling inductance	L_{σ}	75.	6	μH
Dead time	$t_{\rm dt}$	50-3	50	nS
		ABAC	DAB	
Transformer turns ratio	n	5	10	-
Output inductance	$L_{\rm out}$	3	-	μH
Clamp capacitance	$C_{\rm c}$	25-300	-	μF

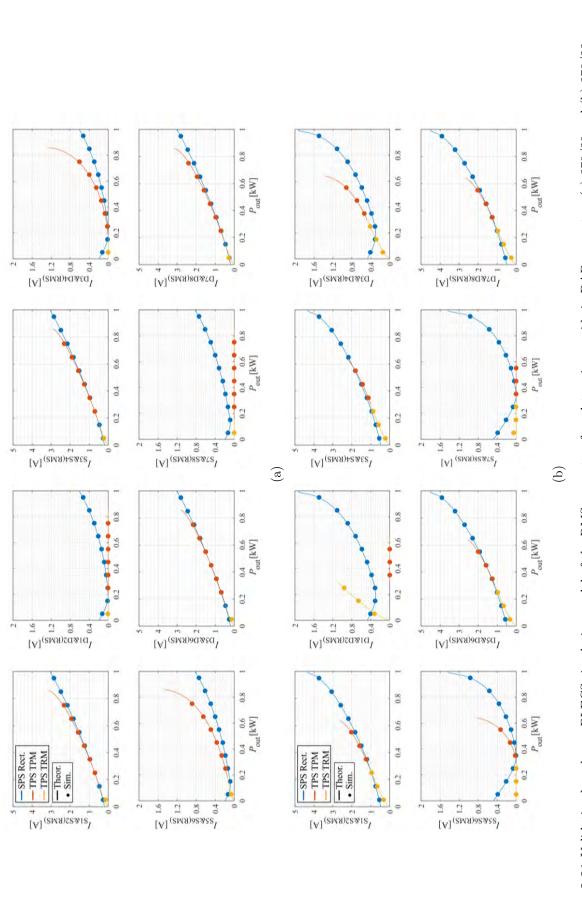
Table 2.13 MEA Design specifications of ABAC and DAB PECs.

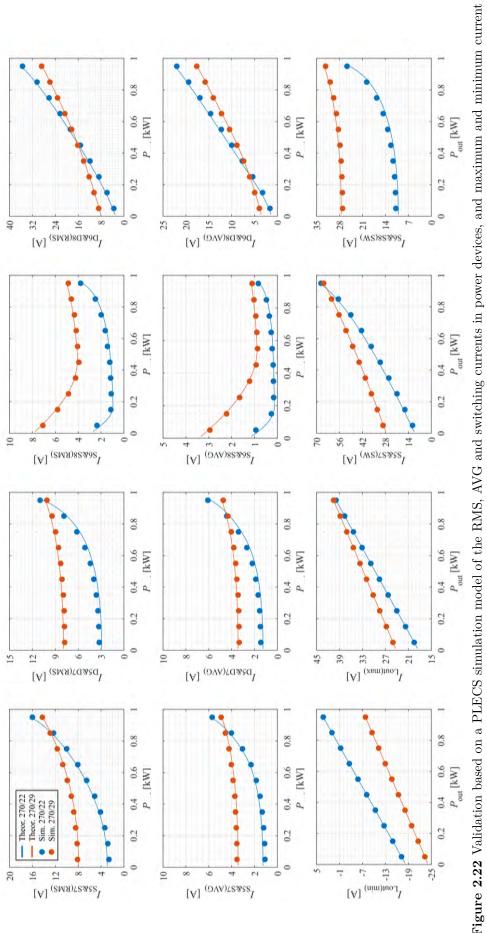
value, i.e. 0 s. The values considered for $t_{\rm dt}$ are 50 ns and 300 ns, which correspond to the 0.5% and 3% of the switching period. It is clear that the influence of $t_{\rm dt}$ on the accuracy of the proposed models is large, especially in semiconductors D_{5-7} and D_{6-8} . This fact is caused by the part of the current waveform that flows through the anti-parallel diode during $t_{\rm dt}$.

To analyze the influence of the C_c on the calculated currents, an analytical model to determine the required capacitance to obtain a desired peak-to-peak voltage ripple has been developed in this work (2.53):

$$C_{\rm c} = \frac{C A \delta}{2 \pi f_{\rm sw} \Delta_{\rm Clamp(pk-pk)} (A - C)} , \qquad (2.53)$$

where $\Delta V_{\text{Clamp}(pk-pk)}$ is the peak-to-peak voltage on the clamp capacitors. The calculated capacitances, i.e. 25 μ F and 300 μ F, correspond to a $\Delta V_{\text{Clamp}(pk-pk)}$ of 0.66 V and 0.05 V respectively, which are the 1.25% and 0.1% of the clamp voltage. This analysis of the C_c reveals that its impact is not significant on the determined RMS and AVG currents.







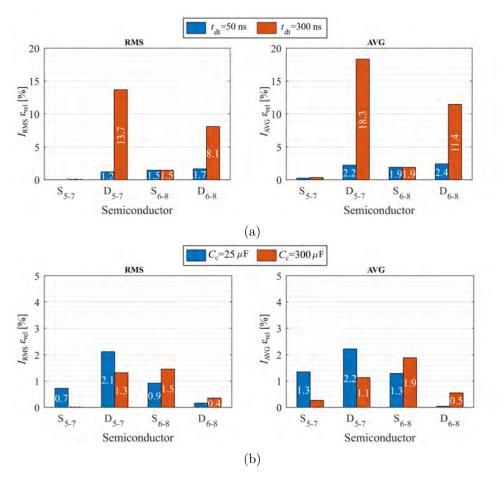


Figure 2.23 Relative error of the analytical models at maximum power transfer considering (a) $t_{\rm dt}$ and (b) $C_{\rm c}$ variations.

The validation detailed in this section expose the good accuracy of the analytical models included in this work. Therefore, the equations extracted are used in Chapter 4 to develop a brute force based optimization algorithm. Furthermore, a deep insight of the mathematical development that have been done to obtain these models is given in section 2.2, as well as the analytical models to determine the peak-to-peak voltage ripple in HVDC and LVDC capacitors of DAB converter in the considered modulation methods.

DC-link capacitors

These models have been validated based on a simulation model developed in PLECS applying the same procedure than in the RMS and AVG currents in power devices. The results of the validation process are presented in Fig. 2.24. It can be noted that, regardless the studied modulation method, the error obtained for the peak-to-peak voltage equations is below the 5%. In the case of the RMS currents, the error reaches the 10 % specially when the converter works close to a unity gain.

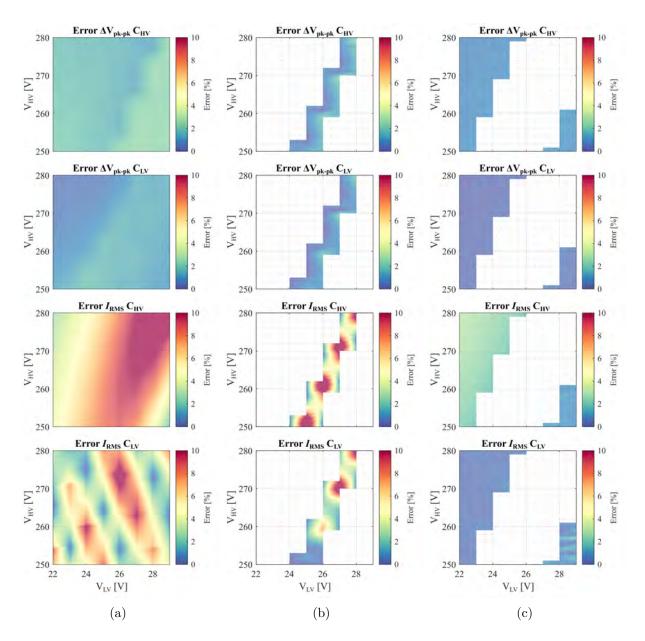


Figure 2.24 Validation of the RMS and peak-to-peak voltage ripple analytical equations presented in this thesis based on a simulation model developed in PLECS: (a) SPS Rectangular modulation, (b) TPS-TPM and (c) TPS-TRM.

IPOP DAB configurations

In Table 2.14, the design specifications utilized in this section are listed. Moreover, SPS rectangular modulation is considered for the design procedure. To determine the corresponding decoupling inductance, the total power transfer P is divided by the number of converters connected in parallel $N_{\rm p}$.

To evaluate the impact of working with different modulation methods, the validation is presented at high, medium and low power transfer. Therefore, the selected power transfer levels are 10, 5 and 1.5 kW when working with SPS rectangular, TPS-TPM and TPS-TRM respectively.

Parameter	Value	Units
$V_{\rm HV}$	270	V
$V_{\rm LV}$	27	V
n	10	-
$N_{\rm p}$	$[2 \ 3 \ 4]$	-
P	10	kW
$f_{\rm sw}$	100	kHz
$\delta_{ m lim}$	70	0
L_{σ}	$[17.32 \ 26 \ 34.65]$	μH
$ \begin{array}{c} L_{\sigma} \\ C_{\rm LV} \end{array} $	3	mF

 Table 2.14 IPOP DAB simulation parameters.

In Fig. 2.25, the RMS current calculated that flows through the output capacitor is shown for different interleaving angles. Regardless the number of paralleled converters, the current stress is symmetric about $\pi/2$. The same trend is observed in all the considered modulations. Furthermore, the minimum current stress in each configuration is found at $\pi/N_{\rm p}$. At high-power transfer, the reduction of the current stress in the global minimum for $N_{\rm p} = 2$ is below the 50 % compared to non-interleaved IPOP DAB, i.e. $\varphi = 0$ rad. However, when the number of converters connected in parallel is increased, the minimum of the normalized current is close to $1/N_{\rm p}$ times the current stress at $\varphi = 0$. This reduction on the current stress slightly increase when working with TPS Trapezoidal at medium power transfer.

Finally, simulation results from PLECS and analytical results computed in MATLAB from the current waveforms are depicted together, showing a good agreement. Main differences between analytical and simulation are found in SPS Rectangular modulation when $N_{\rm p} = 2$ due to the capacitance utilized, which must be higher in this case. Therefore, the analytical models presented in this work are validated.

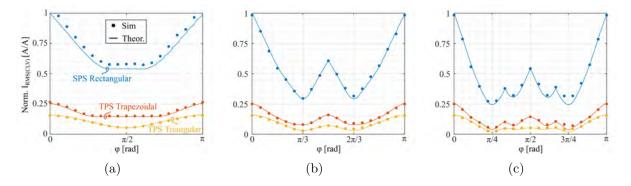


Figure 2.25 RMS current that flows throught output capacitor in interleaved IPOP DAB considering the main modulation methods: (a) $N_{\rm p} = 2$, (b) $N_{\rm p} = 3$ and (c) $N_{\rm p} = 4$.

2.5 Power Losses Analysis

Through this section, the characterization of the power losses in the switching devices of DAB and ABAC PECs based on the analytical models developed in this work is performed. The objective of this study is to analyze the impact of the design variables on the performance of these converters, giving a first outlook of the design trade-offs. The design specifications utilized in this section are gathered in Table 2.13. However, decoupling (ABAC and DAB) and output (ABAC) inductances are modified to determine the influence of the switching frequency, the limit of the modulation angle, and the current ripple ratio of the output inductors on the semiconductor power losses. In each case, the equations (2.2) and (2.48) are utilized to determine these inductances. First, the analytical models to calculate the power losses in the switching devices are presented, together with the required t_{dt} to achieve ZVS. Then, the distribution of the power losses in HVDC and LVDC power devices is presented and compared.

2.5.1 Analytical Models

SiC and Si power devices are considered for the HVDC and LVDC, which are gathered in Table 2.15 and 2.16 respectively together with its main characteristics. The electrical characteristics that are given in these tables define the conduction ($P_{\rm cond}$), dead-time ($P_{\rm dt}$) and switching ($P_{\rm sw}$) losses of each semiconductor. According [131], these losses are determined with (2.54), (2.55) and (2.56) when the parallelization of power devices is contemplated:

$$P_{\rm cond}(@T_{\rm j}) = \frac{R_{\rm DS}(@T_{\rm j})}{N_{\rm sw}} I_{\rm RMS}^{2} , \qquad (2.54)$$

$$P_{\rm dt} = \frac{2 \ (V_{\rm SD} \, I_{\rm sw} \, t_{\rm dt})}{N_{\rm sw}} \, f_{\rm sw} \quad , \tag{2.55}$$

$$P_{\rm sw}(@I_{\rm sw}, V_{\rm DS}) = [E_{\rm on}(@I_{\rm sw}, V_{\rm DS}) + E_{\rm off}(@I_{\rm sw}, V_{\rm DS})] f_{\rm sw} N_{\rm sw} , \qquad (2.56)$$

where $N_{\rm sw}$ is the number of power devices set in parallel and $T_{\rm j}$ is the junction temperature of the device. $P_{\rm dt}$ are the dead-time losses when the turn-on and turn-off free-wheeling voltage drop, switching currents and dead-time are equal. $P_{\rm sw}$ are the switching losses of the power device at the switching current and blocking voltage. The turn-on and turn-off energies ($E_{\rm on}$ and $E_{\rm off}$) are calculated based on approximation models (see Appendix A).

Minimum dead-time for complete ZVS

It is important to take into account that the dead time must be selected considering that the C_{oss} of the power device must be discharged during this time interval. The losses

Parameter	Symbol	1	2	3	4	5	Units
Manufacturer	-	Wolfspeed	Wolfspeed	Infineon	Infineon	Infineon	-
Technology	-	SiC	SiC	SiC	SiC	Si	-
Drain-to-source max. voltage ($@T_j = 25C)$	$V_{\rm DS,max}$	650	650	650	650	650	V
Drain-to-source max. current ($@T_j = 25C)$	$I_{\rm DS,max}$	29	49	26	20	24	A
On resistance ($@T_j = 25C$)	$R_{\rm DS,on}$	60	45	72	107	160	mΩ
Free-wheeling resistance	$R_{\rm SD}$	89	57	71	63	10	mΩ
Free-wheeling voltage drop ($@T_j = 25C, V_{GS} = 0V$)	$V_{\rm SD}$	1.8	2	2	2.1	0.7	V
Output capacitance	C_{oss}	80	101	86	58	1000	pF
Reverse transfer capacitance	$C_{\rm rss}$	9	8	9	7	60	pF
Figure of Merit (FoM)	$(R_{\rm DS,on} C_{\rm oss})^{-1}$	208	220	161	161	6.25	GHz
Package	-	TO-247	TO-247	TO-247	TO-247	TO-247	-
Junction-case thermal resistance	$R_{\rm th,jc}$	0.99	0.85	1.3	1.6	0.31	K/W
Datasheet	-	[121]	[122]	[123]	[124]	[125]	-

 Table 2.15 Electrical and thermal characteristic of the power devices considered in this work (HVDC side).

 Table 2.16 Electrical and thermal characteristic of the power devices considered in this work (LVDC side).

Parameter	Symbol	1	2	3	4	5	Units
Manufacturer	-	Infineon	Infineon	Infineon	Infineon	Infineon	-
Technology	-	Si	Si	Si	Si	Si	-
Drain-to-source max. voltage ($@T_j = 25C)$	$V_{\rm DS,max}$	100	100	55	55	100	V
Drain-to-source max. current ($@T_j = 25C)$	$I_{\rm DS,max}$	120	100	100	80	137	А
On resistance ($@T_j = 25C$)	$R_{\rm DS,on}$	5	3	4.4	6.7	4.5	mΩ
Free-wheeling resistance	$R_{\rm SD}$	16	16	19	22	16	$m\Omega$
Free-wheeling voltage drop ($@T_j = 25C, V_{GS} = 0V$)	$V_{\rm SD}$	0.7	0.7	0.65	0.65	0.7	V
Output capacitance	$C_{\rm oss}$	1600	1940	1330	740	1000	pF
Reverse transfer capacitance	$C_{\rm rss}$	100	69	360	210	60	pF
Figure of Merit (FoM)	$(R_{\rm DS,on} C_{\rm oss})^{-1}$	125	171	171	201	222	GHz
Package	-	TO-220	TO-220	TO-220	TO-220	TO-220	-
Junction-case thermal resistance	$R_{\rm th,jc}$	0.8	0.5	0.5	0.7	0.7	K/W
Datasheet	-	[126]	[127]	[128]	[129]	[130]	-

produced by the energy that is stored in C_{oss} if the selected dead-time is not enough is known in literature as incomplete ZVS (iZVS) [132]. First, it is important to ensure that the inductive energy of the load is higher than the capacitive energies of the device C_{oss} [133]. As detailed in [131], the analytical equation for the calculation of the required t_{dt} to achieve ZVS is adapted for DAB and ABAC converters in (2.57):

$$t_{\rm dt,ZVS} \ge \left(\frac{1}{\omega_{\rm r}}\right) \sin^{-1} \left(\frac{2 V_{\rm DS}}{L_{\sigma} I_{\rm sw} \omega_{\rm r}}\right) ,$$

where $\omega_{\rm r} = \sqrt{\frac{1}{L_{\sigma} C_{\rm oss}}}$ (2.57)

This equation is extracted by solving the circuit shown in Fig. 2.26(a) at the switching instant. To validate the equation of the minimum t_{dt} to achieve ZVS, a simulation model is developed in LTSpice. The inductance (L) of this schematic is determined by solving the well-known equation of the voltage across a inductor to obtain the switching current

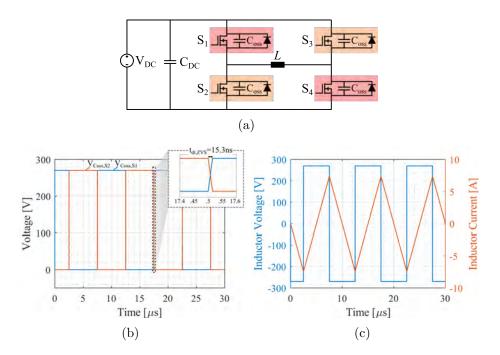


Figure 2.26 Validation of the equation to determine the minimum t_{dt} to achieve ZVS (for HVDC device (2)): (a) schematic of the equivalent circuit, (b) voltage on C_{oss} of the half-bridge formed by $S_1 - S_2$ (zoom at switching instant) and (c) voltage and current on the inductive load.

of DAB and ABAC considering the specifications of Table 2.13. Then, the voltage across the C_{oss} of the half-bridge formed by $S_1 - S_2$ is analyzed, determining the rising and/or falling time of these waveforms, i.e. minimum required t_{dt} to achieve complete ZVS [see Fig. 2.26(b)]. Furthermore, the voltage and current on the inductive load is presented in Fig. 2.26(c) to ensure that the simulation and theoretical switching current is the same.

The validation of this equation is presented in Fig. 2.27(a) (2) power device of HVDC and LVDC sides) for different limits of the modulation angle (δ_{lim}). In Fig. 2.27(b), the minimum t_{dt} to achieve ZVS in 2) device of HVDC side is presented when f_{sw} and δ_{lim} are varied. These two variables modify the reactive power (δ_{lim}), and thus impact on

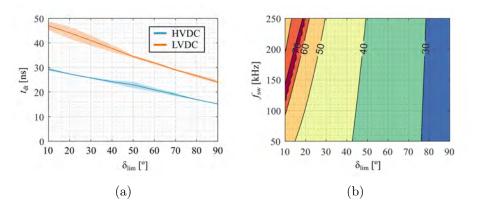


Figure 2.27 Validation of the equation to determine the minimum t_{dt} to achieve ZVS (2) power devices): (a) standard deviation of t_{dt} , (b) minimum t_{dt} to achieve ZVS in HVDC side.

the switching current, and the resulting decoupling inductance (both f_{sw} and δ_{lim}). Since the switching current and the decoupling inductance decrease with δ_{lim} , the required t_{dt} to achieve ZVS is higher. Moreover, the decoupling inductance also decrease when increasing the switching frequency, which also requires of higher t_{dt} since the inductive energy of the load is lower. The same trend is observed in all the power devices selected in this work. Hereinafter, the power losses in these devices are characterized for DAB and ABAC converters.

2.5.2 Losses distribution

First, the power losses distribution of DAB and ABAC converters is shown in Fig. 2.28 considering the specifications listed in Table 2.13. The selected dead-time $(t_{\rm dt})$ is 150 ns in both converters to ensure that ZVS is achieved, and clamp capacitances are considered as ideal voltage sources. The power losses in the primary and secondary power devices are presented and divided in conduction, dead-time and switching losses.

In Fig. 2.28(a) the power losses are presented for the HVDC devices, which is the same in DAB and ABAC. In this side, the losses distribution is similar for devices from (1)-(4), which are SiC devices with low $R_{\text{DS,on}}$. However, the conduction losses are dominant in (5), which is a Si device, due to the higher $R_{\text{DS,on}}$ compared to the SiC devices. In the

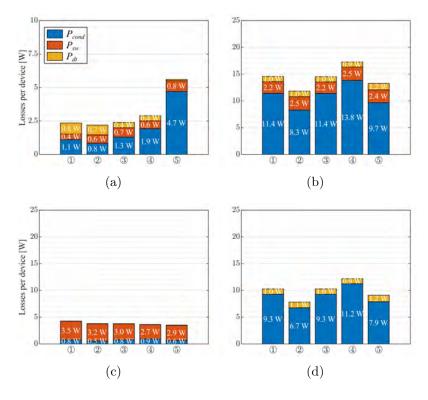


Figure 2.28 Losses distribution (conduction, switching and dead-time) per power device in DAB and ABAC converters (at $V_{\rm HV} = 250$ V and $V_{\rm LV} = 22$ V): (a) HVDC (equal for DAB and ABAC), (b) LVDC (DAB), (c) topside LVDC (ABAC) and (d) bottomside LVDC (ABAC).

LVDC side of DAB converter [see Fig. 2.28(b)], it is clear that the conduction losses are dominant regardless the selected power device. In ABAC converter, the power losses are different in topside and bottomside semiconductors. Then, switching losses are larger in topside devices [see Fig. 2.28(c)], while the conduction losses are almost negligible. The opposite case is found in bottomside devices [see Fig. 2.28(d)], which is due to the current waveforms that flow through topside and/or bottomside devices.

Looking at the total power losses in HVDC and LVDC devices depicted in Fig. 2.29, it is noticeable that the conduction losses are dominant in both sides. Furthermore, it is evident the main drawback of MEA applications, which are the conduction losses produced in the LVDC. As a basic comparison between DAB and ABAC, the power losses distribution is represented in Fig. 2.29(b) and 2.29(c). In these figures is clear the larger losses produced in the whole LVDC side of DAB considering all kind of losses (conduction, switching and dead-time). This is due to the different current distribution between topside and bottomside semiconductors in ABAC converter, which makes that the total power losses in the LVDC side are close to the half than those produced in the same side of DAB.

Finally, it is obvious the needed of parallelization of power devices in the LVDC stage to minimize the conduction losses that are produced. Without any parallelization, the power losses in both stages have a wide impact on the efficiency of both converters, which lies between 6% and 8% in the case of DAB converter only considering the behavior of these components. Furthermore, the selected power devices to perform the optimization algorithm are ③ and ② in the HVDC and LVDC sides respectively. This selection is based on the minimum losses produced as well as in the current condition of the semiconductor market, where the availability of the semiconductors is being limited, making difficult the acquisition of the devices.

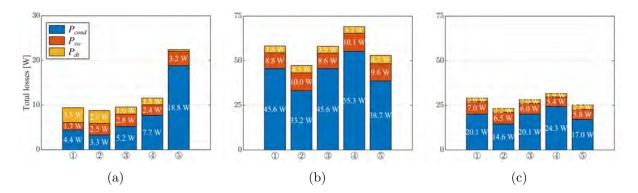


Figure 2.29 Total losses distribution (conduction, switching and dead-time) in DAB and ABAC converters (at $V_{\rm HV} = 250$ V and $V_{\rm LV} = 22$ V): (a) HVDC (equal for DAB and ABAC), (b) LVDC (DAB), and (c) LVDC (ABAC).

2.6 Design Space Analysis of DAB Converter for MEA

The number of parameters that impact on the volume and weight of DAB converter is large. Therefore, the selected design approach determines the resulting power density of the converter. In order to clarify the design trade-offs of this PEC, a design space analysis is carried out in this section based on the analytical models of the current stress of the power semiconductors in [23] and the DC-link capacitors presented in this work. The results of this analysis aid in the design procedure, resulting on the selection of the switching frequency, the δ modulation angle limit, the decoupling inductance and the DC-link bus capacitances.

Since SPS Rectangular modulation is able to transfer the maximum power transfer among the three modulations considered in this study, it is selected to determine the required decoupling inductance. In order to transfer 10 kW at the considered switching frequencies, the resulting decoupling inductances are computed with (2.58):

$$L_{\sigma} = \frac{V_{\rm HV} \, n \, V_{\rm LV} \, \delta_{\rm lim} \, (\pi - \delta_{\rm lim})}{2 \, \pi^2 \, f_{\rm sw} \, P_{\rm max}} \,, \tag{2.58}$$

where P_{max} is the desired maximum power transfer, and δ_{lim} is the theoretical limit of the modulation angle δ . In this work, the decoupling inductance is determined for the nominal values of HVDC and LVDC buses, i.e. $V_{\text{HV}} = 270$ and $V_{\text{LV}} = 27$. Therefore, it is important to note that the modulation angle δ may overcome this limit if the DC voltages on HVDC and LVDC buses vary from its nominal value. The design parameters utilized for the MEA case study analyzed in this section are listed in Table 2.17.

2.6.1 Switching Frequency

The switching frequency of the power devices in the DAB has a relevant influence on the volume of the overall converter. On one side, a high switching frequency can reduce the volume of the power transformer. However, the switching losses in the power semiconductor devices result also higher, and therefore the volume of the required heatsink increases. Therefore, the optimal switching frequency is selected considering the volume of these components.

Moreover, the current level on power devices of DAB converter does not vary when the switching frequency is increased. This is due to the fact that the required decoupling inductance in this converter is lower as higher is the switching frequency, and the product of these two variables is constant when considering the same power transfer, i.e. constant switching and RMS currents. Therefore, conduction losses does not increase with the switching frequency, and the larger switching losses are due to the linear increment of the

Parameter	Value	Units
$V_{\rm HV}$	270 (250-280)	V
$V_{\rm LV}$	27 (22-29)	V
n	10(270/27)	-
P	10	kW
$f_{ m sw}$	10:1:250	kHz
$\delta_{ m lim}$	1:1:90	0
$\Delta V_{\rm HV(pk-pk)}$	6	V
$\Delta V_{\rm LV(pk-pk)}$	1.5	V

 Table 2.17 Specifications utilized for the design space analysis.

switching frequency.

In this section, the volume of the power transformer is determined from the area product considering EE planar core geometries of N97 magnetic material (see Chapter 3). To compute the volume of the heatsink, the required thermal resistance is calculated from (2.59):

$$R_{\rm th} = \frac{(T_{\rm c} - T_{\rm amb})}{P_{\rm tot}}, \qquad (2.59)$$

where T_c and T_{amb} are the case and ambient temperatures respectively, and P_{tot} is the sum of switching and conduction losses in power devices. Then, based on a specific heatsink profile and airflow, the volume of this component is estimated to achieve the desired thermal resistance. The considered power devices for this study are C3M0045065D (SiC) and STP240N10F7 (Si) for HVDC and LVDC sides respectively. In LVDC side, five power devices are placed in parallel to reduce the power losses per device, ensuring that the maximum junction temperature of the device is not exceeded.

In Fig. 2.30, the estimated volume of the power transformer and heatsink are presented together when δ_{lim} is set to 10°. The crossing point between transformer and heatsink volumes lies slightly below 50 kHz. Furthermore, the minimum of the total volume is found at this frequency. Then, the selected switching frequency is 50 kHz for the estimation of

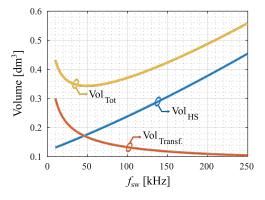


Figure 2.30 Volume of the power transformer and heatsink in DAB versus the switching frequency.

the power losses presented in this section.

It is important to note that the switching frequency in which the minimum volume is obtained may vary when considering different δ_{lim} due to its influence on the power losses, and thus in the required heatsink. Therefore, the analysis of the power losses in switching devices for different δ_{lim} is aimed in the following subsection.

2.6.2 Limit of the Modulation Angle (δ_{\lim})

Active to reactive power ratio in DAB converter strongly depends on the modulation angle δ . A common design choice in DAB design is to limit the maximum modulation angle δ with which the converter transfers the maximum power at nominal operating DC voltages. With this consideration, the reactive power processed by the converter is reduced to transfer the same active power level. Therefore, the resulting RMS and switching currents are lower, which determines the conduction and switching losses of the PEC. The power losses estimated in DAB are depicted in Fig. 2.31 for SPS Rectangular and combined TPS TPM-TRM.

In Fig. 2.31(a), the power losses for 10 kW of power transfer and SPS Rectangular modulation are presented for different limits of the modulation angle and different input to output voltages relationship. These different input and output voltage ratios correspond to the maximum (29/250), minimum (22/280) and unity (27/270) DC gain values ($V_{\rm LV}/V_{\rm HV}$) of the converter. Conduction and switching losses distribution are presented in the worst DC gain case at each $\delta_{\rm lim}$, where the conduction losses shows to be dominant in this application due to the high circulating currents in LVDC side. The reduction of $\delta_{\rm lim}$ decreases the conduction losses in DAB converter when working with SPS Rectangular

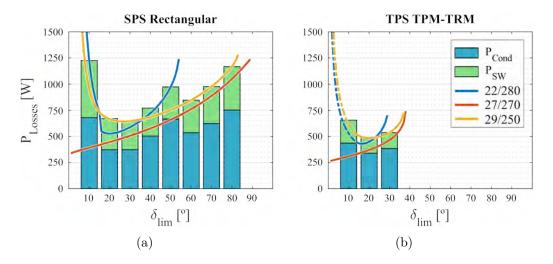


Figure 2.31 Power losses in the power devices of DAB converter for different operating DC voltages with SPS Rectangular and combined TPS-TPM and TPS-TRM modulations. The distribution of conduction and switching losses is depicted in the worst case.

modulation, which are critical in the design of the LVDC-side of the DC/DC converter in MEA applications due to the low-voltage and high-current stress. However, this benefit is mainly found close to the nominal DC gain, and there is a trade-off between δ_{lim} and the power losses when working outside nominal operating condition. Comparing δ_{lim} at 10° and 20° at 22/280 in the worst case, it is noticeable the increment on both switching and conduction losses. The higher switching losses are caused by the operation in hard-switching conditions at high-power transfer, which is the main drawback of decreasing δ_{lim} , while the conduction losses are larger due to the reactive power that flows through the converter when working outside nominal DC voltages with low modulation angles. Furthermore, it can be noted that the nominal power transfer is not achieved at the minimum DC gain for δ_{lim} above 55°. This is due to the fact that the required δ to transmit the maximum output power is above 90°, exceeding the maximum theoretical δ .

In Fig. 2.31(b) the study is presented for combined TPS TPM-TRM. When δ_{lim} is set above 40° it is not possible to transfer the maximum power with this combined modulation method in the considered DC gain relationships. Below 40°, the power transfer is possible in these operating conditions. As in SPS Rectangular modulation at unity DC gain, the power losses are lower when δ_{lim} is decreased, which is also due to the reactive power in the converter. However, the large power losses found at low δ_{lim} values are caused by the higher RMS current levels when working with TPS-TRM at high-power transfer compared to TPS-TPM. Furthermore, the required δ_{lim} to transmit the maximum power at minimum DC gain is below 30°.

Although the variation of DC voltages in MEA applications is not wide (250-280 V in HVDC, and 22-29 V in LVDC), the selection of δ_{lim} must be deeply analyzed to reduce the conduction and switching losses, improving the resulting power density. Therefore, the efficiency of the converter is determined and compared between different δ_{lim} for the modulation methods presented in this work.

2.6.3 Efficiency Analysis

In this section, the efficiency of DAB is analyzed when δ_{lim} is set to 10°, 20° and 25°. The theoretical limit of the modulation angle is selected to be able to transfer the maximum power with the combined TPS TPM-TRM in all the operating points of the converter. Then, the efficiency of the converter is computed considering conduction and switching losses in power devices.

The efficiency map of the DAB converter is presented in Fig. 2.32 for the mentioned δ_{lim} and the considered modulations. In all cases, the highest efficiencies in the converter are found in parallel to the nominal operating condition and close to the nominal working points described in Table 2.17. This phenomena is remarkable as the limit of the modu-

lation angle δ decreases, and is due to the reduction of the circulating reactive power in the converter when working at DC gain values close to unity. Nevertheless, the efficiency starts to decrease outside this condition as a result of the impact of DC bus voltages on the reactive power. Moreover, hard-switching region appear when working with SPS Rectangular modulation, whose impact on the efficiency of the converter is critical.

For $\delta_{\text{lim}} = 20^{\circ}$ and $\delta_{\text{lim}} = 25^{\circ}$, the efficiency of the converter decreases compared with $\delta_{\text{lim}} = 10^{\circ}$. In all cases, the efficiency improvement with combined TPS TPM-TRM regarding SPS Rectangular is considerable.

This analysis leads to the selection of combined TPS TPM-TRM working with low δ angles. In order to examine the influence of δ_{lim} over different load conditions, the study is extended to the whole output power range considering forward and backward power flow direction. To this aim, the average efficiency (η_{AVG}) of the map at the different output power is defined by (2.60):

$$\eta_{\rm AVG} = \frac{1}{\Delta V_{\rm LV} \,\Delta V_{\rm HV}} \int \int \eta \left(V_{\rm HV}, V_{\rm LV} \right) dV_{\rm HV} \, dV_{\rm LV} \,, \tag{2.60}$$

where $\eta(V_{\rm HV}, V_{\rm LV})$ is the efficiency as a function of the DC bus voltages, and $\Delta V_{\rm HV}$ and $\Delta V_{\rm LV}$ are the DC-link voltage ranges in the HVDC and LVDC respectively.

In order to select the best efficiency trade-off, $\eta_{\rm \scriptscriptstyle AVG}$ is computed and compared for the

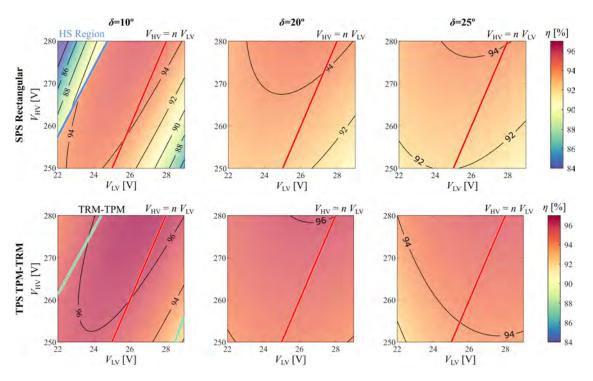


Figure 2.32 Efficiency map of the DAB converter at P = 10 kW when working with SPS Rectangular (topside) and combined TPS TPM and TRM (bottomside) modulations for different δ_{lim} : 10°, 20° and 25°.

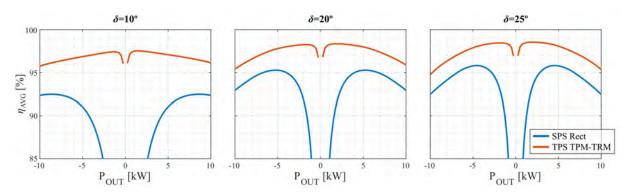


Figure 2.33 Efficiency versus output power (P_{OUT}) in SPS Rectangular and combined TPS TPM-TRM for the considered δ_{lim} : 10°, 20° and 25°.

different voltage gains, transferred power and δ_{lim} , and it is presented in Fig. 2.33. It can be noted that the average efficiency in combined TPS modulation is larger than SPS Rectangular in both forward and backward modes in the whole output power range when δ_{lim} is set to the considered angles. This is due to the hard-switching operation in some operating points while working with SPS Rectangular modulation. This hard-switching region appear at low-power transfer levels when δ_{lim} is increased, leading to lower η_{AVG} . Therefore, TPS TPM-TRM modulation seems to be the most adequate to increase the efficiency of the converter in a wide operating region. With this modulation method, the average efficiency at high-power transfer is increased at low δ_{lim} . However, the efficiency at light load condition is penalized. This fact is due to the operation of TPS-TRM outside nominal DC gain, which increase the RMS current stress in the power devices. Then, the best efficiency tradeoff between full and light load operating conditions is found at $\delta_{\text{lim}} = 20^{\circ}$ for the considered MEA application.

2.6.4 DC-Link Capacitors

One of the critical steps in the design of DAB converter for MEA applications is the large LVDC capacitance required to satisfy the voltage ripple requirements. However, the impact of the switching frequency and LVDC bus capacitance on the voltage ripple have not been aimed yet. Since the analysis is similar for input and output capacitors, this section is focused in output capacitor.

To develop this study, the analytical models presented in section 2.2 of this work are employed to characterize the voltage ripple in LVDC capacitor regarding the selected capacitance and switching frequency. In Fig. 2.34(a), two scenarios are depicted: the influence of switching frequency variations on the peak-to-peak voltage ripple for fixed output capacitances, and also the influence of LVDC capacitance variations for fixed switching frequencies. It can be noted that, for capacitance values below 100 μ F, the switching frequency must be increased above 150 kHz in order to fulfill MEA requirements. As far as the capacitance is increased, the switching frequency required to meet the standard is reduced.

Furthermore, the trend of the output capacitance required at different switching frequencies is shown. At 50 kHz of switching frequency the minimum required capacitance is 550 μ F to achieve a maximum peak to peak voltage ripple of 1.5 V. For higher switching frequencies, the impact of this capacitance is lower, and MEA limits are satisfied for capacitances above 200 μ F for $f_{sw} = 150$ kHz.

The impact of both switching frequency and output capacitance is shown in Fig. 2.34(b). The minimum LVDC capacitance at each switching frequency is defined by the intersection of the LVDC peak-to-peak voltage ripple $(\Delta V_{LV(pk-pk)})$ with the MEA limit plane. This curve is defined by two asymptotic limits that theoretically tends to infinite capacitance when the switching frequency is close to zero, and infinite switching frequency when the output capacitance falls to zero in order to meet the MEA standard. Therefore, the best trade-offs between switching frequency and required capacitance are found in the knee of the curve, which is found between 50 and 100 kHz of the switching frequency for the MEA case study considered in this work. Furthermore, it can be noted that the safety margin regarding MEA limit can be achieved by slightly increasing the minimum capacitance.

The RMS current level that flows through the capacitor also plays an important role in the sizing of this component. The number of capacitors set in parallel must be able to handle the required RMS current. In Fig. 2.35, the normalized RMS current through the output capacitor is presented to find the optimal δ_{lim} for its sizing. For the limit of the modulation angle selected in this section, i.e. 20°, the RMS current is close to its minimum value. Nevertheless, the trend is increasing below 10°.

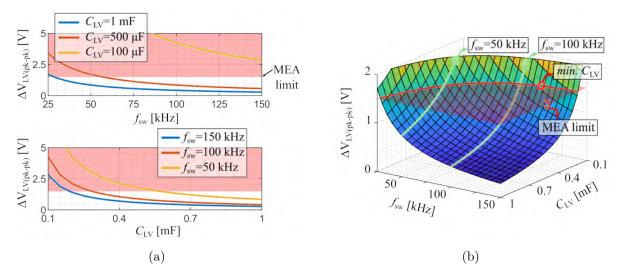


Figure 2.34 Influence of output capacitance $(C_{\rm LV})$ and switching frequency $(f_{\rm sw})$ on the peak to peak voltage ripple $(\Delta V_{\rm pk-pk})$.

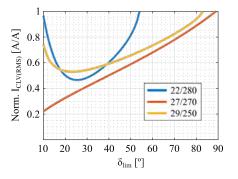


Figure 2.35 Normalized RMS current level versus δ_{lim} for minimum, nominal and maximum DC gain voltages at maximum power transfer.

2.6.5 IPOP Configuration

In this subsection, the selection of the optimal number of converters considering IPOP configurations is aimed. To this objective, the volume of the LVDC and HVDC capacitors is computed based on manufacturer data for MKP capacitors, while the power transformer volume $(V_{\rm Tr})$ is estimated from required area product $(A_{\rm p})$ considering EE planar cores (see Appendix A). In order to compute the power losses in switching devices, the selected HVDC and LVDC semiconductors are C3M0045065D (SiC) and STP240N10F7 (Si).

In Fig. 2.36(a) the resulting volume of the output capacitor and power transformer stage is presented. As long as the number of converters (N_p) increase, the required volume of the output capacitor is lower due to the reduction on the capacitance needed to satisfy MEA specifications. In this study, the maximum voltage ripple allowed is a 50% of the MEA limit, i.e. 1.5V in LVDC. However, the total volume of the transformer stage increase with the number of converters. Therefore, the optimal number of converters to minimize the resulting volume of the most critical passive devices in DAB converter is found from 5-8 converters when considering interleaved IPOP DAB configurations.

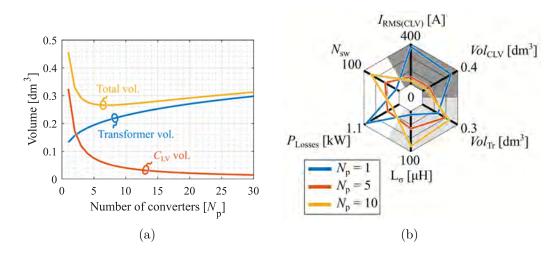


Figure 2.36 Volume of passive devices regarding the number of converters.

Then, a spider-chart comparison is shown in Fig. 2.36(b) to detail the benefits and drawbacks of increasing the number of parallel converters in IPOP DAB configurations. Therefore, minimum, optimal and twice the optimal number of converters, i.e. $N_p=1$, $N_p=5$ and $N_p=10$, are presented. Main benefits are the reduction of the RMS current stress in output capacitor, as well as its required volume. Moreover, the power losses in the converter tends to decrease as higher is the number of paralleled converters due to the reduction of the current stress per power device. Nevertheless, the number of power devices (N_{sw}) , the volume of the power transformer, and the required decoupling inductance are larger. It is important to note that the leakage inductance of the power transformer is often used as the decoupling inductance in order to save volume of the converter, which becomes a complex task as higher is the required inductance. Thus, an external inductor may be added in series to the power transformer, penalizing the resulting power density of the converter.

2.7 Experimental Validation

To conclude with this chapter, the experimental validation of the analytical models given in this work for DAB converter is developed in this section. To this objective, a power converter available at *Ikerlan Technology Research Centre* laboratory of *Power Electronics Area* is utilized. The specifications of this converter are listed in Table 2.18, which are significantly different from MEA applications. Nevertheless, this fact also shows the utility of the models provided in this work regardless the application proposal.

The converter and magnetic components utilized during the experimental validation are shown in Fig. 2.37. As one of the most important details, the converter has been built utilizing power modules of $FF11MR12W1M1_B11$, i.e. $V_{\text{DS,max}} = 1200$ V and $R_{\text{DS,on}} = 11$ m Ω . The control board utilized is a F28379D Launchpad of Texas Instruments. An external gapped inductor is used to control the maximum power transfer, being set its inductance to 200 μ H. The power transformer is formed by two primary and two secondary windings whose turns ratio is 1:2. Then, it allows to adjust the transformer turns ratio

Parameter	Value	Units
$V_{\rm DC}$	250-500	V
$V_{\rm BAT}$	600-800	V
n	0.5	-
P	20	kW
$f_{\rm sw}$	25	kHz
$t_{ m dt}$	50	ns

Table 2.18 Power converter specifications.

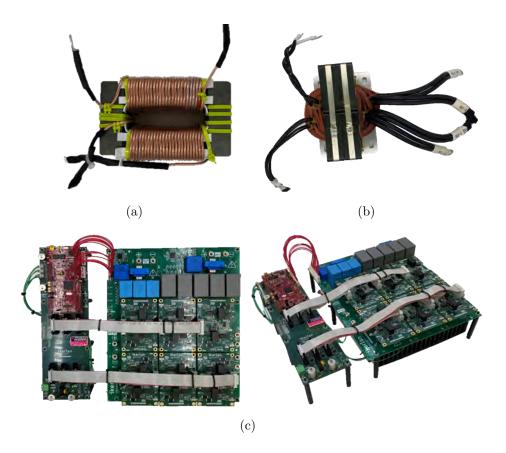


Figure 2.37 Magnetic components, power converter and control board utilized for the experimental validation: (a) Power transfer inductor, (b) power transformer and (c) power converter and control board.

by connecting in series the different primary windings, as same as in the secondary side.

In this work, the transformer turns ratio is set to 1 to perform back-to-back experiments, which allows the user to work with SPS Rectangular and TPS-TPM modulations. Then, a DC voltage source is connected to the battery side of the converter, while an electronic load is connected to the DC bus. This case study simulates the power transfer from the battery side to the DC bus, and has been utilized in all the experiments carried out in this work. It is important to note that the experimentation in this work has been done in open loop configuration, by extracting the corresponding modulation angles from the simulation models developed in PLECS.

The experimental set-ups for the analytical model validation are presented in Fig. 2.38. First, a back-to-back configuration have been tested to validate the analytical models when working at unity gain between input and output ports. This fact limits the number of modulation methods that can be analyzed to SPS Rectangular and TPS-TPM, since it is not possible to work with TPS-TRM in this input to output voltage ratio.

The described experiments are shown in Fig. 2.39. In order to get an insight of the DAB behavior under MEA specifications, 270/270 is one of the selected voltage ratios. In this case, DAB converter could act as the interface between different HVDC buses in case

of failure of a generator in DC/DC MEA EPDS. This is an ideal scenario for the operation of DAB converter since it is able to work in SPS rectangular modulation without loosing ZVS behavior.

Furthermore, 400/400 voltage ratio has been selected in both SPS rectangular modulation and TPS-TPM. The decision to test also at 400/400 has been taken in order to increase the nominal power processed by the converter up to 4 kW in SPS rectangular modulation. The selected δ for these test is set to 10°, 30°, 50°, 70° and 90°. In these angles, the converter is able to transfer 0.385, 1, 1.5, 1.75 and 1.9 kW at 270/270, and 0.8, 2.2, 3.3, 3.8 and 4 kW at 400/400.

As in SPS rectangular modulation, the selected voltage ratios are 270/270 and 400/400 for TPS-TPM in back-to-back operation. In the tested operating points, the power converter is able to transfer 0.2, 0.4, 0.6, 0.8 and 1 kW when working at 270/270, while this power transfer capability increases up to 0.5, 1, 1.5, 2 and 2.5 kW at 400/400.

Since the operation of TPS-TRM is not available in back-to-back set-up, the converter is also tested in normal operation as depicted in Fig. 2.34(b). This set-up is formed by connecting two DC voltage sources to input and output ports, one of them acting as an electronic load (V_{out}). The selected voltage ratios are 400/270 in case of SPS rectangular modulation, in which δ is set to same values as in back-to-back experiments. This fact allows the converter to transfer up to 2.7 kW when working at $\delta = 90^{\circ}$. The selected operating points goes from hard-switching operation at $\delta = 10^{\circ}$ to ZVS when δ is fixed at 50°, 70° and 90°. Finally, combined TPS-TPM and TRM is tested at 0.25, 0.5 (TPS-TRM), 0.75, 1, 1.25 and 1.5 kW (TPS-TPM). It is interesting to see that in these cases, the compensation of the dead time is not perfect due to the unmatched experimental values, i.e. slightly different input and output voltages and/or decoupling inductance, regarding the simulation model in PLECS to get the modulation angles values. This fact is appreciable since zero current levels does not exactly lie in this level, showing an undesired glitch.

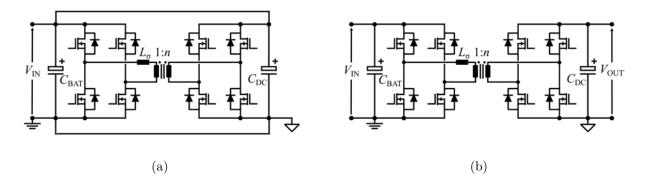
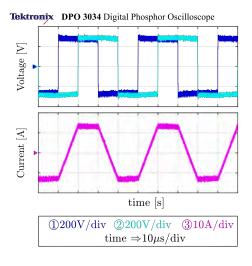
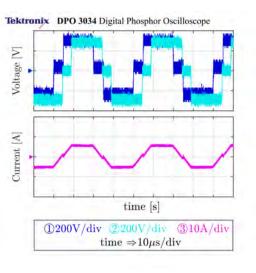
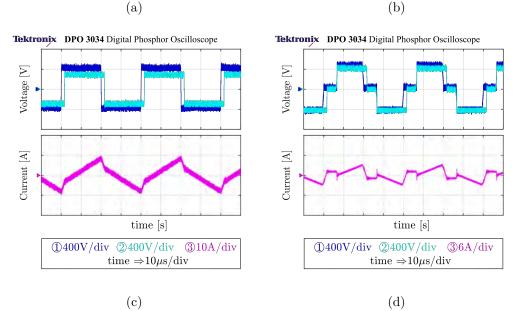


Figure 2.38 Schematic of the experimental set-ups: (a) Back-to-back and (b) normal operation of the power converter.









Tektronix DPO 3034 Digital Phosphor Oscilloscope Voltage [V] Current [A] time [s] (1400V/div (2)400V/div)36A/div time $\Rightarrow 10 \mu s/div$

(e)

Figure 2.39 Experimental transformer voltage and current waveforms: (a) SPS rectangular modulation at $\delta = 90^{\circ}$ in 270/270, (b) TPS-TPM at $P_{\text{out}} = 1kW$ in 270/270, (c) hard-switching operation of SPS rectangular operation at $\delta = 10^{\circ} 400/270$, (d) TPS-TRM at $P_{\text{out}} = 0.25kW$ in 450/400.

With these experimental results, the validation of the analytical models developed in this thesis is performed and depicted in Fig. 2.40 and 2.41. The accuracy of the analytical models shows to be good (maximum relative error of 10.31%), validating the equations also utilizing an experimental set-up. In contrast to simulation results, there are slightly differences specially appreciated at low power transfer of SPS Rectangular modulation and combined TPS-TRM in the whole output power range. These differences are mainly caused by the dead time, which is not considered in the analytical models, as well as the unequal values of input and output voltages and decoupling inductance in the testbench compared to those utilized in the simulation models to obtain the corresponding modulation angles.

With this validation process, it is clear the useful that these analytical models are to determine the current stress in power devices regardless the application proposal. Therefore, the equations presented in this thesis have been utilized along Chapter 4 to develop an optimization procedure, which aims to find the best trade-off between efficiency, power density and leakage-to-decoupling inductance error.

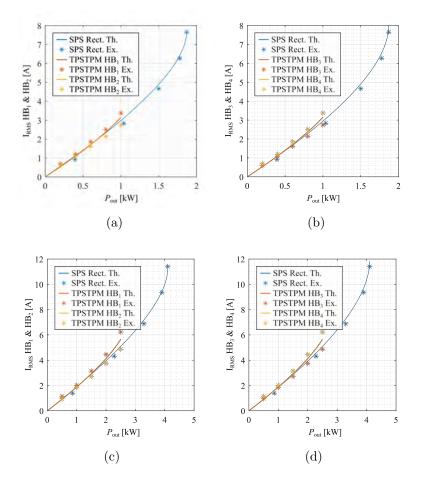


Figure 2.40 Experimental validation of back-to-back operation of the analytical models presented in this work for: (a) primary power devices at 270/270, (b) secondary power devices at 400/400, (c) primary at 400/400 and (b) secondary at 400/400.

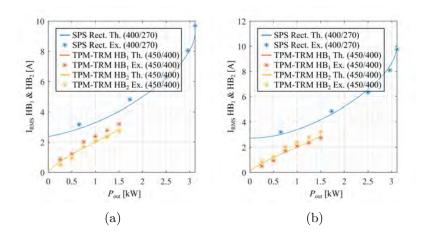


Figure 2.41 Experimental validation of normal operation of the analytical models presented in this work for: (a) primary power devices and (b) secondary power devices.

2.8 Conclusions

In this chapter, the basics of the bidirectional isolated DC/DC PECs considered in this work (DAB and ABAC) have been settled. The analytical models that describe the behavior of both converters have been proposed and validated in this work. In DAB converter, SPS rectangular modulation and combined TPS-TPM and TRM are considered, while only SPS is studied in ABAC converter. Then, the equations of the RMS and AVG currents that flow through the primary and secondary power devices in both converters have been presented and validated based on a simulation model developed in PLECS. Moreover, the equations that describe the ideal ZVS boundaries have been presented for both converters, as well as the semiconductor states in each case. The utilization of parallel structures (IPOP) have been also analyzed for DAB converter as an alternative to reduce the large LVDC capacitance required to meet MEA requirements. The time-domain equations that describe the behavior of these structures are presented considering the number of power converters connected in parallel, which are also validated with PLECS.

To evaluate the error that is produced due to the considerations taken during the mathematical development procedure, i.e. clamp capacitances modeled as ideal voltage sources and negligible dead-time and conduction losses, an analysis is performed based on the results given by the simulation model developed in PLECS for ABAC converter. The analysis reveals that the accuracy of the presented analytical models is not committed by the variation of these parameters.

The power losses that are present in the HVDC and LVDC sides of both converters have been characterized for 1 kW power converter. First, the power losses per device are detailed to evaluate the difference between the secondary stages of DAB and ABAC. In DAB converter, the main contribution to the power losses in each device results from the conduction due to the high currents that are circulating through the LVDC side. Nevertheless, the current distribution in ABAC converter is different for topside and bottomside semiconductors, resulting on unbalanced switching and conduction losses. As a result of this characterization, it is clear that the main contribution to the power losses comes from the conduction of the LVDC side in both converters. Furthermore, an analytical model to determine the minimum required $t_{\rm dt}$ to discharge the $C_{\rm oss}$ has been derived and validated with a simulation model developed in LTSpice. In order to get a deep insight of the trade-offs that are found in DAB, the analysis of the design-space is done. In this case, the switching frequency, modulation methods and $\delta_{\rm lim}$ impact in power losses are presented. Also, the influence of these variables over the LVDC-link capacitor is detailed, which is one of the most critical components in DAB.

Finally, the experimental validation of the analytical models developed in this work to predict the current stress has been carried out by utilizing a power converter available at *Power Electronics Area* laboratory of Ikerlan Technology Research Centre. The validation process shows a good correlation between experimental and theoretical results, which probes the powerful that these analytical models are to predict RMS and AVG. This fact aids the designer to reduce the computational cost of the design process, as well as to calculate the corresponding conduction and switching power losses.

3

Design of Magnetic Components

Summary:

Magnetic devices as inductors and/or transformers are present in almost any converter topology. The design of this components is a complex task due to the wide number of variables, correlated with each other, that impact on its performance and size. Therefore, a thorough review of the fundamental concepts that are involved in the design of these components is presented in this chapter.

3.1 Introduction

Nowadays, almost any PEC has one or more integrated magnetic devices. These components are utilized to store energy as well as to provide galvanic isolation between buses. There are a wide amount of applications that require from magnetic devices for different purposes, as Electromagnetic Interference (EMI) filters and/or to adjust the resonant tank in that kind of converters. Traditionally, the magnetic devices are one of the largest contribution to both weight and volume in most PEC topologies. Therefore, the design of these components is one of the most important steps.

The utilization of magnetic devices is also required in the PECs proposed for MEA applications, in which galvanic isolation between HVDC and LVDC buses is required. Moreover, as presented in Chapter 2, two DC output inductors are also utilized in the case of ABAC converter. Therefore, this chapter gathers the effects that are involved in the behavior of magnetic components. Furthermore, the analytical models provided in the literature for the design procedure of these components are given. It is important to note that this work considers planar magnetic cores due to the power density benefits in comparison to conventional cores.

First, the performance factor of magnetic materials is revisited to get insight of the area product of the magnetic core versus the frequency. Then, the equivalent circuit of power transformers is depicted, in which stray capacitances and leakage inductances acquire a huge importance when considering planar magnetic components. In these devices, the analysis of skin and proximity effects due to an AC current flowing through a conductor plays an important role since it set the maximum height of the Printed Circuit Board (PCB) track.

In the PECs converters considered in this work, a good accuracy when modeling the leakage inductances and stray capacitances is also required. This fact sometimes require of FEA simulations to properly determine the final value in order to get a close value to the decoupling inductance, as well as to calculate the resonant frequency between these components. With this strategy, the implementation of an extra inductor is avoided, earning the corresponding volume and weight. Also, design that do not fulfill a leakage inductance to stray capacitance resonant frequency at least ten times higher than the switching frequency must be discarded.

Finally, the procedure to determine the winding and core losses is detailed. The resulting losses are utilized afterwards to compute the temperatures in different points of the component. The analytical models utilized aids to predict the temperature in both core and windings, being useful to avoid core temperatures larger than or closer to the Curie temperature, which will result on losing the magnetic properties of the material.

3.2 Performance Factor of Magnetic Materials

Traditionally, the world of power electronics has followed the idea that the size of the magnetic device linearly decreases when increasing the switching frequency, following the trend of the Steinmetz equation presented below [134]:

$$P_{\rm v} = K_{\rm c} f^{\alpha} \hat{B}^{\beta} \quad , \tag{3.1}$$

where f is the operating frequency of the magnetic device, \hat{B} is the peak flux density, and $P_{\rm v}$ is the core loss density of the magnetic material. Furthermore, $K_{\rm c}$, α and β are the Steinmetz parameters that describe the core loss of the magnetic material to follow typical core loss curves given by the manufacturers.

However, there is an optimal frequency where the volume of the magnetic component is minimum, which is caused by the fact that core loss curves are not straight lines. In order to catch the two asymptotes that are present in these curves, the Steinmetz equation has been revisited in [135], which leads to (3.2):

$$P_{\rm v} = k_{\rm c} \left(f\hat{B}\right)^{\beta} f^{\alpha-\beta} \left[1 + \left(\frac{f}{f_{\rm cr}}\right)^{\alpha_{\rm cr}}\right] \quad , \tag{3.2}$$

where $f_{\rm cr}$ and $\alpha_{\rm cr}$ are the parameters included to get the trend given by the asymptote found at high frequencies. Then, the performance factor of magnetic materials, which is the product of frequency (f) and flux density (B), is commonly utilized for the comparison of different ferrite materials. This is because the product of these two variables is found in the sizing formulas of power transformers and inductors, as well as in the classical and revisited Steinmetz formulas [(3.1) and (3.2)]. According to [135], the equation that define the area product of a power transformer is (3.3):

$$A_{\rm p} = \left[\left(\frac{k_{\rm c}^{2} \left(\rho_{\rm w} k_{\rm w}\right)^{\beta}}{\left(hk_{\rm t}\right)^{(\beta+2)}} \right) \left(\frac{K_{\rm c}^{2} \left(\beta+2\right)^{(\beta+2)}}{4\beta^{\beta}} \right) \left(\frac{\sum {\rm VA}^{2\beta}}{K_{\rm v}^{2\beta} k_{\rm u}^{\beta} \Delta T^{(\beta+2)}} \right) \right]^{4/(7\beta-2)} f^{8(\alpha-\beta)/(7\beta-2)} \left[1 + \left(\frac{f}{f_{\rm cr}}\right)^{\alpha_{\rm cr}} \right]^{8/(7\beta-2)} , \quad (3.3)$$

which is an elaborated expression that depends on many variables. Among them, the classical Steinmetz parameters (K_c , α and β) and the new proposed parameters (α_{cr} and f_{cr}) are found. Furthermore, k_w , k_c and k_t are the constants that correlates the area product of a magnetic core with the volume of the winding and core, as well as with the surface area, whose typical values are 10, 5.6 and 40 [135]. Other important parameters in the sizing of a power transformer are the coefficient of heat transfer by convection (h), the resistivity of the wire (ρ_w), the voltage waveform factor (K_v) and the temperature

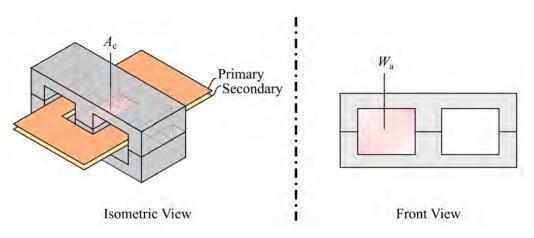


Figure 3.1 Illustration of the isometric (with windings) and front (without windings) views of a planar power transformer.

gradient (ΔT) .

The area product is the result of multiplying the area of the core (A_c) and the window area (W_a) . These two areas, which are illustrated in Fig. 3.1 for a EE planar magnetic core, define the ability of the core to handle the maximum magnetic flux density when the device is in operation as well as the available space to place the primary and secondary windings. The classical formula to evaluate the area product is (3.4):

$$A_{\rm p} = \left[\frac{\rho_{\rm w}k_{\rm w}}{hk_{\rm t}}\frac{\beta+2}{\beta}\frac{1}{k_{\rm u}\Delta T}\right]^{4/7} \left[\frac{\sum {\rm VA}}{K_{\rm v}f\hat{B}_{\rm o}}\right]^{8/7} \quad . \tag{3.4}$$

A more detailed explanation to derive these formulas is found in [135]. In Fig. 3.2, the resulting area product when considering MEA voltage specifications is presented for a 1 kW power transformer. In this case, it is noticeable the difference between these two estimations of the transformer size above 100 kHz of operating frequency (high-frequency),

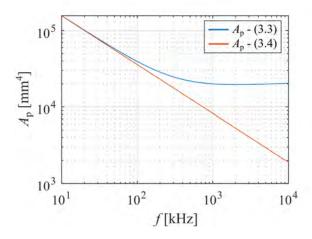


Figure 3.2 Area product versus frequency of a power transformer considering MEA specifications considering classical and revisited equations.

while the result of both calculations is quite similar from 10-100 kHz (medium-frequency).

It is important to note that this study is only applicable to ferrite materials, and thus the considerations taken change when considering other magnetic materials, e.g. amorphous and/or nanocrystalline in medium-frequency and silicon-steel in low-frequency transformers. Alternatively, the scaling laws proposed in [136] aid the designers to explore the design space of the power transformer regardless the selected magnetic material. Moreover, a database with the considered planar magnetic cores is presented in Appendix A. Hereinafter, the fundamentals of the behavior of power transformers are described in detail.

3.3 Equivalent Circuit

The T-type equivalent circuit of a power transformer is shown in Fig. 3.3. First, the simplified equivalent circuit [see Fig. 3.3(a)], where the power losses are neglected. The leakage inductances (L_{k1} and L_{k2}) represent the magnetic flux that is not linked in both primary and secondary windings, while the magnetization of the magnetic core is given by the magnetizing inductance ($L_{\rm M}$). This results on the fact that effective relationship between primary and secondary voltages and/or currents does not meet exactly the ideal turns ratio of the transformer. Based on this circuit, the working principle of the power transformer is set by (3.5) [137]:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} , \qquad (3.5)$$

where L_{11} and L_{22} are the primary and secondary self-inductances and L_{12} is the mutual inductance between both windings. These inductances are calculated as function of the leakage and magnetizing inductances with the following equations:

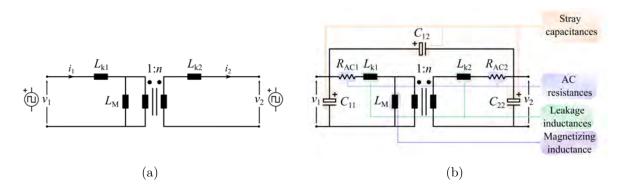


Figure 3.3 Equivalent circuit of power transformer: (a) simplified and (b) considering all the parasitic elements involved in its behavior.

$$L_{12} = \frac{n_2}{n_1} L_{\rm M} \quad , \tag{3.6}$$

$$L_{11} = L_{k1} + \frac{n_1}{n_2} L_{12} \quad , \tag{3.7}$$

$$L_{22} = L_{k2} + \frac{n_2}{n_1} L_{12} \quad , \tag{3.8}$$

being n_1 and n_2 the turns of the primary and secondary windings, and $n = n_2/n_1$ the turns ratio of the power transformer. Then, the equations that describe the working principle of a power transformer are rewritten by solving the matrix system in (3.5) and replacing (3.6)-(3.8), which leads to [138]:

$$v_1 = L_{k1} \frac{\mathrm{d}i_1}{\mathrm{d}t} + L_{\mathrm{M}} \frac{\mathrm{d}i_{\mathrm{M}}}{\mathrm{d}t} \tag{3.9}$$

$$v_2 = nL_{\rm M} \frac{\mathrm{d}i_{\rm M}}{\mathrm{d}t} + L_{\rm k2} \frac{\mathrm{d}i_2}{\mathrm{d}t} \tag{3.10}$$

The determination of the leakage inductance must be studied in detail. However, the magnetizing inductance can be easily determined from the magnetic equivalent circuit of the transformer as a function of the vacuum permeability (μ_0), the relative permeability of the magnetic material (μ_r), the air gap (l_g), the magnetic path length (l), the number of primary turns (n_1) and the area of the core (A_c) [61]:

$$L_{\rm M} = \frac{\mu_0 \, n_1^{\ 2} \, A_{\rm c}}{2 \, l_{\rm g} + \frac{l}{\mu_{\rm r}}} \tag{3.11}$$

Nevertheless, as depicted in Fig. 3.3(b), there are more passive elements that impact on the behavior of a power transformer. First, the AC resistances (R_{AC1} and R_{AC2}), whose value is frequency dependent, define the winding losses of this component. Furthermore, primary (C_{11}), secondary (C_{22}) and primary-secondary (C_{12}) stray capacitances appear due the voltage drop between parallel plates. As the leakage inductances, the determination of this capacitances is a difficult task and its accurate value must be extracted experimentally [139]. However, the analytical extraction of this parameters is useful for some converters, e.g. resonant converters, where these parameters can be utilized as the passive elements of the converter [140]. The analytical calculation of this parameters (AC resistances, leakage inductance and stray capacitances) is addressed along section 3.4.

Once the fundamental equations that describe the behavior of the power transformer have been presented, the aim of the next section is to describe the effects that are present in the windings due to the fact that an AC current is circulating through them are described in depth.

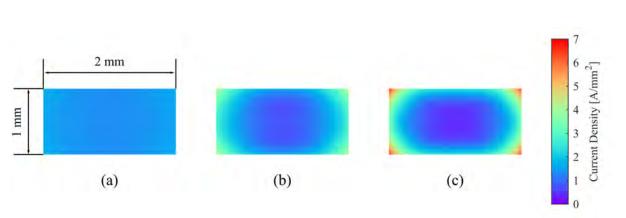
3.4 Frequency Phenomena

Along this section, the well-known frequency effects that characterize the performance of the power transformer are detailed. Since the emergence of wide band-gap semiconductors, the operating frequency of the power converters has been constantly increasing. Therefore, the importance of the non-ideal behaviors, i.e. skin and proximity effects, that are result of the frequency is becoming large.

3.4.1 Skin Effect

In the operation of a any conductor, the AC current that flows through it induces an alternating magnetic flux (ϕ), and the corresponding magnetic flux density (B) and magnetic field strength (H) [141]. Part of this flux stays inside the conductor, originating eddy currents that concentrate the current density in the borders of the conductor. Therefore, although the total current in the conductor does not change, its current density turns to a non-homogeneous distribution [63]. This effect is depicted in Fig. 3.4 for a 2 mm² rectangular conductor, which has been obtained from a FEA simulation software. This simulation shows the distribution of the current density through the conductor. It is excited with a sinusoidal waveform whose RMS value is 2 A, and the operating frequency is set to 10, 50 and 100 kHz respectively. The skin depth effect on the conductor begins noticeable as the operating frequency increase, being lower the uniformity of the current density.

To minimize the impact of this phenomena on the transformer behavior, the maximum height of the rectangular conductor and/or the diameter in round conductors is calculated with:



$$\delta_{\rm sd} = \sqrt{\frac{\rho}{\pi\mu f}} \tag{3.12}$$

Figure 3.4 Current density through a single conductor excited with 2 A RMS for different operating frequencies: (a) 10 kHz, (b) 50 kHz and (c) 100 kHz.

where δ_{sd} is the penetration of the skin depth effect, ρ_w is the electrical resistivity of the conductor material, μ is its magnetic permeability and f is the operating frequency. As a result of this equation, the radial distance from the surface to the center of the conductor that represent a current density drop of 37% is obtained.

3.4.2 Proximity Effect

Similar to the skin effect, the proximity effect is produced by the alternating magnetic flux that is induced in nearby conductors. As well as in the skin effect, this induced flux results in a non-homogeneous distribution of the current density due to the generated eddy currents. In Fig. 3.5 three different cases have been considered: the proximity effect in an open circuit conductor close to a conductor carrying an AC current, and two neighboring conductors whose current flows in the same and opposite directions.

The described non-uniformity of the current density arises from the imposition of an external magnetic field in the induced open circuit conductor [see Fig. 3.5(a)]. It can be seen that the current density in the open circuit conductor is maximum in the borders of the conductor that are the closest and the farthest to its neighboring, while remain zero at the center. However, it is depicted that the eddy currents flow in opposite directions, as given by the sign of the current density.

Hereinafter, the phenomena produced when both conductors are carrying a predefined current level is explained. First, the consequence of placing two conductors with equal current levels flowing in the same direction is shown in Fig. 3.5(b). In this case, the current density is concentrated in the borders of each conductor that are not faced, like the skin depth effect produced in a single conductor whose area and current density are equivalent to the case study. Furthermore, the effect produced when the current that flows through the nearby conductors follows opposite directions is presented in Fig. 3.5(c), being clear

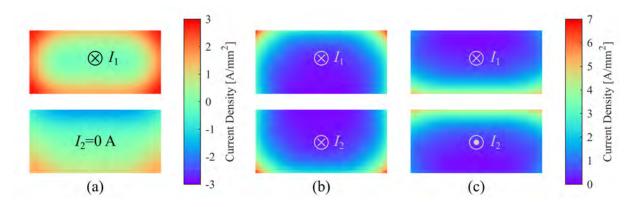


Figure 3.5 Current density of two nearby conductors for various cases: (a) first conductor carries 2 A of current while second conductor is left open circuit, (b) both conductors carrying 2 A in the same direction and (c) both conductors carrying 2 A in opposite directions.

that in this case the current density is accumulated in both cases in the border that face these conductors. As further is the distance to this border, the current density in the conductor decreases.

3.5 Passive Elements

The passive elements that are involved in the behavior of a power transformer have been presented in Fig. 3.3(b). In this section, the analytical models utilized in this work to determine the values of these elements are detailed. Moreover, it is important to note that planar technology is considered for the magnetic devices designed in this work. Then, the models for the calculation of the AC resistance, leakage inductance and stray capacitances are given below.

3.5.1 AC Resistance

The AC resistance of the windings of magnetic devices is the parameter that define the copper losses in the component (see section 3.5), which is calculated from the DC resistance of the conductor. The DC value is computed with (3.13):

$$R_{\rm DC} = \rho \, \frac{l}{A_{\rm w}} \quad , \tag{3.13}$$

where l and A_w are the length and area of the conductor. According to [142], AC and DC resistances are co-related in (3.14) for sinusoidal excitation waveforms (Dowell's eq. [143]):

$$\frac{R_{\rm AC}}{R_{\rm DC}} = \Delta \left[\frac{\sinh\left(2\Delta\right) + \sin\left(2\Delta\right)}{\cosh\left(2\Delta\right) - \cos\left(2\Delta\right)} + \frac{2\left(p^2 - 1\right)}{3} \frac{\sinh\left(\Delta\right) - \sin\left(\Delta\right)}{\cosh\left(\Delta\right) + \cos\left(\Delta\right)} \right] \quad , \tag{3.14}$$

being $\Delta = h_{\rm cu}/\delta_{\rm sd}$ and p the number of layers as depicted in Fig. 3.6.

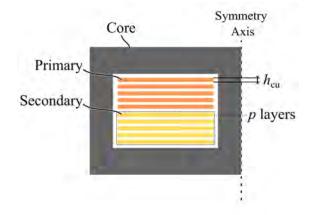


Figure 3.6 Illustration of the front view of a planar transformer.

However, this is not applicable to non-sinusoidal excitation waveforms that are utilized in many power converter topologies. To determine the AC resistance in those cases, (3.15) is given in [142]:

$$\frac{R_{\rm AC}}{R_{\rm DC}} = \frac{1}{\Delta} + \frac{\Psi}{3} \Delta^3 \left(\frac{I'_{\rm RMS}}{\omega I_{\rm RMS}}\right)^2 ,$$
where $\Psi = (5p^2 - 1)/15$.
$$(3.15)$$

The analytical models to determine the RMS current $(I_{\rm RMS})$ and its derivative $(I'_{\rm RMS})$ are found in [142]. In Fig. 3.7 the $R_{\rm AC}/R_{\rm DC}$ resistance ratio is plot versus Δ and the number of layers (p) when considering DAB and ABAC excitation waveforms. It is clear that the resistance ratio is higher when the number of layers is increased for $\Delta > 0.5$. However, this ratio is quasi constant for $\Delta < 0.5$, and the AC resistance is higher as lower is Δ . Therefore, it is possible to find the trade-off between Δ and p in which $R_{\rm AC}/R_{\rm DC}$ ratio is minimum. Theoretically, a copper thickness $(h_{\rm cu})$ equal to the skin depth is enough to reduce the skin effect if a single layer is considered. However, as larger is the number of layers, the value of $h_{\rm cu}$ must be reduced in order to counteract the proximity effect.

This method is useful to have a first look of the copper thickness regarding the skin depth of the application (skin effect) and the number of layers (proximity effect) to find the optimal AC resistance in the windings of the transformer. Other method to reduce the effect of proximity is the interleaving of the windings. This methodology is explained in depth in the next subsection since it is a relevant strategy to define the leakage inductance of the transformer.

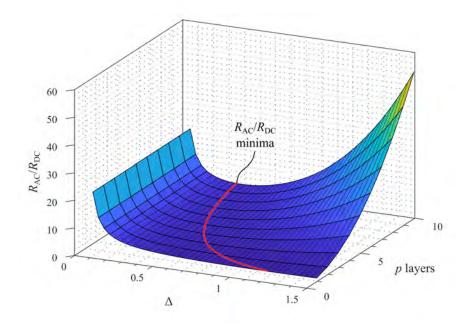


Figure 3.7 $R_{\rm AC}/R_{\rm DC}$ ratio versus Δ and p considering DAB and ABAC waveforms.

3.5.2 Leakage Inductance

As stated before, the leakage inductance emerge from the magnetic flux that does not link both windings of the power transformer, causing a non-ideal coupling between them. In some applications, the value of the leakage inductance is reduced to the minimum possible to avoid the non-idealities that arise from this inductance, as the overvoltage spikes in the drain-to-source voltage of the power devices. However, this is not the case of DAB and ABAC converters, where the leakage inductance (L_k) is commonly utilized as the decoupling inductance of the converter (L_{σ}) . In these converters, L_{σ} define the power transfer level of the converter. Then, reducing the value of L_k means that another inductance must be connected in series to reach the desired value. This fact implies some disadvantages for the power converter, as the necessity of a design stage of this component, the increment of the volume and/or weight and the reduction of the converter efficiency.

Different analytical models have been proposed in literature for the computation of the leakage inductance. A comparison of the accuracy and computational effort of the most applied methods have been studied in [144], providing the advantages and disadvantages of each method. In this work, the analytical models proposed in [70] for the calculation of the leakage inductance, which shows an excellent accuracy versus FEA and experimental results.

In Fig. 3.8 the magnetic field strength inside the window area of a power transformer has been depicted from FEA simulations. The leakage inductance can be accurately computed by determining the integral of the magnetic flux strength in the whole window area, typically utilized in the method of images [145]. However, the analytical model of [70] computes the leakage inductance based on the energy stored by a magnetic field referred to the primary side, which is given by (3.16):

$$E = \frac{1}{2} \int B H \, dV = \frac{1}{2} L_{\rm k} I_1^2 \quad . \tag{3.16}$$

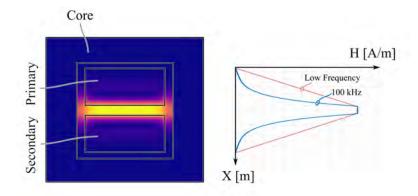


Figure 3.8 Magnetic field strength in the window area of a ferrite core with two conductors carrying currents in opposite directions.

Considering the B-H relationship and substituting the differential volume leads to the equation (3.17):

$$E = \frac{\mu_0}{2} \sum \int_0^{h_{\rm cu}} H^2 \, l_{\rm w} \, b_{\rm w} \, dx \quad , \tag{3.17}$$

where $l_{\rm w}$ and $b_{\rm w}$ are the length and the width of the winding wire.

After the corresponding mathematical development, we arrive to (3.18), which can be applicable to any winding arrangement of planar transformers:

$$L_{\rm k} = \mu_0 \frac{l_{\rm w}}{b_{\rm w}} \left[\frac{k_1 h_{\rm cu1} + k_2 h_{\rm cu2}}{3} + M_{\rm s} \left(\frac{k_1}{b_{\rm w}} \right)^2 h_{\rm ins12} + \sum_{k_1=0}^{k_1-1} \left(\frac{k_1}{b_{\rm w}} \right)^2 (h_{\rm ins1} + h_{\rm ins12}) + \sum_{k_2=0}^{k_2-1} \left(\frac{k_2}{b_{\rm w}} \right)^2 (h_{\rm ins2} + h_{\rm ins12}) \right] , \quad (3.18)$$

being $k_1 = n_1/M_s$, $k_2 = n_2/M_s$. Furthermore, h_{ins1} , h_{ins2} and h_{ins12} are the primaryto-primary, secondary-to-secondary and primary-to-secondary insulation distances. The number of magnetic sections M_s plays an important role when trying to minimize the leakage inductance and the AC resistance of the transformer. To this aim, interleaving strategies are commonly considered (see Fig. 3.9). This arrangements help to reduce the magnetic field strength level, as well as the enclosed area below its shape, defining the value of both parameters. Therefore, the number of magnetic sections are commonly increased when it is necessary to reduce the AC resistance due to the proximity effect or the leakage inductance.

In the MEA application that is scope of this work, the leakage inductance is specially important in order to achieve the required decoupling inductance value. To satisfy this requirement, the insulation distances $(h_{ins1}, h_{ins2} \text{ and } h_{ins12})$ and the number of magnetic sections are the free parameters that will be set carefully once the transformer turns ratio and core size are defined. A comprehensive evaluation of these parameters for the optimal design of DAB and ABAC is done along Chapter 4.

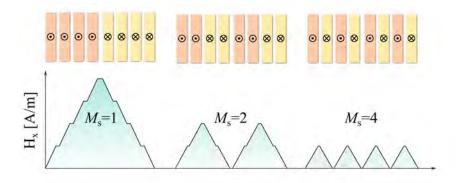


Figure 3.9 Magnetic field strength in the window area of a ferrite core with two conductors carrying currents in opposite directions.

3.5.3 Stray Capacitances

The final passive component that defines the behavior of a power transformer are the stray capacitances. These capacitances form a resonant tank with the leakage inductances of the transformer, originating high-frequency oscillations on the transformer voltage waveforms [146, 147]. Stray capacitances are typically modeled as a single capacitance primary referred. Nevertheless, these capacitances appear in primary and secondary terminals, as well as between primary and secondary [69]. Then, the impact on primary and secondary sides of the power converter must be carefully considered, specially at high operating frequencies since these capacitances affect on the switching performance of the power devices [148]. In this section, a review of the calculation of the stray capacitances is done together with its determination considering a concrete winding arrangement in a multi-layer PCB.

An illustration of the winding arrangement of the planar transformer for DAB converter is shown in Fig. 3.10(a) as example. The transformer turns-ratio is 10 for this converter, the selected turns for this example are $n_1=10$ and $n_2=1$. It is important to note that there is no secondary-to-secondary (C_{22}) since in the secondary winding the four layers of the PCB are connected in parallel to reduce the current density per layer, i.e. equipotentials surfaces. Therefore, only primary-to-primary and primary-to-secondary stray capacitances are present in the windings of the transformer taken as example.

The calculation of each stray capacitance is simple in a planar transformer considering the formula of the capacitance between two parallel plates (3.19):

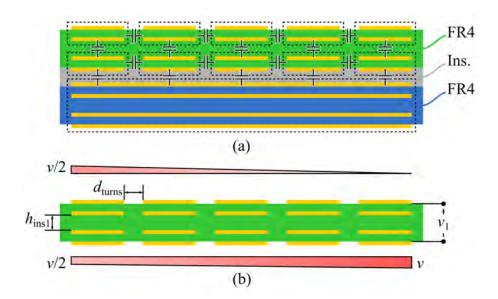


Figure 3.10 Winding arrangement of the power transformer of a DAB converter. Calculation of stray capacitances (equipotential or parallel turns are grouped inside dashed line rectangles): (a) primary and secondary windings together with the layer-to-layer and turn-to-turn capacitances and (b) linear voltage distribution.

$$C = \varepsilon_0 \,\varepsilon_\mathrm{r} \, \frac{S}{h_\mathrm{ins}} \quad , \tag{3.19}$$

where ε_0 is the permittivity of the air, ε_r is the relative permittivity of the insulator material, S is the surface area of the plates facing each other and h_{ins} is the distance between plates, i.e. insulator material. The calculation of the equivalent stray capacitance in each case is related to the associated layer-to-layer stored energy while the turn-toturn capacitance is considered negligible due to the small surface area facing each turn [69]. Considering a linear voltage drop per turn as depicted in Fig. 3.10(b), the voltage distribution per turn is determined with (3.20):

$$V_{\rm i} = \frac{(n_{\rm l}+1)-i}{n_{\rm l}} V$$
, where $i = (1, 2, 3, ..., n_{\rm l})$, (3.20)

being n_1 the number of turns per layer, V_i the voltage drop between the faced layers and V the total voltage applied to the terminals. Assuming that the total energy stored in this winding is the sum of the stored energy between each layer (3.21):

$$E = \sum_{i=1}^{n_{l}} E_{i} = \frac{1}{2} C V^{2} \sum_{i=1}^{n_{l}} \left(\frac{(n_{l}+1) - i}{n_{l}} \right)^{2} = \frac{(n_{l}+1) (2n_{l}+1)}{12n_{l}} C V^{2} , \qquad (3.21)$$

the equivalent capacitance of the winding is given by (3.22):

$$C_{\rm eq} = K_{\rm Ceq} C$$
, where $K_{\rm Ceq} = \frac{(n_{\rm l} + 1) (2 n_{\rm l} + 1)}{6n}$. (3.22)

This approximation with analytical models have been validated with a FEA simulation model, which is depicted in Fig. 3.11. The validation shows a good correlation between analytical and FEA regardless the insulation and the turn-to-turn distances (h_{ins1} and d_{turns}).

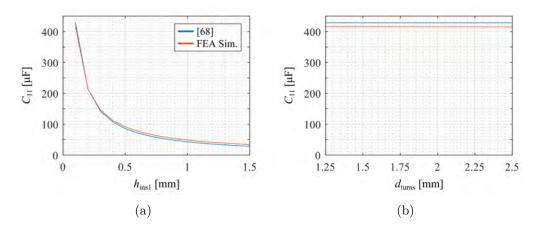


Figure 3.11 Validation of the analytical models found in [69] for the calculation of the stray capacitances.

Along this section, a simple description of the capacitance model in a planar transformer is presented, which is easily modeled according the capacitance between parallel plates [69]. The calculation methodology is simple and easy to apply, taking into account all the layer-to-layer capacitances. Furthermore, it is clear that there is a trade-off between the leakage inductance (proportional) and stray capacitances (inversely proportional) due to the impact of the insulation distances.

3.6 Determination of the Power Losses

In magnetic components, there are two sources of power losses: those that proceed from the windings due to the Joule effect produced in the current conduction and those generated in the core losses from its magnetization. In this section, a review of the calculation of these losses is detailed, which are afterwards utilized in the optimization process proposed in Chapter 4.

3.6.1 Winding Losses

The winding losses are directly related with the current waveform that flows through the component under study. Depending on the device, it can be an AC (transformers and/or AC inductors) or DC plus AC (DC inductors). Due to this fact, the characterization of the winding losses are closely related with the harmonic content of the current waveform (see Fig. 3.12). The harmonic content of the current waveform that flows through the power transformer windings is similar in the different modulation methods considered for the DAB converter, and its contribution is negligible from harmonic number 20 onwards.

As previously stated, the current distribution and AC resistance depend on the winding arrangement and the operating frequency (see section 3.4.1). Thus, the power losses

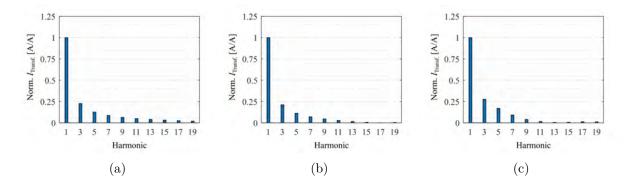


Figure 3.12 Normalized FFT of the current waveform that flows through the primary winding of the power transformer in DAB converter (at 270V/22V and 20% of load conditions in each case): (a) SPS Rectangular modulation, (b) TPS-TPM and (c) TPS-TRM.

characterization due to the conduction behavior must be done by calculating the corresponding AC resistance at the operating frequency and its harmonics. Then, the power losses in the copper of the PCBs that are part of the transformer windings are calculated according:

$$P_{\rm cu} = N_{\rm PCB} R_{\rm AC} \left(f \right) I_{\rm Trans} \left(f \right)^2 \quad , \tag{3.23}$$

where $P_{\rm cu}$ are the total winding losses in the transformer, $N_{\rm PCB}$ is the number of PCBs, $R_{\rm AC}(f)$ is the AC resistance at the frequency of the corresponding harmonic and $I_{\rm Transf}$ is the RMS contribution of each harmonic to the current that flows through the transformer. Finally, the total losses in the copper are computed by adding those that are produced in primary and secondary windings respectively.

3.6.2 Core Losses

The determination of the core losses in a power transformer has been characterized in different ways, which can be applicable depending on the waveform of the excitation voltage. A review of these methodologies is found in [50]. Although the original Steinmetz equation is applicable to sinusoidal waveforms, the majority of the magnetic devices that are found in the modern PECs are excited with non-sinusoidal voltages. This is the case of DAB and ABAC converters, being both excited with square or quasi-square voltage waveforms. Among the different methods that are utilized, the core losses are characterized according the improved Generalized Steinmetz Equation (iGSE).

In this work, the PWL models proposed in [50] are applied. First, the maximum magnetic flux density $(B_{\rm m})$ in function of the applied voltage to primary terminals $(V_{\rm HV})$, the number of primary turns (n_1) , the area of the magnetic core $(A_{\rm c})$, the switching period (T) and the zero-voltage period (T_{Ω}) is defined by (3.24):

$$B_{\rm m} = \frac{1}{2} \frac{V_{\rm HV}}{n_1 A_{\rm c}} \left(\frac{T}{2} - T_{\Omega}\right) , \text{ where } T_{\Omega} = \Omega \frac{T}{2\pi} . \tag{3.24}$$

Then, the time domain PWL function that defines the shape of the magnetic flux density is settled in (3.25):

$$B(t) = B_{\rm m} \begin{cases} -1 + \frac{1}{TD}t & \text{if } 0 < t < \frac{T}{2} - T_{\Omega} \\ 1 & \text{if } \frac{T}{2} - T_{\Omega} < t < \frac{T}{2} \\ 1 - \frac{1}{TD}\left(t - \frac{T}{2}\right) & \text{if } \frac{T}{2} < t < T - T_{\Omega} \\ -1 & \text{if } T - T_{\Omega} < t < T \end{cases}$$
(3.25)

being D the duty cycle of the voltage waveform.

These models aids the designer to determine the shape of the magnetic flux density when the transformer is excited with a non-sinusoidal waveform [see Fig. 3.13(a)]. Furthermore, the simplicity of the model is useful to determine the core losses of the transformer. As previously mentioned, this losses are modeled in this work with the iGSE method, being the core losses density (P_v) determined with (3.26):

$$P_{\rm v} = 2^{(\alpha+\beta)} k_{\rm i} f^{\alpha} B_{\rm m}{}^{\beta} \left(1 - \frac{\Omega}{\pi}\right)^{1-\alpha} ,$$

where $k_{\rm i} = \frac{K_{\rm c}}{2^{(\beta-1)} \pi^{\alpha-1} \left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)} .$ (3.26)

The core losses and maximum magnetic flux densities are depicted in Fig. 3.13(b) for different zero-voltage periods when the applied DC voltage is 270 V and the number of primary turns are 10. It is clear that the maximum flux density decrease linearly as higher is Ω , which directly impacts on the core losses density with a noticeable reduction. Since TPS modulation methods work with higher Ω values, the core losses are lower in these modulation due to the reduction of the maximum magnetic flux density. Therefore, the worst case evaluation must be done in SPS rectangular modulation.

Although iGSE shows the lowest error between calculated and real losses [50], there is a deviation in the estimation due to losses that are produced at zero-voltage periods. This fact has been solved in [149] with a new improved methodology that increase the number of Steinmetz parameters extracted to accurately determine the core loss density. Nevertheless, the extraction of these parameters is done with experimental test that must be performed carefully and stunts the design process. Therefore, iGSE is considered in this work to compute the core losses in the magnetic devices.

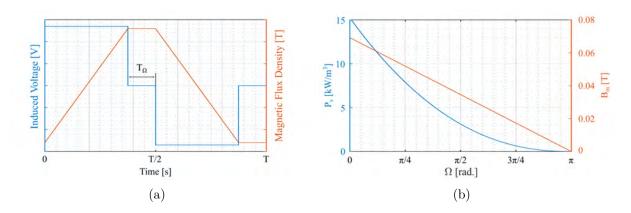


Figure 3.13 (a) Magnetic flux density and induced voltage at $\Omega = \pi/4$ and (b) core losses density evolution for different zero voltage periods.

3.7 Thermal Behavior

One of the most important parameters in the performance of a power transformer is the temperature rise. It must be assured that the operating temperature of the devices does not exceed the Curie's temperature, above which the core material losses its magnetic properties. A common used method for the estimation of the temperature reached in the core of the transformer is employed in [61]. However, this method applies a factor that is extracted with experimental results in [150] from empirical data for specific core geometries.

3.7.1 Heat Transfer Mechanisms

In order to accurately predict the temperature rise in the magnetic devices, the thermal model proposed in [60] is adapted in this work for planar cores. First, the fundamentals of heat transfer are reviewed in this section. There are three mechanism involved in the heat transfer [151]: conduction, convection and radiation (see Fig. 3.14).

Conduction

The heat transfer by conduction occurs between two areas of the same body and/or two bodies in contact that are at different temperatures. The amount of heat transferred (Q)is proportional to the area in contact (A), the thermal conductivity of the material (λ) as well as to the temperature gradient (∇T) [152]:

$$Q = -\lambda A \nabla T \quad , \tag{3.27}$$

Then, the heat transferred per area unit (q) is defined from (3.27) as a function of the conduction heat transfer coefficient (h_{cond}) in (3.28):

$$q = h_{\text{cond}} \Delta T$$
, where $h_{\text{cond}} = \frac{\lambda}{\Delta x}$. (3.28)

In the conduction heat transfer, Δx represents the distance between the considered areas.

Convection

The second kind of heat transfer is known as convection due to the exposure of a surface to a flowing fluid [153]. This heat transfer process is dependent on the velocity and type

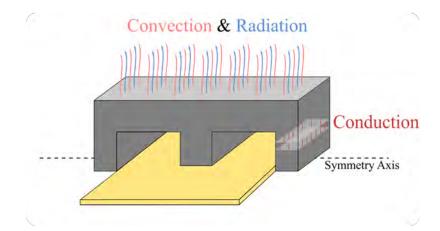


Figure 3.14 Illustration of the heat transfer mechanisms in a planar transformer core.

of fluid, which is defined with the Newton law of cooling as (3.29):

$$q = h_{\rm conv} \Delta T$$
, where $h_{\rm conv} = N u \frac{\lambda}{\Delta x}$, (3.29)

being Nu the Nusselt number, Δx the length of the surface being cooled by the fluid and h_{conv} the conductive heat transfer coefficient. A deep description to determine Nu as a function of the Grasshof and Prandtl numbers (Gr and Pr) is found in [63]. Furthermore, Δx in convection heat transfer is the length of the surface that is exposed to the flowing fluid.

Radiation

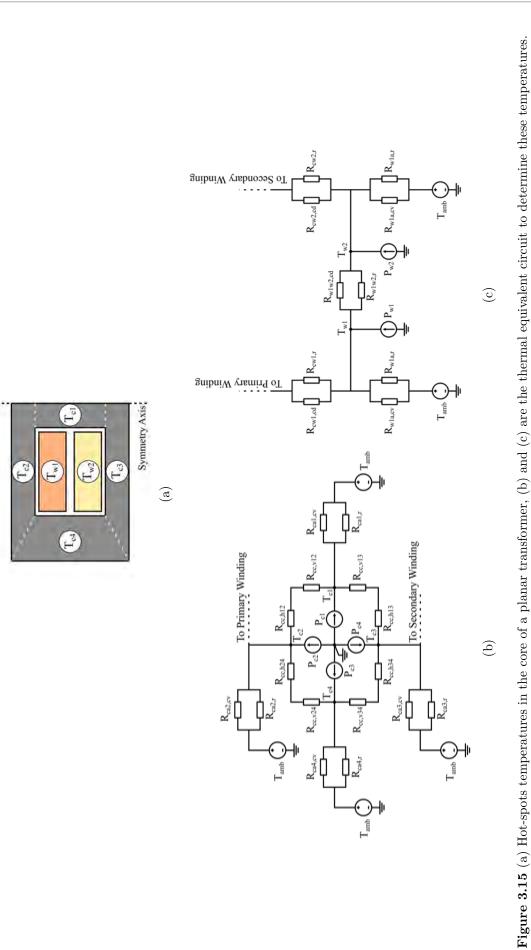
The last heat transfer method is called radiation. This phenomena takes place in any state of matter (solid, liquid or gas) due to the energy that is radiated, which can be absorbed, reflected and/or transmitted once it reach another surface. According to [151], the heat that is transferred by radiation is defined by (3.30):

$$q = \varepsilon \sigma \left(T_1^4 - T_2^4 \right) = h_{\text{rad}} \Delta T$$
, where $h_{\text{rad}} = \frac{\varepsilon \sigma \left(T_1^4 - T_2^4 \right)}{\Delta T}$, (3.30)

being ε emissivity of the material, σ the Stefan-Boltzmann constant, i.e. 5.669·10⁻⁸, and $h_{\rm rad}$ the radiation heat transfer coefficient.

3.7.2 Thermal Network Model

The equivalent network utilized in this work is based on the thermal resistances that involve the conduction, convection and radiation heat transfer mechanism. This model has been presented and validated for conventional core geometries in [60, 62]. The methodology proposed is adapted in this work to planar core geometries as depicted in Fig. 3.15.



The hot-spots temperatures in stationary state of a planar transformer are calculated by solving the thermal equivalent circuit presented in Fig. 3.15(a) and 3.15(c) with the matrix equation given in (3.31) [63]:

$$0 = R_{th1}T + R_{th2}U$$
 (3.31)

where T is the matrix of the temperature in each node, U is the matrix that contains the external excitations and R_{th} are the matrices that contains the thermal resistances of the model. In the case of study settled in this work, these matrices are defined as:

$$T = \begin{bmatrix} T_{c1} \\ T_{c2} \\ T_{c3} \\ T_{c4} \\ T_{w1} \\ T_{w2} \end{bmatrix} \qquad U = \begin{bmatrix} P_{c1} \\ P_{c2} \\ P_{c3} \\ P_{c4} \\ P_{w1} \\ P_{w2} \\ T_{amb} \end{bmatrix} , \qquad (3.32)$$

$$\mathbf{R}_{\text{th1}} = \begin{bmatrix} LD_1 & \frac{1}{R_{\text{cc},12}} & \frac{1}{R_{\text{cc},13}} & 0 & 0 & 0\\ \frac{1}{R_{\text{cc},12}} & LD_2 & 0 & \frac{1}{R_{\text{cc},24}} & \frac{1}{R_{\text{cw},1}} & 0\\ \frac{1}{R_{\text{cc},13}} & 0 & LD_3 & \frac{1}{R_{\text{cc},34}} & 0 & \frac{1}{R_{\text{cw},2}}\\ 0 & \frac{1}{R_{\text{cc},24}} & \frac{1}{R_{\text{cc},34}} & LD_4 & 0 & 0\\ 0 & \frac{1}{R_{\text{cw},1}} & 0 & 0 & LD_5 & \frac{1}{R_{\text{w1w}2}}\\ 0 & 0 & \frac{1}{R_{\text{cw},2}} & 0 & \frac{1}{R_{\text{w1w}2}} & LD_6 \end{bmatrix}, \quad \mathbf{R}_{\text{th2}} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & \frac{1}{R_{\text{ca}}}\\ 0 & 1 & 0 & 0 & 0 & 0 & \frac{1}{R_{\text{ca}}}\\ 0 & 0 & 0 & 0 & 0 & \frac{1}{R_{\text{w1w}}}\\ 0 & 0 & 0 & 1 & 0 & 0 & \frac{1}{R_{\text{w1w}2}} \end{bmatrix}.$$

$$(3.33)$$

The elements of the leading diagonal $(LD_1 \text{ to } LD_6)$ are determined with:

$$LD_{1} = -\left(\frac{1}{R_{cc,12}} + \frac{1}{R_{cc,13}} + \frac{1}{R_{ca,1}}\right) \quad LD_{2} = -\left(\frac{1}{R_{cc,12}} + \frac{1}{R_{cc,24}} + \frac{1}{R_{cw,1}} + \frac{1}{R_{ca,2}}\right)$$

$$LD_{3} = -\left(\frac{1}{R_{cc,13}} + \frac{1}{R_{cc,34}} + \frac{1}{R_{cw,2}} + \frac{1}{R_{ca,3}}\right) \quad LD_{4} = -\left(\frac{1}{R_{cc,24}} + \frac{1}{R_{cc,34}} + \frac{1}{R_{ca,4}}\right)$$

$$LD_{5} = -\left(\frac{1}{R_{cw,1}} + \frac{1}{R_{w1w2}} + \frac{1}{R_{w1a}}\right) \quad LD_{6} = -\left(\frac{1}{R_{cw,2}} + \frac{1}{R_{w1w2}} + \frac{1}{R_{w2a}}\right)$$

$$(3.34)$$

Finally, the temperatures in the core and the windings are determined by rearranging (3.31) into (3.35):

$$T = -R_{\rm th1}^{-1} \ (R_{\rm th2} U) \tag{3.35}$$

In these matrices, the thermal resistances are calculated from the conduction, convec-

tion and radiation coefficients with (3.36):

$$R_{\rm cd,cv,r} = \frac{1}{h_{\rm cd,cv,r} A} \quad , \tag{3.36}$$

where $h_{cd,cv,r}$ are the conduction, convection or radiation heat transfer coefficients and A is the considered heat transfer area.

3.8 DC Inductor Design

In this work, the design of the DC inductors included in ABAC converter is done according the procedure detailed in [41]. First, the specifications of the inductor are given, i.e inductance, current ripple ratio, DC current, frequency, filling factor and maximum desired temperature gradient. Once the specifications are set and the magnetic material is selected, the optimum permeability is calculated in (3.37):

$$\mu_{\rm opt} = \frac{B_{\rm sat} \, l \, r_{\rm I}}{\mu_0 \sqrt{\frac{P_{\rm max} \, N \, W_{\rm a}}{\rho_{\rm w} \, M L T}}} \quad , \tag{3.37}$$

where P_{max} are the maximum power losses allowed in this component and N are the number of turns. Then, the area product of the DC inductors is computed with (3.38):

$$A_{\rm p} = \left[\frac{\sqrt{1+\gamma} r_{\rm I} L I_{\rm pk}^2}{B_{\rm m(Lo)} K_{\rm t} \sqrt{k_{\rm u} \Delta T}}\right] \quad , \tag{3.38}$$

being γ the ratio between copper and core losses, i.e. close to zero when considering low AC current ripples. The following step is to determine the required gap length (3.39), which is commonly employed in this component to increase the energy that can be stored in the core:

$$g = \frac{l}{\mu_{\text{opt}}} \quad . \tag{3.39}$$

Finally, the number of turns are calculated with (3.40):

$$N = \sqrt{\frac{L_{\text{out}} l}{\mu_{\text{opt}} A_{\text{c}}}} \quad . \tag{3.40}$$

The last steps in the design procedure are to determine the copper and core losses of this component in order to predict the maximum temperature in the core and windings. This process is done according the analytical models previously given in this chapter.

3.9 Conclusions

The fundamentals of the behavior of a power transformer have been described in this chapter according the literature of this components. First, the performance factor of ferrite magnetic materials have been revisited for the sizing of the core considering the specifications imposed by the application. Furthermore, the equivalent circuit of the power transformer has been characterized along with the equations that determine its principle of behavior. Then, the frequency phenomena, i.e. skin depth and proximity effects, that impact on the performance of this device have been presented.

Secondly, the analytical models to calculate the passive elements as AC resistances, leakage inductances and stray capacitances are given and discussed. These elements play an important role on the real behavior of the component, since they determine the winding losses, power transfer and undesired ripples on the converter waveforms respectively.

Finally, the heat transfer mechanisms and the thermal model to determine the temperatures on the core and windings of the transformer have been detailed. This is one of the most important studies in the design of a power transformer in order to not exceed the Curie temperature in the core, above which the performance and reliability of this component is compromised.

4

Optimal Design Methodology for MEA

Summary:

Efficiency, power density and cost are the most important parameters when designing a power converter for the electric aircraft. Therefore, the main contributions of this work to the analytical modeling of the most promising power converter topologies are utilized in this chapter to obtain a roadmap of the trade-offs among these variables. Then, a brute force optimization algorithm is developed for the design stage of ABAC and DAB converters.

4.1 Introduction

Nowadays, the complexity of the design of PECs is constantly increasing regardless of the application proposal. There are a wide number of available topologies and modulation and/or control methods. Furthermore, the different semiconductor (i.e. SiC, GaN and/or Si), heatsink (i.e. natural and/or forced convection, water cooled, thermal conductivity of the material) and capacitor [i.e. aluminum-electrolytic, film, Multi-layer Ceramic Capacitors (MLCC)] technologies hinder the evaluation of the most important parameters to take into account in the design stage of the power converter, as the efficiency, volumetric and/or gravimetric power density or the cost per kilowatt. Therefore, the MOO of PECs is frequently required in power electronics designs to obtain a roadmap of the whole design space diversity.

In Fig. 4.1, the illustration of the basic concepts of a MOO procedure proposed in [154] is depicted. The decisions that are commonly done by the designer starts with the most abstract, as the selection of the converter topology, the modulation and/or control algorithms, as well as the technology of each components. Then, the system and component models are utilized to determine the performance of the converter, e.g. efficiency, power density and/or total cost. Finally, the results are typically presented on Pareto plots to evaluate the trade-offs that lead to the optimal converter. In this representation, the power density limit due to the technology constraints is patent. Furthermore, there is no chance to increase the power density by decreasing the efficiency of the converter since the temperature limit of the components, e.g. Curie temperature of the power transformer and junction temperature of the switching devices, avoid this trade-off. A deep insight into the upcoming technology challenges of PECs is discussed in [155], as well as the exploration of a Pareto front optimization of a single-phase Power Factor Correction (PFC) system in [156].

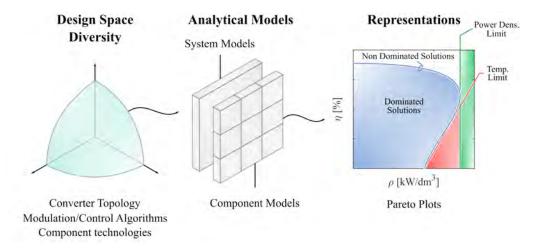


Figure 4.1 Illustration of the MOO concepts for power electronics designs. Adapted from [154].

There are numerous studies that characterize the impact of the trade-off between efficiency (η) and power density (ρ) by exploring the design space of the whole converter [157]- [159]. Furthermore, the design space can be analyzing by focusing on each different component, such as inductors [160], capacitors [161, 162] and/or the power transformer [163]. The wide number of optimization methods available makes difficult to select one methodology. A review of the most common optimization methods found in power electronic designs is discussed in [80]. In this work, the optimization methodology is brute-forced based, which means that the input variables are set in the discrete domain to perform a parametric sweep of all the possible combinations. This method is probably the simplest and easiest to implement when trying to solve an optimization problem. However, the computational cost of this method is the major disadvantage and requires of high-quality coding to increase the speed of the software. Furthermore, parallel computing is typically utilized in brute force optimizations to reduce the computation time.

Despite the fact that it is not considered in this work, the utilization of artificial intelligence for the optimization methods of PECs is acquiring a large importance, especially in the field of magnetic components. In this sense, it is possible to find genetic algorithms [61, 164] as well as neuronal networks [62] to solve the MOO of the control of specific power converters, the design of the power transformer stage and/or the modeling and design of inductors. These optimization methods also carry disadvantages, as the high amount of data required in artificial neuronal networks and/or the properly selection of the cost functions and domain limits in genetic algorithms. In the case of neuronal networks, a common solution is to feed it with a combined analytical, simulation and experimental data, while the genetic algorithms require of a high-expertise of the optimization target to set all the free parameters properly.

Therefore, this chapter deals with the MOO of DAB and ABAC converters with a brute forced optimization algorithm. The methodology employed utilizes the analytical models developed in this work just as the component models presented in Appendix A to reduce the computational effort. Then, the results obtained allow to obtain a roadmap of these converters when considering MEA applications, aiding the designer to select the scenarios and component technologies that enable the utilization of these topologies. Hereafter, the MOO procedure is presented. Afterwards, the results of the MOO are presented and discussed, focusing on the free parameters of the optimization that allow to arrive to the non-dominated solutions of the Pareto plot. Also, two comparative studies are aimed, first to analyze the impact of the technology of each component on the efficiency and/or power density of the converter, and also to analyze the results of the optimization of both converters with the same component technology. Finally, the conclusions of these optimization methodology are given.

4.2 Multi-Objective Optimization Procedure

The multi-objective optimization presented in this work allows the designer to analyze the values of the design variables that lead to the best trade-off between efficiency, power density, and the leakage to decoupling inductances error.

The flowchart of the MOO procedure is presented in Fig. 4.2. The design space variables that are swept in this optimization procedure are the switching frequency (f_{sw}) , the limit of the modulation angle (δ_{lim}) , the number of PCBs set in parallel in primary and secondary windings of the power transformer $(N_{p1} \text{ and } N_{p2})$, the copper thickness of

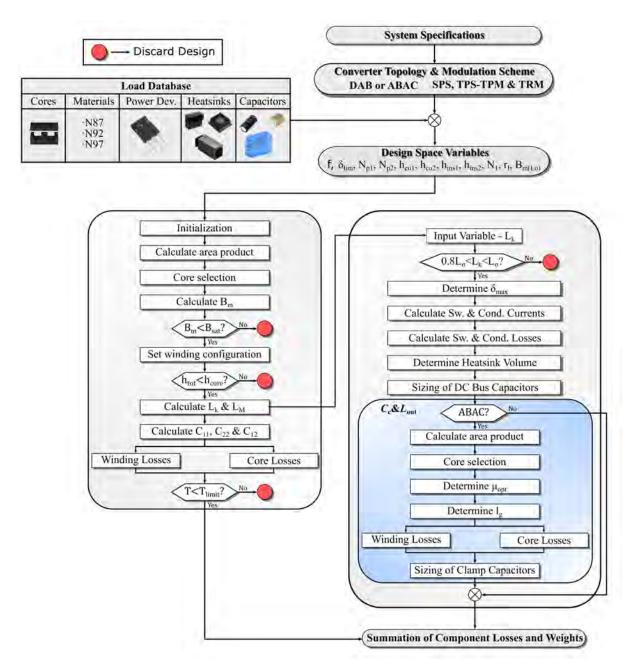


Figure 4.2 Flowchart of the MOO procedure.

these windings (h_{cu1} and h_{cu2}), the insulation distances (h_{ins1} , h_{ins2} and h_{ins12}) and the number of turns of the primary winding (n_1). In the case of ABAC converter, the AC-DC current ripple ratio (r_I) and the maximum magnetic flux of the output inductors ($B_{m(Lo)}$) are also analyzed.

In the first steps, the specifications of the system, the topology of the power converter and the modulation method are set. A database is loaded into the application to evaluate the performance of different component technologies. Then, after the selection of the values of each design space variable, the procedure starts with the design of the power transformer, where the resulting area product is calculated to select the required core size [see (3.3)]. Afterwards, the resulting maximum flux density of the transformer ($B_{\rm m}$) is computed [see (3.24)]. The design is discarded if the value obtained is higher than the saturation flux density ($B_{\rm sat}$) of the magnetic core. After that, the winding configuration is established, where the total height of the windings ($h_{\rm tot}$) is compared to the height of the core window ($h_{\rm core}$). The following step is to determine the leakage and magnetizing inductances [$L_{\rm k}$ and $L_{\rm M}$, according (3.18) and (3.11) respectively], as well as the stray capacitances of the transformer [C_{11} , C_{22} and C_{12} with (3.22)]. To conclude with the power transformer stage, winding and core losses are computed as given in (3.23) and (3.26) respectively, together with the temperature rise in the transformer core and windings (view Section 3.7.2).

The leakage inductance of the power transformer is compared to the decoupling inductance [see (2.2)] of the converter, discarding designs in which the error is over 20%. Then, the maximum modulation angle (δ_{max}) and switching and conduction currents and losses (as detailed in Section 2.5) are calculated to size the heatsink, and the DC bus capacitors (section 2.2.3). Output inductors and clamp capacitors of ABAC converter are designed for different $r_{\rm I}$ and $B_{\rm m(Lo)}$ values. Here, the optimum permeability is determined to find the gap length that is required in the core. Also, the winding and core losses of these magnetic components are computed. Clamp capacitors are sized to handle the voltage ripple and RMS current requirements. Finally, the losses of all the components, as well as the volumes, are computed to determine the efficiency and volumetric power density of each PEC.

The design space variables and specifications considered for the MOO are presented in Table 4.1, which determine the efficiency, volume and/or weight and leakage to decoupling inductance accuracy of the PECs. As previously stated, these variables impact on the design of each component of the PEC, e.g. by minimizing the reactive power that flows through the converter (δ_{lim}) and/or the current density on the transformer windings (h_{cu} and N_p). Furthermore, the MEA specifications of voltage ripple on DC buses determine the capacitance of the DC bus capacitors. Also, the AC-DC current ripple ratio impact on the copper losses of the output inductors (L_o), as well as in the ZVS areas of the ABAC converter. These are examples in which the variables presented in Table 4.1 impact on the efficiency and/or power density of the PECs considered in this work.

Parameter	Symbol	Value		Step	Units
		min.	max.		
Frequency	f	50	200	25	kHz
Limit of the modulation angle	δ_{lim}	10	90	10	0
Paralleled PCB (Pri. & Sec.)	$N_{\rm p1} \ \& \ N_{\rm p2}$	1	5	1	-
Copper thickness (Pri. & Sec.)	$h_{\rm cu1} \& h_{\rm cu2}$	0.035	0.4	-	mm
Ins. distance (Pri. & Sec.)	$h_{\text{ins1}} \& h_{\text{ins2}}$	0.4	1.6	0.4	mm
Ins. distance (PriSec.)	h_{ins12}	0.5	2.5	0.5	mm
Number of turns (Pri.)	N_1	10	20	10	-
AC-DC current ratio	$r_{\rm I}$	0.25	0.75	0.25	-
Max. magnetic flux density	$B_{\rm m(Lo)}$	100	300	25	mT
		ABAC	DAB		
DC input voltage	$V_{\rm HV}$	250-280			V
DC output voltage	$V_{\rm LV}$	22-29			V
Transformer turns ratio	n	5	10		-
Input voltage ripple	$\Delta V_{\rm HV}$	3			V
Output voltage ripple	$\Delta V_{\rm LV}$	0.75			V
Clamp capacitor voltage ripple	$\Delta V_{\rm Cc}$	6			V
Nominal power	$P_{\rm nom}$	1			kW

 Table 4.1 Design space variables of the MOO.

4.3 Pareto Optimization Results

Efficiency and power density are the most important parameters when designing power converters for MEA applications. Therefore, a brute force based multi-objective optimization procedure has been developed in this work for the most promising bidirectional isolated DC-DC topologies for MEA applications.

The results of the MOO procedure are presented in Fig. 4.3. In Fig. 4.3(a) and 4.3(b), the optimal designs for DAB and ABAC PECs are shown considering the same capacitor

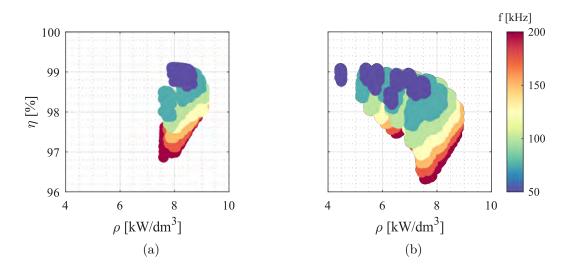


Figure 4.3 η - ρ Pareto optimization for: (a) DAB and (b) ABAC PECs considering selecting the same capacitor technology (MLCC) and heatsink CSPI (10.86).

technology (MLCC) and Cooling System Performance Index (CSPI), i.e. 10.86, of the aircooled heatsink [165]. Both η and ρ values are quite similar for both converters. However, it is important to note that the achievable ρ is noticeable higher at low frequencies in DAB converter, which is caused by the fact that the ABAC converter is penalized in this range by the inclusion of the output inductors. As frequency increases, the drawback of including these inductors is lower, while the impact on the η is larger than in DAB converter. This study identifies the trade-offs that theoretically lead to the Pareto-optimal designs. It is important to note that the results presented in Fig. 4.3 consider that the volume of the magnetic core in the power transformer (DAB and ABAC) and output inductors (ABAC) is proportional to the resulting area product (see Appendix A.3). Actually, power converter designers are limited to the selection of commercial cores, which slightly modifies the results presented in Fig. 4.3.

In Fig. 4.4, the designs that fall on the Pareto-front are presented for DAB converter to get a deep insight of the design space variables that lead to the optimal η - ρ - ΔL trade-off. A common trend found in power electronics is observed when increasing the switching frequency (f), which decrease the efficiency of the converter due to the higher switching losses while enhancing the power density by reducing the volume and/or weight of the passive devices that are included in the PEC. Furthermore, it is noticeable that the limit of the modulation angle (δ_{lim}) is set to low values to reduce the circulating reactive power of the converter. Then, the conduction losses on the LVDC side, which are the major contribution in MEA application, are considerably reduced. The maximum magnetic flux density $(B_{\rm m})$ is comprised above 0.05 and below 0.15 T, being limited by the number of primary turns (n_1) , i.e. 20 for the Pareto-front designs, the switching frequency and the size of the magnetic core.

Moreover, primary-primary and secondary-secondary insulation distance $(h_{\text{ins1}}$ and h_{ins2}) are identical and lies in their minimum value. Therefore, the primary-secondary insulation distance (h_{ins12}) is the degree of freedom that allows obtaining different leakage values to find the minimum error regarding the decoupling inductance (ΔL) . Finally, the number of PCBs set in parallel in primary and secondary windings of the power transformer must be kept as low as possible, which can be incremented to obtain higher efficiencies at the expense of the power density.

The same analysis has been done for ABAC converter and depicted in Fig. 4.5, in which the design trade-offs of the output inductors that lead to the Pareto-front results are also included. In this case, the interpretation of the results is not as clear as in DAB converter due to the large design space that is swept for the study. In ABAC converter, the increment of the switching frequency also impact on the leakage-decoupling inductance error (ΔL), despite the fact that the maximum error is found at 100 kHz and the minimum at 50 and 150 kHz. This behavior is found since h_{ins1} and h_{ins2} in the

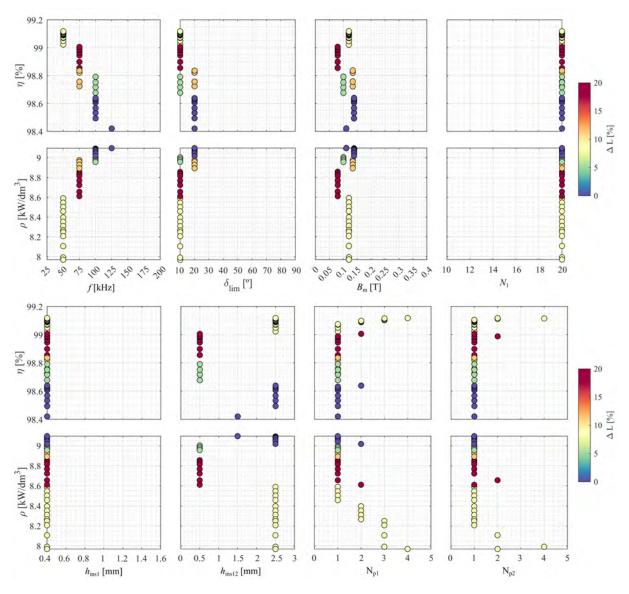


Figure 4.4 Values of the design space variables that fall on the Pareto-front in DAB converter.

Pareto-front designs are not constant, aiding the optimization algorithm to find solutions that fulfill the restrictions criteria. Furthermore, h_{ins12} is the main parameter to adjust the value of leakage inductance to meet the required L_{σ} , whose results are not shown since the conclusions extracted are similar to those in DAB. Also, the low δ_{lim} observed in both converters means that the optimal designs for MEA applications search to decrease the large circulating currents by minimizing the reactive power that flows through the converter.

Although the transformer turns-ratio is 5 in ABAC converter, the number of primary turns (n_1) is the same as in DAB to limit the maximum magnetic flux density in the core. However, $B_{\rm m}$ is slightly larger in the magnetic core of ABAC transformer, which means that it is possible to find smaller cores for the Pareto-optimal designs of this converter since the primary voltage and turns are the same in both converters (see (3.28)). Despite the

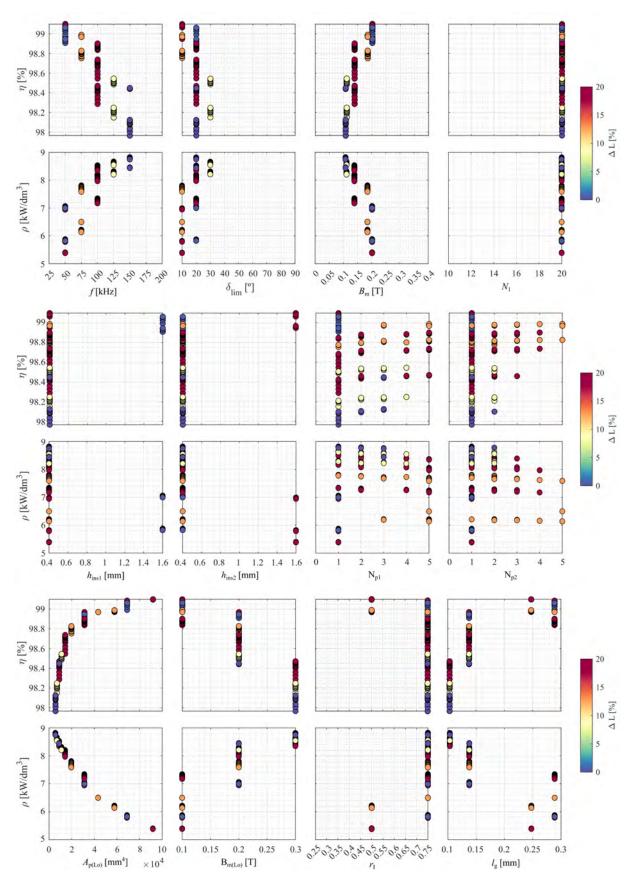


Figure 4.5 Values of the design space variables that fall on the Pareto-front in ABAC converter.

dispersion exposed in the plot, the number of PCB set in parallel in primary and secondary windings (N_{p1} and N_{p2}) follows the same trend as in DAB: higher efficiency and lower power density when increasing N_{p1} and/or N_{p2} . Finally, the variables that impact on the output inductors are analyzed, where it is noticeable that the lower volumes of these inductors are commonly found at high operating frequencies. However, the maximum magnetic flux density of these components as well as the current ripple ratio allowed also impact on the core size. Finally, the resulting gap length is presented, which exhibits higher efficiencies as larger is the gap due to its influence on the maximum magnetic flux density. The impact of this variable on the power density should not be noticed, it is observable that the larger gap lengths appear when the power density is lower, which is corresponded to the highest maximum magnetic flux densities to oust the core from saturation.

4.4 Analysis of Heatsink and Capacitor Technologies

Once the MOO tool has been developed, it allows the designer to evaluate different component technologies. Since the availability of components for PECs is high, this task gives the designer an idea of the technologies that provide an optimal trade-off between η and ρ . This study is frequently done to assess magnetic core materials for the power transformer [48] and/or inductors [160], as well as capacitors [161, 162] and heatsink technologies [165]. Due to the fact that this work considers the utilization of planar core geometries for the construction of the magnetic components, which are commonly utilized at medium and high operating frequencies with ferrite based materials, only capacitor and heatsink technologies are considered for this study.

Therefore, the optimization algorithm has been run for different CSPI air-cooled heatsink and capacitor technologies to deepen the impact of these components over the η - ρ Pareto-front. The databases utilized for the capacitor and heatsink analysis are presented in Table 4.2 and 4.3. In the case of capacitor technologies, Film, Aluminum-Electrolytic (Al-El) and MLCC are evaluated. Meanwhile the considered heatsink are selected regardless the thermal resistance, size and/or air flow, being chosen to satisfy the typical CSPI values found in air-forced cooled technology, i.e. from 1-30. It is important to note that the same heatsink is utilized when modifying the capacitor technology, as well as Film capacitors are selected for the study of the heatsink impact. The results depicted in Fig. 4.6(a) and 4.6(b) for DAB converter reveal that the impact of the capacitor technology on the resulting ρ is higher than the CSPI of the considered heatsink. Therefore, the maximum achievable power density is obtained when MLCC capacitors and the highest CSPI for the heatsink are contemplated.

Code	Type	Capacitance $[\mu F]$	Voltage [V]	Current [A]	ESR $[m\Omega]$	Volume [mm ³]	Weight [g]
B32674D3225	Film	2.2	300	5	18.1	6583.5	9.5
B32674D3335	Film	3.3	300	7	12.2	8465.6	13
B32674D3475	Film	4.7	300	8.5	8.9	10804	16
B32674D3505	Film	5	300	9	8.4	11576	16
B32674D3685	Film	6.8	300	11.5	6.3	15592	20
B32674D3805	Film	8	300	12.5	5.6	16128	30.5
B32674D3825	Film	8.2	300	13	5.5	18711	24.5
B32674D3106	Film	10	300	14.5	4.6	20506	26.3
B32674D3126	Film	12	300	17	4	25294	33
B32524R0226	Film	22	63	9	12	7276.5	10
B32524R0686	Film	68	63	12	4.5	15592	20
B32524R0107	Film	100	63	20	3	25294	33
B40600A5128M003	Al-El	1200	25	7.4	5.1	3848.5	5.9
B40600A5168M003	Al-El	1600	25	8.5	4.4	4618.1	7.1
B40600A5178M003	Al-El	1700	25	9.2	4	5026.5	7.5
B40600A5228M003	Al-El	2200	25	10.5	3.5	6031.9	8.9
B40600A5128M003	Al-El	780	35	7.4	5.1	3848.5	5.9
B40600A5168M003	Al-El	1000	35	8.5	4.4	4618.1	7.1
B40600A5178M003	Al-El	1000	35	9.2	4	5026.5	7.5
B40600A5228M003	Al-El	1400	35	10.5	3.5	6031.9	8.9
CGA6L2X7R1H105K160AA	MLCC	1	50	4	7.7	20	1
CGA6M2X7R1H155K200AA	MLCC	1.5	50	4	6.3	20	1
CGA6M3X7R1H225K200AB	MLCC	2.2	50	5	6	20	1
CGA6P3X7R1H335K250AB	MLCC	3.3	50	4	3.8	20	1
CGA6P3X7R1H475K250AB	MLCC	4.7	50	4	2.8	20	1
CGA6P3X7S1H685K250AB	MLCC	6.8	50	4	1.9	20	1
CGA6P3X7S1H106K250AB	MLCC	10	50	4	2.2	20	1

Table 4.2 Database of the EPCOS capacitors utilized in the	he MOO precedure developed in this work
Table 4.2 Database of the Er COS capacitors utilized in th	ine MOO procedure developed in this work.

Table 4.3 Database of the heatsinks utilized in the MOO procedure developed in this work.

Code	Manufacturer	${\rm CSPI}~[{\rm W}/({\rm K}{\cdot}{\rm dm}^3)]$	$R_{\rm th,ha}$ [W/K]	Volume [mm ³]	Weight [g]	Air flow [m/s]
OMNI-UNI-34-75	Wakefield-Vette	5.22	1	191250	156	1
LA 6 100 24	Fischer Elektronik	10.86	0.2	458800	NaN	3.39
FFM50	Alpha Novatech	26	1.33	28750	26.6	1.57

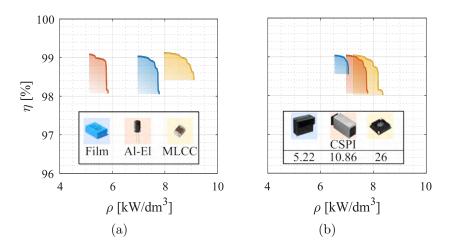


Figure 4.6 η - ρ Pareto optimization of DAB converter considering different (a) capacitor technologies and (b) heatsink CSPI.

Furthermore, there are some interesting conclusions that can be extracted by analyzing the parameters included in the databases (Table 4.2 and 4.3) together with Fig. 4.6. First, the capacitance of the corresponding capacitor is not the most important parameter in the sizing of this component, since the highest capacitance is found in Aluminum-Electrolytic capacitors that are found in the lowest power density designs. This is due to the fact that the limiting factor is the RMS current that flows through the capacitor in the LVDC side, and thus the number of capacitors paralleled must handle the imposed current level. Then, the capacitance must reach the required value to satisfy the voltage ripple requirements, which is got in most cases in the first step (see Appendix A.4). In the case of aircooled heatsink, it is also important to point that although a lower heatsink-ambient thermal resistance $(R_{\rm th,ha})$ is beneficial to the chain that goes from the junction of the corresponding power device to the ambient, this parameter does not aid to obtain the maximum achievable power density in the converter. This is due to the fact that the CSPI relates this parameter with the volume of this component, which plays the most important role. Therefore, the maximum power density is extracted with the heatsink that achieves the higher CSPI despite the fact that is the one with the larger $R_{\rm th,ha}$ since its volume is the lowest of the detailed heatsinks. To deepen on the impact of this components, as well as to compare the power converter topologies presented in this work, a comparative study between ABAC and DAB is performed in the following section.

4.5 Comparative Study: ABAC vs DAB

After the analysis of the capacitor technologies and CSPI, this section presents a comparative study between ABAC and DAB converters in a MEA scenario. This comparison is realized based on the MOO developed in this chapter, selecting in both cases a power converter design that achieves the maximum power density with the different technologies. First, the efficiency and power density of these designs are presented in Table 4.4 together with the heatsink and capacitor technology. In this study, the same heatsink is

No.	Converter	Heatsink	Capacitor Tech.	$ ho \; [{ m kW/dm^3}]$	η [%]
1	DAB	FFM50	Al-El	6.15	98.03
2	DAB	FFM50	Film	8.35	98.02
3	DAB	FFM50	MLCC	9.9	98.35
4	DAB	OMNI-UNI-34-75	MLCC	8.1	98.6
5	DAB	LA 6 100 24	MLCC	9.09	98.42
1	ABAC	FFM50	Al-El	5.38	97.46
2	ABAC	FFM50	Film	7.63	97.48
3	ABAC	FFM50	MLCC	9.51	97.59
4	ABAC	OMNI-UNI-34-75	MLCC	7.88	97.96
5	ABAC	LA 6 100 24	MLCC	8.81	97.96

Table 4.4 Selected designs for detailed comparison of DAB and ABAC converters.

utilized to compare the considered capacitor technologies. Furthermore, the same capacitor technology is set to analyze the impact of the employed heatsink. The volume and losses of these designs are presented in Fig. 4.7 and 4.8. It must be noted that the volume added by the power devices is neglected in this study, as well as the $C_{\rm LV}$ capacitor in case of ABAC converter. In Fig. 4.7 the pie charts that correspond to ABAC designs are depicted. In this case, it is noticeable the importance that acquires the capacitor volume when utilizing Al-El technology (①), since it represents the 57.6% of the total volume. On the other hand, the implementation of film capacitor (②) reveals volume savings in $C_{\rm HV}$ capacitor. Furthermore, it is noticeable the amount of volume earned when considering film capacitor instead of Al-El to obtain similar efficiencies. Finally, the volume of the capacitors included in this converter is almost negligible when considering MLCC technology. If we consider different heatsink CSPI (from ③-⑤), the larger values lead lower volumes on the final system, even if there are less contribution to the power losses added by the switching devices.

In DAB converter (see Fig. 4.8), it is evident how the correct selection of the capacitor technology also aid to reduce the volume of the HVDC and LVDC bus capacitors (from (1)-(3)). This fact is of special interest to reduce the impact of the $C_{\rm LV}$ on the converter volume and/or weight. In this case, the contribution to the power losses of the switching devices is larger than in ABAC converter, and thus the influence of the heatsink CSPI is almost negligible at low values. However, at greater CSPI values, its contribution is reduced in pursuit of the transformer and capacitor volumes. By comparing the results obtained for both converters with the same technologies, it is shown that the volumes are pretty similar in both converters regardless the employed technologies. Nevertheless, there is a reduction close to 5 W in each design in the case of DAB converter, which is mostly caused by the losses added by the output inductor in ABAC converter. Due to this losses difference, both efficiency and the resulting power density are higher in DAB, even though the volumes are slightly larger in this converter. Therefore, the utilization of ABAC is strictly comprised to an scenario in which the voltage ripple on the LVDC bus must be almost negligible due to the load demands, being DAB converter the best choice to optimize the power density to efficiency trade-off. In this terms, although DAB achieves better efficiencies, the resulting volumes are in most cases lower in ABAC converter due to the large LVDC capacitor included in DAB. Thus, a good trade-off to evaluate the power converter topology that fits best with the application requirements is to analyze the impact of the volume and/or weight into the aircraft energy consumption.

Therefore, it has been depicted that ABAC converter achieves slightly higher volumes in almost all the considered technologies, which occurs due to the large LVDC capacitance of DAB converter. Nevertheless, the efficiency achieved in DAB is close to a 0.5 % higher, which results on larger power density levels. This is caused by the fact that four power devices have been considered to develop the LVDC stage, being almost negligible the losses difference depicted in Chapter 2. Then, the importance of the losses added by the output inductors is huge.

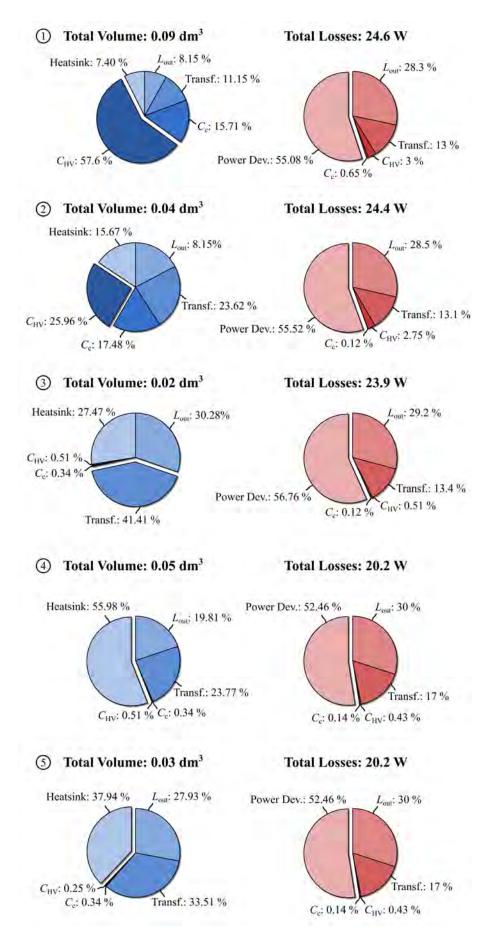


Figure 4.7 Volume and losses pie charts of the selected ABAC converter designs.

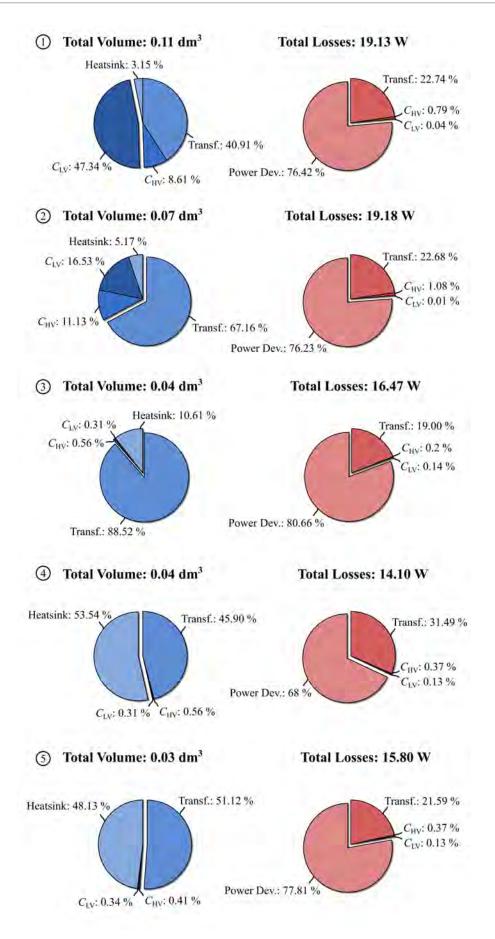


Figure 4.8 Volume and losses pie charts of the selected DAB converter designs.

4.6 Conclusions

During this chapter, a MOO methodology have been developed for the most promising topologies found in MEA applications. To this aim, the design space variables that are found in these converters are detailed and established based on the theoretical behavior of the converters, as well as the typical commercial values found in some components, e.g. copper thickness in PCB windings.

Afterwards, the implementation of the MOO procedure is done, resulting in the η - ρ Pareto charts that are presented in this chapter. These representations reveal that the maximum achieved power density is got with DAB converter, although the difference between both converters is low. Nevertheless, the efficiency obtained in DAB is larger than in ABAC when considering high-power density designs. Furthermore, the values of the design space variables that lead to the Pareto-front of this optimal design have been discussed in detail.

Finally, an analysis of the heatsink and capacitor technologies that enable to improve the resulting power density of the PECs under study have been done, where the impact of the selected capacitors shows to be a greater than the utilized heatsink. Then, the volume and losses of ABAC and DAB converters are compared to get a deep insight of the contribution of each component to these variables, which determine the power density and efficiency of these converters respectively.

5

Conclusions and Future Work

Summary:

In this chapter, the conclusions and future work of this thesis are gathered.

5.1 Summary and Conclusions

A MOO procedure for the most promising bidirectional isolated DC/DC PECs found in MEA applications have been developed in this thesis.

To this aim, first the diversity of EPDS proposed in literature for the DC/DC distribution inside the electric aircraft, along with the upcoming challenges to face in the increasing electrification of this mean of transport. Furthermore, the standards that are established for this application are given, being the peak-to-peak voltage ripple in the LVDC side the most restrictive in this application. The state of the art of bidirectional isolated DC/DC PECs in MEA and electric mobility applications has been also detailed. Among the most studied converters, DAB is the preferred option when bidirectionality and isolation is required. However, ABAC converter is proposed in the literature to reduce the large LVDC capacitance required in DAB converter to fulfill the standards. However, there are some gaps in the literature related with the optimization of the power converters for MEA applications. The volume and/or weight of these systems is of special interest due to the impact that they have on the aircraft, being closely related to the fuel consumption in actual aircraft. Moreover, the efficiency of the resulting converter is a parameter that must be always taken into account regardless the application proposal. Therefore, the MOO methodology proposed in this work searches for relate this two parameters, finding the best trade-off between them.

In this context, the analytical modeling of these converters gains significant weight to reduce the computational effort that is required when simulation tools as FEA are utilized. In the case of artificial intelligence, the utilization of neural networks and genetic algorithms are typically faster than analytical model based optimization. Nevertheless, these methods must be trained with experimental data as in the case of artificial neural networks, although a mixture of analytical, simulation and experimental data are commonly utilized to reduce the data acquisition time. Therefore, the analytical models that describe the behavior of these converters have been developed considering the main modulation methods. Among the presented models, the RMS and AVG models obtained in the Chapter 2 are utilized to characterize the conduction losses on the power devices. Furthermore, the models to determine the current stress and peak-to-peak voltage ripple on the input and output capacitors of DAB are gathered in Appendix A, which are useful to size the corresponding capacitors required in the HVDC and LVDC buses. To complete the analytical modeling presented in this work, the equations that describe the behavior of the magnetic components found in DAB and ABAC are detailed in Chapter 3.

Finally, these models are utilized to develop a brute force based MOO optimization procedure that is presented in Chapter 4. This MOO has been run considering different

technologies of capacitors and heatsink, enabling the evaluation of the impact that the different component technologies have on the converter performance. As a result of this evaluation, MLCC capacitors have shown the greatest impact on the converter power density. Also, the analysis of the heatsink CSPI reveals that there is a narrow difference between the obtained power densities. The interest of these result relies on the fact that other design axis as the cost per kilowatt must be considered to select the required heatsink. It is noticeable that the efficiency variation considering the utilization of any of the capacitor technologies and/or heatsink CSPI is almost negligible. This is caused by the fact that the main influence on the efficiency of these converters comes from the conduction losses of the power devices placed in the LVDC side. To improve the efficiency obtained, four power devices are paralleled in this side to reduce the current that flows through them, minimizing the conduction losses. Furthermore, an analysis of the contribution to the volume and losses of each component placed inside ABAC and DAB converters have been detailed. The presented study details that the volume and/or weight of the LVDC capacitor is minimizing by utilizing the most adequate technology, i.e. MLCC capacitors. Also, the contribution of the heatsink to the final volume is noticeable, although its impact is not as larger as in capacitor case. In terms of power losses, the major contribution comes from the power devices, which establish the resulting volume of the required heatsink.

5.2 Contributions

Hereinafter, the main contributions that are result of the work developed in this thesis are listed below:

• Analytical modeling of the RMS and AVG currents that flow through the switching devices and power transformer in DAB and ABAC converters.

As stated during this work, the main contribution to the power losses in bidirectional isolated DC/DC converters proposed for MEA applications comes from the conduction of the LVDC power devices. In order to accurately determine the conduction losses analytically, the equations that describe the RMS and AVG current stress are given in this work. These equations and the designer to accurately size the required heatsink to avoid junction temperatures larger than the specified in the datasheet of the corresponding device. Furthermore, these models are useful to reduce the computational time that is taken in the MOO optimization process, since it avoid the utilization of simulation models to determine the value of the RMS and AVG currents. The presented models describe the behavior in the main modulation methods of DAB converter, which are SPS rectangular modulation, TPS-TPM and TPS-TRM. This analytical models have been validated based on a simulation model developed in PLECS.

• Analytical modeling to evaluate the utilization of interleaved parallel IPOP DAB converter.

In order to reduce the large LVDC capacitance required in DAB converter when it is considered for MEA applications, the time domain equations that describe the behavior of these configurations have been derived from those proposed in literature for typical DAB structure. The analytical models that describe the behavior of these structures have been validated with PLECS, and its utilization is useful to determine the electrical characteristics of the whole system regardless the number of DAB connected in parallel. Although this structures are useful to reduce the volume of the LVDC capacitor, there is a trade-off between the volume earned in this component and the size increment of the power transformer stage.

• Analytical modeling to determine the RMS current and peak-to-peak voltage ripple in HVDC and LVDC capacitors of DAB converter.

Since the most critical component in DAB converter is the capacitor of the LVDC side, the analytical models to determine the RMS currents and peak-to-peak voltage ripple in HVDC and LVDC capacitors have been obtained in this work. To obtain the corresponding equations, the main modulation methods of DAB converter are considered. The validation is also based on a simulation model developed in PLECS. These models are useful in the design stage, as well as in the optimization procedure presented in this work to reduce impact of this components on the final system.

• MOO methodology and tool for the optimization of DAB and ABAC converters considering MEA applications.

The analytical models derived in this work are implemented afterwards on the MOO procedure proposed in this thesis. The MOO developed is based on a brute force algorithm that sweeps the design space of the converters under study. The aim of this MOO is to obtain a roadmap of η - ρ trade-off in these PECs, as well as to determine the contribution of the different components on the power losses and total volume. This study remarks the benefits and drawbacks of utilizing DAB and ABAC converters in MEA scenarios.

• Evaluation of different capacitor technologies and heatsink CSPI to determine the impact of this components on the optimization procedure.

Finally, the MOO procedure developed is utilized to compare the different capacitor technologies that are commonly utilized in PECs. Furthermore, the impact of the heatsink CSPI when air cooled technologies are considered is analyzed. First, MLCC

capacitors have shown to be the best technology to improve the achievable power density of the converter. However, this is not the case of the heatsink CSPI, which exhibit a minimum impact on the power density when varying the heatsink CSPI from typical low values to highest of air cooled heatsinks.

5.3 Future Work

Along this thesis, the analytical models that describe the behavior of the most promising PECs in bidirectional isolated DC/DC MEA applications have been obtained. These models have been applied afterwards in the brute force based MOO procedure developed in this work. As a result of this work, the following lines of research still being open:

• Development of a configurable power converter that can operate as an ABAC and/or DAB.

The validation of the analytical equations performed in this work has been done based on simulation models developed in PLECS. Furthermore, an experimental set-up has been utilized to validate DAB analytical models when working with the main modulation methods. However, the specifications are slightly different from those used in MEA applications. In order to discuss the non-idealities that arise from the implementation of ABAC and DAB converters under MEA specifications, a configurable power converter must be constructed. This fact will aid to validate and compare both converters in the same test-bench and case studies. Some of these non idealities are voltage and/or current unbalance in clamp capacitors and output inductors respectively in the case of ABAC converter. Furthermore, the impact of the parasitic capacitance of the power transformer must be analyzed in detail in both converters. Finally, the influence of the passive elements on the resulting RMS and AVG currents that flow through the power devices also must be studied.

• Increase the components database in capacitors and heatsinks.

The components database utilized in this work is composed by a short number of capacitors and/or heatsinks to analyze the impact that different component technologies have in the power density and efficiency of the power converter. However, this database must be increased to find the best components that fit with the presented power converters. Furthermore, GaN power devices can be considered for the LVDC side since the electrical characteristics of this technology perfectly match with requirements of the application. Therefore, to increment the number of components considered will feed the opportunity to find the best solution for MEA.

• Utilization of artificial intelligence for the MOO procedure.

In last year, the utilization of artificial intelligence optimization methods based on artificial neural networks and genetic algorithms is increasing in popularity due fast and accurate results obtained. However, the main drawback of this methods are the time consumption in training the artificial neural networks as well as the deep knowledge required in case of genetic algorithms. These optimization methodologies are becoming more important in the industrial sector. Nowadays, it is possible to find many companies that base their business in the employment of artificial intelligence for the optimization of magnetic components and power converters. Therefore, their utilization is of special interest when considering the optimization of PECs in bidirectional isolated DC/DC applications for MEA.

• Cost evaluation of the presented solutions.

Although the PECs studied in this work have been optimized to achieve a good efficiency to power density trade-off, there are other variables that must be analyzed in detail. This is the case of the cost per kilowatt that is achieved in each power converter. Since the number of components is larger in ABAC, it is expected that the cost per kilowatt in this converter is larger than in DAB. This parameter is one of the most important when considering the industrialization of these converters, and therefore it must be analyzed in depth.

• Reliability evaluation of the PECs studied in this work.

Finally, it is also important to evaluate the reliability of the systems that are implemented in MEA applications. In this context, reliability oriented design of PECs is studied in detail in [166], which can be applied to any application proposal.

APPENDICES



Component Models

In this appendix, the component models utilized for the MOO procedure developed in this thesis are presented. These component models are based on analytical equations obtained from the datasheet of the different components, as well as from simulation models developed in LTSpice. Hereinafter, the model of the different components are described in detail.

A.1 Power Semiconductors

In the datasheet of power devices, the conduction characteristics of this components are presented in almost all cases. Nevertheless, this is not the case of the turn-on and turn-off switching energies curves, which are not commonly given specially in the case of discrete semiconductors. To solve this issue, a double pulse test is developed in LTSpice (see Fig. A.1) to obtain the switching energies at different blocking voltages and switching currents of the power devices presented in Chapter 2. Then, these energies are curvefitted with (A.1):

$$E_{\rm on|off} = (a + bI_{\rm sw} + cI_{\rm sw}^{2}) (V_{\rm DS}^{\rm d}) , \qquad (A.1)$$

where a, b, c and d are the constant parameters obtained from the curve fitting, $E_{\rm on|off}$ are the corresponding switching energies and $V_{\rm DS}$ is the applied voltage on the DC bus. The waveforms obtained from the double pulse test are presented in Fig. A.2 together with the results of the curve fitting for the turn-off switching energy of a HVDC side power device. In the case of Fig. A.2(b), the red points represent the data obtained from simulation, while the surface is got after obtaining the corresponding a, b, c and d constants. These parameters are given in Table A.1 for the power devices considered in this thesis. It is important to note that, in the case of the switching devices selected for the LVDC side, these parameters are obtained considering that no power devices are paralleled. Therefore, the presented parameters must be for different number of power devices connected in parallel in order to get the impact of the output capacitance.

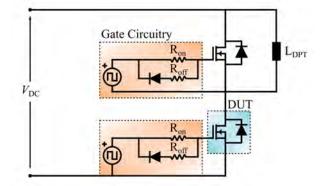


Figure A.1 Schematic of the double pulse test implemented in LTSpice.

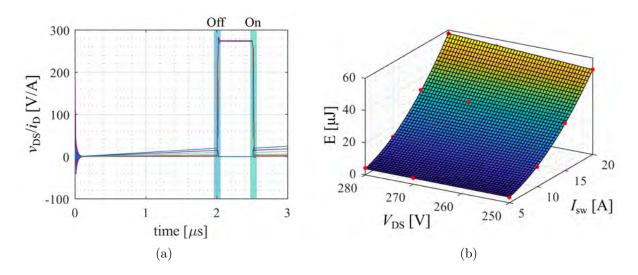


Figure A.2 Double pulse test realized in a HVDC device: (a) Drain current and drain-to-source voltage and (b) curve fitting of the turn-off energies.

Table A.1 Parameters to determine analytically	the switching	energies in	the power	devices	considered
in this work.					

	Parameter $[E_{\rm on}/E_{\rm off}]$						
HVDC Dev.	a	b	с	d			
1	0.0004232/0.07454	0.2396/-0.01169	0.09041/0.001315	0.1118/0.7809			
2	0.0234/0.1465	0.001325/-0.01718	8.908e-05/0.00102	1.263/0.8002			
3	0.04676/0.001162	0.001994/0.003855	-1.418e-06/0.0004739	1.388/0.897			
4	0.02689/0.01805	0.003247/-0.00391	6.971 e- 07/0.001577	1.332/0.8198			
5	-	-	-	-			
LVDC Dev.	a	b	с	d			
1	0.03629/2.383e-13	0.0001815/0.00914	1.951e-05/0.001314	1.897/0.6226			
2	0.1685/2.562e-14	0.001166/0.03852	1.359e-05/0.003406	1.654/0.3295			
3	0.04592/0.02145	0.002915/-0.0123	9.049e-05/0.002932	1.428/0.4317			
4	0.009575/7.688e-05	0.002354/0.007209	4.494e-05/0.01016	1.72/0.0455			
5	0.02067/2.337e-14	-0.0005179/0.04818	2.134e-05/0.004866	1.894/0.2098			

A.2 Heatsink

In most power converter designs, the heatsink is one of the components that takes a huge importance due to the volume and/or weight that add to the system. The heatsinks that are selected for the MOO of this thesis are depicted in the technology analysis detailed in Chapter 4. Once the CSPI of each heatsink is selected, the required volume is obtained from (A.2):

$$CSPI = \frac{1}{R_{\rm th,ha} \, \rm Vol_{\rm HS}} \quad , \tag{A.2}$$

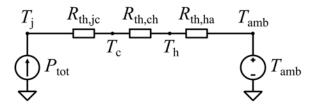


Figure A.3 Steady state thermal model utilized to determine the junction and case temperatures in the power devices.

where $R_{\rm th,ha}$ is the required heatsink thermal resistance, and Vol_{HS} the resulting volume to reach it. To determine $R_{\rm th,ha}$, a simplified thermal resistances model is presented in Fig. A.3. Then, the required $R_{\rm th,ha}$ for the heatsink is computed according (A.3):

$$R_{\rm th,ha} = \frac{\Delta T}{P_{\rm tot}} \quad , \tag{A.3}$$

where ΔT is the thermal jump from ambient to the case of the power device and P_{tot} are the total losses produced in the power devices. Utilizing these basic equations, the calculation of the fictive heatsink volume that must be utilized is done.

A.3 Magnetic Components

In order to determine the volume of the required transformer, a database of EPCOS planar core transformers is developed [167]. This database is presented in Table A.2 considering EE and EI planar cores. As stated along Chapter 2, the power transformer core is selected based on the required area product for the application. The relationship between the area product and the volume is presented in Fig. A.4 for the EE cores detailed in Table A.2.

These data are fitted with (A.4) that relates the mentioned parameters as proposed

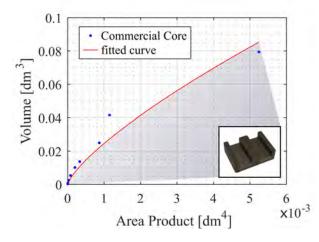


Figure A.4 Curve fitting of volume to area product relationship considering EE planar magnetic cores.

Piece 1	Piece 2	$\begin{array}{c} {\bf Core \ Factor} \\ [{\bf mm}^{-1}] \end{array}$	Eff. length [mm]	Eff. Area [mm ²]	$\begin{array}{c} {\bf Min.} \ {\bf Area} \\ [{\bf mm}^2] \end{array}$	Eff. Volume [mm ³]	$\begin{array}{c} {\bf Window \ Area} \\ [{\bf mm}^2] \end{array}$	$\begin{array}{c} {\bf Area\ product} \\ [{\bf mm}^4] \end{array}$
ELP14/3.5/5	I 14/1.5/5	1.15	16.7	14.5	13.9	242	8	116
ELP14/3.5/5	ELP14/3.5/5	1.45	20.7	14.3	13.9	296	16	228.8
ELP18/4/10	I 18/2/10	0.51	20.3	39.5	38.9	802	10	395
ELP18/4/10	ELP18/4/10	0.62	24.3	39.3	38.9	955	20	786
ELP22/6/16	I 22/2.5/16	0.33	26.1	78.5	77.9	2050	18.88	1482.08
ELP22/6/16	ELP22/6/16	0.41	32.5	78.3	77.9	2540	37.76	2956.608
ELP32/6/20	I 32/3/20	0.27	35.1	130	128	4560	30.48	3962.4
ELP32/6/20	ELP32/6/20	0.32	41.4	130	128	5390	60.96	7924.8
ELP38/8/25	I 38/4/25	0.22	43.6	194	192	8440	51.62	10014.28
ELP38/8/25	ELP38/8/25	0.27	52.4	194	192	10200	103.24	20028.56
ELP43/10/28	I 43/4/28	0.225	50.8	225	217	11430	73.71	16584.75
ELP43/10/28	ELP43/10/28	0.274	61.6	225	217	13748	147.42	33169.5
ELP58/11/38	I 58/4/38	0.22	67.7	310	308	21000	139.75	43322.5
ELP58/11/38	ELP58/11/38	0.26	80.7	310	308	25000	279.5	86645
ELP64/10/50	I 64/5/50	0.13	69.7	519	518	36200	110.67	57437.73
ELP64/10/50	ELP64/10/50	0.15	79.9	519	518	41500	221.34	114875.46
ELP102/20/38	I 102/7/38	0.227	121.2	534.2	524.5	67745	478.8	255774.96
ELP102/20/38	$\mathrm{ELP102}/20/38$	0.274	147.6	538	524.5	79410	975.6	524872.8

Table A.2 Database of the planar magnetic cores utilized in this work.

in [41]:

$$Vol_{\rm tr/ind} = k_{\rm L} A_{\rm p}$$
 (A.4)

where $Vol_{\text{tr/ind}}$ is the volume of the resulting magnetic devices (transformer and/or inductor) and k_{L} is the geometric constant of the core.

A.4 Capacitors

To size the capacitor bank required for the HVDC and LVDC bus capacitors, the selection and design criteria presented in [80] is utilized. This capacitor bank is determined by selecting the number of components that are required to perform the series $(N_{\rm sc})$ and parallel $(N_{\rm pc})$ connections (see Fig. A.5). To determine these variables, the DC bus voltages and RMS currents are utilized according (A.5) and (A.6):

$$N_{\rm sc} = \frac{V_{\rm DC}}{V_{\rm cap}} \quad , \tag{A.5}$$

$$N_{\rm pc} = \frac{I_{\rm RMS}}{I_{\rm cap}} \quad , \tag{A.6}$$

where V_{cap} and I_{cap} are the maximum voltage and RMS current that can be handled by the corresponding capacitor. Finally, if the required capacitance is not fulfilled, the number of parallel branches is incremented up to meet the minimum capacitance condition.

Once the capacitor bank has been sized, the resulting equivalent series resistance

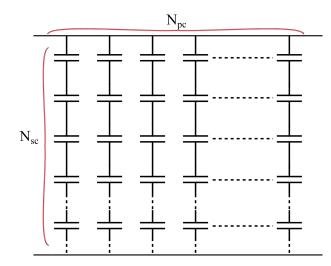


Figure A.5 Capacitor matrix showing the number of series and parallel capacitors that must be computed to size this component.

(ESR) and capacitance are calculated with (A.7) and (A.8):

$$ESR_{\rm eq} = \frac{ESR\,N_{\rm sc}}{N_{\rm pc}} \quad , \tag{A.7}$$

$$C_{\rm eq} = \frac{C N_{\rm pc}}{N_{\rm sc}} \quad . \tag{A.8}$$

Then, these equations follow the basic relationship done in the association of series and parallel resistances and capacitances to determine the equivalent component values.

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