Novel Analytical Method for Estimating the Junction-to-Top Thermal Resistance of Power MOSFETs

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Keywords

≪Thermal model≫,≪Device modelling≫, ≪Packaging≫, ≪Power semiconductor device≫, ≪Double-side cooling (DSC)≫.

Abstract

This papers proposes a new methodology for estimating the thermal resistance from the junction-to-top capsule surface. By placing the transistor in a vertical position, without being soldered to any PCB, and sensing the dissipated power and the temperatures of the device, it is possible to characterize the internal thermal resistance.

1 Introduction

Modern power semiconductors such as Wide bandgap (WBG) devices are well known by their system benefits such as smaller die size, lower $R_{DS(ON)}$ or good switching behaviour [1]. However, these benefits bring to new design challenges that must me solved. Some of them are a more complex loss characterization, critical gate drive design or higher thermal resistance which brings the need to new thermal design approaches.

Classically, the only heat propagation path considered by semiconductor manufacturers is the one from the junction to the bottom capsule of the device [2]. This is because the path from the junction to the top capsule is made of epoxy, which has a low thermal conductivity [3]. However, this new thermal design challenge has led power electronics designers to take the most out of their transistors packages by placing heatsinks at the top side [4]. To correctly assess the thermal behaviour of the transistor, a proper method for measuring the thermal resistance from the junction-to-top capsule (R_{JC_T}) is needed.

A few modern devices now include this parameter into their datasheets as in [5]. However, the methodology to determine this thermal resistance is still not clear and under discussion [6, 7]. In fact, the JEDEC standard describes the proper procedure for measuring the thermal resistance from the junction to-bottom capsule (R_{JC}) and the thermal resistance from the junction-to-ambient (R_{JA}) in [8], but not for the (R_{JC_T}). An example of the different parts of a SMD power transistor is illustrated in Fig. 1.

Commonly the thermal data provided on MOSFET datasheets is very limited. Transistors manufacturers provide typical and sometimes maximum values of R_{JC} and R_{JA}, assuming for its determination a model with a single path of heat propagation, as shown in Fig. 2 but do not report R_{JC_T} values.

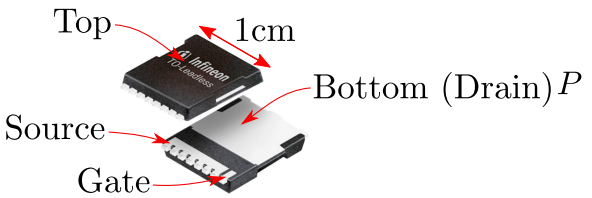


Fig. 1: Parts and dimensions of a SMD power transistor.

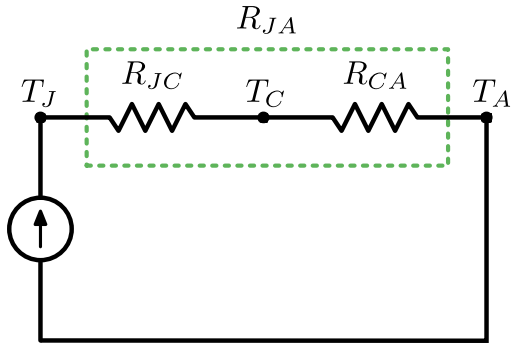


Fig. 2: Compact thermal model considering a single path of heat transfer to the environment.

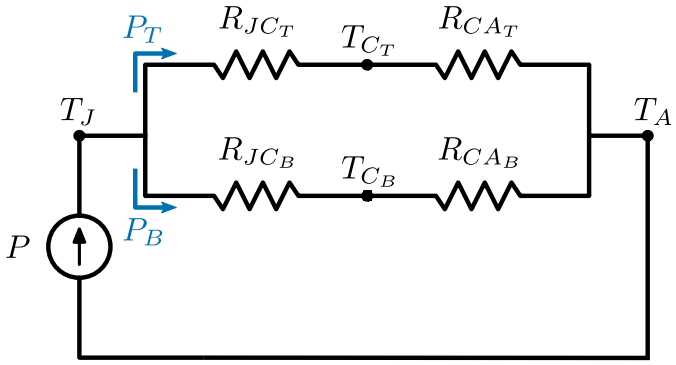


Fig. 3: Compact thermal model considering two paths of heat transfer to the environment.

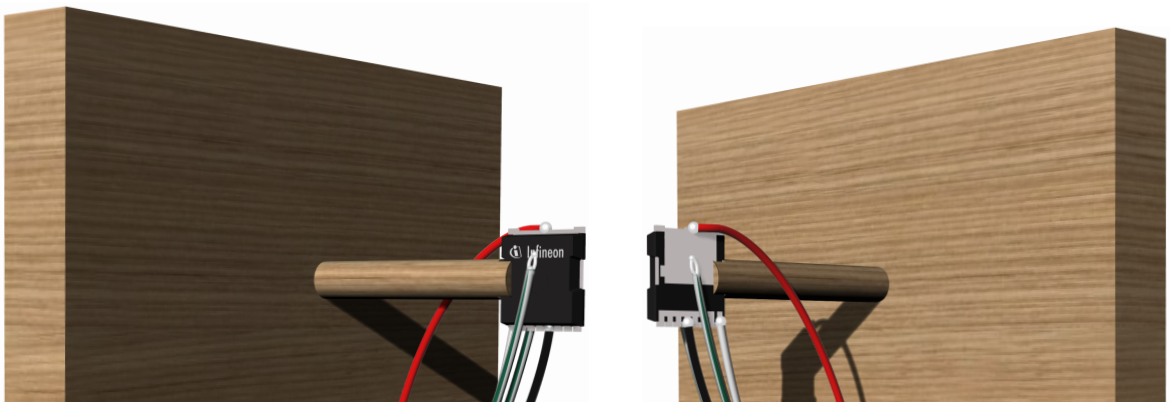
In order to mitigate the above problem, a calculation procedure is proposed. It is based on a propagation compact model of heat considering two heat propagation paths as in Fig. 3.

R_{JC_T}, R_{JC_B}, R_{JA_T} and R_{CA_B} are respectively the thermal resistances between the junction and the top capsule surface, the thermal resistance between the junction and the bottom capsule surface, the thermal resistance between the top capsule surface and the environment and the thermal resistance between the bottom capsule surface and the environment. On the other hand, T_J and T_A are respectively the junction temperature and the ambient temperature. Finally, P, P_T and P_B specify respectively the total power dissipated by the device, the fraction of power circulating through the top path and the fraction of power circulating through the bottom path.

2 Methodology

With the transistor located inside a natural convection still air chamber, in an upright position and without being soldered to any PCB as in Fig. 4, it is reasonable to assume a compact thermal model in which the heat generated in the junction is transmitted to the outside following two paths. One from the junction to the bottom capsule surface and another path from the junction to the top capsule surface. Moreover, in a thermal steady state and in the absence of external excitation, it is appropriate to assume that the temperature of the top and bottom surfaces are equal to the temperature of the junction, being in turn equal to the ambient temperature. Under the above assumptions, the thermal behavior of the transistor can be modeled in a first approximation as an ideal lineal system, analogous to the electrical circuit shown in Fig. 3.

For a proper and repeatable temperature measurement, different sensors can be used taking into account their limitations. If a thermocouple is chosen, as shown in Fig. 4, the position in which it is placed on the package surface, as well as the adhesive used to fix it on this, can be critical for a good measurement as described in [9] and [10]. On the other hand, if an infrared camera is chosen, the emisivity factor and the focal distance must be taken into account. Due to the low emissivity coefficient of the bottom



(a) Frontal view (b) Rear view

Fig. 4: 3D Model of the transistor to air test-bench.

metal capsule, the reflected temperature has a strong influence on the temperature measurement, thus it would be beneficial to increase its emisivity factor. Electrical tape or specific paints that withstand high temperatures can be applied for increasing this parameter.

From the analysis of Fig. 3, it is deduced that the temperature difference between the junction and both package surfaces is equal to

$$T_J - T_{C_T} = P_T \cdot R_{JC_T} = (1-D) \cdot P \cdot R_{JC_T} \tag{1}$$

and

$$T_J - T_{C_B} = P_B \cdot R_{JC_B} = D \cdot P \cdot R_{JC_B} \tag{2}$$

where D is the fraction of total power, P, flowing through the bottom path of the circuit shown in Fig. 3. Subtracting the above expressions, it is possible to find the relationship between both surfaces

$$T_{C_B} - T_{C_T} = [R_{JC_T} - D\,(R_{JC_T} + R_{JC_B})] \cdot P \tag{3}$$

which yields to

$$P_B = D \cdot P = \frac{R_{JC_T} + R_{CA_T}}{R_{JC_T} + R_{CA_T} + R_{JC_B} + R_{CA_B}} \cdot P. \tag{4}$$

Therefore,

$$D = \frac{R_{JC_T} + R_{CA_T}}{R_{JC_T} + R_{CA_T} + R_{JC_B} + R_{CA_B}} = \frac{R_{JA_T}}{R_{JA_T} + R_{JA_B}} \tag{5}$$

and the power flowing through the top path is

$$P_T = (1-D) \cdot P = \frac{R_{JC_B} + R_{CA_B}}{R_{JC_T} + R_{CA_T} + R_{JC_B} + R_{CA_B}} \cdot P. \tag{6}$$

In consequence, the fraction $1-D$ is equal to

$$1 - D = \frac{R_{JC_B} + R_{CA_B}}{R_{JC_T} + R_{CA_T} + R_{JC_B} + R_{CA_B}} = \frac{R_{JA_B}}{R_{JA_T} + R_{JA_B}}. \tag{7}$$

Same way

$$T_{C_B} - T_A = P_B \cdot R_{CA_B} = D \cdot P \cdot R_{CA_B} \tag{8}$$

and

$$T_{C_T} - T_A = P_T \cdot R_{CA_T} = (1 - D) \cdot P \cdot R_{CA_T} \tag{9}$$

If Eq. 8 and Eq. 9 get combined, the relationship between power and temperature difference between top and bottom surfaces is expressed as

$$T_{C_B} - T_{C_T} = P \cdot \frac{R_{JC_T} R_{CA_B} - R_{JC_B} R_{CA_T}}{R_{JA_T} + R_{JA_B}} = P \cdot R_{EQ} \tag{10}$$

where

$$R_{EQ} = \frac{R_{JC_T} R_{CA_B} - R_{JC_B} R_{CA_T}}{R_{JA_T} + R_{JA_B}} \tag{11}$$

On the other hand, the heat transfer in natural convection is described by the Newton's Law of Cooling

$$\dot{Q} = hA(T - T_f)^b \tag{12}$$

where $\dot{Q}$ is the heat transferred per unit time, A is the area of the object, h is the heat transfer coefficient, T is the object's surface temperature, T_f is the fluid temperature, and b is a scaling exponent. The convective coefficient h depends on the absolute temperature, the material property of the fluid, the flow rate of the fluid, the dimensions of the considered surface, the orientation of the considered surface, and the surface texture.

In this case, the influence of the surface texture is quasi-negligible [11]. Therefore, since the area of both surfaces is approximately equal, as well as their lengths, with the transistor placed in a vertical position the thermal resistances R_{CA_T} and R_{CA_B} should also be approximately the same.

For illustration purposes, Fig. 5 shows how ambient temperatures, and therefore the resistances (R_{CA_T} and R_{CA_B}), are equal in both sides of the transistor with this placed in a vertical position. This can be corroborated by observing the result from Finite Element Method (FEM) simulations [12].

Consequently, assuming R_{CA_T} and R_{CA_B} equal to R_{CA}, R_{EQ} results in

$$R_{EQ} = \frac{R_{CA}\,(R_{JC_T} - R_{JC_B})}{R_{JC_T} + R_{JC_B} + 2R_{CA}}. \tag{13}$$

Also, if Eq. 8 is divided by Eq. 9, it is possible to determine the value of D as

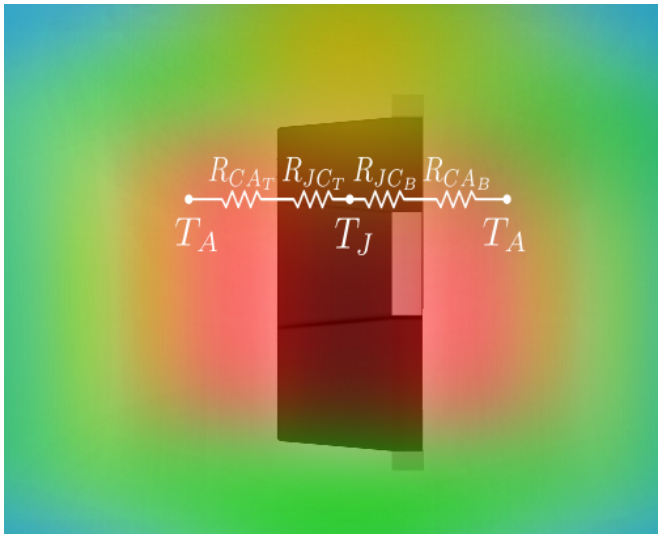


Fig. 5: Illustration of how heat spreads symmetrically when the transistor is not attached to any PCB and it is placed vertically.

$$\frac{T_{C_B} - T_A}{T_{C_T} - T_A} = \frac{D}{1-D} \rightarrow D = \frac{T_{C_B} - T_A}{T_{C_B} + T_{C_T} - 2T_A} \tag{14}$$

Making use of Eq. 4 and Eq. 6 it is also possible to determinate the power along each path. The dependence of D with the total power, and therefore with the temperature, is assumed negligible, as will be shown in the next section.

Regarding R_{CA_B} and R_{CA_T}, both resistances can be determined in a similar way by replacing the value of D in Eq. 8 and Eq. 9 respectively.

On the other hand, considering the single-path model used by the manufacturer and the typical value of thermal resistance capsule-junction R_{JC} provided by it, it is possible to estimate the temperature of the junction:

$$T_J = P \cdot D \cdot R_{JC_{Datasheet}} + T_{C_B} \tag{15}$$

Knowning T_J and D it is possible to determinate R_{JC_T}. This is:

$$R_{JC_T} = \frac{T_J - T_{C_T}}{P \cdot (1-D)} \tag{16}$$

3 Experimental Results

For validating the methodology, the proposed test bench shown in Fig. 4 has been built. The Device Under Test (DUT) is the Infineon 100V OptiMOS™ 5 power MOSFET IPT015N10N5 [13].

Temperatures in both bottom and top surfaces have been recorded for different power values. It is observed that, as no heatsink is used, high temperatures are reached for low power values as depicted in Fig. 7. These temperature values given by the thermocouples have been validated by an infrared camera.

By applying Eq. 14, the negligible dependence of D with power is corroborated as shown in Fig. 8. This allows to estimate the junction temperature (T_J) of the DUT through Eq. 15 and therefore calculate R_{JC_T} by using Eq. 16. This thermal resistance value is shown for different powers values in Fig. 9.

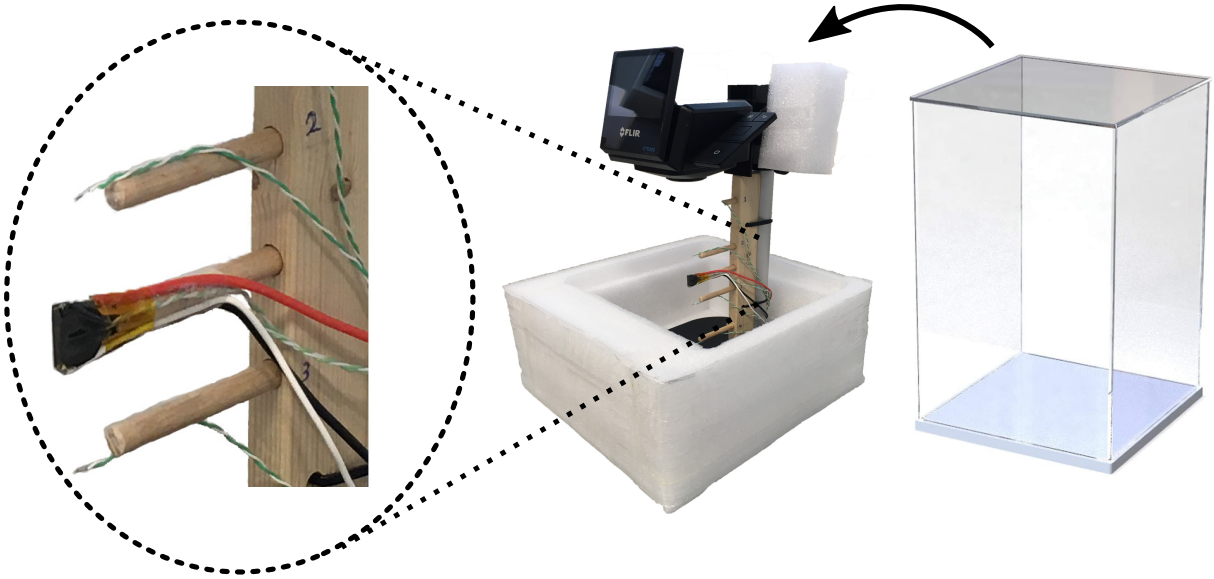


Fig. 6: Images of the built test bench to characterize the transistor inside a still air chamber, in vertical position and without being soldered to any PCB.

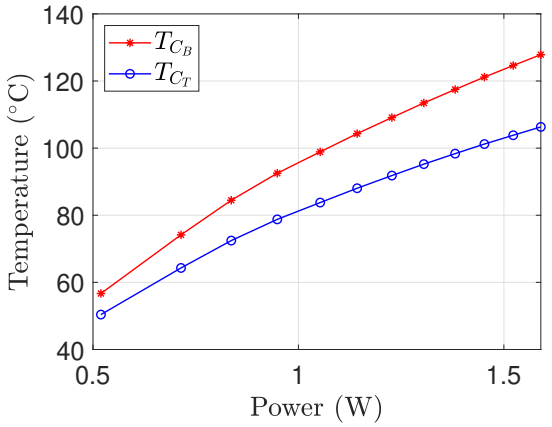


Fig. 7: Experimental relationship between the capsules temperatures (top and bottom) and the total power dissipated in the MOSFET.

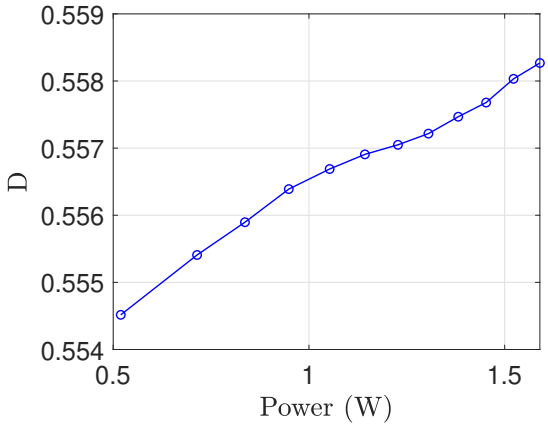


Fig. 8: Experimental relationship between the fraction of the power in the lower path and the total power dissipated in the MOSFET.

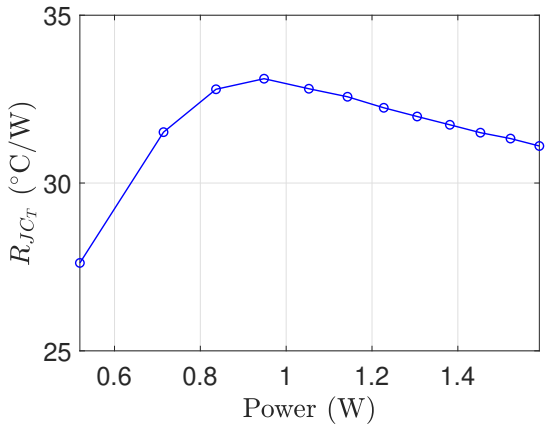


Fig. 9: Experimental values of the thermal resistance from the junction to the top capsule *vs* the power in the transistor.

4 Conclusion

This paper proposes a novel methodology for estimating the thermal resistance from junction-to-top capsule of power semiconductor devices. This characterization procedure takes into account the power from the junction to the top surface. The carried out research is based on the behaviour of a transistor located inside a natural convection still air chamber, in vertical position and without being soldered to any PCB. Under these operating conditions, and as is common in many types of transistor packages, with roughly equal dimensions and geometry on the top and bottom surfaces of the capsule, it is possible to determine the value of thermal resistances in a two-path equivalent thermal circuit, as well as the fraction of power associated with each path. This methodology is applied to a real transistor and results are shown.

References

[1] Giuseppe Iannaccone, Christian Sbrana, Iacopo Morelli, and Sebastiano Strangio. Power electronics based on wide-bandgap semiconductors: Opportunities and challenges. *IEEE Access*, 9:139446–139456, 2021.

[2] Thermal Resistance Theory and Practice. Application note, Infineon Technologies, January 2000.

[3] Gongyue Tang, Tai chong Chai, and Xiaowu Zhang. Thermal optimization and characterization of sic-based high power electronics packages with advanced thermal design. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 9(5):854–863, 2019.

[4] TO-Leaded Top Side Cooling. Application note, Infineon Technologies, May 2021.

[5] ISC230N10NM6 -OptiMOS™ 6 Power-Transistor, 100V. Datasheet, Infineon Technologies, July 2021.

[6] Heng Yun Zhang, Xiao Wu Zhang, B. L. Lau, Sharon Lim, Liang Ding, and M. B. Yu. Thermal characterization of both bare die and overmolded 2.5-d packages on through silicon interposers. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 4(5):807–816, 2014.

[7] Y. Tal and A. Nabi. A simple analytic method for converting standardized ic-package thermal resistances (θ_{ja}, θ_{jc}) into a two-resistor model (θ_{jb}, θ_{jt}). In *Seventeenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.01CH37189)*, pages 134–144, 2001.

[8] JESD51-14 - Methodology for the Thermal Measurement of Component Packages (Singular Semiconductor Device). Standard, JEDEC-Solid State Technology Association, January 2010.

[9] Qinghong He, Shane Smith, and Guohua Xiong. Thermocouple attachment using epoxy in electronic system thermal measurements — a numerical experiment. In *2011 27th Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, pages 280–291, 2011.

[10] Precautions When Measuring the Rear of the Package with a Thermocouple. Application note, ROHM Semiconductor, October 2020.

[11] Papa Momar Souare, Mamadou Kabirou Toure, Stephanie Allard, Benoit Foisy, Bijan Borzou, Eric Duchesne, and Julien Sylvestre. High precision numerical and experimental thermal studies of microelectronic packages in still air chamber tests. In *2018 7th Electronic System-Integration Technology Conference (ESTC)*, pages 1–8, 2018.

[12] Pavel P. Khramtsov Oleg G. Martynenko. *Free-Convective Heat Transfer: With Many Photographs of Flows and Heat Exchange*. Springer Berlin, Heidelberg, 2005.

[13] IPT015N10N5 - 100V OptiMOS™ 5 power MOSFET in TOLL. Datasheet, Infineon Technologies, October 2016.