IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received May 21, 2020, accepted June 11, 2020, date of publication June 22, 2020, date of current version July 2, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3004238

Scalable Modeling Approach and Robust Hardware-in-the-Loop Testing of an Optimized Interleaved Bidirectional HV DC/DC Converter for Electric Vehicle Drivetrains

SAJIB CHAKRABORTY[1,2], (Member, IEEE), MIKEL MAZUELA[3], (Member, IEEE), DAI-DUONG TRAN[1,2], (Student Member, IEEE), JAVIER A. COREA-ARAUJO[4], YUANFENG LAN[1,2], ARGIÑE ALACANO LOITI[3], (Member, IEEE), PATRICE GARMIER[4], IOSU AIZPURU[3], (Associate Member, IEEE), AND OMAR HEGAZY[1,2], (Member, IEEE)

[1]MOBI Research Group, ETEC Department, Vrije Universiteit Brussel (VUB), 1050 Brussels, Belgium
[2]Flanders Make, 3001 Heverlee, Belgium
[3]Electronics and Computing Department, Mondragon Unibertsitatea, 20500 Mondragón, Spain
[4]Applus IDIADA Group, 43710 Santa Oliva, Spain

Corresponding author: Omar Hegazy (omar.hegazy@vub.be)

This work was supported by the European Union's Horizon 2020 Research and Innovation Program under Grant 769935 (HiFi_Elements).

ABSTRACT Automotive Original Equipment Manufacturers (OEMs) require varying levels of functionalities and model details at different phases of the electric vehicles (EV) development process, with a trade-off between accuracy and execution time. This article proposes a scalable modelling approach depending on the multi-objective targets between model functionalities, accuracy and execution time. In this article, four different fidelity levels of modelling approaches are described based on the model functionalities, accuracy and execution time. The highest error observed between the low fidelity (LoFi) map-based model and the high fidelity (HiFi) physics-based model is 5.04%; while, the simulation time of the LoFi model is $\sim 10^4$ times faster than corresponding one of the HiFi model. A detailed comparison of all characteristics between multi-fidelity models is demonstrated in this paper. Furthermore, a dSPACE SCALEXIO Hardware-in-the-Loop (HiL) testbench, equipped with a minimal latency of 18μsec, is used for real-time (RT) model implementation of the EV's HV DC/DC converter. The performance of the entire HiL setup is compared with the Model-in-the-Loop (MiL) setup and the highest RMSE is limited to 0.54 among the HiL and MiL results. Moreover, the accuracy (95.7%) of the passive component loss estimation is verified through the Finite Element Method (FEM) software model. Finally, the experimental results of a full-scale 30-kW SiC DC/DC converter prototype are presented to validate the accuracy and correlation between multi-fidelity models. It has been observed that the efficiency deviation between the hardware prototype and multi-fidelity models is less than 1.25% at full load. Furthermore, the SiC Interleaved Bidirectional Converter (IBC) prototype achieves a high efficiency of 98.4% at rated load condition.

INDEX TERMS DC/DC interleaved converter, EV, efficiency, electro-thermal modelling, multi-fidelity models, optimization, scalable modelling, hardware-in-the-loop, and wide-bandgap technology.

I. INTRODUCTION

The average temperature of global land and ocean in June 2019 was more than 1.71°C above average and it was record-breaking temperature since global records calculation started in 1880 [1]. The potential scarcity of fossil fuels and global warming due to greenhouse gases (GHG) emissions are stimulating the shift towards zero carbon Electric Vehicles (EVs) research. EV research is vastly dependent on the growth of the EV-market, which is expected to grow five-fold between 2017 to 2025 [2], reaching a forecasted global EV-market size of approximately €500 million by 2025 [2], [3]. The EVs are becoming a prime choice thanks to battery lifetime improvements, decreasing battery price, high

The associate editor coordinating the review of this manuscript and approving it for publication was M A Hannan.

performance and reliability of power electronic (PE) components, enhanced energy efficiency, affordability and environmental awareness of policymakers and consumers [4], [5]. To keep pace with the exponentially expanding EV-market, current research is challenged to investigate the reduction of time-to-market, cost, energy consumption, while confirming the improvement in safety and comfort [6]. These challenges demand the growth of the efficacy of the development process and testing time, leading to virtualization in the design phase. Therefore, modelling and simulation have been established as a mandatory part of virtualisation tool at the conceptual design stage in the place of physical tests, as real-time (RT) testing is a time-consuming and highly costly process [6]–[8].

Hence, accurate and scalable modelling of the EV PE components is a crucial method to achieve a highly reliable simulation tool for system characterizations, optimization, validation and performance measurement in the early design phase.

A. ISSUES IN HIGHLY ACCURATE MODEL

To accomplish the safety design functionality of the EV power electronics (PEs) components, several hundred kilometres of test data are required based on targeted vehicle type and legislation such as the New European Driving Cycle (NEDC), a European certified cycle for light-duty EV with an average speed of 33.6 km/h and having 1180s duration, the EPA Federal Test Procedure (FTP-75) and Japanese cycle (JC-08) are certified in the USA and Japan respectively, having an average speed of 34.1km/h and 24.4km/h, and duration of 1874s and 1204s [9], [10]. These tests evaluate the performance (controllability, efficiency, and ageing), safety, and manufacturability of EV components. This process involves extensive test coverage in the virtual platform, which mandates 8000 h–10000 h of the EV simulation as a set of complete life cycle requirements [11]. A detailed and accurate HiFi simulation model could slow down the whole EV simulation process as the HiFi PE component's simulation requires very small simulation step-size (1 μs or 0.1 μs) to attain highly accurate results [12]–[16]. In contrast, a standard step-size for an entire EV simulation is 0.01s [17]. When using 1 μs step size to simulate a HiFi model of an EV, approximately 15 minutes is required to perform just 1ms of simulation using a personal computer (PC) with Intel® Core™ i7 Processors. Hence, this PC would require approximately 52 years to simulate one complete Worldwide Harmonized Light Vehicle Test Procedure (WLTP) driving cycle.

B. SCALABLE MODELLING APPROACH

To speed up the power electronics component's simulation time, a multi-scale modelling approach is proposed as a proper solution [6], [16], [18]. Scalable modelling has consisted of High-Fidelity (HiFi) modelling, Medium-Fidelity (MFi) modelling, Low-Fidelity (LoFi) modelling, and map-based modelling, with simulation step-sizes varying from 0.1 μs to 0.01s. As the simulation step-size are increased, there is a high chance to lose accuracy. A few functionalities need to be compromised from model to model, such as short circuit test, transition impact on voltage and current due to device turn on and off, sensitivity to duty ratio and temperature response during critical behaviour (braking/rush driving) [12], [18]. According to the model's functionalities, the HiFi model is employed for fault diagnosis and prognosis of the optimized PE converter's (PEC) semiconductor module and thermal model. The MFi model is focused on the mission-profile oriented temperature profile of all devices in the context of ageing stress and durability analysis. This modelling technique represents Design for Reliability (DfR) of the PECs in the EVs application to predict reliability and durability benchmarks. Thanks to a less accurate fast models for speeding the several EV optimization tasks and several thousands of EV driving simulation.

C. NECESSITY OF HARDWARE-IN-THE LOOP TESTING

Currently, the OEMs prefer to use Model-based-Development (MBD) techniques for PE components, which introduce HiL tests for the EVs traction subsystems [19], [20]. At the design stage, the HiL testbench can be utilized to verify the effect of the inclusion of Wide Band-Gap semiconductors (WBGs), such as Silicon-Carbide (SiC) and Gallium Nitride (GaN), in the EVs of the PE converters [19], [21]. The stress in the PE converters due to using WBGs is precisely measured using the RT-models. In addition, the RT-models can be utilized as digital-twins for predictive maintenance of the EVs components [22]. Moreover, the RT-models can be used to verify the reliability of the PE converters for different mission profiles, thus providing a guideline to estimate the PE components ageing factor [23]. Hence, an RT-model analysis can facilitate the creation of an innovative system configuration for a new class of affordable, safe and efficient EV with less scrutiny [6], [16].

D. ROLE OF THE HV DC/DC CONVERTER IN THE BEVS

The battery electric vehicles (BEVs) have multiple architectural variants. FIGURE 1 depicts a simplified block diagram of the BEV powertrain, which is the most common architecture of the BEV drivetrain, currently available on the market [24], [25].

The BEV drivetrain architecture consists of:

- Rear Wheel Drive (RWD);
- Electric Motor (EM);
- Differential Transmission;
- Optional High Voltage (HV) DC/DC Converter between Battery and Motor driver (Inverter).

In the BEVs, the voltage level of the propulsion battery system is 48V–375V, which is usually lower than the required voltage of 400V–750V for the EM [26]. Therefore, high voltage (HV) DC/DC converter topologies are commonly used to interface the battery with the HV DC link in the BEVs drivetrains. The HV DC/DC converter can provide a fixed or variable DC link voltage regardless variation of the battery voltage. The DC/DC converter also allows a higher

DC-link voltage than the battery voltage, as mentioned above. The higher voltage offers higher efficiency in the drive system components (such as PE and EM) and prolongs battery lifetime. Furthermore, low voltage in battery systems permit to reduce the complexity of battery packs reducing series connection of cells, increasing safety, recovering more energy during regenerative braking and finally reducing the cost of the battery system. Disadvantages include higher costs and losses from the converter itself [26], [27]. In the BEVs, the HV DC/DC converter needs to support bidirectional power flow while ensuring efficient energy conversion and provides a variable DC link optimizing the inverter efficiency according to the operating modes. In the propulsion mode, energy flows from the battery to the motor load, while in regenerative braking mode, the momentum of the vehicle enables the EM to act as a generator, transferring the energy back to the battery.

E. AUTOMOTIVE HV DC/DC CONVERTER'S RESEARCH TRENDS

In recent years, several bidirectional HV DC/DC converter topologies have been studied and designed for the BEV applications such as Synchronous Boost Converter (SBC) [27], Resonant Boost Converter (RBC) [28], Full-Bridge Converter (FC) [27], ZVS-Boost converter (ZBC) [29], Multidevice Interleaved Boost Converter (MDIBC) [30], Multiport converter (MPC) [31], and 3-Phase Interleaved Bidirectional Converter (IBC) [32]. Each topology has its own advantages and drawbacks and should be chosen based on the functionalities, requirements, efficiency, component count, controllability, compactness, cost and reliability [26]. For the high-power BEV a standard 3-phase IBC topology has been proposed in [4], [22], [26], [31]–[37], thanks to its less device current stress, simple controllability, compact design, high power-density, better efficiency and high reliability. Numerous articles have been published on the HV DC/DC converter for the EVs applications. On the one hand, the MDIBC presented in [30], [38], depicts a converter topology and operation with average losses of converter at rated load, digital control technique and hardware-prototype. In [39], a detailed structure of a 4-Phase IBC is presented, together with an advanced control technique and experimental results. In [31], a suitable MPC topology, an optimization process and an average losses model is proposed. On the other hand, authors in [40], describe a 2-phase IBC with a detailed DSP-based controller and verified results with a 1 kW and 120 V hardware prototype. Additionally, a 6-phase interleaved FC is proposed in [41], it describes a detailed HiL setup for the HV DC/DC converter in Class 3 vehicle system and illustrated advantages of the inclusion the converter in the EVs. A 3-phase DC multifunctional converter is presented in [35], considering the functionality of the topology, the control scheme and the average losses contribution of the semiconductor modules. Finally, a time-efficient electro-thermal model of a 3-phase IBC is presented in [42].

F. CONTRIBUTIONS OF THIS ARTICLE

None of these publications in [26]–[44], discussed converter's optimization processes with detailed modelling issues such as universal switch model, instantaneous loss profile of power device and passive components (inductor and capacitor) and liquid-cooling thermal modelling for dynamic BEV simulation.

The unique scalable modelling approach presented in this article will guide the non-power electronics users (OEMs/end users) to select the appropriate fidelity based on the testing purpose and development objectives of the BEVs as the short circuit testing in the semiconductor module or the energy consumption and the thermal consumption routine optimization of several hundred km of the EV's driving do not required the same level of functionalities, accuracy and speed.

While most of the publications usually present a single semiconductor technology modelling as Silicon [30], [37] or Silicon Carbide (SiC) [15], [43]–[45], this article depicts a universal modelling technique for interchangeable semiconductor technologies and evaluates the superiority of utilizing the WBGs in the DC/DC converter topology in terms of power losses and efficiency.

Moreover, this article presents a detailed HiL model preparation method with a low latency of 18μsec, which could be utilized by all the automotive power electronics engineers to attain acceptable accuracy in comparison with a model-in-the-loop (MiL) model.

G. ARTICLE ORGANIZATION

This article is structured as follows. Section II depicts the converter structure, system specifications and optimization methodology of the converter to meet the system design objectives. Section III presents the detailed electrical behaviour modelling technique of the semiconductor devices, including switch and diode. Section IV describes a comprehensive thermal behaviour modelling approach of the semiconductor devices. Section V shows 1D and 3D modelling and losses estimation techniques of the passive components (inductor and capacitor). Section VI describes the robust RT-modelling method for HiL setup using a minimal sampling rate. Afterward, section VII analyses scalability approaches of the multi-fidelity models. Section VIII illustrates the experimental results of a full-scale 30-kW SiC-based IBC prototype. Section IX presents the comparison between HiL and MiL results and shows performance comparison among multi-fidelity models characteristics. In addition, the accuracy of the passive components losses and IBC efficiency are compared. The conclusions and recommendations are presented in Section X.

II. CONVERTER TOPOLOGY, SPECIFICATIONS AND OPTIMIZATION METHODOLOGY

An interleaved bidirectional 2-Level 3-Phase voltage source converter is selected as the HV DC/DC converter topology.

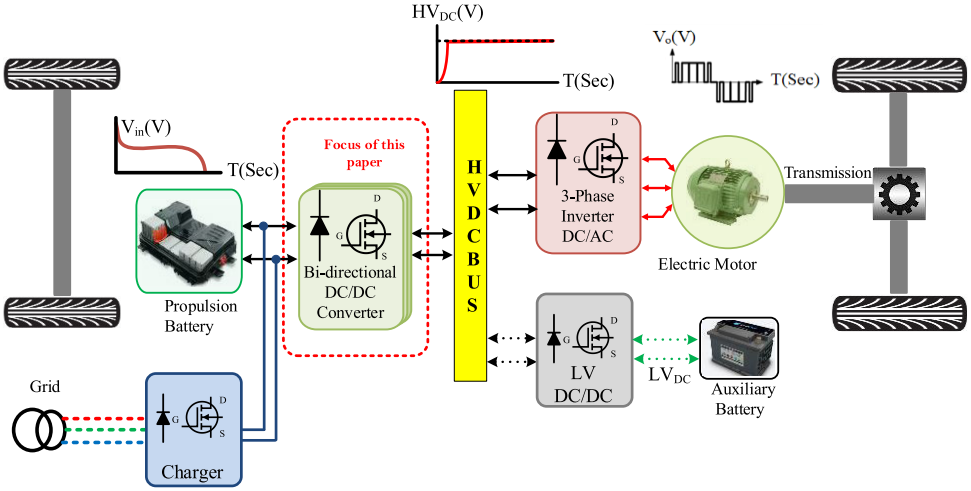


FIGURE 1. Simplified block diagram of battery EV powertrain. $V_{in}(V)$, $HV_{DC}(V)$ and $V_o(V)$ are the battery voltage, High voltage DC bus and Inverter voltage, respectively.

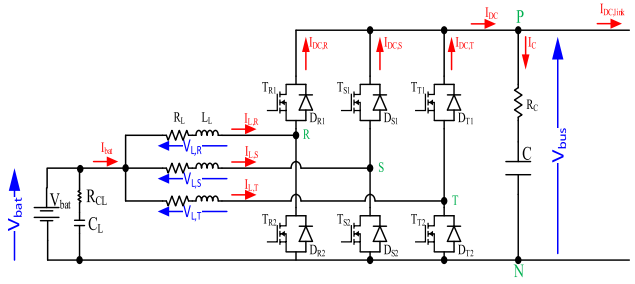


FIGURE 2. Ideal-topology structure of the 2 level 3-phase IBC (with interleaved phase current I_{LRST} and phase voltage V_{LRST}, V_{bat}, six switches and antiparallel diodes, V_{bus} and I_{Dc} are highlighted). Equivalent series resistance (ESR) of the capacitor R_C and internal resistance of interleaved inductors R_L are also highlighted. Here, V_{bat} is the battery voltage, V_{bus} is regulated DC-link voltage and it is connected to the EM through a 3-phase motor drive named as DC/AC converter.

FIGURE 2 depicts the topology structure of the IBC, which comprises six power switches and six antiparallel diodes: T_{R1}-D_{R1}, T_{R2}-D_{R2}, T_{S1}-D_{S1}, T_{S2}-D_{S2}, T_{T1}-D_{T1}, T_{T2}-D_{T2}; three interleaved inductors L_1, L_2 and L_3; a DC-Link capacitor C and input side capacitor C_L.

The limited driving range has constrained growth in the EVs applications in the past decade. Hence, regenerative braking (RB) has been developed as the most appropriate approach for extending the driving range of EVs. Using the RB of the EVs, kinetic energy can be converted into electrical energy in the EM, which charges the battery. The transfer of electrical energy from the EM to the battery requires a converter. For converting load voltage from 400V–750V to 240V–375V, a buck converter is required. As the battery is recharged through the RB, the battery state-of-charge (SoC) increases, which expands the battery lifetime. Besides, the maximum battery charging current is kept limited, even during the maximum power period of the EM, to ensure the battery protection from the large charging current. The detailed operational mode of the IBC is discussed below.

A. MODES OF OPERATION

In the propulsion mode, the IBC operates as a boost converter and the energy flows from the battery to the EM. During this mode T_{R2}, T_{S2} and T_{T2} are used as primary switches, which are alternately switched on or off at the switching frequency f_{sw}, while switches T_{R1}, T_{S1} and T_{T1} remain switched off. When T_{R2}, T_{S2} and T_{T2} are switched on, the current in the inductors increase and store energy by creating a magnetic field. When T_{R2}, T_{S2} and T_{T2} are switched off, the current of the inductor flows through the free-wheeling diode D_{R1}, D_{S1} and D_{T1}. In the RB mode, the IBC operates as a buck converter and energy flows from the EM to the battery, thus allowing the battery to recapture some of the braking energy. During this mode, T_{R1}, T_{S1} and T_{T1} are used as primary switches, which are alternatively switched on or off at the switching frequency f_{sw}, while switches T_{R2}, T_{S2} and T_{T2} remain switched off. When T_{R1}, T_{S1} and T_{T1} are switched on, the inductor current flows linearly from the EM to the battery. When T_{R1}, T_{S1} and T_{T1} are switched off, the current of the inductor flows through the free-wheeling diode D_{R2}, D_{S2} and D_{T2}.

The L_R inductor stores energy in both modes of the IBC operation when T_{R1} or T_{R2} is switched off, the L_S inductor stores energy when T_{S1} or T_{S2} is switched off, and the L_T inductor stores energy when T_{T1} or T_{T2} is switched off. Such inductors operate in propulsion mode as the boost inductors and the braking mode as low-pass filter inductors. The DC-link capacitor and C_L act as the energy buffer for smoothing.

The phase shift between interleaved phase switches is 120°, which reduces the ripple current flowing into these inductors for acceptable ripple voltages on both the DC-link side and the battery side. In addition, this interleaving technique allows the IBC to work at reduced power due to the failure of parallel strings of the battery cells. Hence, in the EVs, the IBC modularity helps the EM to function even under cell-defective conditions, prolonging BEVs' lifespan.

TABLE 1. Specifications and initial design parameters of the target design.

Parameter	Value
Nominal battery pack voltage	324 V
Battery pack configuration	96 series and 2 parallel
Battery pack voltage range	240V~375V
Continuous Charge/Discharge current	75A/-75A
Peak charge/discharge current	150A/-140A
Rated Power	30kW
Peak Power	75kW
DC-link Voltage	400V/700V

TABLE 2. Parameters of HV IBC.

Converter Parameters	Values
Inductance [L]	175.5 µH
○ Inductor Core	AMCC50Metglas
○ Inductor resistance [R_L]	2.53 mΩ
○ Number of turns	17
Output Capacitance [C]	160 µF
○ Type	947C
○ ESR [R_C]	1.80 mΩ
Switching frequency [f_{sw}]	60 kHz
Semiconductor power module	SiC: CAS120M12Bm2 Si: FF150R12RT4
Cooling Process	Liquid
○ Coolant material	50%-50% water glycol
○ Max. allowable Coolant Spread	283.15-363.15 K

B. SYSTEM SPECIFICATIONS

A light-duty commercial BEVs' battery specifications and initial parameters are selected as the target specifications. The boundary value condition for the IBC has been chosen based on the design target. The specifications and initial design parameters are shown in TABLE 1.

C. DESIGN OPTIMIZATION OF THE CONVERTER

The IBC's design parameters are shown in Table 2, which is formulated using a Multi-Objective Genetic Algorithm (MOGA) Optimization tool to achieve high-efficiency and high power density while meeting the specifications and initial design parameters of the system as shown in TABLE 1.

This subsection shows, in chronological order, the steps followed in the optimization tool:

a. First, the objective functions for the optimization process are identified in equation (1):

$$\textit{Objectives}: \underset{X=[N_{ph}\, f_{sw}, idx_{core}, \Delta V_{DC\ Link}]}{\textit{minimize}} \begin{cases} \Delta I_{in}(X) \\ W\Sigma ind(X) \\ Ploss(X) \\ V_{DC\_Link}(X) \end{cases} \tag{1}$$

b. Then, all degrees of freedom (DoF) and constraints in the converter designing process are categorized as per equation (2). Afterward, lower, and upper bound values have been selected to generate meaningful results for each DoF.

$$[\textit{Constraints}] \xrightarrow{s.t.} \begin{cases} 1 \le N_{ph} \le 6 \\ 20\,kHz \le f_{sw} \le 65\,kHz \\ \Delta I_{in_{BAT}} \le 7.5\% I_{in_{BAT}} \\ W_{\Sigma ind} \le 5\,kg \\ \Delta V_{DC\_Link} \le 2.5\% V_{DC\_Link} \end{cases} \tag{2}$$

c. Non-dominated Sorting Genetic Algorithm-II (NSGA-II) [46] is utilized to solve the non-convex and mixed-integer multi-objective optimization problem in (1). The presence of multiple objectives in a problem results in a set of Pareto-optimal solutions, as shown in FIGURE 3.

d. Finally, the average ranking method (*AR*) is used to obtain the most appropriate solution [47] from the set of Pareto-fronts for the above-mentioned system specifications and constraints. The optimal solution is coloured as a red point in FIGURE 3.

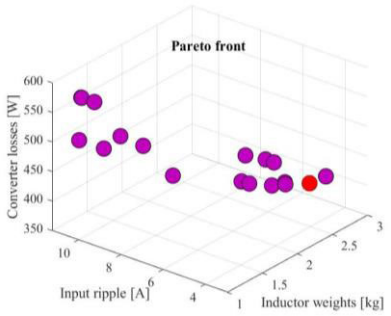


FIGURE 3. Purple points indicate Pareto optimal solutions of the multi-objective optimization and red mark denotes the optimal global solution. Where the total inductor weight is 2.4kg/phase, the ripple current is 3.8A/phase and the average converter loss is 432W (~98.5% η at full load).

The optimal value for the number of phases (N_{ph_min}), switching frequency (f_{sw_min}), the inductance value (L_{ph_min}), and the capacitance value ($C_{DC\_Link\_min}$) are obtained to fulfill the system functional requirements using the developed MOGA optimization tool, whose detailed method is derived in [31].

III. SEMICONDUCTORS: ELECTRICAL BEHAVIOUR MODELLING

As described previously, the semiconductors (three pairs of controlled switches and their antiparallel diodes) allow controlling the transferred power in both buck and boost modes of the DC-DC converter. These semiconductors are modelled in this work considering the following physical phenomena, according to the description of [16]:

- Conduction behaviour;
- Switching power losses;
- Blocking behaviour;
- Thermal behaviour.

To develop a fast simulation tool, a model based on the universal losses model has been implemented, which is named as the 3rd approach in [46].

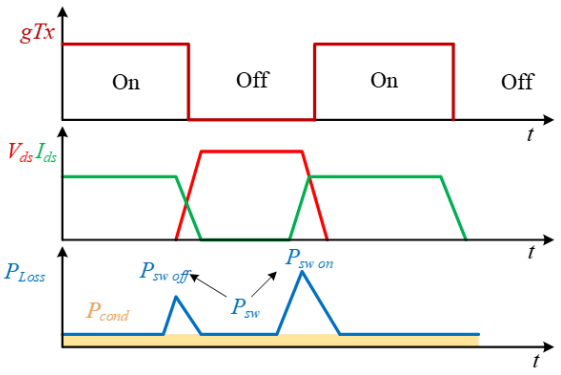


FIGURE 4. Electric behaviour modelling: ideal conduction voltage and current waveform (V_{ds}, I_{ds}), switching waveform (gTx), conduction and switching losses estimation (P_{cond}, P_{sw}).

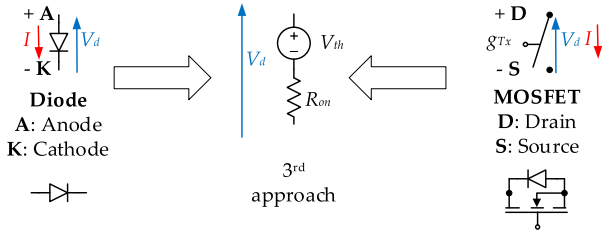


FIGURE 5. Analysis of the implementation of the 3rd approach in a diode and a MOSFET configuration.

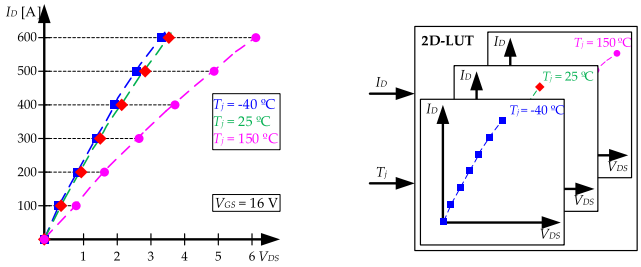


FIGURE 6. 2D-LuT implementation for semiconductor's voltage drop modelling.

The universal losses model comprises the decoupling of the conduction and the switching losses of the semiconductor. The semiconductor is modelled as electrically ideal as shown in FIGURE 4 and the power losses are calculated in parallel considering the obtained ideal current and voltage waveforms.

In the first term, the conduction model requires identifying which semiconductor is conducting, considering the topology of the converter, and depending on the instantaneous current and gate commands of this branch's active switches (gTx). The switching model relies on the identification of the instantaneous conducting semiconductors, i.e. identifying the semiconductors which are switched on and off in each transition. Once the conductive semiconductors are identified, a voltage drop is calculated between their terminals and thus the losses of the conductions are estimated using instantaneous losses (Psw, on, Psw, off), shown in FIGURE 4, according to the ideal waveforms of current and voltage involved.

In terms of the blocking behaviour of the semiconductors, the losses produced during the blocking state can be considered negligible compared to conduction or switching losses. Modelling a specific blocking model could only be worthwhile for a few particular working conditions, such as standby operation. Thus, ideal blocking behaviour (null current conduction during off state) has been considered for most of the developed fidelity models. The blocking behaviour has only been implemented in the Simscape Multibody™ based high-accuracy HiFi model, because it requires a real physical behaviour (a several megaohms resistor has been considered), but the resultant blocking current and losses are negligible.

A. CONDUCTION LOSSES MODEL

The conduction losses of any semiconductor is usually calculated as the sum of a threshold voltage drop (V_{th}) and an on-resistance (R_{on}) voltage drop because of its simplicity and relative accuracy, as shown in FIGURE 5 [48]. Present modelling tools allow implementing more accurate models efficiently utilizing multi-dimensional lookup tables (LuT), which simplify the coupling between different variables such as voltage, current and temperature, in exchange for a slightly higher computational cost.

Taking into account the accuracy and computational cost requirements of a given application, different modelling approaches can be defined, as described in [16], from the most accurate current-and-temperature-dependent LuT-based conduction model to an ideal (null losses) conduction model.

For this work, a 2D-LuT based conduction model, as shown in FIGURE 6, in which the voltage drop produced during conduction (V_d) depends on the conducted current and the junction temperature is considered. The instantaneous voltage applied to the inductance of each interleaved phase depends on the voltage drops of the conducting semiconductors in that phase. The conduction losses are modelled according to the voltage drop by means of equation (3).

$$P_{cond} = V_d \cdot I \tag{3}$$

Different accuracy levels can be achieved regarding the conduction losses depending on the model chosen for the voltage drop, as explained in [16]. As the voltage drop model for this work is based on a 2D-LuT, which couples the current and temperature dependence, the conduction losses are modelled according to equation (4).

$$P_{cond}\left(I, T_j\right) = V_{d,2D-LuT}\left(I, T_j\right) \cdot I \tag{4}$$

B. SWITCHING LOSSES MODEL

As described previously, the universal losses model [12], [49]–[51] simplifies the switching transitions considering them ideal in electrical terms, thus avoiding the coexistence of current and voltage that would notoriously increase the complexity and computational cost of the model. The power losses produced in each transition are added afterwards as instantaneous energy losses ($E_{sw,on}$, $E_{sw,off}$), distributed along a switching step time T_s equation (5), depending on the

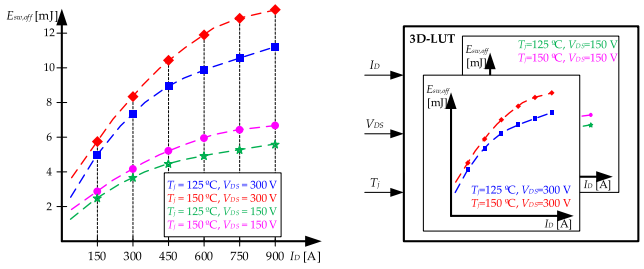


FIGURE 7. 3D-LuT implementation for semiconductor's turn off energy losses modelling.

immediately prior and immediately subsequent ideal voltage and current values.

$$P_{sw} = \frac{E_{sw}}{T_s} \tag{5}$$

The switching losses can be estimated by means of different approaches (ideal, analytical method, LuTs, etc.), as described in [16]. For this work, the most detailed model based on 3D-LuT is chosen, which considers the coupling of conducted current, blocking voltage and junction temperature, as shown in equations (6)-(7).

$$P_{sw,on}\left(I, V, T_j\right) = \frac{E_{sw,on,3D-LuT}\left(I, V, T_j\right)}{T_s}, \tag{6}$$

$$P_{sw,off}\left(I, V, T_j\right) = \frac{E_{sw,off,3D-LuT}\left(I, V, T_j\right)}{T_s} \tag{7}$$

where $E_{sw,on,3D-LuT}\ (I, V, T_j)$ and $E_{sw,off,3D-LuT}\ (I, V, T_j)$ refer to the current, voltage and junction temperature dependent on and off energy losses respectively as shown in FIGURE 7. The data to feed the LuT can be obtained from the datasheet or specific double pulse tests (DPT) performed on the semiconductors.

IV. SEMICONDUCTORS: THERMAL BEHAVIOUR MODELLING

The modelling variants of the semiconductors' electrical behaviour previously described, consider the coupling of the junction temperature with the current and voltage dependence. In order to obtain a junction temperature coupled to the instantaneous power losses, the thermal model of each semiconductor consisting of junction-to-case ($Z_{th,j-c}$), case-to-heatsink ($Z_{th,c-s}$) and heatsink-to-coolant ($Z_{th,s-a}$) models need to be implemented.

A. JUNCTION-TO-CASE THERMAL MODEL

The physical structure of a semiconductor's thermal model is usually represented as a cascaded RC network [12]. Although the Cauer model represents the real physical behaviour of materials inside each thermal layer, it results in a complex model. Therefore, Foster networks are usually preferred [52], as shown in FIGURE 8. The Foster network RC stages do not represent any physical layer; however, it can be provided with a model that mathematically behaves like a Cauer model with reduced complexity while it retains the accuracy.

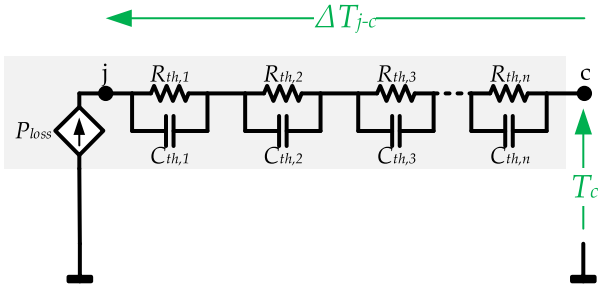


FIGURE 8. n layer Foster thermal circuit of a semiconductor. From junction temperature to ambient temperature, where the semiconductor is marked by a grey area.

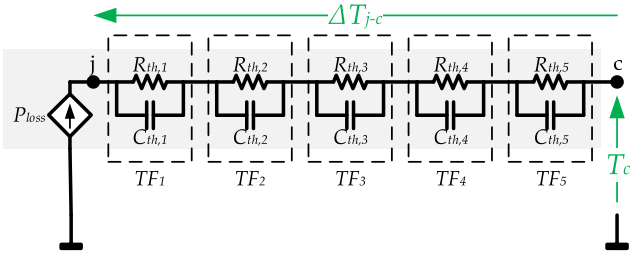


FIGURE 9. 5-layer semiconductor's Foster circuit, where each pair of RC can be transformed into a transfer function.

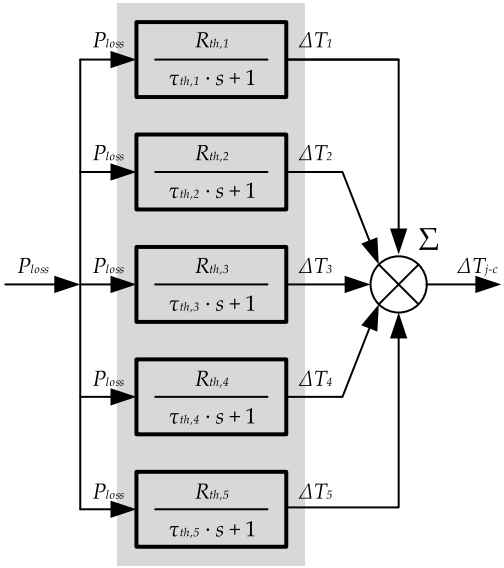


FIGURE 10. Semiconductor temperature calculation via transfer functions. The software underuse is Simulink.

Although different accuracy approaches can be implemented to model the thermal behaviour following the guidelines presented for the inverter in [16], among the different variants, the most accurate individual 5-stage thermal model is chosen for this work. A 5-stage thermal model is good enough for accurate approximation of the foster network.

This model consists of 5 cascaded RC Foster stages. Foster network simplicity lies in the fact that each RC stage can be transformed into a first-order transfer function, as depicted in FIGURE 9 and equation (8), which can easily be implemented in an equation-based simulator, illustrated in FIGURE 10. The sum of the temperature drop of each RC

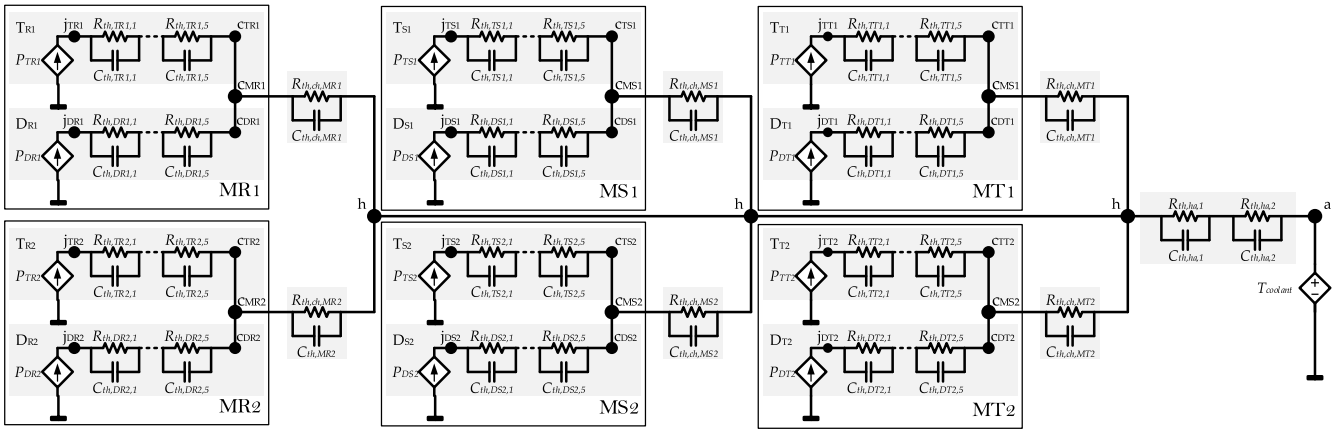


FIGURE 11. Equivalent thermal circuit of the 2 levels 3-phase IBC including heatsink, where each semiconductor's Foster circuit is marked with a grey area, MR1 and MR2 denote the R-phase, MS1 and MS2 denote S-phase and MT1 and MT2 denote T-phase.

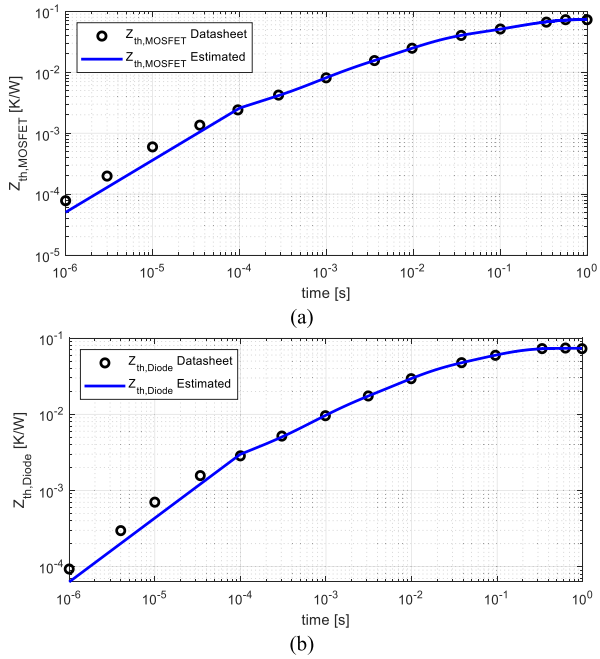


FIGURE 12. Thermal impedance estimation of (a) the MOSFET (b) Diode for Foster thermal network.

stage represents the junction-to-case temperature difference, where their input is the semiconductor's power loss and their output the temperature drop.

$$TF_i(s) = \frac{R_{th,i}}{\tau_{th,i} \cdot s + 1} \tag{8}$$

The parameters of each RC Foster network are obtained from the thermal impedance (junction-case) curve provided by the manufacturer using a single pulse test. The *time* (*x*-axis of *FIGURE 12) and thermal impedance* (*y*-axis of *FIGURE 12)* data from the datasheet curves are taken as input in the Curve fit tool of MATLAB®. Afterward, a coherent curve fitting technique is employed to estimate *Rth,i* and $C_{th,i}$ parameters of the desired RC Foster pairs [12], [52]. Time constant τ_{th} can be found via equation (9):

$$\tau_{th} = R_{th} \cdot C_{th} \tag{9}$$

The thermal model developed for a single semiconductor can be extended to the 2-level 3-phase IBC as depicted in FIGURE 11, and it is accordingly implemented in the Simulink model by linking the transfer function blocks of FIGURE 8 corresponding to each semiconductor.

The dynamic junction temperature can be calculated by using equations (10)-(12):

$$T_{jn} = T_{ch} + \Delta T_{JC} \tag{10}$$

$$\Delta T_{JS} = P_n Z_{th(jC)n} \tag{11}$$

$$Z_{th(jc)} = \frac{R_{th,1}}{\tau_{th,1}s + 1} + \frac{R_{th,2}}{\tau_{th,2}s + 1} + \frac{R_{th,3}}{\tau_{th,3}s + 1} + \frac{R_{th,4}}{\tau_{th,4}s + 1} + \frac{R_{th,5}}{\tau_{th,5}s + 1} \tag{12}$$

where T_{jn} is the junction temperature, ΔT_{JC} is the junction to the case temperature drop, $Z_{th(jC)}$ is the junction to case thermal impedance and P_n is the power losses of n^{th} MOSFET or diode in the converter, $R_{th,1-5}$ and $\tau_{th,1-5}$ are parameters of 5 stage foster network.

B. CASE-TO-HEATSINK THERMAL MODEL

Thermal grease is considered as the case to heatsink material. Again, the RC parameters of thermal grease are determined from vendor datasheet using the Curve fit tool of the MATLAB®. The separate switch and diode power losses merge into the case and flow into the heatsink and dissipate to the coolant. The case-to-heatsink temperature can be represented by equations (13)-(15).

$$T_{ch} = T_H + \Delta T_{ch} \tag{13}$$

$$\Delta T_{ch} = Z_{th(ch)} \sum P_{Total} \tag{14}$$

$$Z_{th(ch)} = \sum_{ch=1}^{2} R_{ch}(1 - e^{-\frac{t}{\tau_{ch}}}) \tag{15}$$

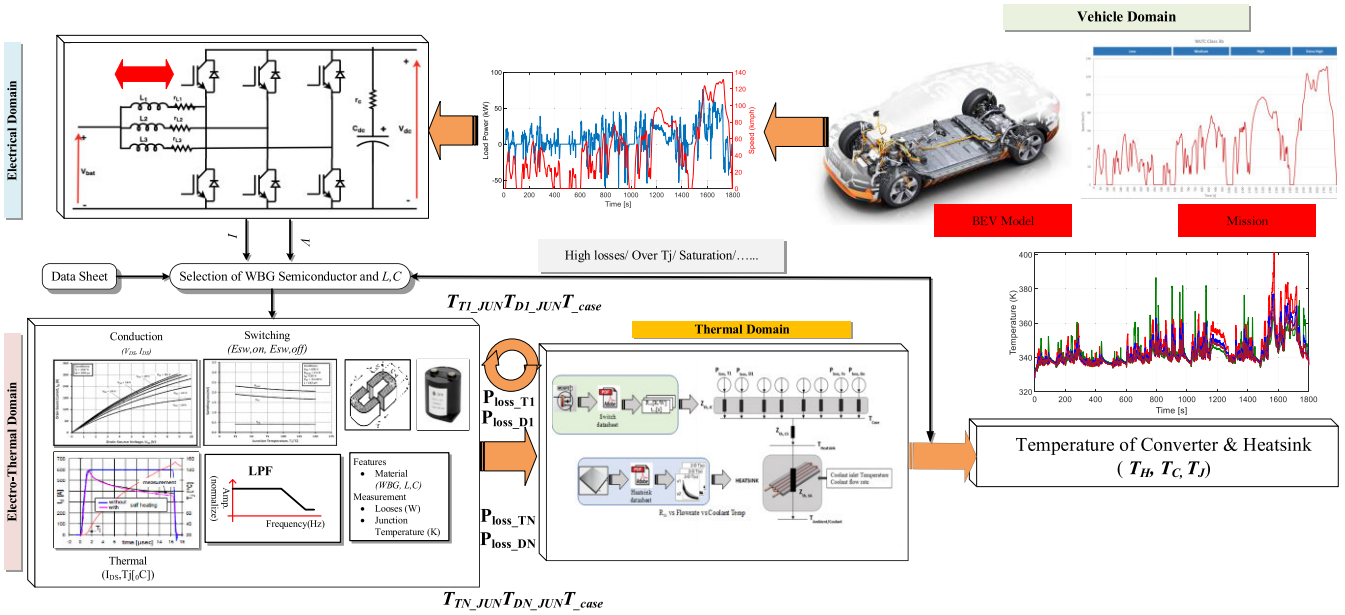


FIGURE 13. Stepwise mission profile based electro-thermal model representation of the IBC associated with the BEVs model.

where T_{ch} is the case temperature, ΔT_{ch} is case-to-heatsink temperature drop, $Z_{th(ch)}$ is the case thermal impedance, $R_{(ch)}$ is the grease thermal resistance and P_{Total} is the total power losses of MOSFET and diode in each switch module.

C. HEATSINK-TO-COOLANT THERMAL MODEL

Modelling an accurate heatsink-to-coolant thermal behaviour is a complex task since it is highly dependent on the mechanical setup of the heat exchanger and the cooling parameters such as coolant flow rate (l/min) and inlet coolant temperature. As explained in [16], two Foster stages model is implemented by following the example described in SEMIKRON's SKiiP1814 GB17E4-3DUW stack and can be formulated as equation (16).

$$Z_{th,ha} = \frac{R_{th,ha,1}}{\tau_{th,ha,2} \cdot s + 1} + \frac{R_{th,ha,2}}{\tau_{th,ha,1} \cdot s + 1} \tag{16}$$

Here, $R_{th,ha,1}$, $R_{th,ha,2}$ $\tau_{th,ha,1}$ *and* $\tau_{th,ha,2}$ represent the thermal parameters of the two Foster networks, and unlike the semiconductors' R_{th} and τ_{th} values, these parameters should be varied depending on the coolant flow rate and inlet coolant temperature. These variations can easily be implemented by means of LuT. The heatsink to coolant output temperature can be expressed as equations (17)-(18):

$$T_{ha} = T_{coolant} + \Delta T_{ha} \tag{17}$$

$$\Delta T_{ha} = Z_{th(ha)} \sum P_{Total,con} \tag{18}$$

where T_{ha} is the heatsink-to-coolant temperature, ΔT_{ha} is heatsink-to-coolant temperature drop, and $Z_{th(ha)}$ is the heatsink thermal impedance, $P_{Total,conv}$ is the total power losses of in the IBC.

The electro-thermal model of the HV DC-DC converter permits the coupling of the electrical losses output with the thermal circuit. The electro-thermal coupling allows accurate power losses to be obtained based on the electrical switching pattern and the junction temperature. A mission profile oriented stepwise modelling method of the IBC for the BEVs applications is depicted in FIGURE 13.

V. PASSIVE COMPONENTS MODELLING

The optimized values of inductance and capacitance have been selected based on the MOGA tool, as mentioned in Section-II. The goal of this section is to model high-performance inductors having high relative permeability with low eddy current using the available data of the vendors and estimating inductor loss accurately. As for the DC-link capacitor, it is selected with low equivalent series resistance (ESR) to reduce ripples and temperature rise in output voltage. Estimation of ESR is considered during the capacitor loss estimation.

A. INDUCTOR MODELLING IN 3D-FEM

A 3D-FEM model has been utilized to simulate the designed inductor. A second-order polynomial fitting function is used to find the inductance value in terms of airgaps and the number of turns, as shown in FIGURE 14(a).

The FEM simulation is also used to verify the optimal inductance value. The losses distribution in the inductor also simulated using FEM and the losses were highly localized on the edges of the core. The accuracy of the FEM losses compared to simulation losses is discussed in Section-IX. FIGURE 14(b) shows the FEM result of the flux density distribution and current distribution in the inductor.

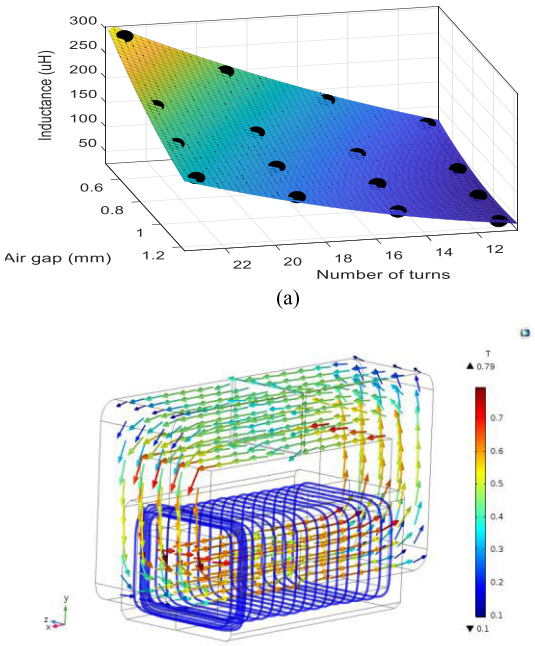


FIGURE 14. (a) FEM result of flux density and current distribution, (b) FEM result of inductance in terms of the air gap(mm) and No. of turns.

B. ESR ESTIMATION FOR CAPACITOR MODELLING

A function is used for capacitor selection based on Equivalent Series Resistance (ESR) as equation (19).

$$\mathrm{ESR} = \frac{R_2}{1 + (2\pi f)^2 C_2^2 R_2^2} + R_1 + R_0 \tag{19}$$

where R_0 = resistance of foil, tabs, and terminals (Ω), R_1 = resistance of electrolyte (Ω), R_2 = dielectric loss resistance (Ω), C_2 = dielectric loss capacitance (F), f = frequency (Hz). In according to system specification for maximum 75kW power ratings, type 947C and type 947D polypropylene DC link capacitors from Cornell Dubilier are analysed. After comparing both types, type 947C has been selected since it offered decidedly smaller ESR, the high capacitance per volume and low voltage ripples and temperature rise. The comparison of ESR as a function of frequency and temperature is shown in FIGURE 15, which ensures optimum response of type 947C capacitor at the same capacitance level.

C. LOSSES MODELLING OF PASSIVE COMPONENTS

The inductor loss is comprised of core loss P_{fe}, air-gap loss P_{gp} and copper loss P_{cu}. Rectangular HF 299 Litz wire is used to wire the inductor. The inductor copper loss P_{cu} can be calculated as equation (20):

$$P_{cu} = R_{Lz} I_{L,RMS}^2 \tag{20}$$

where R_{Lz} is the resistance of Litz wire and $I_{L,RMS}$ is the root-mean-square current of the inductors.

The Improved Generalized Steinmetz Equation (IGSE) is used to estimate the core losses and gap losses of the inductor

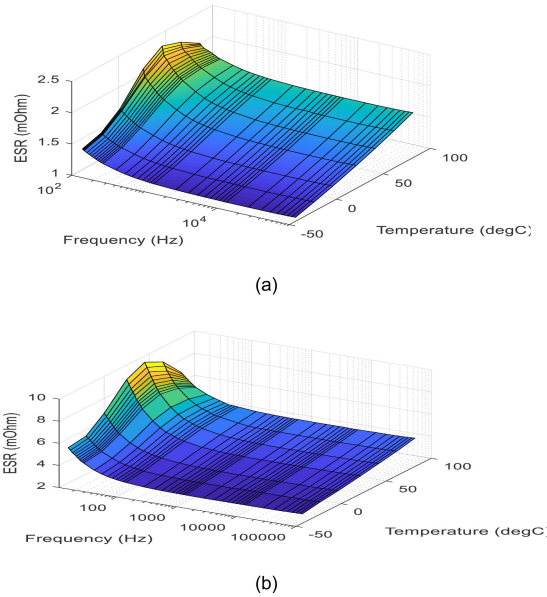


FIGURE 15. ESR model of capacitors at same capacitance: (a) Type 947C (b)Type 947D.

as equations (21)-(23), where SE parameters are taken into consideration. The parameters are accumulated from the vendor datasheet.

$$P_{fe} = W_t \left(k_{ns} k\, f_{sw}^{y} \Delta B_{max}^{x}\right) \tag{21}$$

$$P_{gp} = k_g . k . c . l_g . f_{sw} . \Delta B_{max}^{x} \tag{22}$$

$$\Delta B_{max}^{x} = \frac{0.4\pi NF \left(\frac{\Delta I}{2}\right) 10^{-4}}{l_g + \left(\frac{MPL_{cm}}{\mu_m}\right)} \tag{23}$$

where W_t is the weight of the core material, k_{ns} and k are the loss coefficients for non-sinusoidal waveform and C-shaped core material, f_{sw} is the switching frequency, B_{max} is the maximum flux-swing at the rated condition, x and y are core material parameters, k_g is the coefficient for gap loss, c is the core depth factor, l_g is the air-gap coefficient, N is the number of turns, F is the core packaging factor, ΔI is the current ripple, lg is the total gap length, MPL is the mean path length in cm, and μ_m is the material characteristics.

The expression for calculating DC-link capacitor losses is obtained from equation (24), where $I_{C,RMS}$ is the root-mean-square current value of the DC-link capacitor and ESR is capacitor equivalent series resistance, which is frequency depended shown in FIGURE 15.

$$P_{loss\_C} = I_{C,RMS}^2(t) ESR(f) \tag{24}$$

VI. THE IBC HIL TESTBENCH DEVELOPMENT

Standard modelling procedures are used by OEMs to reduce the time, cost, and risk associated with the full-scale testing of products. For that, model verification-based HiL has become a fundamental methodology used to make engineering predictions with confidence that can be quantified [41]. The HiL test consists of a type of RT simulation that verifies the modelling and the control system strategy of dedicated hardware that is

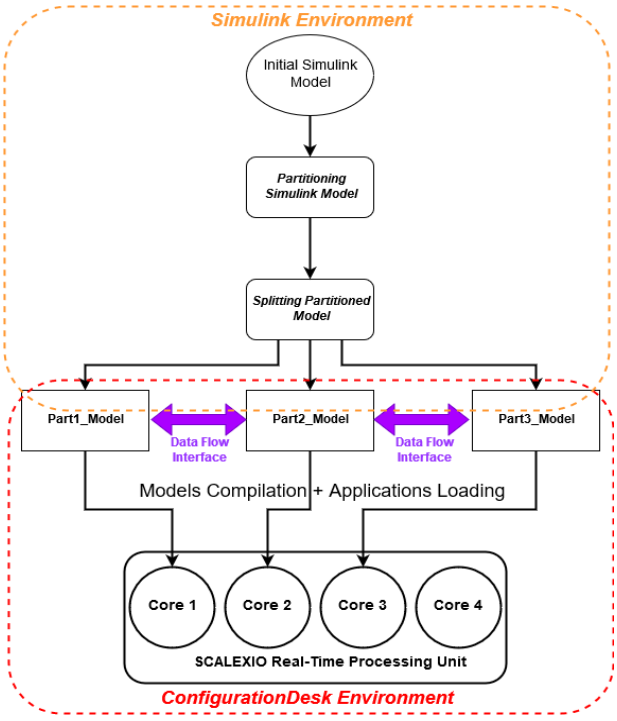


FIGURE 16. SCALEXIO based HiL setup for HV DCDC converter.

often in the development stage [53]. For power electronics systems, RT simulation is used as a step in the engineering process, either to validate the RT compatibility of models or to connect preliminary physical hardware to an RT digital control model to prove data compatibility [54]. The general structure used to evaluate a system model into an RT platform is presented in FIGURE 16.

The RT processing units, such as SCALEXIO is often composed of several different cores allowing parallel executions of simulation models to speed up simulations. To use this capability, the initial model must be split into as many sub-modules as available cores. Hence, a four-core SCALEXIO system is used for the HiL setup, and three cores are available for the execution of the simulation, while one core is dedicated to the management of the service overhead. To ensure the consistency, the equal number of execution tasks are assigned to a specific core of the RT processing unit. Please refer to the appendix to see the specifications of the RT hardware used in this paper.

A. HIL MODELLING PROCESS

In order to go from an initial model running in MATLAB-Simulink environment to an RT application correctly executed in SCALEXIO, several steps must be performed in the correct order. The RT system designing procedure is divided into three main parts:

- **Initial Model Partitioning:** describes how to partition the initial model into several parts in the Simulink® environment and then creates new independent models from the initial model with standardized interfaces utilizing dedicated dSPACE RT blocks.

TABLE 3. Overview of the specifications for the M1 segment EV model.

System/ Component	Specifications
E-Drive	
Number of e-machines	1
Type of e-machine	Induction motor
Rated speed	10000 rpm
Target voltage	400 V
Target power and range	75kW peak / 30kW cont.
Driven axle	Front & rear
Transmission	
Type of transmission	Fixed ratio with single stage gear unit
Battery	
Cell chemistry	NMC
Nominal Pack Voltage	373 V
Max./Min. Pack Voltage	396/250 V
Nominal Energy	134 kWh gross
Vehicle	
Vehicle load model	Vehicle mass 1600kg, rolling resistance C_0 0.009 and C_1 1.5e-6, drag coefficient 0.3, front area 2.25m^2, rotational inertia coefficient 1.21, wheel radius 0.3m, gear box efficiency 98%, inverter efficiency 97%.

- **Partitioned Model Compilation:** describes the different steps for generating the C code from the model and then compiling the applications via a dSPACE tool called "ConfigurationDesk."
- **Partitioned Model Execution:** describes briefly how to use ControlDesk for measuring the correct real-time execution of the partitioned model.

By using the dSPACE application library, it will automatically create the three new independent models with RT interfaces ready for compilation. After compilation of the Simulink model, the application is moved to the dSPACE environment and ConfigurationDesk handles the rest of the process. In ConfigurationDesk, a few more steps are performed before the simulation is sent to the RT platform. First, the machine code is flashed into the RT target memory, then the system description file of the application is loaded to the cores in the RT target; afterward, the description of the variable for each of the three models is initialized.

Finally, when the entire setup is ready, the RT test can be carried out, the subsequent considerations are as follows:

B. VEHICLE DYNAMICS MEASUREMENT

An M1 segment EV RT-measurement is used in this HiL testing. The specifications of the vehicle parameters are shown in TABLE 3 and these parameters have remained constant throughout the test.

C. CURRENT PROFILE

The current profile requested on the input side of IBC lasts 1800s. It corresponds to the different characteristics that the vehicle exhibits, including its mass, drag coefficient, rolling resistance and acceleration during the WLTP cycle.

D. BATTERY PACK VOLTAGE

Currently, the battery pack voltage level in HiL testbench consider the worst-case scenario. IBC is tested for the minimum voltage level of the M1 segment vehicle.

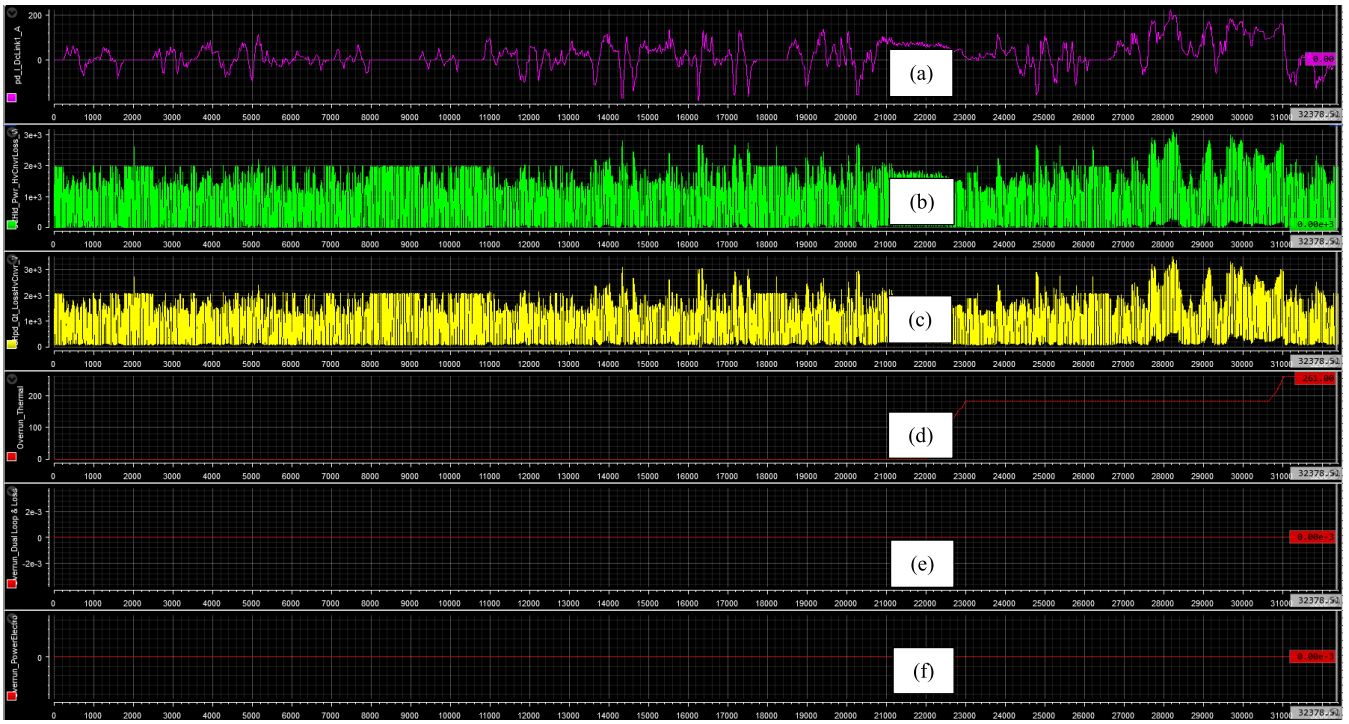


FIGURE 17. *ControlDesk panel of the HiL setup at dSPACE:* **(a) Battery current profile, (b) Total converter losses (W), (c) Semiconductor losses, (d) Overrun count in Thermal block, (e)Overrun count in controller block, (f) Overrun count in Power electronics during a complete driving cycle test.**

E. HIL RESULT ANALYSIS

For analysing the correct execution of the IBC model in the RT target with the given load, the main timing parameters to be checked are: ''Task Turnaround Time,'' which indicates the fastest execution time, and ''Overrun Count'', which depicts the number of times the RT target failed to finish execution within a specific timeframe. The test is executed directly in a multi-core configuration since the performance is slightly enhanced using this method.

The result for power demand load current for the IBC is shown in FIGURE 17(a). The total power losses of the IBC and semiconductor losses of the IBC are shown FIGURE 17(b) and (c), while the overrun in different sub-modules are also shown in FIGURE 17(d), (e) and (f). FIGURE 17 is shown RT execution and measurement using the ControlDesk panel of the dSPACE. It gives the possibility of monitoring the IBC behaviour, and task overruns count during the HiL execution.

The computation effort is quantified in TABLE 4 and TABLE 5. As can be understood from the tables that the model performance is satisfactory on a periodic task of 18μs, though some overruns occur on the execution of the thermal calculation block. However, these overruns mainly occur during model initialization and do not affect normal operation. It can be seen from FIGURE 17 that the total simulation time required for the RT platform is approximately 9 hours ($\sim$32378 s).

It is worth noting that for long homologation tests such as WLTP or NEDC (used in automotive application), simulation using a PC or laptop will be unfeasible because of the high computational time needed and are only possible using an RT testbench such as dSPACE.

TABLE 4. **RT execution compliance - overall results.**

Periodic task= 1.8e-5 s		Task turnaround time (µs)	Task overrun counter
Partition submodule	Power electronics	11.60	0
	Loss Measurement	11.23	0
	Thermal calculation	17.08	261

TABLE 5. **RT computational effort results.**

Timespan defined in Simulink (s)	RT system periodic task (s)	Execution time in SCALEXIO
1801	1.8e-5	32378

VII. MODEL SCALABILITY

There are different levels of fidelity that can be used during simulations involving models of semiconductor-based power electronics systems, which allow the users to adjust to their desired accuracy versus computation cost requirements. While highly accurate models are required to gain critical insights for some cases, during other times, faster simulation speed is desired. To account for such necessities, different scalable levels of model fidelity are designed. The detailed scalable modelling approach is shown in FIGURE 18.

A. HIGH-FIDELITY (HiFi) MODEL

A high-fidelity model is the most accurate simulation of a physical system, often at the cost of enormous

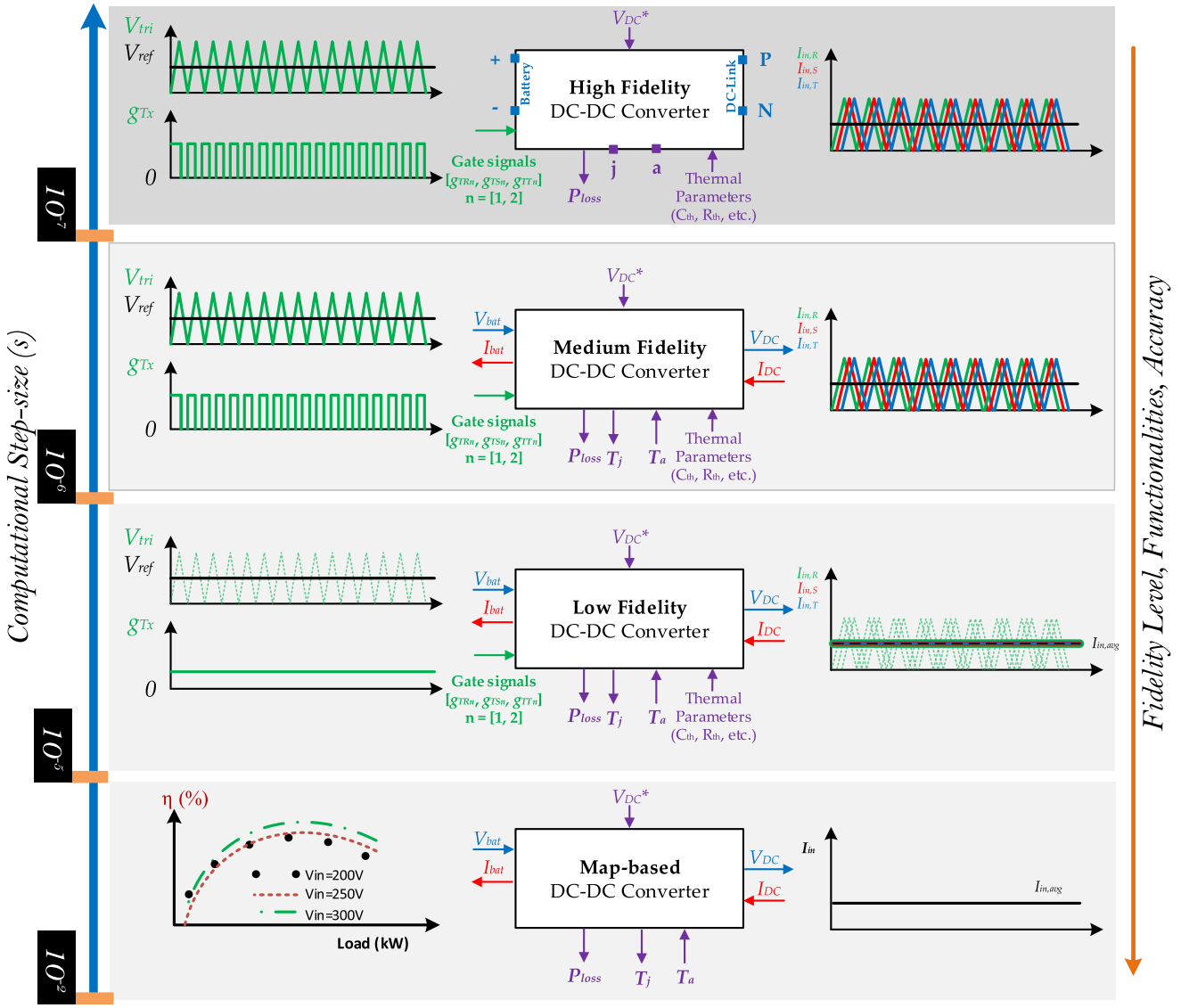


FIGURE 18. The summary of the scalable modelling approach of the HV-IBC is showing model properties as PWM generation (comparison between Vtri and Vref), gate signal *gTx*, 3-Phase interleaved current, model interface I/O, and computational step sequence capability of each model.

computing resources. It models the physical parameters, including the electrical, thermal, mechanical aspects of a system, and often is a highly specific model. For example, a HiFi model can be used to simulate the most detailed electrical phenomena, such as short circuits and other failure situations. In MATLAB/Simulink®, the HiFi models are based on the physical Simscape Multibody™ library. The disadvantage of the HiFi model is the enormous simulation time required just to simulate brief instances of the real system, for example, ∼25 hours of simulation time needed to simulate 0.1 seconds of a PE system.

B. MEDIUM-FIDELITY (MFi) MODEL

To overcome the shortcoming of the HiFi model, a minimal amount of accuracy is traded off to get computationally faster simulation using the medium-fidelity model. The MFi model replaces the physics behind a system with equations describing whichever phenomena are being investigated. Since every single physical aspect is not modelled, the simulation speed increases; this allows users to simulate long periods to detect trends, instead of mere seconds allowed by the HiFi model. In MATLAB/Simulink, the MFi models are based on the Simulink® common blocks. The MFi models provide the same input and output fidelity as a HiFi model, as shown in [6], [18].

C. LOW-FIDELITY (LoFi) MODEL

The low-fidelity model is implemented by averaging techniques, considering only the fundamental harmonic, and thus neglecting the switching behaviour of the converter, as described in [16], [18]. These modelling approaches provide essential improvements in computational cost, which could allow working in real-time (HiL platforms, embedded control systems) or faster than real-time platforms

TABLE 6. Scalability characteristics of the IBC modelling.

Description	HiFi	MFi	LoFi	Map-based
Modelling platform	Simscape Multibody™	Simulink®	Simulink®	Simulink®
Step size	1e-7	1e-6	1e-5	1e-2
Modelling Type	Physics based modelling	Equation based modelling	Average signal modelling	Map based modelling
Loss model	Instantaneous	Instantaneous	Average estimation	Map based
Thermal model	Detailed foster model and physics based heatsink model varied with specific signals as coolant flow rate and coolant temperature	Detailed foster model and second order heatsink model varied with specific signals as coolant flow rate and coolant temperature	Average estimation	Map based
Characteristics	✓ Accurate physics-based switched simulation ✓ Discrete Dual-loop lead-lag control ✓ Short-circuit simulation ✓ Used in fault monitoring ✓ High simulation time required	✓ Accurate equation-based estimation ✓ Discrete Dual-loop lead-lag control ✓ Less simulation time than HiFi ✓ Used in DfR testing	✓ Average modelling technique ✓ Faster than MFi ✓ Used in different vehicle simulation scenario	✓ Map based modelling ✓ Faster than LoFi ✓ Used in vehicle energy management optimization task

(for long-term simulations) while they keep acceptable accuracy levels. Often only the first and second-order dynamic equations are modelled, and the simulation time step is much more significant compared to MFi or HiFi model.

D. MAP-BASED MODEL

The map-based models could be other alternatives tailored to improving the computational cost. The map-based model is described in this paper comprises determining all possible operating conditions of a converter and obtaining detailed losses in each of them and generating a multi-dimensional LuT that can be easily accessed to interpolate instant losses based on immediate operating conditions.

Finally, the scalability approach in terms of modelling technique and platforms, compatibilities and characteristics are summed up in TABLE 6. Based on the specific use cases, the OEMs must benchmark the workflow and type of modelling required for the EVs applications. The detailed performance analysis and accuracy comparison of the scalable models are illustrated in section IX.

VIII. EXPERIMENTAL RESULTS

The SiC-based IBC hardware parameters are presented in TABLE 2. FIGURE 19 shows the experimental setup for the IBC performance validation. A programmable bidirectional EV battery emulator (1000V, 2 × 80kW) is used as a power supply for the IBC. Furthermore, the output is connected to a dynamic resistance-based load, which can be varied from 3 kW to 30kW. A Xilinx Kintex-7 XC7K325T, an FPGA programming board in dSPACE MicroLabBox, is utilized to implement a discrete control strategy for the inner inductor current loop and outer output voltage loop. Life energy motion (LEM) current and voltage sensors are used for measuring feedback signals. Furthermore, a FLIR thermal camera is used to monitor the thermal profile of the IBC, and a *YOKOGAWA WT1806E* power analyser is used to monitor both inputs and outputs of the IBC to determine its efficiency.

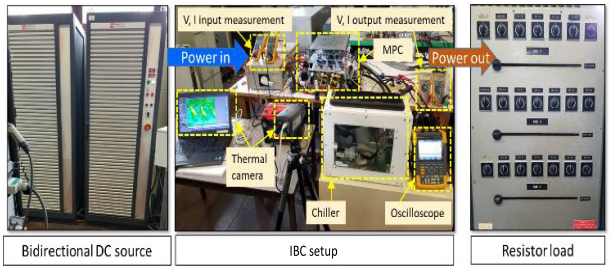


FIGURE 19. Experimental setup of the SiC-based IBC, bidirectional power is supplied by the Digatron EVT module (1000V, 2 × 80kW), liquid-cooling thermal is processed through the chiller, FLIR thermal camera is used to observe the thermal distribution and YOKOGAWA WT1806E power analyser is used to measure the IBC efficiency and variable RLoad (3kW-30kW).

In the IBC, the current controller bandwidth is designed at 3kHz, while the voltage controller bandwidth is maintained at 300 Hz. The interleaved inductor's current response of the IBC, operating in the boost mode for V_{BAT} of 200V, V_0 of 385V and load power of 27kW, is shown in FIGURE 20(a), while FIGURE 20(b) shows interleaved current response for V_o of 395V, V_{BAT} of 200V and load power of 22kW and operating at buck mode. The interleaved inductor current response of the RT system validates the susceptibility of controller design at ∼60kHz switching frequency in bidirectional mode.

The efficiency is obtained for the SiC IBC at different load variations from 10% to 100% for a V_{in} of 200V, V_o of 385V and f_{sw} of 60kHz is illustrated in FIGURE 21. The highest IBC efficiency is obtained 98.4% at 26.5kW by exploiting a *YOKOGAWA WT1806E* precision power analyser (analyser accuracy ∼0.02%).

IX. RESULTS COMPARISON AND DISCUSSIONS

A. SCALABLE MODELS COMPARISON

In order to compare the model accuracy between multi-fidelity models, an operating condition has been chosen as presented in TABLE 7. The responses between the HiFi model and the MFi are quite analogous. Hence, for detailed

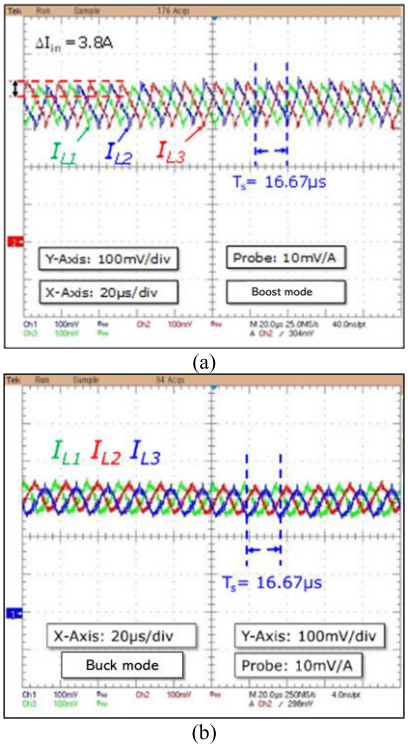


FIGURE 20. 3-Phase interleaved inductor's current response (a) boost operation mode atV_{BAT} = 200V, V_0 = 385V & load power = 27kW, (b)buck operation mode atV_o = 395V, V_{BAT} = 200V & load power = 22kW. In both modes, the switching frequency has remained 60kHz.

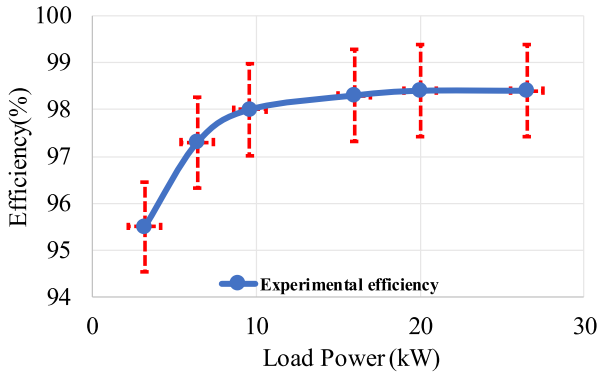


FIGURE 21. Tested IBC efficiency using YOKOGAWA WT1804E power analyser at load power from 3.5kW to 26.5kW during motor operation mode and error bar is showing 1.25% of the error limit.

comparison between the multi-fidelity models, the HiFi model response is not considered.

1) ELECTRICAL CHARACTERISTICS COMPARISON

For electrical characteristics comparison, the output load varies from 30kW to 40kW; the battery voltage changes from 250V to 325V and buck mode is tested at −30kW load condition. FIGURE 22 (a) depicts the interleaved current response and FIGURE 22 (b) illustrates the DC-link voltage response of the IBC for MFi, LoFi and map-based modelling approaches. It can be seen that the electrical characteristics between MFi, LoFi and map-based models have analogous

TABLE 7. Operating characteristics of HV DC/DC converter.

Description	Specifications
Semiconductor power module	Cree_SiC: CAS120M12Bm2 Infineon_Si: FF150R12RT4
Switching frequency	60kHz for SiC and 20kHz for Si
Target voltage	400 V
Target power	30kW
Simulation Sampling time	M-Fi: 1e-6; LoFi: 1e-5 Map-based: 1e-2

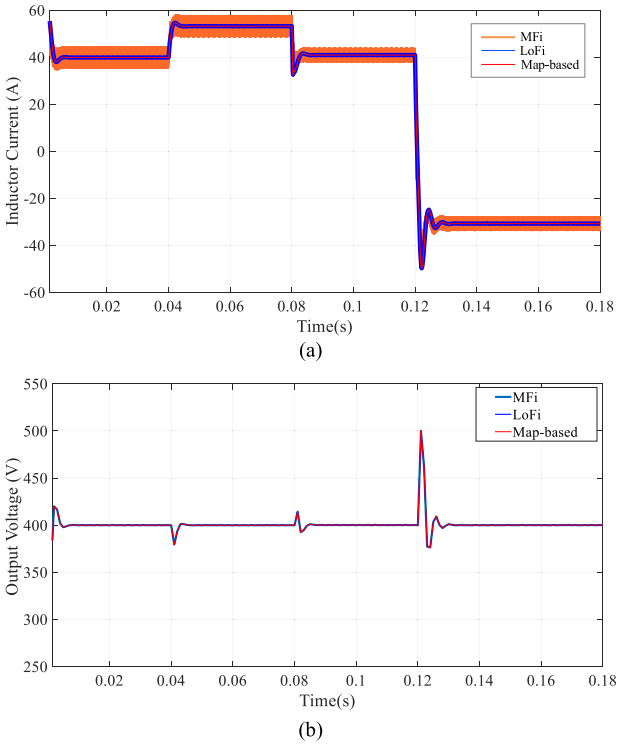


FIGURE 22. Dynamic electrical characteristics evaluation between MFi, LoFi and map-based model for load variation from 30kWto 40kW, battery voltage change from 250V to 325V and mode changes from boost to buck (40kw to −30kW): (a) Interleaved inductor current response comparison and (b) DC-link voltage response comparison.

responses during load variation, battery voltage variation and mode change operation; however, as can be seen from the plots, the LoFi and Map-based models give an average output (or filtered) of the MFi outputs, which accurately models the transients.

2) ELECTRICAL LOSSES COMPARISON

FIGURE 23 (a) depicts the switching losses comparison among the MFi and LoFi models in the steady-state condition. For a fair comparison, the average MFi waveform is plotted. It can be seen from the FIGURE 23(a) that the average MFi switching losses is coinciding with the LoFi switching losses in steady sates and the mean percentage error (MPE) between these two switching losses models is 3.25%. The MPE formula is shown in the appendix. FIGURE 23(b) depicts the switching losses comparison among the MFi and LoFi models in the transient condition. It can be seen from the FIGURE 23(b) that there is a high

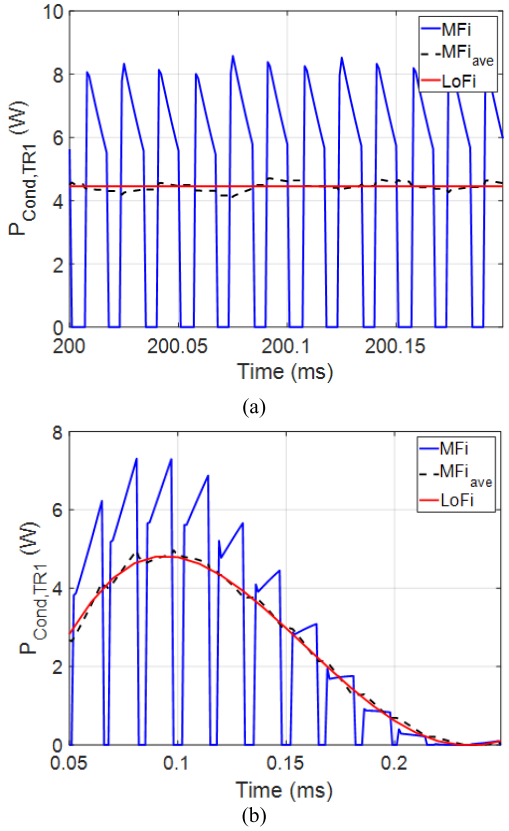


FIGURE 23. Electrical conduction losses characteristics comparison between MFi and LoFi models (a) conduction losses in steady-state condition(b) conduction losses in transient condition.

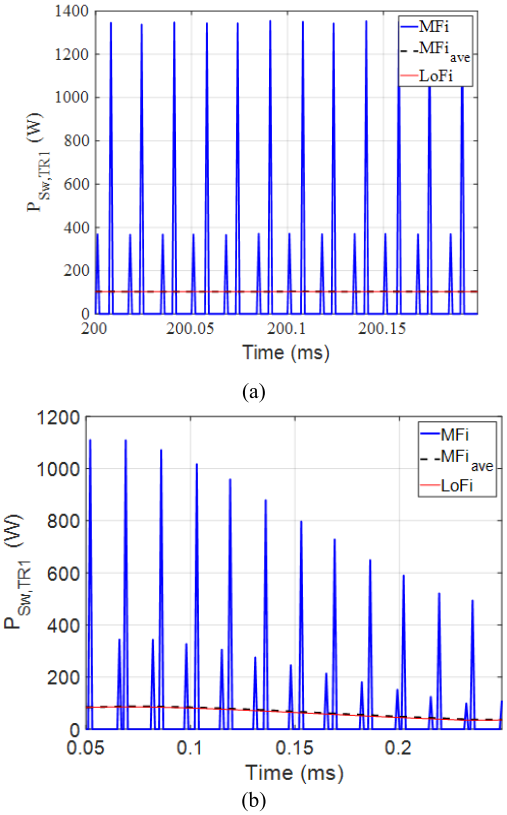


FIGURE 24. Electrical switching losses characteristics comparison between MFi and LoFi models (a) switching losses in steady-state condition(b) switching losses in transient condition.

accuracy between the average MFi switching losses and the LoFi switching losses in transient condition. It should be pointed out that the MPE between these two switching losses models is 1.25%.

FIGURE 24 (a) depicts the switching losses comparison between the MFi and LoFi models in the steady-state condition. It can be seen from the FIGURE 24 (a) that the average MFi switching losses is highly correlated to the LoFi switching losses in steady sates and the MPE between these two switching losses models is 0.15%. FIGURE 24 (b) similarly depicts a high correlation between the average MFi switching losses and the LoFi switching losses in transient and the MPE between these two switching losses models is 0.25%.

3) ACCURACY COMPARISON

The HiFi model is considered as an ideal model with 0% error. The MPE has been considered for the accuracy measurement between multi-fidelity models and calculated as percentage deviation between the HiFi model output and the output of another fidelity level. A maximum of 5% error has been found between the less accurate map-based model and HiFi model for total average power losses estimation. In contrast, there is a very high 99.75% accuracy is found between the HiFi and the MFi models' response. The highest MPE for junction temperature measurement is 0.61%, 4.65% for the average DC-link voltage response, and 2.50% for the interleaved inductors current analysis. The accuracy of the multi-fidelity modelling approaches of the IBC is illustrated in TABLE 8.

TABLE 8. Accuracy comparison of the multi-fidelity IBC simulation.

Model	Step Size (s)	Average Power Losses (W)	Junction Temperature (deg C)	Interleaved Current (A)	Average DC-link Voltage (V)
HiFi	1e-7	0%	0%	0%	0 %
MFi	1e-6	1.55%	0.55%	0.25%	0.55%
LoFi	1e-5	3.59%	0.61%	1.50%	3.49%
Map-based	1e-2	5.04%	-	2.50%	4.65%

TABLE 9. Speed of the multi-fidelity IBC simulation.

Model	Step Size	Simulation *Time(s)*	Time required in model (s)	Execution speed comparison with RT	HiL capacity
HiFi	1e-7	0.1	90720	slower	No
MFi	1e-6	1800	45000	slower	Yes
LoFi	1e-5	1800	1725	Fast	Yes
Map-based	1e-2	1800	270	Faster	Not effective

4) SPEED COMPARISON

It can be viewed from TABLE 9 that the HiFi model is considerably slower than the RT model. The HiFi simulation model requires 90720sec to simulate just 0.1sec. Moreover, the HFi model failed to run in the HiL setup. The MFi model

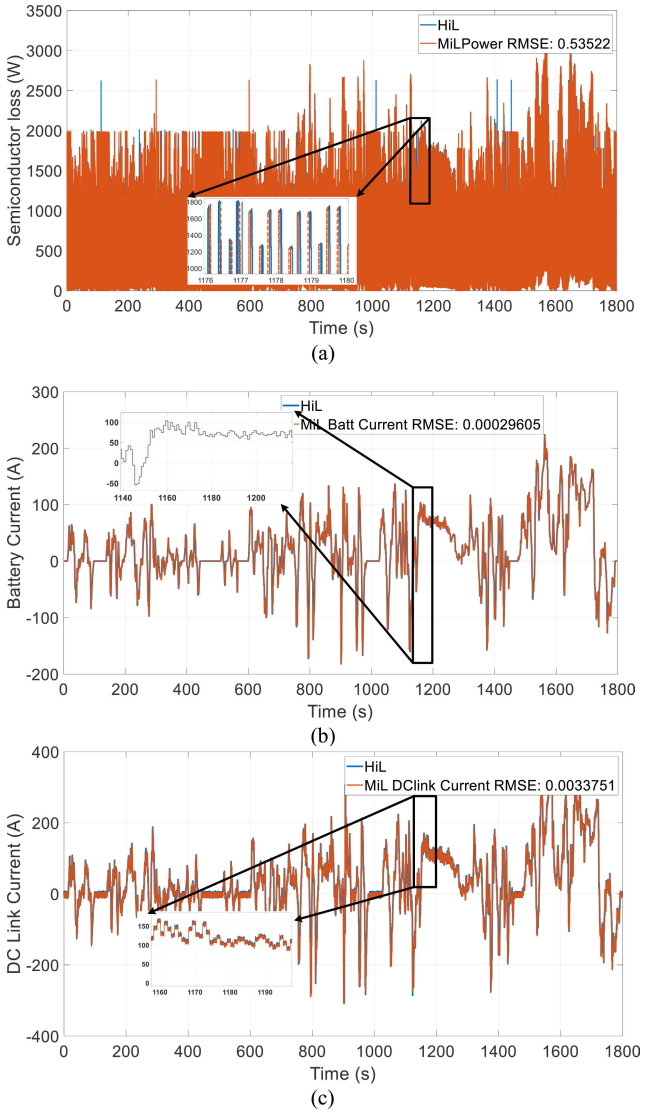


FIGURE 25. The performance validation in the HiL setup. (a) Comparisons of the IBC power losses between HiL and MiL model and RMSE is 0.54; (b) Comparisons of the IBC battery current between HiL and MiL model and RMSE is 0.0003; (c) Comparisons of the IBC DC-link current between HiL and MiL model and RMSE is 0.0034. The RMSE cost function formula is shown in the appendix.

takes 12.5h to simulate a WLTP mission profile. The MFi simulation time is slower than RT; however, the MFi model is capable of the HiL test. The MFi model has decreased simulation time by a factor of 36,288 while sacrificing minimum accuracy in return. The MFi model is compared with the HiL model and a high accuracy is obtained as mentioned in next sub-section. The LoFi model improves simulation time compared to the HiFi and the MFi models and simulates 96.5% faster than the MFi model. The simulation speed of the LoFi model is slightly faster than an RT vehicle test. The map-based model is more than six times faster than RT. Hence, the map-based model is considered for the energy management strategy (EMS) and thermal management strategy (TMS) optimization related task in the BEVs.

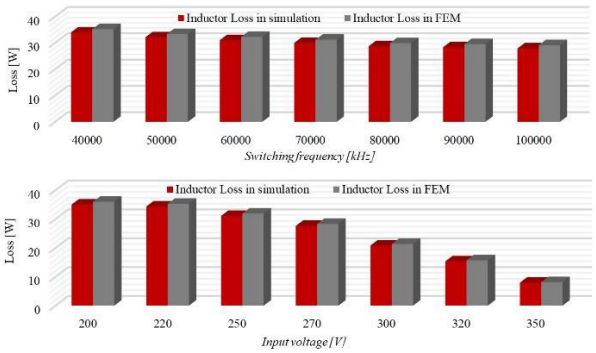


FIGURE 26. (a) Inductor loss comparison between 1D and 3D model concerning switching frequency changes from 40kHz-100kHz; (b) Inductor loss comparison between 1D and 3D model concerning input voltage variation from 200V-350V.

The simulation speed between different fidelity of models is demonstrated in TABLE 9.

B. PERFORMANCE VALIDATION IN THE HiL SETUP

To verify the HiL testbench results, MiL simulation model has been selected, which is an equation based MFi model in Simulink. The same generic base vehicle model, as depicted in TABLE 3 and real-life mission profile WLTP has been taken into consideration for the MiL simulation test. For performance validation, one lap of the IDIADA's dynamic track has been selected as a load test scenario. This dynamic track has a length of 23 km, with highly varying slopes and altitudes. For the validation of the performance between the HiL and the MiL model, a standard statistical method root-mean-square-error (RMSE) is utilized, as shown in appendix. The comparison has been evaluated for three essential characteristics of the converter, which are total power losses of the IBC, battery current (output current of the converter) and DC-link current (load power/DC-link voltage).

FIGURE 25 shows an excellent accuracy between the HiL and the MiL model performances as the highest RMSE is limited to within 0.54 for IBC power losses during the 1800 seconds of dynamic mission-profile. Since the highest RMSEis less than 1, it indicates high degree of correlation between the MiL and the HiL setup performace.

C. INDUCTOR LOSS VALIDATION IN FEM

A comparison of the inductor loss among the 1D simulation model and the 3D FEM model is depicted in FIGURE 26. A high accuracy has been achieved in the simulation loss model in comparison to FEM loss results. In case of switching frequency variation from 40kHz to 100kHz, the maximum error of around 4.3% is obtained at 100 kHz. The error is caused due to the high fringing fields near to the air gap created during high switching frequency, which is difficult to consider in analytical calculation. In case of battery voltage variation from 200V to 350V, the maximum error of around 2.7% is obtained at 200V. The error was high at the lower voltage input as high inductor current and high inductor ripple current limit the accuracy.

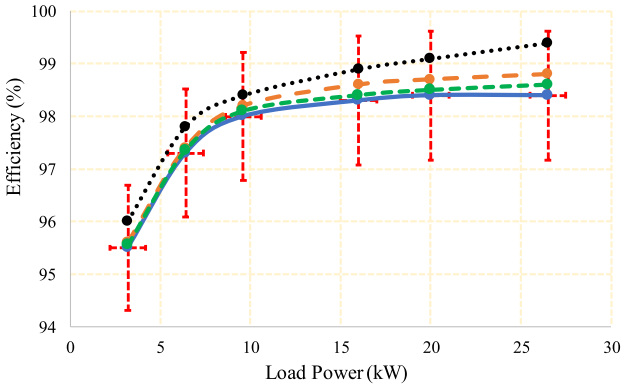


FIGURE 27. The experimental efficiency of the IBC is measured at $V_{in} = 200V$, $V_o = 385V$ and $f_{sw} = 60kHz$, while load power is varied from 3.6kW to 26.5kW. The same operating conditions are retained for measuring the IBC efficiency in HiFi, MFi and LoFi models. The solid blue line is the experimental efficiency; the dotted green line is the HiFi efficiency, the dotted orange line is the MFi efficiency and the dotted black line is the LoFi efficiency. The error bar is depicted 1.25% average percentage error.

TABLE 10. Efficiency error and drive cycle simulation capability comparison among literature study and the proposed article models.

Reference	Used Topology	Driving cycle simulation capacity	Maximum Efficiency error
[30]	3-phase IBC	No	4.19%
[31]	3-phase MPC	No	2.7%
[34]	3-phase MPC	No	8.37%
[35]	3-phase multi-functional DC/DC	Yes	2.01%
[37]	MDIBC	No	5.24%
[39]	4-phase IBC	No	4.50%
[42]	3-phase IBC	Yes	0.49%
[55]	Synchronous buck	No	3.84%
[56]	3-phase converter	Yes	4%
[57]	Synchronous buck	No	3%
[58]	3-phase Inverter	No	0.35%
Models of this article	HiFi	No	0.20%
	MFi	Yes	0.45%
	LoFi	Yes	1.11%

D. EFFICIENCY VALIDATION WITH THE PROTOTYPE

The experimental measured efficiency, as shown in FIGURE 27, is plotted with 1.25% error bar to present the measurement uncertainties. It can be seen from FIGURE 27 that the maximum MPE for efficiency estimation among multi-fidelity models is less than 1.2%. The largest MPE of 0.2% is found in the HiFi model concerning the experimental measured result, 0.45% in the MFi model, and 1.11% in the LoFi model. The maximum deviation between the simulation and experimental results is obtained at full load condition due to the PCB losses, thermal interface material (TIM) losses and sensor errors, which are not taken into consideration in the analytical models.

TABLE 10 is depicted the comparison regarding the maximum error in efficiency estimation among the multi-fidelity models developed in this paper and models mentioned in the literature. The comparison considers the maximum MPE in the efficiency estimation and the capability of a standard driving cycle simulation.

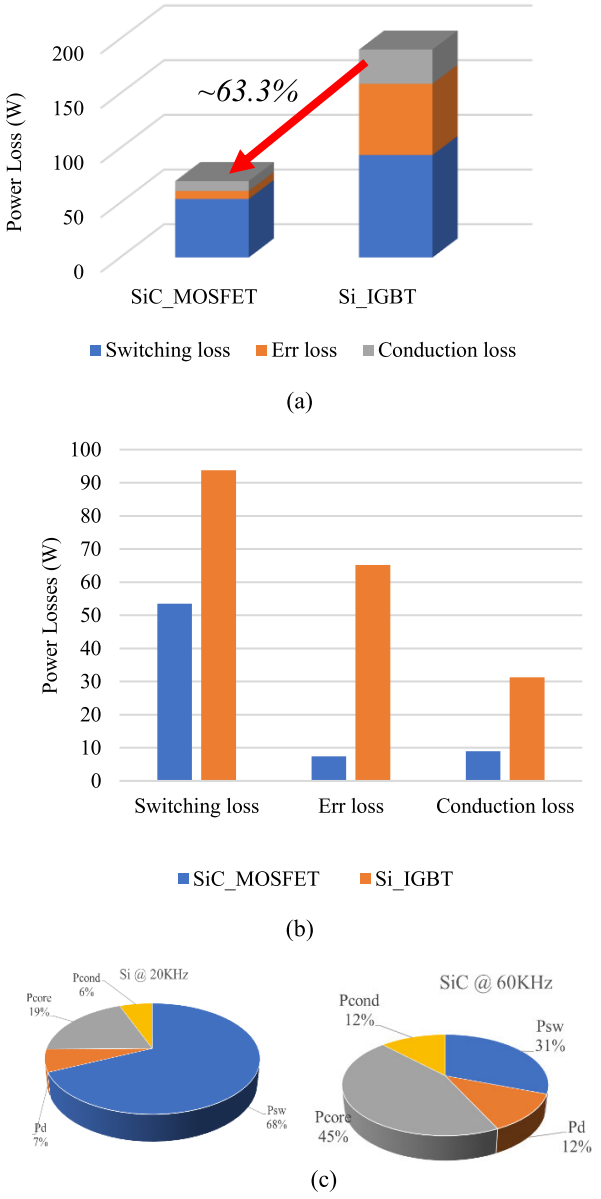


FIGURE 28. Operating conditions of the IBC: $V_{in} = 200V$, $V_o = 400V$, $P_o = 20kW$ and Si $f_{sw} = 20kHz$ and SiC $f_{sw} = 60kHz$; (a) Reduction in semiconductor losses while using SiC MOSFET, (b) Comparison of individual power losses and (c) breakdown of total losses in the IBC.

E. PERFORMANCE COMPARISON BETWEEN SiC & SI

To ensure the superiority of the WBG semiconductor switches over Si, the IBC is assessed to measure the converter losses and efficiency. The most important benefit of replacing the Si IGBT with SiC MOSFET is the reduction in the semiconductor losses around 63.3% at 20kW load, as shown in FIGURE 28 (a). The losses are calculated for Si at 20kHz frequency, whereas for SiC 60kHz frequency is used. Usually, a Si IGBT takes a long time to turn off due to its characteristic tail current, which increases turn-off losses in the IGBT module. The SiC MOSFETs have no minority carriers and thus no tail current, so their turn-off losses are significantly reduced (typically six times lower than an IGBT).

Moreover, the SiC MOSFETs significantly reduce conduction losses and have extremely low reverse recovery losses. The comparison of power losses is shown in FIGURE 28(b) and the total losses breakdown of the IBC is shown in FIGURE 28(c). It can be seen that the semiconductor losses contribution is high around 75% of total losses in case of Si-based IBC, which is reduced comprehensively around 43% of total losses in the SiC-based IBC even at the higher switching frequency. The low power losses of the SiC MOSFET could be improved the efficiency of the overall system, decreased weight, and size, reduced thermal stress and cooling. Hence, the WBG semiconductors allow the use of more-compact heat sinks and supports higher operating temperatures.

X. CONCLUSION

In this paper, a unique scalable modelling concept is presented for the high voltage interleaved bidirectional DC/DC converter to support different stages of the EVs development in a virtual world. The scalable modelling approach is depicted and validated with a full-scale hardware prototype. The maximum MPE of around 0.2% is attained between the experimental measured efficiency and the HiFi model efficiency due to load changes from 10%-100%. The highest efficiency error among hardware and scalable models is restricted to within 1.2%. Furthermore, multi-fidelity models are compared to observe the accuracy and speed between scalable models. The highest MPE is found to be 5.04% between less accurate map-based model and HiFi model in case of average power losses estimation. The highest 99.75% accuracy is achieved between the HiFi and the MFi model's responses. The error in the efficiency estimation among literature studies and the proposed multi-fidelity models is used to verify the accuracy of the proposed methods. In addition, the maximum error between the 3D FEM model and the simulation model of inductor losses is found to be around 4.3% at a high switching frequency. These excellent results between multi-fidelity models ensure the acceptance of the scalable modelling approach for PE converters modelling in EV applications.

A HiL test is executed at a very low latency of 18μs and a high degree of correlation is achieved between the MiL and the HiL model for output characteristic and the highest RMSE between these two models is limited to within 0.54 over an entire driving cycle.

Furthermore, from the performance comparison between SiC and Si, it can be concluded that the IBC could gain substantial improvement in cost, power density and weight while using the SiC MOSFET power modules. Hence, WBG-based IBC can contribute in enhancing the range of EVs.

Finally, the WBG-based optimized IBC prototype has attained the high efficiency of 98.4% at rated load condition during traction mode operation, which could be considered as a significant efficiency improvement.

From these remarkable results, it can be concluded that the scalable modelling approach would be a valuable asset to the EV industry, as scalable models can be rapidly deployed to multi-objective targets, including EMS and TMS optimization, reliability testing, short-circuit fault testing and predictive health maintenance. The requirements dictate whether execution time or accuracy is required to be modelled; but regardless of the selected models, the simulation results are guaranteed to produce deviations within 5%, thereby adding credence to the output. It will be useful for non-PE users of the EV industry to optimize the EV's modelling steps so that the proper selection criteria can be developed in choosing model with the appropriate level of execution speed versus complexity and accuracy.

APPENDIX

The main characteristics of the RT platform are listed below:

- Number of cores: 4
- Model: SCALEXIO Real-Time PC
- Processor: Intel Core XEON E3-1275v3 processor at 3,5 GHz
- RAM: 4GB
- Communication: Port Gigabit Ethernet LAN.

Statistical indices:

$$RMSE = \sqrt{\frac{\sum_{i=1}^{n} (HiL\ data_i - MiL\ data_i)^2}{n}} \quad (25)$$

$$MPE = \frac{abs(HiFi\ data - MFi\ data)}{MFi\ data} \times 100\% \quad (26)$$

ACKNOWLEDGMENT

The authors acknowledge all the project partners involved in the HiFi-Elements project. The authors also acknowledge Flanders Make for the support to our research group.

REFERENCES

[1] *State of the Climate:Global Climate Report for June 2019*, NOAA National Centers for Environmental Information, Asheville, NC, USA, Jan. 2020.
[2] I. Wagner, *Electric vehicles—Global market size 2017 & 2025*. Pune, India: Market Research Future, 2019.
[3] E. Commission, "A European strategy for low-emission mobility," in *Proc. SWD Final*, 2016, p. 13.
[4] G. H. Broadbent, G. Metternicht, and D. Drozdzewski, "An analysis of consumer incentives in support of electric vehicle uptake?: An Australian case study," *World Electr. Veh. J.*, vol. 10, no. 11, pp. 1–15, 2019.
[5] M. Singer, *Consumer Views on Plug-in Electric Vehicles—National Benchmark Report Consumer Views on Plug-in Electric Vehicles—National Benchmark Report*. Golden, CO, USA: National Renewable Energy Laboratory, Dec. 2016.
[6] C. Granrath, M. Meyer, J. Andert, and J. Richenhagen, "Methodology for the developement of a standardized virtual validation environment for electric vehicles," in *Proc. Antriebstechnisches Kolloquium, Conf.*, 2019, pp. 85–98.
[7] M. Krammer, M. Benedikt, N. Amringer, S. Materne, and R. Ruvalcaba, "The distributed co-simulation protocol for the integration of real-time systems and simulation environments," in *Proc. 50th Comput. Simulation Conf. (Summer Sim). Soc. Comput. Simulation Int.*, San Diego, CA, USA, vol. 1, Jul. 2018, pp. 1–14.
[8] J. Andert, F. Xia, S. Klein, D. Guse, R. Savelsberg, R. Tharmakulasingam, M. Thewes, and J. Scharf, "Road-to-rig-to-desktop: Virtual development using real-time engine modelling and powertrain co-simulation," *Int. J. Engine Res.*, vol. 20, no. 7, pp. 686–695, Sep. 2019.
[9] H. Winner, K. Lemmer, T. Form, and J. Mazzega, "PEGASUS-first steps for the safe introduction of automated driving," in *Road Vehicle Automation*, G. Meyer and B. Sven, Eds., 1st ed. New York, NY, USA: Springer, 2019, pp. 185–195.

[10] P. Nyberg, E. Frisk, and L. Nielsen, "Driving cycle equivalence and transformation," *IEEE Trans. Veh. Technol.*, vol. 66, no. 3, pp. 1963–1974, Mar. 2017.

[11] M. Brüll, A. Ayad, A. Greif, S. Rogge, and M. Töns, "Lifetime analysis of electronics and power electronic components in electric vehicles," in *Proc. 32nd Electr. Vehicle Symp. (EVS)*, vol. 2019, pp. 1–12.

[12] C. Sintamarean, F. Blaabjerg, and H. Wang, "A novel electro-thermal model for wide bandgap semiconductor based devices," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, Sep. 2013, pp. 1–10.

[13] J. J. Rodriguez, Z. Parrilla, M. Velez-Reyes, A. Hefner, D. Berning, J. Reichl, and J. Lai, "Thermal component models for electro thermal analysis of multichip power modules," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 37th IAS Annu. Meeting*, Oct. 2002, pp. 234–241.

[14] Ž. Jakopovic, V. Šunde, and Z. Benčić, "Electro-thermal modelling and simulation of a power-MOSFET," *Automatika, Casopis Za Automatiku, Mjerenje, Elektroniku, Racunarstvo I Komunikacije*, vol. 42, nos. 1–2, pp. 71–77, 2001.

[15] D.-D. Tran, S. Chakraborty, A. V. Melckebeke, N.-T. Vu, Y. Lan, M. E. Baghdadi, and O. Hegazy, "Multi-fidelity electro-thermal optimization of multiport converter employing SiC MOSFET and indirect liquid cooling," in *Proc. 14th Int. Conf. Ecol. Vehicles Renew. Energies (EVER)*, May 2019, pp. 1–7.

[16] J. Urkizu, M. Mazuela, A. Alacano, I. Aizpuru, S. Chakraborty, O. Hegazy, M. Vetten, and R. Klink, "Electric vehicle inverter electro-thermal models oriented to simulation speed and accuracy multi-objective targets," *Energies*, vol. 12, no. 19, p. 3608, Sep. 2019.

[17] M. Benedikt and A. Hofer, "Guidelines for the application of a coupling method for non-iterative co-simulation," in *Proc. 8th EUROSIM Congr. Modeling Simulation*, Sep. 2013, pp. 244–249.

[18] C. Granrath and I. J. Andert, "HiFi-ELEMENTS: An interface model standard and workflow for high fidelity electric vehicle modelling and testing," in *Proc. 8th Transp. Res. Arena TRA*, 2020, pp. 1–16.

[19] C. Dufour, S. Cense, and J. Belanger, "FPGA-based switched reluctance motor drive and DC-DC converter models for high-bandwidth HIL real-time simulator," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, Sep. 2013, pp. 1–8.

[20] S. Ciceo, Y. Mollet, M. Sarrazin, J. Gyselinck, H. Van der Auweraer, and C. Martis, "Model-based design and testing for electric vehicle driveability analysis," in *Proc. IEEE 16th Int. Conf. Environ. Electr. Eng. (EEEIC)*, Jun. 2016, pp. 1–4.

[21] C. Dufour, C. Andrade, and J. Bélanger, "Real-time simulation technologies in education: A link to modern engineering methods and practices," in *Proc. Intertech*, Mar. 2010, pp. 7–10.

[22] P. Jain, J. Poon, J. P. Singh, C. Spanos, S. R. Sanders, and S. K. Panda, "A digital twin approach for fault diagnosis in distributed photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 940–956, Jan. 2020.

[23] M. Biglarbegian, M. Baharani, N. Kim, H. Tabkhi, and B. Parkhideh, "Scalable reliability monitoring of GaN power converter through recurrent neural networks," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2018, pp. 7271–7277.

[24] C. C. Chan, "The state of the art of electric, hybrid, and fuel cell vehicles," *Proc. IEEE*, vol. 95, no. 4, pp. 704–718, Apr. 2007.

[25] A. Khaligh and Z. Li, "Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: State of the art," *IEEE Trans. Veh. Technol.*, vol. 59, no. 6, pp. 2806–2814, Jul. 2010.

[26] S. Chakraborty, H.-N. Vu, M. M. Hasan, D.-D. Tran, M. E. Baghdadi, and O. Hegazy, "DC–DC converter topologies for electric vehicles, plug-in hybrid electric vehicles and fast charging stations: State of the art and future trends," *Energies*, vol. 12, no. 8, p. 1569, Apr. 2019.

[27] M. Al Sakka, J. Van Mierlo, and H. Gualous, "DC/DC converters for electric vehicles, electric vehicles," in *Proc. Electr. Veh. Modeling Simulations*, 2011, pp. 309–332.

[28] S.-H. Park, S.-R. Park, J.-S. Yu, Y.-C. Jung, and C.-Y. Won, "Analysis and design of a soft-switching boost converter with an HI-bridge auxiliary resonant circuit," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2142–2149, Aug. 2010.

[29] O. Ellabban, J. Van Mierlo, and P. Lataire, "Experimental study of the shoot-through boost control methods for the Z-Source inverter," *EPE J.*, vol. 21, no. 2, pp. 18–29, Jun. 2011.

[30] O. Hegazy, J. V. Mierlo, and P. Lataire, "Analysis, modeling, and implementation of a multidevice interleaved DC/DC converter for fuel cell hybrid electric vehicles," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4445–4458, Nov. 2012.

[31] D. Tran, S. Chakraborty, Y. Lan, J. Van Mierlo, and O. Hegazy, "Optimized multiport DC/DC converter for vehicle drivetrains: Topology and design optimization," *Appl. Sci.*, vol. 8, no. 8, p. 1351, Aug. 2018.

[32] S. Chakraborty, Y. Lan, I. Aizpuru, M. Mazuela, A. Alacano, and O. Hegazy, "Scalable and accurate modelling of a WBG-based bidirectional DC/DC converter for electric drivetrains," in *Proc. 32nd Electr. Vehicle Symp. (EVS)*, May 2019, pp. 1–11.

[33] X. Chen, A. A. Pise, and I. Batarseh, "Magnetic optimizations for high-power density bidirectional cascaded-buck-boost converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2019, pp. 1444–1451.

[34] E. Nazeraj, O. Hegazy, and J. Van Mierlo, "Modeling and control of interleaved DC/DC boost converters via energy factor approach," in *Proc. 12th Int. Conf. Ecol. Vehicles Renew. Energies (EVER)*, Apr. 2017, pp. 1–8.

[35] L. Pan and C. Zhang, "An integrated multifunctional bidirectional AC/DC and DC/DC converter for electric vehicles applications," *Energies*, vol. 9, no. 7, p. 493, Jun. 2016.

[36] T. Kitamura, M. Yamada, S. Harada, and M. Koyama, "Development of high-power density interleaved DC/DC converter with SiC devices," *Electr. Eng. Jpn.*, vol. 196, no. 3, pp. 22–29, Aug. 2016.

[37] O. Hegazy, R. Barrero, J. Van Mierlo, P. Lataire, N. Omar, and T. Coosemans, "An advanced power electronics interface for electric vehicles applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5508–5521, Dec. 2013.

[38] M. S. Priya and R. Balasubramanian, "Analysis of multidevice interleaved boost converter for high power applications," in *Proc. Int. Conf. Circuits, Power Comput. Technol. [ICCPCT]*, Mar. 2014, pp. 320–327.

[39] Y. Ayoubi, M. Elsied, A. Oukaour, H. Chaoui, Y. Slamani, and H. Gualous, "Four-phase interleaved DC/DC boost converter interfaces for supercapacitors in electric vehicle application based onadvanced sliding mode control design," *Electr. Power Syst. Res.*, vol. 134, pp. 186–196, May 2016.

[40] S. Somkun, C. Sirisamphanwong, and S. Sukchai, "A DSP-based interleaved boost DC–DC converter for fuel cell applications," *Int. J. Hydrogen Energy*, vol. 40, no. 19, pp. 6391–6404, May 2015.

[41] K. Etzold, R. Scheer, T. Fahrbach, S. Zhou, R. Goldbeck, D. Guse, F. Frie, D. U. Sauer, R. W. De Doncker, and J. Andert, "Hardware-in-the-loop testing of electric traction drives with an efficiency optimized DC–DC converter control," SAE Tech. Paper 2020-01–0462, 2020.

[42] P. Azer, R. Rodriguez, J. Guo, J. Gareau, J. Bauman, H. Ge, B. Bilgin, and A. Emadi, "Time-efficient integrated electrothermal model for a 60-kW three-phase bidirectional synchronous DC–DC converter," *IEEE Trans. Ind. Appl.*, vol. 56, no. 1, pp. 654–668, Jan. 2020.

[43] D. P. Urciuoli and C. W. Tipton, "Development of a 90 kW bi-directional DC-DC converter for power dense applications," in *Proc. 21st Annu. IEEE Appl. Power Electron. Conf. Expo. APEC*, Mar. 2006, pp. 1375–1378.

[44] S. Chakraborty, S. Goel, I. Aizpuru, M. Mazuela, R. Klink, and O. Hegazy, "High-fidelity liquid-cooling thermal modeling of a WBG-based bidirectional DC-DC converter for electric drivetrains," in *Proc. 21st Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Sep. 2019, pp. 1–8.

[45] S. Hazra, A. De, L. Cheng, J. Palmour, M. Schupbach, B. Hull, S. Allen, and S. Bhattacharya, "High switching performance of 1700 V, 50A SiC power MOSFET over Si IGBT/BiMOSFET for advanced power conversion applications," *IEEE Trans. Power Electron.*, vol. 3, no. 1, pp. 4742–4754, Jul. 2016.

[46] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan, "A fast and elitist multiobjective genetic algorithm: NSGA-II," *IEEE Trans. Evol. Comput.*, vol. 6, no. 2, pp. 182–197, Apr. 2002.

[47] D. W. Corne and J. D. Knowles, "Techniques for highly multiobjective optimisation: Some nondominated points are better than others," in *Proc. 9th Annu. Conf. Genetic Evol. Comput. GECCO*, 2007, pp. 773–780.

[48] B. Williams, *Power Electronics: Devices, Drivers, Applications, and Passive Components*, 2nd ed. New York, NY, USA: McGraw-Hill, 1992.

[49] M. Witold, R. Bartosz, and S. Zbigniew, "Switching losses in three-phase voltage source inverters," *Czas. Tech.*, vol. 112, no. 2, pp. 47–60, 2015.

[50] J. Pou, D. Osorno, J. Zaragoza, C. Jaen, and S. Ceballos, "Power losses calculation methodology to evaluate inverter efficiency in electrical vehicles," in *Proc. 7th Int. Conf. Workshop Compat. Power Electron. (CPE)*, Jun. 2011, pp. 404–409.

[51] S. Munk-Nielsen, L. N. Tutelea, and U. Jaeger, "Simulation with ideal switch models combined with measured loss data provides a good estimate of power loss," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 21th IAS Annu. Meeting World Conf. Ind. Appl. Electr. Energy*, Nov. 2014, pp. 139–143.
[52] S. S. Sundar Ram and A. Vijayakumari, "Thermal modeling of wide bandgap semiconductor devices for high frequency power converters," *IOP Conf. Ser. Mater. Sci. Eng.*, vol. 310, no. 1, 2018, Art. no. 012133.
[53] S. T. Cha, Q. Wu, A. H. Nielsen, J. Østergaard, and I. K. Park, "Real-time Hardware-In-The-Loop (HIL) testing for power electronics controllers," in *Proc. Asia–Pacific Power Energy Eng. Conf.*, Mar. 2012, pp. 1–6.
[54] W. Paper, "HIL testing for power electronics Systems—National instruments HIL testing for power electronics systems—National instruments," *HIL Test. Power Electron. Syst. Natl. Instrum.*, pp. 1–8, Jun. 2020. [Online]. Available: https://www.ni.com/en-us/innovations/white-papers/12/hil-testing-for-power-electronics-systems.html
[55] S. Chakraborty, M. M. Hasan, I. Worighi, O. Hegazy, and M. A. Razzak, "Performance evaluation of a PID-controlled synchronous buck converter based battery charging controller for solar-powered lighting system in a fishing trawler," *Energies*, vol. 11, no. 10, p. 2722, Oct. 2018.
[56] C. H. van der Broeck, L. A. Ruppert, and R. W. De Doncker, "Spatial electro-thermal modeling and simulation of power electronic modules," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Sep. 2016, pp. 1–8.
[57] W. Lee, D. Han, D. Bobba, and B. Sarlioglu, "Design of single-turn air-core integrated planar inductor for improved thermal performance of GaN HEMT-based synchronous buck converter," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1543–1552, Mar. 2020.
[58] S. Yin, Y. Liu, Y. Liu, K. J. Tseng, J. Pou, and R. Simanjorang, "Comparison of SiC voltage source inverters using synchronous rectification and freewheeling diode," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1051–1061, Feb. 2018.

SAJIB CHAKRABORTY (Member, IEEE) was born in Chittagong, Bangladesh. He received the B.Sc. and M.Sc. degrees (Hons.) in electrical and electronic engineering from Independent University, Bangladesh, in 2013 and 2016, respectively.

He was a Lecturer with Independent University, from 2017 to 2018. He is currently a Ph.D. Researcher with the Power Electronics and Electrical Machines (PEEM) Division, MOBI Research Group, Vrije Universiteit Brussel. His research interests include accurate modeling of power electronics converters, physics of failure-based reliability analysis of the EVs converters, digital twin architecture design of the EVs PE converter, EV modeling, and renewable energy technology. He is a Young Professional Member of the IEEE PELS.

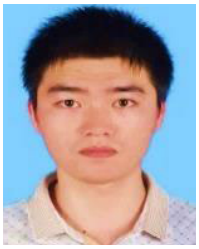
MIKEL MAZUELA (Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from Mondragon Unibertsitatea, Spain, in 2007, 2010, and 2015, respectively.

He joined Ingeteam Power Technology, in September 2015, where he was a Research and Development Engineer with the Industrial and Marine Drives Business Unit. He joined the Electronics Department, Mondragon Unibertsitatea, in 2016, where he is currently a Researcher and a Lecturer. His main research interests include modeling, modulation and control of power converters, multilevel topologies, and advanced modulation techniques.

DAI-DUONG TRAN (Student Member, IEEE) received the B.Sc. degree in electrical engineering from the Hanoi University of Science and Technology, Vietnam, in 2011, and the M.Sc. degree in electrical engineering from Soongsil University, South Korea, in 2016. He is currently pursuing the Ph.D. degree with the Power Electronics and Electrical Machines (PEEM) Division, MOBI Research Group, Vrije Universiteit Brussel, Brussels, Belgium.

He was a Principal Hardware Researcher with the Viettel Research and Development Institute, Hanoi, Vietnam, from 2012 to 2014. His research interests include integrated energy management strategies for (hybrid) electric vehicles (EVs), high-efficiency on-board battery chargers, and power electronics interface for the powertrain system of EVs.

JAVIER A. COREA-ARAUJO was born in San Salvador, El Salvador, in 1984. He received the degree in electrical engineering from the Universidad de Sonsonate, El Salvador, and the M.S. and Ph.D. degrees from Universitat Rovira i Virgili, Spain, in 2010 and 2015, respectively. He was a Researcher with the Universitat Politècnica de Catalunya, Spain, from 2015 to 2018, working on transient analysis of electrical machines and power electronics applications for HVDC systems. He is currently a Research and Development Engineer with Applus IDIADA. His current research interests include power electronics for automotive applications, e-motor drives, and optimal powertrain layouts.



YUANFENG LAN received the B.Sc. degree in engineering from the University of Science and Technology Beijing, and the M.Sc. degree in engineering from Beijing Jiaotong University, China, in 2014 and 2016, respectively. He is currently pursuing the Ph.D. degree with the Power Electronics and Electrical Machines (PEEM) Team, MOBI Research Group, Vrije Universiteit Brussel.

His main research interests include design of switched reluctance machine (SRM), control of SRM, and acoustic analysis of SRM.

ARGIÑE ALACANO LOITI (Member, IEEE) received the B.Sc. degree in industrial electronics engineering, the M.Sc. degree in energy and power electronics, and the Ph.D. degree in electric energy from Mondragon Unibertsitatea, Spain, in 2011, 2013 and 2017, respectively.

Since 2017, she has been a Lecturer with Mondragon Unibertsitatea. Her main research interests include renewable energies, power electronic converters, power transmission and distribution, and energy storage systems.

PATRICE GARMIER was born in Roanne, France, in 1979. He received the degree in electronic from the Université de Saint Etienne. He was with PSA in integration and validation of electronic systems at vehicle level, for a period of seven years. He is currently an Electronic Engineer in HiL bench and real-time systems with Applus IDIADA.

IOSU AIZPURU (Associate Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from Mondragon Unibertsitatea, Spain, in 2006, 2009, and 2015, respectively.

He is currently a Researcher and a Lecturer with the Department of Electronics, Faculty of Engineering, Mondragon Unibertsitatea. He has participated in various research projects in the fields of traction and stationary systems for railway applications, renewable energy applications, energy storage applications for traction, and on-grid and off grip systems. His current research interests include power electronics modeling, energy storage modeling, and control of energy storage systems via power electronic converters.

OMAR HEGAZY (Member, IEEE) received the Ph.D. degree from the Department of Electrical Machines and Energy Technology (ETEC), Vrije Universiteit Brussel (VUB), Belgium. He is currently the Head of the Power Electronics and Electrical Machines (PEEM) Division [Power Electronics Innovation Laboratory (PEIL) and Powertrain Innovation Laboratory (PIL)], ETEC Department, and the MOBI Research Centre, where he coordinates the research activities in this field in several national projects, such as VLAIO (ex. IWT), innoviris, Flux50, and so on., and European projects, such as SAFEDRIVE, UNPLUGGED, ELIPTIC, ORCA, ASSURED, HiFi-Elements, GHOST, HiPERFORM, ACHILES, LONGRUN, eCharge4drivers, and so on. He is the author of more than 120 scientific publications. He is a member of EPE and IEC standards. His research interests include power electronics, electrical machines, electric and (plug-in) hybrid electric vehicles, digital twins, charging infrastructure, power/energy management strategies, battery management systems (BMS), V2x systems, optimization techniques, and smart DC grid with renewable energy.