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Performance Improvement of a Silicon Partial Power Converter over a Silicon Carbide Full Power Converter

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***Abstract*—This article studies the new benefits that partial power processing brings to Silicon (Si) devices compared to wide-bandgap technologies. To prove this, the proposed case study consists of an on-board charger (OBC) application in which a Si-based partial power converter (PPC) is compared with a Silicon Carbide (SiC) based full power converter (FPC). The OBC application considers three different technologies of lithium-ion batteries and the main comparison metrics are: semiconductor switching, temperature rise of semiconductors, volume and device losses (efficiency). This last one is oriented to energy losses (Wh) and not to power losses (W) as classical design. An analytical model is used to compute switching and conduction losses. Depending on the operating point, switching events are segregated into zero voltage switching (ZVS), incomplete ZVS and hard switching. It is shown that the Si-based PPC may enter non-ZVS in certain operating conditions. However, its efficiency remains above 99 %, producing up to 5 times lower energy losses than the SiC-based FPC. Also, the case temperature of the semiconductors is halved and a reduction in the volume and electrical stress of the devices is achieved. This permits a global multi-objective optimization. The results are experimentally validated using a 3 kW prototype of SiC-based FPC and Si-based PPC.**

***Index Terms*— Silicon (Si), wide-bandgap (WBG), silicon carbide (SiC), partial power processing (PPP), partial power converter (PPC), series connected converter, dual active bridge (DAB)**

I. Introduction

Improved energy efficiency and smaller power converter size are the principal advantages that wide-bandgap (WBG) devices offer as compared to traditional Silicon (Si) based semiconductors [1], [2]. In addition, these WBG technologies give devices the ability to work at much higher frequencies (typical application of Gallium Nitride, GaN) and higher voltages/temperatures (typical application of Silicon Carbide, SiC) than the conventional Si semiconductors [3]. In consequence, solar, traction, and electric vehicles (EV) applications are implementing WBG-based devices on their power converters [4]. On the other hand, the Si technology is considered as a very mature technology, and so it still dominates the market of power devices due to its reduced cost and ruggedness. However, when it comes to power density and switching capability, the performance of Si devices has reached its theoretical limitations [5].

Latest literature on power converter architectures describes partial power processing (PPP) based strategies as promising topologies regarding power converter's footprint reduction and system efficiency improvement [6], [7]. This is achieved by decreasing the power processed by the converter (P_{in} or P_{out}). To explain this, Fig. 1 compares the power flow between a full power processing (FPP) solution and a PPP one. On the one hand, a FPP converter (Fig. 1a) processes 100 % of the power flowing from the source to the load. On the other hand, a PPP (Fig. 1b) converter only processes a fraction of the source power. According to [8], PPP strategies for DC-DC applications are classified into three different groups: differential power converters (DPC), partial power converters (PPC), and mixed strategies. DPCs are aimed to control the individual current of elements connected in series to a common voltage bus [9], [10]. PPCs are designed to control the power flow between a source and a load that have a different voltage and current level [11]–[14]. Finally, the mixed strategies group gathers different solutions that present improved performance than DPCs and PPCs at specific conditions.

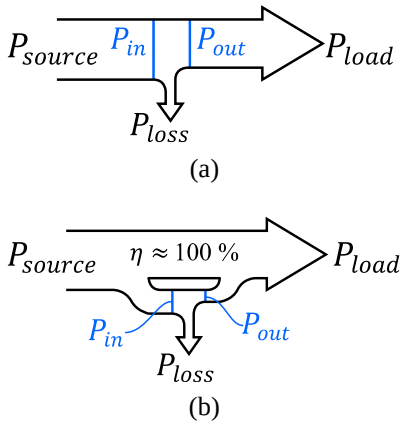

Fig. 1. Power flow diagram. (a) FPP. (b) PPP.

Due to its numerous applications, the present document focuses on PPC architectures. Latest researches on PPCs have achieved lower size and higher efficient solutions than FPP architectures. First, authors in [11] demonstrate certain isolated topologies (for example, phase-shifted full-bridge) can achieve PPP if they are implemented in PPC architectures. Second, [12] concludes that a dual active bridge (DAB) topology implemented on a PPC architectures also achieves PPP. Apart from that, a reduced electrical stress and efficiency improvement compared to its FPP architecture is observed. Due to the reduced converter power and lower voltage/current stress,

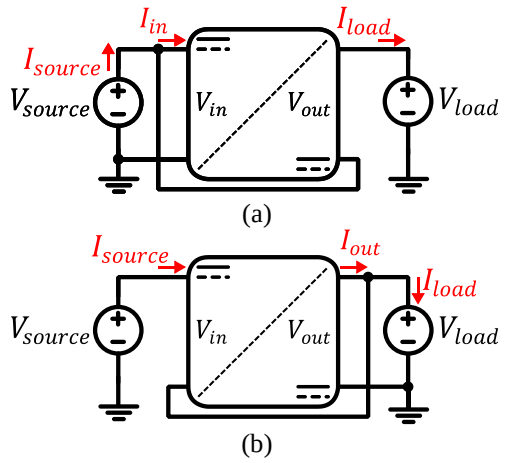

Fig. 2. Connection of PPCs. (a) IPOS. (b) ISOP.

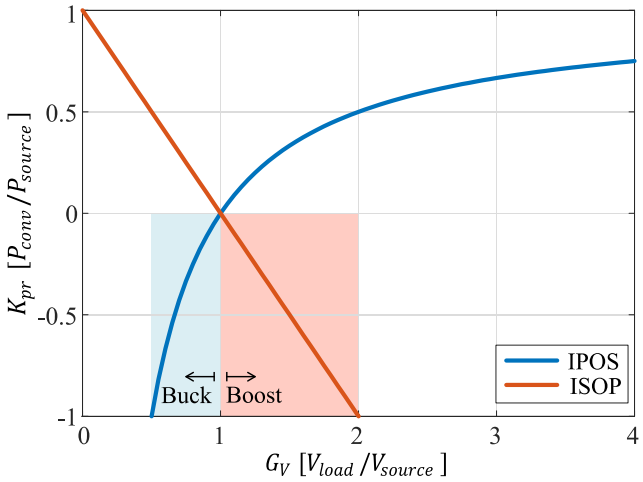

Fig. 3. K_{pr} curves of IPOS and ISOP architectures. System efficiency is considered as ideal (η=1).

conventional Si-based devices can compete with upcoming SiC-based devices. Si-based technology is very mature, and its market offers a wide and highly competitive semiconductor variety. Therefore, if these advantages of Si-based devices are combined with the benefits of PPP, then a Si-based PPP solution may provide better a performance than a WBG-based FPP solution. This paper aims to (i) demonstrate the enhanced performance of Si-based PPCs than SiC-based FPCs and (ii) show the benefits that PPP can offer to the life extension of Si-based devices. The application under analysis consists of the DC-DC stage of an on-board charger (OBC), which is already considered for implementation of WBG technology [15]–[18].

The organization of this paper is as follows. Section II describes the connection and functioning of PPC architectures. Section III presents the OBC application and the battery technologies selected for the analysis. Section IV describes the analytical model to compute the power losses, the hard-soft switching regions boundaries and the control strategy of the power converter. Section V presents simulation and experimental results. In Section VI, the main results and improvements are discussed and, finally, Section VII summarizes the main conclusions.

II. PPC ARCHITECTURES DESCRIPTION

Fig. 2 shows two main architectures of PPC. These are the Input-Parallel-Output-Series (IPOS, Fig. 2a) and the Input-Series-Output-Parallel (ISOP, Fig. 2b). Depending on the working conditions, each architecture presents a different reduction of the converter power (P_{conv}). This is compared by computing the partial power ratio (K_{pr}), which consists of the ratio of the converter power to the system power (1). Applying Kirchhoff's laws, K_{pr} curves of both architectures are obtained as a function of the static voltage gain (G_V) and are defined in (2)-(4) [8].

$$K_{pr} = \frac{P_{conv}}{P_{source}} \tag{1}$$

$$K_{pr_{IPOS}} = 1 - \frac{\eta}{G_V} \tag{2}$$

$$K_{pr_{ISOP}} = 1 - G_V \tag{3}$$

$$G_V = \frac{V_{load}}{V_{source}} \tag{4}$$

Where $K_{pr_{IPOS}}$ and $K_{pr_{ISOP}}$ are the processed power ratios of the IPOS and ISOP architectures. η is the efficiency of the system, which is given in (5). Fig. 3 shows the resulting curves.

$$\eta = \frac{V_{load} \cdot I_{load}}{V_{source} \cdot I_{source}} \tag{5}$$

From Fig. 3, many important conclusions can be obtained. First, it is concluded that as G_V approaches 1, K_{pr} reduces for both IPOS and ISOP architectures. This means that the smaller the difference between the source and load voltage, the less power the converter will process (main objective of PPCs). This can be a disadvantage in high step-up applications. Secondly, for voltage boost ($G_V > 1$) applications, IPOS architecture obtains lower K_{pr} than ISOP. In fact, $K_{pr_{ISOP}}$ curve never exceeds 1 when working in boost mode. On other hand, the ISOP architecture presents K_{pr} values lower than -1 when G_V is higher than 2. When G_V is higher than 2, the converter does not operate inside the PPP range, thus losing all benefits. Thirdly, if the application requires only buck mode ($0 < G_V < 1$), ISOP has lower K_{pr} than IPOS. In buck mode, $K_{pr_{ISOP}}$ never exceeds 1. However, $K_{pr_{IPOS}}$ exceeds 1 when G_V is lower than 0.5. Finally, if the application requires buck-boost functionality, the power converter enters in the shaded red (ISOP case) and blue (IPOS case) areas from Fig. 3. At these regions, the K_{pr} curve presents negatives values, meaning that the converter power flow is reversed [19]. In the case of the IPOS, V_{out} is inversely polarized and the flow of I_{in} changes its direction to the opposite way. Same thing occurs with the ISOP for voltage boost applications. In this case, the polarity of V_{in} and the direction of I_{out} must be inverted. To conclude, the IPOS architecture is the appropriate solution for voltage boost applications and the ISOP for voltage buck applications. If the

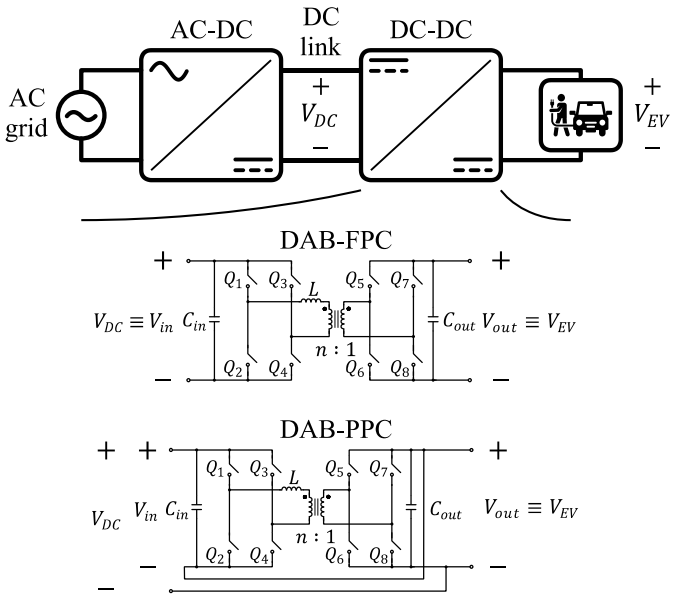

Fig. 4. Simplified diagram of the comparison under analysis: DC-DC stage of an OBC.

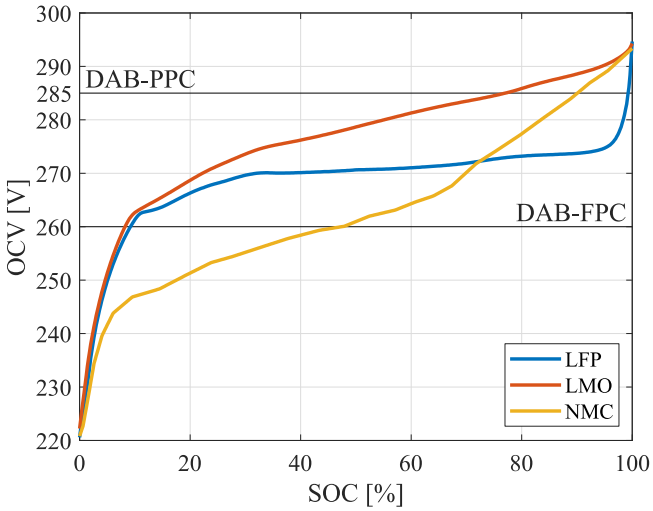

Fig. 5. OCV as a function of SOC for three different lithium-ion technologies. Two horizontal lines are highlighted at 260 V (DAB-FPC case) and 285 V (DAB-PPC case). These indicate specific working points that are discussed in detail later.

application consists of a buck-boost, the selection between the IPOS and the ISOP is not that obvious and a more complex comparison must be carried out. For the next analysis, the selected architecture is the ISOP and the reasons are described in Section III.

III. System Description

This paper is focused on an OBC application. Typically, an OBC is divided in two main stages [20]: AC-DC rectifier and DC-DC stage. The AC-DC stage operates as power factor corrector (PFC) and it regulates the voltage level of the DC link between both stages. The DC-DC controls the charging current of the battery of the EV. In relation to the normative around EV charging OBC systems, at present, the implementation of isolated DC-DC converters is required. Nevertheless, the need of galvanic isolation for DC charging application is not mandatory, and the implementation of non-isolated supply equipment is permitted for EV DC charging [21]. To be more precise, the countries that are included at the corrigendum of the IEC 61851-23 normative are Canada and the United States, which could encourage standards organizations to adapt the regulations. The charger examples presented in [20] locate the isolation border at the AC or the DC stage. Therefore, if a PPC architecture is implemented on the DC stage, the AC-DC rectifier could provide galvanic isolation. According to [22], [23], the benefits of implementing the isolation border in the DC stage are related to safety, minimizing touch currents. Also, it could increase the power density of the whole solution. This work is focused on the design of the DC-DC stage of the OBC, and therefore the isolation issue is suggested for future research. Fig. 4 shows a simplified diagram of the comparison under analysis: a dual active bridge full power converter (DAB-FPC) and a dual active bridge partial power converter (DAB-PPC). Although a non-isolated solution (DAB-PPC case) is compared to an isolated solution (DAB-FPC case), the main objective of this study is to research the new benefits that PPP brings to Si devices compared to WBG technologies.

The concerned application consists of a constant DC source voltage of 300 V (V_{DC}) and the EV's battery voltage (V_{EV}), which is modeled as shown in Fig. 5. There, three different open-circuit voltage (OCV) vs. state of charge (SOC) curves are presented. Each of them represents a different lithium-ion technology: lithium-iron-phosphate (LFP), lithium-manganese-oxide (LMO) and nickel-manganese-cobalt (NMC) [24]. The LFP presents a flat profile from 20 % to 95 % SOC. The LMO and the NMC show linear profiles above 10 % SOC values. The aim of considering batteries of three different chemistries is to demonstrate the impact of each of them on the performance of the DAB-FPC and the DAB-PPC.

Concerning the DAB-PPC solution, since it will operate at a voltage step-down application, an ISOP architecture is selected. Thus, reduced voltage is expected at the primary side ($V_{in} = V_{DC} - V_{EV}$) and reduced current at the secondary side ($I_{out} = I_{EV} - I_{DC}$). The DAB topology is selected for its zero voltage switching (ZVS) operation and bi-directionality. In this research, the DAB is controlled using single phase-shift modulation (PSM) due to its ease of implementation. To utilize the benefits of Si-devices, the DAB-PPC is enabled using Si-devices. The DAB-FPC is enabled using state of the art SiC semiconductors. This way, it is expected to observe the benefits that PPP can bring to the life extension of Si based semiconductor.

Table 1 defines the electrical design parameters of both converters. The first noticeable difference between the two solutions is V_{in}. In the case of the DAB-PPC a maximum voltage of 80 V is expected, which permits the implementation of lower voltage class and better conducting semiconductors (R_{ds}~$V_{DS}^{2.5}$ [25]) in the primary side bridge (Q_{1-4}). This results in lower conduction losses in the primary bridge of the

Table 1. Charging unit electrical parameters.

Parameter	DAB-FPC	DAB-PPC
V_{DC}	300 V	300 V
V_{EV}	From 220 V to 295 V	From 220 V to 295 V
V_{in}	300 V	From 80 V to 5 V
V_{out}	From 220 V to 295 V	From 220 V to 295 V
$\lvert\widehat{P_{conv}}\rvert$	3 kW	0.6 kW

converter. The voltage reduction at the primary side especially benefits Si technology, whose market offers a great variety of semiconductors at a lower cost. Also, a 5 times lower peak power is expected at the DAB-PPC. The converter power for the DAB-PPC is the result of multiplying the power consumed by the battery at the maximum K_{pr} point, which corresponds to the initial charging point (2250 W and 0.266, respectively).

The main drawback of the DAB-PPC is that for certain operating conditions, the converter can operate in non-ZVS regions. This is due to the fact that it has a greater operation range. As it can be observed in Table 1, the DAB-FPC consist of a fixed input voltage ($V_{in_{\text{DAB-FPC}}} = V_{DC}$) and a variable output voltage ($V_{out} = V_{EV}$). Whereas, the DAB-PPC contains both voltages variable: input ($V_{in_{\text{DAB-PPC}}} = V_{DC} - V_{EV}$) and output ($V_{out} = V_{EV}$). Consequently, the voltage gain observed by the DAB ($M = \frac{V_{in}}{V_{out} \cdot n}$) extends its operation range.

IV. Power converter model and control

Numerical simulations are performed to model both solutions: DAB-FPC and DAB-PPC. The power losses computed with this model are the ones related to the passive and active components inside the converter: magnetics, capacitors and semiconductors.

A. Magnetic element power losses

The power losses in the magnetic components of a DAB converter are divided in the series inductance and the isolation transformer.

The series inductances of the designed DAB converters use a high density litz wire. Therefore, skin and proximity losses in the working frequency range are neglected. The saturation flux is also selected as low so the core losses are also negligible. Due to these assumptions, the losses in the inductor are modelled in function of the inductor RMS current and the DC resistance of the inductor coil ($R_{DC_{inductor}}$), see (6).

$$P_{inductor} = R_{DC_{inductor}} \cdot I_{RMS}^2 \tag{6}$$

The transformer losses computation continues the same criteria as the inductor. As the transformer optimization is not the main contribution of the presented paper, high density litz wire and low saturation flux permits to neglect skin, proximity and core losses. Due to that, only DC resistance losses are modelled as given by (7). The DC resistance of the transformer are calculated in the primary side (R_{DC_p}) and secondary side (R_{DC_s}).

$$P_{transformer} = R_{DC_p} \cdot I_{RMS_p}^2 + R_{DC_s} \cdot I_{RMS_s}^2 \tag{7}$$

B. Capacitive element power losses

The power losses in the capacitive elements are dependent on the equivalent series resistance (ESR) of the used capacitors. The ESR is obtained from the datasheet for the fundamental frequency value of the current flowing through the capacitor. The capacitor leakage losses are taken as negligible (8).

$$P_{capacitor} = ESR \cdot I_{RMS}^2 \tag{8}$$

C. Semiconductor power losses

The power losses in the semiconductors are divided into conduction and switching losses.

C.1. Conduction losses

The conduction losses occur due to the current flowing through the inherent resistance of the device. This resistance is the on-state resistance (R_{ds}) of MOSFETs. The conduction loss of a MOSFET is given by (9).

$$P_{cond} = R_{ds} \cdot I_{RMS}^2 \tag{9}$$

C.2. Switching losses

Ideally, when a MOSFET switches from an ON state to an OFF state or vice versa, an instantaneous switch of its voltage and current is assumed. In reality, MOSFET's current and voltage coexist for a certain amount of time, which generates power losses each time they turn on and turn off. Turning a MOSFET off is often assumed to result in negligible losses and they can be up to five times lower than the turn on losses [26]. Bearing this in mind, with the aim of simplifying the analysis, only turn on losses will be considered. These can be classified into three types: ideal soft switching (or ZVS, incomplete ZVS (iZVS) and hard switching.

C.2.1 Ideal soft switching

Soft switching or ZVS occurs when a MOSFET turns on when its output capacitor is completely discharged. Fig. 6a shows a simplified ZVS transition. The switching events in waveforms are exaggerated for explanation purpose.

At interval 0a, the inductor current flows through Q_1 and the output capacitor of Q_2 is completely charged to the source voltage (V_{DC}). Then, the gate signal of Q_1 is turned off and the current stops flowing through its channel. Consequently, the positive flow of the inductor current helps to charge and discharge the output capacitors of Q_1 and Q_2, respectively (interval 1a or t_{ZVS}). Once the output capacitor of Q_2 is fully discharged, its body diode starts conducting until the dead band (t_{db}) time finishes (interval 2a). At this point, the gate signal of Q_2 reaches the threshold voltage and the inductor current flows through its conduction channel (interval 3a). The voltage drop

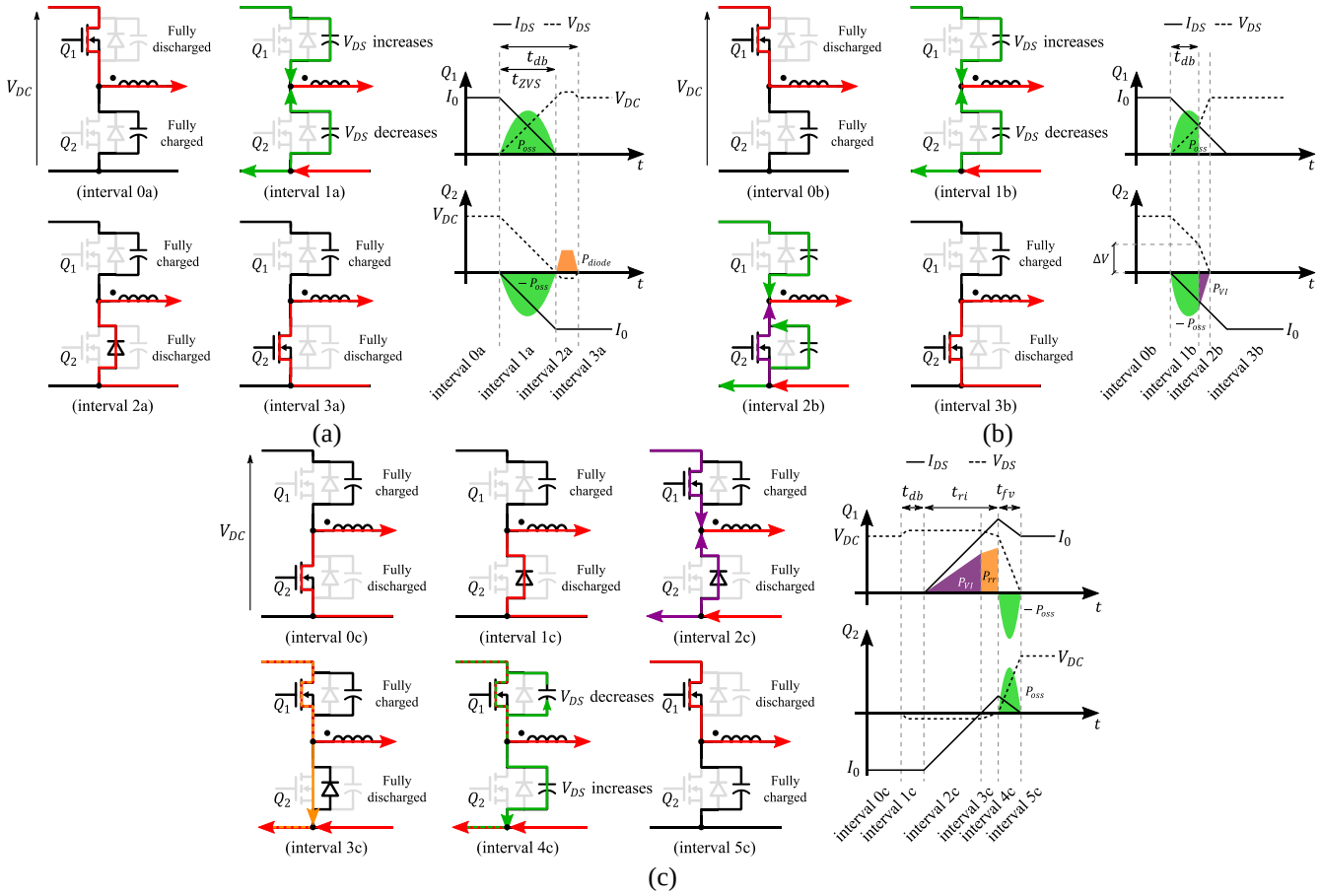

Fig. 6. Turn on of a MOSFET. (a) ZVS. (b) iZVS. (c) Hard switching.

that exits between interval 2a and interval 3a is just due to the transition from Q_2's body diode to its channel.

To sum up, the power losses in ZVS operation occur due to the resonant transition (interval 1a) and the conduction losses of the body diode (interval 2a). These losses are given in (10) and (11).

$$P_{oss} = E_{oss}(V_{DC}) \cdot f_{sw} \cdot \lambda_{oss} \tag{10}$$

$$P_{diode} = (V_{SD} \cdot I_{SD} + R_{SD} \cdot I_{SD}^2) \cdot \frac{t_{db} - t_{ZVS}}{T_S} \tag{11}$$

Where, λ_{oss}=0.5 (the charging/discharging process might dissipate more than 50% of the stored energy [27]), t_{db} is the dead time and t_{ZVS} is the resonant period. t_{ZVS} is computed using the charge stored by the MOSFET and the average switching current (12).

$$t_{ZVS} = \frac{Q_{oss}(V_{DC})}{\frac{I_0}{2}} \tag{12}$$

C.2.2 Incomplete soft switching

Although a semiconductor turns on with $I_{DS} < 0$, if the stored energy in the inductor is not high enough, it would not be able to completely charge and discharge both capacitances. This is known as iZVS and is shown in Fig. 6b.

Compared to ideal soft switching, in this case, t_{db} is not sufficient to complete the charge/discharge process. Therefore, at the end of interval 1b, Q_2 starts conducting while its output capacitor is charged to ΔV. Bearing this in mind, the losses that will be considered during iZVS are related to the resonant transition (interval 1b) and the conduction losses (interval 2b), (13),(14) respectively.

$$P_{oss} = (E_{oss}(V_{DC}) - E_{oss}(\Delta V)) \cdot f_{sw} \cdot \lambda_{oss} \tag{13}$$

$$P_{VI} = \frac{\Delta V^2}{R_{DS}} \cdot \frac{t_{iZVS}}{T_S} \tag{14}$$

Where, t_{iZVS} is the time left to completely charge/discharge the output capacitors and is given by (15).

$$t_{iZVS} = \frac{Q_{oss}(\Delta V)}{\frac{\Delta V/2}{R_{DS}}} \tag{15}$$

The boundary of the iZVS region is calculated by using (16) [27]. Expression (16) determines if the energy stored by the inductor is enough for the charging and discharging process of the MOSFETs' output capacitors.

$$\frac{1}{2} \cdot L \cdot I_0^2 \geq Q_{oss}(V_{DC}) \cdot V_{DC} \tag{16}$$

A.2.3 Hard switching

Hard switching occurs when a MOSFET starts conducting while its output capacitor is still charged to the source voltage. Fig. 6c shows a simplified hard switching.

At the beginning of the transition (interval 0c), the inductor current is free-wheeling through Q_2 and the output capacitor of Q_1 is fully charged to the output voltage (V_{DC}). Then, the gate signal of Q_2 is turned off and immediately, the inductor current flows through its body diode until the end of t_{db} (interval 1c). Contrary to the previous case, the positive flow of the inductor current does not help to discharge the output capacitor of Q_1 and charge the output capacitor Q_2. Therefore, when Q_1 starts conducting, it does with all the DC voltage and a current that rises to I_0 (interval 2c). However, the drain current of Q_1 continues increasing due to the reverse recovery effect of Q_2's body diode (interval 3c). Once the diode reaches its reverse recovery current, the rising current period (t_{ri}) finishes and it starts blocking voltage. At this point, the output capacitor of Q_1 discharges and the output capacitor of Q_2 charges to V_{DC} (interval 4c). Finally, the only current flowing through the channel of Q_1 is the inductor current (interval 5c).

In conclusion, Q_1 works under hard switching conditions when it is turned on with $I_{DS_{Q_1}} > 0$. Same thing occurs with Q_2 if it is turned on with $I_{DS_{Q_2}} > 0$.

To sum up, when hard switching occurs, the power losses that are considered are related to the VI losses (17), the reverse recovery losses (18) and the resonant transition (19).

$$P_{VI} = \frac{1}{2} \cdot I_0 \cdot V_{DC} \cdot \frac{t_{ri} + t_{fv}}{T_S} \tag{17}$$

$$P_{rr} = Q_{rr} \cdot V_{DC} \cdot f_{sw} \tag{18}$$

$$P_{oss} = \left(E_{oss_{Q1}} + E_{oss_{Q2}}\right) \cdot f_{sw} \tag{19}$$

The parameters t_{ri} and t_{fv} are computed using (20),(21). Where, Q_{GS} is the total charge that must be delivered as the gate voltage increases from the threshold voltage (V_{th}) to the plateau voltage (V_{pl}), and Q_v is the total of charge that must be delivered through the plateau. Both values are extracted from the datasheet of the device.

$$t_{ri} = \frac{Q_{GS}}{I_{gate}} = \frac{Q_{GS} \cdot R_{gate}}{V_{driver} - \frac{(V_{th} + V_{pl})}{2}} \tag{20}$$

$$t_{fv} = \frac{Q_v}{I_{gate}} = \frac{Q_v \cdot R_{gate}}{V_{driver} - V_{pl}} \tag{21}$$

D. ZVS, iZVS and hard switching regions for DAB-FPC and DAB-PPC

Estimation of switching loss requires identification of the ZVS boundary for DAB-FPC and DAB-PPC architectures. So, in the first place, the limits of the ZVS regions of each solution are defined following the steps from [28].

Fig. 7 presents the ZVS regions of each solution in function of M and the phase-shift (ϕ). The orange areas represent the hard switching region and the grey ones represent the iZVS region. The iZVS is easier to observe in Fig. 7a (DAB-FPC case) because of its lower M range. The dashed line represents the trajectory of the operating points of the converter through a complete charging process. As it can be observed, at both solutions, this line maintains a constant ϕ value at 60º (nominal ϕ). This corresponds to an ideal lossless behavior of the converter through the constant-current (CC) charging strategy. In reality, the phase-shift will suffer slight variations that must be corrected by a closed-loop control.

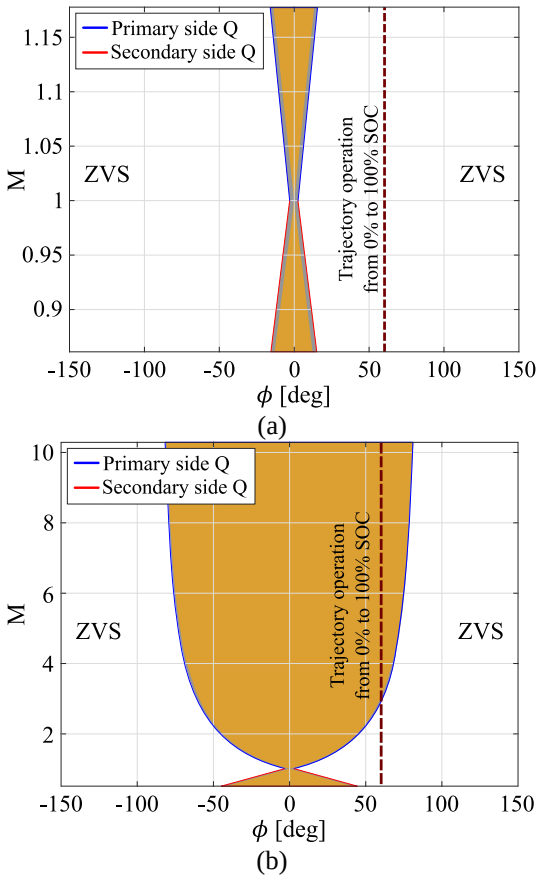

Fig. 7. ZVS regions and boundaries for primary and secondary side semiconductors using PSM. (a) DAB-FPC. (b) DAB-PPC.

In the case of the DAB-FPC (Fig. 7a), the dashed line does not enter into the orange or grey areas, which means that its switching devices always operate under soft switching conditions. However, the DAB-PPC (Fig. 7b) does enter inside the non-ZVS areas when M>3. In this condition, the semiconductors from the primary side do not commute under ZVS and their switching losses increase. Nevertheless, during non-ZVS operation (M>3), V_{EV} is at 280 V. In consequence, the switched voltage by the primary side semiconductors when hard-switching will only be 20 V or less. Therefore, a very low increment of the switching losses increment is expected.

E. Control strategy

A CC charging operation of the battery is considered for comparative evaluation. A closed-loop control strategy is implemented for both solutions and is shown in Fig. 8. It is

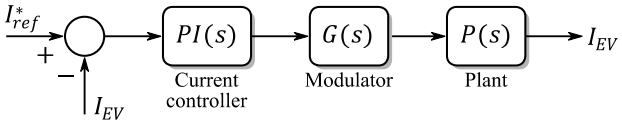

Fig. 8. CC control strategy.

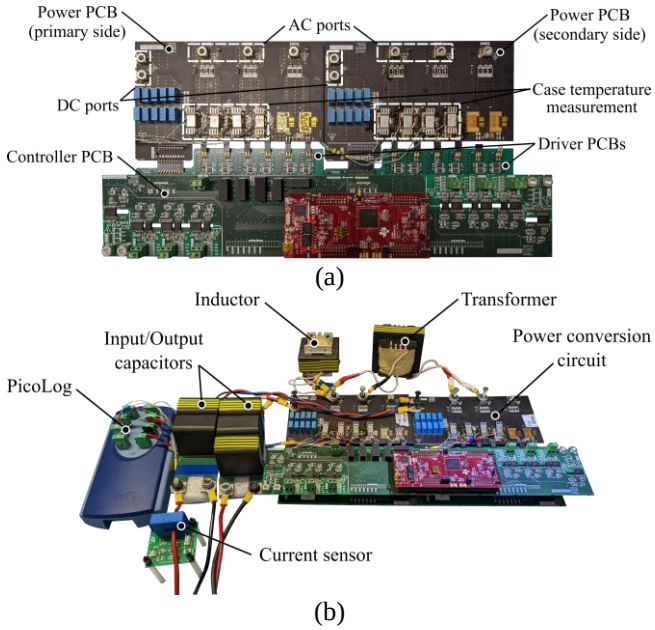

Fig. 9. Experimental prototype. (a) Power conversion circuit. (b) Test set-up.

assumed that the DC link (V_{DC}) is externally regulated. I^*_{ref} is the reference current during the CC mode and it is chosen based on the battery specifications. The difference between I^*_{ref} and the battery current (I_{EV}) is fed to a proportional-integral (PI) type current controller. The PI controller generates the phase shift to control the current output of the converters. Due to the low dynamics of the battery system charging process, the response of the closed-loop control does not require a high bandwidth.

V. Simulation and Experimental Results

The experimental prototype under analysis consists of 5 main PCBs (Fig. 9a): two power PCBs, two driver PCBs and a micro-controller PCB. Additionally two capacitor modules are connected externally to increase the capacitance of the DC filter (Fig. 9b). The feature of this prototype is that the selected footprint for the MOSFETs (D^2PAK7) allows implementing SiC and Si technologies. Also, the case temperature of the semiconductors is measured using a thermocouple data logger, and an external fan (NMB-MAT 4715FS-12T-B50) is used to cool the devices.

Table 2 describes the design parameters and the implemented devices of the SiC-based DAB-FPC and the Si-based DAB-PPC. First, each value of n is defined by applying expression (22), which ensures a low inductor RMS current.

Table 2. Design parameters and selected devices of the SiC-based DAB-FPC and the Si-based DAB-PPC.

Parameter	SiC-based DAB-FPC	Si-based DAB-PPC
f_{sw}	40 kHz	40 kHz
C_{in}	MKP1848C71050JY5[1]	MKP1848C71050JY5[1]
C_{out}	MKP1848C71050JY5[1]	MKP1848C71050JY5[1]
n	1.2	0.2
L	100 µH	15 µH
Q_{1-4}	IMBG65R022M1H[2]	IRFS4115-7P[3]
Q_{5-8}	IMBG65R022M1H[2]	IPBE65R075CFD7A[4]

Table 3. Magnetics' manufacturing parameters.

Parameter	DAB-FPC		DAB-PPC	
	Inductor	Transformer	Inductor	Transformer
Core	EE6527 (CF 139)	EE8020 (CF 139)	EE6527 (CF 139)	EE6527 (CF 139)
Volume	223 cm^3	367 cm^3	223 cm^3	223 cm^3
Nº of turns	16	36:30	10	6:30
Wire	2x95x200 (9.1 cm^3)	1x630x100 (25.9 cm^3)	1x95x200 (2.8 cm^3)	1x95x200 (10.2 cm^3)

$$M = \frac{V_{in}}{V_{out} \cdot n} = 1 \qquad (22)$$

Where, V_{in} and V_{out} are the input/output voltages of each solution when the battery is at 250 V. Then, the inductance is computed by using (23).

$$L_{min} \leq \frac{n \cdot V_{in} \cdot V_{out}}{8 \cdot f_{sw} \cdot |\widehat{P_{conv}}|} \qquad (23)$$

The switching devices from Table 2 are selected based on the voltage to be blocked, V_{in} and V_{out} defined in Table 1. The Si MOSFETs from Table 2 (IRFS4115-7P and IPBE65R075CFD7A) are 2.5 times cheaper than the SiC MOSFET (IMBG65R022M1H). When it comes to SiC, the lower voltage class that can be found in the market is 600 V. Therefore, the advantage of implementing reduced voltage semiconductors is not applicable for SiC devices, at least for the concerned application. GaN technology does offer lower voltage class semiconductors. However, their current capabilities are much lower and their implementation is focused on high frequency applications [2], [29].

The details of the magnetics for both DAB-FPC and DAB-PPC are given in Table 3. A transformer with higher volume is needed for the DAB-FPC than the DAB-PPC. The volume is

[1] 100 µF (C_{in}: 3 parallel connected; C_{out}: 2 parallel connected)
[2] V_{ds}=650 V , R_{ds}=31 mΩ @T_j=175 ºC [SiC]
[3] V_{ds}=150 V , R_{ds}=28.9 mΩ @T_j=175 ºC [Si]
[4] V_{ds}=650 V , R_{ds}=139 mΩ @T_j=150 ºC [Si]

defined as the minimum box which can be put around the active part of the core and windings [30]. The results show that the transformer of the DAB-FPC is 1.64 times bigger than the one required for the DAB-PPC. The litz wire is defined as the number of wires (N_w), times the number of strands (N_s), times the diameter of each strand in μm. The resulting volume of the wire is shown between parentheses, which is given by (24).

$$Volume_{wire} = N_w \cdot N_s \cdot \pi \cdot r_s^2 \cdot N_t \cdot P_E \quad (24)$$

Where r_s is the radius of the strand, N_t is the number of turns and P_E is the perimeter of the inner rectangle of the E core.

The results show that the DAB-PPC requires less wire volume: 3.2 times lower (inductor case) and 2.5 times lower (transformer case). This size reduction in the volume of the magnetics and wire also entails a less costly solution.

Regarding the experiments, these consist of a full charge of the lithium-ion batteries from Fig. 5. A DC power supply is used to act as the DC link and a battery emulator is used to emulate their characteristics. The current reference of the converter is set to 10.2 A and a battery capacity of 2.55 Ah is selected. This configuration ensures a 15 minute charge, time enough to observe the effect of the different OCV vs. SOC curves.

A. Results

In the first place, Fig. 10 and Fig. 11 present the experimental waveforms of the inductor current (i_L), the primary side semiconductor voltage (v_{Q_1}) and the secondary side semiconductor voltage (v_{Q_5}).

Fig. 10 shows the results of the DAB-FPC for three different working points: initial charging point (Fig. 10a), midpoint (Fig. 10b) and end of charging (Fig. 10c). The waveforms of v_{Q_1} and v_{Q_5} show that the maximum voltage blocked by Q_1 and Q_5 is 300 V. This confirms the necessity of implementing 650 V devices. Focusing on the switching, Fig. 10 demonstrates that, from the beginning to the end of the charging process, the DAB-FPC ensures ZVS for all the semiconductors. In the three working points, when Q_2 turns off, a negative i_L helps to charge/discharge the output capacitors. Then, after t_{db} finishes Q_1 turns on with zero voltage. Same thing occurs with $Q_{5,6}$, but with a positive flow of i_L.

Fig. 11 presents the experimental waveforms of the DAB-PPC: initial charging point (Fig. 11a), midpoint where the primary side semiconductors enter in non-ZVS region (Fig. 11b) and end of charging (Fig. 11c). Compared to the DAB-FPC, in the DAB-PPC, the waveforms of v_{Q_1} show that the maximum blocked voltage by Q_1 is 80 V (Fig. 11a), which demonstrates that the primary side semiconductors only block the voltage difference between the DC source and the battery. This value decreases down to 5 V as the battery charges. This can be seen in Fig. 11b and Fig. 11c, where the blocking voltage of Q_1 is 15 V and 5 V, respectively. Although an electromagnetic interference (EMI) analysis is out of the scope of this paper, it can be concluded that due to this low switching voltage at the primary side, the common-mode voltage is reduced [31]. On the other hand, v_{Q_5} shows that the maximum voltage blocked by Q_5 is 300 V, same as in the DAB-FPC case.

Regarding the switching of the DAB-PPC, its waveforms confirm that soft and hard switching conditions occur at the primary side. Firstly, in Fig. 11a, a ZVS operation mode can be observed. Similar to the DAB-FPC, when Q_2 or Q_6 turn off, a negative or positive flow of i_L helps to charge/discharge the output capacitors respectively. Once t_{db} finishes, Q_1 and Q_5 turn on with zero voltage. Secondly, Fig. 11b shows the moment in which the primary side semiconductors leave the ZVS region. This occurs when the battery voltage is around 285 V. At this moment, when Q_2 turns off, a negative flow of i_L helps to charge/discharge the output capacitors. However, during t_{db}, the i_L reverses its flow from negative to positive. Please observe the zoomed area from Fig. 11b. The positive flow of i_L charges the output capacitor of Q_1, provoking a voltage increment of v_{Q_1}. This increment does not last long, since t_{db} finishes and Q_1 turns on. On the other side, Q_5 continues under ZVS conditions. Thirdly, in Fig. 11c, a clear example of hard switching of Q_1 is observed. In this case, when Q_2 turns off, the positive flow of i_L does not help to charge/discharge the output capacitors of Q_1 and Q_2. At this moment, its body diode starts conducting, provoking a slight voltage increment, see the zoomed area. Then, Q_1 turns on with all this blocking voltage, which is only 5 V. To sum up, the only semiconductors that commute under hard switching conditions at the DAB-PPC are the ones at the primary side. Nevertheless, they get out from the ZVS region when the battery surpasses the 285 V. At this point, the primary side voltage is only 15 V, so the switching losses barely have an impact in the efficiency. This is discussed in detail later.

To demonstrate the CC control, the battery current (I_{EV}) and voltage (V_{EV}) are shown in Fig. 12a (LFP case), Fig. 12b (LMO case) and Fig. 12c (NMC case). As it can be observed, the current maintains a constant value as the battery voltage increases.

The case temperature comparison of the most heated MOSFET is shown in Fig. 13. The considered device from the DAB-FPC corresponds to the secondary side and the one from the DAB-PPC corresponds to the primary side. Both devices belong to the high current side. It is interesting to note that the temperature profile of SiC-MOSFETS in DAB-FPC present a similar curve to the OCV profiles from Fig. 5. This is because as the voltage increases from 220 V to 295 V, the switching losses for the devices on the secondary side increase proportionally. It should be also noted that among the three different battery chemistries, the NMC chemistry has a lower temperature in initial charging conditions. This behavior of case temperature with NMC chemistry is correlated with the OCV vs SOC curve. The NMC chemistry has lower OCV than LFP and LCO chemistries at low SOCs. Thus, the switching losses of the devices for NMC chemistry are lower than with LCO and LFP chemistries. This changes at higher SOC values, where the LFP maintains a lower voltage than the other two technologies. The maximum case temperature after considering the three battery chemistries is around 79 ºC.

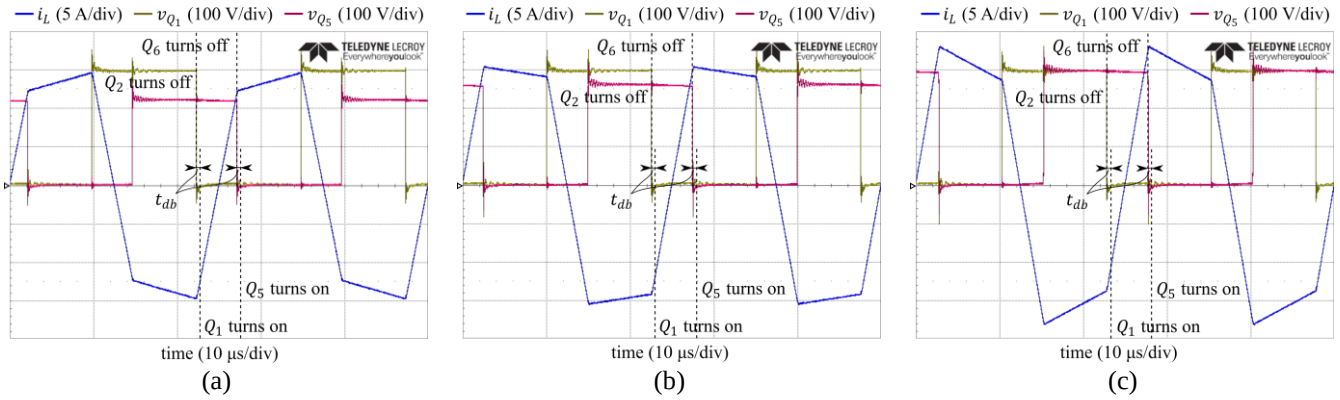

Fig. 10. Experimental waveforms of the DAB-FPC with SiC MOSFETs. (a) Initial charging point (V_{EV}=220 V). (b) Midpoint (V_{EV}=260 V). (c) End of charging (V_{EV}=295 V). All semiconductors work under ZVS.

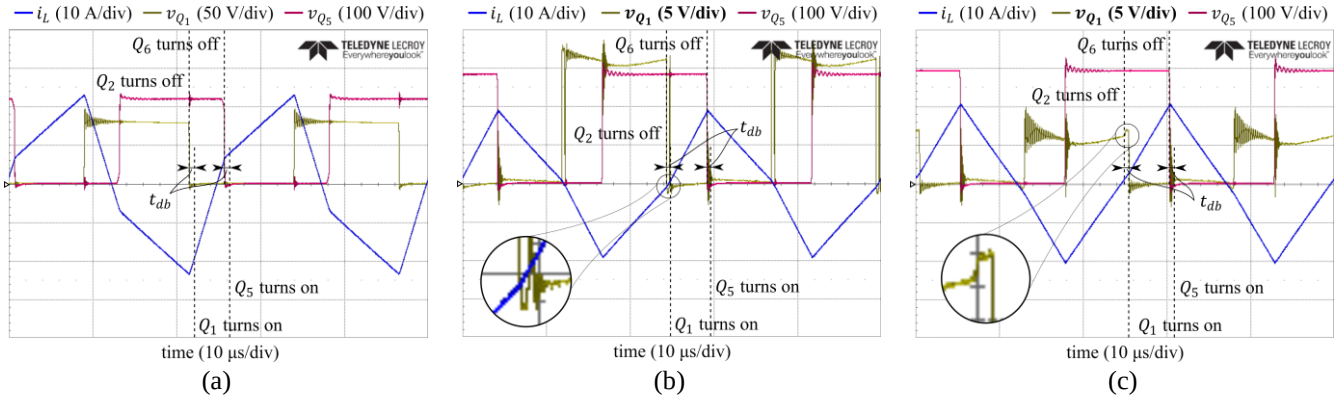

Fig. 11. Experimental waveforms of the DAB-PPC with Si MOSFETs. (a) Initial charging point (V_{EV}=220 V). (b) Midpoint where primary side semiconductors get out the ZVS region (V_{EV}=285 V). (c) End of charging. (V_{EV}=295 V).

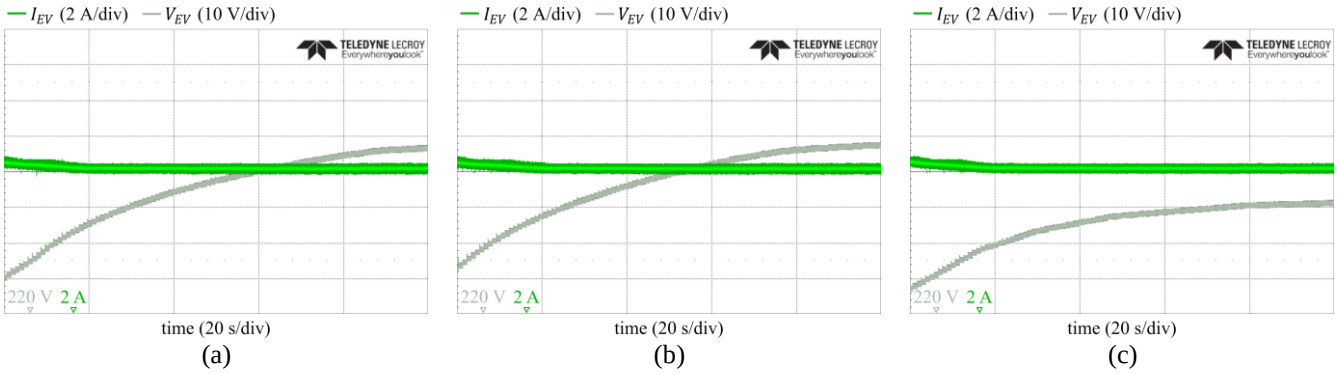

Fig. 12. Experimental battery current and voltage. (a) LFP. (b) LMO. (c) NMC.

For the DAB-PPC architecture, the temperature profile is quite different. Apart from the fact that the maximum case temperature is much lower (37.6 ºC), its curve decreases as the battery charges. This is strictly related to the K_{pr}. As the battery is charged, its voltage gets closer to the 300 V, which reduces the K_{pr}, thus the power processed by the converter. This is observable at the NMC temperature curve. Since its OCV profile presents lower voltage values than the LMO and LFP, the power processed by the DAB-PPC is higher at a low SOC when charging an NMC. For this reason, the NMC profile presents higher temperatures at the beginning.

Focusing on the temperature curves of the DAB-PPC, the effect of operating in the non-ZVS region can also been seen at the end of the charging process (SOC>70 %). At this point, the OCV with LMO chemistry surpasses the 285 V (Fig. 5), thus leading to hard switching of devices. This leads to an increment in the switching losses and hence in the temperature of the primary side devices. Similar behavior is observed with the

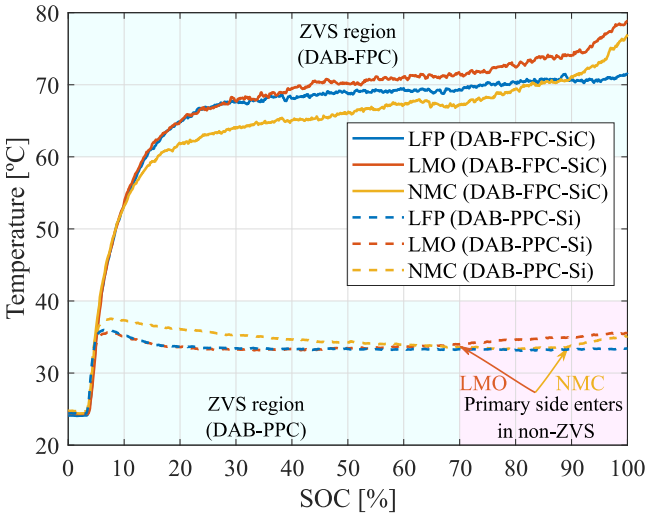

Fig. 13. Case temperature evolution of the most heated semiconductor.

NMC chemistry when SOC>90 %. For the LFP chemistry, the battery voltage exceeds 285 V when the battery is almost completely charged. Thus, the impact of hard switching events with LFP chemistry is minimal. Due to the temperature dependency of the on-state resistance, the low thermal stress achieved with the DAB-PPC results in better conduction characteristics.

Fig. 14 presents the comparison of efficiency of the two architectures using analytical models and experiments. The experimental efficiency results are obtained by using a power analyzer. More detailed information about the equipment used in the experimental tests is given in the Appendix. Fig. 14a compares the results of the DAB-FPC with SiC. As it can be observed, the analytical and experimental results show that the efficiency slightly reduces as the battery charges. The effect of the OCV-SOC curves is also noticeable, since the NMC obtains higher efficiencies than the other two battery technologies at low SOCs. This is directly related to the temperature curves from Fig. 13.

Fig. 14b compares the simulation and experimental efficiency results of the DAB-PPC with Si-devices. As it can be observed, both show a lower system efficiency when a NMC battery is charged. Especially at initial charging conditions, when a lower OCV profile causes higher K_{pr} values. Also, the numerical simulations and experimental tests present a slight efficiency drop when the DAB-PPC enters in hard switching conditions. This occurs when the SOC reaches 70 % (LMO case), 90 % (NMC case) and 99 % (LFP case). This is a direct consequence of their OCV curves surpassing 285 V (Fig. 5).

The experimental results from both solutions are compared in Fig. 14c. It is clear that the DAB-PPC with Si MOSFETs is more efficient than the DAB-FPC with SiC MOSFETs. Indeed, the DAB-FPC does not reach a 97 % efficiency, while the DAB-PPC presents efficiencies higher than 99 % through nearly all the charging process. Similarly to the temperature curves, the NMC profile has visible differences at the efficiency curves. In the case of the DAB-FPC, the lower voltage of the NMC affects

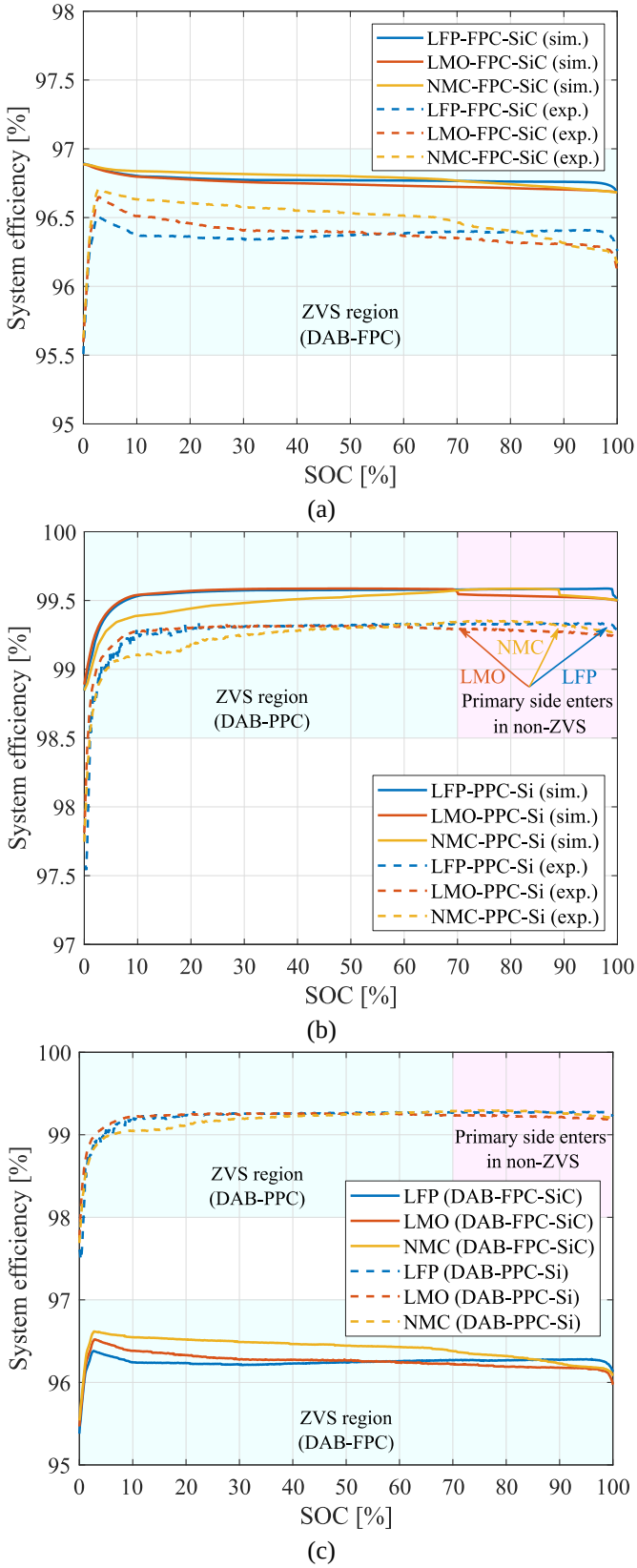

Fig. 14. Numerical simulation and experimental efficiency results. (a) DAB-FPC with SiC. (b) DAB-PPC with Si. (c) Only experimental results.

Table 4. Total energy losses through the battery charging process.

Parameter		SiC-based DAB-FPC		Si-based DAB-PPC	
		E_{loss} [Wh]	$\frac{E_{loss}}{E_{charged}} \cdot 100$ [%]	E_{loss} [Wh]	$\frac{E_{loss}}{E_{charged}} \cdot 100$ [%]
LFP	Sim.	22.76	3.33	3.06	0.45
	Exp.	26.79	3.90	5.39	0.78
LMO	Sim.	23.69	3.36	3.20	0.47
	Exp.	27.50	3.89	5.59	0.79
NMC	Sim.	22.34	3.32	3.41	0.51
	Exp.	25.15	3.73	5.50	0.81

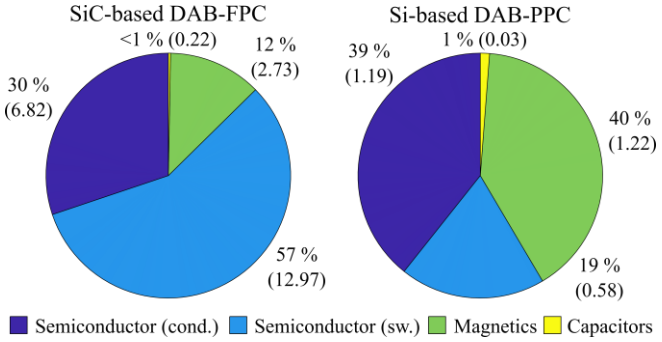

Fig. 15. Energy losses classification through the battery charging process. Simulation results for the LFP case. The results between parenthesis quantify the losses in Wh.

positively to the efficiency. However, in the case of the DAB-PPC the contrary occurs. Table 4 summarizes the total energy losses of each solution and its weight in comparison to the total energy charged. Both, numerical solutions and experimental results conclude that the Si-based DAB-PPC is the most efficient. Also, it can be observed how the different OCV-SOC curves of the battery chemistries impact each solution. For example, the DAB-FPC achieves its lowest E_{loss} values when an NMC battery is implemented. However, in the case of the DAB-PPC, the NMC provokes higher E_{loss} than the other two technologies. As discussed before, this is because of the NMC's low OCV at initial charging conditions. Additionally to Table 4, Fig. 15 classifies the different sources of the power losses for each solution. These simulation results correspond to the LFP case, but very similar values are obtained with the LMO and the NMC. As it can be observed, in both solutions the power losses of the switching devices are predominant (87 % and 58 %, respectively). However, in the DAB-PPC their weight is decreased, especially due to the reduction of the switching losses (from 57 % to 19 %).

Finally, Table 5 presents the electrical stress seen by the passive and active devices [32], which is given by (25). Due to the reduced power processed by the converter, all the passive and active devices, the inductor, the capacitors and the semiconductors of the DAB-PPC present a lower electrical stress than the ones from the DAB-FPC (≈15 % - 77 %). The magnetics and the semiconductors are the components that benefit the most.

Table 5. Electrical stress comparison at worst case. Base current (10 A) and base voltage (300 V) are chosen based on the maximum battery current and voltage respectively.

Parameter	SiC-based DAB-FPC	Si-based DAB-PPC
VA rating of the inductor L (V_{rms}, I_{rms})	2.09 pu	0.43 pu
Stress in C_{in} (V_{pk}, I_{rms})	0.99 pu	0.37 pu
Stress in C_{out} (V_{pk}, I_{rms})	1.30 pu	1.01 pu
Stress in Q_{1-4} (V_{pk}, I_{rms})	1.03 pu	0.30 pu
Stress in Q_{5-8} (V_{pk}, I_{rms})	1.22 pu	0.17 pu

Table 6. Main comparison parameters where a Si-based Dab-PPC outperforms a SiC-based DAB-FPC.

Parameter		SiC-based DAB-FPC	Si-based DAB-PPC
Maximum case temperature of Q		79 ºC	37.6 ºC
Volume	Inductor	223 cm^3	223 cm^3
	Transformer	367 cm^3	223 cm^3
	Total wire	35 cm^3	13 cm^3
Overall $\frac{E_{loss}}{E_{charged}} \cdot 100$		3.84 %	0.79 %
Electrical stress	Inductor L	2.09 pu	0.43 pu
	Input capacitor C_{in}	0.99 pu	0.37 pu
	Output capacitor C_{out}	1.30 pu	1.01 pu
	Primary side switch Q_{1-4}	1.03 pu	0.30 pu
	Secondary side switch Q_{5-8}	1.22 pu	0.17 pu

$$Component\ stress = \frac{V_{pk,rms} \cdot I_{rms}}{V_{base} \cdot I_{base}} \quad (25)$$

VI. Discussion

With the aim of remarking the benefits and advantages of the Si-based DAB-PPC upon the SiC-based DAB-FPC, Table 6 summarizes the main improvements achieved with the PPP-based solution.

Firstly, the maximum case temperature of the switching devices is halved in the DAB-PPC. This reduction of the thermal stress improves the conduction characteristics of the semiconductors. In a second optimization process, this could lead to a reduction in the cooling system, which entails a lowered cost and volume. Secondly, the volume results of the DAB-PPC for the transformer and the wire are 1.6 and 2.7 times lower, respectively. This volume reduction can be related with a cost reduction of passive devices. Together with cheaper semiconductors, the Si-based DAB-PPC turns out as a less costly solution. Thirdly, the average energy losses achieved with the DAB-PPC are 3 points lower. Fourth, an electrical stress reduction of the magnetics, the capacitors and the switching devices is achieved with the DAB-PPC (between 15 % and 77 %). The inductor and the secondary side semiconductors are the devices the present a major reduction.

The main disadvantage of the DAB-PPC relays on the lack of galvanic isolation. Nowadays, OBC chargers are required to provide a galvanic isolation capability, which presents a technical challenge for commercial availability of the DAB-PPC. In this sense, a future research on the safety and faulty

conditions of the DAB-PPC would support the implementation of PPC solutions in OBC applications. In [33], authors compare the faults propagation of a DAB-FPC and a DAB-PPC. The study concluded that the vulnerability of the load in PPC operation increases due to the faulty current that flows through the anti-parallel diodes of the MOSFETs in the low voltage side. However, this issue is tackled by implementing back-to-back switches in the low voltage side. This way, the complexity of the converter is increased, but the K_{pr} can be reduced if buck-boost functionalities are considered [19]. For these reasons, the authors expect that promising non-isolated solutions (such as the DAB-PPC presented in this work) could encourage standards organizations to adapt the regulations.

VII. Conclusion

This study discusses the advantages of Si-based PPCs against SiC-based FPCs. The wide and matured market of Si-devices and their low price makes them an ideal candidate to enable PPC architectures. To quantify the advantages of Si-enabled DAB-PPC architecture, an OBC application is analyzed in this paper. Three different battery chemistries are considered to compare both architectures. The different OCV-SOC curves of each chemistry conclude that the same battery technology has a contrary effect on the performance of both solutions. Due to the benefits of PPP, the DAB-PPC architecture utilizes low blocking voltage semiconductors (with low on-state resistance) and its devices suffer a lower electrical stress. It is also shown that even though the PPC solution may lead to non-ZVS of devices in certain operating conditions, the overall efficiency and performance with respect to case temperature is much better of Si-based DAB-PPC than SiC-based DAB-FPC. Results using numerical simulations and a 3 kW experimental prototype demonstrate that the Si-based DAB-PPC has improved performance than SiC-based DAB-FPC in all metrics: thermal stress, efficiency, volume and cost.

The authors also conclude that future studies on PPC based OBCs should focus on its main challenges, such as: EMI noises, grid harmonics and fault propagation.

Appendix

Table 7 lists the equipment used for the experimental tests.

Table 7. Equipment used at experimental tests.

Description	Reference
Source	TDK-Lambda GEN 500-20
Battery emulator	Chroma 62180D-1200
Power analyzer	Hioki PW6001
Oscilloscope	Teledyne LeCroy MDA810
Temperature measurement	Pico Technology TC-08

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