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# Comprehensive analysis of voltage balancing techniques for 5L-NPC converters

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## Keywords

«Modulation strategy», «Active Front-End», «Multilevel converters», «Voltage Source Converter»

## Abstract

The reduced capability of the 5L-NPC Inverter to balance the voltages of the four DC-bus capacitors makes this converter unattractive for real power applications. This is especially true if the load demands active power. The Back-to-Back (B2B) configuration of two 5L-NPC converters and the use of a Space Vector Modulation (SVM) that exploits the voltage balancing capabilities of the redundant switching vectors, extend the operating conditions range in which a proper voltage balance can be achieved. However, if practical modulation restrictions are considered (limitation of voltage steps, dead times, switching losses, etc.) the voltage balance cannot be achieved for all operation conditions.

This paper introduces the main restrictions that should be considered for the 5L-NPC modulation strategy. The voltage balancing limits of the proposed SVM scheme are shown and additional considerations to improve the voltage balancing capability are proposed and evaluated.

## Introduction

Power electronic converters play an important role in Medium Voltage (MV) drive applications. The development of power semiconductors has extended the voltage and current capability of actual Voltage Source Converters (VSC) on those applications.

The three level Neutral Point Clamped converter (3L-NPC, [1]) is one of the most popular converter topologies for MV drive applications. This converter requires the series connection of semiconductors or a step-up transformer in order to operate at voltage levels above 4.16kV. The use of topologies of higher number of levels allows increasing the operating voltage levels above 6.6kV with standard semiconductors. Furthermore, the use of such topologies can provide improved output voltage quality and even transformerless operation [2-3]. For instance, if the 3L-NPC converter is extended to five voltage levels (5L-NPC, [4]) the same improvements over the 3L-NPC converter could be obtained.

The DC-bus of the 5L-NPC converter is composed by four series connected capacitors, Fig. 1. The five output voltage levels are obtained connecting the output terminal to the different intermediate nodes of the DC-bus capacitors. The main drawback of the 5L-NPC Inverter operation, Fig. 1, is the limited voltage balancing capability of the DC-bus capacitors especially when the load demands active power.

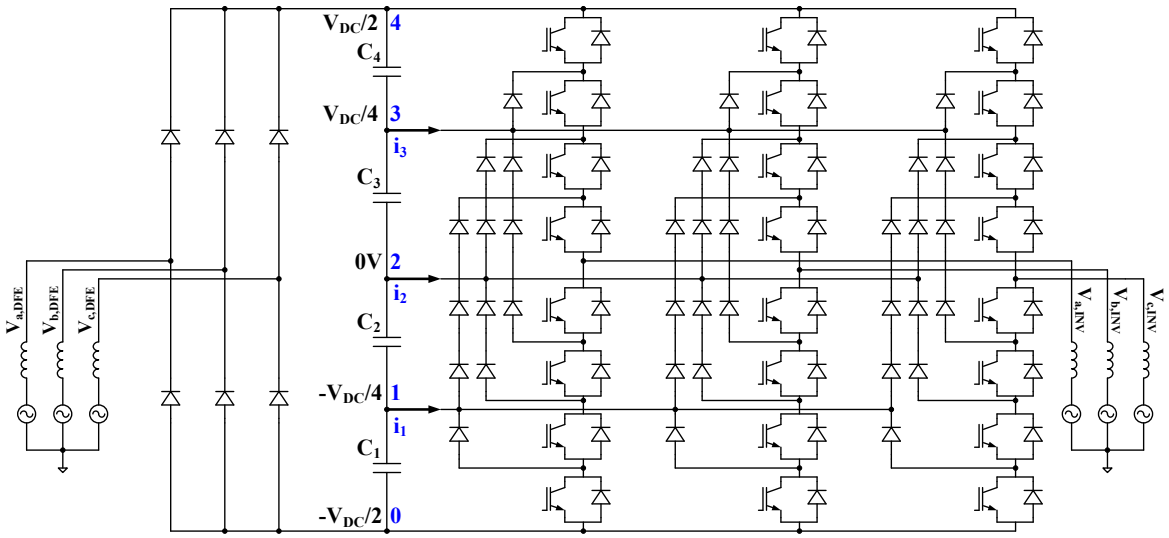


Fig. 1: 5L-NPC Inverter with a Diode Front End (DFE)

The operation of two 5L-NPC converters in a Back-to-Back (B2B) configuration, Fig. 2, in conjunction with a Space Vector Modulation (SVM) that exploits the balancing effect of the redundant switching vectors, results in a notable increase of the voltage balancing capability of the converter. Although several papers have been published describing different voltage balancing methods for the 5L-NPC B2B configuration ([5-8]), usually, those methods require high computational cost [5], do not take care about the number of switching level steps at the output terminals and power losses [6-7] or make use of additional power circuitry to achieve a proper voltage balance [8]. At this point, it could be said that the lack of a standard and practical solution to the DC-bus voltage balancing problem makes difficult the commercial use of this converter.

This paper proposes and describes a SVM modulation strategy for the 5L-NPC converter which considers real restrictions for the modulator scheme such as computational cost, dead times, power losses, number of simultaneous voltage level steps per arm, minimum turn on/off times for semiconductors, etc. In addition, the voltage balancing capability of the proposed modulation scheme is shown and additional considerations to increase the voltage balancing limits are proposed.

Thus, the first part of the paper introduces the main restrictions that should be taken into account for the modulation strategy in order to be used in real power applications. In the second part, the analysis of the voltage balancing capability of the proposed SVM strategy is analyzed and the limitations of the proposed modulation scheme to achieve a balanced operation of the voltages are shown. The third part proposes additional considerations to extend the operating conditions range in which a proper voltage balance is achieved.

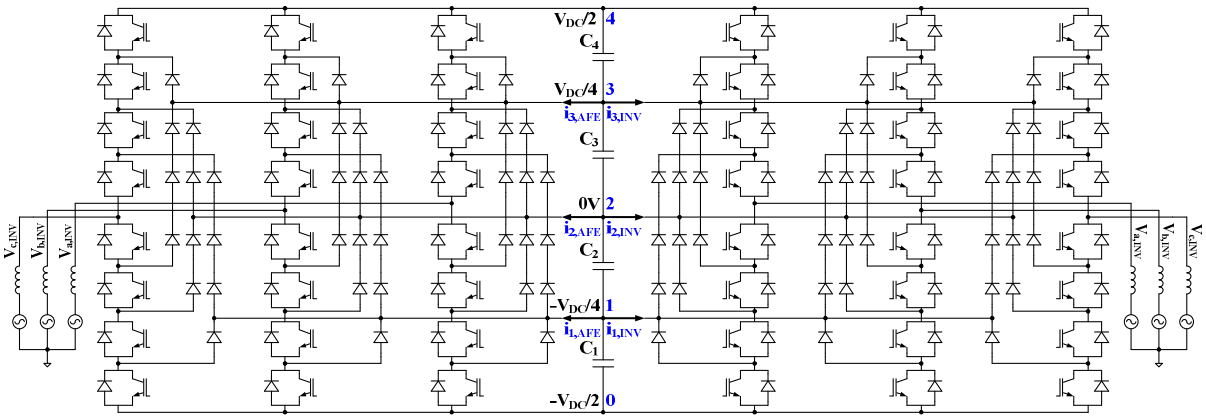


Fig. 2: 5L-NPC B2B converter

## Restrictions considered for the Space Vector Modulation scheme

A 5L-NPC converter can synthesize the 125 different voltage vectors shown by Fig. 3. As shown by Fig. 3, the synthesizable 125 switching vectors are geometrically distributed in 61 positions which represent the applicable 61 line to line voltages by the converter. The switching vectors that share the same position in the Space Vector map generate the same line to line output voltage but have different effect on the currents across the DC-bus intermediate nodes. Those switching vectors are redundant vectors and are necessary to achieve a proper voltage balance of the DC-bus capacitors.

The reference output voltage vector can be represented by:

$$\vec{V}_{ref} = \vec{V}_{\alpha} + j\cdot\vec{V}_{\beta} = V_{a0,ref}\cdot\vec{a}^{0} + V_{b0,ref}\cdot\vec{a}^{1} + V_{c0,ref}\cdot\vec{a}^{2} \quad \text{where} \quad \vec{a} = e^{j\frac{2\pi}{3}} \tag{1}$$

In general, the reference voltage vector must be synthesized combining the applicable switching vectors by the converter, Fig. 3. Furthermore, the proper selection of redundant switching vectors to synthesize the output voltage makes possible the voltage balance of the DC-bus capacitor voltages.

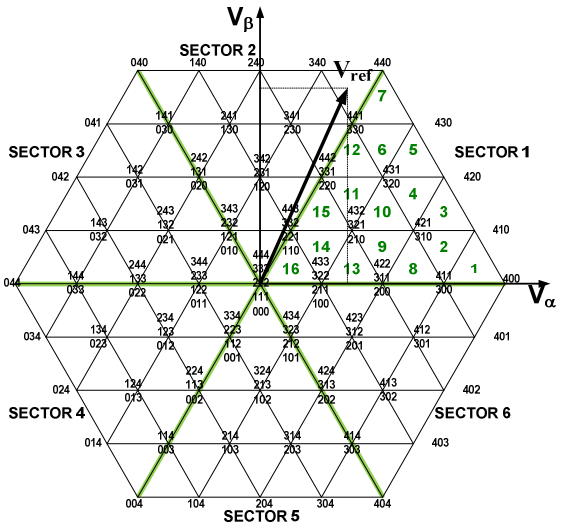



Fig. 3: Five level Space Vector (SV) map

The simplest way to synthesize the reference voltage vector is to combine the nearest switching vectors during a modulation period ($T_{PWM}$), [5]. The reference voltage vector contained in a given region of the Space Vector (SV) map is synthesized combining adjacent switching vectors, that is, vectors from the three vertexes of that region, Fig. 4a. The duty cycles ($d_{Vx60}$, $d_{Vy60}$ and $d_{V0}$) of the applied switching vectors ($v_{x60}$, $v_{y60}$ and $v_0$) depend on the projection of the reference voltage vector to each axe of the region, Fig. 4a and equations (2) and (3).

$$\vec{V}_{ref} = \vec{V}_{x60}\cdot d_{vx60} + \vec{V}_{y60}\cdot d_{vy60} + \vec{V}_{0}\cdot d_{v0} \tag{2}$$

$$d_{vx60} + d_{vy60} + d_{v0} = 1 \tag{3}$$

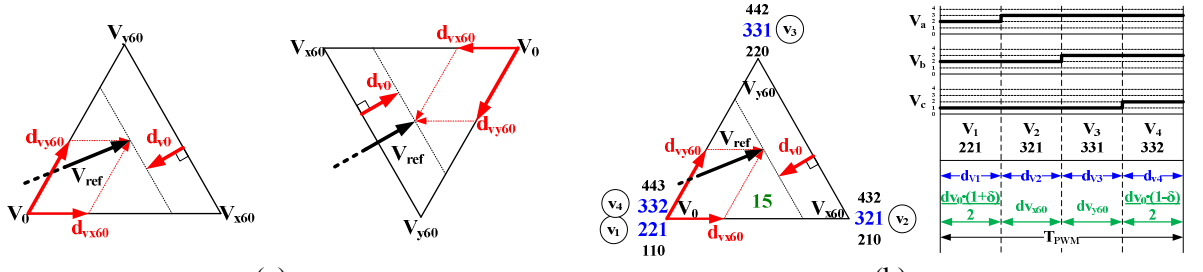



Fig. 4: Four vector sequence construction. a) Nearest Three Vectors distribution; b) Four vector sequence (221-321-331-332)

The main goal of the SVM scheme presented in this paper is the voltage balance of the DC-bus capacitors. However, in order to reduce the switching losses and guarantee a proper operation of the converter, the number of voltage steps per arm allowed between two consecutive switching vectors is limited to one. In addition, the number of evaluated switching vector sequences is limited in order to reduce the computational load of the modulation scheme. Finally, due to minimum turn on/turn off times and dead times imposed by the switching semiconductors, some considerations must be taken into account in order to guarantee the proper synthesis of the output reference voltage vector. All those restrictions guarantee the proper operation of the converter, however they lead to a limited voltage balancing capability of the DC-bus capacitors.

The vector sequences applied by this modulation scheme are composed by four vectors. The first and the fourth vectors of the applied vector sequence are redundant vectors (located in the same vertex of the region), Fig. 4b. The other two vectors applied in the vector sequence are located in the other two vertexes of the region. In order to minimize the switching losses, the only considered vector sequences are the ones that change just one voltage level from an applied voltage vector to its consecutive voltage vector as shown by Fig. 4b.

Among the available voltage vector sequences in a given region of the SV map, the optimal vector sequence must be selected and applied. The selection of the optimal vector sequence to be applied is done in three steps.

In a first step, depending on the last applied vector sequence, the considered sequences are the ones that cause less switching transitions and consequently less switching losses. In addition, due to the minimum turn on/turn off ($t_{on,off,min}$) and dead times ($t_{dt}$) required by the switching semiconductors, it is necessary to consider a minimum duty cycle for the first and fourth vectors ($d_{V1,min}$, $d_{V4,min}$) of the vector sequence (4) in order to ensure that the output voltage is properly synthesized.

$$d_{V1,min} = d_{V4,min} \leq \frac{\left(t_{dt} + t_{on,off,min}\right)}{T_{PWM}} \tag{4}$$

Depending on the position of the reference voltage vector in the SV map, not all the available four vector sequences are able to satisfy the criteria given by (4). Thus, the number of evaluated four vector sequences is considerably reduced leading to a reduced computational cost. Consequently, the considered voltage vector sequences allow the proper operation of the power converter (switching step limitations) and power semiconductors (minimum turn on/off times) maintaining low switching losses and a reduced computational cost.

In a second step, the time distribution for the redundant vectors is calculated in order to improve the voltage balance of the DC-bus capacitors. This is evaluated for all the available switching sequences.

As described above, the first and the fourth vectors of the switching sequences are redundant vectors. This means that these vectors have different influence on the currents of the different DC-bus nodes while generate the same line to line output voltage. δ defines the time distribution of the first and fourth redundant vectors (5). The average current in an intermediate node (n) of the DC-bus, $i_n$, depends on the load current, the applied four vector sequence and the time distribution of the first and fourth redundant vectors (δ), equation (6).

$$\delta = 2 \cdot \frac{d_{V1}}{d_{V1} + d_{V4}} - 1 = 1 - 2 \cdot \frac{d_{V4}}{d_{V1} + d_{V4}} \tag{5}$$

$$\bar{i}_n(\delta) = \left[ i_{V1,n} \cdot \left(d_{V1} + d_{V4}\right) \frac{1+\delta}{2} \right] + \left( i_{V2,n} \cdot d_{V2} \right) + \left( i_{V3,n} \cdot d_{V3} \right) + \left[ i_{V4,n} \cdot \left(d_{V1} + d_{V4}\right) \frac{1-\delta}{2} \right] \tag{6}$$

Note: $i_{vy,n}$ refers to the effect of the $y^{th}$ vector in the n node current and $d_{Vy}$ refers to the duty cycle of $y^{th}$ vector of the vector sequence.

The nonzero average node current during a modulation period ($T_{PWM}$) results in the change of the node voltage error ($\varepsilon_n$), that is, the voltage difference between two adjacent capacitors of the DC-bus ($\varepsilon_n = V_{C,n} - V_{C(n+1)}$). Equation (7) defines the change of the voltage error in the n node during a modulation period:

$$\varepsilon_{fin,n}(\delta) = \varepsilon_{ini,n} - i_n(\delta)\frac{T_{pwm}}{C_{DC}} \tag{7}$$

Note: $C_{DC}$ refers to the capacity of each capacitor of the DC-bus, and $\varepsilon_{ini,n}$ and $\varepsilon_{fin,n}$ refer to the voltage error of the n node at the beginning and at the end of the modulation period respectively.

The optimum time distribution ($\delta$) for the redundant vectors is calculated to minimize the total quadratic error of the three DC-bus capacitor nodes, equation (8).

$$\varepsilon_{total}(\delta) = f(\delta) = \left(\varepsilon_{fin,1}(\delta)\right)^2 + \left(\varepsilon_{fin,2}(\delta)\right)^2 + \left(\varepsilon_{fin,3}(\delta)\right)^2 \tag{8}$$

If the optimum time distribution ($\delta$) for the redundant vectors cannot guarantee minimum turn on/off times, a minimum duty cycle must be applied to achieve the proper operation of the semiconductors. Fig. 6.

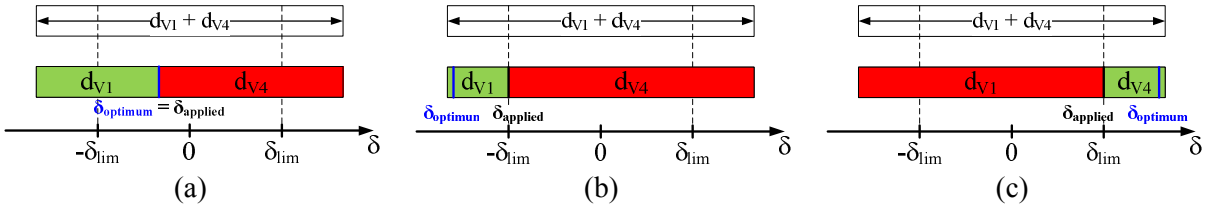



Fig. 6: Redundant vectors time distribution for three different sequences. a) $-\delta_{lim} < \delta_{opt} < \delta_{lim}$, b) $\delta_{opt} < -\delta_{lim}$, c) $\delta_{opt} > \delta_{lim}$

Finally, in a third step, the optimum voltage vector sequence is selected and applied. Basically, the node errors obtained with the different vector sequences are evaluated and the vector sequence that gets the minimum quadratic voltage node error (8) is considered the optimum sequence to apply. This vector sequence will be the voltage sequence applied by the converter.

This modulation strategy is applied independently in both the Inverter and the Active Front End (AFE) of the 5L-NPC B2B converter. The coordinate optimum voltage vector sequence [5] selection results in a poor benefit in terms of voltage balancing capability but increases a lot the computational load.

## Voltage Balancing Capability of the SVM with practical restrictions

In this section the voltage balancing capability of the proposed SVM strategy with the considered practical restrictions has been analyzed. The voltage balancing capability of the DC-bus capacitors is directly related to the achievable currents in the intermediate nodes of the DC-bus. To ensure the voltage balancing of the DC-bus capacitors, the average current of the nodes must be zero. In order to evaluate the ability of the converter to control the current of the DC-bus intermediate nodes two analyses are presented for different load power factors and modulation indexes: the operation of a 5L-NPC Inverter with a Diode Front End (DFE) and the B2B operation of an AFE and Inverter.

### Operation of the Inverter with a Diode Front End (DFE)

The voltage balancing capability of NPC Inverter topologies with more than three output voltage levels has been widely analyzed in the literature [9-10]. In [9] the theoretical voltage balancing capability of the infinite voltage level NPC Inverter is presented, while [10] shows the limits for a 5L-NPC Inverter, Fig. 7.

As it can be deduced from Fig. 7, if a 5L-NPC Inverter operates with reactive power (output current is phase shifted ±90º from the output voltage) it is possible to achieve a proper voltage balance for any modulation index ($m_a$), (9). If the load demands active power, the voltage balancing capability of this

converter becomes worse. This is especially true if the load demands pure active power (current and voltage are in phase). In this case, the maximum modulation index in which the proper voltage balance is achieved is limited to 0.55 approximately. This means that the DC-bus voltage utilization of the 5L-NPC Inverter is very poor in active power demanding applications.

$$m_a = \frac{V_{ll,rms,1}}{V_{DC}} \cdot \sqrt{2} \tag{9}$$

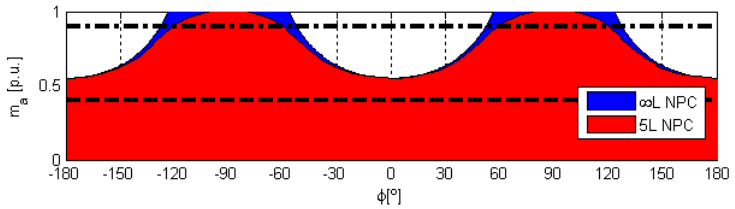
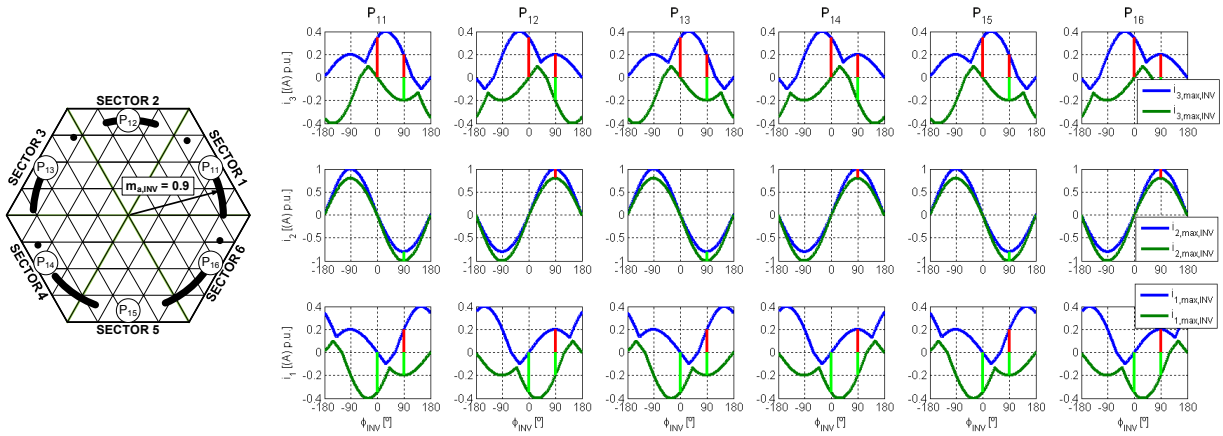



Fig. 7: Balanced operating area for ∞L-NPC [9] and 5L-NPC Inverter [10]

In order to understand the voltage balancing limits shown by Fig. 7, the maximum/minimum synthesizable intermediate node currents have been estimated along six points of the switching trajectory of the reference output voltage vector. This estimation has been done for two different modulation indexes ($m_{a1,INV}$ = 0.9 and $m_{a2,INV}$ = 0.4) and any phase shift between the output voltage and the output current ($\Phi_{INV}$).

Fig. 8 shows the evolution of the node currents (maximum and minimum obtainable values) operating at a high modulation index ($m_{a1,INV}$ = 0.9). As it can be observed, when the load demands pure active power (zero phase shift), the synthesizable $i_3$ node current is positive while the synthesizable $i_1$ node current is negative. Consequently the node 1 will be charged while the node 3 will be discharged. This implies that the voltage balance is not possible for this operation condition. In contrast, if the loads demands pure reactive power (90º phase degree), the synthesizable node currents have positive and negative values. This behavior provides to the SVM the ability to control the sign of the average current of the intermediate DC-bus nodes and therefore the capability to balance the voltages of the DC-bus capacitors.




(a) (b)

Fig. 8: Synthesized currents of the intermediate nodes of 5L-NPC Inverter for $m_{a1,INV}$ = 0.9. a) Trajectory of the voltage vector in SV map for $m_{a1,INV}$ = 0.9; b) Maximum/minimum current of the intermediate nodes at points ($P_{11}$…$P_{16}$)

Fig. 9 shows the evolution of the node currents (maximum and minimum available values) operating at a low modulation index ($m_{a2,INV}$ = 0.4). As it can be observed, when the load demands pure active power (zero phase shift), the SVM can synthesize both positive and negatives node currents and therefore the voltage balance of the DC-bus capacitors is possible. If the converter operates with reactive power the ability to synthesize positive and negative node currents is maintained so the voltage balance is also possible.

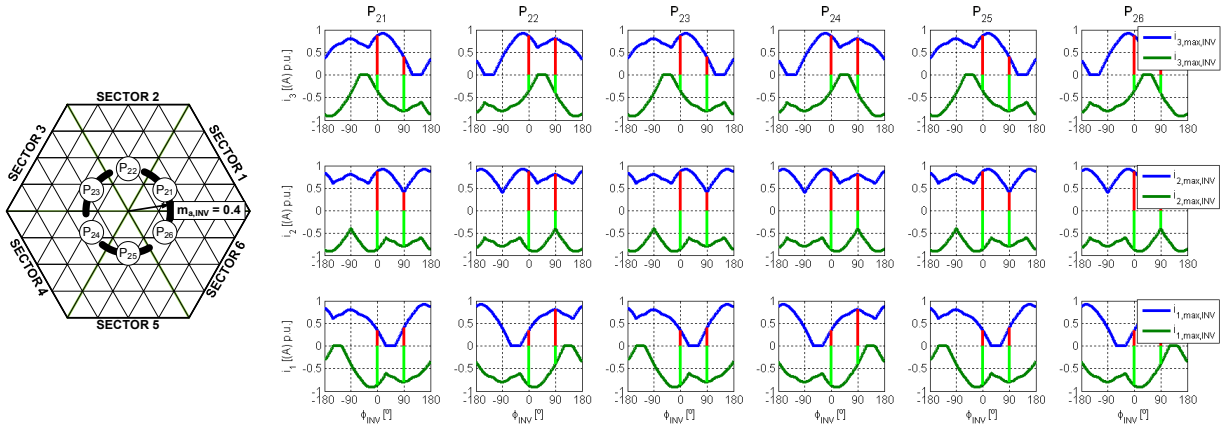



Fig. 9: Synthesized currents of the intermediate nodes of 5L-NPC Inverter for $m_{a2,INV} = 0.4$. a) Trajectory of the voltage vector in SV map for $m_{a2,INV} = 0.4$; b) Maximum/minimum current of the intermediate nodes at points ($P_{21}$…$P_{26}$)

In conclusion, this analysis shows the influence of the modulation index ($m_a$) and the load current phase shift ($\Phi_{INV}$) on the voltage balancing capability of the DC-bus voltages. As it can be observed, the balanced operation of the DC-bus capacitors at high modulation indexes is only possible if pure reactive power is demanded by the load. The balanced operation with an active power demanding load is only possible at low modulation indexes.

## Operation of the converter in a B2B configuration

As concluded in the previous section, the DC-bus voltage utilization of a DFE/5L-NPC Inverter is very poor in active power demanding applications. The B2B configuration of two 5L-NPC converters increases the ability of the modulation scheme to achieve zero average node currents and consequently a balanced operation of the DC-bus capacitors is possible in a wider operation condition range.

Fig. 10 shows the maximum and minimum node currents synthesizable by the active rectifier and the Inverter for similar modulation indexes ($m_{a1,AFE} = 0.88$ and $m_{a1,INV} = 0.80$) and operating at unity power factors. In this operation condition the DFE/5L-NPC Inverter cannot guarantee a proper voltage balance, however, the proposed modulation scheme in a B2B configuration is capable to achieve a proper voltage balance of the DC-bus capacitors.

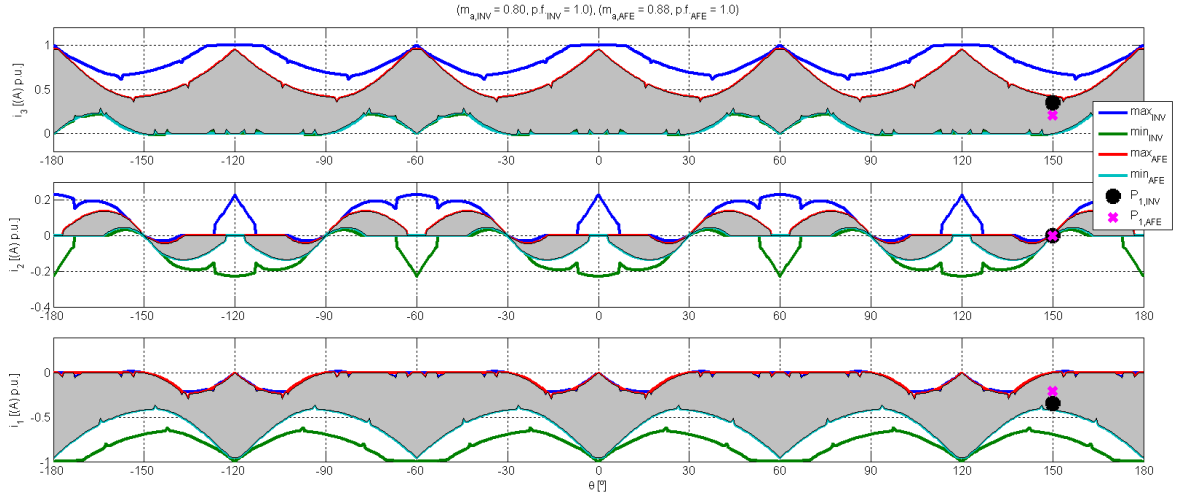



Fig. 10: Maximum/Minimum synthesizable currents of the intermediate nodes of 5L-NPC B2B for $m_{a1,INV} = 0.80$, $\cos\varphi_{1,INV} = 1$, $m_{a1,AFE} = 0.88$, $\cos\varphi_{1,AFE} = 1$

The operation instant ($P_1$) shown by Fig. 10 depicts the three intermediate node currents synthesized by the AFE and the three intermediate node currents synthesized by the Inverter for the given (AFE/Inverter) voltage vector sequence. As it can be observed, the synthesized intermediate node

currents by both converters are not the same but they are quite similar. If the maximum/minimum synthesizable node currents by both converters cover a high common area, the node current differences are low and the DC-bus capacitor is high enough, the node current extracted by one converter can be compensated by the injected node current by the other converter on an entire fundamental waveform cycle with an acceptable transient voltage unbalance. Thus, the proper DC-bus nodes voltage balance is possible.

In contrast, as shown by Fig. 11, as the difference between modulation indexes of both converters becomes bigger ($m_{a2,AFE}$ = 0.75 and $m_{a2,INV}$ = 0.95) the synthesizable maximum and minimum node currents by each converter become notoriously different. In this case, the proposed modulation scheme is not able to achieve a proper voltage balance of the DC-bus capacitors.

Fig. 11 shows an operation instant ($P_2$) in which the synthesized node currents by each converter are shown. At this point, similar $i_1$ and $i_2$ node currents are synthesized by both converters, however, the currents in node 3 are notoriously different. This means that at this operation point it is very difficult for the modulation scheme to synthesize equal node currents and therefore it is very difficult to achieve a proper voltage balance of the DC-bus capacitors. Generally speaking, at high modulation indexes, if modulation indexes of both converters are notoriously different the simultaneous synthesis of similar node currents at the three nodes becomes difficult and in consequence the voltage balance of the DC-bus capacitors is not possible.

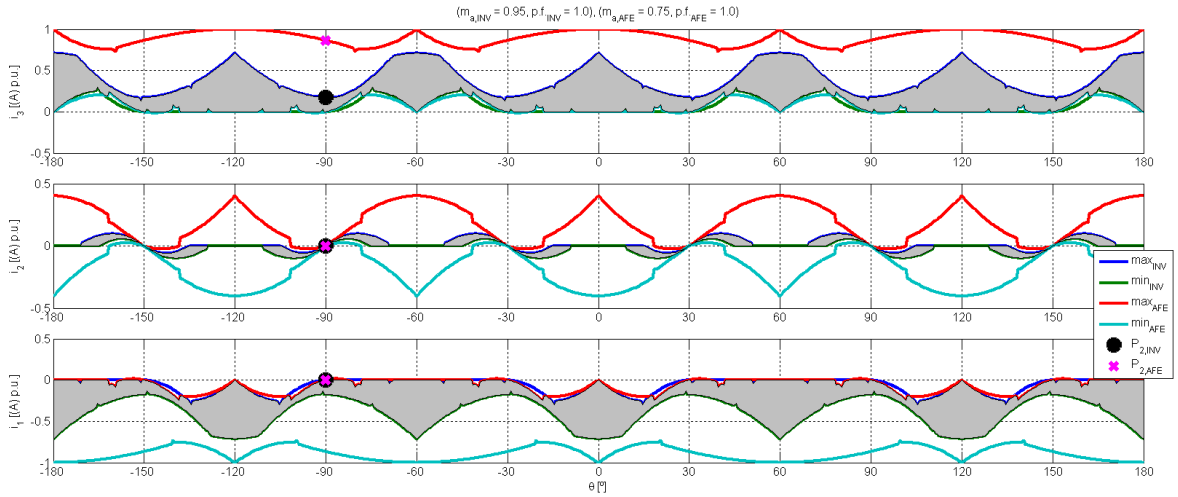
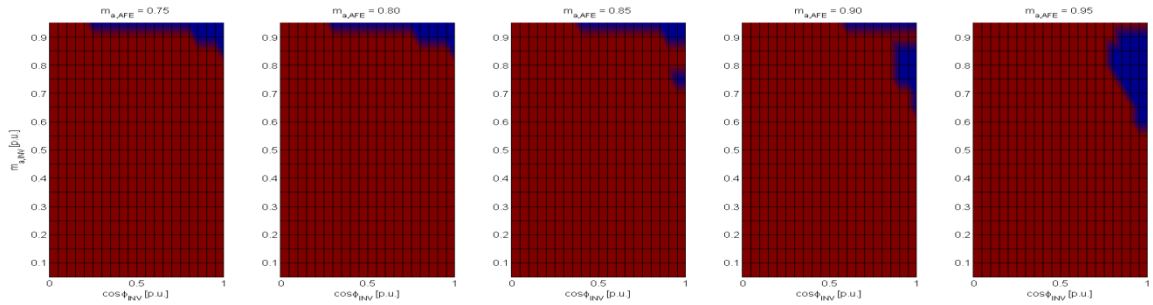



Fig. 11: Maximum/Minimum synthesizable currents of the intermediate nodes of 5L-NPC B2B for $m_{a2,INV}$ = 0.95, $\cos\varphi_{2,INV}$ = 1, $m_{a2,AFE}$ = 0.75, $\cos\varphi_{2,AFE}$ = 1

The voltage balancing capability of the proposed modulation scheme in a B2B configuration is shown by Fig. 12. The blue shaded area represents the non-balanceable operating points. The results show that the SVM cannot guarantee the DC-bus capacitors voltage balance at high modulation indexes of the Inverter, especially for active power loads.




(a) (b) (c) (d) (e)

Fig. 12: Voltage balancing capability with the proposed modulation scheme for 5L-NPC B2B converter at high modulation indexes of the AFE. a) $m_{a,AFE}$ = 0.75; b) $m_{a,AFE}$ = 0.8, c) $m_{a,AFE}$ = 0.85, d) $m_{a,AFE}$ = 0.9, e) $m_{a,AFE}$ = 0.95

## Additional considerations to improve the voltage balance of the DC-bus capacitors

As demonstrated in previous sections, the load power factor has an important influence on the voltage balancing capability of the 5L-NPC converter. In a B2B configuration the Inverter side provides the power demanded by the load. The AFE must extract the required active power required by the load from the grid. If the modulation indexes of the AFE and the Inverter are different, the voltage balance can be achieved if the AFE operates with power factors lowers than the unity. Thus, this paper proposes the increase of the voltage balancing capability by means of the power factor reduction in the AFE.

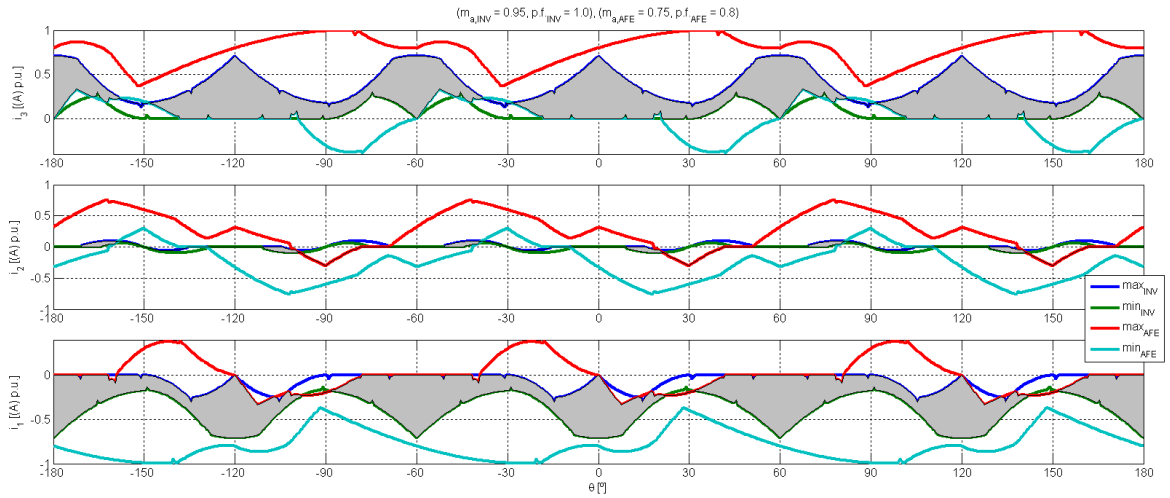
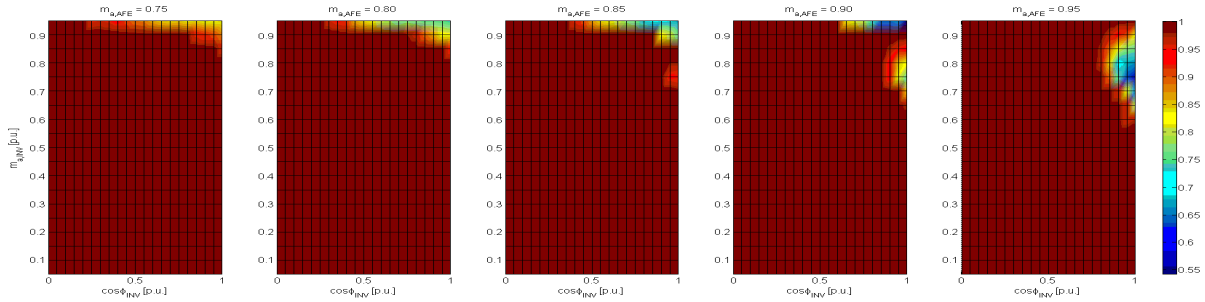



Fig. 13: Maximum/Minimum synthesizable currents of the intermediate nodes of 5L-NPC B2B for $m_{a3,INV} = 0.95$, $\cos\varphi_{3,INV} = 1$, $m_{a3,AFE} = 0.75$, $\cos\varphi_{3,AFE} = 0.8$

Fig. 13 shows the maximum/minimum node currents obtained by the AFE and the Inverter ($m_{a3,INV} = 0.95$ and $m_{a,3AFE} = 0.75$). As shown in the previous section, Fig. 11, if both converters operate with a unity power factor the voltage balance of the DC-bus capacitors is not possible. However, in Fig. 13, the power factor of the AFE is reduced to achieve a proper voltage balance of the DC-bus capacitors. The reduction of the power factor of the AFE has two advantageous effects for the voltage balance. On one hand, the maximum synthesizable node currents by the AFE are closer to the maximum currents synthesizable by the Inverter in nodes 2 and 3, as well as the minimum synthesizable currents in nodes 1 and 2. On the other hand, the currents synthesizable by the AFE in nodes 1 and 3 can be either positive or negative, which improves the self balancing capability of the AFE. As demonstrated in previous paragraphs, both effects have a positive influence on the voltage balancing capability on an entire fundamental waveform cycle and the proper voltage balance is possible in this operation condition.

Thus, at the expense of a worsened power factor, the proper voltage balance of the DC-bus capacitors is possible for any operation condition. The colored areas shown by Fig. 14 depict the power factor required by the AFE to achieve a proper voltage balance. As it can be observed, as far as the modulation indexes and the power factor of the Inverter increase, the required power factor by the AFE is lower. Although some non-practical operation conditions are found in which the demanded power factor by the AFE are too low (0.55), in general it could be said that the reduction of the power factor leads to a better utilization of the DC-bus voltage.




(a) (b) (c) (d) (e)

Fig. 14: Required grid power factor ($\cos\varphi_{GRID}$) to achieve DC-bus capacitors voltage balance with the proposed modulation scheme for 5L-NPC B2B converter at high modulation indexes of the AFE. a) $m_{a,AFE} = 0.75$, b) $m_{a,AFE} = 0.8$, c) $m_{a,AFE} = 0.85$, d) $m_{a,AFE} = 0.9$, e) $m_{a,AFE} = 0.95$

## Conclusions and Contributions

In this paper the voltage balancing capability of a SVM in a 5L-NPC Back-to-Back (B2B) converter is analyzed. For this analysis, practical restrictions related to the modulation are considered. The evaluation of the voltage balancing capability is presented for the DFE/5L-NPC Inverter configuration and the B2B configuration at different power factors and modulation indexes. The results show that the voltage balance is not possible at high modulation indexes and high power factors. Additional considerations have been analyzed to improve voltage balancing capability. The reactive power injection guarantees the DC-bus capacitors voltage balance in any operating condition, but it deteriorates the AFE power factor and consequently decreases the amount of active power that it can provide to the Inverter.

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