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Simple voltage balancing method to protect series-connected devices experimentally verified in a 5L-MPC converter

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***Abstract*—This paper presents a solution for the voltage balance problem of the series-connected devices that can be applied to multilevel converters in which the series-connected devices need to block twice their switched voltage. The solution is based on two ideas, the control of the switching commands to achieve proper switching losses balance and the use of additional circuitry to achieve proper voltage balance during their blocking state. The proposed strategy is experimentally validated into a 5 Level-Multi Point Clamped (5L-MPC) full-scale converter. However, it can be used in any other converter topology in which the devices need to block twice their switched voltage.**

***Index Terms*—Medium voltage (MV), multipoint clamped (MPC), multilevel converter, neutral point clamped (NPC), T-type converter, voltage source converter (VSC), insulated gate bipolar transistors (IGBT), series connection of semiconductors.**

I. Introduction

POWER electronic converters transform electrical energy flow from one form to another, satisfying specific needs of the application. The development of power semiconductor devices has increased the number and type of applications where power converters are used. Among these applications, Medium Voltage (MV) drives [1]–[4] make the variable speed control of synchronous and asynchronous machines possible. In general, a grid side converter controls the common DC-link voltage while a machine side converter transforms the DC voltage into variable frequency and amplitude voltage [5]–[7].

Power electronic converters are mainly based on power semiconductors, being the silicon (Si) the most widely used material for their construction. The relatively narrow band gap of the silicon (1.1eV) limits the maximum voltage-blocking capability of the semiconductor to less than 10 kV. This implies that the voltage blocking capability of these semiconductors cannot be sufficient for real Medium/High Voltage applications [8].

The series connection of power semiconductor devices, enables the operation of well-known few-level converters (2L VSC, 2 Level-Voltage Source Converter; and 3L-NPC, 3 Level-Neutral Point Clamped Converter [9]) at voltage levels higher than the rated voltage of one single semiconductor.

In case that some semiconductors need to be series-connected, the IGBT is the preferred choice over the IGCT because the IGBT allows the control of the switching dynamics by means of the gate terminal. This makes the proper voltage balance of the series-connected IGBTs possible, avoiding the use of bulky and lossy snubber networks or at least minimizing their size [7], [10].

Fig. 1 shows typical voltage unbalances between unmatched series-connected IGBT devices. It can be observed that big time deviations can be measured at turn on and turn off switching transitions. Those time deviations lead to voltage unbalances and power-loss unbalances between the series-connected devices. As it can be observed in Fig. 1, tail current differences have a notorious negative influence on the voltage unbalance for a relatively long time (several tens of microseconds) [11], [12].

There are several proposals to improve the voltage unbalance problem between the series-connected IGBTs. Among the solutions, there are the snubber circuits [13]–[16], active clamp circuits [17] or active gate control methods [11], [12], [16], [18], [19]. Snubbers are reliable and simple solutions to achieve a proper voltage balance between the series-connected devices. However, the increase on the overall power losses make them an unattractive solution [12].

Clamp circuits limit the maximum blocking voltage of any device. The extra losses generated when the IGBT operates in the active region make them unattractive for high power and high switching frequency applications.

Active gate control methods modify the switching behavior of the IGBT controlling the charging process of the gate terminal. Thus, depending on the control strategy, synchronous switching and similar voltage slopes can be obtained between the series-connected devices. However, tail current differences or reverse recovery current differences cannot be controlled by the gate terminal and therefore, the use of some passive

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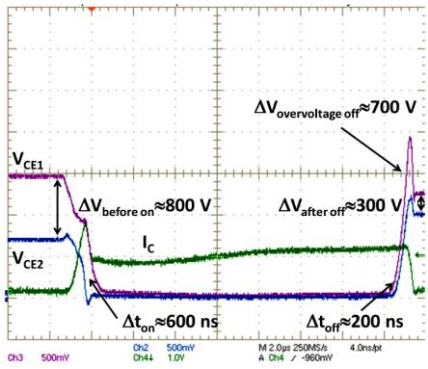
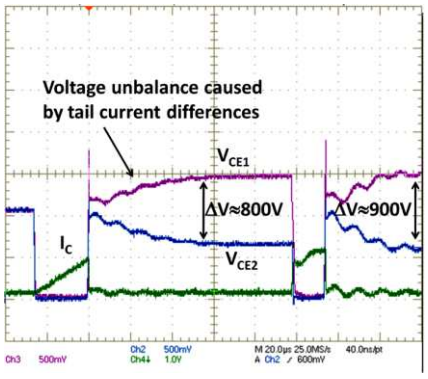
networks are mandatory [11], [12], [16]. Although promising results can be achieved by means of active control methods, the complexity of the gate driver is probably their most important drawback.

Another choice to operate at Medium/High Voltage levels is the use of multilevel converters. In addition to the improved output voltage quality, multilevel converters can avoid the series connection of switching devices or at least, in case that the series connection of semiconductors is mandatory, minimize the problems related to the voltage balance of the series-connected devices [1]–[3], [5]. The maximum voltage to be supported by each semiconductor is determined by the topology and the number of output voltage levels of the converter.

Among the different multilevel converters, cascaded H-bridge converters can operate at High Voltage levels connecting in series simple converter modules. The main drawback of these topologies resides in the isolated power supplies required by each module to operate with active power [20]–[22].



(a)



(b)

Fig. 1. Voltage unbalance during switching transitions between two series-connected IGBTs [11]. (a) Switch on and switch off transitions. (b) Voltage waveforms during the tail current period.

Flying capacitor converters enable the operation at High Voltage levels; however, the large amount of energy stored by the capacitors makes this topology unattractive [3], [23].

Well known 2L-VSC and 3L-NPC converters require the series connection of IGBT/Diodes to operate at Medium/High Voltages. The series-connected devices must support all the DC-link voltage and operate at the switching frequency. This makes the series connection of the switching devices a real challenge.

During the last years, a new multilevel topology has appeared for the Medium Voltage drive market, the 5L-ANPC converter [24]. This converter requires the series connection of switching devices, however, the low switching frequency of the series-connected devices makes less challenging the proper operation of the series-connected devices using simple balancing circuits.

In [7], a 5L-MPC converter is used in a 6.6 kV drive application. This non-patented converter topology has a good harmonic distortion and makes possible the transformerless operation of the converter. The converter is experimentally validated and its suitability for real drive applications is demonstrated showing promising results.

In this converter, several IGBTs and diode pairs are connected in series. However, these devices can operate as non-series-connected devices under hard switching conditions, while they must operate as series-connected devices during the blocking state. In consequence, simple auxiliary circuits are only required for their proper voltage balance during their operation on the blocking state. This makes possible the adoption of simple and effective solutions to guarantee the proper operation of the series-connected devices.

This paper analyzes the 5L-MPC converter and the behavior of the series-connected devices. In addition, this paper proposes a solution to the proper operation of the series-connected devices and finally, the proposed method is experimentally validated. The proposed solution can be adopted by any other multilevel topology in which the series-connected devices need to block twice their switched voltage such as, Stacked MultiCell converter (SMC [25]) or T-type converter (also named as Neutral Point Piloted, NPP, [26]).

II. Voltage Requirements of the Switching Devices in the 5L-MPC

The 5L-MPC [7] topology belongs to the NPC (Neutral Point Clamped) converter family. This converter is based on the connection of a 3L-NPC and two half-bridges, achieving five voltage levels per phase in the output terminals: $V_{DC}/2$, $V_{DC}/4$, 0V, $-V_{DC}/4$ and $-V_{DC}/2$. Table I and Fig. 2 summarize the switching states of each semiconductor to synthetize each output voltage level. As it can be seen, positive voltages are generated with the upper half of the branch while negative voltages are symmetrically generated with the lower half of the branch. Therefore, the semiconductors operation for the positive voltage generation can be extrapolated to the negative voltage generation due to its symmetry.

TABLE I
SWITCHING STATES OF 5L-MPC CONVERTER

V_{ph-o}	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8
$V_{DC}/2$	1	0	1	1	0	0	1	0
$V_{DC}/4$	0	1	1	1	0	0	1	0
0 V	0	1	0	1	1	0	1	0
$-V_{DC}/4$	0	1	0	0	1	1	1	0
$-V_{DC}/2$	0	1	0	0	1	1	0	1

Fig. 2(a) shows the general converter configuration assuming that the used semiconductors can block a voltage up to $V_{DC}/4$. As it can be observed, clamp diodes (D_{C1} and D_{C2}) and inner semiconductors (T_4 and T_5) must be series-connected because

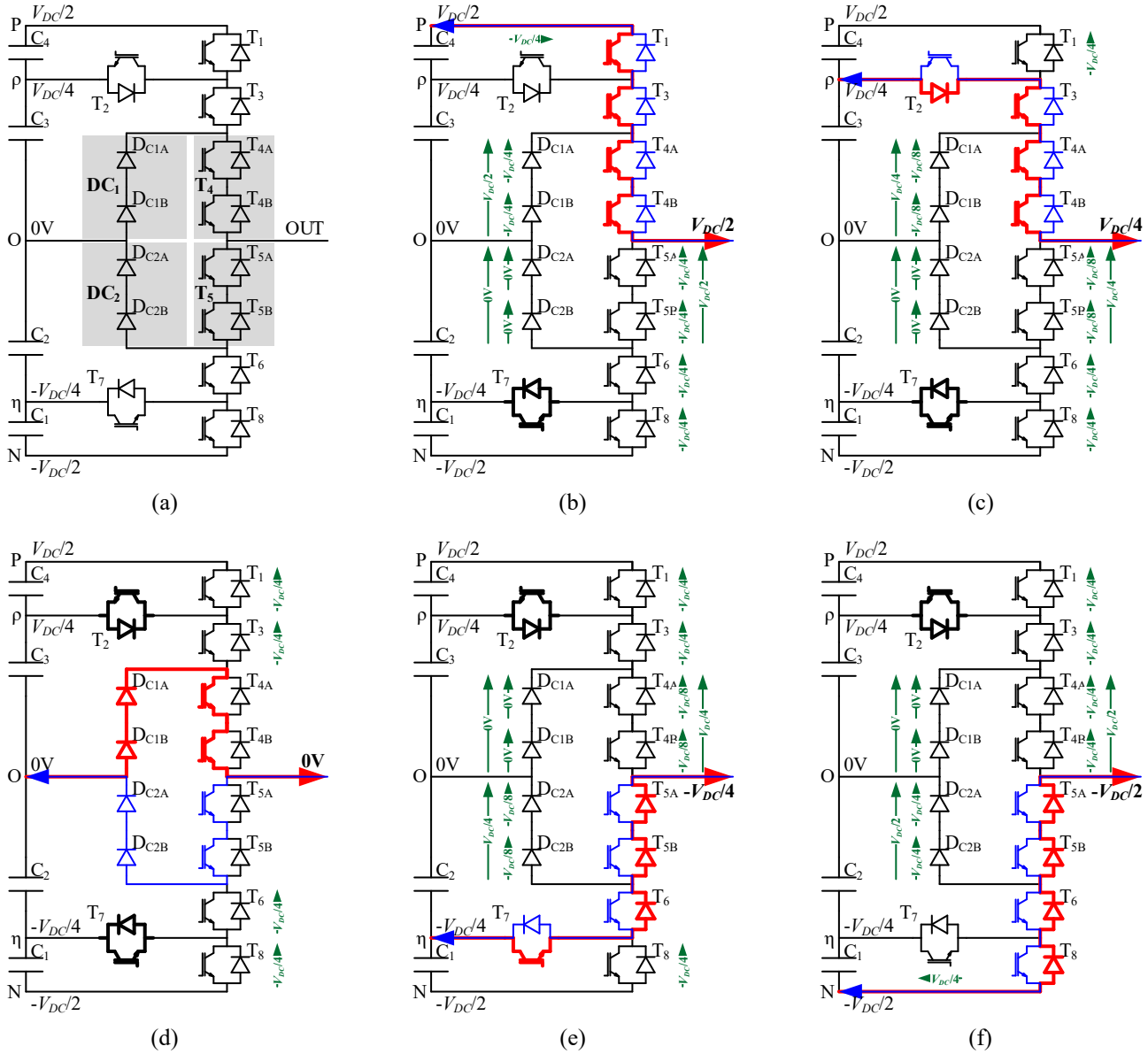


Fig. 2. 5L-MPC phase current circulation (i_{ph} > 0 A: red; i_{ph} < 0 A: blue) and blocking voltages (green) distribution for different switching states. (a) 5L-MPC phase scheme. (b) V_{out} = V_{DC}/2. (c) V_{out} = V_{DC}/4. (d) V_{out} = 0V. (e) V_{out} = -V_{DC}/4. (f) V_{out} = -V_{DC}/2.

when the converter synthetizes an output voltage of V_{DC}/2 or -V_{DC}/2 they must block a voltage of V_{DC}/2, Fig. 2(b) and Fig. 2(f) respectively. However, when the converter is switching between V_{DC}/4, 0V and -V_{DC}/4, inner switches (T_4 and T_5) and clamp diodes (D_{C1} and D_{C2}), operate under hard switching conditions but they only block a voltage of V_{DC}/4, Fig. 2(c)-(e). Therefore, the series connection of these semiconductors is not necessary in these switching states.

It is important to note that during their active switching operation, none of these series-connected devices requires additional circuitry to achieve a proper voltage balance since the series-connected devices are switching the half of their rated voltage. This facilitates the adoption of simple and effective solutions for their series connection. It can be said that the adopted solution must, basically, achieve a proper voltage balance between the series-connected devices during their blocking state and, if possible, proper switching losses balance during their operation under hard switching conditions.

III. Proposed Solution for the Proper Operation of the Series-Connected IGBTs

The proposed solution for the proper operation of the series-connected IGBTs is based on two ideas: the control of the switching commands to achieve proper switching losses balance and the use of additional circuitry to achieve proper voltage balance during their blocking state, Fig. 3. This section describes the solution and the design criteria followed in the real converter [8] (6.6 kV, 1.5MW 5L-MPC with V_{DC} = 11.2 kV and $i_{ph,rms,1,nom}$ = 133 A).

A. *Control of the switching commands*

In order to achieve proper switching loss balance between the series-connected IGBTs, during the switching period, one IGBT is switched on before the other IGBT and the same IGBT is switched off before the other IGBT, Fig. 4. This delay is applied by the switching manager (see Fig. 3), which receives the gate order (g_T) from the modulator, no matter the used modulation technique. With g_T, the switching manager alternatively distributes the power losses among the two series-connected devices (g_{TA}, g_{TB}), applying the delay.

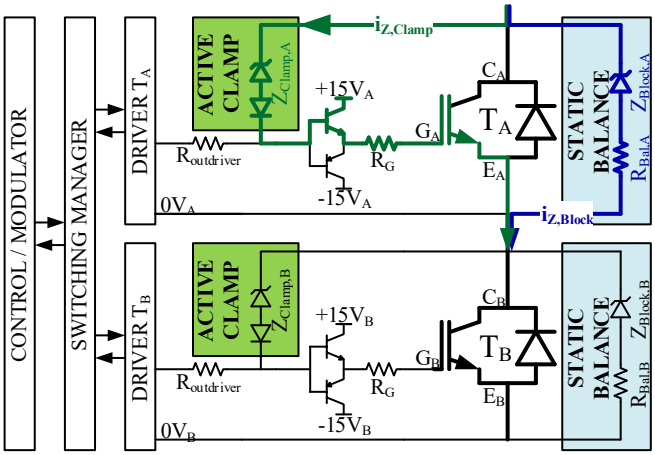


Fig. 3. Proposed switching command manager and voltage balancing circuits.

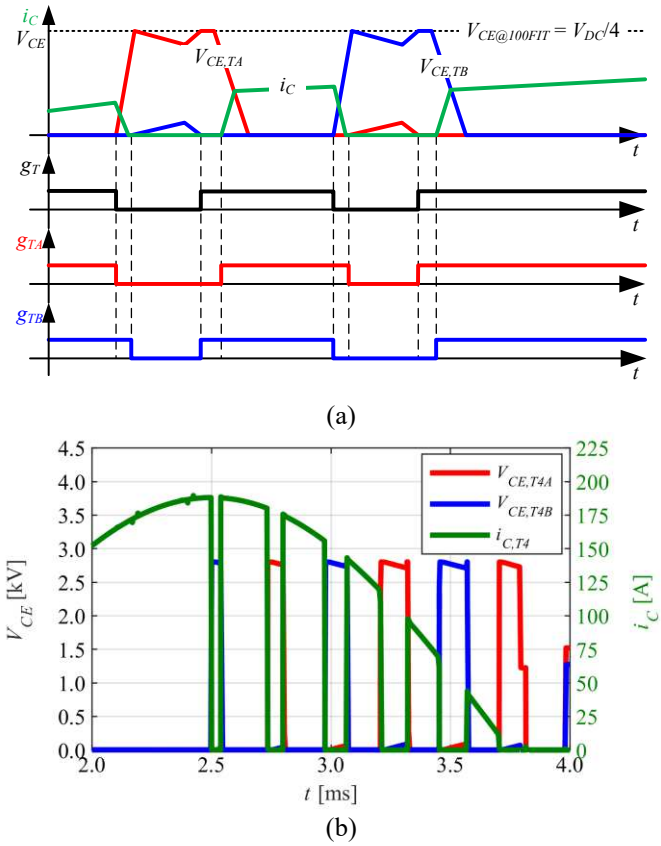


Fig. 4. Ideal switching waveforms of the command control. (a) Theoretical waveforms, where g_T represents gate command of the modulator and g_{TA}-g_{TB} represent the gate orders of the series-connected IGBTs (see Fig. 3). (b) Simulation waveforms at V_{DC} = 11.2 kV and $i_{ph,rms,1}$ = 133 A.

Two cases (switch on and switch off) need to be distinguished in order to know which semiconductor dissipates the switching power losses:

- The switch on losses of the first IGBT are zero while the second IGBT dissipates all the turn on losses.
- During the switch off process, the first IGBT dissipates all the switch off energy while the switch off losses of the second IGBT are zero.

In the next switching period the delays are inversely applied to the series-connected IGBTs to achieve a reasonably good switching losses balance.

B. *Voltage Clamp*

The voltage balancing circuit has two parts: an active voltage clamp ($V_{th,Z,Clamp}$) and a static voltage balancer ($V_{th,Z,Block}$), Fig. 3. Fig. 5 shows the voltage thresholds defined by the active clamp and the voltage balancer.

The ideal behavior during the blocking state is shown in Fig. 5. In this situation, a reasonably good voltage balance between the series-connected IGBTs is achieved without the influence of the external circuit, both of them below the 100 FIT collector emitter voltage ($V_{CE@100FIT}$).

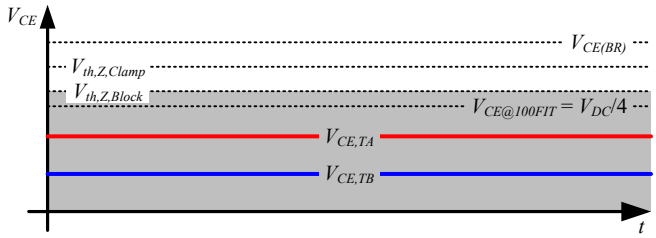


Fig. 5. Proposed voltage thresholds and natural collector-emitter V_{CE} voltage balance of series-connected IGBTs ($V_{CE,TA} < V_{th,Z,Block}$, $V_{CE,TB} < V_{th,Z,Block}$).

However, due to leakage current differences one IGBT could tend to block more voltage than the other. In this case, the static voltage balancer ($i_{Z,Block}$, Fig. 3) should clamp the maximum voltage of the IGBT with lower leakage current, Fig. 6.

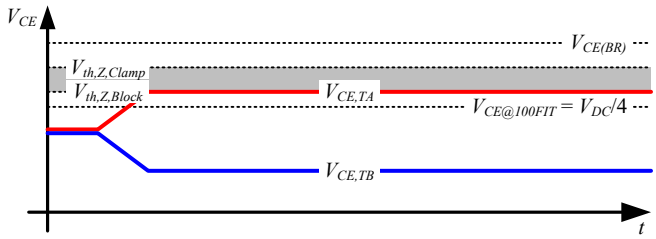


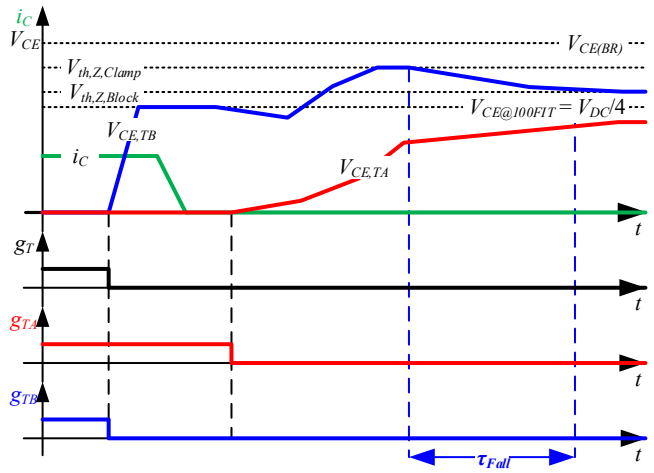
Fig. 6. Influence of the static voltage balancer ($V_{CE,TA} > V_{th,Z,Block}$).

Fig. 7 shows the voltage waveforms when the total blocking voltage increases from V_{DC}/4 to V_{DC}/2. Initially, when the total blocking voltage is V_{DC}/4, in the worst case, one IGBT is blocking approximately V_{DC}/4 while the second IGBT is close to 0V. The output capacitance of the IGBT with higher V_{CE} collector-emitter voltage is lower than the output capacitance of the IGBT with lower voltage. For this reason, when the blocking voltage passes from V_{DC}/4 to V_{DC}/2 the initial voltage slopes of the IGBTs are different, Fig. 7.

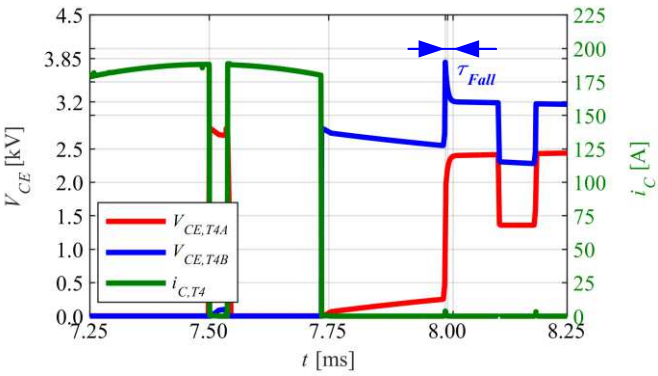
If the collector-emitter voltage of one IGBT exceeds $V_{th,Z,Block}$, the static voltage balancer injects an extra current to charge the output capacitance of the IGBT with lower voltage. Thus the collector-emitter voltage slope of the IGBT with higher voltage is reduced.

When the collector-emitter voltage of one IGBT exceeds the $V_{th,Z,Clamp}$ voltage, the active clamp circuit limits the maximum collector voltage injecting the required gate current ($i_{Z,Clamp}$, Fig. 3). During this time interval, the influence of the current injected by the static balancer can be neglected.

After the active clamping period, the static voltage balancer circuit must reduce the V_{CE} voltage from $V_{th,Z,Clamp}$ to $V_{th,Z,Block}$, Fig. 7. The time required by the static voltage balancer circuit to reach the $V_{th,Z,Block}$ voltage (τ_{Fall}, Fig. 7a and Fig. 7b) depends on the equivalent output capacitance of the IGBT and the R_{Bal} resistor.



(a)



(b)

Fig. 7. Ideal IGBT switching waveforms with the voltage balance. (a) Theoretical waveforms, (b) Simulation waveforms, with V_{DC} = 11.2 kV, $V_{th,Z,Block}$ = 3200 V and $V_{th,Z,Clamp}$ = 3850 V.

In the case of the clamping diodes, there is no IGBT to control the balance of the switching losses. The switching losses balance depends on the unmatched recovery behavior of the series-connected diodes. When the pair of diodes are switching a total voltage of $V_{DC}/4$, there is no risk to exceed the rated voltage of the diodes, Fig. 8.

When the blocking voltage increases up to $V_{DC}/2$, the same active voltage clamp and voltage balancer circuits protect the diodes from excessive overvoltages, Fig. 9.

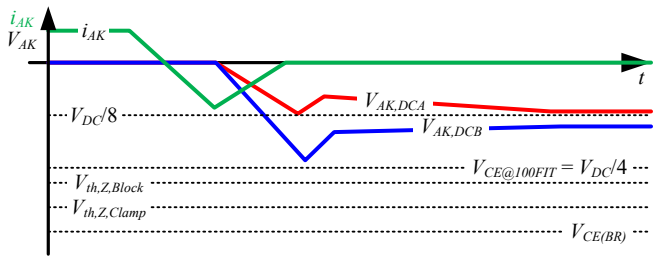


Fig. 8. Ideal diode switching waveforms with the voltage balance the control proposal, $V_{AK,DCA} + V_{AK,DCB} = V_{DC}/4$.

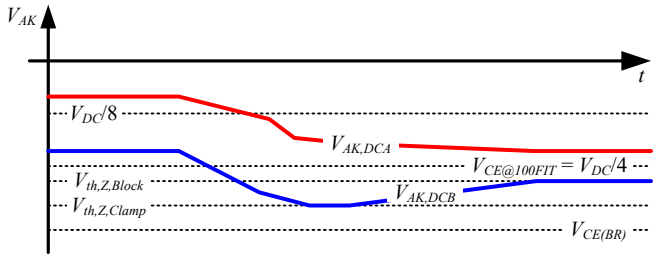


Fig. 9. Ideal diode switching waveforms with the voltage balance, $V_{AK,DCA} + V_{AK,DCB} = V_{DC}/2$.

C. *Design criteria for the proposed solution*

The delay time between the switching commands must guarantee that the first IGBT is completely in the on / off state, before the second IGBT receives the on / off switching command. This is the only mandatory condition. In the presented solution, during the turn on process of the second IGBT the dead time is applied. As the dead time is larger than the total switch on time, only the switch off time must be measured to define the delay time.

The active clamp should not work under nominal hard switching conditions to avoid the increase of the switch off losses in the IGBT. In consequence, the V_{CE} overvoltage must be measured during the switch off process of the IGBT at nominal current. Then, the threshold voltage of the active clamp circuit ($V_{th,Z,Clamp}$) is set at a voltage slightly higher than the measured V_{CE} overvoltage.

It should be noted that the Transient Voltage Suppressor (TVS) used for Z_{Clamp} in the the active clamp circuit has a large dynamic resistor ($r_{d,Z,Clamp}$) and therefore, the real V_{CE} voltage will exceed the $V_{th,Z,Clamp}$ voltage,

$$V_{CE,max} = V_{th,Z,Clamp} + I_{Z,Clamp} \cdot r_{d,Z,Clamp}. \quad (1)$$

In order to protect the IGBT properly, a low value of $V_{th,Z,Clamp}$ is required. To do this, the V_{CE} overvoltage must be reduced and in consequence, a low leakeage inductance in the bus-bar results mandatory.

The threshold voltage of the static voltage balancer circuit ($V_{th,Z,Block}$) is slightly higher than the nominal blocking voltage ($V_{DC}/4$) of the IGBT to avoid unnecessary power losses in the circuit.

The value of blocking circuit resistance R_{Bal} depends on several factors. A high value of R_{Bal} is necessary to reduce the power losses in the static voltage balancer during the turn off process of the IGBT. The overvoltage in the IGBT terminals activates the static voltage balancer and the power losses in the circuit are strongly dependant on R_{Bal}. However, a too large

value of R_{Bal} increases the voltage drop caused by the current in this resistor ($\Delta i_{leakage}$) and in consequence, the blocking voltage of the IGBT with lower leakage current. In addition, R_{Bal} and the output equivalent capacitance of the IGBT defines the time constant of the voltage fall from $V_{th,Z,Clamp}$ to $V_{th,Z,Block}$ (τ_{Fall}, Fig. 7a and Fig. 7b). In consequence, a trade-off must be made between power losses, maximum blocking voltage and the time constant.

IV. Experimental Results

The proposed solution has been experimentally validated in a 1.5 MW back-to-back 5L-MPC converter (V_{DC} = 11.2 kV, $V_{out,ll,rms,1}$ = 6.6 kV, $i_{out,ph,rms,1}$ = 133 A, Fig. 10). As the influence of the command delay control, the active clamp circuit and the static voltage balancer can be only evaluated in the IGBT, this section is focused on the IGBT behaviour in the converter. The converter configuration and the modulation scheme for the DC-link voltage balance have been proposed in [7]. Table II summarizes the parameters of the experimental setup.

TABLE II
Experimental Test Bench Parameters

Parameter	Value
DC-link rated voltage ($V_{DC,nom}$)	11.2 kV
Rated output voltage ($V_{out,ll,rms,1,nom}$)	6.6 kV
Rated output current ($i_{out,ph,rms,1,nom}$)	133 A
Semiconductors switching frequency (f_{sw})	1 kHz
IGBTs minimum conduction time ($t_{on,min}$)	8 µs
IGBTs dead time (t_{DT})	5 µs
Delay Time between series IGBTs (t_{delay})	2 µs
Collector-Emitter Breakdown Voltage ($V_{CE(BR)}$)	4500 V
DC Collector Current (I_c)	150 A
Static Balancer Threshold Voltage ($V_{th,Z,Block}$)	3200 V
Static Balancer Resistor (R_{Bal})	2 kΩ (10 W)
Active Clamp Threshold Voltage ($V_{th,Z,Clamp}$)	3850 V

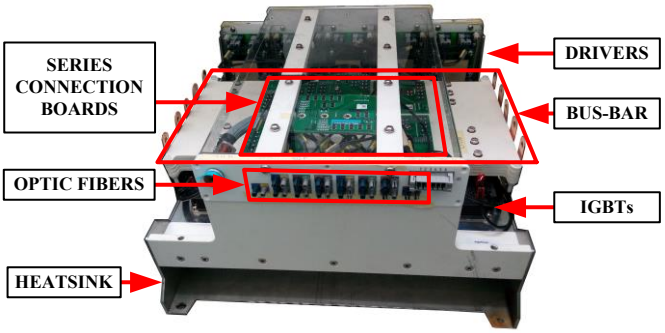
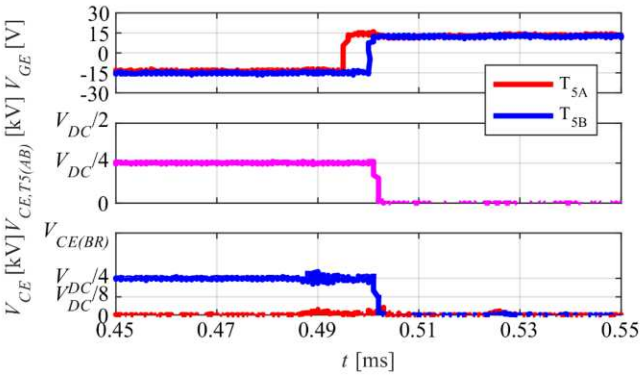


Fig. 10. Developed phase power stack.

As described in [7], each 5L-MPC phase branch is composed of ten 4.5 kV/150 A IGBT modules, which are indistinctly used as IGBT-diode pairs and clamping diodes, D_{C1} and D_{C2}. The voltage balancing circuits are connected to the series-connected devices D_{C1}, D_{C2}, T_3, T_4, T_5 and T_6, Fig. 2. Considering the output capacitance of the IGBT and the R_{Bal} resistor, the V_{CE} voltage requires about 7 µs to converge to $V_{th,Z,Block}$ from $V_{th,Z,Clamp}$. Considering the dynamic resistance of the used TVS devices, V_{CE} voltages up to 4300 V are expected in the worst case scenario. This voltage is quite close from the breakdown voltage of the IGBT/Diodes. However, the large leakage inductance in the bus-bar (up to 800 nH) makes no possible the reduction of the $V_{th,Z,Clamp}$ voltage. The total power losses in each auxiliary circuit is less than 10 W.



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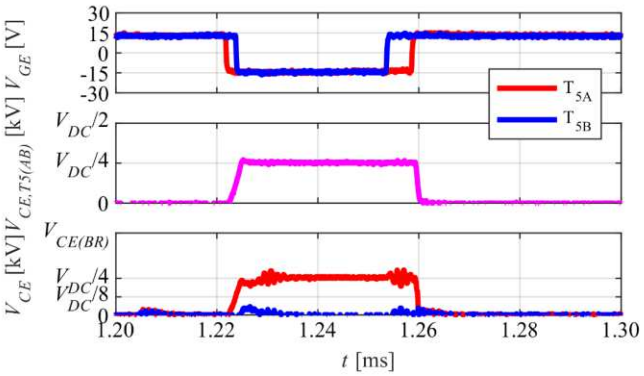

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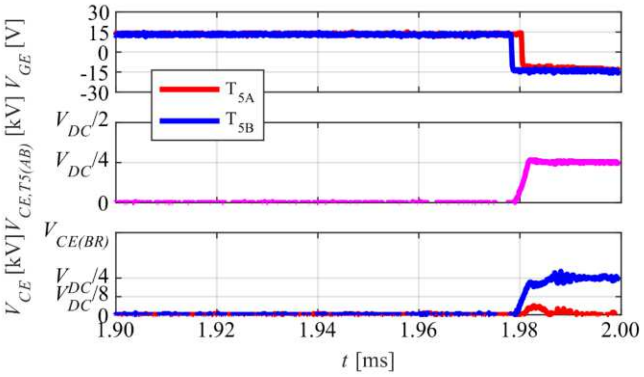

(c)

Fig. 11. Experimentally measured gate-emitter voltages (V_{GE}), total blocking voltage ($V_{CE,T5(AB)}$) and collector-emitter voltages (V_{CE}) during a switching losses distribution sequence, with V_{DC} = 8 kV and cosφ = 0. (a) T_{5B} assumes the switch-on losses. (b) T_{5A} assumes the switch-off losses and switch-on losses consecutively. (c) T_{5B} assumes the switch-off losses.

A. *Control of the switching commands*

Fig. 11 shows the individual switching commands, the total switched voltage and the individual collector voltages of the series-connected T_{5A} and T_{5B} IGBTs. Fig. 11a shows a switch

on process in which T_{5A} is turned on before T_{5B}. As the current cannot circulate until both of them are in the on state, T_{5B} dissipates all the turn on energy.

Fig. 11b shows that T_{5A} is switched off before T_{5B}. In this case, the circulating current is interrumpted by T_{5A}; thus, all the switch off energy is disipated by this IGBT. Fig. 11b also shows that during the next switch on process, T_{5A} is turned on later than T_{5B}; thus T_{5A} dissipates now all the turn on energy. It is important to note that the effective turn on delay between series-connected IGBTs is larger in this case because the dead time (t_{DT}) is applied between the two turn on commands. Finally, Fig. 11c shows the next switch off process, in which T_{5B} assumes the turn off energy losses.

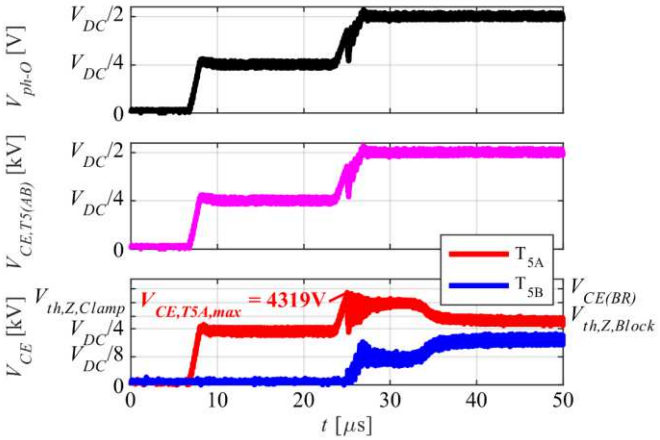

Fig. 12. Experimentally measured phase voltage ($V_{ph\text{-}O}$), total blocking voltage ($V_{CE,T5(AB)}$) and collector-emitter voltages (V_{CE}),with static voltage balancer circuit actuation during a blocking voltage transition from $V_{CE,T5(AB)} \approx V_{DC}/4$ to $V_{CE,T5(AB)} = V_{DC}/2$, with V_{DC} = 11 kV, cosφ = 0.88, $V_{th,Z,Block} \approx$ 3200 V and $V_{th,Z,Clamp} \approx$ 3850 V.

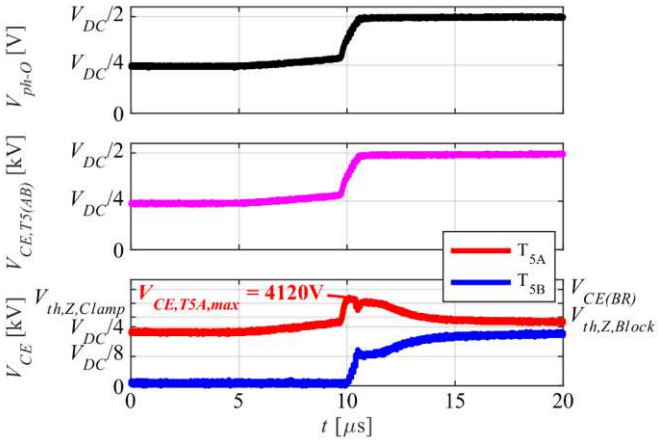

Fig. 13. Experimentally measured phase voltage ($V_{ph\text{-}O}$), total blocking voltage ($V_{CE,T5(AB)}$) and collector-emitter voltages (V_{CE}),with active clamping circuit actuation during a blocking voltage transition from $V_{CE,T5(AB)} \approx V_{DC}/4$ to $V_{CE,T5(AB)} = V_{DC}/2$, with V_{DC} = 11 kV, cosφ = 0, $V_{th,Z,Block} \approx$ 3200 V and $V_{th,Z,Clamp} \approx$ 3850 V.

B. *Voltage clamp*

Fig. 12 (cosφ = 0.88) and Fig. 13 (cosφ = 0) show the phase voltage ($V_{ph\text{-}O}$) and the V_{CE} voltages of the T_{5A}-T_{5B} IGBTs with V_{DC} = 11 kV ($V_{DC}/4$ = 2.75 kV). The phase voltage ($V_{ph\text{-}O}$) changes from 0V to $V_{DC}/4$ and $V_{DC}/2$. This phase voltage is the voltage that must be blocked by the series-connected T_{5A}-T_{5B} IGBTs ($V_{CE,T5(AB)}$). In this transition from 0V to $V_{DC}/4$ (Fig. 12), T_{5A} assumes the total blocking voltage because it is turned off before T_{5B}. When the total blocking voltage increases to $V_{DC}/2$ (Fig. 12 and Fig. 13) the auxiliary circuits protect T_{5A} limiting its maximum V_{CE} voltage. As expected, after the active clamping period, its V_{CE} voltage reaches the $V_{th,Z,Block}$ voltage.

It can be observed that during the transient the achieved maximum V_{CE} voltage is considerably higher than the $V_{th,Z,Clamp}$ voltage due to the dynamic resistor of the TVS. As described previously, in the worst case scenario, the maximum V_{CE} voltage is about 4.3 kV.

Finally, Fig. 14 shows the phase voltage during a fundamental period of the output voltage. In addition, the total blocking voltage of the series-connected IGBTs is shown. The influence of the alternating switching commands on the power loss distribution and the influence of the auxiliary circuits can be observed.

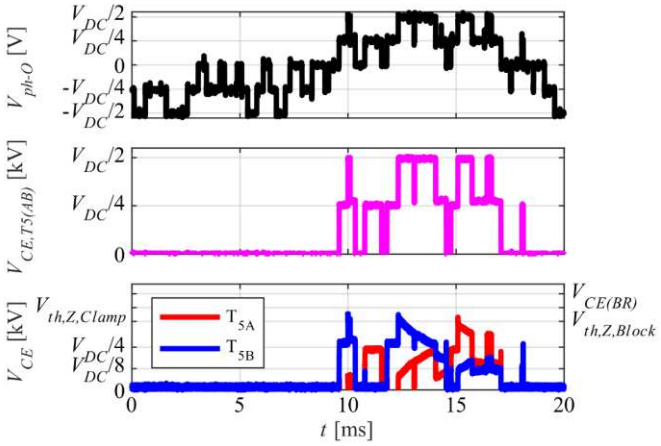

Fig. 14. Experimentally measured phase voltage ($V_{ph\text{-}O}$), total blocking voltage ($V_{CE,T5(AB)}$) and collector-emitter voltages (V_{CE}), with static voltage balancer circuit actuation during a fundamental period of the output voltage, with V_{DC} = 8 kV, cosφ = 0, $V_{th,Z,Block} \approx$ 3200 V and $V_{th,Z,Clamp} \approx$ 3850 V.

V. Conclusion

This paper presents an easy and reliable solution for the voltage balance problem of the series-connected IGBT/Diodes in the 5L-MPC converter.

It is important to note that during the hard switching process these devices can operate as non-series-connected devices. Therefore, solutions to deal with asynchronous switchings and differences in tail and recovery currents are not necessary. This simplifies the problem related to the series connection of switching devices. The proposed solution can be applied to any other multilevel topology in which the series-connected devices need to block twice their switched voltage (5L-SMC, T-Type…).

Basically, the proposed solution consist of the control of the switching commands to achieve a proper switching loss balance and the use of clamp circuits to protect the devices during the off state.

The proposed method has been experimentally evaluated and very promising results have been obtained. Hard switchings have been controlled by the gate command delays and active

clamping and static balancer circuits have properly protected the devices.

VI. References

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L.G. Franquelo, B. Wu, J. Rodriguez, M.A. Perez and J.I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. On Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[2] S. Kouro, J. Rodriguez, Bin Wu, S. Bernet, and M. Perez, "Powering the Future of Industry: High-Power Adjustable Speed Drive Topologies," *IEEE Ind. Appl. Mag.*, vol. 18, no. 4, pp. 26–39, Aug. 2012.

[3] A. Sanchez-Ruiz, M. Mazuela, S. Alvarez, G. Abad, and I. Baraia, "Medium Voltage–High Power Converter Topologies Comparison Procedure, for a 6.6 kV Drive Application Using 4.5 kV IGBT Modules," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1462–1476, Mar. 2012.

[4] H. Abu-Rub, S. Bayhan, S. Moinoddin, M. Malinowski, and J. Guzinski, "Medium-Voltage Drives: Challenges and existing technology," *IEEE Power Electron. Mag.*, vol. 3, no. 2, pp. 29–41, Jun. 2016.

[5] J. Rodriguez, Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[6] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Limits of the neutral-point balance in back-to-back-connected three-level converters," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 722–731, May 2004.

[7] M. Mazuela, I. Baraia, A. Sanchez-Ruiz, I. Echeverria, I. Torre, and I. Atutxa, "DC-Link Voltage Balancing Strategy Based on SVM and Reactive Power Exchange for a 5L-MPC Back-to-Back Converter for Medium-Voltage Drives," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7864–7875, Dec. 2016.

[8] J. A. Sayago, T. Bruckner, and S. Bernet, "How to Select the System Voltage of MV Drives—A Comparison of Semiconductor Expenses," *IEEE Trans. Ind. Electron.*, vol. 55, no. 9, pp. 3381–3390, Sep. 2008.

[9] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[10] F. Kieferndorf, M. Basler, L. A. Serpa, J. H. Fabian, A. Coccia, and G. A. Scheuer, "A new medium voltage drive system based on ANPC-5L technology," in *2010 IEEE International Conference on Industrial Technology*, 2010, pp. 643–649.

[11] I. Baraia, J. A. Barrena, G. Abad, J. M. Canales Segade, and U. Iraola, "An Experimentally Verified Active Gate Control Method for the Series Connection of IGBT/Diodes," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 1025–1038, Feb. 2012.

[12] I. Baraia, I. Atutxa, S. Alvarez, and M. Mazuela, "Analysis and experimental evaluation of two low loss auxiliary circuits for the series connection of IGBT devices," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10.

[13] Ju Won Baek, Dong-Wook Yoo, and Heung-Geun Kim, "High-voltage switch using series-connected IGBTs with simple auxiliary circuit," *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1832–1839, Dec. 2001.

[14] R. Roesner, J. Holtz, and R. Kennel, "Cellular driver/snubber scheme for series connection of IGCTs," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, 2001, vol. 2, pp. 637–641 vol.2.

[15] N. Y. A. Shammas, R. Withanage, and D. Chamund, "Review of series and parallel connection of IGBTs," *IEE Proc. - Circuits Devices Syst.*, vol. 153, no. 1, pp. 34–39, Feb. 2006.

[16] F. Zhang, X. Yang, Y. Ren, L. Feng, W. Chen, and Y. Pei, "A Hybrid Active Gate Drive for Switching Loss Reduction and Voltage Balancing of Series-Connected IGBTs," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7469–7481, Oct. 2017.

[17] Soonwook Hong, Venkatesh Chitta, and D. A. Torrey, "Series connection of IGBT's with active voltage balancing," *IEEE Trans. Ind. Appl.*, vol. 35, no. 4, pp. 917–923, Aug. 1999.

[18] A. Petterteig, J. Lode, and T. M. Undeland, "IGBT turn-off losses for hard switching and with capacitive snubbers," in *Conference Record of the 1991 IEEE Industry Applications Society Annual Meeting*, 1991, pp. 1501–1507 vol.2.

[19] P. R. Palmer and A. N. Githiari, "The series connection of IGBTs with active voltage sharing," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 637–644, Jul. 1997.

[20] D. G. Holmes and B. P. McGrath, "Opportunities for harmonic cancellation with carrier-based PWM for a two-level and multilevel cascaded inverters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 574–582, Apr. 2001.

[21] J. A. Barrena, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, "Individual Voltage Balancing Strategy for PWM Cascaded H-Bridge Converter-Based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 21–29, Jan. 2008.

[22] A. Sanchez-Ruiz, G. Abad, I. Echeverria, I. Torre, and I. Atutxa, "Continuous Phase-Shifted Selective Harmonic Elimination and DC-Link Voltage Balance Solution for H-bridge Multilevel Configurations, Applied to 5L HNPC," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2533–2545, Apr. 2017.

[23] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, 1992, pp. 397–403 vol.1.

[24] P. Barbosa, P. Steimer, L. Meysenc, M. Winkelnkemper, J. Steinke, and N. Celanovic, "Active Neutral-Point-Clamped Multilevel Converters," in *2005 IEEE 36th Power Electronics Specialists Conference*, 2005, pp. 2296–2301.

[25] G. Gateau, M. Fadel, P. Maussion, R. Bensaid, and T. A. Meynard, "Multicell converters: active control and observation of flying-capacitor voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 998–1008, Oct. 2002.

[26] V. Guennegues, B. Gollentz, F. Meibody-Tabar, S. Rael, and L. Leclere, "A converter topology for high speed motor drive applications," in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–8.

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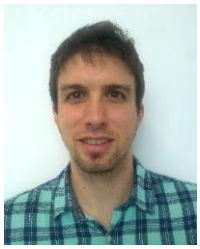

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