Analytical Model of the Current Stress in Active-Bridge Active-Clamp Converter for More Electric Aircraft

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***Abstract*—Nowadays, the emergence of electrically supplied actuators and energy storage systems is leading the aeronautic industry to develop aircrafts with more electrical power installed. Therefore, different Power-Electronic Converters (PECs) have been proposed to satisfy the requirements of More Electric Aircraft (MEA) applications. Among them Active-Bridge-Active-Clamp converter is one of the most promising isolated DC/DC PEC topologies. To expand the characterization of this PEC, the analytical model to determine the root mean square and average currents in secondary power devices is presented in this work when working with single-phase shift rectangular modulation. Furthermore, a simulation model is developed in PLECS to validate the analytical model proposed in this work in MEA scenarios. Finally, the simulation model is employed to determine the error caused by dead time and clamp capacitances in the currents that are calculated analytically.**

***Index Terms*—DC-DC Power Conversion, Active-Bridge-Active-Clamp, Analytical Modelling, More Electric Aircraft.**

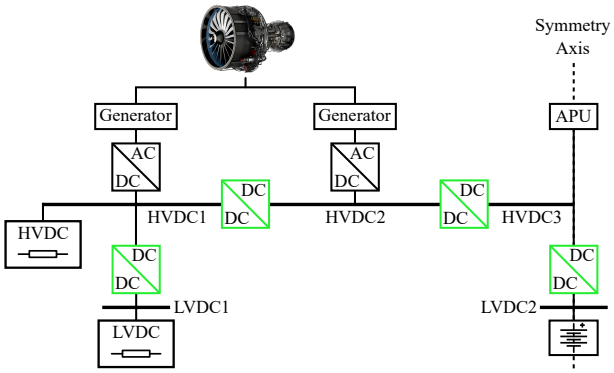


Fig. 1. Distributed electric power distribution network in MEA. The ilustration is focused on the DC distribution network for hybrid and electric aircraft.

I. Introduction

In last years, the electrification of the aircraft has experienced a large increment in R&D effort. The aim is to reduce the enviromental impact and to improve passenger safety and comfort. Bidirectional isolated DC/DC Power Electronic Converters (PECs) play an important role in new electric power distribution networks proposed for More Electric Aircraft (MEA) [1]. In MEA electric power distribution networks, these DC/DC PECs are mainly found in energy storage systems and/or power flow regulation among DC buses, as shown in Fig. 1. In this context, Dual-Active-Bridge (DAB) converter, first presented in [2], has been studied in literature considering different modulation methods [3] and switches thermal behavior [4]. However, main disadvantage of DAB converter is the required large capacitance to satisfy the low voltage ripple requirement in some MEA applications (e.g. interfacing High Voltage DC (HVDC) and Low Voltage DC (LVDC) buses).

As an alternative to DAB, Active-Bridge-Active-Clamp (ABAC) converter has been proposed to solve this issue [5]. In this converter, the secondary stage is modified by including clamp capacitances and output inductances. Since secondary half-bridge branches work at 50 % of duty cycle and are complementary switched, these inductances are in phase oposition, and thus the resulting ripple on the LVDC bus is cancelled. DAB and ABAC converters have been compared in literature in terms of volume, weight and efficiency [6], [7]. Furthermore, ABAC converter has been studied considering advanced modulation methods, as trapezoidal or triangular modulations [8], [9], which improve the converter performance when working outside nominal input and/or output voltage at low power transfer. Moreover, the influence of the mismatch of different design parameters on the output characteristics, as current sharing or voltage ripple cancelation, can be found in literature [10]. The behavior of the primary stage in ABAC is the same as in DAB, whose analytical model for the current stress has been developed in [11] for different modulation methods. Therefore, the analytical model of the currents in the secondary stage of ABAC converter is presented in this work. Based on these equations, the current stress in the switching devices can be compared in any case study. Moreover, these equations are useful in the sizing of switching devices and cooling system.

This work is organized as follows. The working principle

of ABAC converter when working with Single-Phase Shift (SPS) rectangular modulation is exposed in section II. In section III, the validation of the proposed analytical model is carried out by developing a simulation model in PLECs. Moreover, the relative error considering clamp capacitances and dead time variations is calculated in this section. Finally, main conclusions of this work are gathered in section IV. In the appendix, the analytical model of the Root Mean Square (RMS) and Average (AVG) currents is presented.

II. SPS Rectangular Modulation in ABAC Converter

The schematic of ABAC converter is shown in Fig. 2. It is formed by a full-bridge in the primary stage and two half-bridge branches in the secondary side, which can act as inverter and/or rectifier connected through an isolation transformer. Semiconductors $S_1 - S_4$ and $D_1 - D_4$ connect the primary side of the transformer with the HVDC bus, while the secondary side is connected through $S_5 - S_8$ and $D_5 - D_8$ to the clamp capacitances (C_c) and the output inductances (L_{out}). These output inductances act as interface between the secondary half-bridges and the LVDC bus.

Among the different modulation methods that can be implemented on this topology, SPS rectangular modulation is the simplest and the most commonly used. Therefore, the analytical model of the RMS and AVG currents in secondary switching devices of ABAC converter when working with this modulation method is presented in this section.

In Fig. 3, voltage waveforms in primary (v_1) and secondary (v_2) windings of the power transformer togheter with current waveform through the decoupling inductor ($i_{L\sigma}$) are depicted. Furthermore, the current through output inductor (i_{Lout}) is exposed. Looking at the configuration of the secondary side in ABAC converter, RMS and AVG currents in secondary switching devices depend on the currents that flow throught the secondary winding of the power transformer and through the output inductors. After applying Kirchhoff current law in nodes X and Y (see Fig. 2), the current distribution in the power devices of this stage is obtained. Moreover, the current through topside (S_{5-7} and D_{5-7}) and bottomside (S_{6-8} and D_{6-8}) semiconductors is not the same, as it is shown in Fig. 3. In order to characterize the RMS and AVG current stress in

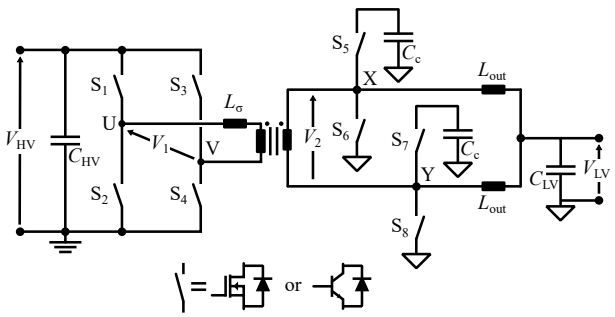


Fig. 2. Bidirectional isolated DC/DC ABAC converter for MEA.

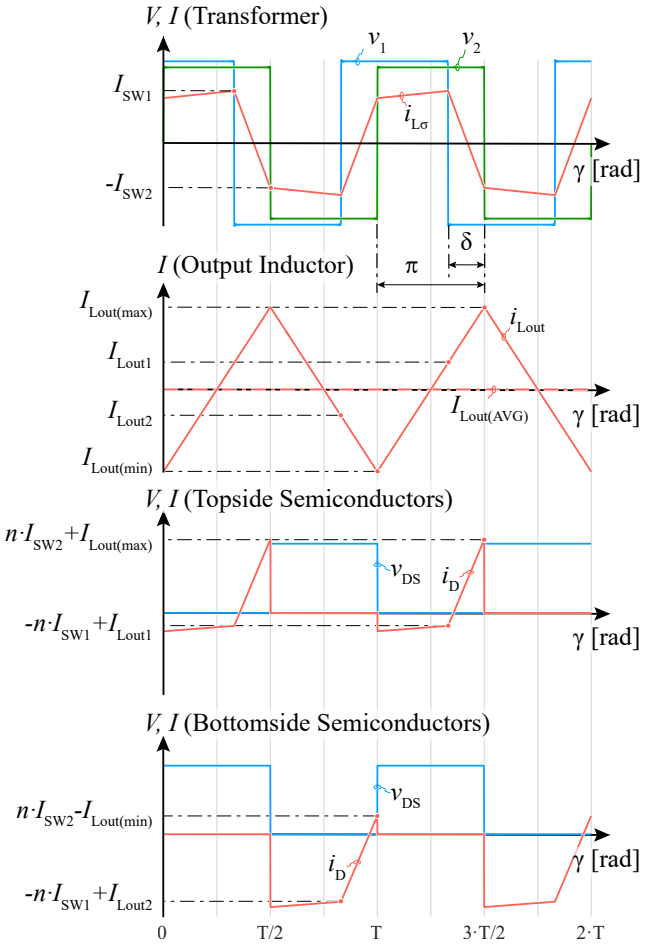


Fig. 3. Main waveforms in secondary side of ABAC converter under SPS rectangular modulation. From top to bottom: Voltage in primary (v_1) and secondary (v_2) windings of the power transformer and current through decoupling inductor ($i_{L\sigma}$), current through output inductor (i_{Lout}), and blocking voltage (v_{DS}) and drain current (i_D) in topside semiconductors (S_{5-7} and D_{5-7}), and in bottomside semiconductors (S_{6-8} and D_{6-8}). These waveforms are obtained assuming ideal clamp capacitors.

these devices, the current levels at $(\pi - \delta)$ and switching instants are defined as A,B,C,D in (1) and (3) to simplify the mathematical development of this work:

$$A = (I_{\mathrm{Lout(max)}} + n\, I_{\mathrm{sw2}}) \ , \tag{1}$$

$$B = (I_{\mathrm{Lout(min)}} - n\, I_{\mathrm{sw2}}) \ , \tag{2}$$

$$C = (I_{\mathrm{Lout1}} - n\, I_{sw1}) \ , \tag{3}$$

$$D = (I_{\mathrm{Lout2}} + n\, I_{\mathrm{sw1}}) \ , \tag{4}$$

where n is the transformer turns ratio, I_{sw1} and I_{sw2} are the current values in the primary winding of the power transformer at switching instant of primary and secondary power devices, $I_{\mathrm{Lout(max)}}$ and $I_{\mathrm{Lout(min)}}$ are the maximum and minimum

current values in the output inductance, and I_{Lout1} and I_{Lout2} are the current in the output inductance at switching instant in primary side. The equations to determine these currents are presented in (5)-(10):

$$I_{\mathrm{sw1}} = \frac{V_{\mathrm{HV}}\,\pi + n\,V_{\mathrm{Clamp}}\,(2\,|\delta| - \pi)}{4\,\pi\,f_{\mathrm{sw}}\,L_{\sigma}}\ , \tag{5}$$

$$I_{\mathrm{sw2}} = \frac{V_{\mathrm{HV}}\,(2\,|\delta| - \pi) + n\,V_{\mathrm{Clamp}}\,\pi}{4\,\pi\,f_{\mathrm{sw}}\,L_{\sigma}}\ , \tag{6}$$

$$I_{\mathrm{Lout(max)}} = I_{\mathrm{Lout(AVG)}} + 0.5\,\Delta I_{\mathrm{Lout(pk-pk)}}\ , \tag{7}$$

$$I_{\mathrm{Lout(min)}} = I_{\mathrm{Lout(AVG)}} - 0.5\,\Delta I_{\mathrm{Lout(pk-pk)}}\ , \tag{8}$$

$$I_{\mathrm{Lout1}} = I_{\mathrm{Lout(min)}} + \frac{\left(I_{\mathrm{Lout(max)}} - I_{\mathrm{Lout(min)}}\right)}{\pi}\,(\pi - \delta)\,, \tag{9}$$

$$I_{\mathrm{Lout2}} = I_{\mathrm{Lout(max)}} + \frac{\left(I_{\mathrm{Lout(min)}} - I_{\mathrm{Lout(max)}}\right)}{\pi}\,(\pi - \delta)\,, \tag{10}$$

where V_{HV} is the voltage on the HVDC bus, V_{Clamp} is the voltage on the clamp capacitances ($V_{\mathrm{Clamp}} = 2\,V_{\mathrm{LV}}$), f_{sw} is the switching frequency and L_{σ} is the decoupling inductance. Furthermore, current ripple ratio (r_{I}), peak-to-peak current ripple ($\Delta I_{\mathrm{Lout(pk-pk)}}$) and AVG current ($I_{\mathrm{Lout(AVG)}}$) in the output inductance are defined in (11)-(13):

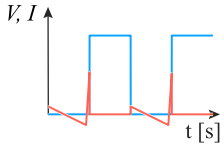
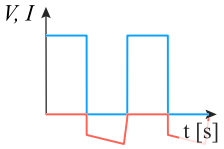
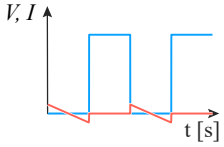
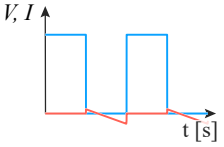
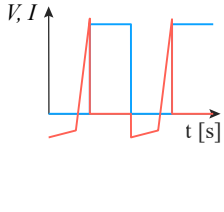
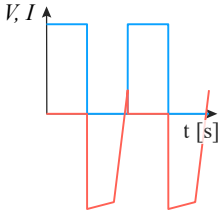
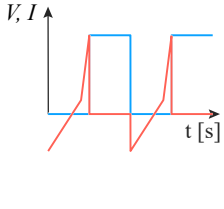
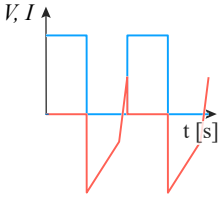
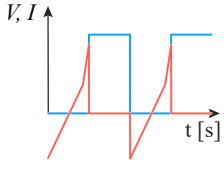
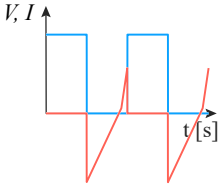
$$I_{\mathrm{Lout(AVG)}} = \frac{P_{\mathrm{out}}}{V_{\mathrm{Clamp}}}, \tag{11}$$

$$\Delta I_{\mathrm{Lout(pk-pk)}} = \frac{V_{\mathrm{LV}}}{2\,L_{\mathrm{out}}\,f_{\mathrm{sw}}}, \tag{12}$$

$$r_{\mathrm{I}} = \frac{\Delta I_{\mathrm{Lout(pk-pk)}}}{I_{\mathrm{Lout(AVG)}}} = \frac{(V_{\mathrm{LV}})^2}{L_{\mathrm{out}}\,f_{\mathrm{sw}}\,P_{\mathrm{out}}}. \tag{13}$$

TABLE I

SUMMARY OF ZVS AND HS CASES, BOUNDARY CONDITIONS AND VOLTAGE AND CURRENT WAVEFORMS IN POWER DEVICES (FORWARD MODE).

Case	**Boundary condition**	v_{DS} **&** i_D **waveforms**	
		S_{5-7} & D_{5-7}	S_{6-8} & D_{6-8}
I a.	$n\,I_{\mathrm{sw2}} - I_{\mathrm{Lout(min)}} \leq 0$		
I b.	$n\,I_{\mathrm{sw2}} + I_{\mathrm{Lout(max)}} \leq 0$		
II a.	$-n\,I_{\mathrm{sw1}} + I_{\mathrm{Lout1}} \geq 0$ & $-n\,I_{\mathrm{sw1}} - I_{\mathrm{Lout2}} \geq 0$		
II b.	$-n\,I_{\mathrm{sw1}} + I_{\mathrm{Lout1}} \geq 0$		
II c.	$-n\,I_{\mathrm{sw1}} - I_{\mathrm{Lout2}} \geq 0$		

Different operating modes are defined for ABAC converter in order to differenciate if the current is flowing through switch or diode. Furthermore, this operating modes describe hard-switching (case I) and zero-voltage-switching (case II), divided in case I a, case I b, case II a, case II b and case II c. These distinctions in case I and case II are done to differenciate whether the current level is possitive or negative at π and $(\pi - \delta)$ instants respectively in topside and bottomside power devices. The corresponding boundary conditions are presented in Table I together with the blocking voltage and drain current waveform of each operating mode.

Then, RMS and AVG current equations are obtained for top-side and bottomside semiconductors in each operating mode. The analytical models of the defined operating modes are presented in Tab. III-VI, which are gathered in the appendix of this work. Furthermore, the required modifications to calculate the RMS and AVG currents in secondary switching devices in backward mode, i.e. LV to HV power transfer, are described in the appendix based on the presented analytical models.

III. Simulation Analysis

To validate the analytical model proposed in this work, a simulation model is developed in PLECS. The design values considered in this work are gathered in Table II based on typical MEA specifications [5]. Furthermore, the values of clamp capacitance and dead time utilized in this section to determine the error when considering non-idealities are also presented.

TABLE II
MEA Design Parameters

Parameter	Value	Units
V_{HV}	270	V
V_{LV}	28	V
n	5	-
P_{out}	10	kW
F_{sw}	100	kHz
L_{σ}	7.56	μH
L_{out}	3	μH
C_{c}	25-300	μF
t_{dt}	50-350	ns

A. Validation based on simulation

In order to simplify the validation procedure, the following assumptions are taken. To idealize the simulation model, dead time in switching devices and conduction losses in passive devices are not considered. Moreover, clamp capacitances are modeled as ideal voltage sources.

In Fig. 4, RMS and AVG currents in topside and bottomside switching devices are depicted in two MEA scenarios, i.e. $V_{\mathrm{LV}} = 22$ V and $V_{\mathrm{LV}} = 29$ V. At high power transfer, higher currents are expected in all semiconductors when working with low voltage in LVDC bus. In topside semiconductors, the current stress is similar in both cases at medium and low power transfer. However, this is not the case of bottomside semiconductors. In these semiconductors, the current level in diodes is higher at 22 V in LVDC bus in the whole output power

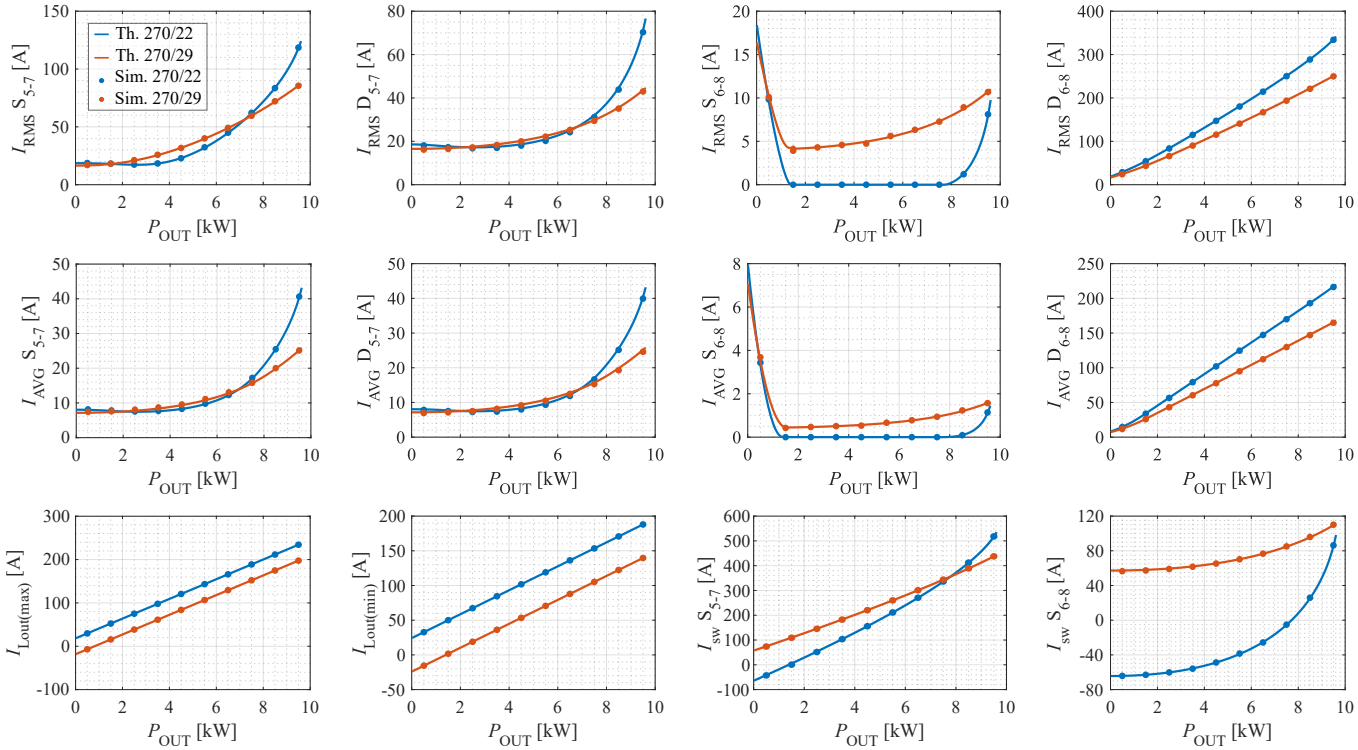


Fig. 4. Switching, RMS and AVG currents in secondary switching devices $\mathrm{S}_5 - \mathrm{S}_8$ and $\mathrm{D}_5 - \mathrm{D}_8$ together with maximum and minimum current in the output inductors in ABAC converter (at V_{HV}=270 V, F_{sw}=100 kHz, L_{σ}=7.56 μH, L_{out}=3 μH and n=5), when V_{LV}=29 V and/or V_{LV}=22 V

range. In S_{6-8}, the worst case occurs at high output voltage, due to the fact that no current flows through these switches when working in case I a. Furthermore, it is noticeable that the worst operating condition in these semiconductors is found at zero power transfer. This fact repercutes on the corresponding conduction losses of these power devices at low power transfer.

To provide a complete validation of the equations included in this paper, the maximum and minimum current level through the output inductor and switching currents in topside and bottomside semiconductors are also presented. Both maximum and minimum currents in $L_{\rm out}$ are defined by the same slope. Moreover, the higher secondary switching currents expected in topside semiconductors compared to bottomside devices are observed.

To validate the accuracy of the equations included in this work, theoretical values are presented toghether with simulation results. A good correlation between analytical and simulation results of the RMS and AVG currents is exposed in Fig. 4, validating the analytical models presented in this work.

B. Impact of clamp capacitances and dead time

The simplifications assumed in previous steps facilitate the mathematical development to obtain the analytical model presented in this work. However, the expected RMS and AVG currents are affected by clamp capacitances and dead time. In order to analyze the impact of these non-idealities, the relative error ($\varepsilon_{\rm rel}$) of the analytical models is calculated with the developed simulation model.

First, the clamp capacitance is swept from 25-300 μF to study the deviations of the analytical model when clamp capacitor peak-to-peak voltage ripple ($\Delta V_{\rm Clamp(pk-pk)}$) is varied. These capacitances correspond to 11.5 V (25 μF) and 0.25 V (300 μF) of $\Delta V_{\rm Clamp(pk-pk)}$. The required capacitance to obtain the desired $\Delta V_{\rm Clamp(pk-pk)}$ is computed with (14):

$$C_{\rm c} = \frac{C\,A\,\delta}{2\,\pi\,f_{\rm sw}\,\Delta V_{\rm Clamp(pk-pk)}\,(A-C)} \tag{14}$$

Second, the dead time ($t_{\rm dt}$) is presented for 50 ns and 500 ns, which correspond to 0.5 % and 5 % of the switching frequency selected in this work, i.e. $f_{\rm sw} = 100$ kHz.

In Fig. 5, the relative error in LV side semiconductors of the analytical models developed in this work is presented for $V_{\rm LV} = 29V$ at maximum power transfer. The impact of clamp capacitance variations is depicted in Fig. 5(a). In both RMS and AVG currents, $\varepsilon_{\rm rel}$ tends to decrease as higher is the clamp capacitance. This is due to the fact that the resulting $\Delta V_{Clamp(pk-pk)}$ is inversely proportional to the clamp capacitance. Thus, the difference between analytical and simulation results are lower as higher is this capacitance. In the case of S_{6-8} bottomside semiconductors, the relative error shown is caused by the short time interval in which the current is flowing through these semiconductors at high-power transfer.

When considering dead time variations [see Fig. 5(b)], $\varepsilon_{\rm rel}$ increase as higher is the selected dead time in all semiconductors. As same as in capacitance variations, the tend in S_{6-8} is inverse to the expected, which is also caused by the sensitivity of these semiconductors to the variation of the dead time. Furthermore, it is noticeable that the impact of the dead time in the presented analytical models is higher than clamp capacitance since the accuracy of the equations is considerable lower when dead time is increased.

In order to completely characterize the limitations of the analytical models, the relative error is also studied for output power variations from 35%-95% of the maximum output power. Therefore, $\varepsilon_{\rm rel}$ map is presented in Fig. 6 to study the impact of clamp capacitance and dead time variations on the RMS currents of S_{5-7} semiconductors. Considering the impact of the $C_{\rm c}$ shown in Fig. 6(a), it is noticeable that the accuracy of the models is good. However, this accuracy is worst as lower is the clamp capacitance in the whole output power range. In this work, the maximum relative error of topside semiconductors is 15 % for 25 μF of clamp capacitance, that corresponds to $\Delta V_{\rm Clamp(pk-pk)} = 11$ V, i.e. 20 % of the voltage in the clamp capacitance. Furthermore, $t_{\rm dt}$ influence is presented in Fig. 6(b). The results show a good agreement between analytical and simulation when working at low dead time in the considered output power range. However, there is a limitation of the analytical models when the output power is decreased or the dead time increased, i.e. the area where $\varepsilon_{\rm rel}$ is higher than 15 %.

Then, the analysis of the ABAC converter with the presented analytical models must be carefully checked when

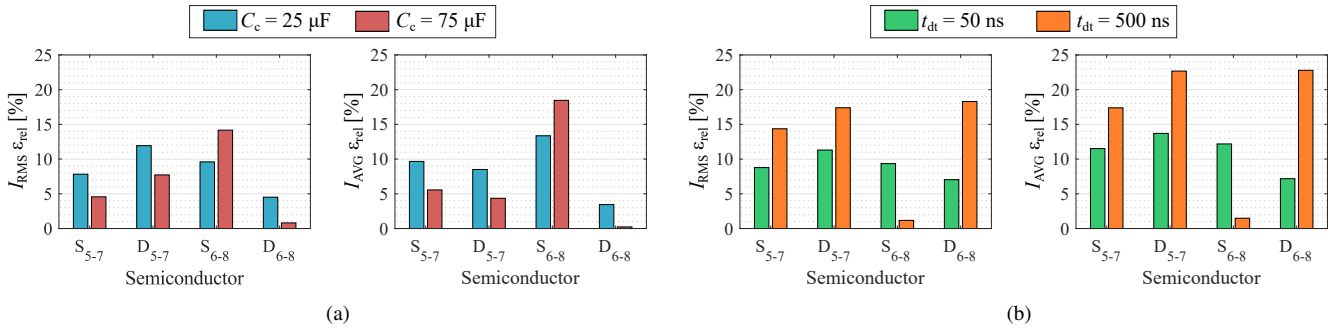


Fig. 5. Relative error ($\varepsilon_{\rm rel}$) bar chart of the analytical models presented in this paper working at $V_{\rm LV}$=29 V and maximum power transfer in forward mode for: a) clamp capacitances and b) dead time variations.

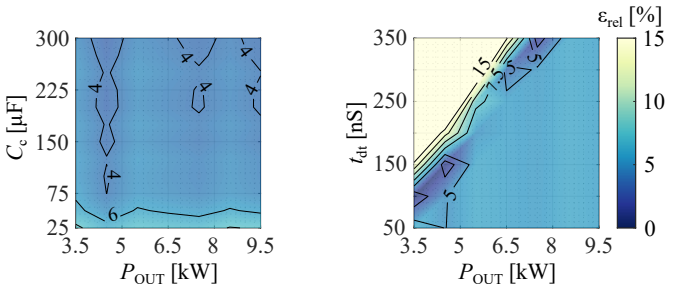


Fig. 6. Relative error ($\varepsilon_{\mathrm{rel}}$) map of the analytical models presented in this paper in topside S_{5-7} power devices when V_{LV}=29 V in the whole output power range for: a) clamp capacitances and b) dead time variations.

working under these conditions. The impact of varying clamp capacitance and dead time in ABAC converter has been presented to find the limitations of the equations included in this work. The accuracy of the models shows to be good when $\Delta V_{\mathrm{Clamp(pk-pk)}}$ is set below 20 % of the voltage in C_{c}. Nevertheless, this is not the case of dead time influence, whose increment considerably increase the resulting error especially when working at low power transfer.

IV. Conclusion

In this work, analytical models of the RMS and AVG currents in secondary switching devices in ABAC converter have been obtained. To this end, SPS Rectangular modulation is considered for the study since it is the simplest and easiest to implement. Based on the presented models, RMS and AVG currents in the aforementioned switching devices in both forward and backward power transfer can be calculated.

The results obtained with the simulation model developed in PLECS validate the analytical model in a MEA scenario, considering the highest and lowest voltages on LVDC side. The behavior of topside semiconductors shows to be similar in the considered cases. However, the current stress in bottomside switches is higher when the output voltage is increased. Furthermore, large current levels flow through diodes when the output voltage is lower.

To analyze the non-idealities of the analytical model, as clamp capacitances and dead time in power devices, on the resulting RMS and AVG currents from the analytical models, the relative error compared to the simulation model has been presented for secondary semiconductors working at maximum power transfer. At this power transfer level, the accuracy of the equations show to be good when varying clamp capacitance and/or dead time. However, the error presented in bottomside semiconductors S_{6-8} is above 15 %. This is due to the short time in which the current is flowing through these semiconductors, being the influence of the non-idealities higher on them. Furthermore, the error is analyzed for different output power levels in order to see the limitations of the models. The worst agreement between analytical equations and simulation model is found when the dead time is increased at low-power transfer.

The validation of these equations allows its utilization in the sizing of power devices and cooling system. Furthermore, this work is useful for optimization routines for the design of ABAC PEC for different application proposals, where the high computational cost of the simulation model is avoided.

Appendix
RMS and AVG equations in secondary power devices

In Tables III, IV, V and VI, the equations of the RMS and AVG currents are summarized. Each case correspond to an operating mode of ABAC, which are described in section II. Case II b. is not found in tables since the equations that describe its behavior are obtained from cases II a (for bottomside semiconductors) and II c (for topside semiconductors).

Furthermore, the presented models can be utilized for forward (HV to LV power transfer) and backward (LV to HV power transfer) operating modes. However, some adaptations must be done in order to adapt these models to backward operation. When the converter works in backward mode, the sign of the current waveform is the opposite of the forward mode. Therefore, the RMS and AVG current stress are calculated by swapping the equations of S_{5-7} with D_{5-7}, and S_{6-8} with D_{6-8} in each operating mode.

TABLE III
RMS and AVG current equations in case II a. (power transfer from HV to LV)

Switch	RMS	AVG
S_{5-7}	$\sqrt{\left(\frac{1}{T_{\mathrm{sw}}}\right)\frac{A^3}{3\,(A-C)}\,T_\delta}$	$\left(\frac{1}{T_{\mathrm{sw}}}\right)\frac{A^2}{2\,(A-C)}\,T_\delta$
S_{6-8}	$\sqrt{\left(\frac{1}{T_{\mathrm{sw}}}\right)\frac{B^3}{3\,(B-D)}\,T_\delta}$	$\left(\frac{1}{T_{\mathrm{sw}}}\right)\frac{B^2}{2\,(B-D)}\,T_\delta$
D_{5-7}	$\sqrt{\left(\frac{1}{T_{\mathrm{sw}}}\right)\left(\left(\frac{(C-B)^2}{3}+B\,C\right)\left(\frac{T_{\mathrm{sw}}}{2}-T_\delta\right)+\frac{C^3}{3\,(C-A)}\,T_\delta\right)}$	$\left(\frac{1}{T_{\mathrm{sw}}}\right)\left(\frac{-(C+B)}{2}\left(\frac{T_{\mathrm{sw}}}{2}-T_\delta\right)+\frac{C^2}{2\,(A-C)}\,T_\delta\right)$
D_{6-8}	$\sqrt{\left(\frac{1}{T_{\mathrm{sw}}}\right)\left(\left(\frac{(D-A)^2}{3}+A\,D\right)\left(\frac{T_{\mathrm{sw}}}{2}-T_\delta\right)+\frac{D^3}{3\,(D-B)}\,T_\delta\right)}$	$\left(\frac{1}{T_{\mathrm{sw}}}\right)\left(\frac{D+A}{2}\left(\frac{T_{\mathrm{sw}}}{2}-T_\delta\right)+\frac{D^2}{2\,(D-B)}\,T_\delta\right)$

TABLE IV
RMS AND AVG CURRENT EQUATIONS IN CASE II C. (POWER TRANSFER FROM HV TO LV)

Switch	RMS	AVG
S_{5-7}	$\sqrt{\left(\frac{1}{T_{sw}}\right)\left(\frac{C^3}{3\,(C-B)}\left(\frac{T_{sw}}{2}-T_\delta\right)+\left(\frac{(A-C)^2}{3}+A\,C\right)T_\delta\right)}$	$\left(\frac{1}{T_{sw}}\right)\left(\frac{C^2}{2\,(C-B)}\left(\frac{T_{sw}}{2}-T_\delta\right)+\frac{C+A}{2}T_\delta\right)$
S_{6-8}	$\sqrt{\left(\frac{1}{T_{sw}}\right)\left(\frac{D^3}{3\,(D-A)}\left(\frac{T_{sw}}{2}-T_\delta\right)+\left(\frac{(B+D)^2}{3}-B\,D\right)T_\delta\right)}$	$\left(\frac{1}{T_{sw}}\right)\left(\frac{D^2}{2\,(A-D)}\left(\frac{T_{sw}}{2}-T_\delta\right)+\frac{-(B+D)}{2}T_\delta\right)$
D_{5-7}	$\sqrt{\left(\frac{1}{T_{sw}}\right)\frac{B^3}{3\,(B-C)}\left(\frac{T_{sw}}{2}-T_\delta\right)}$	$\left(\frac{1}{T_{sw}}\right)\frac{B^2}{2\,(C-B)}\left(\frac{T_{sw}}{2}-T_\delta\right)$
D_{6-8}	$\sqrt{\left(\frac{1}{T_{sw}}\right)\frac{A^3}{3\,(A-D)}\left(\frac{T_{sw}}{2}-T_\delta\right)}$	$\left(\frac{1}{T_{sw}}\right)\frac{A^2}{2\,(A-D)}\left(\frac{T_{sw}}{2}-T_\delta\right)$

TABLE V
RMS AND AVG CURRENT EQUATIONS IN CASE I A. (POWER TRANSFER FROM HV TO LV)

Switch	RMS	AVG
S_{5-7}	$\sqrt{\left(\frac{1}{T_{sw}}\right)\left(\frac{B^3}{3\,(B-C)}\left(\frac{T_{sw}}{2}-T_\delta\right)+\frac{A^3}{3\,(A-C)}T_\delta\right)}$	$\left(\frac{1}{T_{sw}}\right)\left(\frac{B^2}{2\,(B-C)}\left(\frac{T_{sw}}{2}-T_\delta\right)+\frac{A^2}{2\,(A-C)}T_\delta\right)$
S_{6-8}	0	0
D_{5-7}	$\sqrt{\left(\frac{1}{T_{sw}}\right)\left(\frac{C^3}{3\,(C-B)}\left(\frac{T_{sw}}{2}-T_\delta\right)+\frac{C^3}{3\,(C-A)}T_\delta\right)}$	$\left(\frac{1}{T_{sw}}\right)\left(\frac{C^2}{2\,(B-C)}\left(\frac{T_{sw}}{2}-T_\delta\right)+\frac{C^2}{2\,(A-C)}T_\delta\right)$
D_{6-8}	$\sqrt{\left(\frac{1}{T_{sw}}\right)\left(\left(\frac{(D-A)^2}{3}+D\,A\right)\left(\frac{T_{sw}}{2}-T_\delta\right)+\left(\frac{(B-D)^2}{3}+B\,D\right)T_\delta\right)}$	$\left(\frac{1}{T_{sw}}\right)\left(\frac{(A+D)}{2}\left(\frac{T_{sw}}{2}-T_\delta\right)+\frac{(B+D)}{2}T_\delta\right)$

TABLE VI
RMS AND AVG CURRENT EQUATIONS IN CASE I B. (POWER TRANSFER FROM HV TO LV)

Switch	RMS	AVG
S_{5-7}	$\sqrt{\left(\frac{1}{T_{sw}}\right)\cdot\frac{B^3}{3\cdot(B-C)}\cdot\left(\frac{T_{sw}}{2}-T_\delta\right)}$	$\left(\frac{1}{T_{sw}}\right)\cdot\frac{B^2}{2\cdot(B-C)}\cdot\left(\frac{T_{sw}}{2}-T_\delta\right)$
S_{6-8}	$\sqrt{\left(\frac{1}{T_{sw}}\right)\cdot\frac{A^3}{3\cdot(A-D)}\cdot\left(\frac{T_{sw}}{2}-T_\delta\right)}$	$\left(\frac{1}{T_{sw}}\right)\cdot\frac{A^2}{2\cdot(D-A)}\cdot\left(\frac{T_{sw}}{2}-T_\delta\right)$
D_{5-7}	$\sqrt{\left(\frac{1}{T_{sw}}\right)\cdot\left(\frac{C^3}{3\cdot(C-B)}\cdot\left(\frac{T_{sw}}{2}-T_\delta\right)+\left(\frac{(A-C)^2}{3}+A\cdot C\right)\cdot T_\delta\right)}$	$\left(\frac{1}{T_{sw}}\right)\cdot\left(\frac{C^2}{2\cdot(B-C)}\cdot\left(\frac{T_{sw}}{2}-T_\delta\right)-\frac{A+C}{2}\cdot T_\delta\right)$
D_{6-8}	$\sqrt{\left(\frac{1}{T_{sw}}\right)\cdot\left(\frac{D^3}{3\cdot(D-A)}\cdot\left(\frac{T_{sw}}{2}-T_\delta\right)+\left(\frac{(B-D)^2}{3}+B\cdot D\right)\cdot T_\delta\right)}$	$\left(\frac{1}{T_{sw}}\right)\cdot\left(\frac{D^2}{2\cdot(D-A)}\cdot\left(\frac{T_{sw}}{2}-T_\delta\right)+\frac{D+B}{2}\cdot T_\delta\right)$

Then, the equations gathered in this work aid in the determination of the current stress in the LV side power devices of ABAC in both forward and backward operating modes considering all the hard switching and zero-voltage-switching cases.

REFERENCES

[1] G. Buticchi, S. Bozhko, M. Liserre, P. Wheeler, K. Al-Haddad, "On-board Microgrids for the More Electric Aircraft - Technology Review", *IEEE Transactions on Industrial Electronics*, Vol. 66, No. 7, pp. 5588-5599, July 2019.

[2] M. Kheraluwala, R. Gascoigne, D. Divan, E. Baumann, "Performance characterization of a high-power dual active bridge dc-to-dc converter", *IEEE Transactions on Industry Applications*, Vol. 28, No. 6, pp. 1294-1301, November-December 1992.

[3] A. Garcia-Bediaga, I. Villar, A. Rujas, L. Mir, "DAB modulation schema with extended ZVS region for applications with wide input/output voltage", *IET Power Electronics*, Vol. 11, No. 13, pp. 1755-4535, November 2018.

[4] R. A. Mastromauro, M. C. Poliseno, S. Pugliese, F. Cupertino, S. Stasi, "SiC MOSFET Dual Active Bridge Converter for Harsh Environment Applications in a More-Electric-Aircraft", in *International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS)*, March 3-5, Aachen, Germany, 2015.

[5] L. Tarisciotti, A. Costabeber, L. Chen, A Walker, M. Galea, "Evaluation of isolated DC/DC converter topologies for future HVDC aerospace microgrids", in *IEEE Energy Conversion Congress and Exposition (ECCE)*, October 1-5, Cincinnati, OH, USA, 2017.

[6] L. Tarisciotti, A. Costabeber, L. Chen, A Walker, M. Galea, "Current-

fed Isolated DC/DC Converter for Future Aerospace Microgrids", *IEEE Transactions on Industry Applications*, Vol. 55, No. 3, May-June, 2019.

[7] A. Ojeda-Rodríguez, P. González-Vizuete, J. Bernal-Méndez, M. A. Martín-Prats, "A Survey on Bidirectional DC/DC Power Converter Topologies for the Future Hybrid and All Electric Aircrafts", *Energies*, 2020, 13, 4883.

[8] L. Chen, L. Tarisciotti, A. Costabeber, P. Zanchetta, P. Wheeler, "Advanced modulation for the Active-Bridge-Active-Clamp (ABAC) Converter", in *IEEE Southern Power Electronics Conference (SPEC)*, December 4-7, Puerto Varas, Chile, 2017.

[9] L. Chen, L. Tarisciotti, A. Costabeber, F. Gao, P. Wheeler, P. Zanchetta, "Advanced Modulations for a Current-Fed Isolated DC-DC Converter With Wide-Voltage-Operating Ranges", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Vol. 7, No. 4, pp. 2540-2552, December, 2019.

[10] L. Chen, L. Tarisciotti, A. Costabeber, P. Zanchetta, P. Wheeler, "Parameters Mismatch Analysis for the Active-Bridge-Active-Clamp (ABAC) Converter", in *IEEE Southern Power Electronics Conference (SPEC)*, December 4-7, Puerto Varas, Chile, 2017.

[11] A. Fernandez-Hernandez, A. Garcia-Bediaga, I. Villar, G. Abad, "Analytical Equations of the Currents in Dual Active Bridge Converter for More Electric Aircraft", in *Vehicular Power and Propulsion Conference (VPPC)*, 2020.