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Partial Power Processing Based Charging Unit for Electric Vehicle Extreme Fast Charging Stations

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***Abstract*—This paper presents an analysis and design of a charging unit inside an electric vehicle extreme fast charging station. Due to the benefits that partial power processing achieves in terms of size reduction and efficiency improvement, it is decided to implement a partial power converter architecture. This type of architectures reduce the power to process by the converter but, they require an isolated topology. Therefore, a dual active bridge is selected for the study. Then, design wise, four different turns ratio values are selected and their performance results are compared in terms of processed power by the converter, semiconductors stress factor and energy loss. Finally, it is concluded that the turns ratio value is a key factor that must be correctly selected for optimizing the concerned comparison parameters.**

Keywords—fast charging station, electric vehicle, partial power converter, component stress factor, series connected converter, active power, non-active power, dual active bridge

I. INTRODUCTION

There is no doubt that the emergence of the electric vehicle (EV) is imminent [1]. Indeed, due to its efficient performance and reduced green-house emissions, the EV is turning into a real alternative to conventional combustion based vehicles. However, EVs' main disadvantage is their low autonomy, which can reach up to 550km [2]. In addition, the lack of charging infrastructure can lead to driving range anxiety [3]. Therefore, in order to avoid this, an extensive and solid EV charging stations grid is required. When it comes to the installation of the charging stations, one can find different types of solutions divided by their power level [4]. On one hand, up to 10kW AC charging stations can be found. On the other hand, DC wise, two main groups exist: fast charging stations (between 20kW and 120kW) and extreme fast charging stations (higher than 120 kW). Due to the high peak power values, the charging times can be reduced up to 15 minutes or higher [5], which makes the EV more attractive to the customer. Regarding fast charging stations, they are structures that are divided in different phases [6]. Usually, they are connected to a medium voltage AC grid and, then, the voltage level is reduced and rectified. Finally, several DC/DC power converters are implemented to charge each EV at the station. This paper will focus on the design of this DC/DC converter, which is connected between a common DC bus and the energy storage system (ESS) of the EV. Since the mentioned converter is required to process great power values (≥120kW), its size, cost and performance are key factors that must be optimized through its design. Due to this, recent literature around EV fast charging applications presents advance architectures based on partial power processing (PPP) [7]. This type of architectures aim to reduce the power processed by the converter, achieving reduced size and more efficient converters [8], [9]. Therefore, it is concluded that PPP based converters are very suitable for the concerned application. For example, authors from [4], [5], [7] present a partial power converter (PPC) based on an isolated full bridge for a fast charging application. There, it is concluded that PPCs achieve converter rating reduction and efficiency improvements. In addition, [4] concludes that a comparative analysis based on the turns ratio of the transformer is essential for achieving a reduction of the non-active power processed by the converter.

Bearing this in mind, in this work, a converter based on PPP is designed for an EV extreme fast charging application. In contrast to previous designing criteria presented in the literature, the present paper proposes to design the turns ratio value not only by judging the power processed by the converter but, also, the energy lost through the complete charging process.

II. BASIS OF PPP

As its name indicates, a power converter based on the PPP concept only processes a reduced percentage of the total power that goes from the source to the load. As example, Fig. 1 shows the power flow of a converter based on Full Power Processing (FPP) and a converter based on PPP. On one hand, as it can be observed in Fig. 1a, the FPP converter is designed to process the 100% of the power consumed by the load, generating a given quantity of losses. On the other hand, Fig. 1b shows the PPP

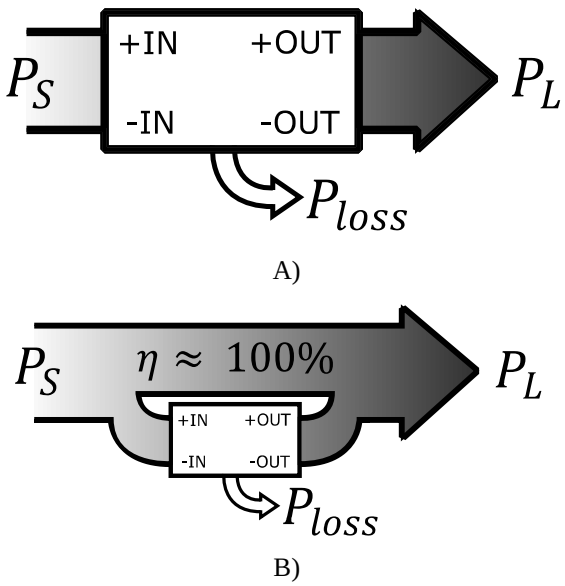

Fig. 1. Power flow diagram. A) FPP. B) PPP.

concept, which is based on achieving a reduction of the power processed by the converter. This way, the losses generated by the power converter are reduced, as well as its size. Furthermore, maintaining the same efficiency for the power converter, the global efficiency of the system increases. Equations (1),(2) describe how the efficiency of the converter affects the efficiency of the system in a different manner depending on if it is based on FPP or PPP.

$$\eta_{system_{FPP}} = \frac{P_L}{P_S} = \eta_{converter} = \frac{P_{out}}{P_{in}} \quad (1)$$

$$\eta_{system_{PPP}} = 1 - K_{pr} \cdot (1 - \eta_{converter}) \quad (2)$$

Where, η_{system} and $\eta_{converter}$ are the efficiencies of the system and the converter, respectively, and K_{pr} is the processed power ratio of the converter. The term K_{pr} will be further explained in detail.

The PPP concept was presented for the first time in spacecraft industry [10], where downsizing power converters connected to photovoltaic (PV) panels was the main priority. This way, a more efficient converter with higher power density was achieved without affecting the robustness of the system. As time passed by, this same concept was developed for further renewables applications based on wind generation [11], ESS and EV fast charging applications. On one side, wind generation wise, the most known example is the Doubly Fed Induction Generator (DFIG), where the power processed by the converter is just a fraction of the total power generated by the machine.

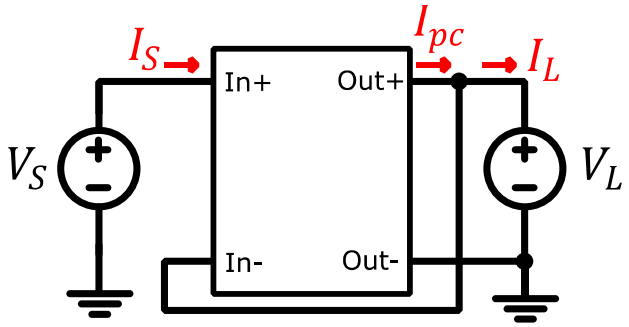

Fig. 2. ISOP step-down PPC architecture.

On the other side, when it comes to DC applications, different advanced architectures that reduce the power processed by the converter were developed. In first place, there exist differential power converters (DPC) that aim to correct current imbalances between series connected elements [12]–[14]. This type of converters only process power when current correction is required and, therefore, they are considered as PPP based converters. Secondly, authors from [4], [7], [15] present PPC architectures that reduce the power processed by the converter. In addition, PPCs achieve voltage step-up or step-down and power flow control from the source to the load. Since the present paper is focused on an EV charging application, it is concluded that the appropriate solution must be based on a PPC architecture. For example, Fig. 2 shows an input-series-output-parallel (ISOP) type PPC. This architecture achieves voltage step-down and if Kirchhoff's laws are applied on it, equations (3) and (4) are obtained. In addition, the efficiency of the system can be defined as shown in (5).

$$V_S - V_{in} = V_L \quad (3)$$

$$I_S + I_{pc} = I_L \quad (4)$$

$$\eta_{system} = \frac{V_L \cdot I_L}{V_S \cdot I_S} \quad (5)$$

On the other hand, the processed active power ratio of the converter (K_{pr}) is defined as the division between the processed power of the converter and the source's power (6).

$$K_{pr} = \frac{P_{conv}}{P_S} = \frac{V_{out} \cdot I_L}{V_S \cdot I_S} \quad (6)$$

Applying equations (3),(4) and (5) on (6), it is possible to obtain the K_{pr} curve of an ISOP step-down architecture in function of the static voltage gain $\left(G_V = \frac{V_L}{V_S}\right)$, see (7).

$$K_{pr} = \eta_{system} - G_V \quad (7)$$

Finally, Fig. 3 shows the curve from (7) compared to a FPC. As it can be observed, the FPC always processes the 100% of the power that goes from the source to the load, no matter G_V. However, the PPC processes less power as G_v gets closer to 1.

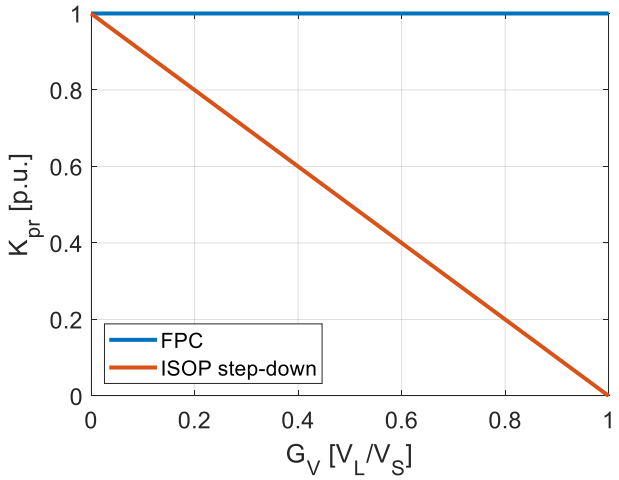

Fig. 3. Processed power ratio by a FPC and an ISOP PPC architecture.

III. EV EXTREME FAST CHARGING CONVERTER DESIGN CONSIDERATIONS

The present section aims to describe the main factors that must be taken into account when designing an EV fast charging converter and, therefore, it is divided into 3 main subsections: (i) description of the application, (ii) comparison parameters and (iii) results.

A. *Application description*

In first place, Table 1 describes an EV extreme fast charging application example. In addition, Fig. 4 presents typical voltage and power curves of an EV charging application up to a state of charge (SOC) of 80 % [16].

Table 1. Electrical parameters of an EV fast charging station.

Parameter	Value
V_S [V]	600
V_{EV} [V]	240 ÷ 400
P_{EV} [kW]	150

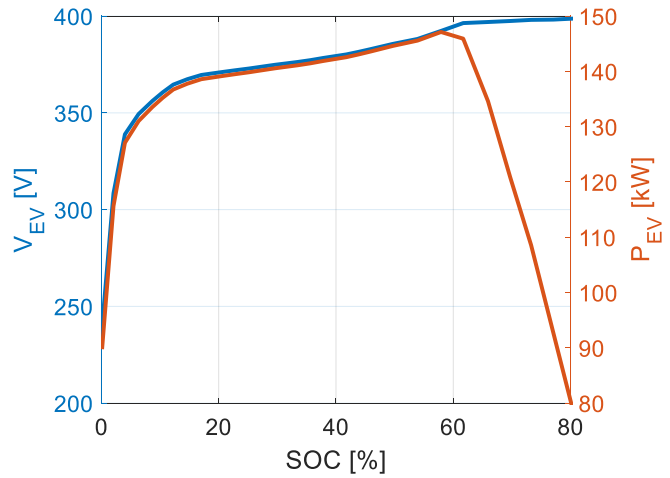

Fig. 4. Voltage and power level of the EV through the charge.

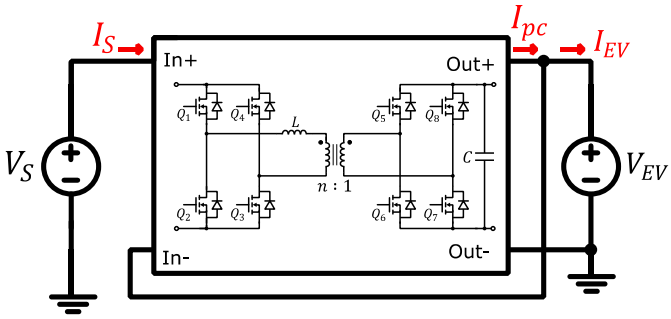

Fig. 5. DAB topology implemented on an ISOP step-down architecture.

Then, since the ISOP step-down architecture requires an isolated topology and the application demands high power levels, a dual active bridge (DAB) is chosen for the example, see Fig. 5. When it comes to the power flow control, phase shift modulation (PSM) is chosen due to its simplicity. Finally, Table 2 details the circuit parameters from Fig. 5. At first glance, it is observed that the input voltage of the converter and the maximum power that it must process are lower than the ones defined at Table 1.

Table 2. Electrical parameters of the DC-DC charging unit.

Parameter	Value			
V_{in} [V]	360 ÷ 200			
V_{out} [V]	240 ÷ 400			
$P_{converter}$ [kW]	60			
f_{sw} [kHz]	20			
n	1.5	1.166	0.833	0.5
L [µH]	15	11.66	8.33	5
C [µF]	600			
Semiconductor	FF200R12KE4 (primary) FF150R17KE4 (secondary)			

When it comes to the turns ratio, 4 different values are defined (together with their corresponding inductors). Regarding the values of the turns ratio, $n = 1.5$ and $n = 0.5$ are obtained by using equation (8). The other two values ($n = 1.166$ and $n = 0.833$), are calculated to maintain the same distance between each value.

$$M = \frac{V_{in}}{V_{out} \cdot n} = 1 \qquad (8)$$

The aim of this is to observe how this parameter affects on different factors that are related to the behavior of the converter. Indeed, the charging process presented in Fig. 4 is a variable scenario that provokes large working ranges inside the converter and, in consequence, there exists an ideal turns ratio for each working point. Once all the parameters have been described, the next step is to simulate the charging process of an EV. In order to achieve it, a sweep of simulations is carried out where the voltage of the EV is changed at each simulation.

B. *Comparison parameters*

With the aim of taking into account different factors that affect the behavior of the converter, 3 comparison parameters are considered: processed active and non-active power by the converter, semiconductors' component stress factor and energy lost through the charging period.

1) Processed active and non active power ratio

According to the definition given by IEEE [17], during the steady state of a DC-DC converter, the energy processed by storage components (capacitors and inductors) and that is not transferred from the source to the load is considered as non-active power flow (N). Do not confuse with reactive power (Q). Taking this into account, through this subsection, both types of powers (active and non-active) processed by the converter are described.

On one hand, the processed active power ratio of the converter is the average value of the instantaneous power during a period divided by the source power (6). On the other hand, the energy stored and delivered by reactive components causes losses, and therefore, the main components that consume non-active power are inductors and capacitors, see (9),(10),(11).

$$N_L = \frac{2 \cdot \Delta E_L}{T_s} = \frac{2 \cdot \int_0^{D \cdot T_s} |v_L(t) \cdot i_L(t)| dt}{T_S} \quad (9)$$

$$N_C = \frac{2 \cdot \Delta E_C}{T_s} = \frac{2 \cdot \int_0^{D \cdot T_s} |v_C(t) \cdot i_C(t)| dt}{T_S} \quad (10)$$

$$N_{total} = N_L + N_C \quad (11)$$

Where T_S represents the switching period and D the duty cycle. In order to follow the example from (6), equations (9),(10) will also be divided by the source power and represented in per unit (p.u.).

2) Semiconductors' component stress factor

When it comes to comparing the behavior of different power converters, there is another important parameter called the component stress factor (CSF) [18]. This method quantifies the stress suffered by the components inside the converter and it is useful for measuring the behavior of the converter. Equation (12) shows how to calculate the CSF value of the semiconductors.

$$SCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{max}^2 \cdot I_{rms}^2}{P_S^2} \quad (12)$$

Where $\sum_j W_j$ represents the total quantity of components, W_i the quantity of the specific component and V_{max} represents the maximum voltage that the semiconductor withstands in steady state.

3) Energy losses

Since each of the turns ratio presented in Table 2 obtains a peak efficiency at a different working point through the charging period, the aim of this subsection is to compare the accumulative amount of losses generated by each one through the whole process, see (13).

$$E_{loss_{i+1}} = \frac{P_{loss_{i+1}} + P_{loss_i}}{2} \cdot \frac{\mathrm{SOC}_{i+1} - \mathrm{SOC}_i}{100} + E_{loss_i} \quad (13)$$

Where P_{loss_i} represents the power losses generated by the converter at the i^{th} simulation (14), $\mathrm{SOC_i}$ represents the state of charge of the EV at the i^{th} simulation and E_{loss_i} is the accumulated the energy loss at the i^{th} simulation.

$$P_{loss_i} = P_{S_i} - P_{EV_i} \quad (14)$$

Where P_{S_i} represents the source power and P_{EV_i} represents the load power, which in this case corresponds to the EV.

C. Results

The present subsection compares the results obtained by the circuit from Fig. 5 with 4 different turns ratio values.

1) Processed active and non active power

In first place, Fig. 6 shows the processed active power ratio of the converter through the charging process. As it can be observed, the four curves obtain similar reduced processed active power ratios, which are directly dependent on the static voltage gain (7). The slight differences that exist at Fig. 6 are because the simulations are carried out in open loop, causing small differences at the output voltage.

In second place, there is the processed non-active power ratio, see Fig. 7. In this case, a remarkable difference exists between each case. For example, at low SOC values (bellow 5%), $n = 1.5$ obtains the lower values. However, as the battery charges and its voltage level increases, lower non-active power is processed with turns ratio values closer to $n = 0.5$.

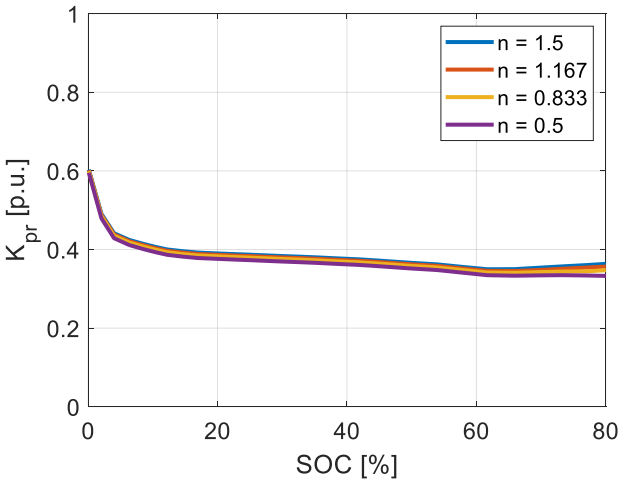

Fig. 6. Processed active power ratio of the converter.

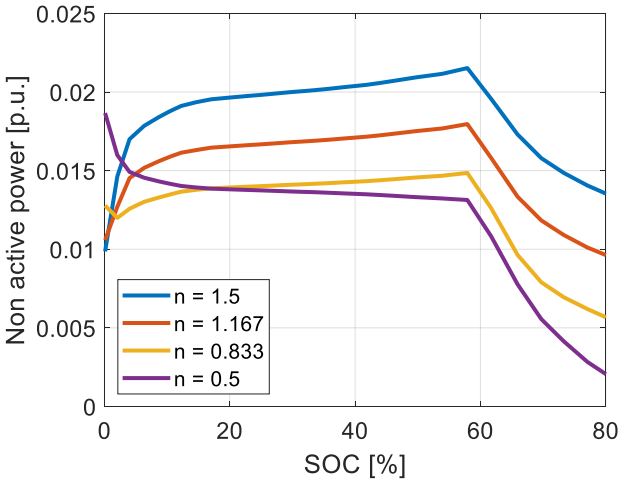

Fig. 7. Processed non-active power ratio of the converter.

2) Semiconductors' component stress factor

According to Fig. 8, the turns ratio value also affects the stress that the semiconductors suffer. Similar to Fig. 7, at low SOC values (bellow 5%), $n = 1.5$ causes lower stress on semiconductors but, as the battery charges, values closer to $n = 0.5$ turn out to be more favorable.

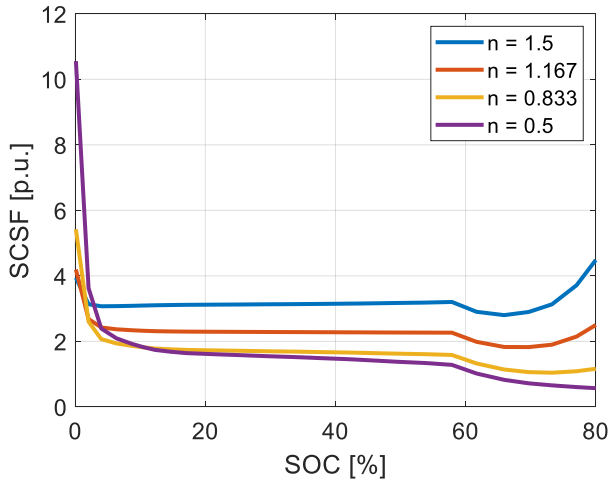

Fig. 8. Semiconductors' component stress factor.

3) Energy loss

Finally, Fig. 9 presents the accumulated energy lost through the charging process. As it can be observed, the turns ratio that achieves less energy losses is $n = 0.833$, followed by $n = 0.5$. However, at SOC values higher than 60%, the $n = 0.5$ curve shows a flatter slope, which means that lower losses are obtained at the last moments.

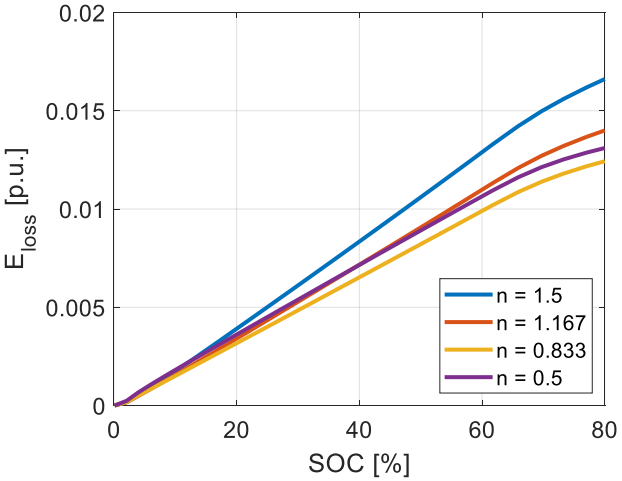

Fig. 9. Accumulated energy losses through the charging period.

IV. Conclusions

In the present paper an analysis and design of an EV charging unit for an extreme fast charging station has been carried out. The concerned converter is based on a DAB-PPC and with the aim of observing the effect of the turns ratio on the performance of the converter, different factors have been analyzed. On one hand, when it comes to the processed active power ratio, negligible differences exist. However, non-active power wise, significant variations are observed. Same thing happens with the SCSF and the accumulated energy loss. These last three comparison parameters conclude that the optimal turns ratio must be closer to $n = 0.5$. Indeed, $n = 0.833$ and $n = 0.5$ achieve the most favorable results. To be more precise, $n = 0.5$ provokes less stress on semiconductors through great part of the charging process (Fig. 8) but, according to Fig. 9, $n = 0.833$ is the most appropriate turns ratio value in terms of efficiency.

V. Future Lines

With the aim of improving the present paper, the next future lines are proposed:

- Extend the comparison to the stress suffered by the inductors and capacitors.
- Realize a second iteration of the comparison process with turns ratio values between $n = 0.5$ and $n = 0.833$.
- Build a small-scale prototype that confirms the obtained conclusions.

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