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Review of Architectures Based on Partial Power Processing for DC-DC Applications

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ABSTRACT This paper presents a review of advanced architectures based on the partial power processing concept, whose main objective is to achieve a reduction of the power processed by the converter. If the power processed by the converter is decreased, the power losses generated by the power converter are reduced, obtaining lower sized converters and higher system efficiencies. Through the review 3 different partial power processing strategies are distinguished: Differential Power Converters, Partial Power Converters and Mixed strategies. Each strategy is subdivided into smaller groups that entail different architectures with their own advantages and disadvantages. Also, due to the lack of agreement that exists in the sources around the naming of the different architectures, this paper seeks to stablish a nomenclature that avoids confusion when indexing this type of architectures. Regarding Partial Power Converters an extensive application oriented description is also developed. Finally, the main conclusions obtained through the review are presented.

INDEX TERMS DC-DC power converters, differential power converters, partial power converters, partial power processing, series connected converters.

I. INTRODUCTION

Over the last decade, Partial Power Processing (PPP) has turned into an attractive solution regarding power converter downsizing and efficiency improvement [1]. Furthermore, the advantages that PPP offers are very suitable for present and future coming applications, such as, energy storage systems (ESS) connected to renewable sources [2], [3] and electric vehicle (EV) fast charging stations [4]. This type of applications are usually considered as DC, but, there also exists some research around DC-AC inverters based on PPP [5], [6]. However, the present document focuses on describing PPP solutions for DC-DC applications. Indeed, the interest around PPP and the necessity of settling the knowledge around this type of power converters has increased, so as, the literature about it. In relation with the published literature, different strategies of PPP have been presented, each one with its corresponding advantages and disadvantages. However, there is no criteria in the naming of the PPP strategy nor in the classification according to their characteristics. As a result, one can easily get confused with the different names that the PPP strategies have and do not understand the real purpose of the given literature. Therefore, in order to avoid this type of confusion and describe the actual scenario around PPP, this document has as main objective grouping and defining the main PPP architectures that exist. Bearing this in mind, Section II introduces the basis that supports the PPP concept. Then, Section III describes the different PPP strategies that exist in the literature. After, Section IV presents a simple application of PPP, and, finally, Section V presents the main conclusions.

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II. BASIS OF THE PPP CONCEPT

The PPP concept was presented for the first time in spacecraft industry [7], where downsizing power converters connected to photovoltaic (PV) panels was the main priority. This way, a more efficient converter with higher power density was achieved without affecting the robustness of the system. As time passed by, this same concept was developed for further renewables applications based on wind generation [8], ESS and EV fast charging applications. On one side, wind generation wise, the most known example is the Doubly Fed Induction Generator (DFIG), where the power processed by the converter is just a fraction of the total power generated by the machine. On the other side, when it comes to DC applications, different advanced architectures that reduce the

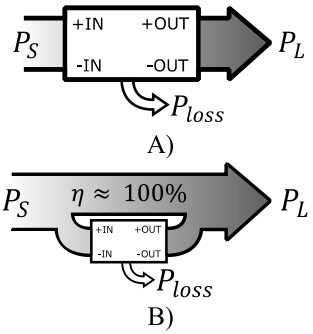

FIGURE 1. Power flow diagram. A) FPP. B) PPP [9].

power processed by the converter were developed. Each of these architectures present different advantages in function of the characteristics of the application, and the aim of this document is to organize PPP architectures regarding the application point of view. For this purpose, first, it is mandatory to clarify where the PPP terms come from.

As its name indicates, a power converter based on the PPP concept only processes a reduced percentage of the total power that goes from the source to the load. As example, Figure 1 shows the power flow of a converter based on Full Power Processing (FPP) and a converter based on PPP. On one hand, as it can be observed in Figure 1a, the FPP converter is designed to process the 100% of the power that flows from the source to the load, generating a given quantity of losses. On the other hand, Figure 1b shows the PPP concept, which is based on achieving a reduction of the power processed by the converter. In other words, the power converter based on PPP processes only a fraction of the power that flows from the source to the load. This way, the losses generated by the power converter are reduced, as well as its size. Furthermore, maintaining the same efficiency for the power converter, the global efficiency of the system increases [1]. Equations (1), (2) describe how the efficiency of the converter affects the efficiency of the system in a different manner depending on if it is based on FPP or PPP.

$$\eta_{systemFPP} = \frac{P_L}{P_S} = \eta_{converter} = \frac{P_{out}}{P_{in}} \tag{1}$$

$$\eta_{systemPPP} = 1 - K_{pr} \cdot (1 - \eta_{converter}) \tag{2}$$

where, η_{system} and $\eta_{converter}$ are the efficiencies of the system and the converter, respectively, and K_{pr} is the processed power ratio of the converter. The term K_{pr} will be further explained in detail.

III. ADVANCED ARCHITECTURES BASED ON PPP

The most recent literature presents different naming convention or PPP architectures. In order to obtain an universal naming criteria 3 main PPP strategies are proposed (see Figure 2):

1. Differential Power Converters (DPC).
2. Partial Power Converters (PPC).
3. Mixed strategies.

Therefore, the present section is divided into three subsections, one for each PPP strategy.

A. DIFFERENTIAL POWER CONVERTERS

The architectures based on the DPC concept are well defined in [10] as power converters that are aimed at correcting current imbalances that exist between different elements connected in series to the same voltage bus. In consequence, this type of power converters are designed to process the mentioned imbalance, and not the total power consumed/supplied by the sum of the elements. This type of architectures were presented in [11]–[13] as a ''new technique for equalizing a series battery stack''. There, different active balancing architectures are proposed, such as parallel connected Flyback modules and buck-boost current diverters. Later, the same architectures were further developed in [14]–[18] by implementing diverse topologies, for example: buck-boost with shared-core inductors and Dual Active Bridge (DAB). In consequence, the implementation of this type of architectures extended to current balancing of PV panels [19]–[23]. Then, although DPCs are defined as series connected element balancers, [24] also considers current balancing of parallel connected elements as PPP. In this case, authors from [24] present an advanced architecture based on PPP for LED current balancing applications. Finally, [25] is recommended for extended information around DPC architectures, specifically, sections 4 and 5.

On the other hand, when referring to this type of architectures there is a considerable confusion from various authors from the literature. Firstly, author from [12] introduced the term ''equalizer'' to refer to an active balancing power converter based on a buck topology. Later, the same architecture is presented in [14] as a ''battery system equalizer''. However, years after, authors from [19], [21], [23] introduced the term DPC for referring to the same current balancing architecture. Furthermore, authors in [20], [22] present a similar architecture for PV balancing, but, described as ''current diverter converter'' or ''parallel-connected PPC''. Also, when it comes to [15]–[18], each author uses a different term for referring to the same architecture: ''returned energy architecture'', ''Parallel connected submodule integrated converter'', ''input series output parallel'' and DPC.

As it can be observed, within the literature around active balancing, there exists a considerable confusion when it comes to naming this type of converters. Therefore, it must be clear that when the power converter has current balancing purposes, it should be considered as DPC.

Within this type of architectures there are 2 main groups:

1. Element to Element (E2E): the energy is transferred between neighboring elements.
2. Bus to Element (B2E): the energy is transferred from a common bus to the element or vice versa.

1) ELEMENT TO ELEMENT

In order to correct current imbalances between series connected elements, E2E type architectures (Figure 3) are focused on transferring the energy between neighbor elements [12], [14], [17], [19]–[22]. This can be observed in

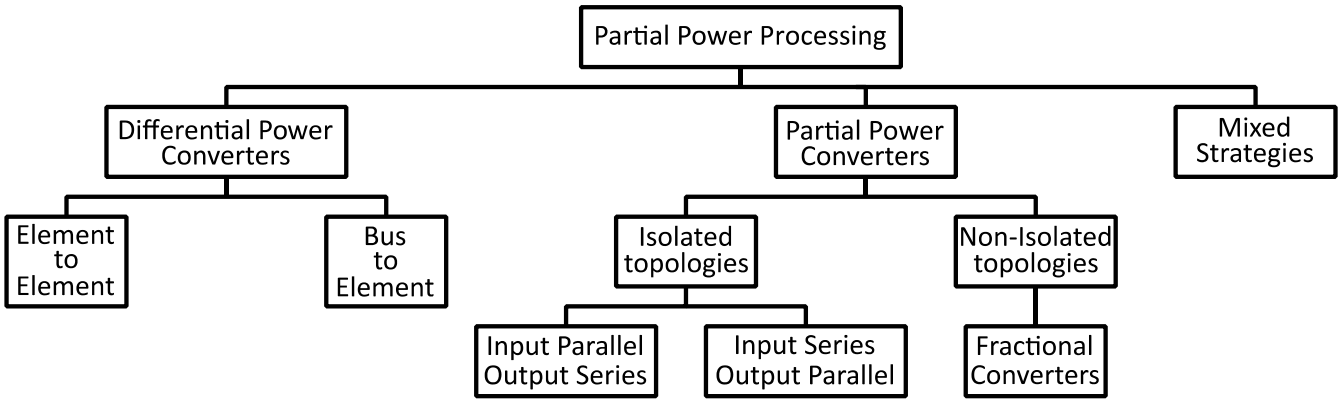

FIGURE 2. Overview of PPP strategies.

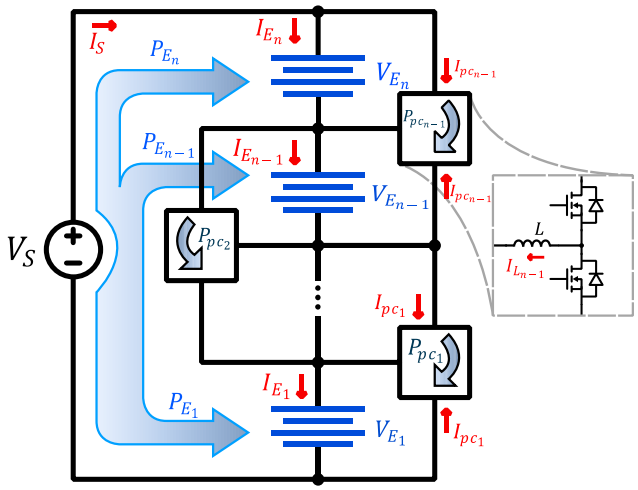

FIGURE 3. E2E type DPC architecture with buck-boost topology [22].

Figure 3, where the existing current and power flows are presented by red and blue arrows, respectively. On one hand, the power delivered by the source is divided by n, which is the number of elements. On the other hand, each converter processes a given power that will depend on the current that flows through the inductor. Their main advantage is that the components are designed at lower voltage and current values. However, one of their disadvantages is that the switching states of the converters are not independent. In addition, the voltage V_S is the result of the sum of the elements connected in series, therefore, if one would like to raise or reduce this voltage, it would be necessary to implement an additional converter that would process all the power.

Analyzing the different elements from Figure 3, it can be seen that, in order to regulate the current of n elements, only $n-1$ power converters are necessary. In this case, each power converter consist of a Buck-Boost topology and the total power processed is the sum of the power processed by each one (3).

$$P_{E2E} = \sum_{i=1}^{n-1} V_{E_i} \cdot \left| I_{L_i} \right| \tag{3}$$

On the other hand, by applying Kirchhoff's current law to the intermediate nodes between the series connected elements, the average inductor current value of each converter is obtained, see equation (4).

$$I_{L_i} = I_{E_i} - I_{E_{i+1}} + D_{i-1} \cdot I_{L_{i-1}} + (1 - D_{i+1}) \cdot I_{L_{i+1}} \tag{4}$$

where, I_{L_i} is the average inductor current of the i^{th} converter, I_{E_i} is the current of the i^{th} element and D_i is the duty ratio of the high side switch of the i^{th} converter.

As can be seen in (4), the average inductance current inside the converter depends on the currents of the adjacent elements.

2) BUS TO ELEMENT

B2E type architectures (Figure 4) focus on transferring energy between an element in series and the common bus [11], [13], [15], [16], [18]. This common bus can be a virtual bus voltage (represented as C_{bus} in Figure 4a) or the same input/output bus (represented as V_S in Figure 4b). Furthermore, its main purpose is to compensate an instantaneous power mismatch by injecting or rejecting current to series connected elements. Compared to E2E architectures, B2E type offer greater modularity and independence between converters. However, the voltage and current values at which the components are designed are higher [10], [19]. On the other hand, as with E2E type architectures, in case it is desired to regulate the value of V_S, B2E architectures also require an additional converter that processes all the power.

In the examples shown in Figure 4, it is observed that to regulate the current of n elements, n power converters are necessary and each of these converters contains a bidirectional Flyback topology. Furthermore, the total power processed by the sum of each is described by equation (5).

$$P_{B2E} = \sum_{i=1}^{n} V_{E_i} \cdot \left| I_{DC_i} \right| \tag{5}$$

Finally, equation (6) shows the current that each converter must process.

$$I_{DC,i} = I_i - I_{i+1} + I_{DC,i+1} \tag{6}$$

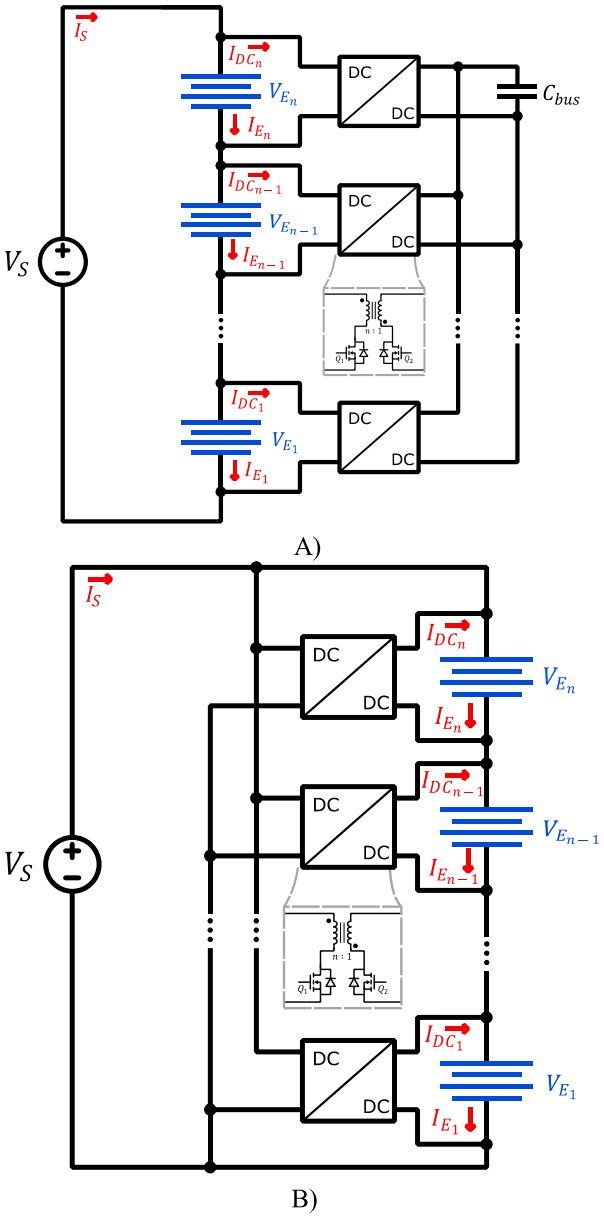

FIGURE 4. B2E type architecture with bidirectional Flyback topology. A) Virtual bus. B) Common bus.

3) OVERVIEW

With the aim of resuming the main results extracted from the literature around DPC, Table 1 points out the key characteristics of the main sources. Since each prototype is tested under different conditions, the aim of Table 1 is not to compare the obtained results by each one, but to make the reader see the goals achieved by each converter presented in the literature (together with their corresponding solutions). At first glance, it can be observed that both E2E and B2E architectures are implemented equally. However, the most popular topology in E2E architectures is the Buck-Boost and, in B2E, isolated topologies, specially, the Flyback. When it comes to the processed power ratio, the first literature around this type of architecture do not specify this value, since it was not their main objective. Nevertheless, according to [19], [21], the power processed by E2E converters goes from zero up to 50%-66%, depending on the mismatch to correct. On the other hand, there is the B2E architecture, whose processed power ratio also varies in function of the mismatch, but, according to [16], a higher peak efficiency is obtained. Finally, the main applications of this type of converters are related to PV and ESS state of charge (SOC) balancing.

B. PARTIAL POWER CONVERTERS

Compared to DPC architectures, PPCs are not designed to correct unbalances between series connected elements. Indeed, their main goal is to control the power flow, current and voltage level between a source and a load. Similarly, as in DPC literature, there also exists a wide variety of names to refer to the same PPC architecture, which can lead to confusion. Therefore, this chapter classifies and describes the different PPC architectures presented in the literature. Although different sources assume that PPC architectures always require galvanically isolated topologies [1], [26], [27], there exists literature that presents PPC architectures that do not require isolated topologies [28], [29]. Therefore, the present section is divided in two: PPC architectures that require galvanically isolated topologies and PPC architectures that do not.

1) PPC THAT REQUIRE ISOLATED TOPOLOGIES

The first PPC architecture to be presented was the one showed in Figure 5a [7], and it was defined as series connected boost unit (SCBU). As its name indicates, the objective of this converter is to elevate the voltage level of the source by connecting it in series to the output of the converter. It must be mentioned that the DAB topology presented in Figure 5a is just an example of how the converter would be connected in a PPC architecture. Same way could be implemented on the rest of the architectures from Figure 5. After, with the aim of extracting more power from a PV source, in [30] the same architecture is parallelized several times. Later, authors from [31], [32] presented different series connected architectures, see Figure 5b and Figure 5c. However, as it will be observed later, the architectures from Figure 5b and Figure 5c can be considered as the same architecture. Indeed, the power ratio processed by the converter at each architecture is the same, but the power flow inside it is reversed. Afterwards, similar architectures started to be used for voltage step-down applications [4], [33]–[35], see Figure 5d, Figure 5e and Figure 5f. In fact, Figure 5d, Figure 5e and Figure 5f are the same architectures as Figure 5a Figure 5b and Figure 5c, but exchanging V_S and V_L. Finally, authors from [36] discuss the dynamic behavior of two PPC architectures (Figure 5a and Figure 5b) by developing their small-signal models.

As well as with DPCs, PPCs from Figure 5 receive very different naming in the literature, which can lead to confusion. In the first place, Figure 5a was defined as series connected boost unit (SCBU) by [7]. However, novel

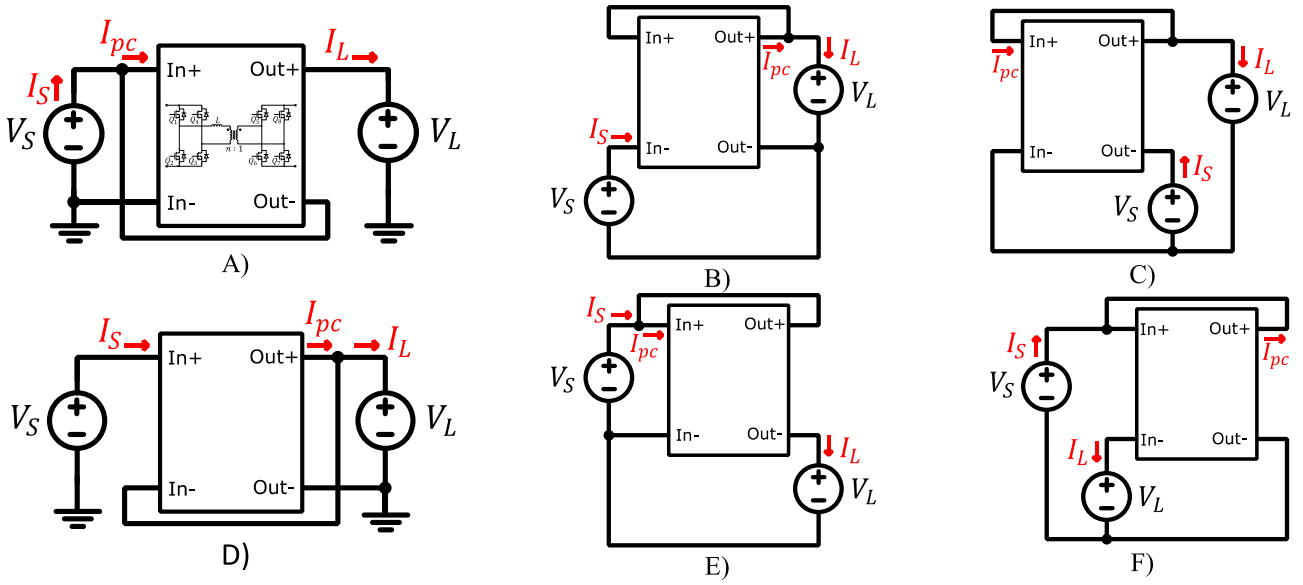

FIGURE 5. PPC architectures that require isolated topologies. A) IPOS step-up. B) ISOP-I step-up. C) ISOP-II step-up. D) ISOP step-down. E) IPOS-I step-down. F) IPOS-II step-down.

architectures were presented later (Figure 5b and Figure 5c), and in consequence, the name SCBU turned to be obsolete. Therefore, authors from[32] introduced the terms "Input-Parallel-Output-Series" (IPOS) and "Input-Series-Output-Parallel" (ISOP) for the architectures showed in Figure 5a and Figure 5b, respectively. However, great part of the literature continued using diverse terms such as "partial rated charging converter"[37], [38] or "series connected PPP converter" [39]. Apart from that, when it comes to the step-down architectures (Figure 5d, Figure 5e and Figure 5f), the same term "step-down PPC" is used by [4], [33], [34] for referring to different architectures, such as, Figure 5d and Figure 5f. In conclusion, there exists a lack of agreement on the terms used for naming each architecture from Figure 5. Therefore, in order to propose a unifying criteria for the naming of the PPC architectures, Figure 5 defines each architecture according to the criteria proposed in [32]. Finally, it must be remarked that all the architectures shown in Figure 5 require an isolated topology that avoids a short circuit in V_S or V_L [27], [40].

Once the architectures have been presented, the next step is to compare the processed power ratio of the converter at each architecture from Figure 5. For that purpose, the architecture from Figure 5a is taken as an example. Firstly, Kirchhoff's laws are applied on the architecture, obtaining equations (7) and (8). In addition, the efficiency of the system can be defined as shown in (9).

$$V_S + V_{out} = V_L \tag{7}$$

$$I_S = I_{pc} + I_L \tag{8}$$

$$\eta_{system} = \frac{V_L \cdot I_L}{V_S \cdot I_S} \tag{9}$$

On the other hand, the processed power ratio of the converter (K_{pr}) is defined as the division between the processed power of the converter and the source's power (10).

$$K_{pr} = \frac{P_{conv}}{P_S} = \frac{V_{out} \cdot I_L}{V_S \cdot I_S} \tag{10}$$

Applying equations (7), (8) and (9) on (10), it is possible to obtain the K_{pr} curve of an IPOS step-up architecture in function of the static voltage gain $\left(G_V = \frac{V_L}{V_S}\right)$ (11).

$$K_{pr} = \eta_{system} - \frac{\eta_{system}}{G_V} \tag{11}$$

Applying the same procedure to the rest of the architectures shown in Figure 5, the equations shown in Table 2 are obtained (in order to simplify, $\eta = \eta_{system}$).

The equations from Table 2 are plotted in Figure 6, where η is considered ideal.

Analyzing Figure 6, it is observed that each PPC architecture obtains a different power ratio curve. On the one hand, the K_{pr} curves obtained by the step-up architectures (Figure 5a, Figure 5b and Figure 5c) are located at $G_V > 1$. In this case, the step-up architecture that obtains the minimum processed power ratio curve is the IPOS step-up (Figure 5a). In contrast, ISOP-I step-up and ISOP-II step-up (Figure 5b and Figure 5c) obtain K_{pr} values greater than 1 when the static voltage gain is superior to 2. Apart from that, as mentioned before, the only difference between these last two architectures is the power flow direction inside the converter. On the other hand, the K_{pr} curves obtained by the step-down architectures (Figure 5d, Figure 5e and Figure 5f) are located at $G_V < 1$. In this case, ISOP step-down (Figure 5d) is the architecture that achieves a lower power ratio curve. Furthermore, IPOS-I step-down and IPOS-II step-down (Figure 5e and Figure 5f) architectures obtain K_{pr} values greater

TABLE 1. Key parameters extracted from the literature around DPC.

Source	Architectures	Processed Power ratio	Eff.	Topology	Application
[11]	B2E	-	-	Flyback	ESS balancing
[12]	E2E	-	-	Buck-Boost	ESS balancing
[13]	B2E	-	-	Multi input Flyback	ESS balancing
[14]	E2E	-	-	Buck-Boost	ESS balancing
[16]	B2E	0÷66%	98%	Flyback	PV local MPPT
[17]	E2E	-	92%	Buck-Boost	-
[18]	B2E	-	95%	DAB	Data center
[19]	E2E	0÷66%	95%	Buck-Boost	PV local MPPT
[21]	E2E	0÷50%	95%	Buck-Boost	PV local MPPT
[15][1]	B2E	0÷60%	-	Flyback	PV local MPPT
[24][1]	Parallel	0÷90%	-	Buck-Boost	LED balancing

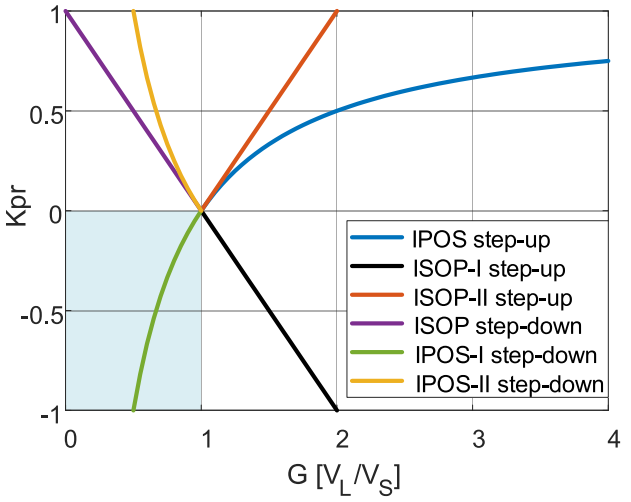

FIGURE 6. Processed power ratio by the converter for the architectures showed in Figure 5.

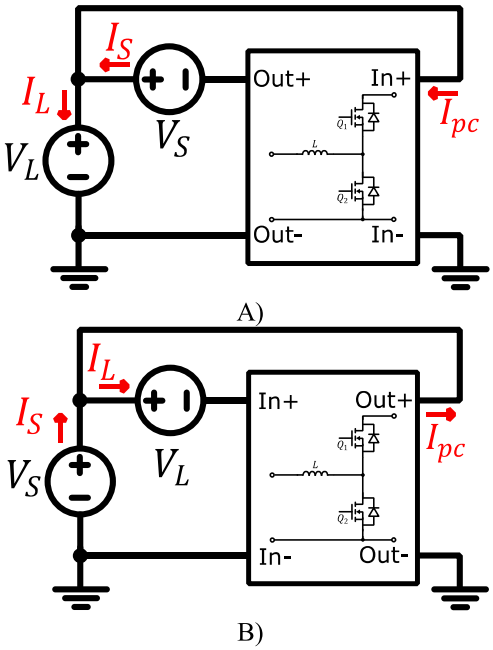

FIGURE 7. PPC architectures that do not require isolated topologies. A) FCC step-up. B) FCC step-down.

than 1 when the static voltage gain is inferior to 0.5. Again, the only difference between them is the power flow direction inside the converter.

2) PPC THAT DO NOT REQUIRE ISOLATED TOPOLOGIES

All the literature around PPC presented until now considers as essential the application of isolated topologies at the conversion stage. However, in [28], [29] a novel architecture is presented and named as ''fractional charging converter (FCC)'', see Figure 7b. The main advantage of this architecture is that it allows non-isolated topologies inside the power converter, which simplifies the design and manufacturability of the conversion stage. Same thing occurs with Figure 7a, but, for step-up applications. It must be mentioned that the Half-Bridge topology presented in Figure 7 is just an example of how the converter would be connected in a FCC architecture. Indeed, authors from [28], [29] implement a DAB.

Applying the procedure described in equations (7)-(11), the K_{pr} curve of a FCC architecture is obtained in function of the static voltage gain (G_V), see Table 3.

TABLE 2. Processed active power ratio by the different architectures from Figure 5.

Architecture type	K_{pr}
IPOS SU	$\eta - \frac{\eta}{G_V}$
ISOP-I SU	$\eta - G_V$
ISOP-II SU	$G_V - \eta$
ISOP SD	$\eta - G_V$
IPOS-I SD	$\eta - \frac{\eta}{G_V}$
IPOS-II SD	$\frac{\eta}{G_V} - \eta$

The equations from Table 3 are plotted in Figure 8, where η is considered as ideal. Analyzing Figure 8, it is concluded that the FCC architectures presented in Figure 7 are limited to a

TABLE 3. Processed active power ratio by the different architectures from Figure 7.

Architecture type	K_{pr}
FCC-SU	$G_V - \eta$
FCC-SD	$\frac{\eta}{G_V} - \eta$

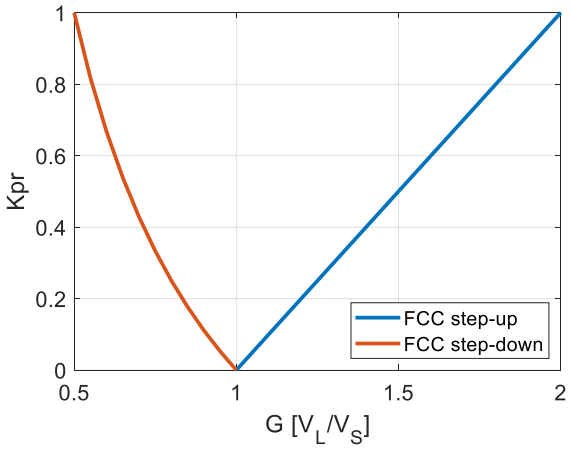

FIGURE 8. Processed power ratio by the converter for the architectures showed in Figure 7.

G_V value of 2 and 0.5, respectively. Indeed, both architectures can be considered as the same, but, with reverse power flow between V_S and V_L.

Finally, it must be outlined that the architectures from Figure 7 are still under research. Indeed, one can easily observe that if a buck or boost topology is implemented on them, since only 2 switching states exist, the semiconductors and passive elements (for example, inductor) will process the same current and voltage as in a FPC. Therefore, further analysis on advanced topologies that can avoid processing the full current and voltage levels is required.

3) OVERVIEW

With the aim of resuming the main points extracted from the literature around PPC, Table 4 details different characteristics of each reference. Since each prototype is tested under different conditions, the aim of Table 4 is not to compare the obtained results by each one, but to make the reader see the goals achieved by each converter presented in the literature (together with their corresponding solutions). In the first place, architecture wise, although different architectures have been applied at each literature, IPOS step-up is the most popular. On the other hand, when it comes to the processed power ratio of the converter, a wide variety of values are obtained. This is due to the fact that K_{pr} is directly proportional to the static voltage gain of the application, which varies from one literature to another. In consequence, due to the low K_{pr} values, high overall efficiencies are obtained (>95%). Then, analyzing the applied topology for the stage of conversion, it is observed that all of them use isolated topologies (even [29]), being the isolated full bridge topology the most popular one. Nevertheless, it must be remarked that

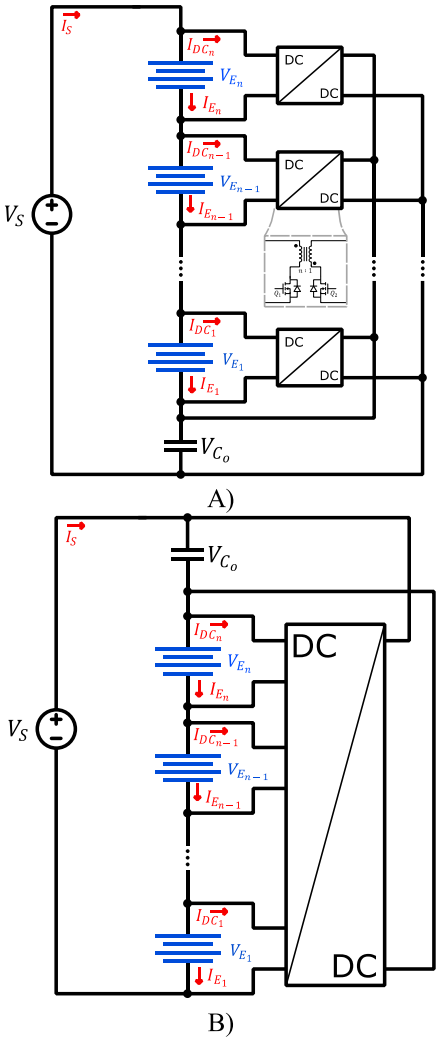

FIGURE 9. Alternative PPP architectures that mix DPC and PPC strategies. A) [48]. B) [49].

although isolated topologies are used for the stage conversion, the system is not. Indeed, there is not any galvanically isolated solution that achieves PPP. Apart from that, as expected, the great majority of the applications are related to PV systems, followed by ESS and EV charging. Finally, analyzing systems' and converters' power flow, it can be concluded that there exists a lack of researching around bidirectional PPCs. In fact, [26], [29], [33] are the only references that present a bidirectional prototype. Apart from that, as it can be observed in [40]–[42] although the system's power flow is unidirectional, the applied power converter is bidirectional. This is due to the fact that the power converter is working as both step-up and step-down (extended information is detailed in Section IV).

C. MIXED PPP ARCHITECTURES

The disadvantages of DPC and PPC converters give reason to investigate alternative architectures which can offer better performances for specific applications. First, authors from

TABLE 4. Key parameters extracted from the literature around PPC.

Source	Architectures	Processed Power ratio	Eff.	Topology	Application	Power flow	
						Conv.	Sys.
[26]	IPOS step up	10%÷25%	98.9%	DAB	ESS integration	Bi.	Bi.
[30]	IPOS step up	20%	96.25%	IFB+Rec.[2]	PV	Uni.	Uni.
[31]	ISOP-II step up	20%	96%	Flyback	PV	Uni.	Uni.
[32]	IPOS step up ISOP-I step up	40% 50%	95.5% 92%	Flyback	PV	Uni.	Uni.
[33]	ISOP step down	72÷80%	96.74%	DAB	-	Bi.	Bi.
[34]	ISOP step down	10÷30%	98.6%	IFB+Rec.	PV	Uni.	Uni.
[38]	IPOS-II step-down	33%	-	IFB+Rec.	EV Fast charging	Uni.	Uni.
[40]	IPOS step up	15%	99.5%	IFB-CT+Rec.[3]	PV	Bi.	Uni.
[29]	FCC-step-down	21.5%	98.2%	DAB	ESS	Bi.	Bi.
[41]	ISOP-II step up	-	98.8%	Cuk isolated+ Unfolder	PV+ESS	Bi.	Uni.
[43]	IPOS step up	10%÷70%	90%	Flyback	PV	Uni.	Uni.
[44]	IPOS step up	17%÷30%	98.55%	IFB+Rec.	EV Fast charging	Uni.	Uni.
[45]	IPOS step up ISOP-I step up ISOP step down	- 5%÷15% 15%÷25%	- 99% 98.5%	Flyback IFB+Rec. IFB+Rec.	PV	Uni.	Uni.
[2][1]	IPOS step up	20%÷40%	-	DAB	PV+ESS	Bi.	Bi.
[3][1]	IPOS step up	40%	-	DAB	PV+ESS	Bi.	Bi.
[4][1]	ISOP step down	35%	98%	IFB+Rec.	EV Fast charging	Uni.	Uni.
[37][1]	ISOP-I step up	5%÷35%	99%	IFB+Rec.	PV	Uni.	Uni.
[42][1]	IPOS step up	-	96%	DAB+Unfolder	Wind generation	Bi.	Uni.
[46][1]	IPOS step up	83%	97.6%	Flyback	PV	Uni.	Uni.
[47][1]	ISOP-I step up	15%	98.76%	Flyback	PV	Uni.	Uni.

[48] and [49] present a novel architecture that mixes DPC and PPC strategies, see Figure 9a and Figure 9b, respectively. As it can be observed, both examples are very similar to a B2E architecture (Figure 4), but, locating the common bus in series with the other elements. This way, according to [48], the processed power ratio by the converter is defined by (12).

$$K_{pr} = \frac{V_{C_o}}{V_{E_1} + \cdots + V_{E_n}} \tag{12}$$

Comparing Figure 9a and Figure 9b, several differences can be observed. In the first place, C_o wise, authors from [48] locate it connected to the ground, whereas, authors from [49] locate it connected to the higher potential point. Apart from that, when it comes to the stage of conversion, authors from [48] install modular flyback converters, one for each element. However, authors in [49] decide to make use of a multi-input DAB converter.

Another alternative to DPC and PPC architectures is to implement an auxiliary series converter that regulates the output voltage by processing partial power [50]. This way, the main converter always works in a peak efficiency working point. However, adding an extra power converter may result in a bigger volume and lower efficiency. Furthermore, [50] concludes that the polarity of the auxiliary voltage affects directly to the processed power ratio of the main converter, and, in consequence, to the efficiency.

Apart from that, there is the PPP strategy presented in [51], where a single converter is used for charging and discharging 2 different ESS, see Figure 10. This way, authors from [51] claim that the multi-source converter from Figure 10 reduces

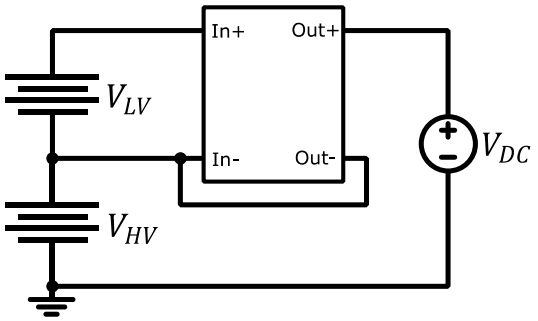

FIGURE 10. Multi ESS charging converter.

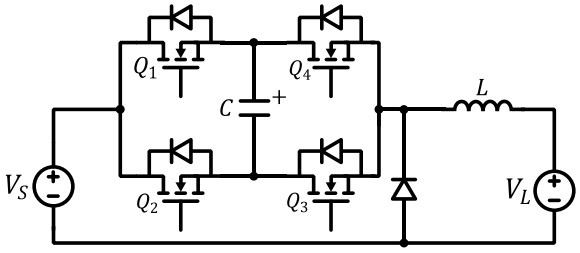

FIGURE 11. Pseudo partial power converter based proposed in [52].

the cost of the converter and it achieves high efficiency and high power density due to the reduction of power processed. When it comes to the stage of conversion, isolated and non-isolated topologies can be applied on it.

Finally, authors from [52] propose a pseudo partial power converter based on a switched capacitor topology, see

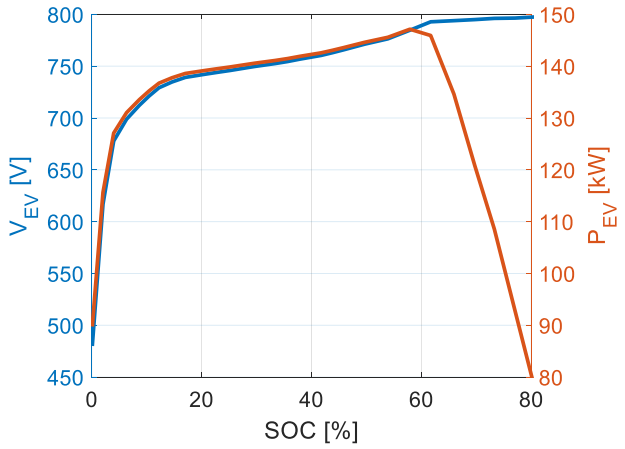

FIGURE 12. Voltage and power level of the EV through the charge.

Figure 11. The presented converter is designed for step down applications and allows the implementation of semiconductors with lower ratings. Its operation principle is based on regulating the voltage level of the switched capacitor by adjusting the duty cycles of the pair semiconductors $Q_{1,3}$ and $Q_{2,4}$.

1) OVERVIEW

With the aim of summarizing the main points extracted from the literature around mixed PPP strategies, Table 5 details the key characteristics of each reference. Since each prototype is tested under different conditions, the aim of Table 5 is not to compare the obtained results by each one, but to make the reader see the goals achieved by each converter presented in the literature (together with their corresponding solutions).

At first glance, it is observed that a great variety of alternative solutions to DPCs and PPCs exists. The first one consists of mixing both strategies in order to achieve active balancing of series connected elements and voltage step-up. In this case, isolated topologies are recommended. Indeed, comparing [48] and [49], it is concluded that applying a multi-input DAB converter achieves higher efficiencies. Then, there is the auxiliary architecture proposed in [44]. However, authors conclude that the obtained converter is slightly less efficient (-0.3%) and bigger ($+10\%$). On the other hand, when it comes to the multi-ESS architecture[51], it can be considered as the most promising one due to its high efficiency and simple power conversion circuit. Finally, representing AC applications, authors from [46] present a high efficiency and high power density (25 kW/L) prototype based on a buffer architecture.

IV. PPP APPLICATION EXAMPLE

With the objective of remarking the main benefits of PPP, the present section shows an application example of an EV fast charging station such as the one described in Table 6.

Apart from that, Figure 12 presents the voltage and power curves of the EV for each value of SOC.

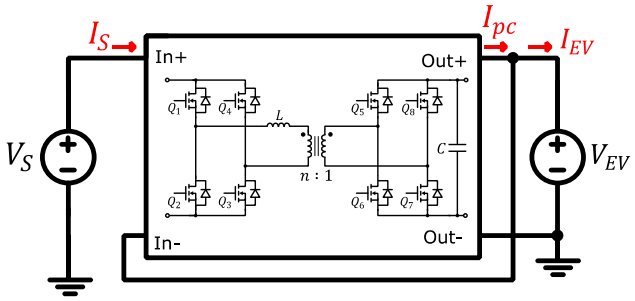

FIGURE 13. DAB topology implemented on an ISOP step-down architecture.

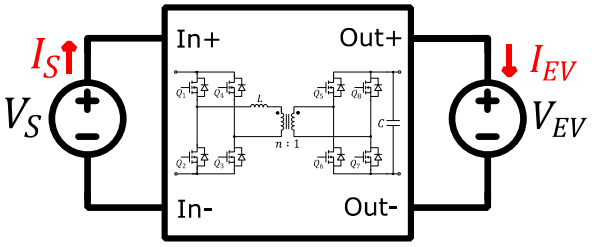

FIGURE 14. DAB topology implemented on a FPC architecture.

A. ARCHITECTURE AND TOPOLOGY SELECTION

In first place, regarding the main objective of the application (power delivery to a given load), it is decided that the appropriate PPP strategy must be based on PPC. Then, concerning the voltage values from Table 6, it is obvious that a step-down architecture is required. Therefore, since the ISOP step-down (Figure 5d) is the PPC architecture with lower K_{pr} curve, it is concluded that the ISOP step-down architecture is the most appropriate. Once the PPC architecture is chosen, the next step is to select a converter topology. Since the ISOP step-down architecture requires an isolated topology and the application demands high power levels, a DAB is chosen for the example, see Figure 13. Then, due to its simplicity, phase shift modulation (PSM) is chosen for controlling the power flow between the source and the load.

On the other hand, in order to observe the benefits of PPC architectures and based on [26], [44], the circuit shown in Figure 13 is compared to its FPC version, see Figure 14.

Finally, Table 7 details the circuit parameters from Figure 13 and Figure 14. At first glance, the main differences between them are the input/output voltage of the converter and the maximum power that it must process. In consequence, the PPC will process less power and it will require lower rating devices, increasing the efficiency and reducing the cost of the whole system.

B. COMPARISON PARAMETERS

With the aim of taking into account different factors that affect the behavior of the converter, 3 comparison parameters are considered: processed active power by the converter, component stress factor (CSF) and system's and converter's efficiency.

TABLE 5. Key parameters extracted from the literature around mixed strategies.

Source	Architectures	Processed Power ratio	Eff.	Topology	Application
[48]	DPC+PPC	50%	95%	Flyback	ESS
[49]	DPC+PPC	-	97.5%	Multi-input DAB	ESS
[50]	Auxiliary	-	97.7%	DAB-LLC+Auxiliary IFB	-
[51]	Multi-ESS	30%	99.63%	Buck-boost	EV power train
[52][1]	Pseudo partial	57%	99.3%	Switched capacitor	EV fast charging

TABLE 6. Electrical parameters of an EV fast charging station.

Parameter	Value
V_S [V]	820
V_{EV} [V]	480 ÷ 800
P_{EV} [kW]	150

TABLE 7. Electrical parameters of an EV fast charging station.

Parameter	DAB-FPC	DAB-PPC
V_{in} [V]	820	340 ÷ 20
V_{out} [V]	480 ÷ 800	480 ÷ 800
$P_{converter}$ [kW]	150	40
f_{sw} [kHz]	20	20
n	1.366	0.408
L [µH]	37.35	11.16
C [µF]	500	600
Semiconductor	FF300R17KE4	FF200R12KE4 (primary) FF150R17KE4 (secondary)

1) PROCESSED ACTIVE POWER

Based on equation (10), the present subsection compares the processed power ratio obtained by each converter from Figure 13 and Figure 14. As expected, the DAB-FPC processes the 100% of the power that flows from the source to the battery, no matter the charging point. However, the DAB-PPC processes a maximum of 40% of the application power. Indeed, this value decreases through the charging period, as the static voltage gain gets closer to 1.

2) SEMICONDUCTORS' CSF

When it comes to comparing the behavior of different power converters, there is another important parameter called the CSF [53]. This method quantifies the stress suffered by the components inside the converter and it is useful for measuring the behavior of the converter IV-B3.

$$SCSF_i = \frac{W_i}{\sum_j W_j} \cdot \frac{V_{max}^2 \cdot I_{rms}^2}{P_S^2} \tag{13}$$

where, $\sum_j W_j$ represents the total quantity of components, W_i the quantity of the specific component, V_{max} represents the maximum voltage that the semiconductor withstands in steady state and P_S represents the power source.

Based on (13), Figure 16 shows the SCSF obtained at the FPC and the PPC. There, it is concluded that due to the reduction of the power processed by the converter, the semiconductors inside it suffer from less stress through all the charging period.

3) SYSTEM'S AND CONVERTER'S EFFICIENCY

In this subsection, the efficiency of the system and the efficiency of the converter are calculated. As shown in (1) and (2), in the case of a FPC, both terms are the same. However, in a PPC they are related by the K_{pr} value. This is confirmed in Figure 17, where it is observed that although the converter's efficiency at the PPC is lower than in the FPC, system's efficiency at the PPC results in high value. This is due to the low K_{pr} values obtained in Figure 15. Finally, it must be mentioned that the low efficiency values obtained by the converter at the PPC are due to the large working range: from $V_{in/out} = 340/480$ to $V_{in/out} = 20/800$.

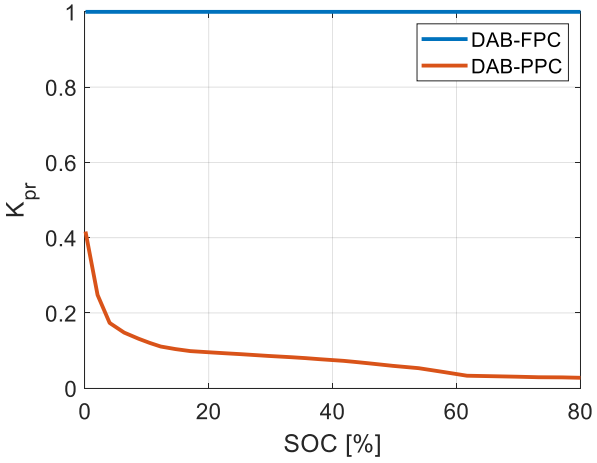

FIGURE 15. Processed power ratio obtained by each converter from Figure 13 and Figure 14.

Finally, although the concerned application example does not require step-up and step-down, it is worth mentioning that all the architectures shown in Figure 5 can achieve it. However, certain concepts must be considered. In order to explain this, IPOS step-up architecture (Figure 5a) will be taken as an example for the step-down application presented in Table 6. In order to achieve voltage step-down by implementing an IPOS step-up, V_{out} from Figure 5a must result in a negative value. Consequently, the power converter

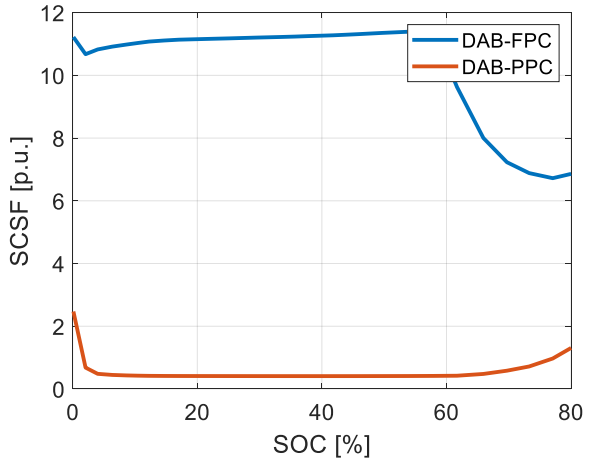

FIGURE 16. Semiconductors CSF at each converter from Figure 13 and Figure 14.

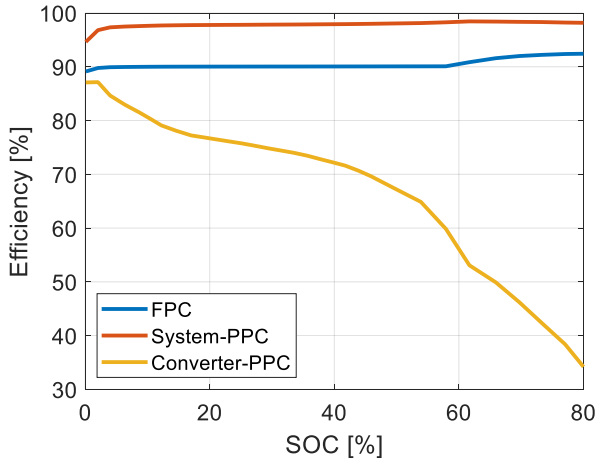

FIGURE 17. System and converter efficiency obtained by each converter from Figure 13 and Figure 14.

must be able of inverting the polarity of the mentioned voltage and managing the power-flow inside the converter in the other direction. This is because the power converter is working inside the shaded zone from Figure 6. The same will occur for the rest of the architectures from Figure 5. An example of it is shown in [40], [41], where a voltage step-up/down prototype is presented. Indeed, by adding some extra switches, authors from [40]–[42] make use of the architectures presented in Figure 5 for applications where both, buck and boost capabilities are required. This way, since the working range of the application is closer to $G_V = 1$, a lower K_{pr} value is achieved, reducing the size of the converter. However, when it comes to the FCC architectures presented in Figure 7, this type of architectures do not offer the possibility of achieving both, step-up and step-down. For example, analyzing Figure 7a, if V_{out} is inverted, V_S and V_L result in the same voltage level. Same thing would happen in Figure 7b.

C. MAIN DRAWBACKS OF PPP

Until now, only advantages of PPP have been presented, but this type architectures also have significant drawbacks that must be considered. First, there is no architecture based on PPP that ensures galvanic isolation between the source and the load. This fact can be unacceptable in several applications. Secondly, since the elements inside the converter are rated for low voltage levels, an over voltage protection circuit must be added for starting conditions. Although extra devices affect the efficiency, the PPC should still generate less power losses than a FPC [51]. Then, focusing on DPCs, their main disadvantage is that their implementation is limited to application where the voltage V_S is the result of the sum of the elements connected in series. In other words, there is no necessity of raising or reducing this voltage. Apart from that, in relation with E2E architectures, there is a risk of exceeding the power rating of the converter if correct dimensioning is not carried out in function of the mismatch to correct [22].

On the other hand, PPC wise, the processed power ratio of the converter is directly dependent from the static voltage gain. So, if there is a high step-up/down between the source and the load, PPCs may result inadequate. Also, compared to FPC architectures, PPCs cause a larger operation range inside the power converter [44]. For example, considering the application presented in Table 6, it can be concluded that a FPC will work with a fixed input voltage and a variable output voltage. However, if an ISOP step-down PPC architecture is implemented (Figure 5d), a variable input voltage and a variable output voltage are obtained. Apart from that, according to [1], when comparing a FPC and a PPC it is important to take into account not only the active power processed by the converter, but also the non-active power [54], which affects directly to the sizing of energy storage elements such as capacitors and inductors. Indeed, authors from [1] conclude that a Flyback PPC topology obtains same non-active power results as a conventional boost FPC topology. Finally, when it comes to PPC architectures that do not require isolated topologies (Figure 7), the voltage and current sizing of the devices inside the power converter are the same as in a FPC, which forces to carry on with further research around advanced non-isolated topologies.

V. CONCLUSION

This paper presents a review and a universal naming of PPP based architectures that achieve a reduction of the power processed by the converter. This type of architectures are mainly focused on DC applications, such as: PV generation, ESS integration and EV fast charging. Furthermore, depending on their structure and functionalities, PPP architectures can be divided in 3 groups: DPC, PPC and Mixed strategies. On the one hand, DPC architectures' main objective is to balance current mismatches between series connected elements. As observed in Table 1, the processed power ratio of this type of converters varies according to the mismatch between the elements. If there is no mismatch, the converter does not process any power. However, the main disadvantage of this type of PPP strategy is that it requires an extra power converter for adapting the voltage of the series elements to the voltage bus. On the other hand, when it comes to PPC

architectures, their main objective is to control the power flow and adapt the voltage levels between a source and a load. They can be divided in two sub-groups: architectures that require isolated topologies and architectures that do not. By comparing their K_{pr} curves (Figure 6 and Figure 8), it is concluded that for a step-up application, the implementation of an IPOS step-up or a FC step-up entails a trade-off between the processed power ratio and the simplicity of the power conversion circuit. Same thing would happen for a step-down application between, ISOP step-down and a FC step-down. Finally, there are the mixed PPP strategies, which offer alternatives combining DPC and PPC solutions.

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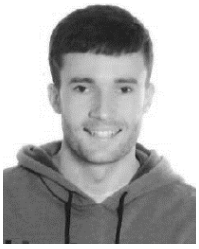

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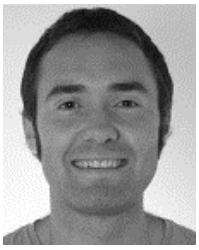

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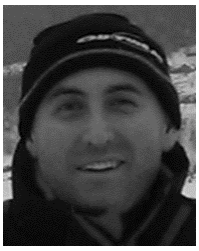

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