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IMPACT OF WIDE BANDGAP SEMICONDUCTORS ON VERTICAL TRACTION SYSTEMS

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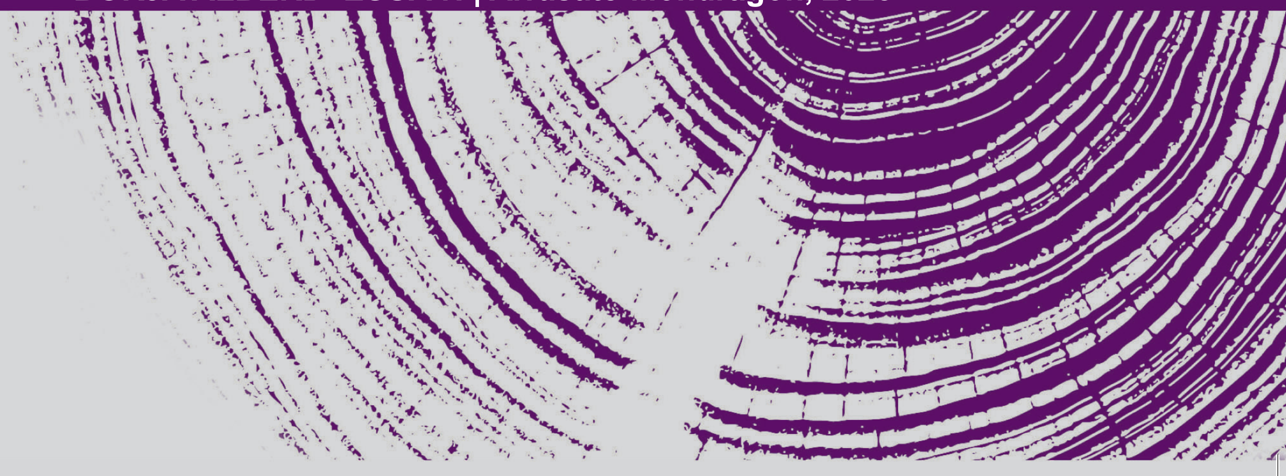

Mondragon Unibertsitatea Goi Eskola Politeknikoa

Impact of Wide Bandgap Semiconductors on Vertical Traction Systems

Borja Alberdi Esuain

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Impact of Wide Bandgap Semiconductors on Vertical Traction Systems

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Presented by
Borja Alberdi Esuain
Directed by
Dr. Mikel Mazuela Larrañaga
Dr. Jon San-Sebastian Bengoetxea

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Acknowledgments

If someone had asked me four years ago how I would see myself today, I'm not sure how I would have responded, but I certainly wouldn't have imagined how much this journey would give me. Apart from reinforcing my interest and ambition in power electronics, for which I am especially grateful to my university professors, this journey has been quite a rollercoaster of emotions. Sometimes, I have experienced moments of joy and happiness, but also stress, sadness, and moments of desperation. It hasn´t been an easy journey, but everything becomes much easier when you are surrounded by the right people. And in that sense, I have been really lucky.

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Amaitzeko, eskerrik asko huts egiten ez duten lagun hoiei. Zuri ere, Maria, behar nuenean nire alboan egoteagatik, beti entzuteko eta laguntzeko prest. Eta batez ere familiari. Ama, aita, Itsaso eta Beñat, nahiz eta batzuetan urrun egon arren, beti gertu sentitu zaituztet ibilbide luze honetan, behar nuen bultzada ematen. Hitzak ez dira nahiko ematen didazuen guztia eskertzeko.

Eskerrik asko denoi,

Abstract

As global energy demands grow and competition intensifies, industries face the dual challenge of reducing emissions while maintaining performance. In this context, optimizing power management systems, which are built around semiconductor transistors, plays a key role. Silicon has long dominated this field, but the emergence of Wide BandGap (WBG) semiconductors, offering superior electrical properties, is set to reshape the landscape. Leveraging their advantages can enhance the competitiveness of power electronics, though their adoption requires a comprehensive system redesign. The full potential of WBG materials in industrial applications remains underexplored, and further research is needed. This thesis presents a comprehensive study and practical framework for the integration of WBG semiconductors in power electronic systems. The document begins with a state-of-the-art review of WBG materials and emerging semiconductor technologies, comparing their advantages using various Figures of Merit (FOM) and examining current market trends, Chapter 2. Chapter 3 focuses on GaN HEMT technology, with particular emphasis on Gallium Nitride (GaN) Gate Injection Transistors (GIT) for high-voltage applications. Key integration challenges are discussed, supported by experimental analysis of critical factors such as saturation current, dynamic on-resistance, and short-circuit robustness. To support WBG integration in power converter design, an equation-based, customizable analytical model is developed in Chapter 4, which is configured to estimate switching transitions and power losses. The model is validated experimentally using a Silicon Metal Oxide Field Effect Transistor (MOSFET) push-pull DC/DC converter. In Chapter 5, the lift application is explored as a case study, and after studying various possible scenarios for WBG integration, a GaN-based DC/DC converter is designed. In this design, the presented tool is employed and experimentally validated, confirming the model's applicability to WBG devices. A soft-switching converter using Si-MOSFETs is also developed under the same specifications, enabling a comparative discussion of hard- vs. soft-switching topologies across semiconductor technologies. Lastly, a high-voltage GaN HEMT converter design is presented, outlining future research directions and concluding the work.

Laburpena

Industriaren energia eskaera handitzen joan da azken urteetan zehar, eta honekin batera negutegi efektuko isuriek marka berriak hautsi dituzte. Industriako sektore ezberdinak birplanteatzeko beharra dago, ikuspuntua mundu iraunkorrago batean jarrita, baina aldi berean, lehiakortasuna mantentzea funtsezkoa da hainbat sektoretan. Energiaren kontrolak eta manipulazioak garrantzi handia dauka ikuspuntu berri honetan. Potentzia elektronikari erreparatuta, material erdieroaleetan oinarritutako transistoreak erabili dira bihurgailuak sortzeko, eta orain arte Silizioa izan da transistoreak eraikitzeko erabili den materiala. Transistoreen eskaera mailaren hazkundearekin batera hobekuntza jarraia jasan du teknologia honek gaur egun arte; alabaina, azken urteetako material erdieroale berriek, banda zabaleko erdieroaleek (WBG) hain zuzen ere, Silizioak baino ezaugarri elektriko hobeagoak eskaintzen dituzte. Banda zabaleko erdieroaleetan oinarritutako transistoreek egungo bihurgailuak birplanteatzeko eta hobetzeko aukera ematen digute. Hala ere, transistore hauen portaera eta eskaintzen dituzten onuren aprobetxamendua aztertzeko dago oraindik, eta Silizioan oinarritutako sistema batetan integratzea ez da berehalakoa. Horregatik, tesi dokumentu honetan, banda zabaleko transistoreak egungo potentzi elektronikan integratzeko prozesua eta honen inguruan egindako ikerketa biltzen dira. 1. kapitulua tesiaren sarrerari eta planteamenduari dagokio. Dokumentu honen 2. kapituluan Siliziozko eta WBG erdieroaleen egungo egoera azaltzen da. Hainbat adierazleei (FOM ezberdinei) erreparatuta, teknologia hauen konparaketa erakusten da, merkatuaren joera berriak azalduz. 3. kapituluan, GaN teknologiaren ikerketa sakonago bat aurkezten da. Bertan, GaN GIT transistoreen ezaugarriak eta ezberdintasunak aztertzen dira tentsio altuko aplikazioetarako, bereziki saturazio korrontean, erresistentzia dinamikoan, eta zirkuitu laburreko ezaugarrietan erreparatuta. Banda zabaleko erdieroaleen integrazioa errazteko, ekuazio polinomikoak oinarri bezela hartuz modelo analitiko bat garatu da 4. kapituluan, transistore ezberdinen konparaketa egiteko eta hauen uhin forma kritikoak estimatzeko erabili dena. Aurkeztutako modelaketa prozesua Siliziozko push-pull bihurgailu batekin balidatu ondoren, 5. kapituloan, trakzio bertikaleko sistema baten nondik norakoak azaltzen dira, potentzi elektronikako ikerketa kasu bezela. GaN erdieroaleak erabiliz, eta aurkeztutako modeloen laguntzaz, DC/DC bihurgailu baten diseinua gauzatu da. Propotipoaren emaitzak alderatzeko asmoz, beste DC/DC bihurgailu bat disenatu da, oraingoan Siliziozko MOSFETak erabilita, baina konmutazio gogorrak izan ordez, konmutazio lehunak lortzeko topologia aldaketa bat proposatu da. Azkenik, GaN GITetan oinarritutako hirugarren bihurgailu baten diseinua aurkezten da, eta dokumentuari amaiera emateko, etorkizunerako ildoak eta tesian lortutako ondorio nagusiak aurkezten dira.

Resumen

En las últimas décadas, el aumento de la demanda energética industrial ha impulsado récords históricos de emisiones. Para mitigar el cambio climático, es necesario replantear los sectores industriales con un enfoque sostenible. No obstante, la alta competitividad de algunos sectores dificulta esta transformación. En este contexto, el control y la conversión de energía eléctrica cobran especial relevancia. La electrónica de potencia moderna ha evolucionado gracias al Silicio, cuyo uso en dispositivos de potencia ha alcanzado un alto grado de madurez, acercándose a los límites físicos del material. No obstante, todo apunta a un cambio de rumbo, donde nuevos materiales semiconductores de banda ancha prohibida (WBG) prometen mejores prestaciones eléctricas que las del Silicio. Estos semiconductores ofrecen la posibilidad de rediseñar y mejorar la electrónica de potencia actual. Sin embargo, todavía queda trabajo y tiempo de investigación hasta llegar a la integración completa de estos nuevos dispositivos. Una vez se han definido las bases fundamentales de la tésis a desarrollar en el Capítulo 1, el documento prosigue con una revisión del estado del arte sobre los materiales WBG y las nuevas tecnologías de semiconductores, comparando sus ventajas mediante diversas Figuras de Mérito (FOM) y analizando las tendencias actuales del mercado, Capítulo 2. El Capítulo 3 se centra en la tecnología GaN HEMT, con especial énfasis en los dispositivos GaN GIT para aplicaciones de alta tensión. Se discuten los principales desafíos de integración, respaldados por análisis experimentales de factores críticos como la corriente de saturación, la resistencia dinámica en conducción y la robustez frente a cortocircuitos. Para facilitar la integración de dispositivos WBG en el diseño de convertidores de potencia, en el Capítulo 4 se desarrolla un modelo analítico flexible basado en ecuaciones polinómicas, configurado para estimar las transiciones de conmutación y las pérdidas de potencia. El modelo se valida experimentalmente mediante un convertidor push-pull DC/DC basado en Si-MOSFET. En el Capítulo 5 se estudia la aplicación en sistemas de elevación como caso de estudio. Tras analizar diversos escenarios posibles para la integración de WBG, se diseña un convertidor DC/DC basado en GaN. En este diseño se utiliza y valida experimentalmente la herramienta presentada, confirmando su aplicabilidad a dispositivos WBG. También se desarrolla un convertidor con conmutaciones suaves utilizando Si-MOSFETs bajo las mismas especificaciones, lo que permite una comparativa detallada entre topologías de conmutación dura y suave a través de diferentes tecnologías de semiconductores. Finalmente, se presenta el diseño de un convertidor de alta tensión basado en GaN HEMTs, y se concluye el documento señalando posibles líneas de investigación futuras.

Declaración de originalidad

Yo Borja Alberdi Esuain declaro que este trabajo de disertación de la tesis doctoral es original, fruto de mi trabajo personal, y que no ha sido previamente presentado para obtener otro título o calificación profesional. Las ideas, formulaciones, imágenes, ilustraciones tomadas de fuentes ajenas han sido debidamente citadas y referenciadas.

Hereby I, Borja Alberdi Esuain declare, that this document is my original authorial work, which I have worked out by my own. All sources, references and literature used or excerpted during elaboration of this work are properly cited and listed in complete reference to the due source.

Hernani, 2025

Borja Alberdi Esuain

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List of Abbreviations

C_{sw}	Switch Node Capacitance
L_{G}	Gate Loop Inductance
L_{S}	Common Source Inductance
L_{loop}	Power Loop Inductance
2DEG	Two Dimensional Electron Gas
AFE	Active Front End
ARS	Automatic Rescue System
BAT	Best Available Technologies
BGA	Ball Grid Array
BJT	Bipolar Junction Transistor
BNAT	Best Not-yet-Available Technologies
CCM	Continuous Conduction Mode
CCPAK	Copper Clip Package
CSP	Chip-Scale Packages
D2PAK	Double Decawatt Package
DCM	Discontinuous Conduction Mode
DFE	Diode Front End
DFN	Dual Flat No-lead
DOD	Door Operator Drive
DPT	Double Pulse Test
DUT	Device Under Test
EMC	Electromagentic Compatibility
EMI	Electromagentic Interference
EMN	Energy Management Node
EMS	Energy Management System
ESS	Energy Storage System
FDA	Frequency Domain Analysis
FEM	Finite Element Method
FET	Field Effect Transistor
FHA	First Harmonic Approximation
FOM	Figure of Merit
FRD	Fast Recovery Diode

GaN	Gallium Nitride
GIT	Gate Injection Transistor
HEMT	High Electron Mobility Transistor
HNO	Hybrid Normally-off Structures
HS	Hard-Switching
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
LGA	Land Grid Array
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking strategy
MRL	Machine Room-Less
MRN	Manual Rescue Node
OVMC	On-state Voltage Measurement Circuit
PMSM	Permanent Magnet Synchronous Machine
QFN	Quad Flat No-lead
RES	Renewable Energy Sources
SBD	Schottky Barrier Diode
SBD	Schottky Barrier Diode
SGT	Schottky Gate Transistor
Si	Silicon
SiC	Silicon Carbide
SMPS	Switch Mode Power Supplies
SOA	Safe Operating Area
SPICE	Simulation Program with Integrated Circuit Emphasis
TDA	Time Domain Analysis
TO	Transistor Outline
TOC	Typical Output Characteristics
TOLG	TO-Leaded with Gullwing
TOLL	TO-Leadless Package
TOLT	TO-Leaded Top-Side cooling
UPS	Uninterrupted Power Supply
VNA	Vector Network Analyzer
VSI	Voltage Source Inverter
WBG	Wide BandGap
WLCSP	Wafer Level Chip Scale Package
ZCS	Zero-Current-Switching
ZVS	Zero-Voltage-Switching

Chapter 1

INTRODUCTION

1.1. Background

The foundation of the modern semiconductor industry can be traced back to the invention of vacuum tubes in the early 20th century. However, the true beginning of semiconductor technology as it is known today started with the invention of the transistor. In 1925, Austro-Hungarian physicist Julius Edgar Lilienfeld proposed and filed a patent for the first concept of a Field Effect Transistor (FET). Unfortunately, he could not materialize the idea due to technological limitations at the time. The breakthrough came in 1947 when American physicists John Bardeen, Walter Brattain, and William Shockley at Bell Labs demonstrated the first working transistor, known as the point-contact transistor. This was followed by Shockley's invention of the Bipolar Junction Transistor (BJT) in 1948, which marked a significant milestone in semiconductor technology. Over the next decade, various types of transistors were developed. However, it was not until 1959, following the experimental work on surface passivation by Egyptian engineer Mohamed Atalla, that the modern Metal Oxide Semiconductor Field Effect Transistor (MOSFET) was invented. The MOSFET became a cornerstone of modern electronics due to its scalability and efficiency. Later, the Insulated Gate Bipolar Transistor (IGBT) was conceptualized and patented by K. Yamagami and Y. Akagiri of Mitsubishi Electric. The first experimental demonstration of the IGBT was achieved in 1979 by B. Jayant Baliga and Margaret Lazeri. This device combined the advantages of MOSFETs and BJTs, making it highly suitable for power electronics applications. From vacuum tubes, various materials and structures have been used to create transistors. Today, MOSFETs and IGBTs are the most studied and optimized devices in power electronics, [1]. Most of the modern transistors are based on Silicon (Si). This material undergoes doping and microfabrication processes in a wafer format before being sliced and encapsulated in protective packaging to create the power device. Each step, from material to transistor, defines the ratings of the final result. The quality of wafer processing and packaging has been constantly improving in recent years, until reaching the point where the main bottleneck to improve the transistor has become the Silicon material itself. In this scenario, the research for new semiconductor materials with better properties than Silicon has seen an increasing trend. Two promising materials that have gone further than laboratory experimentation are Silicon Carbide (SiC) and Gallium Nitride (GaN), also known as Wide BandGap (WBG) materials.

Some of the main advantages of WBG materials include faster transitions between conductive / non-conductive states, better conductivity, and faster electron mobility, which result in transistors with higher switching frequency capabilities and lower power losses, [2], [3]. As a result, these transistors can outperform their silicon-based counterparts. With higher switching frequencies and lower losses, the power converters can be reduced in size and volume, and the

efficiency can be increased, reducing the overall electricity demand towards a greener electric system.

1.1.1. Electrical properties of WBG and Si

From the semiconductor's perspective, WBG materials are known for having a wider bandgap level than Silicon, over 2 eV. This means more energy is needed to add or remove an electron from the valence or conduction band. Currently, various WBG materials are available in the industry. Among all of these, GaN and different types of SiC are the most promising materials for power semiconductor devices. The most important parameters of semiconductor materials are shown below in Table 1.1.

Table 1.1: Properties and electrical characteristics of semiconductor materials [1].

Material property	Si	3C-SiC	4H-SiC	6H-SiC	GaN
Bandgap, E_g (eV)	1.12	2.3	3.26	2.9	3.4
Thermal conductivity, K (W/mK)	253	490	490	490	253
Electron mobility, μ_n (cm^2/Vs)	1400	1000	800	415	2000
Hole mobility, μ_p (cm^2/Vs)	450	45	115	101	305
Electron Saturation Velocity, V_{nsat} (10^6 cm/s)	10	25	22	19	14
Critical Electric Field, E_c (MV/cm)	0.3	2	3.18	2.4	4.9
Relative Permittivity, ϵ_r	11.9	9.6	9.7	9.7	10.4

These values are for pure material and do not include the variations generated when power devices are created with them.

Bandgap

The bandgap or energy gap is the energy that the electrons need in a solid material to move freely in the crystal lattice and conduct an electric current. The wider bandgap of SiC and GaN means that these materials' electrons need more energy than Silicon to become free electrons, but at the same time, they can withstand higher temperatures without changing the materials' state and have lower leakage currents. The bandgap is also related to higher critical electric fields. GaN has the widest bandgap between the listed materials with 3.4 eV, followed by 4H-SiC with 3.26 eV.

Thermal conductivity

The thermal conductivity indicates the capability of the material to dissipate heat. A higher thermal conductivity is related to faster heat dissipation, which becomes a critical parameter when losses are generated by conduction and switching current. The packaging of commercial devices is also critical for heat dissipation, worsening the overall thermal conductivity of the power device. SiC is known for having the highest thermal conductivity, with 490 W/mK, and for this reason, it is gaining attention for high-temperature applications. On the contrary, GaN does not improve thermal conductivity compared to Si, so special care and focus are

taken when designing the packages and the thermal dissipation systems of devices based on this material.

Electron Mobility

The material's resistance $R_{\mathrm{DS(on)}}$ is dependent on the mobility of electrons (μ_{n}), the number of electrons (N_{D}), and the width of the channel or drift region (w_{drift}).

$$R_{\mathrm{DS(on)}} = \frac{w_{\mathrm{drift}}}{q\mu_{\mathrm{n}}N_{\mathrm{D}}} \tag{1.1}$$

Where q is the charge of electrons ($1.6 \cdot 10^{-19}$ C). At the same time, the critical field, E_{c}, the permittivity (vacuum permittivity ϵ_0 can be approximated as $8.854 \cdot 10^{-12}$ F/m, and the relative permittivity of the material,ϵ_{r}), and the width of the channel w_{drift} define the number of electrons, N_{D}.

$$N_{\mathrm{D}} = \frac{\epsilon_0\epsilon_{\mathrm{r}}E_{\mathrm{c}}}{w_{\mathrm{drift}}q} \tag{1.2}$$

So, from these previous expressions, the following definition of ON-resistance is obtained.

$$R_{\mathrm{DS(on)}} = \frac{w_{\mathrm{drift}}^2}{\mu_{\mathrm{n}}\epsilon_0\epsilon_{\mathrm{r}}E_{\mathrm{c}}} \tag{1.3}$$

Higher electron mobility is inversely proportional to ON-resistance $R_{\mathrm{DS(on)}}$, meaning the higher electron mobility of wide-bandgap devices offers lower conduction losses. GaN provides the best conductivity over Si and SiC.

Critical Electric Field

The critical electric field E_{c} is the maximum electrical field that the material can withstand without failure. From the power electronics point of view, it defines the breakdown voltage of the transistor (V_{BR}).

$$V_{\mathrm{BR}} = \frac{1}{2}w_{\mathrm{drift}}E_{\mathrm{c}} \tag{1.4}$$

Where w_{drift} is the width of the drift region. Among the compared semiconductor materials, GaN has the higher critical field, and theoretically, it can withstand almost 15 times higher breakdown voltage than Silicon; in other words, the same V_{BR} can be achieved with 15 times closer terminals. This is translated into a 15 times thinner drift region and, as demonstrated in (1.3), 15^2 times lower ON-resistance. However, up to now, GaN transistors do not exploit the full potential of the material due to their structure, as pure vertical GaN transistors are not available. On the other hand, SiC MOSFETs use the drift region to conduct the current, so higher breakdown voltages than lateral structures are achieved.

Relative Permittivity

As well as having closer terminals, WBG materials offer lower relative permittivity than Silicon, which allows for decreasing even more the conductive resistance of the material (equation (1.3)). Relative permittivity reflects the material's ability to store static energy in an electric field. A lower value is preferred in power electronics as it decreases the build-up of static charge in the material and, in consequence, the parasitic capacitance values, decreasing switching losses.

1.1.2. Dynamic performance of WBG and Si

The electrical differences in the materials provide unique conditions for creating power semiconductors for power electronics. GaN and SiC have the right properties to create more compact and, therefore, faster power switches compared to Silicon-based ones, which can be used to improve state-of-the-art Switch Mode Power Supplies (SMPS). The electrical properties mentioned above are key factors to improve switching performance, [4].

The insulator separating the *Gate* from the *Body* and the dielectric capacity of the material are the main causes of parasitic capacitances limiting the maximum switching speed. These capacitances can be identified as the capacitances created between the *Gate* and the *Drain* (C_{GD}), the *Gate* and the *Source* (C_{GS}), and the *Drain* and the *Source* (C_{DS}). Note that this nomenclature corresponds to field effect transistors, but a similar notation can be used for IGBTs (similarly extendable to BJTs) as *Collector-Gate* capacitance (C_{CG}), *Emitter-Gate* capacitance (C_{EG}), and *Collector-Emitter* capacitance (C_{CE}). Manufacturers usually give the information about these capacitances in values of input capacitance (C_{ISS}), output capacitance (C_{OSS}), and feedback capacitance (C_{RSS}).

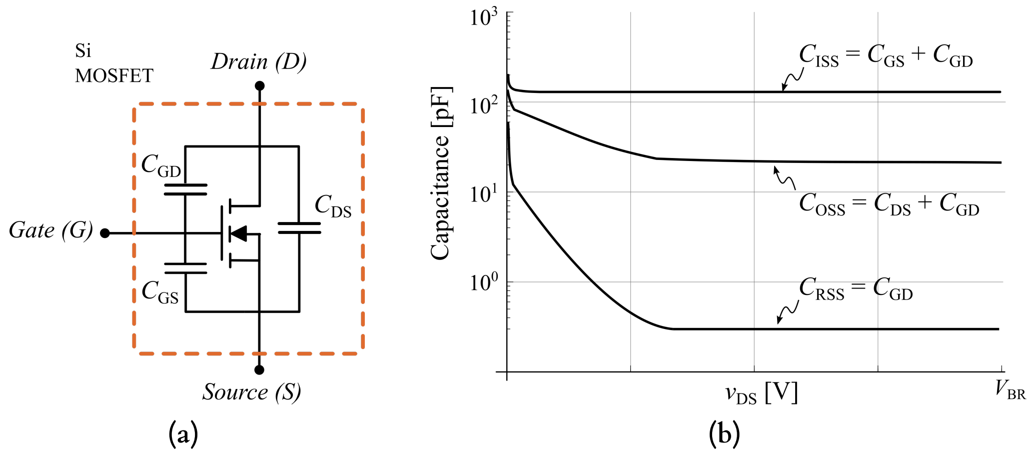


Figure 1.1: Typical simplified MOSFET model with equivalent parasitic capacitances in (a), and parasitic capacitance values given in a datasheet in (b).

The gate-source capacitance (C_{GS}) can be considered approximately constant. However, the output capacitance (C_{OSS}), which is the combination of C_{DS} and C_{GD}, varies significantly with the drain-source voltage. This variation is primarily due to the Miller capacitance (C_{GD}), which depends on the depletion region of the drain junction and changes with the drain voltage [5]. Another important parameter is the charge needed to supply the *Gate* terminal to charge the input capacitances and to increase gate voltage enough to sustain the ON state, which is referred to as Q_G. The relation between Q_G and V_{GS} is not linear, as more than one process is involved, Fig. 1.2. First, gate-source capacitance is charged (Q_{GS}). The gate voltage increases above the threshold voltage, where the drain current starts increasing. Once the drain current reaches the current required at the power circuit, the drain voltage, which was at V_D, starts to decrease (V_{DD} in the figure). During this stage, the Miller capacitance is discharged (C_{GD}), as it was previously charged at V_{DD} (during the OFF state of the MOSFET). This gate voltage level is known as the voltage plateau or Miller plateau, and the gate voltage remains almost constant during this Miller stage. Once that Miller capacitance is fully discharged, the gate voltage can continue increasing to reach the desired value. The process is inverted for switch-OFF transitions.

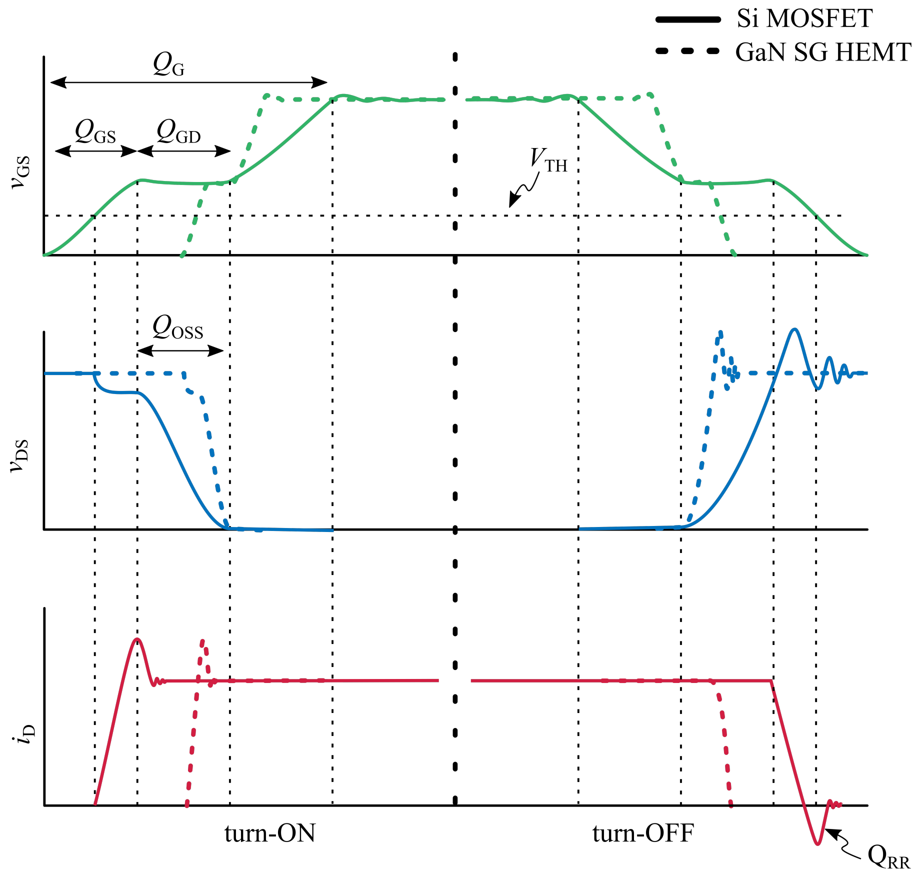


Figure 1.2: Si-based MOSFET and GaN-based SG High Electron Mobility Transistor (HEMT) approximated voltage and current waveforms during turn-ON and turn-OFF transitions. [6]

The driver circuit is responsible for supplying the sum of the gate charges to the transistor, Q_G, so it is a crucial part of defining the switching speed of the device. At the same time, wide-bandgap materials offer the possibility to create lower area transistors than silicon for the same working conditions, reducing parasitic capacitance values, and increasing the switching speed and frequency limits compared to silicon devices. These properties of GaN and SiC enable the construction of converters with higher efficiencies, lower volumes, and higher working temperatures than Silicon-based ones [7]. GaN and SiC seem to be promising materials to dominate today's market, each one being more suitable for certain applications, as depicted in Fig. 1.3.

SiC has reached its adoption earlier than GaN in the industry. Their wide bandgap permits the creation of already known structures, like MOSFETs and IGBTs, for applications over 650 V, outperforming Silicon-based transistors. Therefore, for now, SiC is mostly employed in applications with voltages over 650 V, and GaN is still working its way under this voltage level with HEMT structure. Both technologies are covered in the following.

Although their outstanding features, WBG materials still have some drawbacks to be taken into account. On the one hand, the switching transitions with the new materials can be faster than with Silicon, producing steeper current or voltage derivatives, which roughly translates into maximization of the parasitic effects of the circuit. These transitions also affect EMI/EMC emissions negatively, requiring higher effort for filtering. In the end, the current circuitry must be redesigned and optimized to keep every part working under safe conditions. The control circuits and measurement methods used with Silicon transistors can lead to inaccurate

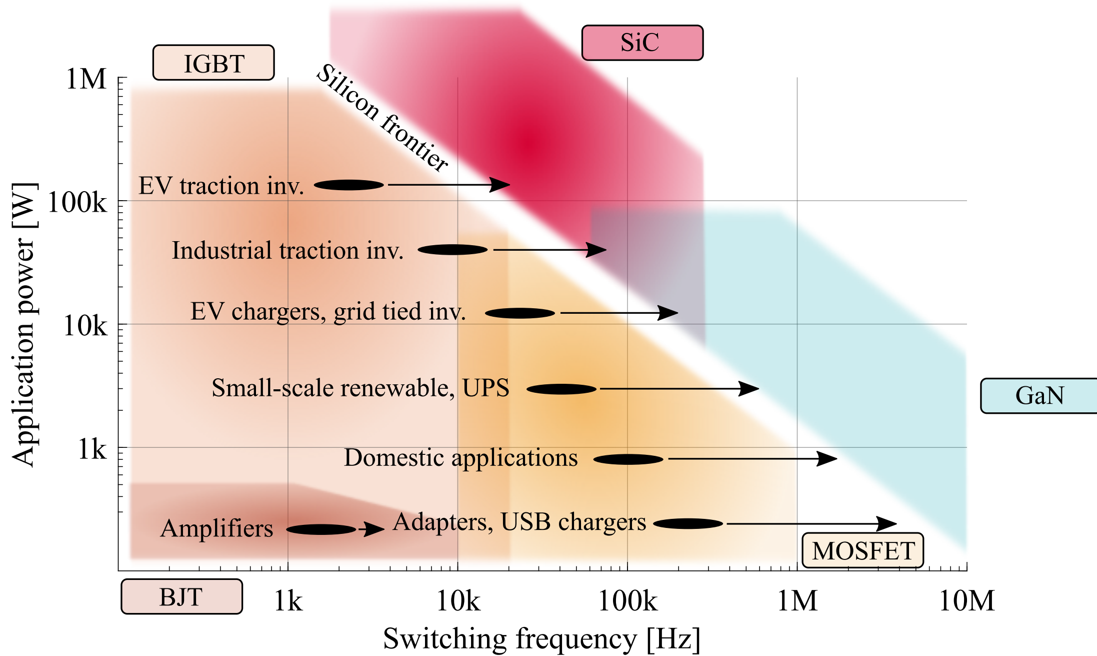


Figure 1.3: Application range and scope for wide-bandgap materials [7]

results or even unwanted behaviours when using WBG transistors, requiring higher precision and wider bandwidth equipment for the designs.

On the other hand, the price of transistors is closely related to their demand. Silicon has been used practically in every power converter until the last few years. Its high demand rate has decreased Silicon-based transistor prices to very competitive values. On the contrary, the emerging materials are still being researched and the transistors optimized, gaining popular trustworthiness little by little, so they are not fully adopted in the current market yet. The lower demand for new materials entails a higher price, which can not compete against Silicon. However, the benefits can be exploited to have stronger significance than the device price difference for the end user.

1.1.3. Challenges with the use of WBG semiconductors in power electronics

Modelling of SiC and GaN Devices

Modelling WBG devices is a complex task due to their unique working principles and fast evolution. Their high-speed switching characteristics and intricate internal current paths complicate the estimation of their behaviour under different working conditions. While simulation tools like Simulink or LTSpice can integrate predefined models created by manufacturers, their accuracy and transparency vary. The difficulty of creating an electrical model for WBG devices lies in the prediction of the current flowing through the different paths in the device, and the prediction of the power losses within them. The primary path for the current is the channel, which is the main source of the power losses, but as the switching speed has increased the current flowing through the parasitic capacitances of the device becomes significant, [8], and using the drain current i_{D} for power loss estimation may lead to significant errors compared to the real behaviour of the device. The channel current, i_{ch}, can not be measured directly,

and estimations are needed to predict this current and, therefore, calculate the power losses. A model capable of predicting the channel current is necessary, especially for GaN devices, while being computationally efficient, achieving a good balance between accuracy and speed.

An analytical model of the semiconductor device can be used to obtain fast results based on mathematical equations and the values provided in the datasheets. While this approach has been widely used for silicon-based devices, its applicability to SiC and GaN is still under investigation, [9]–[10]. Several assumptions are taken during the process to simplify the problem, [11]. This method is preferred over physical and behavioural modelling for analyzing multiple scenarios and multi-objective optimization problems, for instance, due to their good compromise with accuracy and computational effort.

On the other hand, behavioural models represent device behaviour using equivalent electrical circuits composed of capacitors, inductors, and current sources. The circuit's complexity will determine the precision of the model compared to real behaviour. For example, a simplified model can be observed in Fig. 1.4 where the power device is represented by an electrical circuit with capacitors, resistors, and a current source, [12]–[13].

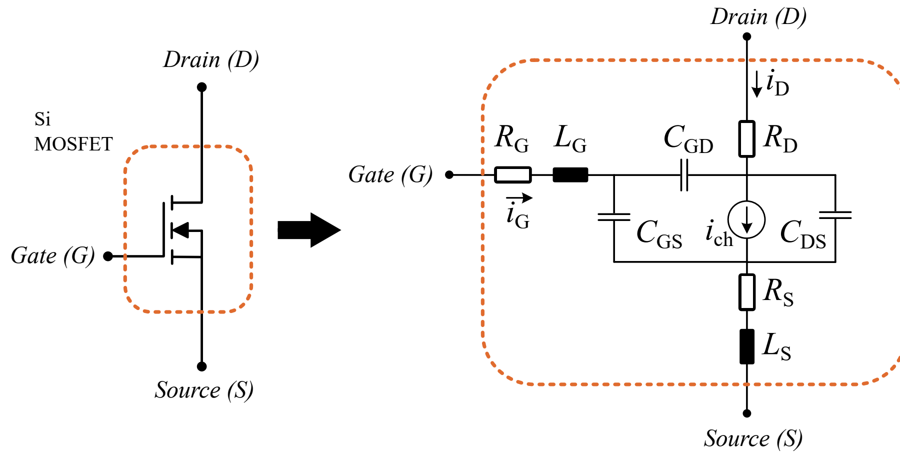


Figure 1.4: Symbol and equivalent circuit of a Silicon-based enhanced mode MOSFET.

The values of the capacitors C_{GS}, C_{GD} and C_{DS} are variable, and R_G, R_D and R_S correspond to the gate, drain and source parasitic resistances respectively. These values vary with different power devices. Apart from the internal structure of the power devices, the packaging of the device and the PCB parasitic inductances can also be represented in the diagram shown in Fig. 1.4, obtaining more precise results.

Once the electrical losses are calculated by analytical equations or electrical models, the thermal behaviour is studied. For that, analytical approaches can also be used, converting directly the power losses into temperature values, or it can be modeled by an electrical circuit as it is typically done with Si devices, Fig. 1.5. Infineon [14], [15], Nexperia [16], and other manufacturers provide information about this modelling technique and the corresponding values of each of the electrical variables in the datasheets. For the equivalent circuit, the thermal resistances must be estimated from the device's junction to the ambient. These resistances depend on the path from which the heat is dissipated, the way the PCB is routed, the method used (heatsink, vias,...), and the power device packaging. In the case of GaN transistors, a wide variety of packaging types can be found in the market, from through-hole to surface-mounted, which complicates the unification of a unique thermal equivalent circuit.

Thermal and electrical models are essential for sizing components such as heatsinks, induc-

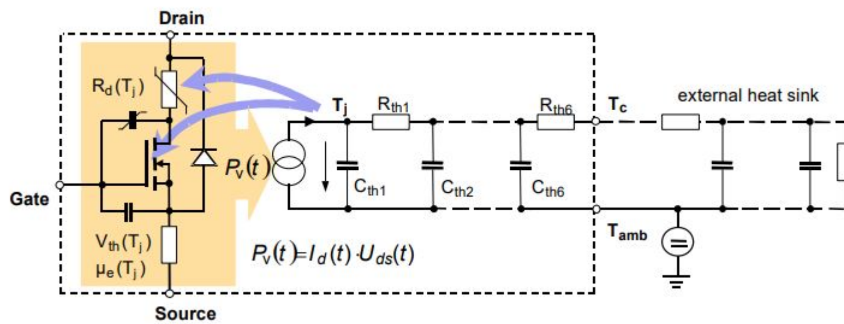


Figure 1.5: Principle circuit diagram of a model with an interactive coupling of electrical and thermal component description, [14].

tors, and capacitors. Their volume and cost depend on material selection, current and voltage waveforms, and converter topology. Cost models, such as the one presented in [17], integrate these factors into a comprehensive design process. The challenge lies in developing precise models that accurately capture interdependencies among electrical, thermal, cost, and volume characteristics.

Fast Dynamic Limitations and EMI Considerations

When using WBG semiconductors for power conversion, the fast dynamics of these switches can aggravate unwanted effects. The primary concern is the high voltage and current derivatives dv/dt and di/dt, which can induce voltage and current spikes due to stray inductances and capacitances in the circuit. As switching transients accelerate, these stray components become critical, [18], and depending on the application, they can have damaging effects on the power switch itself or even on the surrounding components. For instance, the dv/dt produced by the low-side switch in a half-bridge configuration can induce a circulating current through the high-side transistor's gate loop, affecting the gate voltage, and risking the correct operation of the power switch. On the other hand, the di/dt produced in the main power loop can create overvoltage spikes (v_{ov}) which can surpass the breakdown voltage of the used transistor. The v_{ov} produced in the gate by the high di/dt can also be problematic, especially in GaN-based devices due to the very sensitive gate characteristics.

SiC and GaN devices enable higher switching frequencies, providing greater design flexibility. They can reduce voltage and current ripple using passive components of the same size, allow for smaller components while maintaining similar ripple levels, or achieve a compromise between both approaches, depending on design priorities. However, the accelerated dv/dt and di/dt and the increased switching frequency also increase conducted and radiated Electromagentic Interference (EMI) emissions. Without proper design measures, these effects can degrade system performance and complicate EMI compliance. In various power conversion systems, the main sources are current ripple, which depends on the switching frequency, and leakage current (i_{lk}), which arises from the dv/dt applied to the stray capacitances of the circuit. Increasing the switching frequency reduces the current ripple magnitude but shifts its corresponding emissions to higher frequencies in the spectrum. For EMI caused by leakage current, its magnitude is determined by dv/dt, parasitic capacitances, and the switching frequency, with higher frequencies also shifting the associated emissions in the spectrum. In the case of DC/AC converters, the principle is the same, but it is more common to have higher stray inductance and capacitance values in the circuit, as they are used to drive inductive loads, electric motors, for instance. What is more, in typical Voltage Source Inverter applications

where the motor is directly connected to the output, increasing the switching frequency does not mean higher power density. Moreover, the connection cables and the insulations of the motor can worsen the EMI problems. The cables can be considered as inductances, and high *di/dt* can cause overvoltage spikes in the motor windings, [19]. At the same time, the insulations behave as stray capacitances, and *dv/dt* can cause current spikes which are harmful to the motor. Thus, the switching speed is typically limited. The problem can be mitigated using filters between the converter and the motor, increasing the volume and cost of the solution considerably. These filters' volume is reduced by increasing the switching frequency, so the use of WBG devices can be beneficial for the application in these cases.

Deadtime in half-bridge topologies affects EMI and power losses. For now, WBG devices have higher reverse conduction voltage drops than Si devices, increasing losses. A proper analysis of the required deadtime and the reverse conduction voltage drop is needed to minimize the reverse conduction losses and avoid excessive heating.

PCB layout optimization and integration

In power converters, the main source of parasitic inductances and capacitances is the layout of the PCB. Optimizing the layout is crucial for the converter's performance as well as EMI reduction. The interconnections between the power components, like the power switches and the input capacitors, generate void loops where high-frequency electric and magnetic fields are stored. Parasitic inductors and capacitors originate from these fields. The fast dynamics of WBG semiconductors worsen the impact of these parasitic elements in the performance of the power converter, and their influence can be catastrophic if they are not deeply analysed.

These high-frequency loops are generated during the arrangement of the different components of the power converter; therefore, special care should be taken when designing the PCB. The most important high-frequency loops to consider are the gate drive loop and the power loop. The gate drive loop is formed by the driver, the power device, and the high-frequency gate capacitor, whereas the power devices and the input capacitors form the power loop. In a half-bridge scenario with a bus capacitor, the power loop is formed by the two power switches and the high-frequency input capacitor. Both loops are depicted in Fig. 1.6.

When WBG is used for increasing switching frequencies, the parasitic inductances of these loops need to be minimized as much as possible. These inductances can be summarized into the Gate Loop Inductance (L_{G}), the Common Source Inductance (L_{S}), and the Power Loop Inductance (L_{loop}). The Switch Node Capacitance (C_{sw}) is also a key parasitic element in a half-bridge configuration.

The parasitic inductances and capacitances can be minimized by reducing the loop's physical size and therefore the magnetic and electric fields. Different techniques can be used to reduce the size of the loops, as placing the components as close as possible, in the same layer of the PCB, or on top of opposite layers, creating a vertical loop that depends on the width of the PCB. For the magnetic field cancellation, opposite traces and planes can be used where the current flows in opposite directions. In this way, the magnetic field generated by the planes or traces cancel each other, achieving a general reduction in the overall inductance value. A shielding layer can also be used, in parallel to the inductance loop, to generate a current flowing in the opposite direction and cancelling the magnetic field. Other approaches from the literature include the integration of the power devices inside the PCB, minimizing the power loop, and shielding the device as shown in Fig. 1.7, [20], [21], [22].

The current and voltage measurement method is another important factor to take into account when talking about parasitics. The measurement units introduce parasitic impedances

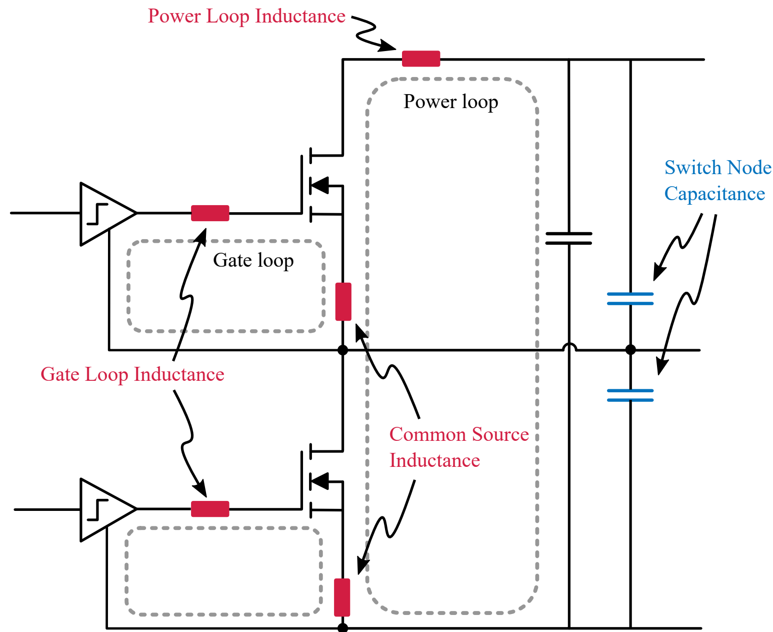


Figure 1.6: Simplified equivalent schematic of a half-bridge power stage showing power and gate drive loops with Power Loop Inductance, Gate Inductance, and Common Source Inductance

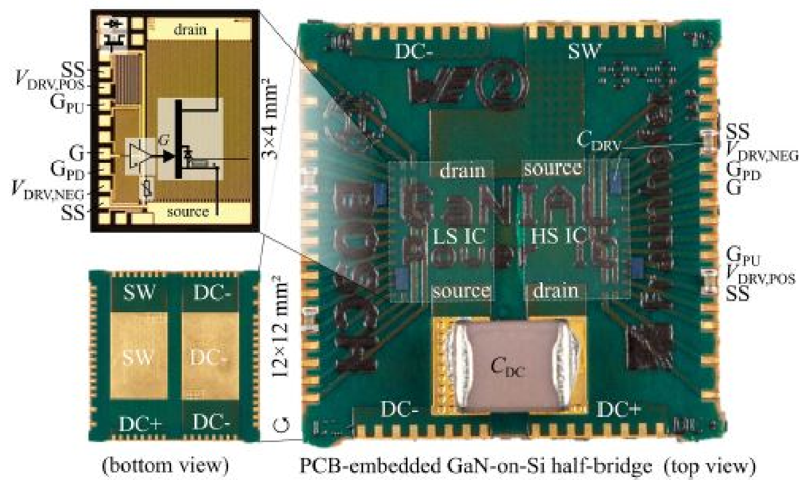


Figure 1.7: PCB-embedded GaN half-bridge with on-package gate/dc-link capacitors, [22].

in the circuit, and with high frequencies, it is recommended to have the lowest possible invasion level, especially in high-frequency loops. Least invasive methods include Hall sensors or Rogowski coils, but their bandwidth is typically limited to below 50 MHz, which is not enough to measure accurately the rise time and fall times of GaN devices for example, following the equation (1.5), [12]. Other, more invasive measurement units, such as current-sense resistors or coaxial shunts, can have bandwidths up to 2 GHz, but they have a much higher impact on the circuit.

$$t_{\text{rise}(10\text{-}90\%)} = \frac{0.35}{BW_{\text{-3dB}}} \tag{1.5}$$

where, the $BW_{\text{-3dB}}$ is the bandwidth of the measurement system, and $t_{\text{rise}(10\text{-}90\%)}$ is the

minimum rise time of the measurable transient.

The package of the power device is also critical in terms of parasitic elements. For example, various packages offer separate gate drive and power return paths, which enable the decoupling of the gate drive loop and the power loop, reducing the L_S. In general, the lower inductance packages come with the expense of lower chip size areas, and thus lower thermal dissipation areas. A good heat dissipation system is required to achieve high power density along with high efficiency in a power solution. As mentioned, the package type determines the possibilities of the thermal system. The bigger package enables direct connection with heatsinks, achieving better dissipation, whereas smaller chip size requires other techniques such as heat dissipation vias in the PCB, or Insulated Metal Base (IMS) PCBs, as shown in the example [23].

Modelling SiC and GaN devices requires a multi-faceted approach that balances electrical, thermal, cost, and EMI considerations. Analytical models provide quick insights, while behavioural models offer improved accuracy. Optimized PCB layout and careful dead-time control help mitigate EMI, ensuring high efficiency and reliability in power electronics applications. Achieving an optimal trade-off between thermal performance, EMI suppression, and overall efficiency remains a key challenge in WBG device integration.

1.2. Objectives

The primary objective of this thesis is to investigate the integration and performance enhancement of advanced power electronics solutions employing wide bandgap (WBG) transistors, harnessing the unique benefits of GaN and SiC semiconductor technologies. This study is carried out in the context of a vertical traction system, which comprises multiple converter topologies designed for distinct subsystem requirements. To accomplish this goal, the thesis follows a structured and multidisciplinary approach. It begins with the modelling and simulation of different semiconductor technologies and converter architectures to evaluate their electrical and thermal behaviour. This foundational analysis supports a comprehensive comparison of multiple design strategies, aimed at identifying the most promising solutions in terms of performance, reliability, and integration. The final phase involves the practical realisation and experimental validation of selected converter prototypes, thereby confirming the effectiveness of the proposed models and design methodologies.

Based on a critical review of the state-of-the-art, this work formulates and explores the following hypotheses regarding the use of WBG-based power converters:

- Replacing Silicon transistors with WBG devices leads to a significant reduction in overall power losses under equivalent operating conditions. Depending on the application and working point, efficiency improvements can range from 1% to 10%. This gain can potentially eliminate the need for bulky heatsinks, simplifying the thermal management system and enhancing the competitiveness and cost-efficiency of commercial products.
- WBG transistors enable operation at substantially higher switching frequencies—typically 2 to 10 times higher than their Silicon counterparts. This capability allows for a reduction in the size of passive components, such as inductors and capacitors, thus decreasing the overall converter volume while maintaining the required voltage and current ripple. These advantages can be leveraged to enhance existing functionalities or introduce new ones, such as increased output power or higher power density.
- Despite the higher unit cost of WBG devices, the reduction in passive component size and simplification of auxiliary systems (e.g., thermal management) can lead to lower overall converter costs. This system-level optimisation paves the way for more competitive and economically viable WBG-based solutions.
- The high-speed switching characteristics of WBG devices make converter performance more sensitive to parasitic inductances and capacitances. Therefore, careful design optimisation and parasitic minimisation are essential for reliable operation. The development and application of novel modelling techniques are critical not only for the effective integration of WBG devices but also for enhancing the performance of conventional Silicon-based systems.

To validate the previous hypotheses, the following sub-objectives are proposed:

- Analyse the various transistor structures employed in GaN and SiC technologies, assess the current market landscape, and identify key manufacturers and commercially available components relevant to power electronics applications.

- Formulate accurate electrical models that capture the behaviour of WBG devices under different operating conditions, including high-frequency operation and fast transient responses, enabling precise performance prediction and design optimisation.
- Model and design one or more power converters tailored to a specific application, demonstrating improvements in efficiency, volume, and cost over conventional designs. Apply multi-objective optimisation techniques to balance competing design constraints and exploit the full potential of WBG devices.
- Construct the designed converters and integrate WBG devices with careful attention to layout optimisation, minimisation of parasitic elements, and mitigation of high-frequency switching effects. Use experimental measurements to validate the analytical models and simulation results, thereby confirming the feasibility and advantages of the proposed solutions.

1.3. List of Publications

Journal articles

- B. Alberdi, M. Mazuela, J. San-Sebastian, R. Sánchez, A. Arruti and I. Aizpuru, "Design and Validation of a Cost-Effective 300 W GaN-Based Step-Up Push-Pull Converter," in IEEE Access, vol. 12, pp. 169533-169544, 2024, doi: 10.1109/ACCESS.2024.3494553.
- M. Chen et al., "MagNet Challenge for Data-Driven Power Magnetics Modeling," in IEEE Open Journal of Power Electronics, vol. 6, pp. 883-898, 2025, doi: 10.1109/OJPEL.2024.3469916.

Conference papers

- B. Alberdi, M. Mazuela, J. Azurza, C. Ostermaier, J. San-Sebastian and R. Sanchez, "Experimental Dynamic Saturation Current Evaluation of 650V GaN GITs," PCIM Conference 2025; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nürnberg, Germany, 2025, pp. 1581-1586, doi: 10.30420/566541207.
- C. Koller, M. J. Kasper, B. Butej, D. Wieland, B. Alberdi, and O. Häberlen, "Catalyzing Innovation: Bridging System Efficiency to Fundamental Device Physics," 2024 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2024, pp. 1-4, doi: 10.1109/IEDM50854.2024.10873485.
- B. Alberdi, M. Mazuela, J. San-Sebastian and R. Sánchez, "Switching losses estimation for a push-pull converter based on analytical models considering parasitic elements," 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023, pp. 1-8, doi: 10.23919/EPE23ECCEEurope58414.2023.10264274.

1.4. Dissertation Outline

CHAPTER 1 – INTRODUCTION

This chapter defines the motivation, scope, and objectives of the research. It introduces the role of WBG semiconductors in modern power electronics, and highlights their potential to improve efficiency, reduce size, and increase integration in vertical traction systems and auxiliary DC/DC converters.

CHAPTER 2 – SILICON AND WBG SEMICONDUCTORS: STATE OF THE ART

A comprehensive review of WBG device technologies is provided, focusing on their physical characteristics, packaging evolution, and application domains. SiC devices are studied for high-voltage and thermally demanding applications, while GaN devices are positioned as optimal candidates for compact, high-frequency systems. Key challenges, such as reverse conduction behaviour and gate sensitivity, are also addressed. A comparative Figure of Merit (FOM) analysis is included to benchmark GaN, SiC, and Si technologies under different switching conditions.

CHAPTER 3 – GAN TECHNOLOGY AND CHALLENGES

This chapter presents an in-depth experimental characterisation of GaN devices, focusing on three critical aspects: saturation current limits, dynamic on-resistance, and short-circuit robustness. Testing setups, including Zero-Current-Switching (ZCS) and a custom On-state Voltage Measurement Circuit (OVMC), are employed. The results highlight superior performance of GaN GITs over SGTs, and confirm their suitability for high-performance applications. Short-circuit results further demonstrate the feasibility of GaN-based designs for robust converter operation.

CHAPTER 4 – MODELLING WBG POWER TRANSISTORS

An analytical modelling tool based on the Double Pulse Test (DPT) is developed to predict switching waveforms and losses based solely on datasheet parameters and parasitics. The model incorporates gate and power loop inductances and is validated using a Silicon-based push-pull converter. The method achieves strong agreement with experimental data and offers high computational efficiency. It is then applied as a tool for comparing different semiconductor technologies and evaluating parasitic sensitivity across various converter topologies.

CHAPTER 5 – POTENTIAL APPLICATIONS FOR GAN

This chapter translates previous findings into practical converter designs tailored to elevator systems:

A high-frequency GaN-based push-pull converter is designed, optimised, and validated, achieving improved efficiency and reduced volume compared to the Silicon baseline.

A resonant LLC half-bridge converter is developed and experimentally characterised. Both Frequency Domain Analysis (FDA) and Time Domain Analysis (TDA) are used to optimise the resonant tank. Silicon MOSFETs are selected based on cost and soft-switching suitability.

A non-isolated synchronous buck converter is analysed to complement the LLC stage and provide output voltage regulation. GaN and SiC devices are compared, with GaN emerging as the most suitable candidate for this stage.

A combined LLC + Buck two-stage solution is proposed and benchmarked against the baseline and single-stage designs. The architecture demonstrates the highest efficiency under full regulation, while offering scalability, reduced volume, and competitive cost.

CHAPTER 6 – OUTLOOK AND CONCLUSIONS

The final chapter compiles the key insights of the thesis and outlines the broader implications of WBG integration in power converters for vertical mobility systems. Both fully WBG-based and hybrid WBG–Si solutions are discussed in terms of trade-offs between performance, reliability, cost, and volume. The chapter concludes with future directions, highlighting the relevance of the growing maturity of WBG technologies for next-generation power electronic systems.

Chapter 2

SILICON AND WBG SEMICONDUCTORS: STATE OF THE ART

This chapter introduces the fundamental concepts as well as the current situation of the semiconductor devices used in power electronics, providing a timeline and an overview of the technological evolution in power electronics. Starting with the description of different types of Silicon transistors, their operation mode is detailed and compared with Wide BandGap (WBG)-based transistors. Following this comparison, the chapter explores the landscape for power semiconductors, listing some of the main manufacturers and comparing available power semiconductor devices based on different Figure of Merit (FOM)s. To conclude this chapter, a literature review is presented, summarizing significant contributions from recent literature related to WBG integration in power electronics, providing a comprehensive understanding of the necessities and challenges faced when integrating new semiconductor technologies in power electronics.

2.1. Silicon and Wide Bandgap Semiconductors

Silicon (Si) is the main material used to create switching devices. Having four electrons in the outer shell of the atomic structure, the Fermi level lies between the conduction band and the valence band, needing equal energy to add or remove an electron. Silicon behaves as an insulator at room temperature; however, it can be doped using pnictogens such as phosphorus, arsenic, or antimony to add an extra electron per dopant, moving the Fermi level to the conduction band, creating an N-type semiconductor. On the other side, it can be doped using group 13 elements such as boron, aluminum, or gallium, to create a material more acceptable than repellent for electrons, creating a P-type semiconductor. Combining N-type and P-type semiconductor regions in the same substrate piece, the widely known semiconductor junction is created, which is shown in the next Fig. 2.1. As a consequence of the different potential levels of the regions, a depletion region or zone appears in between them, where free electrons are depleted to the P-type region and holes in the N-type region until reaching an equilibrium point. The semiconductor devices, like diodes or transistors, are constructed by combining layers or sequences of this structure in different ways.

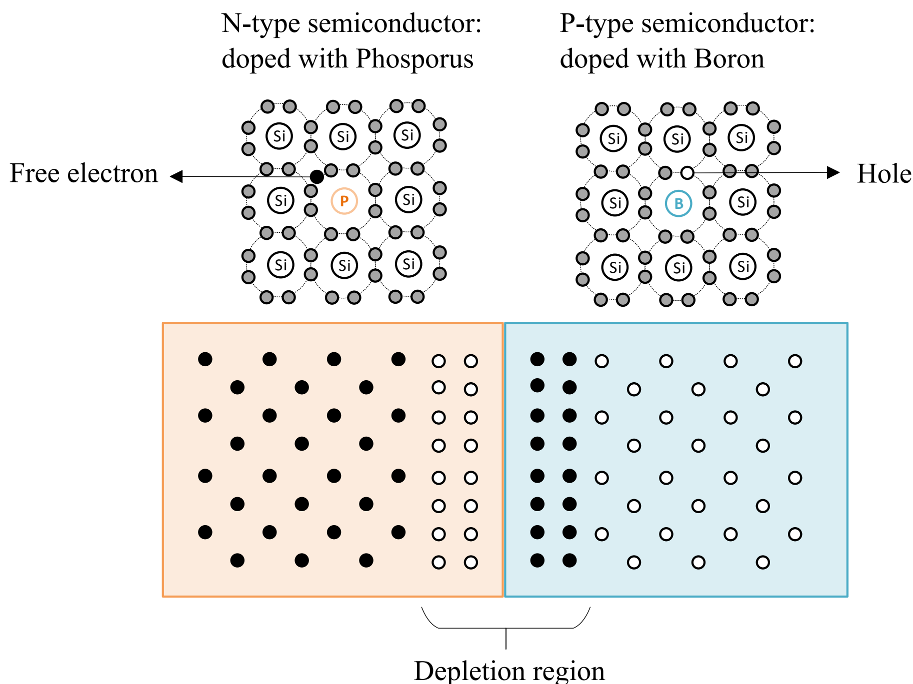


Figure 2.1: Typical semiconductor junction, combining N-type and P-type regions to create a depletion zone. Adapted from [24].

2.1.1. Silicon BJTs, MOSFETs and IGBTs

The Bipolar Junction Transistor (BJT) is created using one thin region of one of these two types of semiconductor in the middle of opposite type regions, following the 'sandwich' structure. It can be a PNP (P-type) structure, or an NPN (N-type) structure, Fig. 2.2. It is a bipolar transistor because it works using two types of carriers: electrons from N-type regions and 'holes' from P-type regions. Using a terminal connected to the middle region, called the *Base*, and applying a voltage between *Base* and *Emitter*, the minority carriers enter a recombination

process, opening the conductive path between *Collector* and *Emitter*. The figure shows a symmetrical representation of the BJT structure; however, in reality, the regions are optimized for forward conduction, and the external regions are not identical in dimensions.

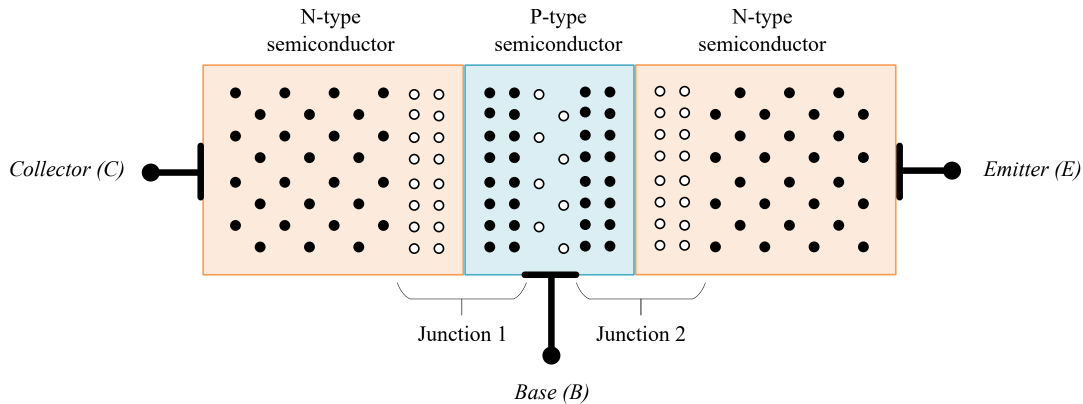


Figure 2.2: NPN type BJT representation showing the 'sandwich' structure. The three terminals are the *Base*, *Emitter*, and *Collector*. Adapted from [24].

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) working principle is also based on P-N junctions, however, the working principle is different from that of BJTs. The lateral MOSFET structure is formed by two conductive pads which are placed on top of the substrate, also called the *Body*, to create the main structure of the device as shown in Fig. 2.3 below. These two pads are named as the *Source* and the *Drain* terminals, and they are responsible for defining the beginning and the end of the conduction channel in the transistor.

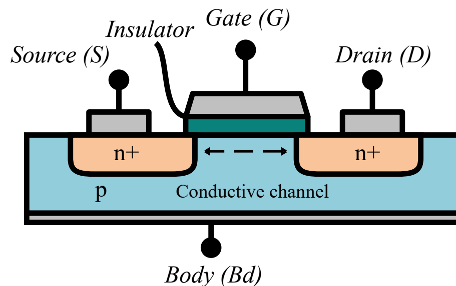


Figure 2.3: Lateral N-type Field Effect Transistor (FET) structure (NMOS), showing the semiconductor regions, and the four terminals corresponding to the *Drain*, the *Gate*, the *Source* and the *Body*. Adapted from [24].

Underneath each terminal, a region is doped with majority carriers, which can be free electrons (n^+ in the figure) or holes, whereas the rest of the substrate is doped with minority carriers (p in the figure). Between different regions of the substrate the charges are distributed creating depletion zones and thus reaching a steady state. On top of the substrate and between the *Source* and the *Drain*, an insulator (SiO_2 typically in the case of MOSFETs) is placed, followed by a third conductive terminal, called the *Gate*. Applying a differential voltage between the *Gate* terminal and the *Body*, an electric field is induced which attracts positive or negative charges from the substrate towards the *Gate*. These charges are concentrated under the insulator, creating a charged region. If this region is wide enough to connect the doped drain and source regions, a highly conductive path is created. In lateral structures, the maximum forward current and maximum breakdown voltage (V_{BR}) ratings of the MOSFET are proportional to the channel dimensions, and most of the substrate is not exploited. This is the main difference and disadvantage when comparing with vertical structures, Fig. 2.4. In

these second ones, the *Drain* is placed on the opposite side of the *Source* and the *Gate*. The *Body* is formed by a minority carrier doped substrate (blue area p^+), together with a majority carrier doped layer called the drift region. This region is depicted with n^- due to poor doping of the substrate. In this configuration, current flows from bottom to top, taking advantage of the whole *Body*'s dimensions. The maximum current and maximum breakdown voltage ratings are proportional to the height and the doping of the drift region, and devices with higher breakdown voltage and lower ON-resistance can be created compared to lateral structures; this is the key for using them as power MOSFETs.

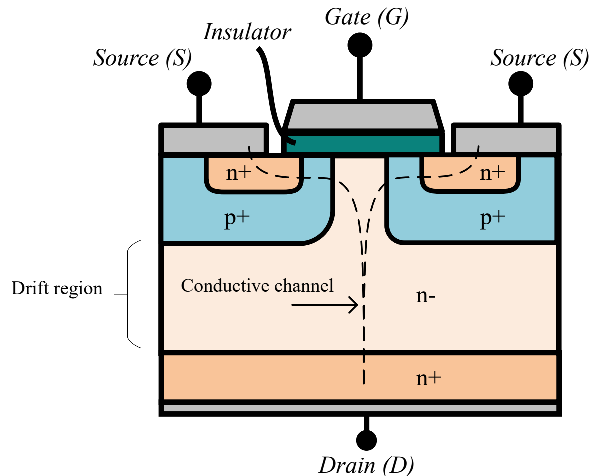


Figure 2.4: Vertical N-type FET structure (NMOS), showing the semiconductor regions, and the four terminals corresponding to the *Drain*, the *Gate*, the *Source*. Adapted from [24].

In MOSFETs the conduction is made only by one type of carrier (majority carrier), this is why they are considered unipolar devices. Depending on the doping type of drain and source regions and the rest of the substrate, the transistor is considered NMOS (with free electrons as carriers) or PMOS (with holes as carriers). In the case of an NMOS, when a positive voltage is applied in the *Gate* terminal concerning the *Source*, the induced electric field creates a negative charge channel (N-channel) under the insulator. The minimum voltage necessary to induce enough electric field and open the channel is called the threshold voltage (V_{TH}). On the other hand, in a PMOS, when a negative voltage is applied to the *Gate* concerning the *Source*, a negative electric field forms a channel for holes (P-type channel) under the insulator layer. The mobility of holes is lower than that of free electrons, as they are more attracted by the atomic force pulled by the nucleus. Therefore, the conductivity of PMOS is typically lower than that of NMOS, making it less preferred for power electronics.

The *Body* is considered as the fourth terminal. It is typically connected to the *Source*, to use it as a reference for the gate voltage. This configuration gives the MOSFET stability in different working conditions, but it is also responsible for creating intrinsic diode properties due to the PN junction created between the *Drain* and the *Source*, so the device becomes incapable of blocking reverse-biased voltage, behaving like a diode. In power electronic applications, it is common to switch between reverse conduction and blocking states, and in this situation, the intrinsic diode changes its state from conducting to blocking, involving the movement of the internal positive and negative charges from the depletion region. The transition is not instantaneous and becomes a source of power loss when it switches from forward-biased to reverse-biased. The charge needed to modify the state of the semiconductor is known as the reverse recovery charge (Q_{RR}).

Following the same structure as vertical MOSFETs but adding another layer of minority carrier doped substrate between the *Drain* and the *Body* (called injection layer and represented with a p^+), the Insulated Gate Bipolar Transistor (IGBT) is created (Fig. 2.5).

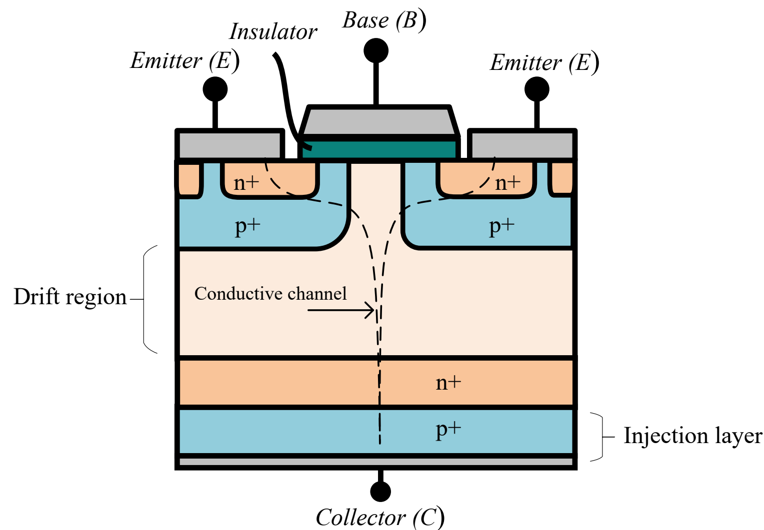


Figure 2.5: IGBTs internal structure, showing the semiconductor regions, and the three terminals corresponding to *Emmiter*, *Gate*, and *Collector*. Adapted from [24].

It combines the BJT's high conductivity characteristics with the *Gate* structure of FETs. IGBTs are bipolar devices, which means both majority and minority carriers are involved in the conduction process. With both types of charges involved, their switching performance becomes intrinsically slower than that of unipolar devices, [25].

IGBTs do not have reverse diodes due to the extra minority doped region, and they cannot conduct in both directions, only from *Collector* to *Emitter*. For this reason, a freewheeling diode is usually added between *Collector* and *Emitter* terminals to have the same bidirectional current conduction functionality as the MOSFET. Contrary to these last ones, their forward conduction involves minority carrier injection in the drift layer, known as conductivity modulation, increasing the conductivity of the material and decreasing significantly their forward voltage drop. This voltage is mainly dependent on the width of the drift region, and it is typically lower than MOSFETs over a certain current level, typically in the range of hundreds of amps. On the contrary, this working mode also implies a tail current related to the charge displacement when switching off, creating additional power losses.

Each type of transistor has its own suitable application range (see Fig. 2.6). BJTs are used where simplicity and robustness are desired, but their main drawback is the switching speed, typically lower than 10 kHz. IGBTs share these properties, with increased switching frequencies, and can withstand higher currents. At the same time, the conductivity modulation effect makes them suitable for voltages over 600 V with Silicon. In contrast, MOSFETs can achieve higher switching speeds; however, the relationship between substrate width and on-state resistance imposes a limitation on their breakdown voltage [4]. Their unipolar nature is advantageous for fast switching [25], but their maximum switching speed is ultimately constrained by parasitic capacitances, primarily introduced by the insulating layer between the *Gate* and the *Body*.

Most of the applications in power electronics are covered with Silicon BJTs, IGBTs, and MOSFETs. They have been constantly evolving to higher switching speeds, lower power losses, and better overall performance; however, the industry is reaching the theoretical limit

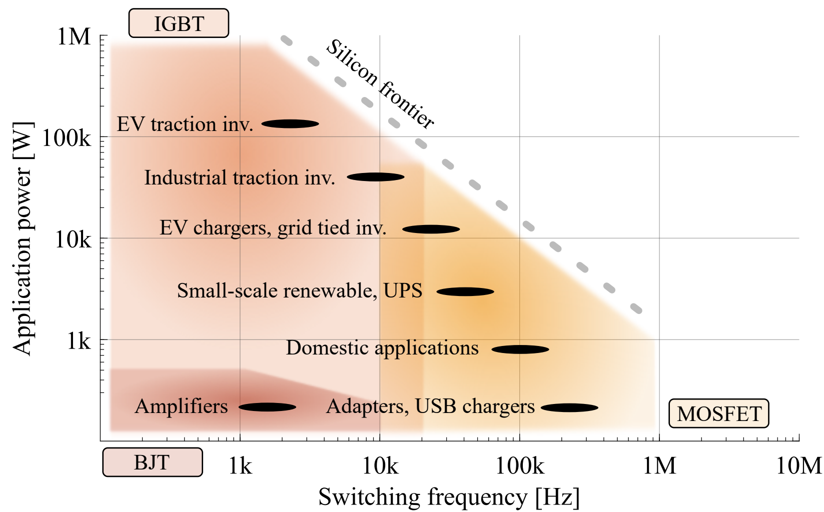


Figure 2.6: Approximated application range and scope of Silicon BJTs, IGBTs, and MOSFETs, adopted from [4], [26]

defined by Silicon, and WBG materials are emerging as an alternative to keep improving power electronics in general terms.

2.1.2. SiC diodes and MOSFETs

Since the early 2000s, Silicon Carbide has been used to create MOSFETs, IGBTs, diodes, or similar power devices as Silicon-based ones, [27]. The integration of this new wide-bandgap material in the power semiconductor industry started especially with Schottky Barrier Diode (SBD), which outperforms Silicon Fast Recovery Diode (FRD) as it provides better conduction and switching characteristics. PN and FRD diodes have a depletion region that needs to store charge for conduction. This charge requires a recombination process when moving from conduction to blocking state, producing reverse current flow and unwanted oscillations for a short period of time. The Schottky Barrier Diode (SBD) eliminates almost completely the need for a depletion region with a metal-semiconductor junction, notably reducing the reverse recovery effect and being more suitable for high-frequency and high-power applications. The reverse recovery charge in SBD is only related to discharging the junction capacitance, [28].

Silicon's narrow bandgap and electrical properties limit constructing SBDs over 200 V, requiring Fast Recovery Diodes to reach higher voltages. On the other hand, a wider bandgap of Silicon Carbide (SiC) allows the construction of SBDs for voltages up to 3.3 kV [29]. Above this voltage level, bipolar diodes, PN, can be created with SiC, reaching higher voltages than any Silicon diode on the current market.

Overall, Silicon Carbide diodes provide lower reverse recovery losses compared to a similar device made of Si. SiC is replacing Silicon in power diodes in the current market. For example, in a 1 kW AC/DC power converter reported in [29], with a rated input of 100 Vac and 60 Hz, and an output of 400 V_{dc} and 2.5 A, the reverse recovery current peak is decreased from 54 A to 14 A by only replacing Si FRDs with SiC SBDs. At the same time, with lower losses, the efficiency of the power conversion could be improved by more than 2%.

SiC MOSFETs

Up until recently, high density of defects in the epitaxial layers such as dislocations, micropipes, and polytype inclusions made only possible to create small surface SiC transistors, such as microwave Metal Semiconductor Field Effect Transistors (MESFET) [28]. The first Silicon Carbide MOSFETs came to the market in 2011 when Cree developed the first high-quality wafer [30]. With a ten times higher critical electric field than Silicon, SiC MOSFETs offer a higher breakdown voltage than Si or the same breakdown voltage but with a thinner drift region and lower drift-resistance R_{drift} (up to 500 times lower than typical Silicon MOSFET) as shown in Fig. 2.7. These MOSFETs can easily compete against the same voltage IGBTs, expecting no tail current, and a very low reverse recovery charge, [29].

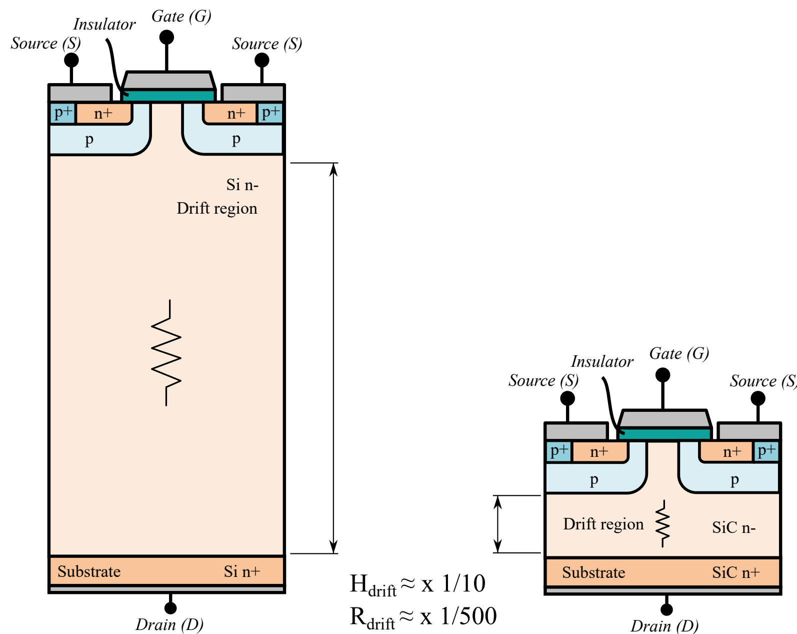


Figure 2.7: Size comparison of Si and SiC planar gate MOSFET for the same breakdown voltage [31]

A lower area of the device also translates to lower parasitic capacitance values and thus higher switching speeds. This makes it possible to replace Si IGBTs with SiC devices that can switch faster, reducing the overall size and cost of the passive components. The advantages of SiC over Si are not so clear below 600 V, as the difference in conduction and switching performance is counterbalanced in part by the increased cost of the new semiconductors [32].

Just like Si MOSFETs, SiC MOSFETs have an intrinsic diode due to their internal layer structure. They can conduct current through their body diode if reverse-biased, however, due to the wider bandgap of the material, the voltage drop is higher than with Si transistors. This voltage (v_{SD}) can reach values up to 4 V for a reverse current (I_S or I_{SD}) of 20 A in some cases [33], and carries an increase in reverse conduction power losses compared to Si, requiring an optimization of the reverse conduction. One way of optimizing the reverse conduction is typically to minimize the reverse conduction time. Although MOSFETs can work in the third quadrant using the same channel as in forward conduction, this also enables lowering the voltage drop for reverse conduction, applying a positive gate voltage ($v_{\text{GS}} > v_{\text{GS,th}} > 0V$).

Another option for lowering the reverse voltage drop is to use antiparallel SiC diodes with the MOSFET, creating a hybrid SiC solution (Si MOSFET + SiC SBD). It competes with the only MOSFET solution. In the majority of cases, the hybrid solution becomes more

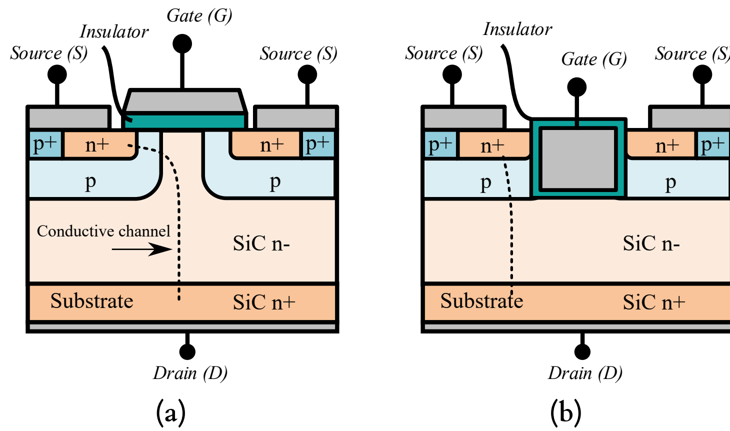


Figure 2.8: Simplified SiC-based MOSFET with planar gate structure (a) and trench structure (b).

expensive than the single MOSFET one, [33]. In contrast with SBD, this Q_{RR} charge of the (SiC) MOSFET increases with the temperature due to the minority carrier injection.

One of the main concerns related to SiC MOSFETs is reliability. Finding a reliable and stable gate oxide material has been challenging, and gate oxide can still be considered one of the main bottlenecks to improving this technology. Improving the channel mobility has also been a key challenge, which has forced manufacturers to move from planar MOSFET to Trench MOSFET technology, [34]. Due to the properties of the wide-bandgap material, the SiC-based MOSFETs require different gate voltages to switch on compared to Si MOSFETs. The typical required voltage levels are between 18 V to 20 V, slightly above the used 10 V to 15 V with Silicon MOSFETs.

2.1.3. GaN structures

The commercialization of Gallium Nitride power devices gained traction in the 2010s. Gallium Nitride crystals are made of hexagonal structures, which are responsible for giving the piezoelectric properties to the material. Matching different doped layers together can produce an electric field within the crystal, creating a high concentration of electrons in a small region. Due to the various properties of this wide-bandgap material compared to Si, as well as several material and technological limitations, GaN-based power switches differ structurally from Silicon-based MOSFETs and IGBTs.

GaN-based High Electron Mobility Transistor (HEMT) have dominated this market. A thin layer of Gallium Nitride (GaN) doped with aluminum atoms (AlGaN), working as the barrier, is put on top of another layer of pure GaN (see Fig. 2.9). The combination is responsible for displacing the atoms in the hexagonal structure and inducing constant stress, thus creating a Two Dimensional Electron Gas (2DEG) zone near the junction. Some transition layers are essential to match the GaN thin layer with the substrate. These layers' configuration and material are dependent mostly on the substrate used, which normally is Si, SiC, or sapphire.

At the two ends of the junction are located drain and source contacts, which provide and collect electrons when connected internally to the 2DEG. By nature, when the junction is first created, the *Drain* and *Source* terminals are electrically connected by the 2DEG. This is the working mode for a normally ON switch, also called a depletion-mode switch. The most used switches in the industry are enhancement mode switches. Therefore, some changes are required in the manufacturing process to work as a normally OFF transistor. Different

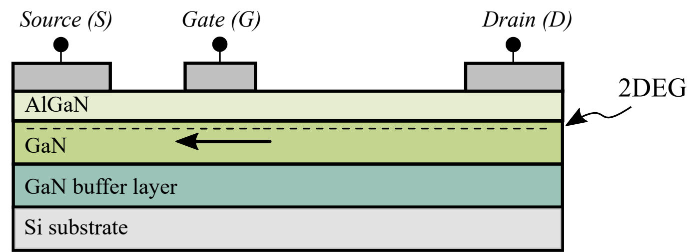


Figure 2.9: Cross section of typical depletion mode GaN HEMT, based on [8]

solutions have been analysed in literature [12] in order to obtain an enhancement-mode device. Currently, the most popular methods are the pGaN gate structure, which is created by adding a positively charged layer on top of the AlGaN layer; and the hybrid normally OFF structure, which is created by adding a Silicon low voltage MOSFET in series with a GaN depletion-mode transistor, which will be explained in the following subsections.

pGaN gate structure

This variant involves adding a doped GaN layer on top of the AlGaN barrier as shown in Fig. 2.10. This new positively charged region (pGaN) has a built-in positive voltage, which is higher than the voltage generated by the GaN heterostructure. Due to polarization occurring in the AlGaN layer, the electrons deplete from the 2DEG, converting the transistor into enhancement mode.

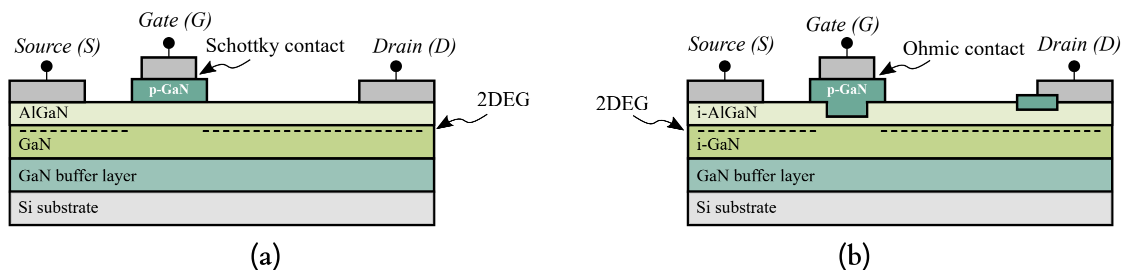


Figure 2.10: Simplified GaN-based Schottky Gate structure (a) and Ohmic Gate structure (b).

The benefits of using only the GaN HEMT and acting directly on its *Gate* without adding any extra components involve lower switching and conduction losses, and lower size and weight of the device. At the same time, it offers more opportunities to be integrated monolithically with the rest of the circuit. The gate threshold voltage is dependent on the piezoelectric properties of GaN substrate and the built-in voltage in the pGaN layer under the *Gate* terminal. Typically, the device starts conducting with 1.4 V [12], whereas typical Si MOSFETs have a minimum threshold voltage of around 3 V [35]. This can affect the immunity of the system and provoke unwanted switching if circuit parasitics are not properly addressed, [36]. Another challenging property of the GaN HEMTs, especially with Schottky Gate Transistor (SGT), is their gate sensitivity for overvoltages. SGT structures can have a maximum gate voltage as low as 7 V.

In the early stages of GaN power devices Panasonic and Infineon developed another type of enhancement mode HEMT, called the Gate Injection Transistor (GIT), which is worth mentioning. It is still being developed and manufactured, and its main difference with the typical enhancement mode HEMT is that instead of having a Schottky contact under the *Gate*,

an ohmic contact is used. This gives unique properties to this transistor such as overvoltage immunity in the gate, but the driver circuit becomes more complex as discussed later in this section. At the beginning positively doped AlGaN layer was used under the *Gate*, however, it can be also made with a doped GaN layer.

In HEMT devices, the differential voltage between gate and the power terminals is responsible for opening and closing the 2DEG conduction channel. When the device is forward biased, the gate-source differential is used for this, and if it is maintained over the threshold voltage, the channel can conduct current in either direction. However, considering a fully symmetrical device the working mode can be inverted, and applying a voltage between the *Gate* and the *Drain*, the device can also conduct current. The relation between the terminal voltages is rigged by the following equation:

$$v_{DS} = v_{DG} + v_{GS} \quad or \quad v_{GD} = v_{GS} - v_{DS} \tag{2.1}$$

This relation shows that the drain-gate voltage v_{DG}, or inverted, gate-drain voltage v_{GD}, is dependent on the applied gate voltage v_{GS} and the output voltage v_{DS}. The gate voltage with reference to the drain (v_{GD}), needs to cover the threshold level V_{TH} in order to form the 2DEG channel ($v_{GD} > V_{TH}$), and following the expression in (2.1), the following condition can be deducted:

$$v_{GS} - v_{DS} > V_{TH} \tag{2.2}$$

The equation (2.2) shows a condition that must be fulfilled with v_{GS} and v_{DS} to form the 2DEG when v_{DS} is negative. It is important to note that the condition $v_{GS} > V_{TH}$ is also required to form the channel. With these formulas, the working quadrants are embodied in Fig. 2.11.

Giving another point of view for the understanding, when negative voltage is applied between drain-source (v_{DS}) and 0 V between gate-source (v_{GS}), the *Gate* can be considered to be at the same potential as the *Source*, being v_{DS} equal to inverted v_{GD} (equation (2.1)). If v_{GD} is higher than V_{TH}, the 2DEG channel is closed, allowing reverse conduction. In most scenarios, v_{GS} will not be 0 V, and the switch OFF of the device is done with negative voltage to increase immunity against Electromagnetic Interference. In this case, the voltage relation must fulfill equation (2.2) to conduct current.

Working on quadrants 1 and 2, the device is switched ON by v_{GS}, and the voltage drop across the device (v_{drop}) will depend on $R_{DS(on)}$ and the current flowing through the channel I_{DS}. During the reverse conduction in quadrant 3, the voltage drop is the difference between the gate threshold voltage, and the applied voltage between gate-source, $v_{drop} = V_{TH} - v_{GS}$, [37]. Finally, in quadrant 4, the device is OFF.

The main difference between reverse and forward conduction is the voltage drop across the device when no gate bias is applied. Compared to its counterpart Si transistors, where the voltage drop is directly the forward voltage drop of the body diode (in case of MOSFETs), or freewheeling diode (in case of IGBTs), the GaN devices tend to have higher voltage drops, typically in the order of 1.5 V-2 V [37], and applying a negative voltage in $v_{GS(GaN)}$ increases, even more, this voltage drop. This increases the losses in reverse conduction over Silicon transistors. In [38] this problem is deeply analysed and a strategy for reducing the losses during the deadtimes is proposed by using adaptive times.

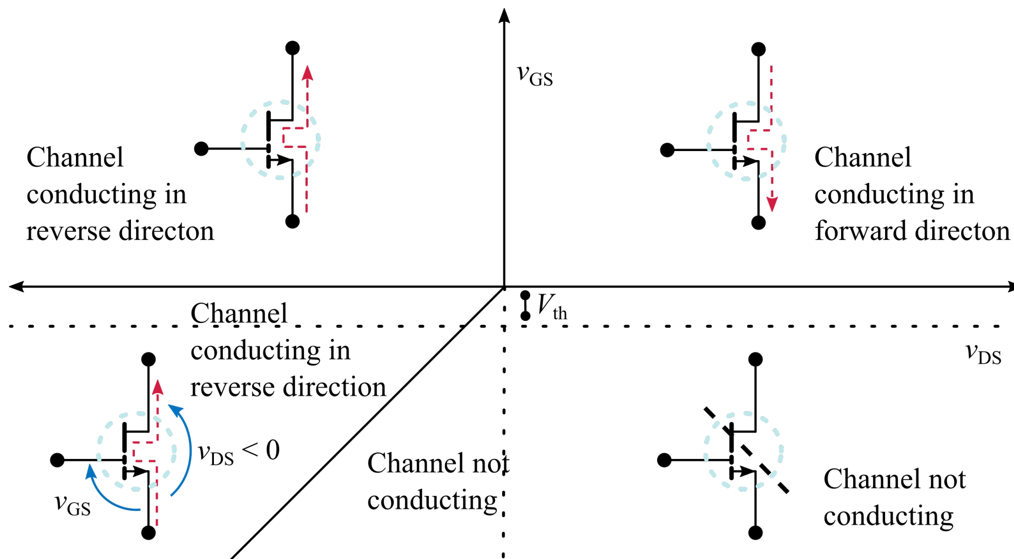


Figure 2.11: Enhancement mode GaN HEMT operation modes, depending on *Gate* to *Source* voltage v_{GS} and drain-source applied voltage v_{DS}. The dashed red line indicates the current direction. v_{DS} polarity is indicated with a blue arrow.

Hybrid Normally OFF (HNO) structure

This method for achieving an enhancement-mode device is the least invasive one for the original depletion-mode GaN transistor. It does not involve any modification in the GaN/Al-GaN layers. An enhancement-mode Silicon MOSFET is connected to a depletion-mode GaN HEMT, creating the enhancement-mode GaN FET. The Si MOSFET directly controls the GaN HEMT. These configurations offer the advantages of the MOSFET's *Gate* terminal (typically a low-voltage automotive standard MOSFET to have better performance) as robust *Gate* structure and typical *Gate* voltage (± 20 V), the combination of reverse recovery characteristics of both transistors and high voltage transient capability.

As discussed in [12] and [39], at lower voltages, the characteristics of the Silicon MOSFETs are more noticeable, overlapping the advantages of the GaN HEMT and losing the performance of the combination of both. With the increase of the breakdown voltage, the benefits of the GaN HEMT become stronger. Currently, two configurations are used to form the Hybrid Normally-off Structures (HNO) structure:

Cascode structure: For this configuration, the HEMT's *Gate* terminal is connected to the *Source* terminal of the Si MOSFET (see Fig. 2.12). In this structure, when a positive signal is applied to the MOSFET's *Gate* terminal, the *Source* of the GaN HEMT equals its *Gate* voltage through the connection of the MOSFET, enabling the 2DEG path. On the other hand, when the voltage is removed from the MOSFETs *Gate*, it enters the linear region. Its drain voltage starts increasing until reaching the threshold voltage of the GaN HEMT and depleting the 2DEG. At this point, the HEMT enters its linear region, until reaching saturation and blocking all the drain voltage,[40]. The Si MOSFET only supports part of the drain voltage, corresponding to the GaN HEMTs gate voltage. Therefore, low-voltage automotive standards MOSFETs are used.

Enable/direct drive structure: In the Enable/direct-drive configuration, an enhancement-mode Si MOSFET is also connected in series with the GaN depletion-mode HEMT, although in this case, the *Gate* terminal of the HEMT is not connected to the *Source* of the MOSFET.

It is operated externally from the driver circuit, at the same time as the *Gate* of the Silicon transistor, granting a more direct switching control over the GaN HEMT. The main drawback of this structure over the previous one is the need for an extra input *Gate* signal corresponding to the GaN *Gate*.

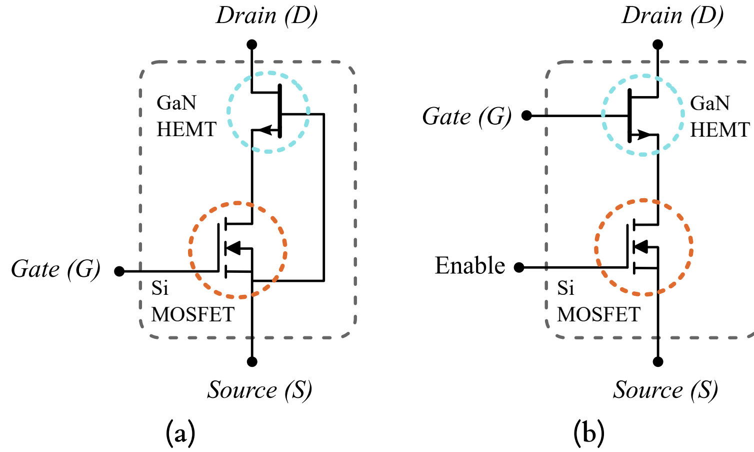


Figure 2.12: (a) Cascode structure GaN FET, showing the terminals, and the internal connections, and (b) Enable/direct-drive GaN FET, showing the terminals, and the internal connections.

In the case of HNO FETs, the GaN device is a depletion mode transistor, and it conducts when its gate-source voltage, $v_{GS(GaN)}$, is negative. The current can flow through the MOSFET's diode, creating a forward-bias voltage drop, which becomes $v_{GS(GaN)}$. In this case, the voltage drop of the whole circuit will be similar to the HEMT case, but in the case of cascode configuration, with a fixed applied voltage in $v_{GS(GaN)}$ that will be equivalent to the MOSFET's body diodes forward voltage.

Comparing both concepts of enhancement-mode GaN devices (HNO and pGaN), it is clear that the selection is dependent upon the application where it is being used. The frontier is quite diffuse, but it can be said that below 200 - 300 V applications [12, 39, 41], where the *Gate* immunity is not critical, the *pGaN Gate* HEMT or enhancement mode GaN HEMT have more benefits than HNO GaN FETs, as the fast switching and low conduction resistance of the GaN is fully exploited. The dilemma comes in applications above these levels of voltage and power, where voltage and current transients can induce unwanted noise in the *Gate* terminal, and the immunity becomes critical. As mentioned before, the effect of the series MOSFET loses weight with the increase of breakdown voltage. In general, at higher voltage levels, the HNO is preferred. In the current market, the mentioned configurations can be found available, and the frontier between HNO and pGaN seems to be user-dependent. For instance, Efficient Power Conversion (EPC) manufactures pGaN discrete transistors up to 200 V in die form, whereas GaN Systems has available 650 V pGaN devices with increased *Gate* immunity. On the other hand, Transphorm, Nexperia, or Infineon focus on 600-650 V cascode FETs.

2.2. Market Overview for GaN Semiconductors

A market analysis has been conducted to identify the available GaN products with their main distinctions compared to Si-based products. Key manufacturers of GaN transistors are listed and described in this section, including their strategic portfolios, and their distinctions. GaN, SiC, and Si discrete devices are compared based on different FOMs.

2.2.1. Key GaN manufacturers

The GaN power semiconductor industry is growing at an unprecedented speed. More companies are getting involved in the industry, and new GaN products are expected every year. Here, an overview for 2025 is presented, listing the key manufacturers of GaN technology.

Infineon Technologies

This well-known manufacturer offers GaN HEMTs from 40 V to 650 - 700 V breakdown voltages. The key difference from its competitors lies in the type of HEMT used for the high-voltage-class devices, a GaN GIT. This structure allows the channel to be switched on and off using gate current, providing greater robustness and immunity compared to the SGT technology. These devices are branded as CoolGaN™ and are available in TO-Leadless Package (TOLL), TO-Leaded Top-Side cooling (TOLT), TO-Leaded with Gullwing (TOLG), and Dual Flat No-lead (DFN) packages. Most of these packages include a cooling pad to facilitate power dissipation.

GaN Systems - Infineon Technologies

Offering a wide variety of GaN HEMTs, primarily in DFN packages, this manufacturer focuses on 100 V and 650 V devices. GaN Systems was acquired by Infineon Technologies in 2023. Their package is designed with a considerable thermal pad to enhance power dissipation. Some products are available in GaNpx® packages, which help minimize parasitic effects. Most models are offered with either top or bottom cooling pads, allowing customers to choose the most appropriate format for their design. Following the acquisition by Infineon Technologies, the range of available packages has expanded.

Efficient Power Conversion

This company is focused on low-voltage (< 200 V) GaN HEMTs, offering the widest variety of GaN devices in the range of 10 to 200 V. The power devices are offered in Chip-Scale Packages (CSP), with Ball Grid Array (BGA) or Land Grid Array (LGA) for soldering. Thanks to the simplified format, they can achieve the lowest parasitic inductance and capacitance values in the market, and at the same time, it allows them to manufacture the product at a competitive cost. The last development of this company is a 350 V power device, [42].

ROHM

This company began mass-producing its GaN technology in 2022. Their technology is based on an SGT structure, but they distinguish themselves from their competitors by offering a gate withstand voltage of up to 8 V, enhancing the robustness of this technology. Their GaN portfolio includes 150 V, and 650 V discrete devices, as well as discrete integrated devices with

their drivers in the same Integrated Circuit (IC). Their products are mostly offered in DFN packages.

STMicroelectronics

STM is another company developing GaN HEMTs, featuring a self-designed PowerFLAT package, very similar to Infineon's DFN packages. They already offer 650 V GaN power transistors based on SGT structure, but their primary focus is on ICs that integrate discrete HEMTs with the drivers, targeting half-bridge applications. The IC family is called MasterGaN.

Innoscience

Founded in 2015, this manufacturing company is a leading provider of GaN-on-Si wafers. They offer low-voltage GaN HEMTs with SGT structure for breakdown voltages of 30 V, 40 V, 60 V, 100 V, and 150 V, as well as high-voltage 650 V up to 900 V devices. Their power transistors are available in CSP, DFN or even Transistor Outline (TO) packages. They provide GaN ICs with integrated drivers too.

Nexperia

Nexperia offers a wide range of GaN power switches. They differentiate themselves from competitors by providing e-mode GaN HEMTs based on SGT structure, as well as cascode structures for 650 V applications. Their SGT GaN FETs are available in CSP format for 100 V, 150 V, and 650 V. For high voltage applications, they offer devices in DFN format, while their cascode devices feature a proprietary packaging structure, Copper Clip Package (CCPAK), which comes in leaded packages similar to TOLT packages. They offer both top and bottom-cooled device options.

Cambridge GaN devices

CamGaN is a promising company focused on GaN HEMTs, but with the distinction of a different type of *Gate* terminal. Their 650 V GaN H1 series features a well-developed *Gate* terminal with similar characteristics as Silicon MOSFETs, making the device easier to use and more robust to gate fluctuations. They can be used with typical Silicon drivers, and they provide a Kelvin source and a current sensing terminal. Their devices are offered in DFN package, similar to the one used by Innoscience or Infineon.

Transphorm - Renesas

The company, now part of Renesas, was founded in 2007 and specialized in GaN cascode structure FETs. Offering a wide variety of 650 V power devices, their portfolio extends up to 900 V, and 1200 V class cascode devices. In 2024, Transphorm was acquired by Renesas. Transphorm FETs are available in DFN and TO packages (TO-220, TO-247, and TO-263), with the cooling pad located on the bottom side for the DFN packages.

Texas Instruments

Their catalogue includes GaN power devices with integrated drivers within the same package. The power switch is an HNO FET featuring a direct-drive structure. The integrated driver enables the control of both the GaN depletion-mode HEMT and the accompanying Si

MOSFET. The company offers solutions for both 600–650 V and sub-200 V applications, incorporating a range of protection features such as over-current protection, over-temperature protection, and temperature monitoring. Devices are available either as individual FETs with drivers or as complete half-bridge configurations, all in Quad Flat No-lead (QFN) packages. Cooling options include both top and bottom-cooled variants, with the top-cooled version also available in an automotive-qualified format.

VisIC Technologies

Based on an innovative fabrication process known as D^3GaN, VisIC Technologies is dedicated to HNO structures based on direct drive depletion mode configuration. They specialize in automotive applications with high voltage (650 V) and high current (100 A, 200 A) devices. Their power switch solutions implement safety functions to ensure safe operation during system start-up and shutdown modes.

Navitas Semiconductor

This company is mostly dedicated to GaN ICs. They offer a GaN FET integrated with the drive and logic circuitry in the same die, for the gate regulation and *dv/dt* control. Unlike Texas Instruments' ICs, Navitas does not include protections in its products. The FastGaN ICs are packaged in QFN, and some of them do not have a cooling pad, making them ideal for simple and low-stress applications.

Power Integrations

This manufacturer stands out by offering ICs specifically designed for flyback converters, known as the InnoSwitch family. Power Integrations initially offered these products using Silicon-based technology but has recently incorporated GaN to enhance performance. The ICs integrate the primary-side switch and controller with the secondary-side controller, along with sensing elements and a safety-rated feedback mechanism. The secondary controller is designed to drive an external Si MOSFET. These ICs support output power levels up to 250 W, with voltage ratings up to 1700 V. In addition to the flyback ICs, Power Integrations also offers a notable solution for bus capacitor reduction through an active power buffer known as the MiniE-CAP.

Summarizing Key GaN manufacturers

Table 2.1 presents an overview of the leading GaN manufacturers and their product portfolios. The power devices are categorized by package type, breakdown voltage, and device type.

Looking at the package styles, it is clear that the DFN/QFN is becoming the preferred one for GaN-based transistors at different breakdown voltages. This package type offers much better switching characteristics than the standard TO packages used with Silicon, due to shorter interconnections between the chips and the terminals. Low parasitics are ideal for GaN technology, as their fast dynamics present a challenge when parasitics are involved. The improvement in switching performance comes with the cost of worse thermal performance, as they typically lack a top heat dissipation pad. Power switches from 100 V up to 900 V can be found in this package. QFN packages are preferred for GaN ICs. Low-voltage (< 200 V) devices are mostly provided in CSP format, offering the best switching performance but making it difficult to dissipate the generated heat. Some manufacturers are working with TOLL/TOLG and TOLT packages, which offer a good balance between switching and thermal performance,

Table 2.1: Key GaN manufacturers and their portfolios by July, 2025.

Packaging	CSP	DFN/QFN	TOLL/TOLG	TOLT (or sim.)	D2PAK	TO-220/TO-247
Thermal performance	✗✗	✗	✓	✓✓	✓	✓✓✓
Switching performance	✓✓✓	✓✓	✓	✓	✗	✗✗
Infineon Technologies	40-200 V *	100-650 V */***	650-700 V *	650-700 V *		
Gan Systems (Infineon)		100-700 V *				
Efficient Power Conversion	10-200 V */***					
ROHM		150-650 V */***				
STMicroelectronics		650 V */***				
Innoscience	30-150 V */***	650-900 V */***				650-900 V */***
Nexperia	10-150 V *	650 V *		650 V */**		
CamGaN		650 V *				
Transphorm (Renesas)		650 V **	650 V **		650 V **	650-1200 V **
Texas Instruments	100 V ***	80-650 V ***	650 V ***			
ViSiC Technologies		650 V **				
Navitas Semiconductor		650-700 V ***	650-700 V ***	650-700 V ***		
Power Integrations		650-1700 V ***				

(*) Discrete e-mode SGT or GIT HEMT, (**) Discrete cascode or direct-drive FET, (***) Discrete GaN (d-mode, e-mode, cascode or direct-drive) integrated with driver and/or protections.

and target higher-power applications. And lastly, a few manufacturers work with Double Decawatt Package (D2PAK) and TO packages with GaN. These manufacturers are especially focused on cascode devices.

2.2.2. Discrete power switches comparison

It is not easy to compare different power transistor technologies without considering any application. However, using different FOMs, the performance of discrete devices can be characterized for a straightforward comparison of the technologies. Different FOMs have been used in literature to address different applications. For a general comparison of Switch Mode Power Supplies (SMPS) applications, the input FOM $R_{DS(on)}Q_G$ is considered a good performance indicator. The multiplication of these two attributes describes the properness of any transistor in an application where both switching losses and conduction losses are important. Several discrete devices are compared in Fig. 2.13 based on the Input FOM. The lower the FOM value, the better the performance would be.

Looking at the results using the input FOM, the difference between GaN, SiC, and Si is notable. The lowest values are obtained with GaN HEMTs for the entire voltage spectrum. There is no GaN device over 900 V breakdown voltages yet, so over this voltage, SiC becomes dominant. GaN devices describe the minimum input FOM frontier for the available technologies. However, it must be noted that the Silicon FOM value is higher than the GaN FOM, with lower breakdown voltages.

Another critical FOM is defined by $R_{DS(on)}Q_{OSS}$. This indicator is used for applications where the output charge (Q_{OSS}) has a strong implication in the switching performance of the transistor. This is the case for Zero-Voltage-Switching (ZVS) converters, where the output

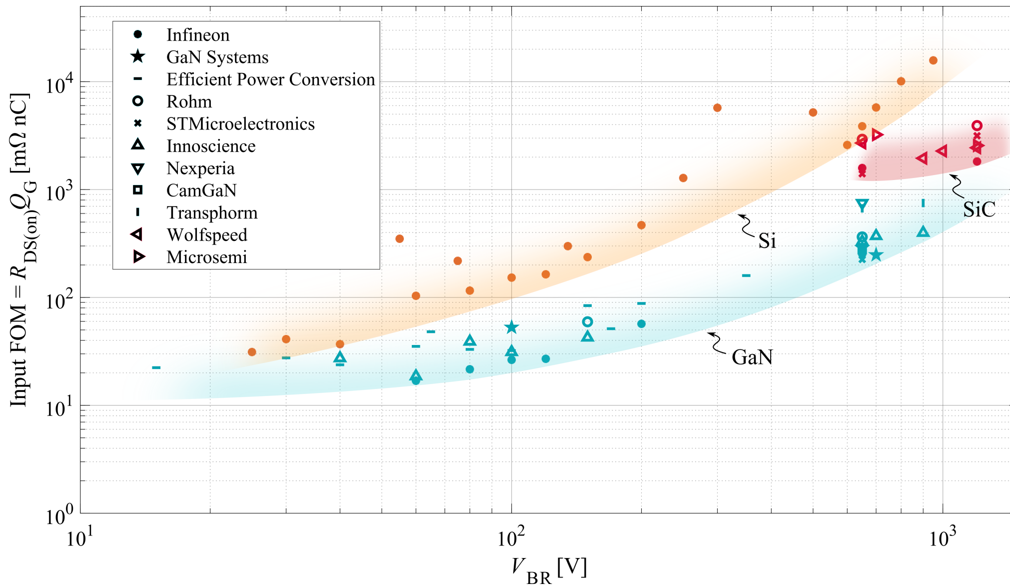


Figure 2.13: Input FOM $R_{DS(on)}Q_G$ for GaN, SiC, and Si-based discrete devices, for breakdown voltages starting at 30 V up to 1.2 kV.

and input dynamics of the transistor are decoupled. Under soft-switching conditions, the switching losses are mostly related to the Q_{OSS}. The results obtained using the soft-switching FOM are plotted in 2.14.

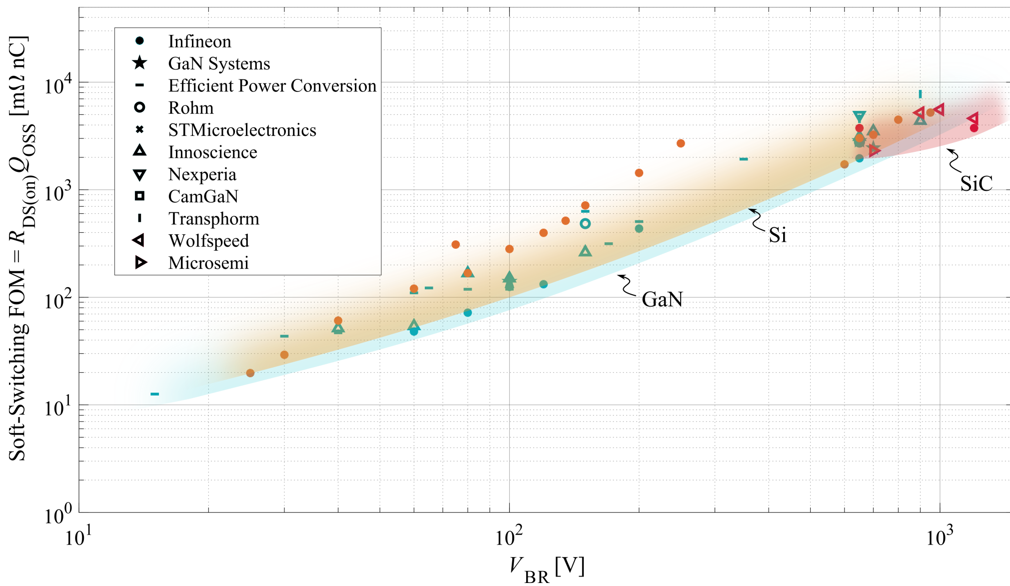


Figure 2.14: Soft-switching FOM $R_{DS(on)}Q_{OSS}$ for GaN, SiC, and Si-based discrete devices, for breakdown voltages starting at 30 V up to 1.2 kV.

The soft-switching FOM shows an interesting result when comparing different technologies. GaN, SiC, and Si devices describe limits that are very close for the entire breakdown voltage spectrum. Even with the newest technology of GaN, the $R_{DS(on)}Q_{OSS}$ product has not improved much. Even if GaN and SiC can offer more compact devices, the output charge is affected by the wider bandgap of these materials, and the achieved FOM value is similar to the Silicon FOM. It can be said that Si, GaN, and SiC could perform similarly under soft-switching

conditions.

Lastly, a third FOM is calculated for hard-switching applications, for which the product of $R_{DS(on)}$ and Q_{GD} is used. Under hard-switching conditions, the switching speed is conditioned by the Miller plateau, and the charge (Q_{GD}) involved during this period (see Fig. 1.2). This charge is considered a good indicator of hard-switching losses. The results for hard-switching FOM are shown in 2.15.

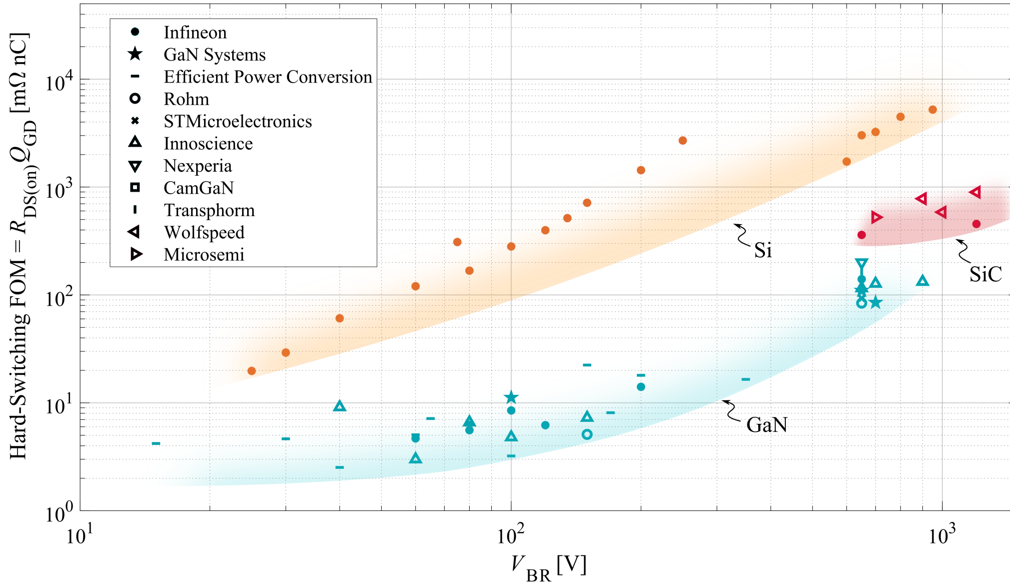


Figure 2.15: Hard-switching FOM $R_{DS(on)}Q_{GD}$ for GaN, SiC, and Si-based discrete devices, for breakdown voltages starting at 30 V up to 1.2 kV.

Similar to the input FOM, the hard-switching FOM shows an improvement in the performance of wide-bandgap materials compared to Silicon under hard-switching conditions. Their lower Miller charge for the same conduction resistance improves the switching speed, consequently reducing the switching losses. By examining various FOMs, the differences between technologies become evident. The results demonstrate that GaN is a superior technology compared to silicon, particularly in switched-mode power supplies (SMPS) and hard-switching converters. However, the technological advantage is less pronounced in soft-switching applications. It is important to emphasise that these FOM represent general trends and should not be used to predict the performance of a specific device under particular operating conditions.

2.3. Conclusions

The transition from traditional Silicon-based BJTs, MOSFETs, and IGBTs to WBG technologies such as SiC and GaN represents a major advancement in power semiconductor performance. While Silicon devices remain dominant in low- to mid-voltage applications due to their maturity, reliability, and cost-effectiveness, WBG materials offer significant benefits across a broad range of operating conditions. SiC diodes and MOSFETs provide lower conduction and switching losses, improved thermal handling, and extended voltage capabilities, making them well-suited for high-voltage applications above 600 V. GaN-based devices, particularly enhancement-mode HEMTs and HNO structures, demonstrate excellent performance in high-frequency and compact designs. However, challenges such as gate voltage sensitivity and increased reverse conduction losses must be carefully considered. The choice between pure HEMT and cascode configurations is highly application-dependent, requiring a balance between switching performance, gate immunity, and driver compatibility. Understanding the limitations of each device technology is essential to fully exploit their advantages in real-world applications.

As a newer and more diverse technology, the GaN semiconductor market exhibits a broader range of device architectures and packaging strategies compared to SiC. The landscape of key GaN manufacturers reflects this diversity, with each company offering unique solutions tailored to specific use cases. These include innovative packaging to minimize parasitics and enhance thermal performance, integration of gate drivers and protections, and various structural approaches such as GITs, pGaN gates, and cascode configurations. These differences are crucial when selecting components for particular applications, especially as GaN competes directly with both Si and SiC across multiple voltage classes. To assess the practical implications of these technologies, several FOMs are used to benchmark device performance. Metrics such as $R_{DS(on)}Q_G$, $R_{DS(on)}Q_{OSS}$, and $R_{DS(on)}Q_{GD}$, provide valuable insights into the suitability of different technologies under varying switching conditions. The input FOM ($R_{DS(on)}Q_G$) commonly used for evaluating SMPS performance, and the hard-switching FOM ($R_{DS(on)}Q_{GD}$) clearly show that current GaN devices can outperform Si and SiC devices across nearly all voltage ranges in terms of speed and efficiency. In contrast, the soft-switching FOM ($R_{DS(on)}Q_{OSS}$) reveals less variation between technologies, suggesting that under soft-switching conditions, Si, SiC, and GaN can exhibit comparable performance. However, these metrics do not account for other important factors such as dead-time conduction behaviour or reverse recovery characteristics, which can significantly influence overall device performance. As a result, drawing definitive conclusions solely from these FOMs can be challenging. These observations underscore the importance of conducting application-specific analyses when selecting semiconductor technologies for power conversion systems.

Chapter 3

GAN TECHNOLOGY AND CHALLENGES

Gallium Nitride (GaN) technology is driving significant progress in the semiconductor industry. Its unique properties enable higher switching frequencies and reduce power losses to levels that were previously unattainable in power electronic applications such as Switch Mode Power Supplies (SMPS). However, GaN is not yet as mature as conventional Silicon-based technologies. As mentioned earlier, manufacturers are following different strategies to commercialize GaN, including variations in transistor structures and the development of fully integrated power stages. New transistor structures have emerged due to the unique properties of GaN. The most promising structures are the Gate Injection Transistor (GIT) and the Schottky Gate Transistor (SGT). The GIT uses a titanium gate metal and p-doped GaN to control the conductivity of the Two Dimensional Electron Gas (2DEG) channel, forming an ohmic contact in series with a GaN diode between gate and source. Meanwhile, the SGT uses a Schottky contact with the p-doped GaN to control the 2DEG channel, [43]-[44]. While the SGT requires less gate drive current, and hence power, than the GIT, the ohmic contact of the GIT allows for broader control of the channel while offering a more robust gate that is immune to overvoltages to a practical extent. Despite undergoing research work, several critical characteristics of this emerging technology remain under investigation and continue to evolve with each new generation. Some of these factors may pose challenges for specific applications and must be well understood.

Among them, three stand out due to their importance in the SMPS field: the saturation current, which limits the maximum current flow through the device channel; the dynamic $R_{DS(on)}$, which tends to be more critical in GaN compared to mature Silicon technologies; and the short-circuit robustness, which is generally more limited in GaN devices. This chapter discusses these three aspects in detail to provide essential insight before adopting GaN-based solutions.

3.1. Dynamic Saturation Current in GaN HEMTs

The maximum current at which the semiconductor channel saturates, known as the saturation current, plays a fundamental role in power electronic applications. In some cases, the saturation current can affect the short-circuit capability of the device [45–47]. In other cases, it becomes a limitation due to the high current requirements of the application, especially under transient working conditions, such as during startup or AC line cycle dropout. Reports have claimed that with the latest GaN technologies, the saturation current is improved, [48]; however, these limits are still lower with GaN technologies than with Silicon technologies for the same $R_{DS(on)}$ value. In fact, the saturation current can present a bottleneck for using the same $R_{DS(on)}$ GaN devices where Silicon devices were used before, requiring reconsideration for bigger chips or parallel configurations, [49].

Furthermore, unlike Silicon Metal Oxide Semiconductor Field Effect Transistor (MOSFET)s, GaN-based switches exhibit a pronounced dynamic behaviour in their saturation current characteristics. The maximum current that the device can conduct is not fixed but varies depending on the switching conditions, whether the device is operating in Hard-Switching (HS), Zero-Current-Switching (ZCS), or Zero-Voltage-Switching (ZVS) regimes. These variations can be partially observed in the datasheets through the Typical Output Characteristics (TOC) and the Safe Operating Area (SOA) plots, as shown in Fig. 3.1. The inconsistency of the maximum current level observed in both graphs lies in the methods employed for extracting these values. While the TOC is extracted using continuous condition tests, the SOA is extracted considering switching transitions. Despite being a critical parameter, the dynamic behaviour of the saturation current is rarely investigated in the current literature.

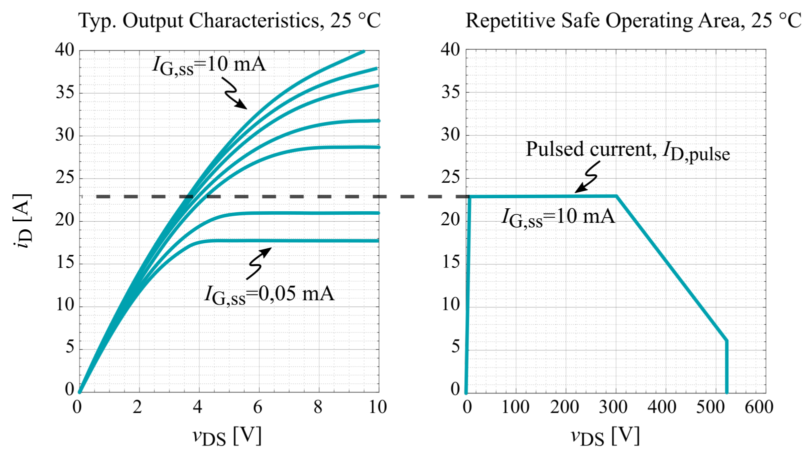


Figure 3.1: Typical output characteristics curve and the repetitive safe operating area side by side, for IGLD65R140D2 GaN GIT from Infineon, at 25 °C.

In this context, the saturation current of GaN semiconductors has been studied to better comprehend its behaviour and observe the limits of GaN technology. For this, Infineon's GIT technology is used. The release of the second generation of GIT technology (marketed as CoolGaN™ 650V G5) is expected to bring significant improvements compared to the first generation. Furthermore, a comparative study between first- and second-generation devices is presented, highlighting promising advancements in the latest generation related to saturation current. The results are published in [50], with contributions to [51].

3.1.1. Experimental test bench and method

A half-bridge configuration has been employed to measure the saturation current of GaN High Electron Mobility Transistor (HEMT) devices, Fig. 3.2. Using a Double Pulse Test (DPT), the drain current through the Device Under Test (DUT) can be raised until the channel reaches saturation. Looking into Fig. 3.3, the DUT is the low side switch (S_{ls}), and the high side switch (S_{hs}) is used in synchronous mode. The device is considered saturated when the drain-source voltage (v_{DS}) reaches a predefined threshold during the conduction state. In this study, this threshold has been set at 50 V (v_{sat}). For the test, a 100 μH inductor is used, and the bus voltage is set to 400 V, which defines the slope of the drain current of the DUT.

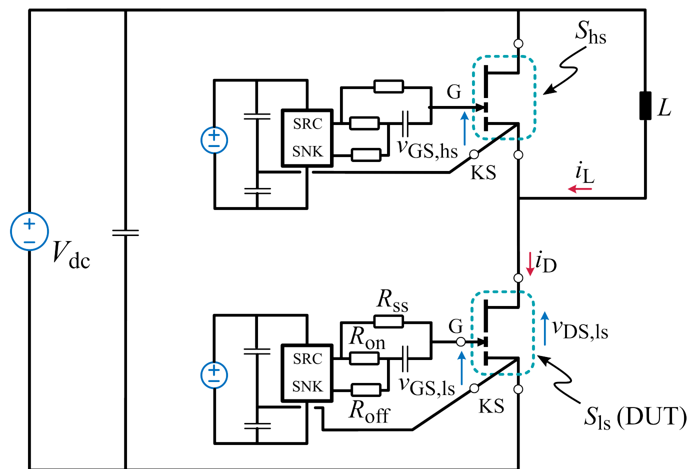


Figure 3.2: Half-bridge schematic used for the $i_{D,sat}$ testing of GaN GITs. The bus voltage is configured at 400 V, and the tests are performed using 100 μH inductor, [50, 51].

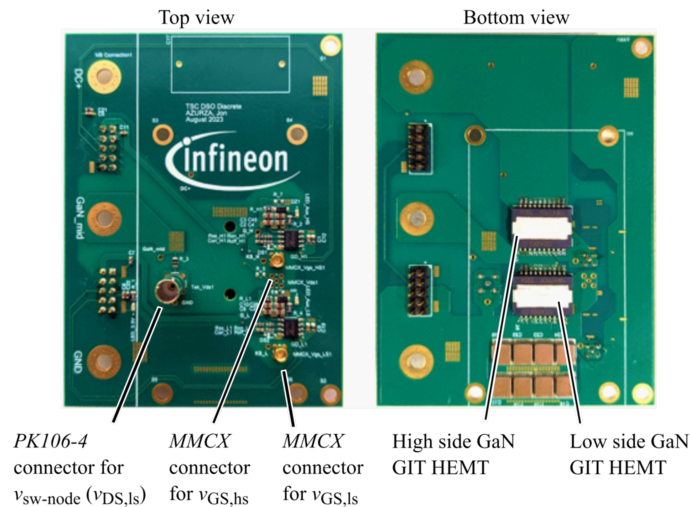


Figure 3.3: Top and bottom view of the half-bridge used for $i_{D,sat}$ characterization of GaN HEMTs. Switches are top-side cooled DSO packages. Image courtesy of Infineon Technologies Austria AG, [50, 51].

The duration of the first and the second pulse, t_{p1} and t_{p2} respectively in Fig. 3.4, can be configured to change the turn-on current, $i_{turn\text{-}on}$, and to study the influence of Hard Switching and Zero Current Switching on the saturation current. To evaluate the saturation current under ZCS conditions ($i_{turn\text{-}on} = 0$ A) both t_{off} and t_{p2} are set to zero and a single pulse

is applied (t_{p1}) to the Device Under Test (DUT) until it reaches saturation. To evaluate the saturation current under HS, a t_{off} is set between the two pulses, and t_{p1} and t_{p2} are gradually increased. Various turn-on currents are evaluated. The saturation state is never extended over 200 ns, as it has been observed that prolonged exposure to saturation can cause the DUT to fail. Under the tested conditions, no device failures were observed for saturation times below 200 ns. The current flowing through the inductor is measured using a TCP 0150 current probe, which corresponds to the drain current of the DUT, except during the freewheeling phase (during t_{off}). The drain-source voltage is measured with a PHV 1000 probe, and the gate-source voltage using a Tektronix TPP1000 probe. Fig. 3.5 shows the typical experimental waveforms obtained in the saturation test, with a first-generation 140 mΩ_{typ} device. In Fig. 3.5(a), a single pulse corresponding to the ZCS test is shown, where the saturation current reaches 40 A. In Fig. 3.5(b), a DPT for the same device is presented under hard-switching conditions with a current of 23 A (the recommended pulse current from the datasheet, see Fig. 3.1), where the saturation current reaches 35 A. Default conditions are set for switching the device, shown in Tab. 3.1.

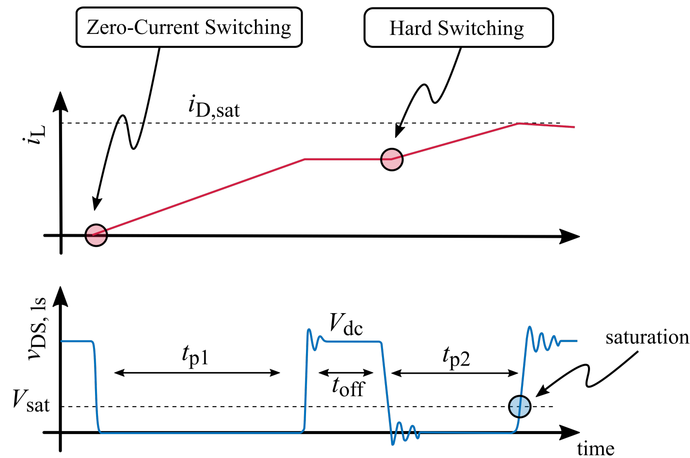


Figure 3.4: Ideal voltage and current waveforms of the half-bridge circuit when performing a hard-switching double-pulse test, [50, 51].

3.1.2. Experimental evaluation of $i_{D,sat}$

Using the mentioned test bench and method, various experiments are carried out to analyse the influence of some parameters on the $i_{D,sat}$. Default values for the test are listed in Tab. 3.1.

Table 3.1: Default values of main parameters in the circuit for $i_{D,sat}$ testing.

	IGLD60R140D1/D2	IGOT60R035D1/D2
Positive gate voltage, v_p	7.5V	7.5V
Negative gate voltage, v_n	3 V	3V
Turn-on resistance, R_{on}	22 Ω	10 Ω
Turn-off resistance, R_{off}	2.7 Ω	1 Ω
Steady-state gate resistance, R_{ss}	470 Ω	120 Ω
gate capacitance, C_g	10 nF	10 nF

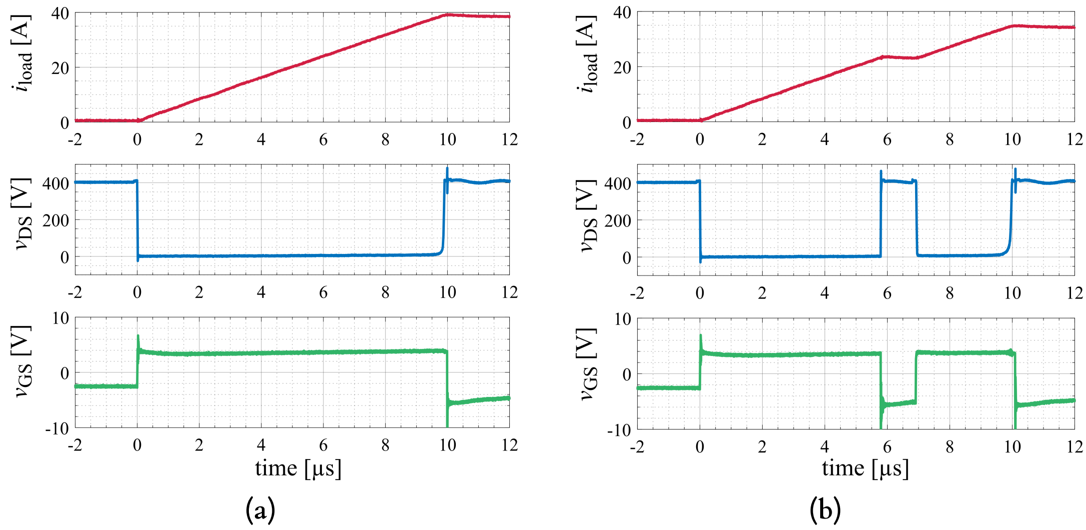


Figure 3.5: Experimental voltage and current waveforms of the half-bridge circuit in ZCS test (a) and HS test (b). The driving parameters are set according to Tab. 3.1 to define a steady-state gate current of 8 mA for the 140 mΩ_{typ} device, [50, 51].

Influence of turn-on current on $i_{D,sat}$

This process provides a complete image of the $i_{D,sat}$ evolution related to the $i_{turn\text{-}on}$. The results for the 35 mΩ_{typ} and 140 mΩ_{typ} devices are depicted in Fig. 3.6. The test is performed at two case temperatures, 25 °C and 125 °C, while the maximum recommended pulse current values in the datasheet are indicated by $I_{D,pulse}$. As listed in Tab. 3.1, the continuous gate current is configured according to manufacturer recommendations, 8 mA for the 140 mΩ_{typ} devices, and 35 mA for the 35 mΩ_{typ} devices (both first and second generation).

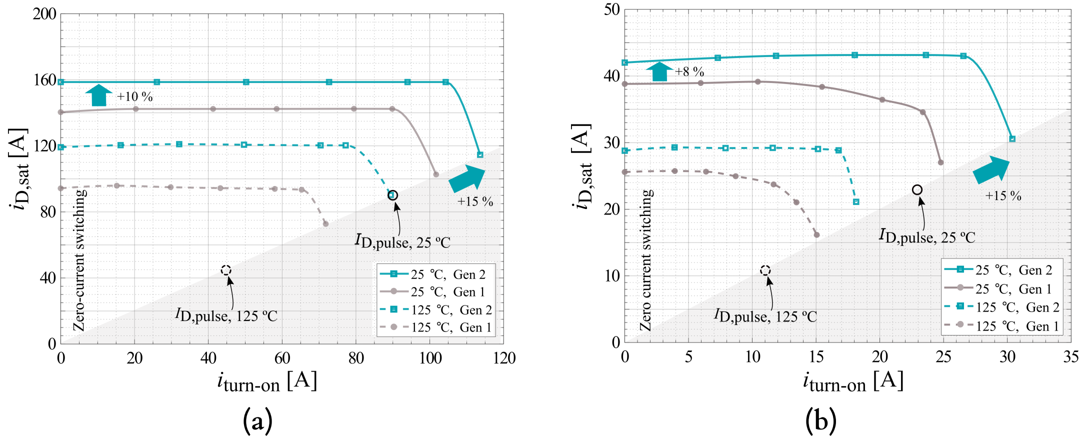


Figure 3.6: (a) $i_{D,sat}$ evaluation for 35 mΩ_{typ} 650 V GaN GIT, IGOT60R035D1/D2, and (b) 140 mΩ_{typ} 650 V GaN GIT, IGLD60R140D1/D2, using 35 mA and 8 mA steady-state gate current respectively. The results are obtained for two different case temperatures, 25 °C and 125 °C, [52], [50, 51].

The results demonstrate how the saturation current is affected by the turn-on current. The dynamic behaviour can be observed in the results: hard-switching close to the recommended $i_{D,pulse}$ current limits the $i_{D,sat}$ down to its minimum value, while zero-current-switching transition describes a saturation current limit that can be above 50 % of the $i_{D,pulse}$ given in the datasheet. Between these two extreme cases, the evolution of $i_{D,sat}$ is merely affected by

the hard-switching turn-on current, especially when using second-generation devices. The flat trend in the saturation current before the sharp decrease near the recommended $i_{D,pulse}$ suggests that channel saturation occurs due to two different causes. The first is not fully related to switching losses, while the second is primarily influenced by them. This hypothesis is discussed in more detail in the following. The experimental results also demonstrate that the devices can be used in ZCS and HS applications (HS up to 80-90 % of $i_{D,pulse}$) with a great $i_{D,sat}$ margin compared to the recommended value. Comparing first and second-generation devices, an $i_{D,sat}$ increase of 8 to 15 % for all the ZCS-HS range can be observed with the latest generation.

Influence of turn-on resistance and turn-off period on $i_{D,sat}$

The first experimental results reveal the influence of the turn-on current on the saturation current. To investigate the hypothesis that switching losses (proportional to the turn-on current) could be the primary contributor to channel saturation near the $i_{D,pulse}$, further study is required to examine other parameters that may affect switching losses. Therefore, the turn-on resistor R_{on} is modified, and the saturation current is measured for the second-generation 140 mΩ_{typ} 650 V GaN GIT, shown in Fig. 3.7, (a).

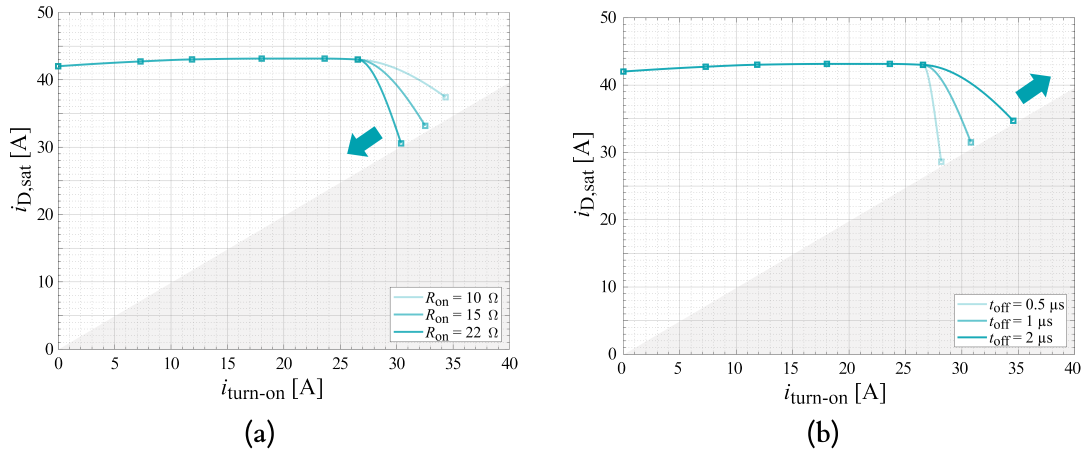


Figure 3.7: $i_{D,sat}$ saturation current values for different turn-on resistors in (a), and different turn-off periods in (b), using the second generation 140 mΩ_{typ} 650 V GaN GIT, [50, 51].

The lower the turn-on resistor, the faster the switch will turn-on, reducing the switching losses and improving the saturation current. The turn-on resistance is modified from 10 Ω to 22 Ω. The experimental results demonstrate that the turn-on resistance can either reduce or increase the saturation current, but only under the highest turn-on current conditions (the most critical scenarios for the switching losses perspective). With lower switching currents, the saturation current remains unchanged, even if the turn-on resistance is modified. As expected, the highest saturation currents are achieved with the lowest turn-on resistance of 10 Ω, reaching up to 37 A, an increase of 20 % compared to the value reached with the highest turn-on resistance. Similarly, the turn-off losses generated at the end of the first pulse in the DPT may influence the saturation current. To study this effect, the turn-off period is modified from 0,5 µs to 2 µs. The same device is tested under different t_{off} conditions, and the results are shown in Fig. 3.7, (b).

Modifying the off-state period (t_{off}) has a similar effect on the saturation current as changing the turn-on resistance. When t_{off} between two pulses is extended, the tested device can reach

a higher current before entering the saturation state. This behaviour could be attributed to the extension of the relaxation time or the cooling of the channel during the off-state. By separating the turn-off from the turn-on losses, the channel is given more time to return to its initial state. Notably, the saturation current is affected only under hard-switching conditions with current values close to the recommended pulse current.

Both the turn-on resistance and the turn-off period significantly impact the saturation current under the most critical hard-switching conditions. This supports the hypothesis that channel saturation under harsh hard-switching conditions is partially linked to switching losses. On the contrary, modifying the switching losses or the relaxation time does not influence the saturation when operating under softer switching conditions, such as in ZCS.

Influence of gate current on $i_{\mathrm{D,sat}}$

One critical parameter in GaN GITs is the continuous gate current needed to operate in conduction state. The datasheet of the GIT provides the typical output characteristic curve relating the continuous gate current to the drain-source voltage and the drain current (see Fig. 3.1). In the following, the influence of the gate current on the presented $i_{\mathrm{D,sat}}$ results is studied for a second-generation 140 $\mathrm{m}\Omega_{\mathrm{typ}}$ GIT. Following the same test setup and method, the $i_{\mathrm{D,sat}}$ values for minimum (ZCS) and maximum (HS) $i_{\text{turn-on}}$ values are measured for different steady-state gate currents $i_{\mathrm{G,ss}}$. The steady-state gate current is adjusted by modifying the R_{ss} value of the driving circuit, Fig. 3.2. The results, showing how the saturation current under ZCS and the HS with the highest turn-on current is reshaped, are plotted in Fig. 3.8.

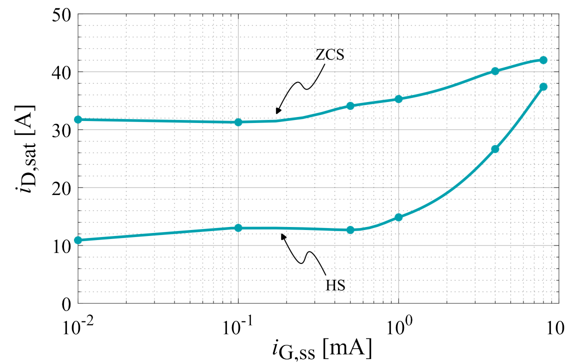


Figure 3.8: $i_{\mathrm{D,sat}}$ saturation current values for different gate currents, from 10 µA up to 8 mA, using the second generation 140 $\mathrm{m}\Omega_{\mathrm{typ}}$ 650 V GaN GIT, [50, 51].

Looking at the results, the gate current affects both the ZCS and the HS saturation current limits. These limits are reduced with the gate current until they reach minimum values. Interestingly, the results also demonstrate a stabilization in the saturation current values for very low (below 1 mA) gate currents, indicating that GITs can be operated with gate currents similar to those of SGTs (below 100 µA gate currents), penalizing the maximum drain current.

Finally, SGTs are evaluated using the same methodology. SGT devices with $R_{\mathrm{DS(on)}}$ values comparable to those of the previously assessed GaN GITs are selected, and their results are presented in Fig. 3.9. To enable a fair comparison, the current density is calculated based on the gate width, w_{g}, of each device, which can be obtained from manufacturer-provided SPICE models. When comparing the two GaN technologies, it is evident that GIT-based devices achieve higher saturation current levels than their SGT counterparts, a fact that has already been discussed in technical reports [53]. However, this advantage decreases with

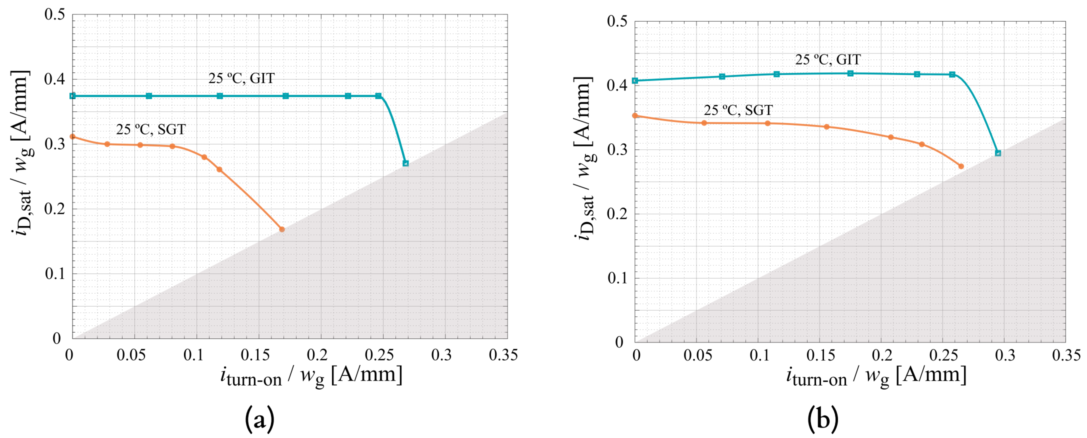


Figure 3.9: (a) $i_{D,sat}$ evaluation for 35 mΩ_{typ} 650 V GaN GIT, IGOT60R035D2, vs 37 mΩ_{typ} 700 V GaN SGT, GS-065-030-LR-TR, and (b) 140 mΩ_{typ} 650 V GaN GIT, IGLD60R140D2, vs 150 mΩ_{typ} 700 V GaN SGT, GS-065-011-2-L-TR.

smaller chip sizes. In other words, as $R_{DS(on)}$ increases, the performance difference between the two technologies becomes less significant.

It should be noted that only a limited number of samples have been tested, which restricts the ability to draw statistically robust conclusions. Variability between samples could shift or narrow the observed differences between the technologies. Furthermore, the performance of future devices may improve substantially, as already demonstrated by the latest GIT generations. Despite these limitations, the results offer valuable insights into the behaviour of saturation current under varying operating conditions and its dependence on multiple design factors. These findings provide further information to adequately design a power converter using GaN HEMTs.

3.2. Dynamic On-resistance in GaN HEMTs

GaN technology has enabled the development of transistor chips with significantly lower specific on-resistance (i.e., resistance relative to chip area) compared to Silicon and Silicon Carbide (SiC) technologies. However, GaN power devices are known to exhibit a notable dynamic behaviour in their resistance characteristics. This behaviour is particularly evident immediately after a switching event, where the on-resistance is noticeably higher than the expected steady-state value provided in datasheets, [54], [55]. The dynamic variation in on-resistance appears to be influenced by the switching conditions, such as voltage, current, and timing parameters, together with off-state bias conditions, Fig. 3.10.

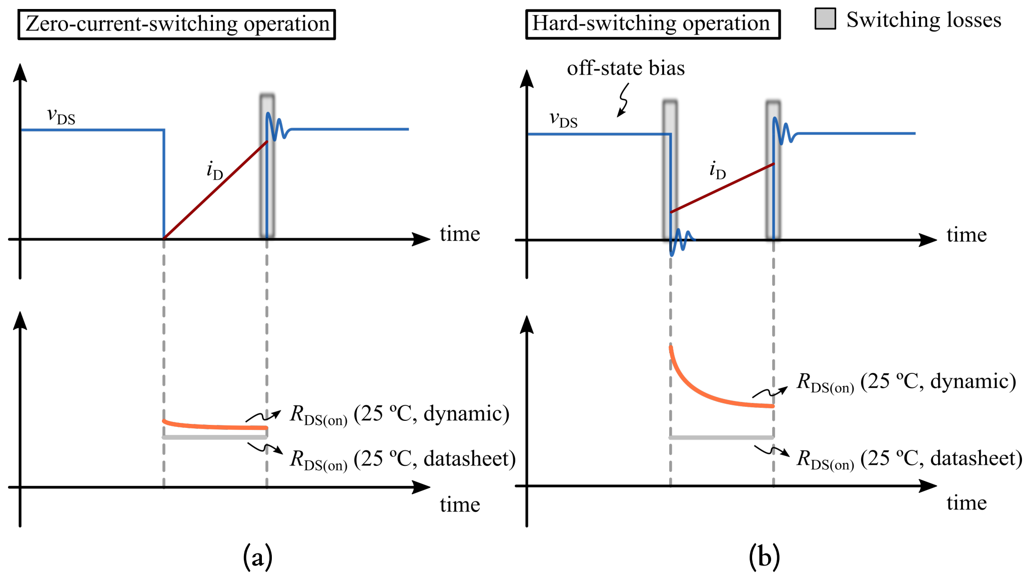


Figure 3.10: Ideal zero-current switching (a) and hard-switching (b) waveforms showing the dynamic behaviour of the $R_{DS(on)}$ on GaN HEMTs. Hard-switching, as well as harsh off-state bias conditions, increases dynamic on-resistance compared to the theoretical steady-state value provided in the datasheet by manufacturers.

Although the exact physical mechanisms responsible for this phenomenon are difficult to verify experimentally, numerous studies in the literature suggest that the dynamic behaviour of on-resistance in GaN HEMTs is primarily linked to electron trapping within the device structure. The factors influencing the severity of electron trapping within the switch are a matter of bibliographic research. Two main factors can be deduced and classified as hot electron trapping and off-state trapping.

During switching events, particularly at high frequencies or under high-voltage conditions, energetic (hot) electrons can become trapped in defect states located in the buffer layer or near the gate-drain access region. This charge trapping distorts the electric field distribution and impairs channel conductivity, resulting in a temporary increase in the $R_{DS(on)}$ immediately after the device turns on. Experimental investigations confirm that switching losses are critical in triggering this hot-electron trapping. Increased switching energy leads to stronger transient effects, further aggravating the dynamic resistance rise. As a result, the switching behaviour of the device can substantially impact overall conduction losses. In particular, devices operating with hard switching or high dv/dt and di/dt conditions are more susceptible to these effects, [56], [57].

In addition to hot-electron trapping, another mechanism associated with dynamic $R_{DS(on)}$ temporary degradation is off-state trapping. This phenomenon is influenced by the duration and magnitude of the voltage applied during the off-state. When the device is held in the off-state at high drain voltages, electrons can become trapped in surface states or buffer traps, especially under long blocking periods. This leads to what is referred to as "off-state degradation," which manifests itself as an elevated on-resistance during the on-state, [54], [58], [59].

Both mechanisms contribute to the overall dynamic behaviour of GaN HEMTs. Their combined effects must be carefully considered when designing power converters, especially in applications involving high switching frequencies and/or high voltages. Dealing with these effects is essential for ensuring reliable performance and maximizing the efficiency benefits offered by GaN technology.

Understanding the fundamentals and origins of the dynamic behaviour of the on-resistance in GaN HEMTs is only one part of the challenge addressed in the literature. Accurately measuring the on-resistance also presents significant technical difficulties. This measurement requires specialized equipment capable of detecting voltage drops in the millivolt range with high precision while connected across the *Drain* and the *Source* terminals of the power device. At the same time, the equipment must be able to withstand high blocking voltages, up to the device's breakdown voltage (typically 650 V for many high-voltage GaN HEMTs). In addition to being relatively expensive, such probes often have bandwidth limitations that can hinder accurate on-resistance measurements during the device's conduction period. To address this, several studies have proposed innovative clamping circuits that can block high voltages while enabling precise measurement in the millivolt range during conduction. One particularly affordable and reliable approach was proposed by Guacci et al. [60]. Their circuit employs Schottky diodes in combination with a low-voltage isolated power supply, enabling it to activate the measurement path only during the conduction phase. The circuit features a blanking time of approximately 200 ns to transition from blocking to measurement mode, which is sufficiently fast (valid for switching frequencies up to 1 MHz and 50% duty cycle) for capturing the on-resistance of GaN HEMTs. A simplified schematic of this proposed configuration is shown in Fig. 3.11.

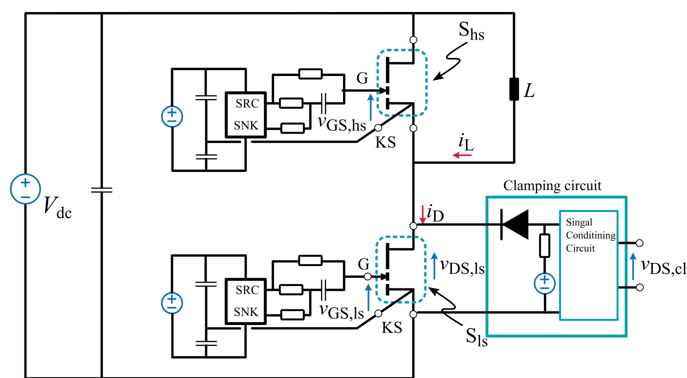


Figure 3.11: Half-bridge schematic used to evaluate the dynamic $R_{DS(on)}$ of GaN GIT switches. The voltage drop across the low-side device is measured using a clamping circuit based on the design presented in [54].

The presented board shown in Fig. 3.12 has been tested and calibrated in an attempt to measure the dynamic behaviour of the $R_{DS(on)}$ of first-generation GaN GITs from Infineon. After a proper calibration, the drain-source voltage is measured during conduction in a

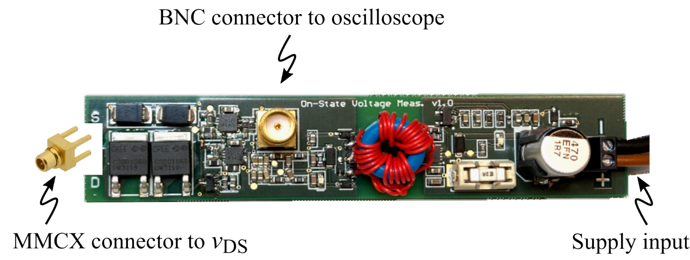


Figure 3.12: PCB used for evaluating and measuring the voltage drop across the low-side device during conduction, enabling the extraction of the $R_{DS(on)}$ of GaN GIT switches. Image courtesy of Infineon Technologies Austria AG.

multiple-pulse test. The results for the 35 mΩ_{typ} device are presented in Fig. 3.13. The device is driven with the same setup used in the previous subchapter to measure the saturation current. 35 mA steady-state gate current is used, 400 V bus voltage, 100 µH inductor, and the length of the pulses is 1 µs while stopping for 1.5 µs.

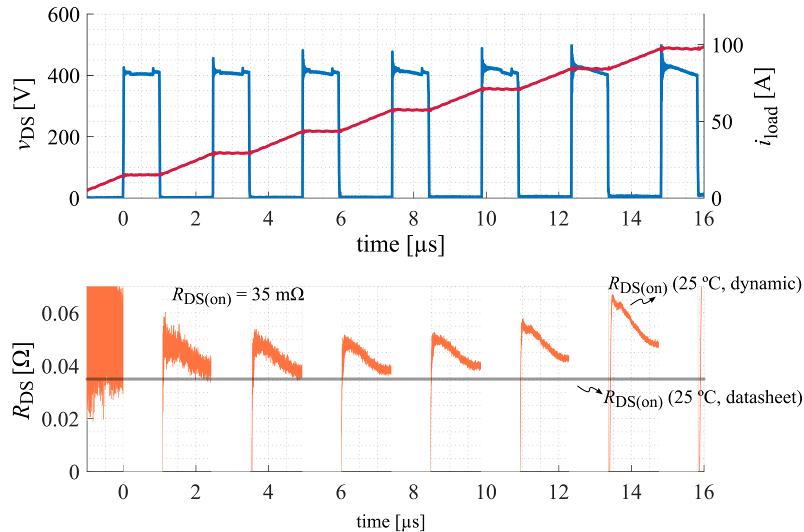


Figure 3.13: Experimental multiple-pulse test performed with the first-generation GaN GIT power switch, IGOT60R035D1. The $R_{DS(on)}$ is measured with a customized PCB based on the presented circuit in [60]. The On-state Voltage Measurement Circuit (OVMC) is calibrated accordingly before the test is performed.

The dynamic behaviour of the $R_{DS(on)}$ can be observed in the figure. In every pulse, the measured on-resistance value is higher immediately after the device is turned on, and it goes down close to the theoretical value given in the datasheet. With 0 A inductor current, the device shows an $R_{DS(on)}$ close to the expected value, $R_{DS(on)}$. While the inductor current increases during the test, the dynamic behaviour seems to be more and more pronounced. The last pulse shows a resistance value that reaches steady-state establishing at approximately 50% higher than estimated. It should be noted, that these current values are close to the recommended $i_{D,pulse}$ of the selected device. As observed in the previous subchapter, the saturation boundary under hard-switching conditions is close to 100 A. In this region, the beginning of saturation is observable, and it becomes really difficult to distinguish between what is saturation, and what is dynamic on-resistance. Combining these tests with the previous analysis about saturation current, it can be concluded that there is no clear frontier between

saturation and dynamic on-resistance. One phenomenon could be linked to the other.

Still, these values of $R_{\mathrm{DS(on)}}$ displacement are far from what some other manufacturers showed in their reports. Technological differences in the construction of the GaN device can provide significant differences in the dynamic magnitude of the $R_{\mathrm{DS(on)}}$, even reaching suppression with some latest technologies, [61], [62]. To note, the GIT technology has demonstrated promising properties for suppressing this phenomenon, especially with second-generation devices, [53] [63], as well as the newest SGT generations claimed by some manufacturers, [64].

3.3. Short-Circuit Robustness with GaN HEMTs

Short-circuit robustness is a key topic in the literature addressing the challenges and characteristics of GaN devices. In certain power electronic applications, such as variable-speed drive systems and in compliance with some automotive standards (e.g., AEC-Q101, ISO 26262), power semiconductors are expected to withstand short-circuit events lasting up to 10 µs to ensure safe and reliable operation [65, 66]. This minimum withstand time provides a critical window for protection circuits to detect the fault and safely turn off the device. Silicon and SiC-based devices have already proven their robustness under short-circuit conditions, [67]. In this context, GaN HEMTs offer unique behaviour compared to their Silicon and SiC counterparts. Recent studies have shown that GaN devices exhibit a self-protection mechanism during short-circuit events: the device channel saturates, limiting the drain current and thereby reducing the energy dissipated, [68–70]. According to experimental results, under certain conditions, GaN HEMTs can withstand short-circuit durations of up to 100 µs. However, in less favorable conditions, the withstand time can drop below 1 µs. Given this variability, a deep understanding of the physical mechanisms governing GaN HEMT behaviour during short-circuit events is essential to ensure safe and reliable operation across different applications.

During a short-circuit event, the power device experiences intense power dissipation over a very short duration. This leads to a rapid increase in channel temperature due to high current and voltage stress. As the device heats up, its channel conductivity decreases, similar to when the device is saturated. This effect is particularly pronounced in GaN HEMTs, where the saturation mechanism plays a critical role in self-limiting the drain current. As the temperature rises, the reduction in conductivity further decreases the drain current, effectively limiting the total power dissipation during the fault event. This intrinsic behaviour contributes to the device's self-protection capability, potentially enhancing its short-circuit robustness, provided the thermal and electrical limits are not exceeded.

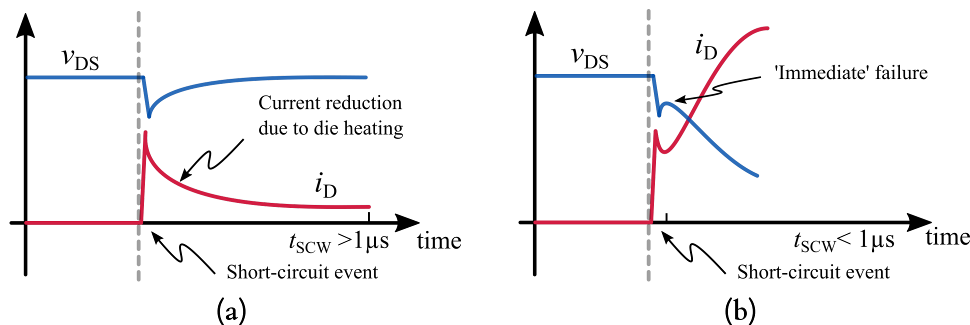


Figure 3.14: Two different types of short-circuit withstanding scenarios for GaN HEMTs. In (a), the device handles the starting current spike to reduce the drain current with self-protection properties. In this case, GaN HEMTs' short-circuit withstanding times are typically longer than 1 µs. In (b) an immediate destruction of the device is shown after the short-circuit event. In this second case the short-circuit withstanding time can be as low as 160 ns, [71].

GaN devices have demonstrated a remarkable ability to remain in this self-protection mode without destruction, primarily due to their strong temperature-dependent transconductance. This characteristic enables the device to limit current as the temperature rises, effectively avoiding thermal runaway. However, this protective behaviour is not universally guaranteed. It is effective mainly at bus voltages below 350–400 V. Under different operating conditions, particularly at higher bus voltages or more severe fault scenarios, device failure can occur in as little as 160 ns, during the initial current spike of the short-circuit event [71, 72]. The

causes of such early-stage failure have been actively investigated in the literature, with multiple contributing factors identified.

Trying to explain the causes of such variability on the short-circuit withstanding time, studies have identified two primary mechanisms responsible for the failure of GaN HEMTs under short-circuit conditions: electrical failure and thermal failure [73–75]. The electrical failure mechanism can occur within the first few nanoseconds of the short-circuit event, especially when the device is operated under bus voltages exceeding its rated specifications (e.g., >400 V for 650 V-rated devices). In such cases, failure times as short as 160 ns have been reported. This defines a critical boundary for GaN short-circuit robustness and should be considered when evaluating the safe operating limits of these devices. While electrical failure is strongly dependent on the applied bus voltage, other parameters, such as the magnitude of the initial drain current spike and the gate current, have also been suggested as contributing factors [76]. Consequently, several patents and research efforts have focused on limiting the drain current spike during the onset of a short circuit in order to extend the withstand time of GaN devices [77].

In cases where the bus voltage is kept within safe limits and the initial drain current spike is effectively controlled, the GaN HEMT is more likely to enter a saturation regime without immediate failure. In this state, the device limits the drain current through channel saturation, allowing it to withstand the fault for a longer duration, typically several microseconds, before any destructive event occurs. Under these conditions, the dominant failure mechanism shifts from electrical to thermal breakdown. During the sustained short-circuit event, high power dissipation causes rapid heating of the device's channel and junction. If the thermal energy exceeds the material or package limits before the fault is cleared, the device may fail due to thermal overstress.

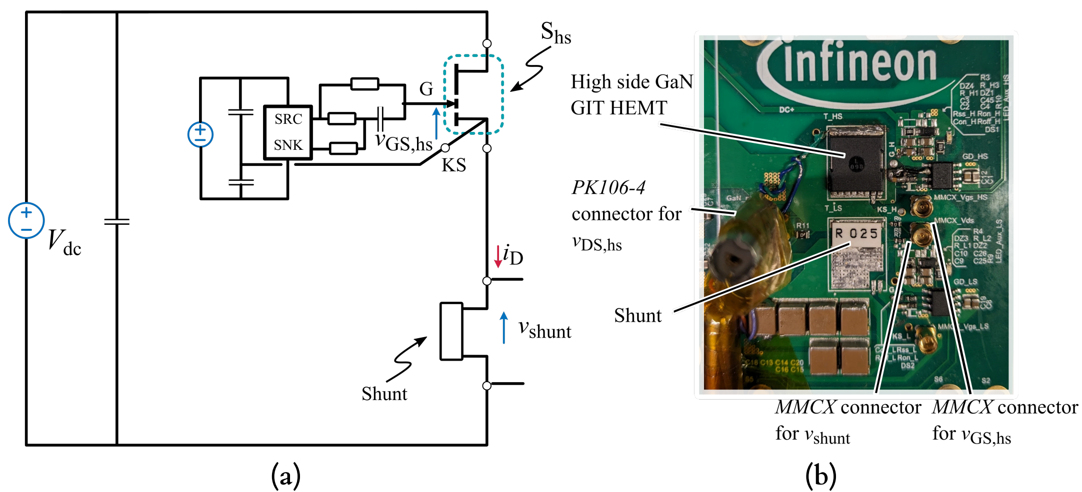


Figure 3.15: Single-switch schematic (a) and PCB board (b) used to evaluate the short-circuit robustness of GaN GIT switches. The voltage drop across the shunt is measured to estimate the drain current of the high-side switch.

To observe this second case where the GaN switches can handle long short-circuit withstanding times, several first-generation GITs have been tested. The previously used half-bridge configuration is modified, replacing the low-side switch with a shunt resistor and removing the DPT inductor from the circuit. In this way, only the high-side switch is left connected in series with the shunt resistor, and the short-circuit can be triggered with the gate driver, see Fig. 3.15, (a). The shunt voltage drop is measured, from which the drain current is deduced

($i_D \equiv i_{shunt}$). The drain-source voltage and the gate-source voltage of the high-side switch are measured too. The modified PCB can be seen in Fig. 3.15, (b). In this case, first-generation 55 mΩ_{typ} GaN GIT switches are tested. To validate the short-circuit robustness under reduced bus voltage conditions, the bus voltage is configured to 320 V. Different steady-state gate currents have been used, from 1 mA to 20 mA. Positive rail gate voltage is set to 7.5 V, while negative is set to -3 V. The turn-on resistance is 10 Ω and the turn-off resistance is 2 Ω.

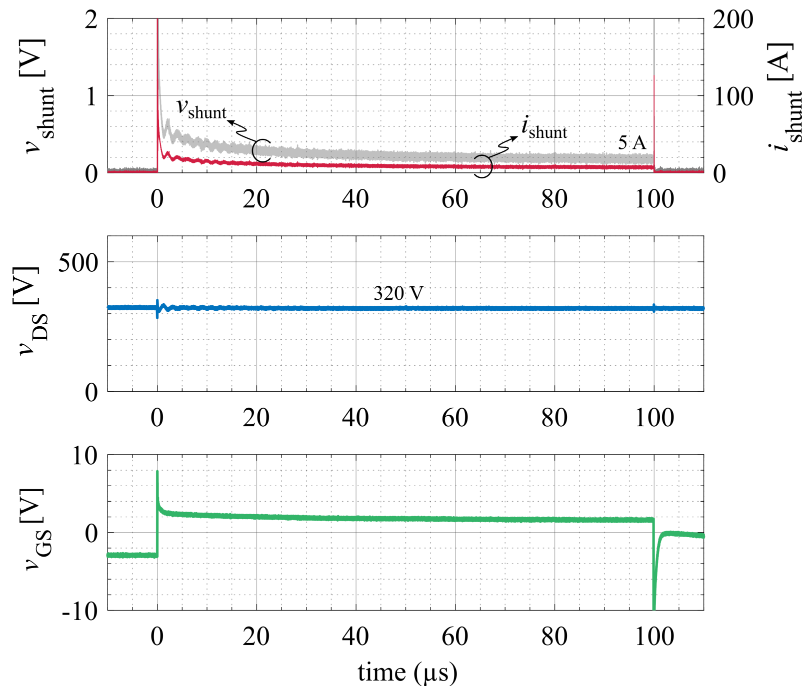


Figure 3.16: Experimental short-circuit test performed with the first-generation GaN GIT power switch, IGLT60R055D1. The drain current i_D, equivalent to the shunt current i_{shunt} is measured with a 25 mΩ shunt resistor.

Among several tested samples, not a single device has failed during the mentioned test. Even with the highest steady-state gate currents (20 mA), the devices have been subjected to 100 μs short-circuit pulses. Due to the nature of GaN, the channel gets so saturated that the drain current drops below 5 A, see Fig. 3.16. Some anomalies have been observed with extended short-circuit pulses (>100 μs), however, the devices could continue working. Repetitive tests have not been performed, and therefore, continuous degradation is not evaluated. Overall, in the performed tests, first-generation GaN GITs have demonstrated short-circuit robustness for reduced bus voltage conditions.

3.4. Conclusions

GaN HEMTs demonstrate clear advantages over traditional Silicon, SiC, and even cascode GaN-based technologies. Nevertheless, certain characteristics of GaN HEMTs pose integration challenges or require careful reconsideration when deployed in power converter applications. Beyond their distinct gate drive requirements, aspects such as saturation current, dynamic on-resistance, and short-circuit robustness remain insufficiently explored. This chapter has addressed these three aspects, including partial experimental validation.

First, the saturation current, defined as the maximum current level at which the device enters saturation, is investigated. This current limit tends to be more restrictive in GaN HEMTs compared to their Silicon counterparts, particularly when comparing devices with equivalent $R_{\mathrm{DS(on)}}$ values. This limitation is especially critical in applications subject to transient high-current demands, such as startup or fault conditions.

The saturation behaviour of both GaN GITs and SGTs is evaluated experimentally using a half-bridge configuration operating in DPT mode. The saturation current is evaluated under various transition modes, ranging from ZCS to HS, varying the switching current and time between pulses. The results show that the saturation current is partially influenced by the turn-on current and the associated switching losses, particularly near the $i_{\mathrm{D,pulse}}$ threshold. It is observed that the minimum saturation current can be modified by adjusting the turn-on resistance or the turn-off duration, which in turn affects the device's thermal and electrical relaxation. Under ZCS conditions, the saturation current increased by up to 50% compared to the minimum values observed in HS operation. Consequently, the datasheet-recommended $i_{\mathrm{D,pulse}}$ should be regarded as a conservative limit valid primarily for HS applications where the turn-on current approaches or exceeds 80% of the stated value. This confirms that GaN GITs are viable candidates for applications involving high transient peak currents, especially under ZCS conditions. Additionally, a comparison between first- and second-generation devices revealed that newer-generation GaN GITs exhibit an 8–15% increase in $i_{\mathrm{D,sat}}$ under identical gate drive conditions. A comparison between GaN GITs and SGTs further validates that GITs can offer higher saturation limits.

The dynamic on-resistance is another critical parameter that must be carefully considered when employing GaN technology. It is well established that GaN devices are particularly susceptible to variations in on-resistance under dynamic operating conditions. Numerous studies have investigated this behaviour, attributing it primarily to electron trapping effects within the device structure, particularly at the surface and buffer layers. To further explore and experimentally validate this phenomenon, a customized clamping circuit, adapted from a published literature work, is employed to accurately measure the on-resistance of a GaN GIT under a multiple-pulse test. The experimental results confirm the presence of dynamic $R_{\mathrm{DS(on)}}$ effects. However, they also reveal that GaN GIT technology exhibits a more stable and consistent $R_{\mathrm{DS(on)}}$ compared to other GaN technologies reported in the literature. This indicates that GITs may offer improved robustness against dynamic mechanisms, enhancing their suitability for demanding power conversion applications.

Finally, the short-circuit robustness of GaN HEMTs is investigated. Several studies in the literature have highlighted the unique behaviour of GaN devices under short-circuit conditions, identifying two primary failure mechanisms that depend on the operating conditions. When the drain-source voltage is below the device's rated value (e.g., 400 V for 650 V-class devices), GaN HEMTs are capable of withstanding single short-circuit pulses lasting over 100 µs. However, when the drain-source voltage exceeds a certain threshold, which is

often not explicitly defined, devices can suffer early failure, sometimes occurring within the first microsecond of the event. In this context, the case of reduced drain-source voltage is experimentally validated using GaN GITs. Short-circuit pulses of 100 μs are applied without experiencing device failure, confirming the device's robustness under these conditions. This combined bibliographic and experimental investigation provides valuable insight for the design of short-circuit protection strategies.

Chapter 4

MODELLING WBG POWER TRANSISTORS

Power converter design involves multiple stages, starting from defining the requirements for a specific application, progressing through various simulation processes, and ultimately reaching prototyping and experimental validation. One of the most critical steps in achieving a successful design is the simulation phase. Before any physical implementation, it is essential to predict how different components of the power converter will behave under the expected operating conditions. In some cases, the simulation process is skipped or supplemented with experimental testing to obtain accurate estimations of the final converter's performance. However, these additional steps extend the design timeline and can even increase overall project costs. Moreover, unexpected behaviour during experimental validation may hinder the development of a cost-effective solution. To minimize the need for experimental validation, a fast, accurate, and reliable simulation model is crucial.

Simulation tools provide an initial estimation of a power switch's behavior under specific operating conditions, offering data about circuit performance before physical implementation. Each tool varies in modelling detail and computational cost. Simulation Program with Integrated Circuit Emphasis (SPICE)-based tools like LTspice, PSpice, and SIMetrix are widely used for circuit-level simulations, delivering accurate transient and steady-state analyses of power converters. Meanwhile, specialized tools such as PLECS and PSIM focus on system-level modelling, enabling faster simulations tailored for power electronics applications. Additionally, Finite Element Method (FEM) tools like ANSYS and COMSOL are employed for electromagnetic and thermal analysis, crucial for high-power and high-frequency designs.

In this thesis, starting from the basis of SPICE modelling, an analytical model of a virtual Double Pulse Test (DPT) has been developed based on manufacturer-provided data, eliminating the need for experimental characterization. The model is formulated using state-space equations and solved with MATLAB solvers. By incorporating various circuit parasitics, it provides accurate results that closely reflect real-world behavior. This model enables the analysis of semiconductor device performance under different operating conditions, allowing for the extraction of valuable data, such as switching energy maps. This data enables the simulation and comparison of different topologies and semiconductor technologies, facilitating the design and optimization process.

4.1. Equation-Based Analytical Model

With the continuous advancement of power electronics and the emergence of faster switching devices, the consideration and analysis of circuit parasitics is becoming increasingly critical. In SPICE simulations, power switches such as Metal Oxide Semiconductor Field Effect Transistor (MOSFET), Insulated Gate Bipolar Transistor (IGBT), and Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) devices are modelled using a combination of physical equations, empirical data, and manufacturer-provided subcircuits. These models incorporate essential parameters, including charge dynamics, channel conduction behaviour, and junction temperature effects, to ensure realistic performance predictions. Furthermore, parasitic elements, such as stray inductances, capacitances, and resistances, are integrated to account for PCB layout effects and high-frequency switching behaviour. This high level of detail is essential for accurately predicting circuit performance, optimizing efficiency, and ensuring reliable operation before moving to hardware prototyping. One of the main challenges with SPICE models is the lack of standardization among switch models provided by different manufacturers. Furthermore, most manufacturers offer limited or no information on the underlying principles or methodologies used to develop these models, making it difficult to compare or modify them for specific applications. This inconsistency highlights the need for a unified approach to power switch modelling, which is a key objective of the modelling method presented in this work.

Any active semiconductor is usually approached as a set of parasitic capacitors, resistors, and inductors, together with the semiconductor's channel. Fig. 4.1 shows the equivalent model of a power switch (MOSFET, HEMT), derived from the ones presented in [78] and in [79]. The circuit includes, the input parasitic capacitances $C_{\mathrm{GS}}(f(v_{\mathrm{GS}}))$ and $C_{\mathrm{GD}}(f(v_{\mathrm{GD}}))$, and the output capacitance $C_{\mathrm{DS}}(f(v_{\mathrm{DS}}))$. These parasitic capacitances are nonlinear as their values vary with the voltage across their terminals. This voltage and capacitance ratio is typically displayed in the datasheets. The channel's current-voltage behaviour is also known as the transconductance $i_{\mathrm{ch}}(f(v_{\mathrm{GS}}, v_{\mathrm{DS}}))$, and is also provided in the datasheet. The parasitic resistances of the *Drain*, the *Gate*, and the *Source* terminals are represented by two equal resistances R_{D} and R_{S}, corresponding to the internal bond wires and/or connections between the chip and the external circuit, and the gate resistance R_{G} corresponding to the internal gate resistance. Drain and gate leakage inductances are not integrated into the power device model but are considered as external components and analysed later. The circuit of the semiconductor model is presented in Fig. 4.1.

Most parameters to feed the described semiconductor model can be obtained directly from the datasheets provided by the manufacturers, these include C_{GS}, C_{GD}, and C_{DS} as a function of v_{DS}, the transconductance curve, i_{ch}, as a function of v_{GS} and v_{DS}, and the gate parasitic resistance, R_{G}. Depending on the manufacturer, the values for the components present in the model (especially the parasitic inductances and resistances) are not directly provided; however, some of them can be found described within the SPICE model's libraries (.lib). Otherwise, literature information can be used to give reasonable value to these parasitics, [80–84].

However, the information provided in manufacturers' datasheets is sometimes limited. Insufficient details about the measurement methods and setups can become a bottleneck for accurate modelling. For example, C_{GS} and C_{GD} are typically given as a function of v_{DS} only. Some corrections and adjustments have been presented in the literature to improve the accuracy of different simplified models [11, 85]. Another example could be the lack of resolution in the transconductance curve, especially during the increase of the current with very low v_{DS} voltages. In this work, a set of assumptions is adopted to simulate the power

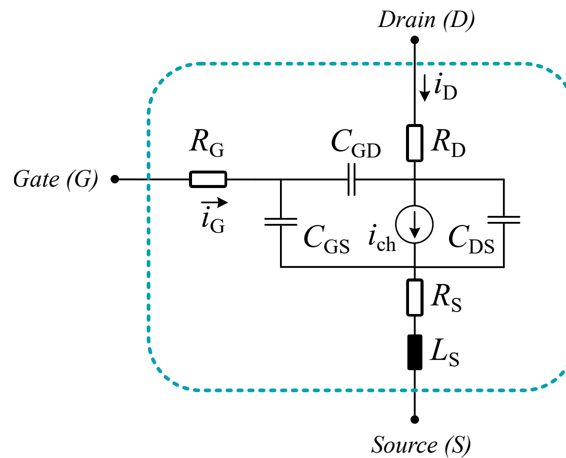


Figure 4.1: Electrical circuit used for the semiconductor model, showing the channel current i_{ch}, drain, source and gate resistances R_D, R_S, R_G, and parasitic capacitances C_{GD}, C_{DS} and C_{GS}.

Table 4.1: Main packages used for discrete power switches and their estimated parasitic values.

Packaging	CSP	DFN/QFN *	TOLL/TOLG/TOLT *	D2PAK	TO-220/TO-247
Stray inductance L_S [nH]	0.1-0.2	0.5-1	0.5-1	4-5	5-15
Stray resistance (R_D + R_S) [mΩ]	0.2-0.5	0.5-1	1-2	1-2	2-10

* A notorious difference is observed with different kinds of internal connections (copper-clip, bond-wires...)

device by leveraging and adapting datasheet information.

- Transconductance curve in the datasheet is given for continuous operation, measuring current and external voltage $v_{DS\text{-}ext}$ on the terminals of the package. In this context, the voltage drop generated by the current on R_D and R_S is not separated and therefore, is considered for correction in the model.
- C_{GS} and C_{GD} should be related to their terminal voltages. In case of C_{GD}, the influence of v_{GS} is minimal; therefore, no correction is needed. But in the case of C_{GS}, the influence of v_{GS} is notorious and is taken into account.
- The model does not include reverse recovery charges (in the case of MOSFETs). Therefore, it is not optimized for the reverse conduction state. The model is created purposely for switching loss and transient waveform estimation, and the reverse recovery phenomenon should be considered a posteriori.

The development of a customized model not only ensures data transparency for the user but also provides a universal framework for characterizing semiconductors from different manufacturers using a consistent methodology. By relying solely on datasheet values, the most standardized and widely available information, model discrepancies that could favor certain manufacturers are effectively avoided.

Beyond enabling the comparison of different semiconductors under specific operating conditions, the simplified model is designed for cross-platform compatibility (e.g., Python, MATLAB), allowing for flexible data exchange and the creation of tailored code solutions. This opens up a wide range of possibilities for data analysis and integration in diverse environments.

4.1.1. Transconductance description by polynomial function

To start with the construction of the model, the transconductance is extracted from the datasheet. A polynomial approximation has been used to replicate the transconductance curve presented in the datasheet of a selected device. Similar polynomial functions have been employed by manufacturers in their SPICE models for a wide range of devices, including Si, SiC, and GaN devices, [86].

$$i_{\mathrm{ch(dts)}} = a(1 + g v_{\mathrm{DS}})[\log(1 + \exp((v_{\mathrm{GS}} - b)/c))^{d} - \log(1 + \exp((v_{\mathrm{GS}} - b - e v_{\mathrm{DS}}^{f})/c))^{d}] \tag{4.1}$$

where a, b, c, d, e, f, and g are constant parameters that need to be adjusted for each semiconductor. This can be easily achieved by using a curve fitting tool. It is important to note that defining parameter boundaries in the curve fitting tool can help achieve the required values. In this work, all the lower boundaries have been defined as 0, to have all the variables positive and avoid any convergence issues, and the upper boundaries as infinite, except in the case of b, which is defined in $1.5V_{\mathrm{TH}}$.

The presented equation can describe the transconductance curve given by any manufacturer with a high accuracy level. Nevertheless, some errors could be present in the same curve or could arise when extracting the data points due to graphical inaccuracy, especially when analysing low-ohmic devices. For this reason, a correction factor is added to the equation. This factor matches the curve with the theoretical curve described by the given $R_{\mathrm{DS(on)}}$. The error is mostly observed within the low voltage drop region ($v_{\mathrm{DS}} < 1$ V), see conflictive region in Fig. 4.2, which is why the correction factor is implemented with an exponential effect, starting from maximum correction value and converging into unity after v_{DS} is higher than 1 V. The correction factor is calculated for a current value I_{Kc},

$$K_{\mathrm{C}} = \frac{I_{\mathrm{Kc}}}{i_{\mathrm{ch(dts)}}(v_{\mathrm{GS(max)}}, v_{\mathrm{DS(Kc)}})} \tag{4.2}$$

where $v_{\mathrm{DS(Kc)}}$ is the theoretical voltage drop $I_{\mathrm{Kc}}R_{\mathrm{DS(on)}}$ at the selected current.

$$i_{\mathrm{ch}} = i_{\mathrm{ch(dts)}}(1 - (1 - K_{\mathrm{C}})(\frac{1}{\exp(5v_{\mathrm{DS}})})) \tag{4.3}$$

Besides the correction factor, the defined curve $i_{\mathrm{ch(dts)}}$ does not separate the voltage drop generated in the R_{S} and R_{D} parasitic resistances, and thus, can not be considered equal to the channel current function required by the semiconductor model, i_{ch}. To solve this issue, after doing all the curve fitting and calculating the correction factor, the v_{DS} input value in the polynomial equation is multiplied by a factor of $1+(R_{\mathrm{D}}+R_{\mathrm{S}})/R_{\mathrm{DS(on)}}$. Various semiconductors have been characterized by this method for comparison purposes and to design high-frequency power converters. The estimated values of different variables in the polynomial equation are presented in the Table 4.2:

4.1.2. Parasitic capacitances description by interpolation

The parasitic capacitances C_{ISS}, C_{OSS}, and C_{RSS} are extracted from the device datasheet and then translated into the capacitance components used in the model. Based on fundamental

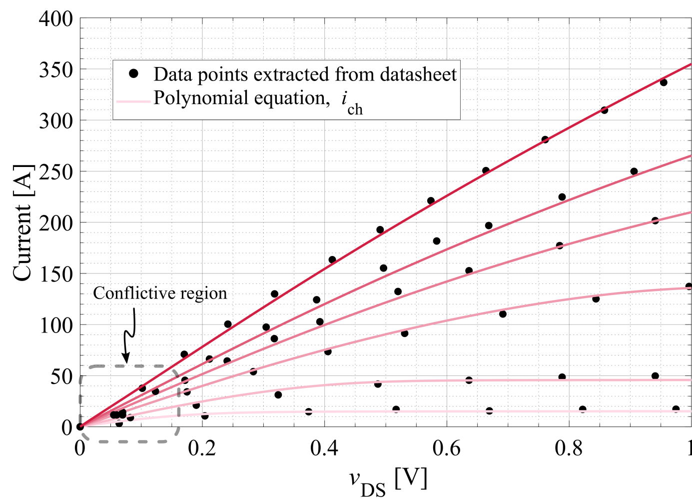


Figure 4.2: Extracted transconductance data from the datasheet for different v_{GS} values, and the calculated curves with the polynomial equation, side by side for 100 V, 2.7 mΩ, ISC027N10NM6 MOSFET.

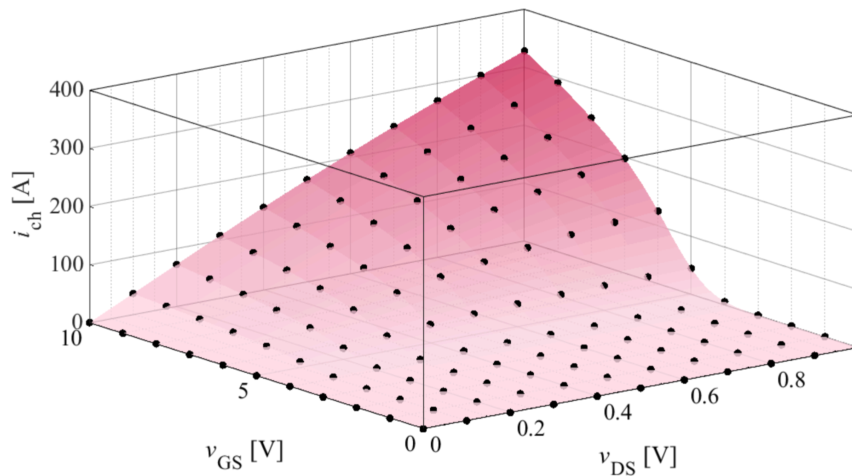


Figure 4.3: 3D representation of the extracted transconductance data points from the datasheet and the obtained curves with the polynomial equation, for 100 V, 2.7 mΩ, ISC027N10NM6 MOSFET.

relationships, C_{GD} corresponds directly to C_{RSS}, while C_{DS} is obtained as $C_{OSS} - C_{RSS}$. According to their terminals, C_{DS} depends on v_{DS}, consistent with the datasheet values. Although C_{GD} can also be influenced by v_{GS}, especially at low v_{DS}, its dependency on v_{DS} is considered significantly stronger. Therefore, for simplicity, the C_{GD} is adopted directly from the datasheet as a function of v_{DS}, Fig. 4.4 (a).

The capacitance C_{GS} could be estimated as $C_{ISS} - C_{RSS}$; however, it is largely unaffected by v_{DS} and strongly dependent on v_{GS}. This behaviour is not captured in the capacitance curves provided in the datasheet.To model C_{GS} more accurately, Q_G versus v_{GS} curve is used. The value of C_{GS} is derived from the slope (dQ/dV) representing the gate charge Q_G as a function of v_{GS}. This graph also reveals the Miller plateau, a region where gate capacitance increases as the channel begins to conduct. When the conduction channel forms, the *Gate* becomes coupled to the *Source* through the channel, introducing additional capacitance. To

Table 4.2: Values used for the parameters describing the typical output characteristics curve, obtained by curve fitting, for various GaN HEMTs, and Silicon (Si) MOSFETs.

Code	**semi.**	V_{BR}	a	b	c	d	e	f	g	K_C
EPC2206	GaN	80	6.110	1.800	0.166	1.688	1.084	0.943	1.618e-11	0.684
EPC2218	GaN	100	18.519	1.800	0.260	1.293	1.763	0.795	2.166e-10	0.366
GAN3R2-100CBE	GaN	100	3.154	1.650	0.154	1.597	1.335	0.958	4.753e-12	0.994
GS61008T	GaN	100	0.790	1.679	0.042	1.270	1.630	0.917	2.337e-14	0.438
ISC009N06LM5	Si	100	75.903	2.627	0.182	1.171	1.428	0.960	0.077	0.689
ISC027N10NM6	Si	100	12.271	4.110	0.385	1.546	1.775	0.941	1.353e-4	0.743
IAUCN08S7N013	Si	100	22.030	4.200	0.113	1.212	1.451	0.986	0.143	0.912
GS66506B/T	GaN	650	2.197	1.805	0.044	1.130	0.152	0.957	1.583e-11	0.895
GS0650111L	GaN	650	0.735	2.079	0.131	1.130	0.679	0.973	2.337e-14	0.985
GS0650116L	GaN	650	1.171	2.550	0.193	1.012	0.791	0.994	6.813e-10	0.987

prevent convergence issues caused by a theoretically infinite capacitance during the plateau, this increase is approximated with a linear transition, Fig. 4.4 (b).

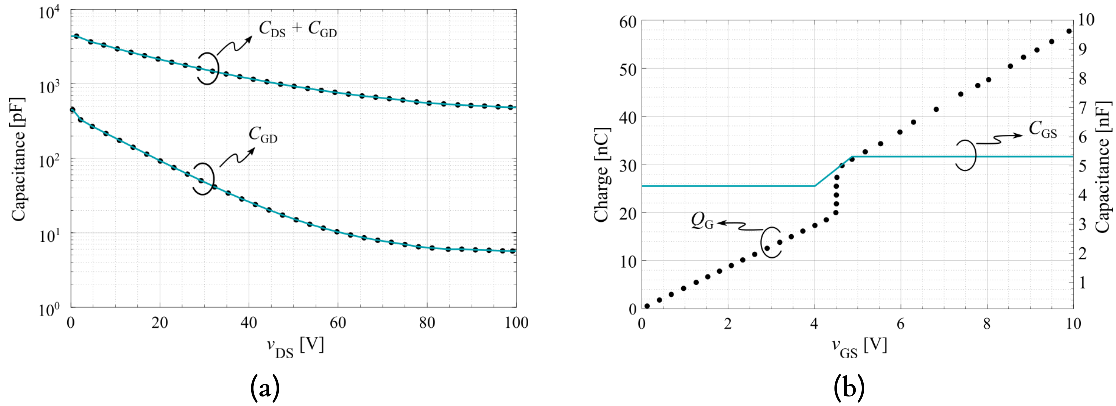


Figure 4.4: Extracted capacitance data points from the datasheet and the obtained curves with interpolation, side by side for 100 V, 2.7 mΩ, ISC027N10NM6 MOSFET.

Finally, the capacitance values used in the model are obtained through interpolation of the extracted data. Instead of employing curve-fitting techniques, gridded interpolant functions are utilized. This approach allows the model to directly reference a pre-defined set of capacitance values over a grid of voltage points, providing a more accurate and efficient representation of the non-linear behaviour of parasitic capacitances.

By relying on interpolation rather than mathematical fitting, the implementation is simplified, and the computational burden is significantly reduced. This results in faster simulation times without compromising the fidelity of the model, particularly in regions where capacitance values change abruptly, such as around the Miller plateau. The use of gridded interpolants also ensures that the model remains flexible and can easily be adapted to different devices by updating the input datasets.

4.1.3. Generic semiconductor models

Using the same methodology, generic models have been developed for both Silicon MOSFETs and GaN HEMTs. These models enable consistent comparisons across different chip sizes and semiconductor technologies, significantly reducing the effort and time needed to extract parameters from datasheets. Moreover, they allow for broader semiconductor analyses involving various converter topologies, case studies, and application scenarios. The generic models are derived from a reference device, with their transconductance characteristics and parasitic capacitances scaled to emulate a target chip size corresponding to a specified $R_{DS(on)}$. The objective of these models is not to emulate with high accuracy a desired device, but to compare multiple chip sizes and semiconductor technologies under the same working conditions.

To begin with, the transconductance curve is adjusted to match the theoretical behaviour expected from a device with the desired $R_{DS(on)}$. This is accomplished by scaling the polynomial equation (defined in Equation 4.3) by a constant factor. This approach enables the construction of a theoretical transconductance profile representative of a generic power transistor, Fig. 4.5.

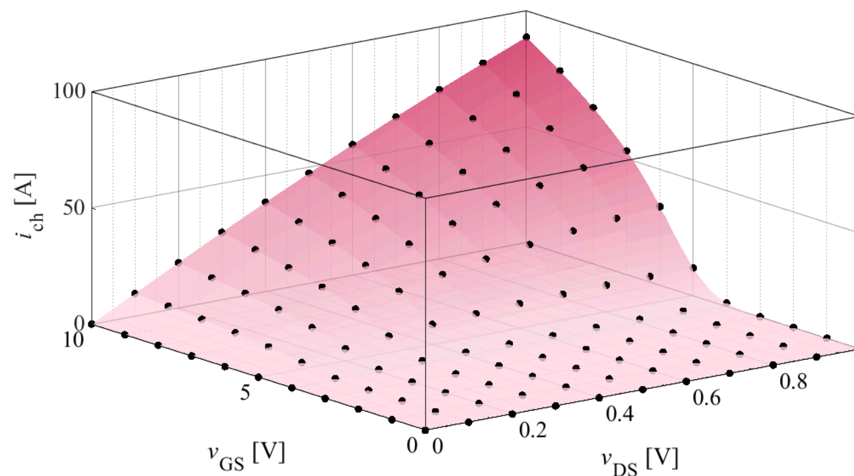


Figure 4.5: Example of the transconductance surface generated for a 100 V, generic power transistor with an on-resistance of 10 mΩ. The plot shows the output current i_{ch} as a function of gate-source voltage v_{GS} and drain-source voltage v_{DS}.

The value of $R_{DS(on)}$ is also used to scale the parasitic capacitances. However, the relationship between these parameters is nonlinear and highly dependent not only on the device's breakdown voltage (v_{BR}) but also on the underlying technology (planar, Superjunction,...). For this reason, a brief market analysis is conducted by selecting and examining a range of commercially available power semiconductor devices. The parameters under study include the typical on-state resistance $R_{DS(on)}$, as well as the constant capacitance values specified at a given drain-source voltage and gate conditions: $C_{ISS@\ vds\text{-}rated}$, $C_{OSS@\ vds\text{-}rated}$, and $C_{RSS@\ vds\text{-}rated}$. The selected devices are categorized based on their breakdown voltage, with groups formed for power switches rated between 80 V and 100 V, and between 650 and 700 V. The typical rated voltage at which the constant capacitance values are given ($vds - rated$) is 40 V for 80 V devices, 50 V for 100 V devices, and 400 V for 650 V devices. This analysis aims to identify the typical relationship between $R_{DS(on)}$ and the associated parasitic capacitances and charge values. The results are plotted in Fig. 4.6, Fig. 4.7, and Fig. 4.8.

All the scattered data is fitted into a second-order exponential equation, where $R_{DS(on)}$ is

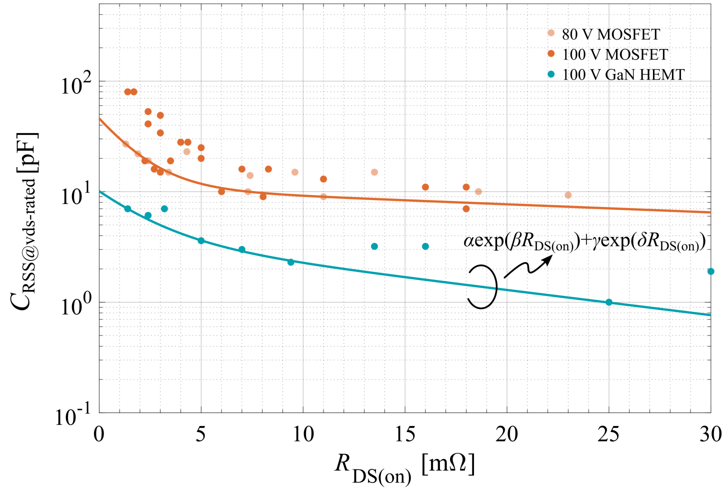


Figure 4.6: Relationship between typical on-resistance $R_{\mathrm{DS(on)}}$ and reverse transfer capacitance C_{RSS} at the rated drain-source voltage ($v_{\mathrm{DS}} = v_{\mathrm{rated}}$) for various power devices. The plot includes data for 80 V and 100 V Silicon MOSFETs, as well as 100 V GaN HEMTs. The curves illustrate the general exponential trend of C_{RSS} as a function of $R_{\mathrm{DS(on)}}$, fitted using the model $\alpha \exp(\beta R_{\mathrm{DS(on)}}) + \gamma \exp(\theta R_{\mathrm{DS(on)}})$.

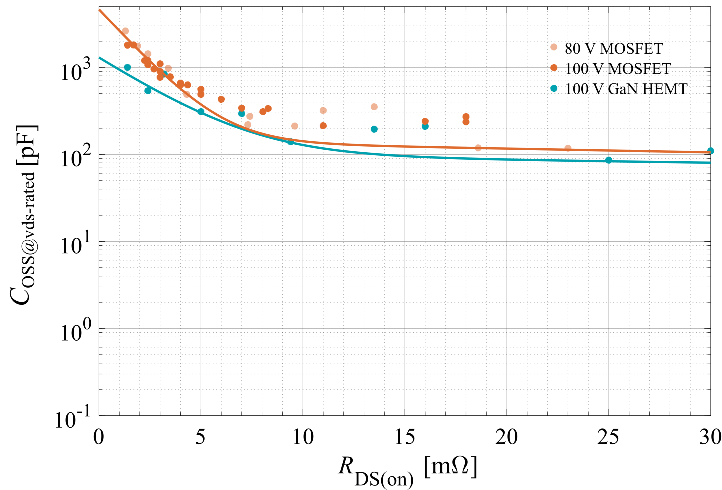


Figure 4.7: Relationship between typical on-resistance $R_{\mathrm{DS(on)}}$ and output capacitance C_{OSS} at the rated drain-source voltage ($v_{\mathrm{DS}} = v_{\mathrm{rated}}$) for various power devices. The plot includes data for 80 V and 100 V Silicon MOSFETs, as well as 100 V GaN HEMTs.

given in [mΩ], and the result in [pF] for capacitance, and [nC] for charge:

$$C/Q_{@vds-rated} = \alpha \exp(\beta R_{\mathrm{DS(on)}}[\mathrm{m\Omega}]) + \gamma \exp(\theta R_{\mathrm{DS(on)}}[\mathrm{m\Omega}]). \quad (4.4)$$

This equation defines the minimum boundary obtained from the market analysis, and thus represents the best-in-class power switches for each group. This guarantees that the obtained results with different semiconductor groups are up to date with the latest generation improvements. The variables α, β, γ, and θ used in Equation 4.4 obtained by the curve fitting technique are presented in Tab. 4.3.

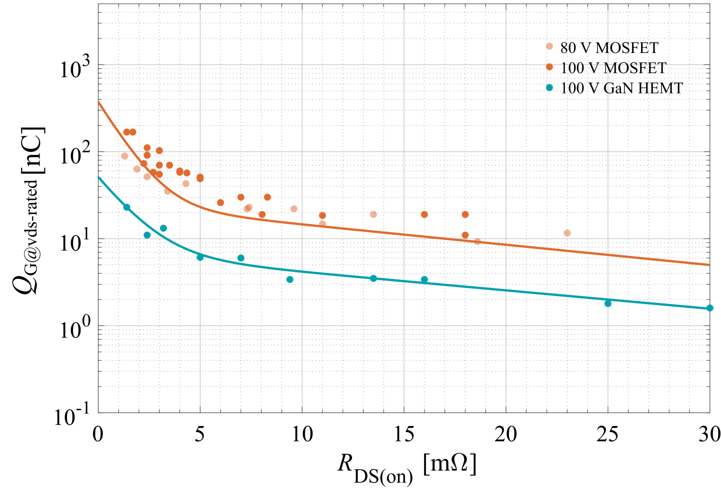


Figure 4.8: Relationship between typical on-resistance $R_{DS(on)}$ and total gate charge Q_G at the rated drain-source voltage ($v_{DS} = v_{rated}$) for various power devices. The plot includes data for 80 V and 100 V Silicon MOSFETs, as well as 100 V GaN HEMTs.

Table 4.3: Parameters for estimating parasitic capacitances and gate charge at rated voltage for different semiconductor groups.

Generic model	Capacitance	α	β	γ	θ
80 V / 100 V Si MOSFET	$C_{RSS@vds\text{-}rated}$	35.2012	-0.5839	10.7487	-0.0168
	$C_{OSS@vds\text{-}rated}$	4500	-0.5861	142.5503	-0.0100
	$Q_{G@vds\text{-}rated}$	350	-0.8894	24.9038	-0.0536
100 V GaN HEMT	$C_{RSS@vds\text{-}rated}$	6.4292	-0.4165	3.6677	-0.0540
	$C_{OSS@vds\text{-}rated}$	1200	-0.3523	100	-0.0073
	$Q_{G@vds\text{-}rated}$	44.5578	-0.7009	6.7413	-0.0486
650 / 700 V Si MOSFET	$C_{RSS@vds\text{-}rated}$	200.0000	-0.0728	3.4385	-0.0000
	$C_{OSS@vds\text{-}rated}$	222.9897	-0.0450	53.2343	-0.0060
	$Q_{G@vds\text{-}rated}$	270.7714	-0.0379	53.4426	-0.0044
650 / 700 V GaN HEMT	$C_{RSS@vds\text{-}rated}$	78.6010	-0.0870	0.5320	-0.0019
	$C_{OSS@vds\text{-}rated}$	155.2427	-0.0225	14.7238	-0.0000
	$Q_{G@vds\text{-}rated}$	20.9112	-0.0448	4.0594	-0.0056

4.1.4. DPT circuit analysis and evaluation

In addition to constructing a semiconductor model based on datasheet parameters and polynomial equations, the model must be integrated into an environment that accurately replicates the behaviour of a power converter, including typical external parasitic elements. A well-established method for characterizing semiconductors under such operating conditions is the construction of a half-bridge DPT circuit, which allows the prediction of the behaviour of the device in various working scenarios. Traditionally, the DPT is implemented experimentally to obtain real measurement data. However, this approach requires a dedicated test bench with integrated measurement capabilities, which in addition, has to replicate the target application, making it impractical when characterizing a wide range of semiconductor devices with differ-

ing sizes and properties. Furthermore, the fast switching dynamics of Wide BandGap (WBG) semiconductors and the sensitivity to external parasitics complicate the acquisition of reliable results [87].

To enable consistent comparison of different devices under defined operating conditions, a fully analytical model of a DPT half-bridge circuit is proposed, as shown in Fig. 4.9. This model includes external parasitic effects, which on a power converter are typically present, and is composed of two semiconductor blocks (T_1, and T_2) driven by datasheet-derived parameters, enabling performance estimation without the need for physical testing.

An input DC voltage source V_{dc} supplies the input capacitor C_{in} of a half-bridge. The wiring and connection between the input and the capacitor are represented as a resistance R_{in} and inductance L_{in} in series. The input capacitance holds the input voltage v_{in} switched by both semiconductors in a half-bridge configuration. In a DPT environment, this switched voltage is applied to one terminal of the load, whereas the other terminal is connected to the positive rail of the input (comprising an inductor). In the analytical model, the inductive load is modelled by a known current source. Other parasitics of the model include the power loop inductance L_{loop} and resistance R_{loop} in series with the Device Under Test (DUT), and the gate loop's external resistance $R_{\mathrm{G\text{-}ext}}$ and inductance L_{G}. For simplicity, $R_{\mathrm{G\text{-}ext}}$ and R_{G} are combined into R_{G}. A snubber is also included in the circuit if overvoltage mitigation is desired.

The DPT circuit is defined by 12 equations, (4.5)-(4.16), and reshaped in state-space format, (4.17) and (4.18). I_{L}, V_{dc}, $V_{\mathrm{G,T1}}$ and $V_{\mathrm{G,T2}}$ are defined as input signals to the model (**U**). T_1 and T_2 which can also be addressed as the device under test (for T_1) and the synchronous device (for T_2) represent the semiconductor devices.

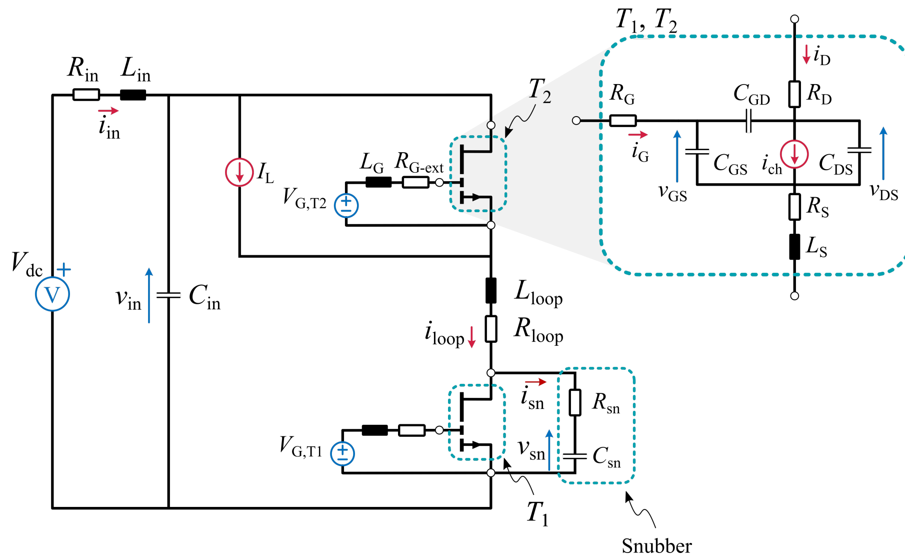


Figure 4.9: Description of the analytical model of a half-bridge, showing the same configuration used in typical DPT. The semiconductor devices, T_1 and T_2, are defined according to the semiconductor's datasheet parameters. The rest of the components are defined according to the requirements and literature.

$$V_{\mathrm{G,T1}} = v_{\mathrm{GS,T1}} + i_{\mathrm{G,T1}} R_{\mathrm{G,T1}} + \frac{di_{\mathrm{G,T1}}}{dt}(L_{\mathrm{G,T1}} + L_{\mathrm{S,T1}}) + \frac{di_{\mathrm{D,T1}}}{dt} L_{\mathrm{S,T1}} + R_{\mathrm{S,T1}}(i_{\mathrm{G,T1}} + i_{\mathrm{D,T1}}) \tag{4.5}$$

$$V_{\mathrm{G,T2}} = v_{\mathrm{GS,T2}} + i_{\mathrm{G,T2}} R_{\mathrm{G,T2}} + \frac{di_{\mathrm{G,T2}}}{dt}(L_{\mathrm{G,T2}} + L_{\mathrm{S,T2}}) + \frac{di_{\mathrm{D,T2}}}{dt} L_{\mathrm{S,T2}} + R_{\mathrm{S,T2}}(i_{\mathrm{G,T2}} + i_{\mathrm{D,T2}}) \tag{4.6}$$

$$v_{\mathrm{sn}} = v_{\mathrm{DS,T1}} + L_{\mathrm{S,T1}}(\frac{di_{\mathrm{G,T1}}}{dt} + \frac{di_{\mathrm{D,T1}}}{dt}) + R_{\mathrm{D,T1}} i_{\mathrm{D,T1}} + R_{\mathrm{S,T1}}(i_{\mathrm{G,T1}} + i_{\mathrm{D,T1}}) - R_{\mathrm{sn}}(i_{\mathrm{loop}} - i_{\mathrm{D,T1}}) \tag{4.7}$$

$$v_{\mathrm{in}} = v_{\mathrm{sn}} + R_{\mathrm{sn}}(i_{\mathrm{loop}} - i_{\mathrm{D,T1}}) + i_{\mathrm{loop}} R_{\mathrm{loop}} + \frac{di_{\mathrm{loop}}}{dt} L_{\mathrm{loop}} + v_{\mathrm{DS,T2}} + R_{\mathrm{S,T2}}(i_{\mathrm{G,T2}} + i_{\mathrm{D,T2}}) + i_{\mathrm{D,T2}} R_{\mathrm{D,T2}} + L_{\mathrm{S,T2}}(\frac{di_{\mathrm{G,T2}}}{dt} + \frac{di_{\mathrm{D,T2}}}{dt}) \tag{4.8}$$

$$i_{\mathrm{G,T1}} = \frac{dv_{\mathrm{GS,T1}}}{dt}(C_{\mathrm{GS,T1}} + C_{\mathrm{GD,T1}}) - \frac{dv_{\mathrm{DS,T1}}}{dt} C_{\mathrm{GD,T1}} \tag{4.9}$$

$$i_{\mathrm{D,T1}} = i_{\mathrm{ch,T1}} + \frac{dv_{\mathrm{DS,T1}}}{dt}(C_{\mathrm{DS,T1}} + C_{\mathrm{GD,T1}}) - \frac{dv_{\mathrm{GS,T1}}}{dt} C_{\mathrm{GD,T1}} \tag{4.10}$$

$$i_{\mathrm{G,T2}} = \frac{dv_{\mathrm{GS,T2}}}{dt}(C_{\mathrm{GS,T2}} + C_{\mathrm{GD,T2}}) - \frac{dv_{\mathrm{DS,T2}}}{dt} C_{\mathrm{GD,T2}} \tag{4.11}$$

$$i_{\mathrm{loop}} = I_{\mathrm{L}} + i_{\mathrm{ch,T2}} + \frac{dv_{\mathrm{DS,T2}}}{dt}(C_{\mathrm{DS,T2}} + C_{\mathrm{GD,T2}}) - \frac{dv_{\mathrm{GS,T2}}}{dt} C_{\mathrm{GD,T2}} \tag{4.12}$$

$$\frac{dv_{\mathrm{sn}}}{dt} = (i_{\mathrm{loop}} - i_{\mathrm{D,T1}})/C_{\mathrm{sn}} \tag{4.13}$$

$$\frac{di_{\mathrm{L}}}{dt} = \frac{di_{\mathrm{loop}}}{dt} - \frac{di_{\mathrm{D,T2}}}{dt} \tag{4.14}$$

$$i_{\mathrm{in}} = C_{\mathrm{in}} \frac{dv_{\mathrm{in}}}{dt} + i_{\mathrm{loop}} \tag{4.15}$$

$$V_{\mathrm{dc}} = v_{\mathrm{in}} + R_{\mathrm{in}} i_{\mathrm{in}} + L_{\mathrm{in}} \frac{di_{\mathrm{in}}}{dt}. \tag{4.16}$$

State-space variables (**X**) are selected to be the following

$$\boldsymbol{X} = [v_{\mathrm{GS,T1}}, i_{\mathrm{G,T1}}, v_{\mathrm{GS,T2}}, i_{\mathrm{G,T2}}, v_{\mathrm{DS,T1}}, v_{\mathrm{DS,T2}}, i_{\mathrm{D,T1}}, i_{\mathrm{D,T2}}, v_{\mathrm{in}}, i_{\mathrm{in}}, v_{\mathrm{sn}}, i_{\mathrm{loop}}]'. \tag{4.17}$$

Among different available solvers, **ode23s** has been chosen for its suitability for this kind of stiff problem and the trade-off between accuracy and speed. The state-space equations are solved with MATLAB,

$$\frac{d\boldsymbol{X}}{dt} = \boldsymbol{AX} + \boldsymbol{BU}. \tag{4.18}$$

Unlike the typical DPT test bench which requires two full periods to measure correctly hard-switching on and off transitions, the initial conditions can be defined to start in steady-state mode, for that, I_{L} can be defined as a DC $I_{\mathrm{L,dc}}$ with a known current ripple ΔI_{L}, requiring

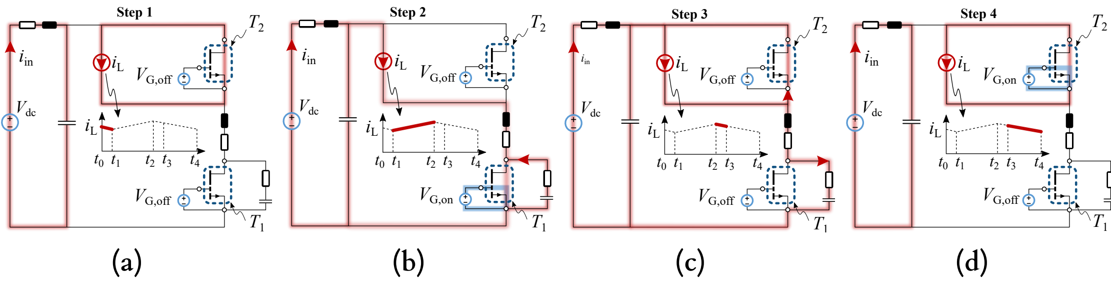


Figure 4.10: (a) Step 1 refers to the deadtime (t_{dt}), when both switches are off ($V_{G,T1} = V_{G,off}$ and $V_{G,T2} = V_{G,off}$), (b) Step 2 refers to the time in which the T_1 switch is on, $V_{G,T1\ (t1 \to t2)} = V_{G,on}$, (c) Step 3; between t_2 and t_3 a deadtime t_{dt} is applied where the two switches remain switched off ($V_{G,T1} = V_{G,off}$ and $V_{G,T2} = V_{G,off}$) and (d) Step 4 refers to the time in which the T_2 switch is on, ($V_{G,T2\ (t3 \to t4)} = V_{G,on}$)

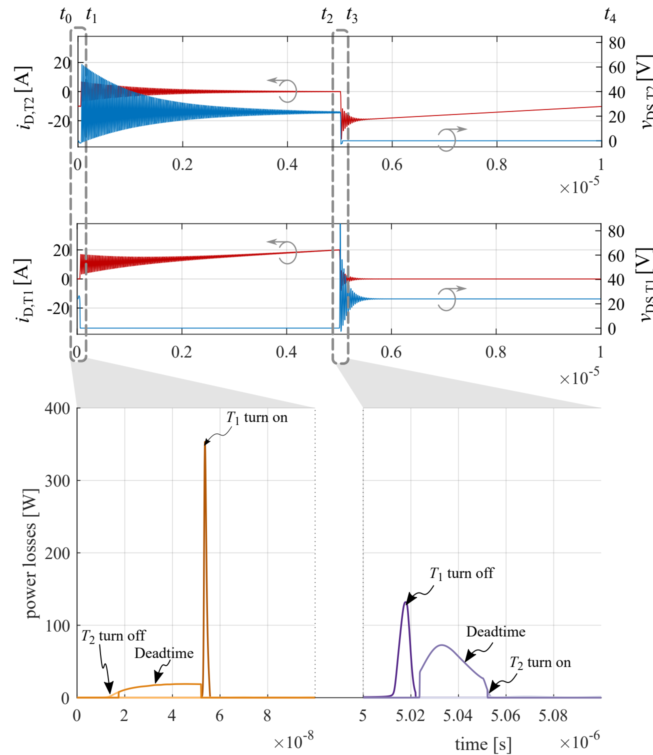


Figure 4.11: Analytical model results using EPC2218 devices. For the simulation: $L_{loop} = 20\,\text{nH}$, $R_{loop} = 20\,\text{m}\Omega$, $C_{sn} = 0.5\,\text{nF}$, $R_{sn} = 2.2\,\Omega$, $R_{G\text{-on}} = 4.8\,\Omega$, $R_{G\text{-off}} = 6.2\,\Omega$, $\delta = 50\%$, $t_{dt} = 50\,\text{ns}$, $V_{dc} = 24\,\text{V}$, $V_{G\text{-on}} = 5\,\text{V}$, $V_{G\text{-off}} = 0\,\text{V}$, $I_{L,dc} = 15\,\text{A}$, and $\Delta I_L = 10\,\text{A}$.

only a single period simulation to estimate hard-switching on and off transitions. In this way, the process is described in four steps, conditioned by the input signals, as shown in Fig. 4.10.

The results for a period are presented in Fig. 4.11, along with the calculation of different power losses. In this simulation, the selected switch for T_1 and T_2 is the EPC2218 from Efficient Power Conversion.

4.2. Parasitics Influence in Power Converters

The analytical model serves as a simulation tool to study the behaviour of power switches under various scenarios, particularly when parasitic elements vary in significance. The impact of these intrinsic components has been previously analysed in the literature [88], [89], [90]. In the following, the influence of several parasitic elements in the electrical schematic shown in Fig. 4.9 is investigated. Using the GaN HEMT EPC2218 (100 V, 3.2 mΩ) as the reference switch, the effects of modifying individual parasitics (power loop inductance (L_{loop}), common source inductance (L_{S}), gate loop inductance (L_{G}), and gate resistance (R_{G})) on the switching losses of the device under test are studied for inductor currents ($I_{\text{L}} \equiv i_{\text{o}}$) ranging from 2 A to 20 A. Switching energy (E_{sw}) is calculated based on the analysis of current and voltage waveforms, as illustrated in Fig. 4.11. The analysis assumes no snubber network ($C_{\text{sn}} = 0$, $R_{\text{sn}} = \text{inf}$). The baseline parameters for the simulations are: $L_{\text{in}} = 1$ nH, $R_{\text{in}} = 5$ mΩ, $L_{\text{loop}} = 1$ nH, $R_{\text{loop}} = 5$ mΩ, $R_G = 5$ Ω, $L_G = 3$ nH, duty cycle $\delta = 50\%$, dead time $t_{\text{dt}} = 100$ ns, $V_{\text{dc}} = 24$ V, $V_{\text{G-on}} = 5$ V, $V_{\text{G-off}} = 0$ V, and inductor current ripple $\Delta I_L = 0$ A.

4.2.1. Gate resistance

First, the gate resistance R_{G} is changed from 5 Ω to 15 Ω. The power losses are calculated with each resistance value, and the switching energy for the DUT switch is estimated. The results for the turn-on and turn-off switching energy are shown next, in Fig. 4.12.

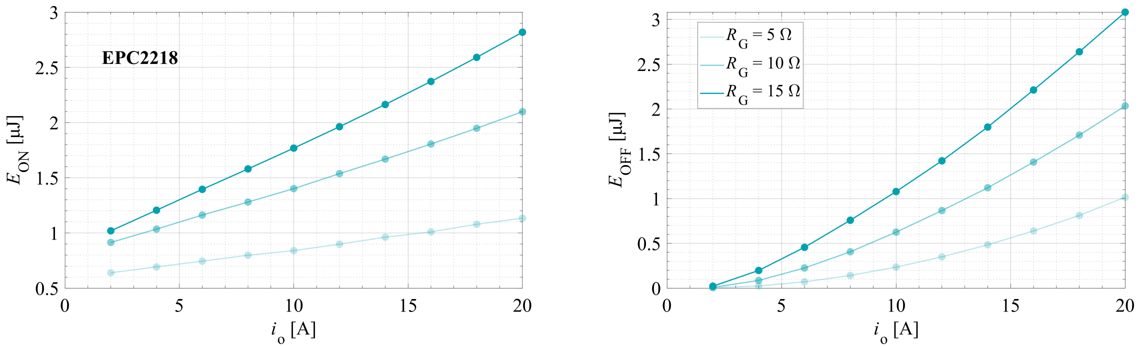


Figure 4.12: Switching losses map for EPC2218 obtained using the analytical model, with different gate resistance values going from 5 Ω to 15 Ω. The output current is defined from 2 A to 20 A.

Looking at Fig. 4.12, it is clear that a higher gate resistance represents higher switching losses, which seems reasonable according to higher resistance implies slower switching transitions. In the studied case with the selected switch, the switching energy increases almost threefold along with the gate resistance. Establishing a deadtime of 100 ns, the shoot-through between the DUT and synchronous switch is avoided for all studied cases.

4.2.2. Gate inductance

Similarly, the gate resistance is fixed at 5 Ω, and the gate inductance L_G is modified from 1 nH up to 10 nH to see how minimizing the gate loop could influence the dynamics of the DUT. The effect of the gate parasitic inductance in the switching losses is estimated and shown in Fig. 4.13.

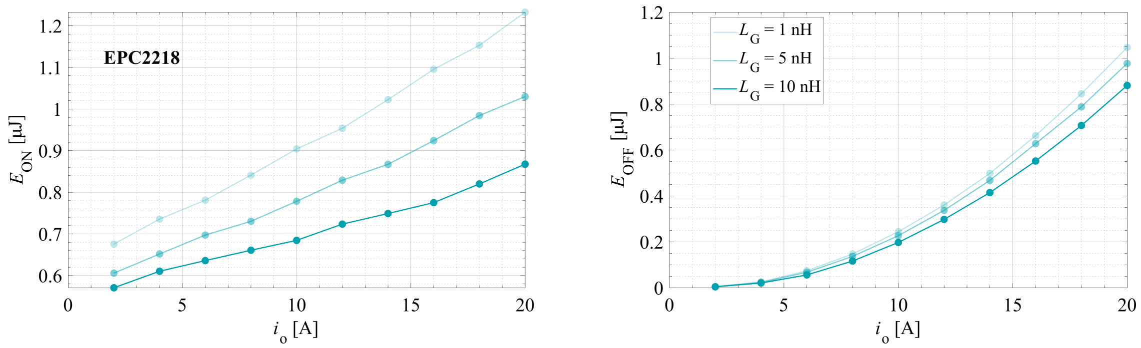


Figure 4.13: Switching losses map for EPC2218 obtained using the analytical model, with different gate inductance values going from 1 nH to 10 nH. The output current is defined from 2 A to 20 A

The switching energy losses obtained for varying gate inductance values, ranging from 1 nH to 10 nH, indicate that increasing gate inductance does not necessarily lead to higher losses. In fact, a moderate increase in gate inductance can reduce switching losses. This behaviour has also been observed and discussed in the literature [90]. When the gate inductance increases up to a certain optimal value, it can enhance gate drive dynamics, leading to faster transitions and thus lower energy losses. However, beyond this optimal point, further increases in inductance begin to slow down the switching transitions, which results in increased losses.

Gate parasitics influence not only the switching dynamics but also the gate overvoltages. These voltage spikes must be carefully monitored and controlled, particularly in GaN Schottky Gate Transistor (SGT) devices, as their maximum gate voltage ratings are very close to their nominal operating voltages. To address this, the gate voltage behaviour is also analysed in Fig. 4.14.

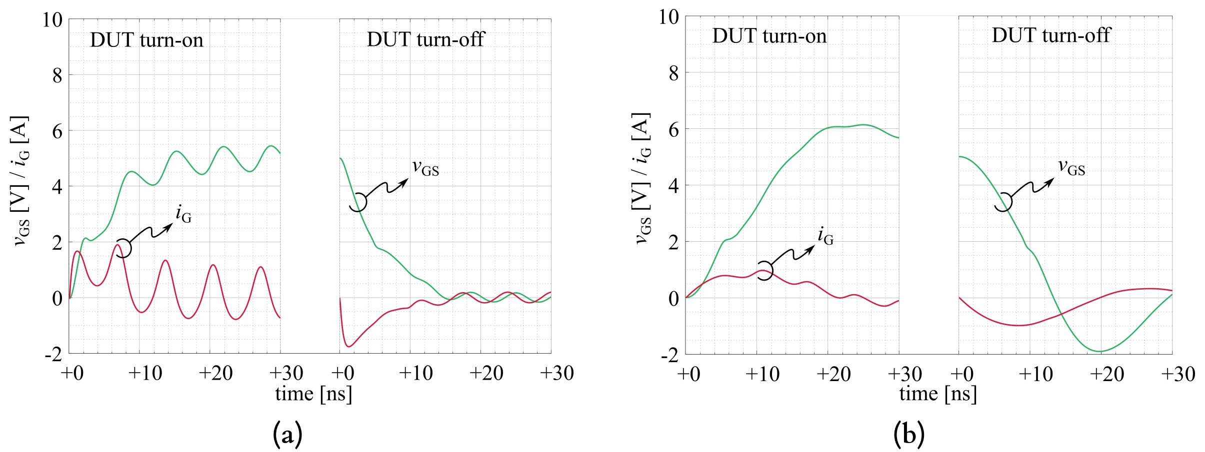


Figure 4.14: Voltage and current waveforms using EPC2218 device, and a) with 1 nH of power loop inductance, and b) with 10 nH gate loop inductance. Output current of 20 A, and switching frequency of 100 kHz.Turn-on gate voltage is 5 V, and 0 V for turn-off.

The results show that both gate voltage overshoot and undershoot increase with higher gate inductance, a trend that is consistent with findings reported in other literature, [91]. Operating with a gate loop inductance of 10 nH can lead to gate voltage overshoots and undershoots of approximately ±1 V relative to the nominal values. While this may appear non-critical in some technologies, it becomes a significant concern when using GaN SGTs, which typically have absolute maximum and minimum gate voltage ratings of +6 V and -2 V,

respectively. Moreover, gate resistance also plays a key role in shaping this behaviour, affecting both the magnitude and duration of voltage transients. Consequently, careful attention must be paid to the design of the gate loop when working with GaN devices to ensure reliable and safe operation.

4.2.3. Power loop inductance

Next, the power loop inductance is modified from 1 nH to 10 nH, with fixed gate inductance and resistance values. The switching energy losses during the turn-on and turn-off transitions are shown in 4.15.

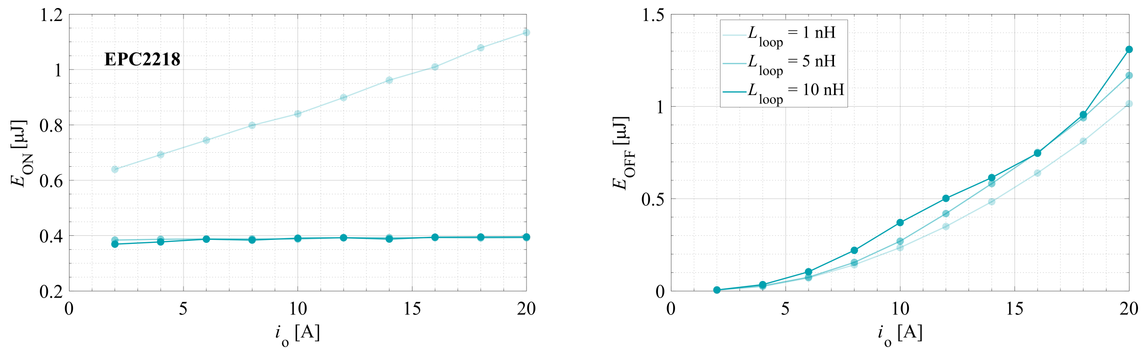


Figure 4.15: Switching losses map for EPC2218 obtained using the analytical model, with different power loop inductance values going from 1 nH to 10 nH. The output current is defined from 2 A to 20 A. L_G is 3 nH, and R_G is 5 Ω.

In terms of power losses, the results indicate that turn-on energy losses are reduced, while turn-off energy losses tend to increase. The presence of a series inductance in the current path slows down the current rise during the turn-on transition. Additionally, it introduces a voltage drop opposite in polarity to the drain-source voltage of the DUT, effectively reducing the overlap between voltage and current while the output capacitance is still being discharged, thereby lowering turn-on losses. Conversely, during the turn-off transition, the same inductance slows down the current fall, and the resulting voltage drop adds to the drain-source voltage. This leads to an increased voltage across the DUT's terminals, which contributes to higher energy losses during turn-off.

Below, in Fig. 4.16, voltage and current waveforms of the DUT switch are shown for a power loop inductance of 1 nH (a) and 10 nH (b).

The main difference between the waveforms in (a) and (b) is the oscillation introduced by the parasitic inductance. The voltage spike occurring during the turn-off of the top switch is the most critical event to consider, as its magnitude can become a limiting factor and may lead to device failure if not properly mitigated. Several studies have addressed this issue by minimising inductance through layout optimisation [92], and have also shown that the resulting oscillations can significantly worsen electromagnetic interference (EMI) [93].

4.2.4. Common source inductance

The common source inductance, L_S, affects the behaviour of the power loop as well as the control loop simultaneously, hence its name. It is mainly defined by the kind of package used

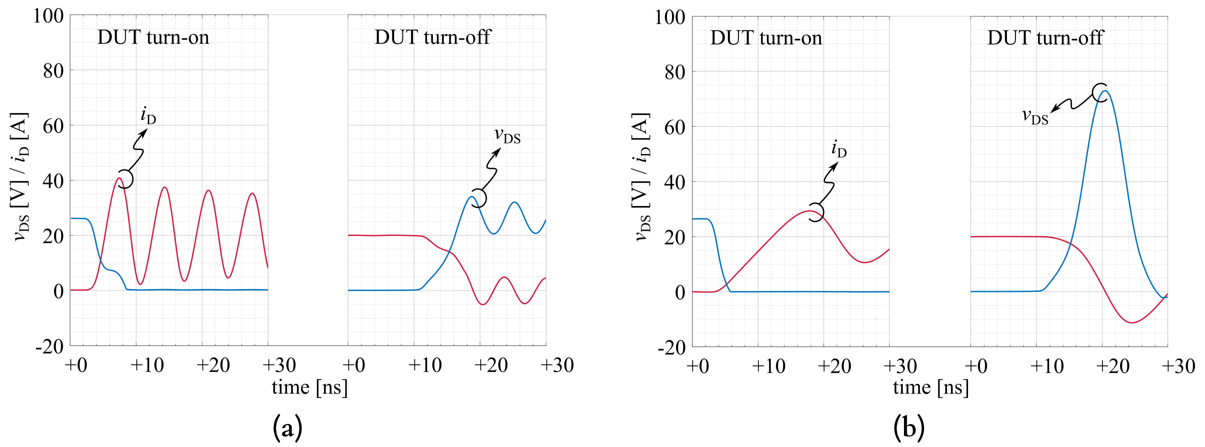


Figure 4.16: Voltage and current waveforms using EPC2218 device, and a) with 1 nH of power loop inductance, and b) with 10 nH power loop inductance. Output current of 20 A, and switching frequency of 100 kHz. Switching voltage is 24 V.

with the power switch and the interconnections between the chip and the terminals. The switching losses are shown in Fig. 4.17 along with the switching drain current for different common source inductance values, L_S, ranging from 100 pH to 1000 pH.

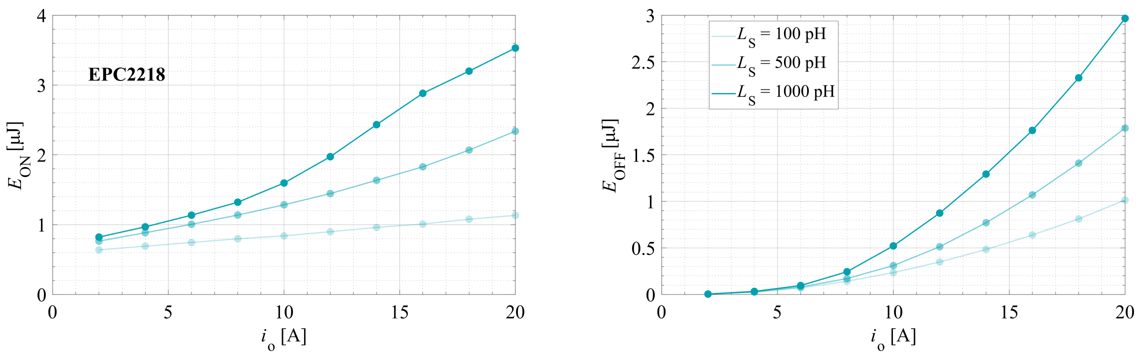


Figure 4.17: Switching losses map for EPC2218 obtained using the analytical model, with different common source inductance values going from 100 pH to 1000 pH. The output current is defined from 2 A to 20 A.

Fig. 4.17 shows that the inductance value significantly increases the switching energy losses of the hard-switching device, as also reported in the literature [94], [88]. The inductance is responsible for coupling the power loop with the gate loop, linking drain current and drain-source voltage dynamics to gate dynamics. Higher inductance leads to increased drain-source and gate voltage oscillations, which in turn prolong the switching transition time and thus increase switching losses. The switching losses can increase by more than 3 times with a 1000 pH inductance than with 100 pH at 20 A drain current. This analysis verifies the importance of using optimized packages, especially with the latest generation of power switches.

4.3. Experimental Validation: Silicon-based Push-pull Converter

A case study is selected and thoroughly analysed employing the proposed analytical model to compare the results against experimental measurements. Electrical and thermal measurements are obtained experimentally under different operating conditions and compared with the values estimated with the analytical model. The case study focuses on a voltage-fed push-pull converter based on Silicon MOSFETs, operating under hard-switching conditions, where the switches are significantly affected by the circuit's parasitic inductances. First, the circuit's current and voltage are experimentally measured to validate the overvoltage estimations at the terminals of the power switches. Subsequently, a calorimetric test is conducted under nominal conditions to validate the analysis and estimation of the switching losses. The original work is presented in [95].

4.3.1. Voltage-fed push-pull topology

The voltage-fed push-pull topology is recognized for its minimal component count, offering a cost-effective solution for applications where efficiency is not the primary concern. It is characterized by having two conversion stages (primary and secondary) separated by an isolation transformer. The primary side consists of two switches referenced to the primary's ground, while each of the *Drain* is connected to one winding of the primary side of the transformer, as shown in Fig. 4.18. The converter's ideal current and voltage waveforms are plotted in Fig. 4.19. T is the full switching period.

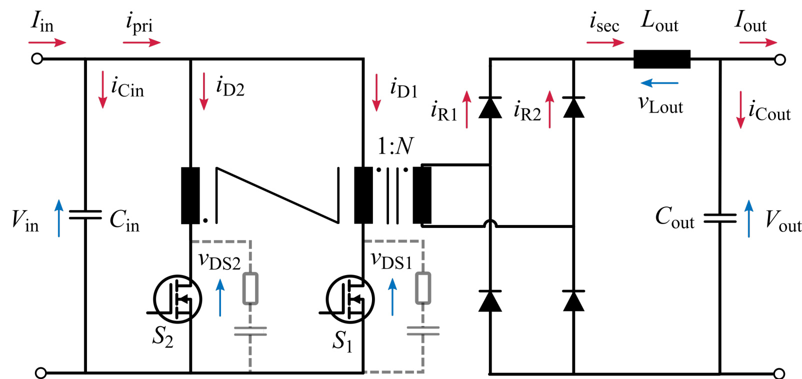


Figure 4.18: The studied push-pull converter topology, with the main primary switches S_1 and S_2, the input capacitance C_{in}, transformer, output rectifying diodes, output LC filter with L_{out} and C_{out}, and RC snubbers (in grey).

The conduction time of each semiconductor, t_{on}, is determined by the duty cycle (δ), which controls the applied voltage to the transformer's primary side and, consequently, regulates the output voltage. Both active switches operate in a complementary manner: when S_1 is on, the energy is transferred to the secondary side, and the transformer is magnetized. During this time, the voltage applied to half of the primary winding is reflected in the other half, causing switch S_2 to block $v_{DS2} = 2V_{in}$. When S_1 is turned off, the core demagnetizes through the secondary winding. In the second half of the cycle, S_2 turns on, repeating the process with the core magnetizing in the opposite direction, [96]. The leakage inductance of the transformer L_{lk} can be considered as part of the power loop, affecting the switching

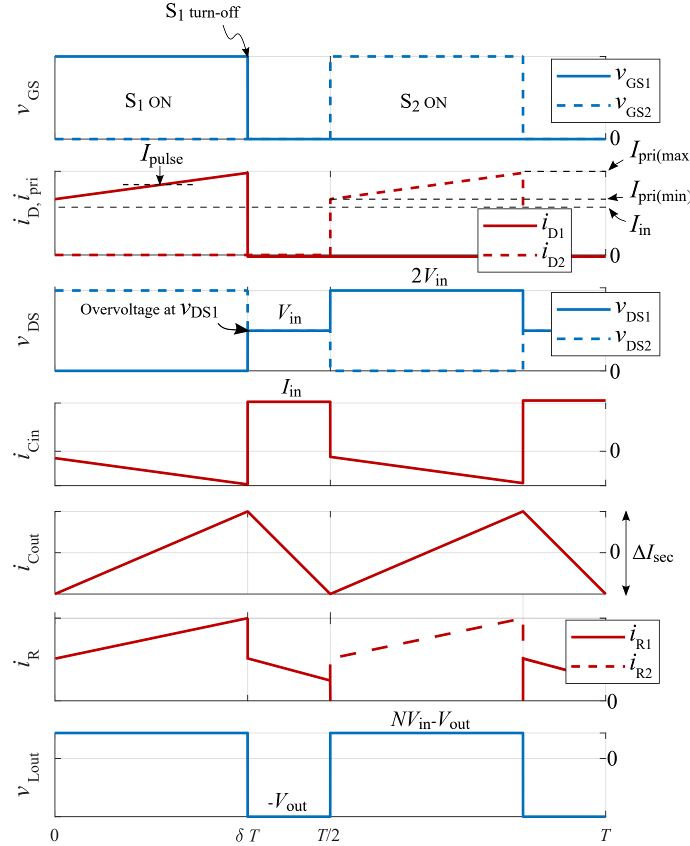


Figure 4.19: Push-pull converter's ideal waveforms, with $\delta = 35\%$ for each switch, showing gate-source voltage (v_{GS}), drain current (i_{D}), drain-source voltage (v_{DS}), input capacitor's current (i_{Cin}), output capacitor's current (i_{Cout}), output rectifiers' current (i_{R}), and output inductor's voltage (v_{Lout}).

dynamics of the semiconductors. The *di/dt* during switching transitions generates a voltage drop across the leakage inductance, reducing the v_{DS} during turn-on and increasing it during turn-off. Considering the voltage drop across the power loop inductance, especially during the transistors' turn-off, is crucial when selecting the right semiconductors and estimating the limits of the push-pull converter. The turn-off *di/dt* (di/dt_{fi}), which is defined by the turn-off current and the turn-off speed, and the power loop inductance (mainly leakage inductance of the transformer), define the magnitude of the voltage spike between the drain-source of the switches, Fig. 4.20.

$$di/dt_{\mathrm{fi}} = \frac{I_{\mathrm{pulse}} + \Delta I_{\mathrm{pri}}/2}{t_{\mathrm{fi}}}. \tag{4.19}$$

I_{pulse} is the average drain current i_{D} of the switches during the on-state, which can be calculated following

$$I_{\mathrm{pulse}} = \frac{P_{\mathrm{in}}}{2V_{\mathrm{in}}\delta}. \tag{4.20}$$

And the primary current ripple ΔI_{pri} equals

$$\Delta I_{\mathrm{pri}} = I_{\mathrm{pri(max)}} - I_{\mathrm{pri(min)}} = \frac{V_{\mathrm{in}}\delta}{L_{\mathrm{m}} f_{\mathrm{sw}}} + \frac{N V_{\mathrm{out}}(1-2\delta)}{2L_{\mathrm{out}} f_{\mathrm{sw}}}. \tag{4.21}$$

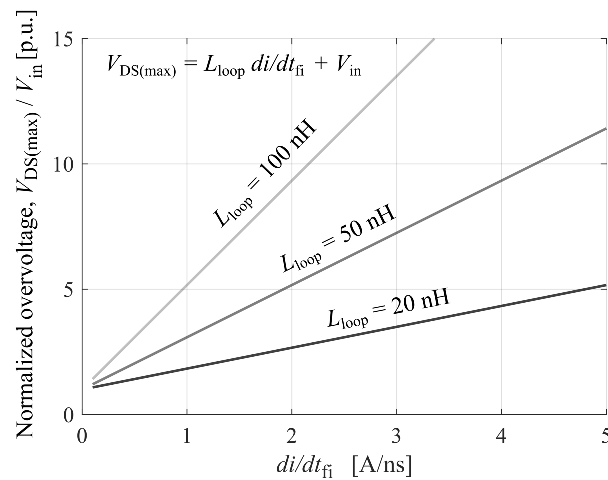


Figure 4.20: The power loop inductance L_{loop} and the turn-off di/dt effect on the normalized overvoltage affecting the power switches.

Minimizing the leakage inductance is the key to optimizing the voltage-fed push-pull converter. Conversely, extending the turn-off time for a given turn-off current can reduce overvoltage but may increase switching losses.

4.3.2. Experimental prototype

An experimental prototype of a voltage-fed push-pull converter is employed to validate the theoretical analysis. This converter is considered the baseline for future converter designs.

The converter is designed to be supplied by a 24 V nominal battery and must deliver an output voltage of 200 V with a 300 W load, with regulation capacity down to 100 V. Due to legislative requirements, galvanic isolation is mandatory. To meet these requirements, a high-frequency transformer is used with a turn ratio of $N = 9$. The nominal switching frequency is 20 kHz. The main design specifications are summarised in Table 4.4.

Table 4.4: Design characteristics of the Silicon-based push-pull converter

Parameter	Symbol	Value
Nominal output power	P_{out}	300 W
Nominal output voltage	V_{out}	100 V / 200 V
Nominal input voltage	V_{in}	20...28 V
Switching frequency	f_{sw}	20 kHz
Semiconductors	S1, S2	IRFB4410
Gate resistance	R_G	93 Ω

The push-pull converter is shown in Fig. 4.21. The analysis begins with the study of the baseline transformer. The leakage inductance is measured using a Vector Network Analyzer (VNA). Subsequently, analytical models are employed to estimate the switching losses of the main switches under nominal conditions, and the voltage and current waveforms are measured to validate the analysis. Finally, the heat sink used for dissipating the power losses is thermally characterised, enabling further experimental validation of the estimated losses. As a baseline, the

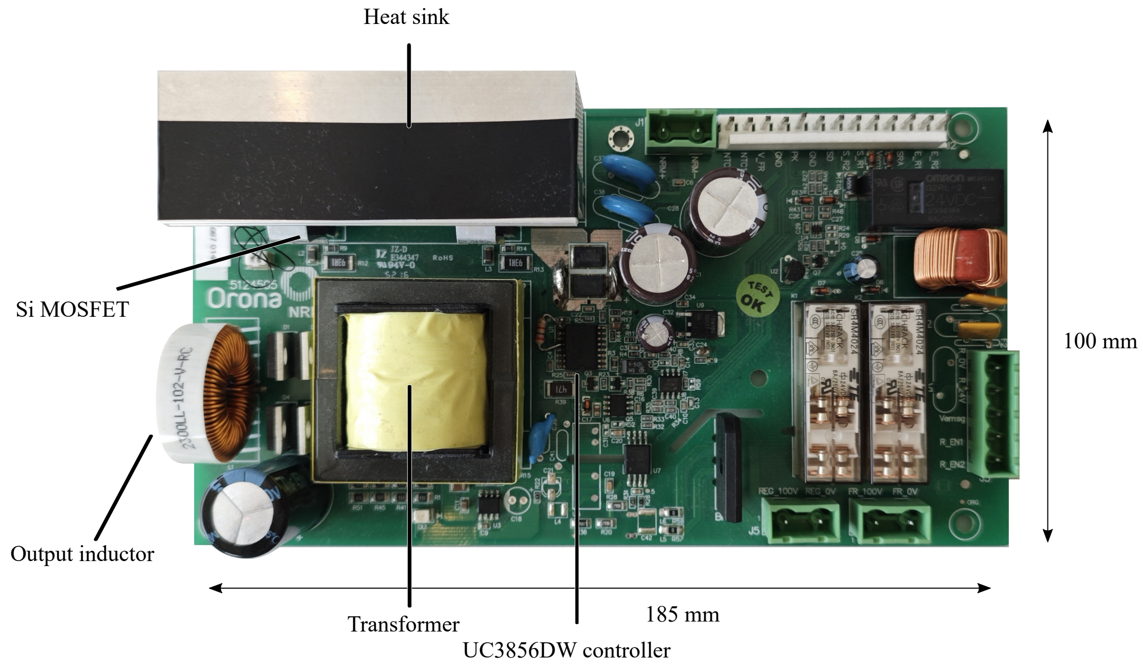


Figure 4.21: The Silicon-based push-pull prototype. The prototype is 185 mm in length, 100 mm in width, and 50 mm in height.

total volume of this converter is 925 cm^3 (725 cm^3 excluding the Electromagentic Interference (EMI) filter and safety relays), with a total cost of €11.5 for main components (power switches, transformer, and passive components). The efficiency operating under nominal conditions (V_{in} = 24 V V_{out} = 200 V, P_{out} = 300 W) reaches 91%, however, when regulating the output voltage, the efficiency drops down to 79.5%, which is considered the worst-case scenario (V_{in} = 20 V V_{out} = 100 V, P_{out} = 300 W), specially for the power switches. The efficiency curves are plotted in Fig. 4.22.

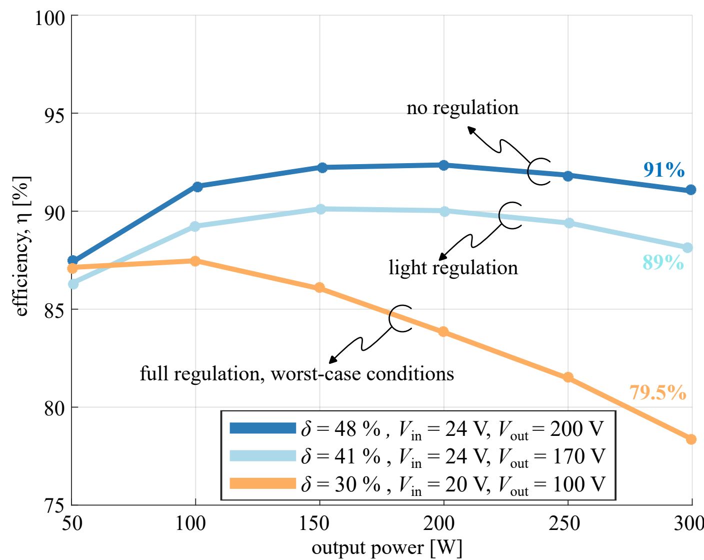


Figure 4.22: Measured efficiency of the baseline Silicon-based push-pull converter, working at different duty cycles, and power ranging from 50 W to 300 W. The operating frequency is 20 kHz.

4.3.3. Electrical measurements and calculations

In the experimental case study, the leakage inductance of the transformer is measured using a Bode100 VNA from OMICRON Lab. The measurement is performed over a frequency range from 10 kHz to 40 MHz. The turn ratio of the transformer is $N = 9$. Results for primary winding measurement are plotted in Fig. 4.23 (b), showing a primary leakage inductance value between 200 nH and 350 nH, while an equivalent result (multiplying primary inductance by N^2) is obtained measuring the secondary winding, Fig. 4.23 (d). Additionally, the magnetizing inductance is measured, with the results presented in Fig. 4.23 (a) and (c).

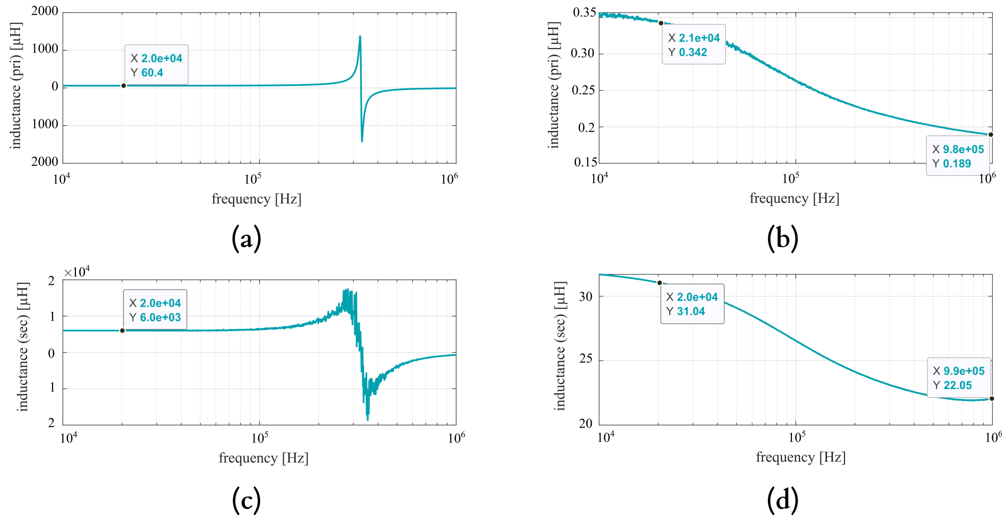


Figure 4.23: Experimental measurements using Bode100 VNA showing the transformer's magnetizing inductance in (a), (c), and the leakage inductance in (b), (d), in the Si-based push-pull converter.

The overvoltages caused by the leakage inductance are observed through experimental measurements. Turn-off waveforms captured with the oscilloscope at different power levels are shown in Fig. 4.24(a) and 4.24(b). The drain-source voltage (v_{DS}) of one switch is plotted together with the output current (i_o), which is obtained from the voltage drop across a shunt resistor. The used switch in the converter, the IRFB4410, is modelled with the presented method, considering $S_1 \equiv T_1$, and $i_{\mathrm{D}} \equiv i_{\mathrm{o}}$ in each half-period.

Both experimental and estimated switching waveforms exhibit strong agreement during the current rise and fall transitions, as shown in Fig. 4.24. The estimated drain-source voltage and the peak voltage reached during turn-off closely match the measured values, with an error of less than 10%, indicating a reliable estimation of the overvoltage. However, once the switching transitions are completed, the residual oscillations predicted by the model deviate from the measured behaviour, likely due to the model's simplifications and the omission of non-linear effects.

By relating the turn-off overvoltage and the current derivative (di/dt) from the experimental results it is demonstrated that the stray inductance seen by the active switch falls within the range of 200–350 nH. This confirms that the stray inductance impacting the turn-off of each switch is mainly due to the transformer's leakage inductance.

Experimental waveforms of i_{D} and v_{DS} are measured under different operating conditions, and the corresponding switching losses are calculated by integrating power losses. Various output levels are tested to obtain switching waveforms at different current levels. The results are presented in Fig. 4.25. A second model, here called the iterative model, is adopted from

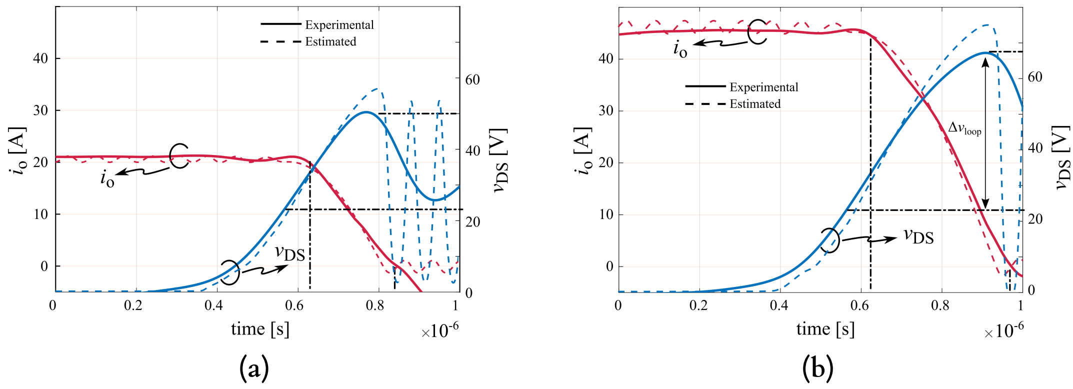


Figure 4.24: Experimental measurements and estimated waveforms of drain current ($i_D \equiv i_o$) and drain-source voltage V_{DS} of S_1 during turn-off switching, operating at (a) 300 W and 200 V output, and (b) 300 W and 100 V output. Estimated values are obtained modelling the IRFB4410 device with a $L_{loop} = 200$ nH, $L_S = 10$ nH, and $L_G = 10$ nH. Updated from [95].

the literature [11], and is included as a reference baseline and tested alongside the others for comparison.

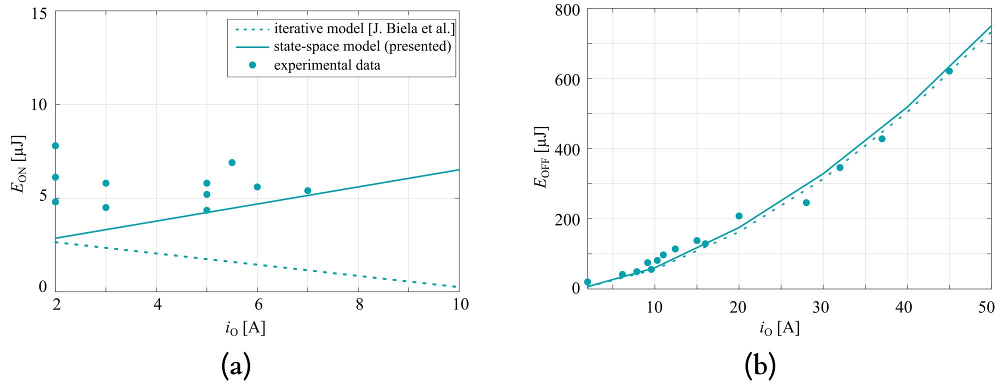


Figure 4.25: Experimental vs analytical turn on and turn off switching losses comparison of IRFB4410 power MOSFET. Estimated values are obtained modelling the IRFB4410 device with a $L_{loop} = 200$ nH, $L_S = 10$ nH, and $L_G = 10$ nH. A literature model is also replicated to compare the results and validity of the developed model, [11], [95].

The turn-on losses are plotted up to 10 A, which, based on the trapezoidal shape of the current waveforms, corresponds to the lowest duty cycle conditions ($P = 320$ W, $\delta = 21\%$, $I_{pri\text{-}min} = 10$ A, $I_{pri\text{-}max} = 50.4$ A, $I_{S\text{-}RMS} = 15.5$ A). Accordingly, the turn-off losses are analysed up to 50 A. It is observed that turn-on losses are several orders of magnitude lower than turn-off losses, a direct consequence of the overvoltage and oscillations generated by the high power loop inductance. Both models predict turn-on losses below 10 µJ. The model presented in this thesis provides a more accurate estimation of the turn-on losses, properly accounting for the effects of the power loop inductance, whereas the iterative model notably underestimates these losses.

Regarding the turn-off losses, the model presented in this thesis shows excellent agreement with the experimental fitting, confirming its validity for accurately estimating switching losses under these conditions. The comparison demonstrates that the developed model can be reliably used for preliminary calculations of total switching losses when designing a push-pull converter with similar characteristics, providing improved accuracy compared to conventional iterative

methods.

4.3.4. Calorimetric characterization of the heat sink

While capturing current and voltage waveforms during switching transitions is often considered a quick method for estimating switching losses, it is also highly sensitive to measurement inaccuracies. Since the loss calculation relies on the multiplication of two independently measured signals, any noise, bandwidth limitation, or temporal misalignment can significantly distort the resulting calculation.

A more robust and reliable alternative is the use of calorimetric methods, which determine losses based on temperature measurements in a thermally controlled and isolated environment. By directly measuring the heat dissipated by the device under nominal conditions, calorimetry eliminates the need to synchronize voltage and current waveforms, offering a more straightforward and accurate quantification of total power losses, particularly useful for benchmarking and validating analytical or simulation-based models. For this reason, in the following, a calorimetric analysis is presented to complement the validation of the analysis and the estimations obtained with the presented model.

The heat sink to which both MOSFETs are thermally coupled is characterized under controlled conditions to further validate the estimations obtained from the analytical models. A controlled current source is connected between the *Source* and the *Drain* terminals of the MOSFETs, and by adjusting the current at different levels, constant conduction losses are generated in the Silicon die due to the voltage drop across the body diode. Starting from 3 A, the current is incrementally fixed at various levels, and at each step, the temperature evolution is monitored for up to 330 seconds (over 5 minutes). For each current level, the heat sink is allowed to cool down to ambient temperature before proceeding to the next test. The temperature evolution for dissipated powers ranging from 2 W to 37 W (corresponding to the combined losses of S_1 and S_2) is shown in Fig. 4.26. The dissipated power is measured using a YOKOGAWA WT1600 wattmeter, and the heat sink temperature is monitored with thermocouples.

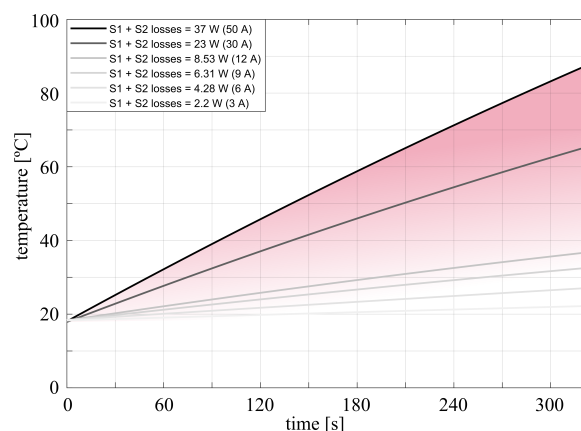


Figure 4.26: Temperature evolution of the heat sink with different input power values in the power MOSFETs S_1 and S_2, [95].

After obtaining the temperature evolution of the heat sink under fixed power losses, the push-pull converter is tested under two different operating conditions, defined as Test A and

Test B in Table 4.5. These conditions represent nominal operation scenarios for the intended application. Based on the converter's output power and voltage values, the current ripple (ΔI), the average current, and consequently the maximum and minimum currents (I_{max} and I_{min}) flowing through switches S_1 and S_2 can be determined. Once the turn-on and turn-off current values are identified, the switching energy can be estimated using the results obtained from the analytical models, as shown in Fig. 4.25. Consequently, the average switching losses can be calculated for a given switching frequency:

$$P_{\text{sw-S}} = f_{\text{sw}}(E_{\text{ON}} + E_{\text{OFF}}) \tag{4.22}$$

Simultaneously, the RMS current of each switch ($I_{\text{S-RMS}}$) is computed to estimate the conduction losses, which are obtained by multiplying the RMS current by the ON-state resistance. The ON-state resistance is extracted from the semiconductor datasheet at a junction temperature of 100 °C, providing a conservative estimate of conduction losses across the entire operating range. The total power loss in each switch is thus estimated as the sum of the switching losses and the conduction losses.

$$P_{\text{cond-S}} = I_{\text{RMS}}^2 R_{\text{DS(on)}} \tag{4.23}$$

Table 4.5: Operating conditions for the analysed push-pull converter and corresponding estimated switching losses using the developed model.

Parameter	*Test A*	*Test B*
Output power	300 W	320 W
Output voltage	200 V	100 V
Duty cycle	47%	21%
Current ripple (S pk-pk)	11.31 A	40.36 A
RMS current (S)	9.15 A	15.48 A
Turn on / off current (S)	7 A / 18 A	10 A / 50.36 A
Estimations with State space model		
Turn on / off energy (S)	5 µJ / 170 µJ	7 µJ / 750 µJ
Switching losses, $P_{\text{sw-S}}$	3.5 W	15.14 W
Conduction losses, $P_{\text{cond-S}}$	1 W	3.6 W
Total power losses (S_1 + S_2)	8.9 W	37.4 W

The heat sink's temperature evolution is monitored separately during both tests, and the resulting curves are plotted alongside the fixed power loss curves in Fig. 4.27. It can be observed that the heat sink reaches a temperature of 35 ° C after 5 minutes of operation under Test A conditions, and 60 ° C after 5 minutes under Test B conditions. As expected, the operating conditions of Test B (output regulation at 100 V) are significantly more demanding for the MOSFETs compared to Test A. The lower duty cycle in Test B results in a substantial increase in the average primary current ($I_{\text{pri(avg)}}$) and the turn-off current, leading to a significant rise in switching losses. Although conduction losses also increase, their rate of increase is comparatively lower.

From the temperature evolution of the heat sink during the experimental tests, it can be deduced that the total power losses of both MOSFETs at Test A conditions match with the 8.5 W losses scenario, while under Test B conditions the results are very similar (slightly higher) than 37 W scenario, as shown in Fig. 4.27. These results align closely with the estimations presented in Table 4.5 (8.9 W and 37.4 W for Test A and Test B conditions, respectively), with an error margin of around 5% for Test A and approximately 2% for Test B.

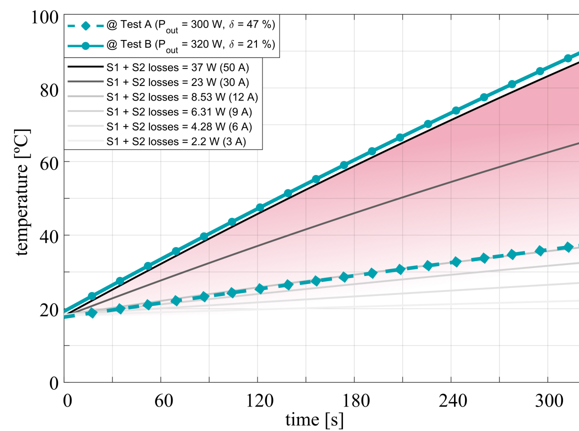


Figure 4.27: Temperature evolution of the heat sink with different input power values in the power MOSFETs S_1 and S_2, and during operation at test A and test B conditions specified in table 4.5, [95].

From these experiments, it can be observed that the majority of the MOSFETs' power losses occur during the turn-off transitions, mostly due to the high stray inductance present in the converter, highlighting the importance of external parasitic consideration when estimating the behaviour of power switches in Switch Mode Power Supplies (SMPS).

A thermal image of the converter operating under Test B conditions is shown in Fig. 4.28, where the heat sink, MOSFETs, rectifying diodes, and output inductor are visible.

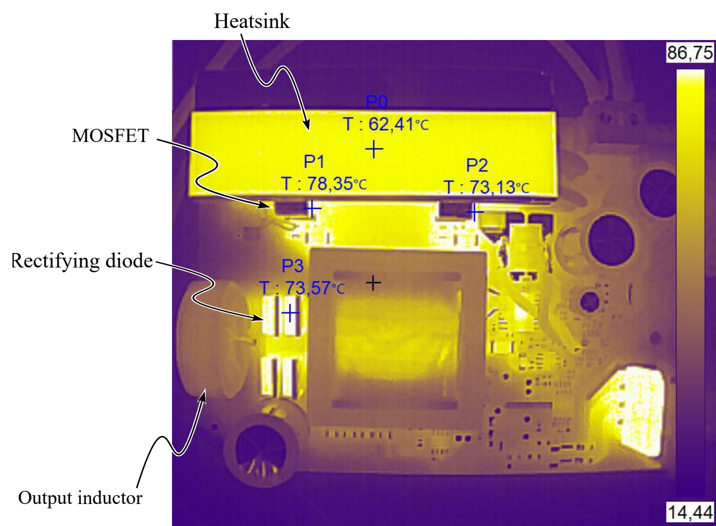


Figure 4.28: Thermal shot of the analysed push-pull converter during operation at Test B conditions, after 3 minutes. A black tape is attached to the heat sink to avoid reflection, [95].

The experimental results for both switching losses and overvoltage in the push-pull converter validate the effectiveness of the proposed method in predicting the behaviour of Silicon switches under the influence of parasitics, such as power loop inductance. The turn-off overvoltage was estimated under two different operating conditions, with an error of less than 15% in the peak voltage. Moreover, the predicted voltage and current transients closely match the measured waveforms during both the rising and falling edges, enabling an accurate estimation of the switching losses. Although some discrepancies are observed in the post-switching

oscillations, most likely caused by inaccuracies in the modelling of parasitic elements, these deviations have minimal impact on the overall accuracy of the model for the desired purposes. This is confirmed by the precise estimation of switching losses, which were indirectly validated using a calorimetric measurement approach. This validation process was based on Silicon switches; however, the knowledge obtained from this study has been employed to construct a GaN-based push-pull converter with very similar specifications, which is presented in this thesis, and the validation process is repeated to study the effectiveness of the presented model with novel GaN semiconductors.

4.4. Conclusions

In this chapter, an analytical model of a DPT is presented. The model consists of a theoretical half-bridge circuit, where both the high-side and low-side switches are built entirely from datasheet parameters. A current source emulates the inductor load. The modelling process begins with the construction of the power switch. Its output characteristics are described using polynomial equations similar to those found in SPICE models provided by some manufacturers. A correction factor is applied to compensate for potential inaccuracies during the extraction of datasheet information. Parasitic capacitances are also modeled, using fitted curves to represent their nonlinear behaviour. Slight adjustments are made in the case of C_{GS}, due to its dependency on gate-source voltage. Package-related parasitics, such as R_D, R_S, and L_S, are incorporated into the switch model. Parameters for ten different power switches are extracted and implemented, including both GaN and Si technologies. The half-bridge circuit is completed with parasitics representing the power loop and the gate-driving loop, such as L_{loop} and L_G. The full analytical model is simulated using MATLAB's ode23s solver, achieving high computational efficiency. The simulation time remains below five seconds for a full switching cycle under the defined conditions. This modelling approach requires only datasheet information, making it a universal and accessible method for characterizing modern power switches.

The influence of various parasitics on the switching behaviour of the half-bridge circuit is analysed. The relationship between switching dynamics and gate loop parameters is explored, showing that both the gate resistance R_G and the gate inductance L_G have a direct impact on switching speed. In particular, an optimal value of L_G can be identified, since excessively low inductance may lead to instability, while higher values can slow the transitions. Minimizing L_G is especially critical for devices that are sensitive to gate overvoltages, such as GaN SGTs. In addition to gate loop effects, the power loop inductance is found to play a key role in shaping the switching waveforms. It decouples the voltage and current slopes during turn-on, thereby reducing turn-on losses. However, during turn-off, it generates a voltage overshoot that increases energy dissipation and could cause device failure if not properly controlled. This effect becomes more pronounced in converter topologies with large parasitic inductance, such as push-pull architectures, and in fast-switching technologies like GaN. Another important contributor to the rise of switching losses is the common source inductance L_S, which influences both turn-on and turn-off behaviour. By coupling the gate-driving loop with the power loop, L_S slows down the switching transitions and increases total losses. This highlights the need to minimize or carefully design this inductance in high-performance switching applications.

Following the parasitic analysis, an experimental case study is presented to validate the estimations obtained with the analytical model. The case study focuses on a push-pull converter based on Silicon MOSFETs. First, the converter topology is thoroughly analysed in order to define the key current and voltage waveforms, as well as the parasitics required to accurately predict the switching behaviour. The leakage inductance of the high-frequency transformer is measured using a VNA and included in the model as the power loop inductance. The selected power semiconductors are modelled under nominal operating conditions to generate the corresponding current and voltage waveforms. These estimated waveforms are then compared with experimental measurements, showing strong agreement, particularly in the overvoltage caused by the transformer's leakage inductance during the turn-off transition. Although some discrepancies appear in the oscillations after the switches turn off, most likely due to minor inaccuracies in parasitic modelling, these differences have minimal impact on the overall accuracy of the model. The converter losses are indirectly measured using calorimetric tests

and compared with the estimated values. The results confirm that the proposed model can accurately predict both the switching behaviour and losses of Silicon power switches under the influence of parasitics such as power loop inductance. Finally, the case study in this chapter enabled the development of a GaN-based push-pull converter with similar specifications. This second converter is discussed in detail later in the document.

Chapter 5

POTENTIAL APPLICATIONS FOR GAN

Wide BandGap (WBG) semiconductors can significantly enhance the performance of modern power electronic systems. In the context of global efforts to reduce energy consumption and greenhouse gas emissions, WBG devices play a critical role in enabling more sustainable technologies. Their superior material properties, such as higher breakdown voltage, faster switching speeds, and improved thermal conductivity, translate into greater efficiency, reduced power losses, and increased power density. However, sustainability is not defined by efficiency alone. Factors such as cost, volume, reliability, and integration complexity are equally important. By reducing the size and weight of passive components, minimizing cooling requirements, and enabling simpler converter topologies, WBG semiconductors can lower the overall system footprint and life-cycle costs. These advantages enhance the competitiveness of power electronics across a wide range of applications, from electric vehicles and renewable energy systems to industrial drives and data centers. In summary, the adoption of WBG devices contributes not only to performance improvement but also to achieving long-term environmental and economic sustainability. Currently, Gallium Nitride (GaN) devices are being increasingly adopted in low-voltage applications (typically below 1200 V), while Silicon Carbide (SiC) technology is gaining traction in medium- and high-voltage systems such as three-phase motor drives. Each application must be carefully analysed to ensure the correct integration of WBG devices and to fully exploit their advantages.

A particularly promising field for WBG adoption is lift (elevator) systems, where high performance, reliability, and energy efficiency are critical. Traditionally, elevator power electronics have relied on silicon-based power converters, using Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and Insulated Gate Bipolar Transistor (IGBT) technology, which, despite their maturity, are constrained by switching speed and thermal limitations. WBG devices, by contrast, offer the potential for significant improvements in switching efficiency, power density, and thermal management, ultimately enabling more compact and cost-effective solutions.

5.1. Lift Application

Lift applications significantly improve accessibility within buildings, enabling the vertical transportation of both people and heavy goods across multiple floors. These systems typically rely on an electric motor to drive the cabin, which houses the passengers or cargo. In addition to the main traction system, lifts incorporate several power electronic conversion stages, such as DC/DC, AC/DC, and DC/AC converters, that have traditionally been implemented using Silicon-based transistors. However, recent advancements suggest that these stages can be more efficiently handled using GaN or SiC devices, depending on the voltage and power requirements of the system.

The energy impact and efficiency of elevator systems in Europe have been studied extensively in [97] and [98]. Based on data from the INTELLIGENT ENERGY EUROPE project, finished in 2013, the studies revealed that the total annual energy consumption of elevators amounted to approximately 18.4 TWh, with standby operation alone accounting for about 4.5 TWh per year. Notably, this standby consumption represented 68% of the total standby energy use in the tertiary (services) sector. Two prospective scenarios were evaluated to estimate potential energy savings. The first involved retrofitting elevator systems with Best Available Technologies (BAT) that were already commercially available at the time of the study (2010–2012). The second scenario considered the deployment of Best Not-yet-Available Technologies (BNAT), representing innovative solutions not yet on the market but expected to deliver superior performance. The study concluded that energy savings of up to 11.5 TWh per year (representing 62%) could be achieved by implementing BAT, while savings could reach 13.6 TWh per year (74%) with the adoption of BNAT. These comparisons highlight the substantial opportunity for energy savings and system optimization in elevator applications, an opportunity that can be further amplified by the integration of WBG-based power electronics.

It is important to contextualize these results by considering the publication dates of the studies, which date back over a decade. Since then, the field of elevator technology and power electronics has evolved significantly, with continuous improvements in efficiency, control, and component integration. Nonetheless, the conclusions remain valuable as indicative benchmarks for assessing current elevator systems. Today's WBG semiconductor technologies make it feasible not only to realize the improvements outlined in the BAT and BNAT scenarios, but potentially to exceed them. In addition to energy efficiency, WBG devices enable substantial reductions in system size and weight, as well as improved thermal management, factors that should also be taken into account when evaluating the next generation lift systems.

Naturally, various elevator configurations exist on the market today, each tailored to specific applications and performance requirements. These configurations differ in their electrical circuitry and arrangement of electronic subsystems. Analysing every possible architecture would be a limitless task; therefore, to define the scope, a Machine Room-Less (MRL) electric elevator has been selected for further analysis. This configuration is the most widespread among the systems offered by the manufacturer under consideration. A simplified electrical diagram of the selected configuration is shown in Fig. 5.1. In this type of elevator, the traction motor is mounted directly above the cabin, eliminating the need for a separate machine room. The main components include the car or cabin that transports passengers within a vertical shaft, the three-phase AC grid connection, the energy management system (typically integrated with the central control unit), the traction drive responsible for motor control, the door drive mechanism for opening and closing operations, the braking system, and various auxiliary elements.

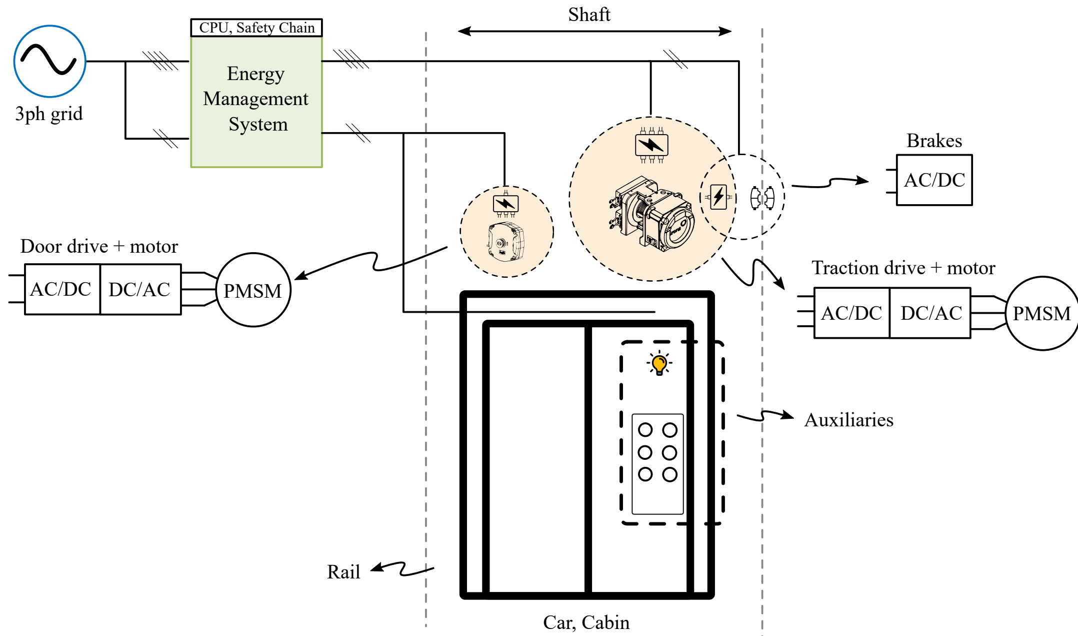


Figure 5.1: Visual representation of the simplified electric circuit and electronic components in a lift application.

Following the diagram, the main power electronic units and components of a machine room-less elevator are listed and described below.

5.1.1. Drives and brakes

The traction motor drive is the primary control unit of the elevator, responsible for actuating the motor to move the cabin up and down. Nowadays, most of the installed motors in elevators are gearless Permanent Magnet Synchronous Machine (PMSM), and their actuation is done with a rectifier and a Voltage Source Inverter (VSI) as shown in Fig. 5.2.

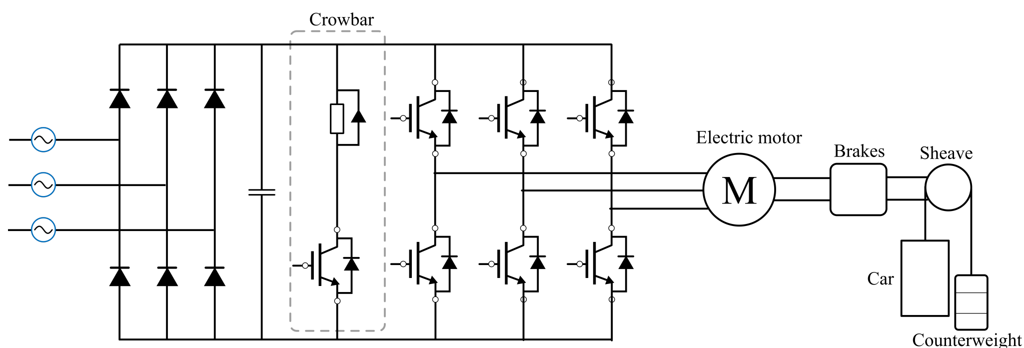


Figure 5.2: Modern gear-less electric drive for an elevator, [99].

The three-phase grid serves as the main power supply for the drive, which typically includes a Electromagentic Interference (EMI) filter at its input. Within the drive, a passive rectifier,

commonly a three-phase diode bridge, converts the AC input into a DC voltage. The resulting DC-link voltage approximately corresponds to the peak of the three-phase line voltage. The inverter stage (DC/AC) then converts this DC voltage into a pulse-width modulated AC output to drive the motor. The amplitude and frequency of the three-phase output are regulated by the inverter switches, typically arranged in a three-phase VSI configuration using IGBTs. These IGBTs usually operate at switching frequencies between 2 and 16 kHz. The total converter power typically ranges from 1 kW to 15 kW, depending on the elevator load and nominal speed, which can correspond to capacities of up to 12–15 passengers and 1 m/s speed. The Diode Front End (DFE) rectifier is typically connected to the grid through an L or LC filter.

Depending on the direction of elevator movement, the load, and the counterweight, the electric motor may operate as a generator, feeding energy back into the system. In such cases, the inverter functions bidirectionally, returning power to the DC-link. However, with a conventional DFE rectifier, this energy cannot be transferred back to the grid due to the unidirectional nature of the diode bridge. As a result, a crowbar circuit is typically required to dissipate the excess energy and maintain the DC-link voltage within safe limits. Recovering this otherwise wasted energy is a key aspect of future strategies aimed at improving system efficiency. One such approach is the use of a regenerative drive system, which replaces the passive diode bridge with a Active Front End (AFE) composed of controllable switches. This allows surplus energy to be fed back into the grid, eliminating the need for a crowbar, as illustrated in Fig. 5.3.

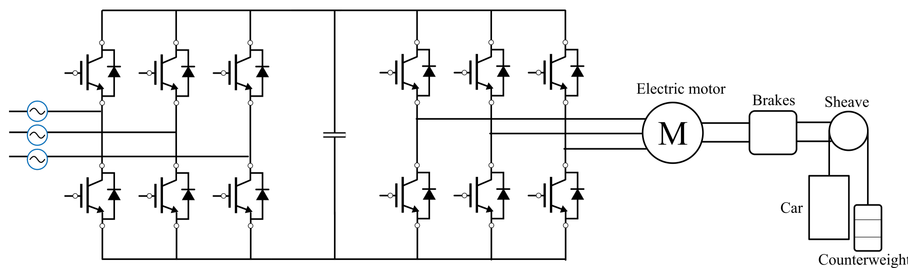


Figure 5.3: Modern regenerative gearless electric drive for an elevator.

This regenerative drive has six more active switches than the first solution (Fig. 5.2), and offers completely bidirectional operation. Currently, Silicon IGBTs are being used in this type of drive due to the required voltage and current levels.

Brakes

The brake of the elevator is a safety device based on an electromechanical system within the machine that is capable of stopping the car in case of an emergency stop. The simplest electronic interface for the electromechanical brakes is formed with a diode bridge rectifier, and the rectified output is directly connected to the brake actuator (electromagnet), requiring very few components. However, more and more MOSFETs are being introduced in the circuit in series with the electromagnet to control the current flow and reduce the consumption. In this way, different brakes can be controlled individually. For safety reasons, the brake is a normally closed (NC) mechanism, that is, it requires to be fed to be opened, allowing the cabin movement. Thus, if current is conducted through the inductance, the brake is open and the movement of the cabin is allowed. On the contrary, when the supply is interrupted (usually at AC stage employing AC relays), the brake is triggered, stopping the cabin.

Door drive

The elevator door system incorporates a conversion topology similar to that of the main traction drive. It consists of a single-phase diode bridge, a capacitive DC-link, and a three-phase voltage source inverter (VSI) that supplies a Permanent Magnet Synchronous Machine (PMSM) responsible for driving the doors. Unlike the main drive, the Door Operator Drive (DOD) is typically powered from a single-phase grid, as its power demand is significantly lower, limited to a few hundred watts, with the DC-link voltage charged to approximately 325 V.

This electric drive typically delivers between 50 and 110 V (RMS) and around 150 W to the motor, which usually operates at a nominal speed of 500 to 600 rpm. The PMSM generally includes 5 to 10 pole pairs [99]. The inverter employs IGBTs, resulting in a switching frequency typically limited to below 20 kHz.

5.1.2. Energy Management System

The Energy Management System (EMS) is responsible for managing the energy that flows through the different components within the elevator. The system is composed of the Energy Management Node (EMN), the Manual Rescue Node (MRN), and an auxiliary 24 V battery.

Energy Management Node

In normal working conditions, the elevator's electric system is supplied by the three-phase grid as shown in Fig. 5.4 through an input EMI filter. The Energy Management Node is responsible for monitoring the proper operation of the grid and managing the electronics in the elevator system in case it detects a grid fault. The EMN includes a phase fault detection system to sense if all three phases are working correctly. However, the EMN only needs one of those phases to work, the same which provides electricity to the Safety Chain, the door operator, and the brakes. This single phase is monitored independently inside the node for safety reasons. The single-phase supplies the AC/DC voltage source that provides 24 V to feed the essential elements as the master CPU, the teleservice, and the emergency lighting, which must stay ON during a faulty situation at least for a certain amount of time (typically around 1 hour).

24 V is achieved with an AC/DC step-down power converter, typically a full-bridge diode rectifier with a DC/DC converter. The converter has a power rating of 60 to 90 W. One of the main purposes of the EMN is to respond to a fault or an anomaly in the main power supply (single-phase or three-phase), following the instructions commanded by the master CPU. In case an anomaly occurs to the 24 V power supply, another energy source is used to supply that DC voltage. This voltage is usually provided by a 24 V NiMH battery pack, which is kept charged by an AC/DC converter included in the EMN, with a typical power rating of 15 W. This NiMH battery is externally connected to the EMN board, as depicted in Fig. 5.4.

The AC/DC battery charger consists of a full-bridge rectifier followed by a DC/DC converter that steps down the voltage. In this configuration, the DC/DC stage operates with MOSFETs at a switching frequency between 50 and 100 kHz, delivering a variable DC voltage to charge the battery using a constant current–constant voltage (CC-CV) strategy. In the event of a fault or an anomaly such as the one previously described, passengers may become trapped inside the elevator cabin. To address this, regulations require the presence of a rescue system capable of evacuating passengers, which can be either manual or autonomous.

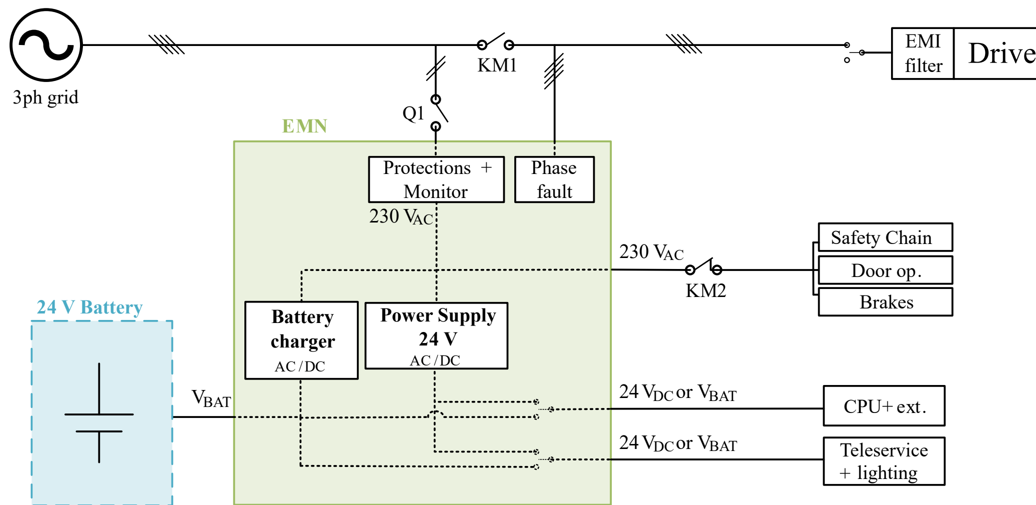


Figure 5.4: Energy management system diagram including the main three-phase grid, the Energy Management Node, and the Battery Pack. The EMN shows the internal battery charger.

Manual Rescue Node (MRN)

During a rescue operation, the elevator operator must follow a specific sequence to move the cabin and evacuate the passengers. The previously mentioned 24 V battery serves as the energy source to release the brakes and power the main drive, allowing the cabin to move, typically toward the nearest floor requiring the least energy. However, 24 V is insufficient to supply either the main drive or the brakes directly. Therefore, a DC/DC step-up converter is required to boost the voltage. The brake system demands an initial peak of 200 V to release and a sustained 100 V to remain open. As for the main drive, its minimum operating DC-link voltage depends on the motor size, but in most cases, it can be powered by the same 100 V used to hold the brakes open, as illustrated in Fig. 5.5.

MOSFETs are normally used for the primary side switches. Depending on the size of the main drive, the DC/DC is designed for different rated powers, which usually range between 300 W to 500 W.

When an anomaly affects the main power supply, battery charging is interrupted. Therefore, the battery must store enough energy to enable at least one strategic cabin movement, typically to the nearest floor, to safely evacuate the passengers. The drive must also be properly configured to avoid tripping due to a low DC bus voltage and to allow cabin movement under these conditions. Unlike the brakes, which are consistently powered by the 24 V battery via a DC/DC converter, the main drive may be supplied by an Uninterrupted Power Supply (UPS) connected in parallel with the Manual Rescue Network (MRN), particularly when the 24 V battery alone is insufficient.

Autonomous rescue system (ARS)

Unlike manual rescue systems, autonomous rescue systems do not require external personnel; the elevator's CPU manages the operation to safely evacuate passengers. Their installation is not mandatory under current European regulations and is typically offered as an optional feature. This system includes an additional UPS that provides 230 V (RMS) to power the door

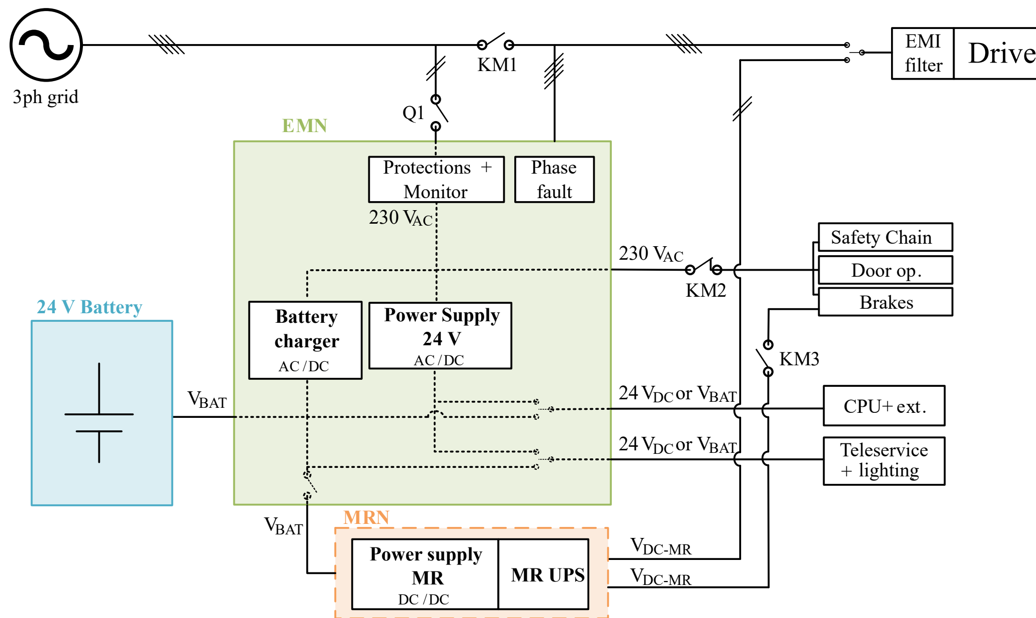


Figure 5.5: Energy management system diagram including the main three-phase grid, the Energy Management Node, the Battery Pack, and the Manual Rescue Node. The MRN shows the internal DC/DC power supply and the UPS.

mechanism, safety circuits, and brakes. The total power demand depends on the elevator's size and the consumption of these subsystems, so the UPS is dimensioned accordingly, typically ranging from 500 W to 5 kW.

5.1.3. Renewable energies and storage systems integration

Elevator modernization efforts increasingly focus on enhancing energy efficiency and reducing emissions. The integration of Renewable Energy Sources (RES) and Energy Storage System (ESS) is gaining traction in the development of next-generation elevators, with their adoption expected to grow in the coming years. To enable this integration, both the electrical and electronic architectures must be adapted, and various implementation strategies can be considered. Some manufacturers in the elevator sector are already working on solutions that combine renewable energy sources (RES) and energy storage systems (ESS). One of these manufacturers, specialised in isolated DC/DC converters, is Epic Power, [100], which offers a wide range of output power and voltage regulation options.

Microinverters for photovoltaic integration

To integrate photovoltaic (PV) panels into a conventional elevator system with minimal invasiveness, microinverters present a suitable solution. These converters enable the connection of individual panels externally, without requiring modifications to the existing system architecture.

Microinverters are DC/AC converters that transform the DC output of the solar panels into AC power, which can be directly injected into the single-phase grid. As such, they offer

an almost non-invasive method for incorporating renewable energy sources into any grid-connected application. A typical microinverter consists of a DC/DC stage, which regulates the power flow and maximizes PV output through an Maximum Power Point Tracking strategy (MPPT) algorithm, followed by a DC/AC stage that generates an AC voltage synchronized with the grid. Different conversion topologies can be implemented, although nowadays a flyback topology is preferred for the DC/DC stage in low-power applications, due to its cost-effective ratio. However, different topologies such as resonant converters or full bridges can also be found in the current market, [101].

ESS and RES integration solution (Energy Hub)

An approach for integrating both ESS and RES into the elevator system is the Energy Hub solution. This solution is a combination of various conversion stages to achieve the required functionalities for the adoption of ESS and RES. The schematic in Fig. 5.6 shows the *Energy Hub*.

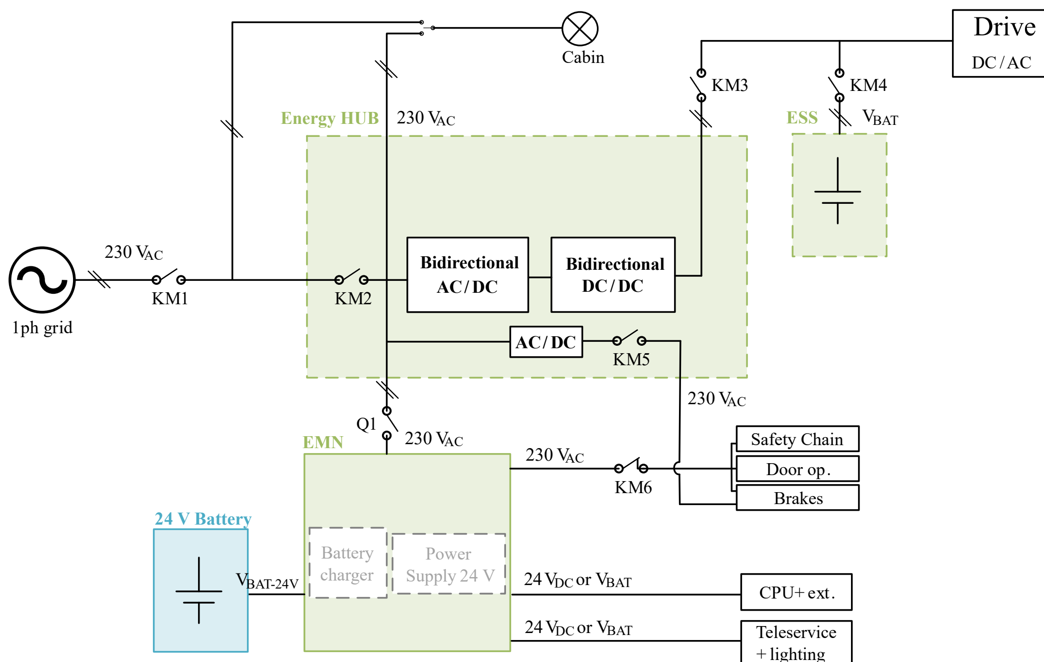


Figure 5.6: Energy Hub solution diagram including possible connections between ESS, Grid, and Load

The *Energy Hub* comprises two bidirectional power stages, which can manage the energy and power consumption more efficiently with the help of an ESS. On the one hand, the solution enables saving the elevator-regenerated energy in the ESS, reducing the energy demand from the grid. The power demand can also be reduced as the solution can provide the highest power peaks from the ESS. On the other hand, the utilization of the ESS can provide backup energy to the whole elevator system under grid fault situations, through the bidirectional converter stages. Furthermore, these converter stages allow the system to be supported with energy from PV panels, with the help of the microinverter or dedicated DC/DC converter. This power converter allows for reducing the overall consumption of the elevator moving energy in both

directions, considerably minimizing the power consumption from the grid and optimizing the use of ESS and RES.

5.1.4. Summary and new opportunities with WBG

In summary, this section has reviewed the key components and power electronic architectures commonly found in modern elevator systems, highlighting their functionalities, energy requirements, and potential for renewable integration. This summary serves as a reference for analysing the various opportunities for integrating WBG semiconductors. Table 5.1 lists the previously identified power converters, detailing their power conversion stages, associated power levels, and the types of semiconductors employed.

Table 5.1: Elevator systems current and near future power electronics.

Component	Conversion stages	Power level	Semiconductor type
Drive: traction motor (NR)	AC/DC & DC/AC (3ph)	1 kW to 15 kW	Diodes & IGBTs
Drive: traction motor (R)	AC/DC & DC/AC (bi-3ph)	1 kW to 15 kW	IGBTs
Drive: Door operator	AC/DC & DC/AC (1ph/3ph)	100 W to 150 W	Diodes & IGBTs
Brake	AC/DC	50 W to 100 W	Diodes
EMN PS	AC/DC & DC/DC(1ph)	60 W to 90 W	Diodes & MOSFETs
EMN charger	AC/DC & DC/DC (1ph)	15 W	Diodes & MOSFETs
MRN	DC/DC (1ph)	300 W to 500 W	Diodes & MOSFETs
Automatic Rescue System (ARS)	AC/DC & DC/AC (3ph)	500 W to 5 kW	Diodes & MOSFETs/IGBTs
Microinverters	DC/DC & DC/AC (1ph)	250 W to 1 kW	Diodes & MOSFETs
Energy Hub	AC/DC & DC/DC (bi-1ph)	1 kW to 2 kW	MOSFETs

<NR> stands for Non-Regenerative; <R> stands for Regenerative; <bi> stands for bidirectional; <1ph> stands for single phase; <3ph> stands for three phase

Within the elevator's power electronics architecture, the most power-demanding converter is the one driving the main traction motor, typically rated between 1 kW and 15 kW to support elevator capacities of up to 12–15 passengers. These drives are conventionally based on Silicon IGBTs operating at switching frequencies below 20 kHz. The next most powerful subsystem is the commercial UPS, which is optional and not always installed. Most of the remaining converters operate below 1 kW and are used in auxiliary systems such as door drives, brake controls, and control units, Fig. 5.7.

The main drive is a promising candidate for the integration of SiC MOSFETs, given their suitability for higher voltage and power levels. Their use could improve efficiency, thermal performance, and enable the reduction of output filters, leading to a more compact and lightweight design. However, the significantly higher cost of SiC devices compared to Silicon IGBTs may limit their commercial viability in this application unless cost-performance trade-offs can be justified. In contrast, the rest of the power electronic subsystems present an ideal scenario for GaN-based devices. Their superior switching performance and high power density could lead to notable improvements not only in size, volume, and cost but also in functional integration. This could enable the consolidation of multiple converters into a single, multifunctional unit, thereby simplifying the system architecture.

Based on this analysis, the development of a dedicated DC/DC converter in the 300–500

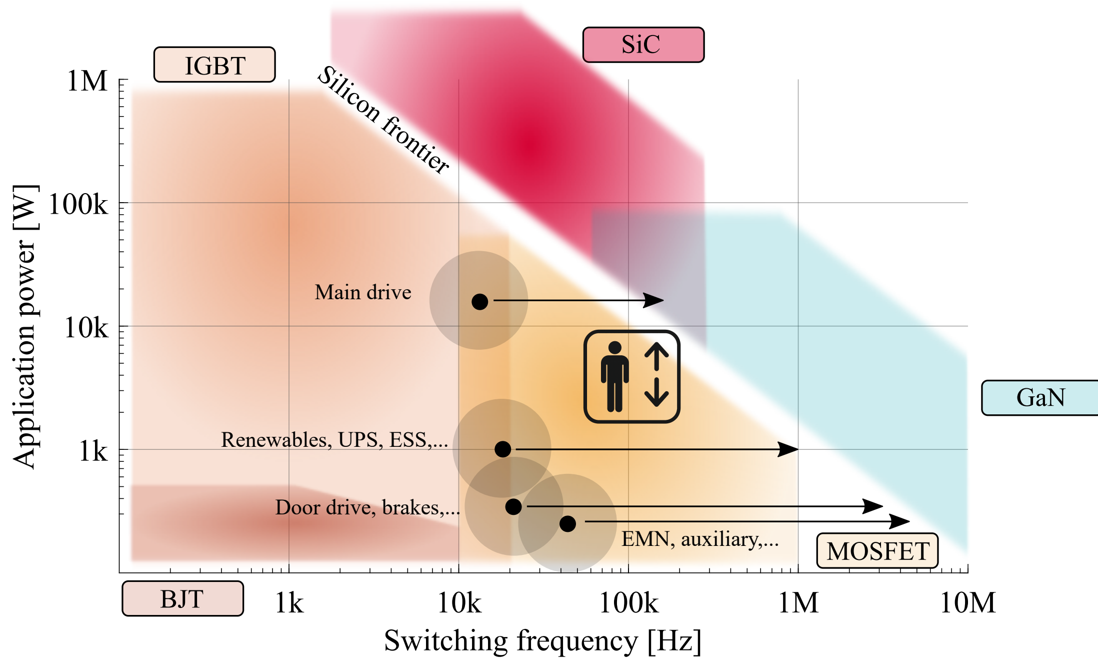


Figure 5.7: Application range and scope for wide-bandgap materials, focusing on lift application.

W range emerges as a particularly promising opportunity, especially for applications such as brake control, auxiliary supplies, and integration with energy storage or renewable sources. Specifically, for the Manual Rescue Network (MRN), improving converter performance could unlock new possibilities for system simplification and application merging. Integrating WBG semiconductors at this stage could yield significant advances. To accelerate the design of such converters, the selection of the optimal topology can be discussed, and multi-objective optimization methods (e.g., Pareto optimization) can be employed to simultaneously balance efficiency, cost, reliability, and power density. These approaches have been widely studied in the literature and offer a systematic way to identify optimal trade-offs in converter design [102], [103], [104].

5.2. Case Study: Low Power DC/DC Application

The lift system under study includes a low-power (< 500 W) isolated DC/DC converter used in the MRN application. A 24 V nominal NiMH battery powers this step-up converter and generates an output voltage ranging from 100 V to 200 V. While the nominal power is 300 W, it can reach up to 450 W depending on the load conditions. The main specifications of the converter are summarized in Table 5.2.

Table 5.2: Requirements for the low power DC/DC application

Parameter	Symbol	Value
Input voltage	V_{in}	20 V ... **24** V ... 28 V
Output voltage	V_{out}	100 V ... **200 V**
Output power	P_{out}	**300 W** ... 450 W
Maximum input current ripple	ΔI_{in}	$<$ **70%** of I_{pri}
Maximum output current ripple	ΔI_{out}	$<$ **70%** of I_{sec}
Maximum input voltage ripple	ΔV_{in}	$<$ **2%** of V_{in}
Maximum output voltage ripple	ΔV_{out}	$<$ **2%** of V_{out}

The baseline converter, which is currently used in the reference lift application, is used to validate the presented model in Chapter 3. GaN technology is introduced as a promising alternative to replace the existing Silicon-based MOSFETs. The current design has been critically evaluated and redesigned, beginning with a comparative study of multiple converter topologies to identify the most appropriate candidates.

Four power converter topologies, along with their main variants, are described. For each topology, both primary and secondary side components are analysed, with particular attention given to the operating mode of the high-frequency transformer and the minimum component count required for implementation. The analysis emphasizes the primary side, while the secondary is considered passive for simplicity. However, more complex secondary-side configurations will be addressed in future work. The section concludes with a comparative Table summarizing the main characteristics of each topology variant [96].

Flyback

The flyback topology is one of the most widely used isolated DC/DC converter architectures for low-power applications. Below the 100 W power range, it offers a simpler and more cost-effective design compared to other topologies. Consequently, it is commonly employed in commercial low-power products, such as mobile phone chargers rated up to 100 W [105]. However, reference designs are also available for power levels up to 200 W [106].

The standard flyback converter diagram is shown in Fig. 5.8. This topology consists of an active switch on the primary side S_1, a high-frequency transformer, and a diode on the secondary side for rectification, D_1. Input and output voltages are typically filtered using bulk capacitors. When the primary switch is turned on, the magnetising inductance (L_m) stores energy by building up a magnetic field in the transformer core. When turning the switch off, this stored energy is transferred to the secondary side and rectified through the diode. During the switch-off transition, the transformer's leakage inductance induces a voltage spike across the main switch, which can be suppressed using clamping circuits, either active or passive. In the example shown, the clamping network consists of an auxiliary switch S_2 and a capacitor. The clamping circuit can provide the switch with Zero-Current-Switching (ZCS) or Zero-Voltage-Switching (ZVS) conditions, improving the converter's performance. As

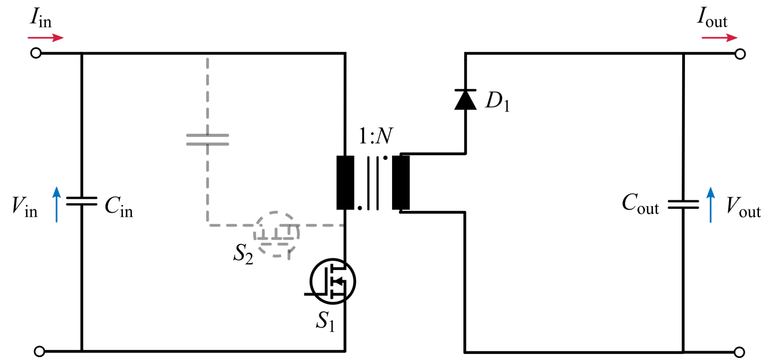


Figure 5.8: Flyback converter, consisting of input capacitor C_{in}, one primary switch S_1, transformer, rectification diode D_1, and output capacitor C_{out}, [96]. Dashed lines indicate an optional clamping circuit.

the output power increases, a larger transformer core is needed to store the required energy, potentially leading to reduced efficiency.

Forward

The Forward converter is derived from the non-isolated buck topology and is illustrated in Fig. 5.9. Its primary side consists of a single switch and a diode. Unlike the flyback converter, the transformer includes two primary windings: one for power transfer and another for core demagnetization. The power-transfer winding is connected in series with the main switch, while the demagnetizing winding is connected with a diode to reset the core. During the ON state of the switch, energy is directly transferred to the secondary side. During the OFF state, the output inductor continues to supply the load with the stored energy, while the residual magnetic flux in the core induces a negative voltage across the primary winding. This negative voltage forward-biases the reset diode (D_1 in the figure), allowing the core to discharge. Compared to the flyback topology, the forward converter utilizes the transformer core more efficiently since it does not rely on energy storage within the core but instead transfers it directly. However, the core is still magnetized with a single polarity. Forward converters are typically used in applications with power levels up to 150 W [107].

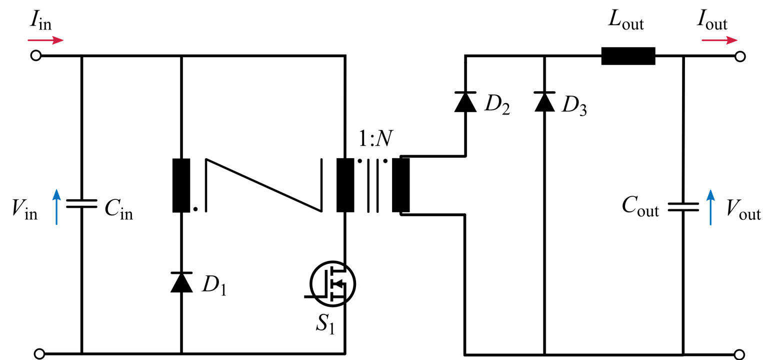


Figure 5.9: Forward converter, consisting of input capacitor C_{in}, one primary switch S_1 with series connected winding n_1, one primary diode D_1 with series connected demagnetizing winding n_2, transformer, rectification diodes D_2 and D_3, output inductor L_{out}, and output capacitor C_{out}, [96].

Similar to the flyback topology, the forward converter can be adapted to operate under ZVS conditions. This is typically achieved by incorporating an active clamp on the primary side,

consisting of a capacitor and either an active switch or a diode. The active clamp significantly reduces switching losses, leading to higher efficiency compared to the conventional forward converter. Moreover, this approach eliminates the need for a dedicated demagnetizing winding on the transformer [108]. Another variation is the two-transistor forward converter, in which the primary side includes two switches and two diodes. This configuration also eliminates the need for a demagnetizing winding. During the ON state, both transistors conduct simultaneously to energize the transformer, while the diodes facilitate core demagnetization during the OFF state. An added benefit of this topology is that each transistor only needs to block half of the input voltage, allowing for improved conduction and switching performance. Two-transistor forward converters are typically used in designs up to 300 W [107], while single-switch forward converters are more common in lower-power applications, typically up to 200 W [109].

Push-pull

The push-pull converter, derived from the forward topology, features two switches on the primary side arranged in a symmetrical configuration. This is the topology currently used in the MRN application. The transformer has a center-tapped primary winding, with the center connected to the input voltage and each end connected in series with one of the two switches. As a result, the two primary windings are wound in opposite directions to allow bidirectional magnetization of the core, as shown in Fig. 5.10. Similar to the forward converter, the secondary side can be implemented using either a center-tapped winding with two diodes or a single-ended winding with a full-wave rectifier composed of four diodes.

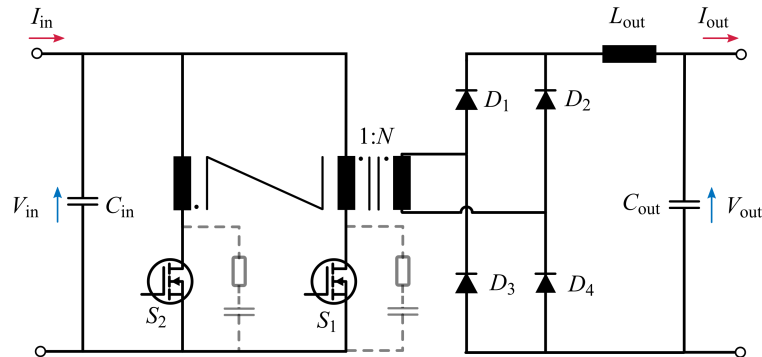


Figure 5.10: Push-pull converter, consisting of input capacitor C_{in}, one primary switch S_1 with series connected winding n_1, one primary diode D_1 with series connected primary winding n_2, transformer, rectification diodes D_1, D_1, D_3, and D_4, output inductor L_{out} and output capacitor C_{out}, [96]. Dashed lines indicate optional snubber circuits.

In a push-pull converter, the two transistors operate alternately and must never conduct simultaneously. When one switch turns ON, energy is transferred to the secondary side, and the transformer core is magnetized. During this period, the voltage applied to one half of the primary winding is reflected onto the other half, causing the drain-source voltage of the OFF transistor to rise to approximately $2V_{in}$. When the conducting switch turns OFF, the core is demagnetized via the secondary winding. In the second half of the switching cycle, the other transistor turns ON, repeating the process with the magnetic flux oriented in the opposite direction. Due to the series connection of the windings with the switches, the transformer's leakage inductance generates voltage spikes during switching transitions. Consequently, the transistors must withstand voltage stresses of at least $2V_{in}$ plus the overvoltage spike. For this

reason, push-pull converters are typically used in low-voltage applications, with power ratings up to 500 W [107].

A critical risk in push-pull operation is the simultaneous conduction of both switches, which generates equal and opposite fluxes in the transformer, effectively creating a short-circuit path from the input source to ground through the transformer's center-tap. To prevent shoot-through, an input-side inductor is often added between the DC source and the center-tap of the transformer. This modification results in a current-fed push-pull configuration, which also eliminates the need for a large input capacitor.

Various techniques similar to those used in flyback and forward converters can be applied to reduce switching losses. For example, an active clamp circuit can be implemented by adding a switch and a capacitor [110]. More recently, a promising variant has been proposed in the literature that achieves ZVS by forming a resonant tank on the primary side using a single capacitor in the current-fed push-pull topology [111].

Half-bridge

The half-bridge converter features two switches connected in series on the primary side. The midpoint between the two transistors is connected to one end of the transformer's primary winding, while the other end is tied to the midpoint of the input DC bus. This midpoint is established using two identical capacitors connected in series across the input voltage. With this configuration, when the upper switch is ON, half of the input voltage $(+V_{in}/2)$ is applied across the transformer primary. Conversely, when the lower switch is ON, the opposite polarity $(-V_{in}/2)$ is applied. The basic half-bridge topology, therefore, comprises a single primary winding, two active switches, and two bus capacitors that serve to split the input voltage and provide a stable virtual ground. The secondary side can be implemented either with a center-tapped winding and two rectifier diodes, or with a single winding and a full-wave rectifier composed of four diodes, as illustrated in Fig. 5.11.

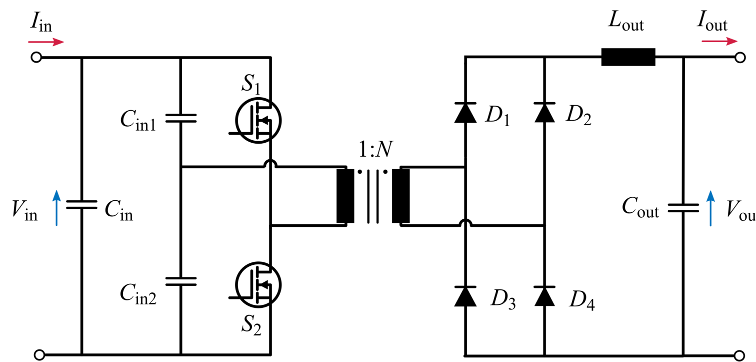


Figure 5.11: Half-bridge converter, consisting of input capacitors C_{in1} and C_{in2} in series, two primary switches S_1 and S_2 in half-bridge configuration, transformer, rectification diodes D_1, D_2, D_3, and D_4, output inductor L_{out} and output capacitor C_{out}, [96].

Using a single primary winding simplifies the half-bridge design compared to the push-pull topology and significantly reduces the transformer's leakage inductance. However, like the push-pull converter, the half-bridge is also susceptible to magnetic flux imbalance in the core, which can lead to saturation over time. To mitigate this, current-mode control is often employed. Unlike the push-pull configuration, only half of the input voltage is applied across the transformer primary during each switching interval. As a result, each switch must handle approximately twice the primary current to deliver the same output power as an

equivalent push-pull converter. One of the most widely adopted variants of this topology is the resonant half-bridge, encompassing a broad family of configurations. By introducing resonant elements on the primary side, soft switching (such as Zero Voltage Switching) can be achieved, significantly reducing switching losses. Each resonant topology has its advantages and trade-offs [96], but the LLC resonant converter stands out due to its excellent efficiency, compactness, and adaptability across a wide operating range. Moreover, both the transformer's leakage inductance and magnetizing inductance can be utilized as part of the resonant tank, reducing the number of external passive components required.

Topology comparison for the case study

Following the general description of different topologies for isolated DC/DC converters, the main characteristics are listed in the Table 5.3.

Table 5.3: Possible topologies list and their main characteristics for low-voltage DC/DC application

DC/DC topology		A. s.	Tr. w.	P. e.	SS/HS
Flyback	Standard	1	1:1	2	HS
	Quasi-reso.	1	1:1	3	QSS
	Active clamp	2	1:1	3	SS
Forward	Standard	1	2:1	3	HS
	Active clamp	2	1:1	4	SS
	2 switch	2	2:1	3	HS
Push-pull	Standard	2	2:2	3	HS
	Current fed reso.	2	2:2	3	SS
Half-bridge	Standard	2	1:2	3-5	HS
	Reso. LLC	2	1:2	3-5	SS

<A. s.> stands for active semiconductors in the primary side; <Tr. w.> for transformer's primary and secondary winding numbers; <P. e.> for passive elements; <SS> for soft switching; <HS> for hard switching.

Given the power level required by the application under analysis, single-switch topologies have been ruled out of the list. These architectures rely on a single switch to handle all the power and make poor use of the transformer, which limits both power density and output capacity. Among the two-switch topologies, the push-pull converter offers a promising balance between simplicity and performance, with typical power ratings well aligned with the application's requirements. Furthermore, the fact that the system demands a step-up conversion makes the push-pull topology particularly attractive when compared to the half-bridge configuration. In a push-pull converter, the two primary switches operate complementarily. Their parallel arrangement, combined with a center-tapped transformer, enables the generation of a bipolar square wave (as seen from the transformer) with the full input voltage amplitude. This allows the effective duty cycle (the proportion of the period during which voltage is applied to the transformer) to extend up to 1. In contrast, the half-bridge topology uses two switches in series and splits the input voltage via two bus capacitors. As a result, only half of the input voltage is applied to the transformer at any given time, yielding a maximum effective duty cycle of 0.5. This key difference significantly impacts the RMS current in the primary winding: for the same output power, the half-bridge converter experiences approximately twice the RMS primary current compared to the push-pull configuration. Consequently, conduction losses can be up to four times greater in the half-bridge topology for a given primary-side resistance. It is worth noting, however, that the lower voltage stress on each switch in the half-bridge topology can lead to reduced switching losses. Both topologies have been analysed in detail,

with optimal semiconductor selections explored for each case. As a result, two converter prototypes have been developed for experimental comparison.

5.3. Push-pull Converter Design

After comparing the different topologies, the push-pull converter introduced in Chapter 4 is redesigned using GaN-based switches. Implementing a GaN-based step-up push-pull converter allows for a fair comparison between Silicon and GaN technologies under identical operating conditions. The original work was presented in [112], and in this study, several values have been updated as of June 2025.

As previously discussed, the converter is powered by a 24 V nominal NiMH battery and is designed to generate an output voltage ranging from 100 V to 200 V. Although the nominal power is 300 W, the application may demand peak power levels of up to 450 W, depending on load conditions. Based on these requirements, the main specifications of the GaN-based push-pull converter are summarized in Table 5.4. To facilitate the initial design phase, the specification range has been slightly constrained. The output voltage is regulated by adjusting the duty cycle according to the relationship $V_{out} = 2\delta N V_{in}$, where δ is the duty cycle and N the turns ratio. The switching frequency is set between 200 kHz and 500 kHz; the lower limit ensures that the maximum flux density in the transformer is not exceeded with a single primary turn, while the capabilities of available commercial controller ICs constrain the upper limit.

Table 5.4: Requirements for the designed GaN-based step-up push-pull converter

Parameter	Symbol	Value
Input voltage	V_{in}	**24 V**
Output voltage	V_{out}	197 V ... **230 V**
Output power	P_{out}	**300 W**
Maximum input current ripple	ΔI_{in}	$<$ 70% of I_{pri}
Maximum output current ripple	ΔI_{out}	$<$ 70% of I_{sec}
Maximum input voltage ripple	ΔV_{in}	$<$ 2% of V_{in}
Maximum output voltage ripple	ΔV_{out}	$<$ 2% of V_{out}
Switching frequency	f_{sw}	200 - 500 kHz

In this design, three key aspects are prioritized: efficiency, volume, and cost. Each major component, particularly the power switches, is analysed to assess these indicators. Based on the application requirements, the passive elements, including the input/output capacitors and output inductor, are dimensioned within the targeted switching frequency range, while the high-frequency transformer is designed to meet the required voltage conversion ratio. For the GaN-based push-pull converter, minimising leakage inductance is identified as critical, leading to the selection of a planar transformer with a single primary turn. Once the electrical conditions are defined, various semiconductor switches are evaluated using the developed modelling tool in Chapter 3 to estimate power losses and switching behaviour. With these inputs, a design optimisation is performed to select the most suitable device and refine the converter architecture. As a result, a GaN-based push-pull converter is designed and experimentally validated.

5.3.1. Passive component design

Following the general sizing process of capacitors and inductors, the input capacitor (C_{in}), output capacitor (C_{out}), and output inductor (L_{out}) are sized to fulfill the requirements of the maximum current and voltage ripple as defined in Table 5.4 [96]. The results for capacitance and inductance for different frequencies ranging from 200 kHz to 500 kHz are shown in Fig. 5.12.

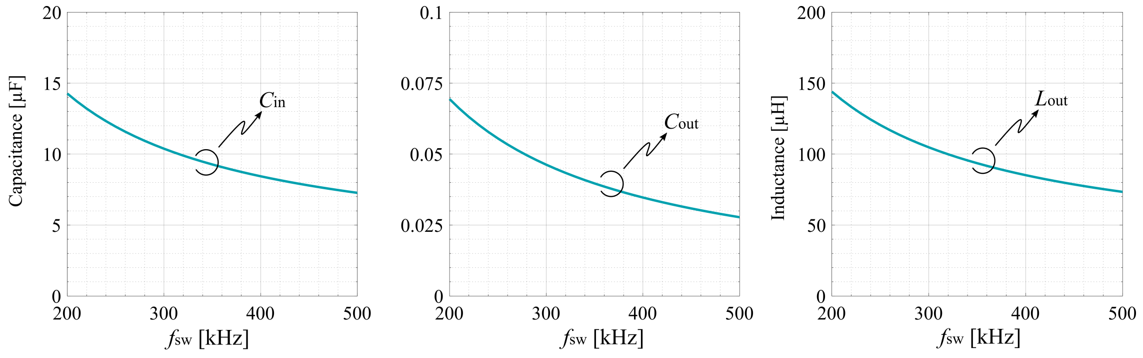


Figure 5.12: Input and output passive components size for different switching frequencies ranging from 200 kHz to 500 kHz.

Cost and volume functions have been developed based on the market analysis for SMD capacitors and inductors, [113], [114]. For the input capacitors, the search is filtered to 1210-sized and 100 V-rated 1 µF capacitors, and for the output to 1210-sized and 450 V-rated 0.1 µF capacitors. The required number of parallel devices is calculated, estimating the total cost and volume. On the other hand, the output inductor's cost and volume functions are estimated based on shielded power inductors. The volume functions (5.1)-(5.3) and cost functions (5.4)-(5.6) are obtained with the curve fitting method, for 100 V-rated capacitors, 450 V-rated capacitors, and 3 A-rated inductors, respectively.

$$f^{volume}_{\text{C, 100 V rated}} = 5.2955 \cdot 10^3 C_{\text{in}}, \tag{5.1}$$

$$f^{volume}_{\text{C, 450 V rated}} = 1.3239 \cdot 10^5 C_{\text{out}}, \tag{5.2}$$

$$f^{volume}_{\text{L, 3 A rated}} = 3.8144 \cdot 10^5 L_{\text{out}}^{1.2454}, \tag{5.3}$$

where, capacitance and inductance values are in *Farads* and *Henries*, to get the volume in cm^3.

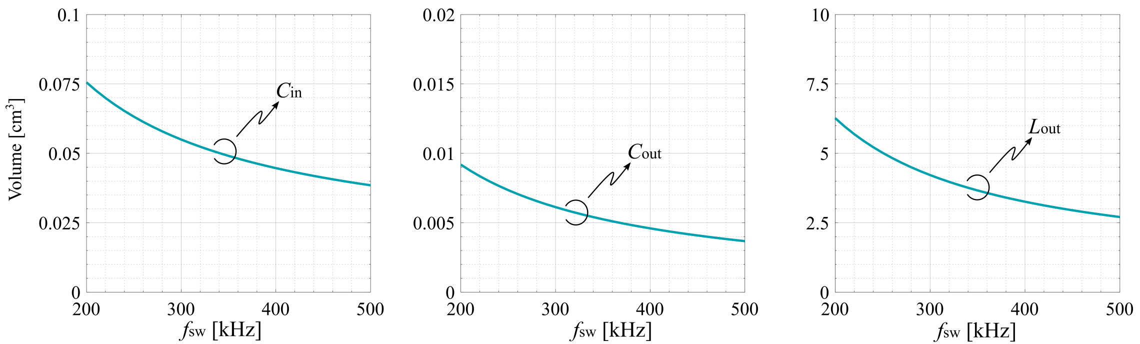


Figure 5.13: Input and output passive components volume for different switching frequencies ranging from 200 kHz to 500 kHz. Commercially available SMD components are selected.

$$f^{cost}_{\text{C, 100 V rated}} = 2.667 \cdot 10^5 C_{\text{in}}, \tag{5.4}$$

$$f^{cost}_{\text{C, 450 V rated}} = 1.638 \cdot 10^6 C_{\text{out}}. \tag{5.5}$$

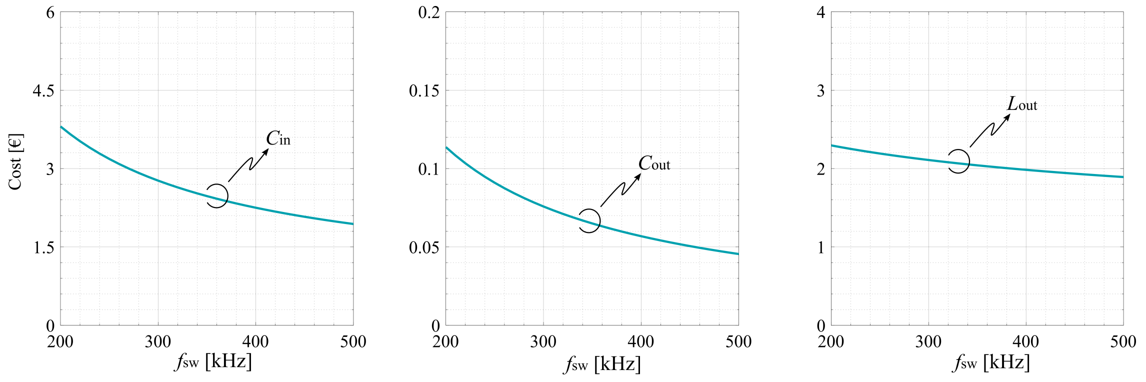


Figure 5.14: Input and output passive components cost for different switching frequencies ranging from 200 kHz to 500 kHz. SMD components are selected from the market.

$$f^{cost}_{\text{L, 3 A rated}} = 7.218 - 1.752 L_{\text{out}}^{-0.1168}, \tag{5.6}$$

From the analysis presented, it can be observed that the output inductor is the most significant component in terms of volume, primarily due to the compact size of the ceramic capacitors used (1210 footprint). In contrast, the input capacitor has a major impact on the overall cost, as meeting the required input capacitance to limit voltage ripple demands the use of multiple units or components with higher capacitance values. Although the output capacitor does not contribute significantly to either volume or cost, it remains essential for attenuating the output voltage ripple.

5.3.2. Planar transformer design

To fully exploit the fast-switching capabilities of GaN semiconductors and enable high-frequency operation, minimising the transformer's leakage inductance is essential. For this purpose, a planar transformer with PCB-integrated windings is considered. The transformer is designed and analysed within the context of the proposed converter, with particular emphasis on estimating its leakage inductance. Three core sizes from the EELP family are evaluated: the ELP 43/10/28, ELP 38/8/25, and ELP 32/6/20 ($n_C = 3$).

Table 5.5: Candidate cores for the push-pull converter

	A_e	V_e	Material	u. cost per 1000u
EELP 32/6/20	130 mm^2	5390 mm^3	3F36	0.93 €
EELP 38/8/25	194 mm^2	10200 mm^3	3F36	1.28 €
EELP 43/10/28	225 mm^2	13748 mm^3	3F36	1.75 €

The unit cost @ 1000 units is updated from Octopart (June, 2025).

To achieve a cost-effective solution, various configurations of the primary and secondary windings are explored using a 4-layer PCB. Each configuration can influence the leakage inductance of the transformer. Additionally, the thermal dissipation capability of each PCB layer must be taken into account. Therefore, to reach a compromise between a reduced leakage inductance and a thermally reliable assembly, two different mounting configurations are compared, and shown in Fig. 5.15: Primary-Secondary-Secondary-Primary (PSSP), and Secondary-Primary-Primary-Secondary (SPPS). Only symmetric configurations are

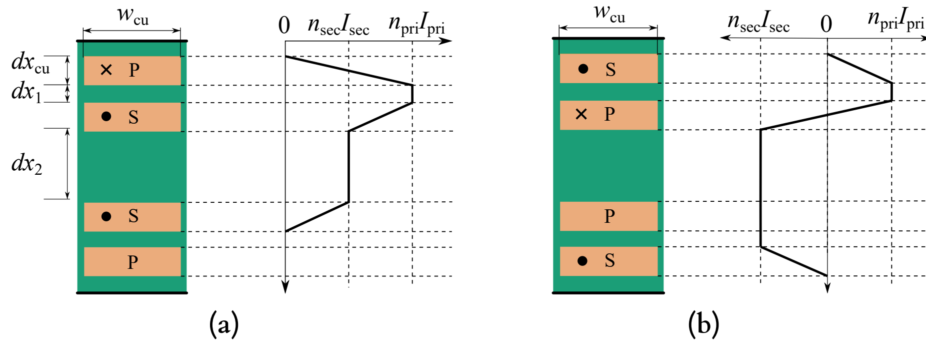


Figure 5.15: Magneto-Motive Force distribution across PCB height with configuration (a) PSSP and (b) SPPS, [112].

considered, and other configurations, such as SPSP or PSPS are discarded, thus achieving a symmetric behaviour in both switches.

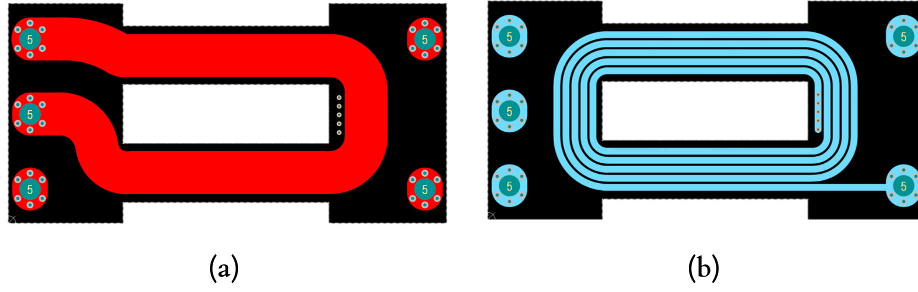
In the figure, dx_{cu} refers to the height of the copper (70 µm for 2 oz), dx_1 to the height of the insulator (prepreg) between layer 1 and layer 2 (same as between layer 3 and layer 4), and dx_2 to the height of the insulator between layer 2 and layer 3. These parameters can be chosen when designing the PCB and depend mostly on the options offered by the PCB manufacturer. According to the manufacturer's availability, heights of 0.31 mm (dx_1) and 0.7 mm (dx_2) are considered. The trace width of the primary winding W_{cu} is limited by the core's window width.

The leakage inductance L_{lk} for both configurations can be approximated following the formulas presented in [115],

$$L_{\mathrm{lk}} = \mu_0 n^2 L_{\mathrm{MTL}}/W_{\mathrm{cu}} \sum_{\mathrm{i}=1}^{n} F_{\mathrm{M,i}}^2 dx_{\mathrm{i}}. \tag{5.7}$$

For simplicity, the copper thickness dx_{cu} is neglected in the calculations. The number of turns on the side to which the leakage inductance is referred is denoted by n, then, μ_0 represents the vacuum permeability, L_{MTL} is the mean turn length of the windings, and $F_{\mathrm{M},i}$ is the magnetomotive force (MMF) at the i-th insulation layer, normalized concerning the absolute maximum MMF value.

The estimated leakage inductance for the EELP set with ELP 43/10/28 size, 6.1 mm trace width, and an L_{MTL} of 140 mm, using PSSP configuration, is 13.9 nH, and 10.4 nH for the SPPS configuration. Among both configurations, the chosen layout is the PSSP distribution due to thermal management reasons, since the primary is expected to have higher winding losses than the secondary, and the outer layers dissipate the heat more easily. Other configurations could be possible with multiple PCBs, which could reduce the leakage inductance much more (for example, 2 parallel SPPS), this option is discarded due to cost and complexity reasons. Additionally, the routing distance between the input capacitors and the winding terminals may increase the effective length of the primary winding, slightly raising both the leakage inductance and copper resistance beyond the estimated values. To account for these uncertainties, a conservative design margin is applied, and a leakage inductance of 20 nH is considered. The defined PCB winding is constructed and shown in Fig. 5.16, and the leakage inductance is measured with a Bode 100 Vector Network Analyzer (VNA) to be within the range of 20 nH.



(a) (b)

Figure 5.16: Planar transformer's PCB a) primary winding in top layer and b) part of secondary winding in mid-layer.

The power losses of the planar transformer are calculated for three different core sizes from the EELP set: ELP 32/6/20, ELP 38/8/25, and ELP 43/10/28. Total transformer losses are obtained by summing the core losses (P_c) and the copper winding losses (P_w) in both primary and secondary sides, including high-frequency effects. Core losses are primarily determined by the Steinmetz equation, which depends on the material-specific parameters K, α, and β, as well as the effective core volume V, the peak flux density B, and the switching frequency f_{sw}. Ferroxcube's 3F36 ferrite is selected for the following calculations. From the specification datasheet of the material, the coefficients K, α, and β (2.4×10^{-4}, 2.19, and 2.7, respectively) are obtained to calculate the core losses in kW, given by

$$P_c = VP_{cv} = VKB^{\beta} f_{sw}^{\alpha} \tag{5.8}$$

where P_{cv} denotes the core losses per unit volume. The peak flux density in the core depends on the voltage applied to the windings and can be estimated using standard equations from the literature [116].

Regarding the copper losses in the windings, both DC and AC components must be considered for the primary and secondary sides, i.e.,

$$P_w = P_{w\text{-dc}} + P_{w\text{-ac}}. \tag{5.9}$$

The DC component is calculated using Ohm's law, based on the resistivity of copper ρ, the number of turns in each winding n ($n = 1$ for the primary and $n = 10$ for the secondary), and the mean turn length L_{MTL}.

$$P_{w\text{-dc}} = R_{\text{cu-dc}} I_{\text{dc}}^2 = \frac{nL_{\text{MTL}}\rho}{A_w} I_{\text{dc}}^2 \tag{5.10}$$

where A_w is the cross-sectional area of the copper trace on the PCB. For the secondary winding, A_w is assumed to be ten times smaller to allow the same PCB area to accommodate more turns. The AC resistance arises due to skin and proximity effects, and the ratio between AC and DC resistance, denoted as F_r, can be approximated as follows [117]:

$$Fr = \frac{\chi}{2} \frac{\sinh\chi + \sin\chi}{\cosh\chi - \cos\chi} + (2m-1)^2 \frac{\chi}{2} \frac{\sinh\chi - \sin\chi}{\cosh\chi + \cos\chi} \tag{5.11}$$

where χ is the skin depth penetration factor (defined as the ratio of conductor height to skin depth), and m is the number of PCB layers used for a given winding section. Since the skin

depth varies with frequency, the AC resistance differs for each harmonic h of the current waveform. Consequently, the resistance must be computed individually for each harmonic, and the total copper losses are obtained by summing the contributions of all harmonics.

$$P_{\text{w-ac}} = \sum_{\text{h=1}}^{\infty} (R_{\text{cu-dc}} F r_{\text{h}}) I_{\text{RMS,h}}^2. \tag{5.12}$$

To accurately calculate the AC winding power losses, the frequency spectrum of the actual current waveform is required, including the high-frequency oscillations introduced by the parasitic elements present in the circuit. These oscillations are captured using the analytical model, as illustrated in the waveforms of Fig. 4.11. In this analysis, it is assumed that the current through each primary winding of the push-pull converter corresponds to the simulated $i_{\text{D,T1}}$, and that the total primary current i_{pri} is the sum of the currents through both primary windings.

5.3.3. Semiconductor selection

Due to device availability and the expected overvoltage conditions in the application, 100 V-rated GaN High Electron Mobility Transistor (HEMT)s and Si MOSFETs have been selected, in reduced parasitic packages such as Quad Flat No-lead (QFN), or Wafer Level Chip Scale Package (WLCSP). The considered devices are EPC2218, IGC033S10S1 (IQC0800NLS in the cited work), GAN3R2-100CBE, GS61008T-MR, and ISC027N10NM6. It is important to note that both the device codes and cost information have been updated as of June 2025, relative to the original analysis presented in [112]. Their key specifications are summarized in Table 5.6.

Table 5.6: Transistor comparison for the presented push-pull converter

	Tech.	I_{D}	$R_{\text{DS(on)}}$	Q_{G}	Package	U. Cost per 1000u
GS61008T-MR (GaN Systems)	GaN HEMT	90 A	9.5 mΩ	8 nC	QFN	4.2 €
EPC2218 (EPC)	GaN HEMT	60 A	3.2 mΩ	10.5 nC	WLCSP	2.45 €
GAN3R2-100CBE (Nexperia)	GaN HEMT	60 A	3.2 mΩ	9.2 nC	WLCSP	2.152 €
IGC033S10S1 (Infineon)	GaN HEMT	76 A	3.3 mΩ	10 nC	WLCSP	1.828 €
ISC027N10NM6 (Infineon)	Si OptiMOS6	192 A	2.7 mΩ	58 nC	QFN	1.935 €

The unit cost @ 1000 units is updated from Octopart (June, 2025).

These semiconductors are compared using the analytical model. Considering the impact of leakage inductance on the performance of the power switches, a snubber circuit is integrated with the power switches, reducing the drain-source overvoltage produced during the turn-off event. The snubber capacitor (C_{sn}) and snubber resistor (R_{sn}) are connected in parallel with each switch. To begin with the semiconductor comparison, the snubber capacitance C_{sn} and the snubber resistance R_{sn} have been sized initially following [118].

$$C_{\text{sn}} = C_{\text{OSS @ 24V}}, \tag{5.13}$$

$$R_{\text{sn}} = (L_{\text{loop}} / C_{\text{OSS @ 24V}})^{1/2}, \tag{5.14}$$

where L_{loop} is equal to the transformer's leakage inductance L_{lk}. Equations (5.13) and (5.14) can be used to run the first simulations and to ensure that the overvoltage will not exceed the maximum allowed drain-source voltage for each device. A safety threshold is set to 80 V, for 100 V breakdown voltage devices. Other parameters of the circuit, apart from L_{loop} and C_{OSS}, may also affect the voltage spike magnitude, which can be the gate resistance R_{G} or the gate-source capacitance C_{GS}. Therefore, the capacitance value of the snubber is adjusted through an iterative process using the analytical model. To run these testing simulations, the gate and snubber parameters are selected as listed in Table 5.7.

Table 5.7: Initial snubber and gate configuration for semiconductor comparison

	$R_{\text{DS(on)}}$	$R_{\text{G-on}}$	$R_{\text{G-off}}$	$C_{\text{OSS @ 24 V}}$	C_{sn}	R_{sn}
GS61008T-MR (GaN Systems)	9.5 mΩ	4.8 Ω	6.2 Ω	290 pF	1.5 nF	4.7 Ω
EPC2218 (EPC)	3.2 mΩ	4.8 Ω	6.2 Ω	800 pF	0.5 nF	4.7 Ω
GAN3R2-100CBE (Nexperia)	3.2 mΩ	4.8 Ω	6.2 Ω	700 nF	1 nF	4.7 Ω
IGC033S10S1 (Infineon)	3.3 mΩ	4.8 Ω	6.2 Ω	650 pF	1.2 nF	4.7 Ω
ISC027N10NM6 (Infineon)	2.7 mΩ	4.8 Ω	6.2 Ω	750 pF	0.5 nF	4.7 Ω

The total power losses are calculated, and the required dissipation area is estimated. For thermal dissipation, PCB copper planes are used, with thermal vias. To approximate the required area A_{plane} for a junction to ambient temperature difference ΔT_{ja} of 75 °C, and a certain amount of power losses $P_{\text{s}} + P_{\text{sn}}$, the following expression is used,

$$A_{\text{plane}} = R_{\text{thja}}(P_{\text{s}} + P_{\text{sn}})/\Delta T_{\text{ja}} \tag{5.15}$$

where R_{thja} is the thermal resistance from junction to ambient, for a 10 cm^2 plane (A_0) with 30 thermal vias, around 36 °C/W using the tool provided by EPC [119].

5.3.4. Multi-objective design

Once the snubber circuits are defined, the analytical model introduced in Chapter 4 is employed to estimate the switching and conduction losses of both the semiconductors and the snubbers across a frequency range of 200 kHz to 500 kHz. The total power losses are calculated under nominal operating conditions. Regarding the model's input parameters, V_{in} for the application or V_{in} in the model is taken from Table 5.4, I_{pulse} or I_{L} for the model, which is the average drain current i_{D} of the switches during the on-state, is calculated following

$$I_{\text{pulse}} = \frac{P_{\text{out}}}{2V_{\text{in}}\delta}. \tag{5.16}$$

And the primary current ripple ΔI_{pri}, or ΔI_{L} for the model, equals

$$\Delta I_{\text{pri}} = I_{\text{pri(max)}} - I_{\text{pri(min)}} = \frac{V_{\text{in}}\delta}{L_{\text{m}} f_{\text{sw}}} + \frac{N V_{\text{out}}(1 - 2\delta)}{2L_{\text{out}} f_{\text{sw}}}. \tag{5.17}$$

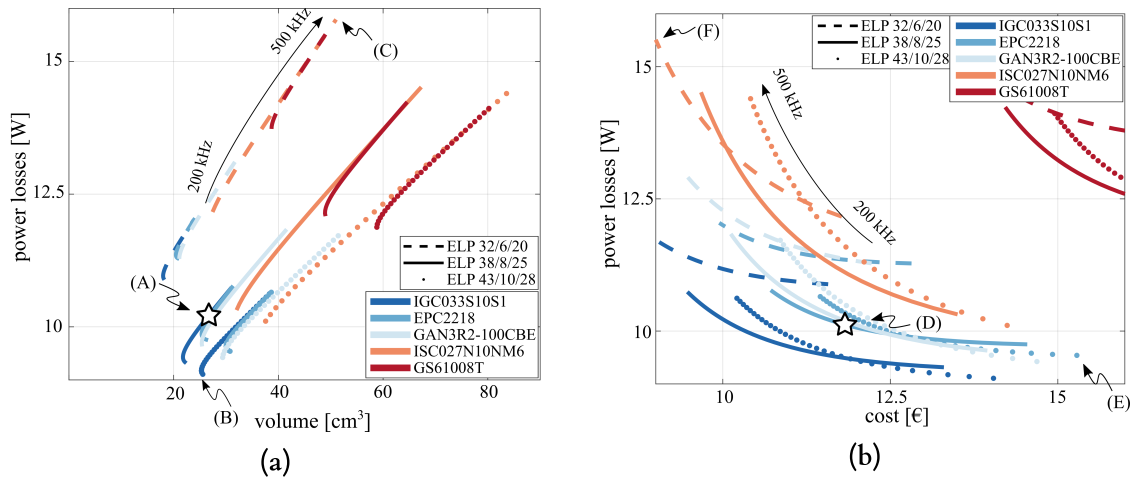


Figure 5.17: Power losses vs volume (a) and power losses vs cost (b) for three different core sizes, and five different 100 V semiconductors with low input FOM. The cost and the volume of the passive components are also included. Updated from [112].

For the multi-objective design process, the volume of the thermal dissipation area, A_{plane}, is also included in the evaluation. The volume and cost of the passive components are also incorporated into the analysis. Finally, by including the transformer's losses, volume, and cost, the overall performance indicators for the complete push-pull converter are obtained and summarized in Fig. 5.17. The results have been updated as of June 2025, with particular emphasis on revised semiconductor codes and cost data compared to the original work presented in [112].

Consistent with the presented results in the cited work, the volume of the system starts increasing close to the minimum switching frequency. This trend is primarily attributed to the minimal volumetric impact of surface-mounted passive components and the dominant contribution of the required area for thermal dissipation to the overall volume. As illustrated in Fig. 5.17(a), the point of minimum power loss, marked as (B), corresponds to the use of ELP 43/10/28 magnetic cores and the IGC033S10S1 semiconductor, operating at the lowest switching frequency of 200 kHz. The results further confirm that switches with lower $R_{\text{DS(on)}}$ values are more advantageous for this application, with the GaN Systems HEMT (GS61008T-MR) showing the poorest performance among the evaluated devices. At the time of the converter's initial design, the IGC033S10S1 was not yet commercially available, and the GS61008T-MR was excluded due to its significantly higher cost, visible in the losses versus cost comparison shown in Fig. 5.17(b). In this context, the lowest cost configuration is achieved using Infineon's Silicon MOSFET at the highest switching frequency, identified as point (F). The original work highlighted a more pronounced gap between Silicon and GaN technologies. However, the evolution of GaN technology over the past year has significantly improved its competitiveness, particularly in terms of cost. For Silicon devices, the lowest-cost option results in substantially higher power losses, as demonstrated by the equivalence between points (C) and (F $\equiv$ C). Conversely, excluding the GS61008T-MR, the most expensive solution is indicated by point (E). Overall, a well-balanced trade-off among power loss, volume, and cost is obtained at one of the lowest tested switching frequencies, approximately 250 kHz, corresponding to points (A) and (D $\equiv$ A). Based on this multi-objective evaluation, the EPC2218 GaN HEMT was selected for the final converter design, offering an optimal compromise in terms of cost, availability, and performance for the considered components. The ELP 38/8/25 core was chosen for the construction of the EELP magnetic core set. At the targeted design point, the

total power losses of the analysed components, including GaN switches, passive elements, and magnetic components, are estimated to be 10.2 W, with a compact volume of 27 cm^3 and an approximate cost of 12 €.

Snubber optimization for EPC2218

After selecting the semiconductors for the case study, the combination of switch and snubber components is further optimised. The optimisation focuses on the worst-case operating condition for the switches, which occurs at the minimum duty cycle required to achieve the lowest output voltage. As the duty cycle δ decreases, the peak current I_{pulse} increases (as shown in (4.20)), leading to higher turn-off overvoltages and increased switching losses for the same output power and switching frequency. To identify an optimal trade-off between switching losses and turn-off overvoltage, various combinations of snubber components and gate resistor values $R_{G\text{-off}}$ are evaluated using the analytical model. The analysis spans $R_{G\text{-off}}$ values from 4.7 to 18 Ω, snubber resistors R_{sn} from 0.22 to 5.6 Ω, and snubber capacitors C_{sn} from 0.47 to 1.47 nF. In all cases, the leakage inductance L_{lk} is assumed to be 20 nH.

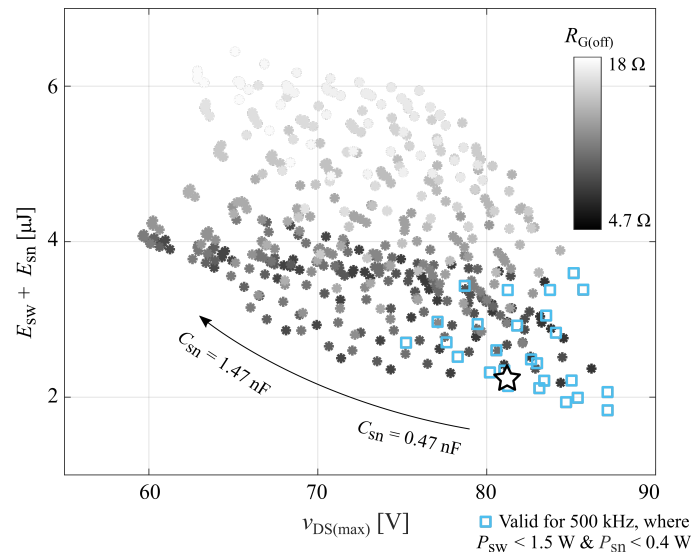


Figure 5.18: Semiconductor's maximum v_{DS} vs total switching energy (semiconductor and snubber) obtained using the analytic model. $R_{G\text{-off}}$ is analysed from 4.7 to 18 Ω, R_{sn} from 0.22 to 5.6 Ω, and C_{sn} from 0.47 to 1.47 nF, [112].

The relationship between the maximum drain-source voltage v_{DS} during turn-off and the total switching energy dissipated in each semiconductor and snubber combination is depicted in Fig. 5.18. The total switching energy ($E_{sw} + E_{sn}$), when multiplied by the switching frequency, determines the corresponding power losses. A threshold is set at 1.5 W for semiconductor switching losses and 0.4 W for snubber resistor losses. This allows the use of standard 0.5 W resistors in the snubber network. Based on the initial design specifications, only the configurations marked with blue squares meet both criteria, at the maximum switching frequency of 500 kHz. As observed from the greyscale in the plot, increasing the turn-off gate resistance $R_{G\text{-off}}$ results in higher switching losses. Conversely, increasing the snubber capacitance C_{sn} helps reduce the overvoltage, but also increases snubber power losses proportionally. Additionally, a higher snubber resistance R_{sn} contributes to increased snubber losses by damping oscillations more rapidly. The selected configuration is $R_{G\text{-off}} = 6.2$ Ω, $R_{sn} = 0.68$ Ω, and $C_{sn} = 0.5$ nF.

5.3.5. 300 W prototype validation

To validate the presented theoretical analysis, a proof-of-concept of the GaN-based push-pull converter has been materialized based on the component values derived from the described multi-objective design strategy.

Table 5.8: GaN-based push-pull prototype specifications and main components

Component	Name	Specifications
Transistors	EPC2218	100 V, 3.2 mΩ GaN HEMT
Output diodes	C6D04065E	600 V, 4 A SiC Schottky
Transformer core	EELP 38/8/25, 3F36	4.6 μH for one turn
Transformer wind.	PSSP, 2 oz copper	15–20 nH @ 100 kHz-10 MHz
Controller	UC3856DW	1 MHz current mode controller
Shunt	FCSL110R005DER	5 mΩ, low inductance
Thermal pad	–	900 mm^2, 30 vias per transistor
Input capacitor	12101C335K4T2A	100 V rated 3.3 μF x4
Output capacitor	C1210C104KCRAUTO	450 V rated 0.1 μF x2
Output inductor	MSS1583-224KED	3 A rated 220 μH

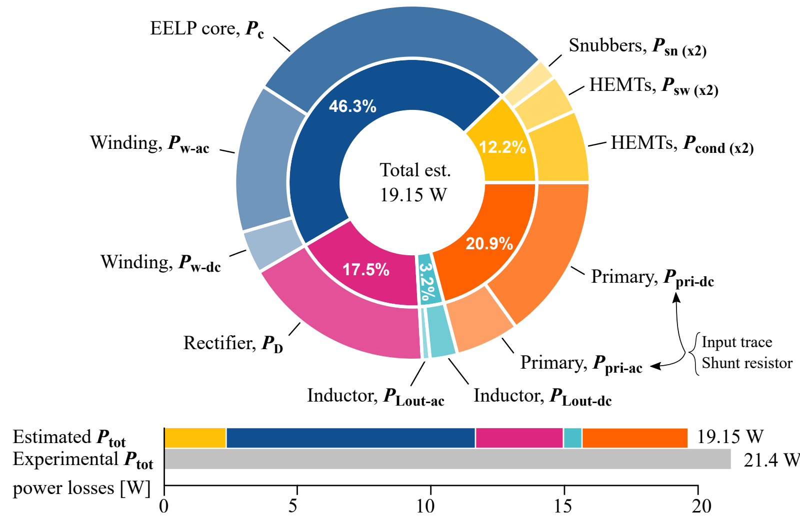


Figure 5.19: Power losses estimation for the proposed push-pull converter, working at 250 kHz, 48% δ, 24 V V_{in} and 230 V V_{out}. The total estimated losses are compared with experimental measurements, [112].

With the selected components, the total power losses and their distribution among various elements are calculated under nominal operating conditions, as illustrated in Fig. 5.19. The analysis includes losses generated by the shunt resistor and the resistance of the input PCB traces (from the connectors to C_{in}). These are grouped and split into DC and AC contributions, denoted as $P_{pri\text{-}dc}$ and $P_{pri\text{-}ac}$, respectively. Similarly, the output inductor losses are divided into $P_{Lout\text{-}dc}$ and $P_{Lout\text{-}ac}$ components. The losses on the secondary side due to the diode bridge, P_D, are estimated based on conduction characteristics extracted from the datasheet. The total estimated power loss, P_{tot} is 19.15 W, corresponding to an overall converter efficiency of 93.6%. A breakdown of the power loss distribution reveals that 46.3% of the total losses are attributed to the transformer, with the core contributing more than half of that figure. The

rectifier accounts for 17.5% of the total losses, while the shunt and trace resistors contribute 20.9% . Power switches represent 12.2% of the total losses, and the output inductor contributes just 3.2%.

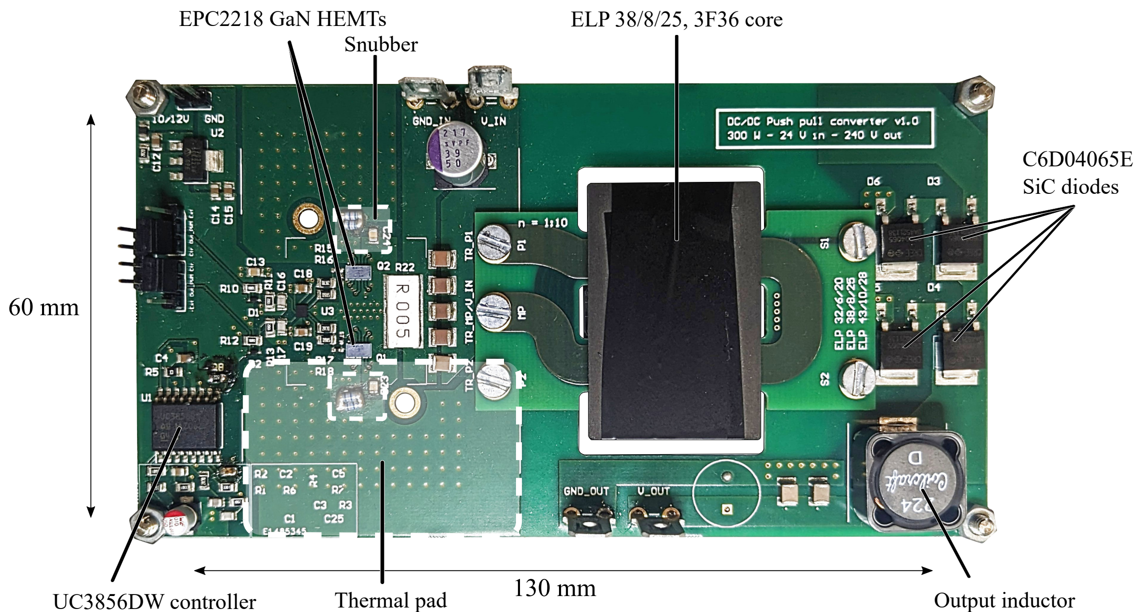


Figure 5.20: The 300 W GaN-based push-pull prototype. The prototype is 130 mm in length and 60 mm in width. The planar core is 16 mm in height, [112].

The constructed prototype is shown in Fig. 5.20, with a total footprint of 130 × 60 mm and a height of 16 mm, constrained by the planar transformer (EELP 38 cores). The resulting power density is 2.23 W/cm^3. The total cost of the magnetic components, capacitors, and semiconductors, including the GaN HEMTs and rectifier diodes, is estimated at 17.5 €.

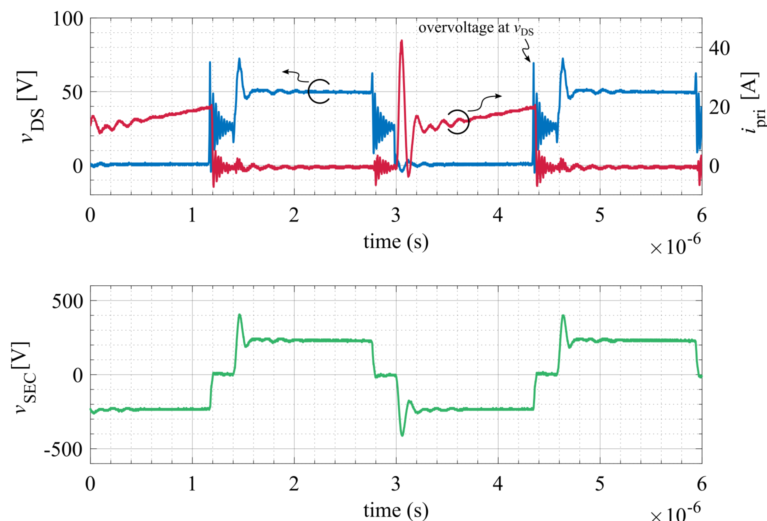


Figure 5.21: Experimental waveforms of drain-source voltage v_{DS} and drain current i_D of a single switch, and the secondary side voltage v_{sec} of the planar transformer, working at 41% duty cycle and 300 W output power. Updated from [112].

The drain current is measured using a Rogowski coil surrounding one primary winding

of the transformer, and is plotted in Fig. 5.21 with the corresponding drain-source voltage of the switch. The transformer's secondary side voltage is also measured with an isolated voltage probe. The waveforms are measured working under the worst-case scenario for the switches (41% duty cycle). The results confirm that the maximum reached drain-source voltage falls below 80 V, as defined in the analysis. The waveforms also indicate a notable ringing in the current during the turn-on of the switches, probably due to the charging of the parasitic capacitance of the windings, which was not considered in the analysis.

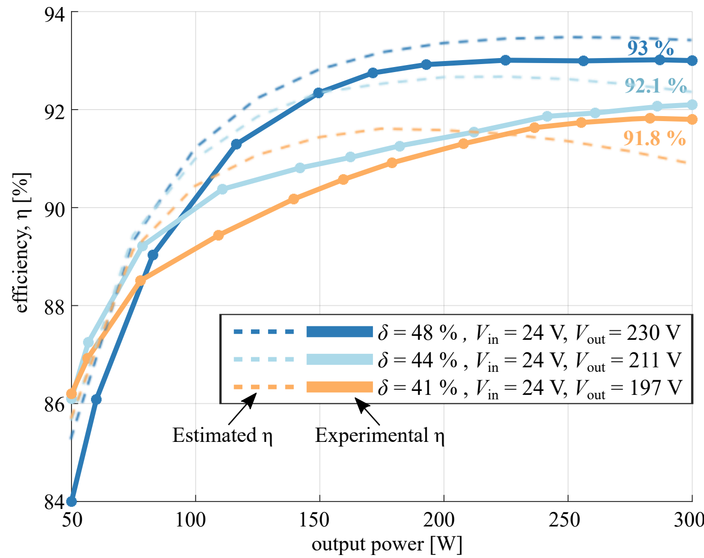


Figure 5.22: Measured and estimated efficiency of the experimental prototype, working at different duty cycles, and power ranging from 50 W to 300 W. The operating frequency is 250 kHz for 48% duty cycle, 270 kHz for 44% duty cycle, and 310 kHz for 41% duty cycle, [112].

The converter's efficiency was evaluated at three different duty cycles, with output power levels ranging from 50 W to 300 W, as shown in Fig. 5.22. A peak efficiency of 93% is achieved under nominal operating conditions (V_{in} = 24 V, V_{out} = 230 V) at a duty cycle of 48% and a switching frequency of 250 kHz. The switching frequency is slightly adjusted to obtain the desired duty cycles using the selected current-mode controller and the prototype's limitations. At 270 kHz and 44% duty cycle (V_{out} = 211 V), a peak efficiency of 92.1% is recorded, while 91.8% is achieved at 310 kHz and 41% duty cycle (V_{out} = 197 V).

The Silicon-based push-pull converter used to validate the analytical model presented in Chapter 4 was also tested under varying duty cycles, down to 41%, and operated at a switching frequency of approximately 20 kHz. Under nominal conditions (≈ 210 V, 300 W output), the Silicon-based converter achieves an efficiency of 91%, with 8.9 W of power losses generated in the primary switches. When the duty cycle is reduced to 41% to regulate the output voltage (down to 170 V), the efficiency decreases to 89%. In comparison, the GaN-based converter improves the overall efficiency by 2–3% within the studied operating range and reduces primary switch losses by more than 70%. Furthermore, the converter volume is reduced by a factor of four, mainly due to the use of a PCB-integrated heat dissipation system and low-profile components.

5.3.6. Calorimetric characterization

To further validate the analytical estimations of the total converter losses and their distribution among individual components, a calorimetric thermal analysis is carried out, following the same methodology used for the Silicon-based push-pull converter presented in [95]. In this method, the power supply is used to selectively feed specific components (e.g., switches, inductor, transformer), intentionally forcing them to dissipate controlled amounts of power. By monitoring the thermal response of each component to a known power dissipation, a relationship between power loss and temperature rise can be established. This calibrated thermal behaviour can then be applied in reverse: by observing the temperature evolution of each component during normal operation, its corresponding power loss can be estimated. Although this calorimetric method requires individual characterisation of each component, the high level of integration and thermal coupling in this design limits the ability to isolate the temperature vs. power loss relationship for all devices. Such limitations are evident, for example, in the primary-stage components, including the switches, snubbers, and shunt resistor, where thermal coupling prevents independent measurement. A similar effect is observed between the diode bridge and the output inductor on the secondary side. To address this, thermal interactions between components are approximated by simplified equations, coupling the components or the regions, as represented in Fig. 5.23.

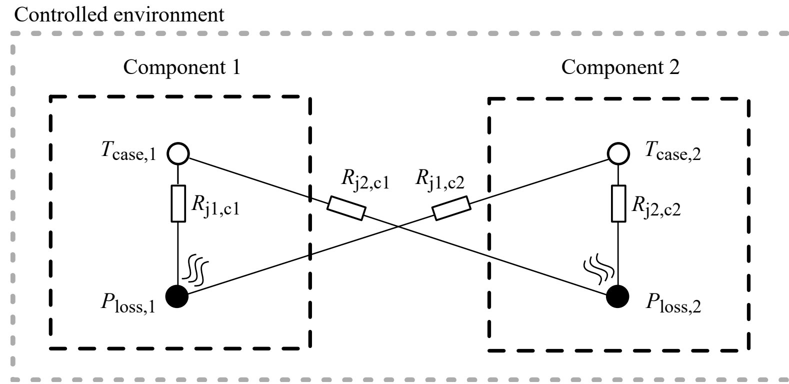


Figure 5.23: Thermal coupling representation of two components of the converter.

The coupling represented in Fig. 5.23 shows two power loss sources (black points $P_{\text{loss},1}$ and $P_{\text{loss},2}$) representing the power loss source of the coupled components. The coupling equivalent resistance between the first component's power loss source and its case is $R_{\text{j1,c1}}$, and between the same component's power loss source and the case of the second component is $R_{j1,c2}$. For the second component, these parameters are $R_{\text{j2,c2}}$ and $R_{\text{j2,c1}}$. The measured temperatures of both components are $T_{\text{case-1}}$ and $T_{\text{case-2}}$. The coupling equations 5.18 and 5.19 are solved between the shunt resistor and the GaN HEMTs + snubbers in the primary side, and between the output rectifying diodes and the inductor in the secondary side.

$$T_{\text{case-1}} = P_{\text{loss},1}R_{\text{j1,c1}} + P_{\text{loss},2}R_{\text{j1,c2}} \tag{5.18}$$

$$T_{\text{case-2}} = P_{\text{loss},2}R_{\text{j2,c2}} + P_{\text{loss},1}R_{\text{j2,c1}} \tag{5.19}$$

First, the secondary side is tested. Using a current source to insert power losses into the output diode bridge, the temperature of one of the diodes is monitored and plotted in Fig. 5.24 (b). At the same time, the inductor's temperature, which has been left out of the electric

loop and has no losses in this test, is monitored to obtain the thermal coupling between the two different elements.

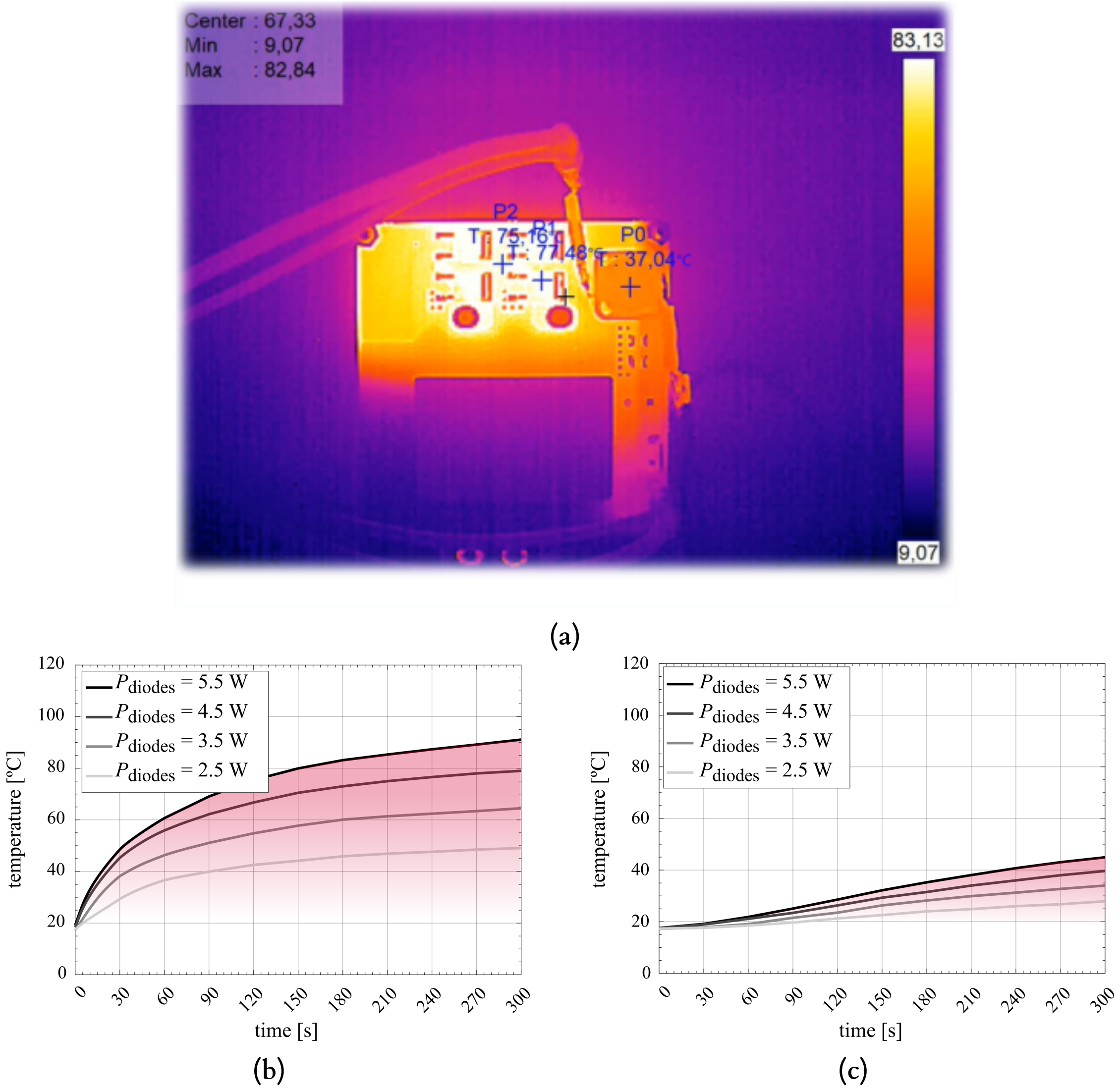


Figure 5.24: (a) Thermal capture, (b) temperature evolution of one rectifying diode, and (c) temperature evolution of the output inductor, dissipating power in the diodes ranging from 1.5 W to 5.5 W.

A similar test is repeated, but now inserting the power losses only in the output inductor. The inductor's and the diodes' temperatures are monitored and plotted in Fig. 5.25.

Knowing the temperature evolution of diodes and inductor at different test conditions makes it possible to estimate the thermal coupling of the simplified model. For that, two equations are formulated:

$$T_{\text{diode}} = P_{\text{loss,diode}} R_{\text{diode,diode}} + P_{\text{loss,ind.}} R_{\text{diode,ind.}} \tag{5.20}$$

$$T_{\text{ind.}} = P_{\text{loss,ind.}} R_{\text{ind.,ind.}} + P_{\text{loss,diode}} R_{\text{ind.,diode}} \tag{5.21}$$

These two equations are resolved for two different cases: case 1, where all the power losses are dissipated in the rectifying diodes, meaning that $P_{\text{loss,total}}/4$ equals $P_{\text{loss,diode}}$ and

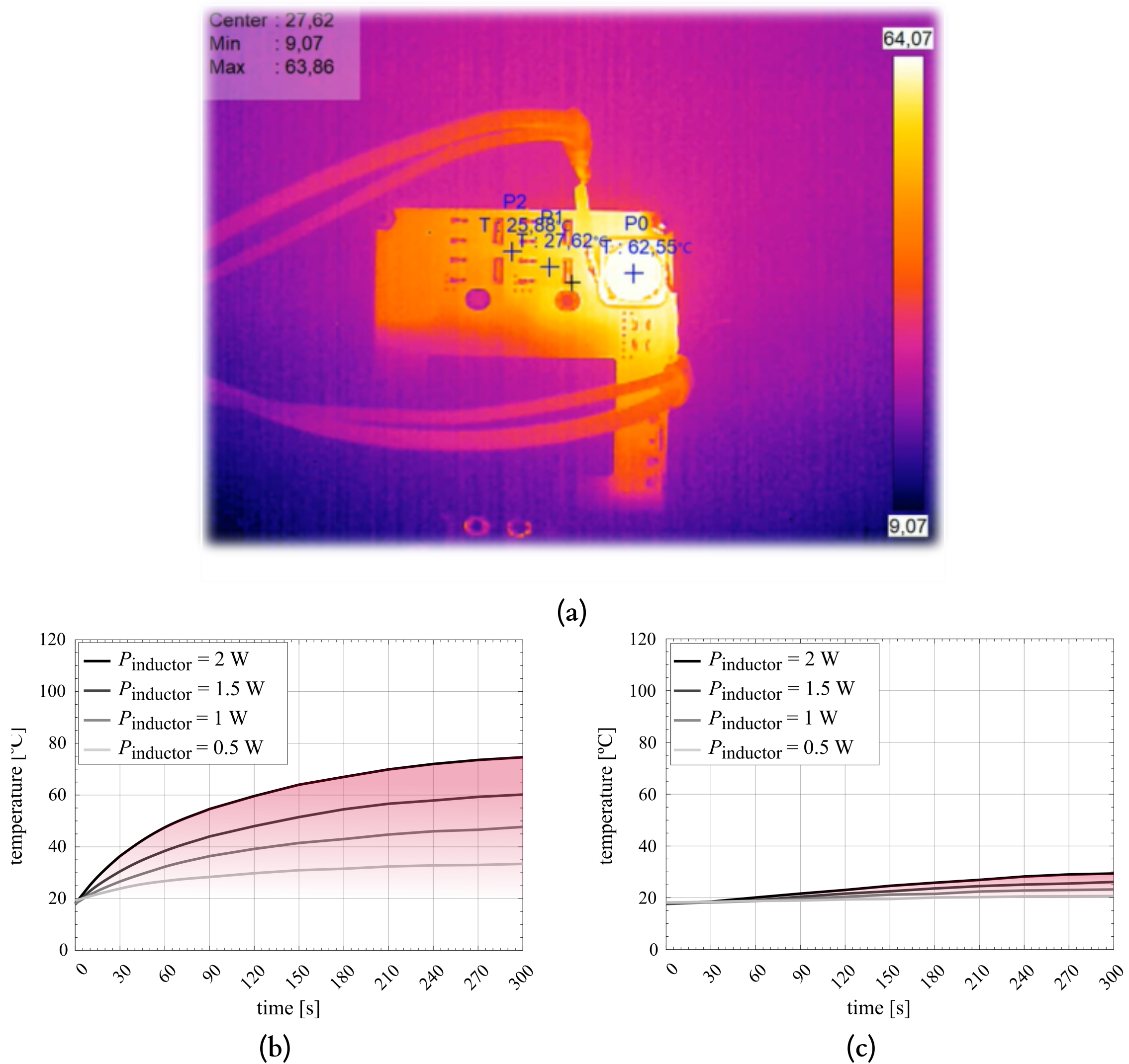


Figure 5.25: (a) Thermal capture, (b) temperature evolution of output inductor, and (c) temperature evolution of one rectifying diode, dissipating power in the output inductor ranging from 0.5 W to 1.5 W.

$P_{loss,ind.}$ is zero, and case 2 where all the power is dissipated in the inductor, meaning $P_{loss,total}$ equals $P_{loss,ind.}$ and $P_{loss,diode}$ is zero. Once the four unknown variables $R_{diode,diode}$, $R_{ind.,ind.}$, $R_{diode,ind.}$, and $R_{ind.,diode}$ are obtained, it is possible to estimate the power loss distribution only by monitoring the temperature of the diode and inductor.

The same process is repeated with the primary side components. First, the current source is connected to the input V_{in} terminals inversely, inserting current in the reverse direction to the switches. In this manner, the power is dissipated mostly in the active switches due to the reverse voltage drop created in the HEMT channel. A power loss consumption is also generated in the shunt resistor, which can be considered negligible compared to the reverse conduction voltage drop of the GaN devices. The temperature evolution of both switches is monitored and plotted in Fig. 5.26.

The second test is performed by connecting the current source forward-biased to the input terminals. The active switches are closed with constant Gate voltages (V_{GS} = 5 V). It is

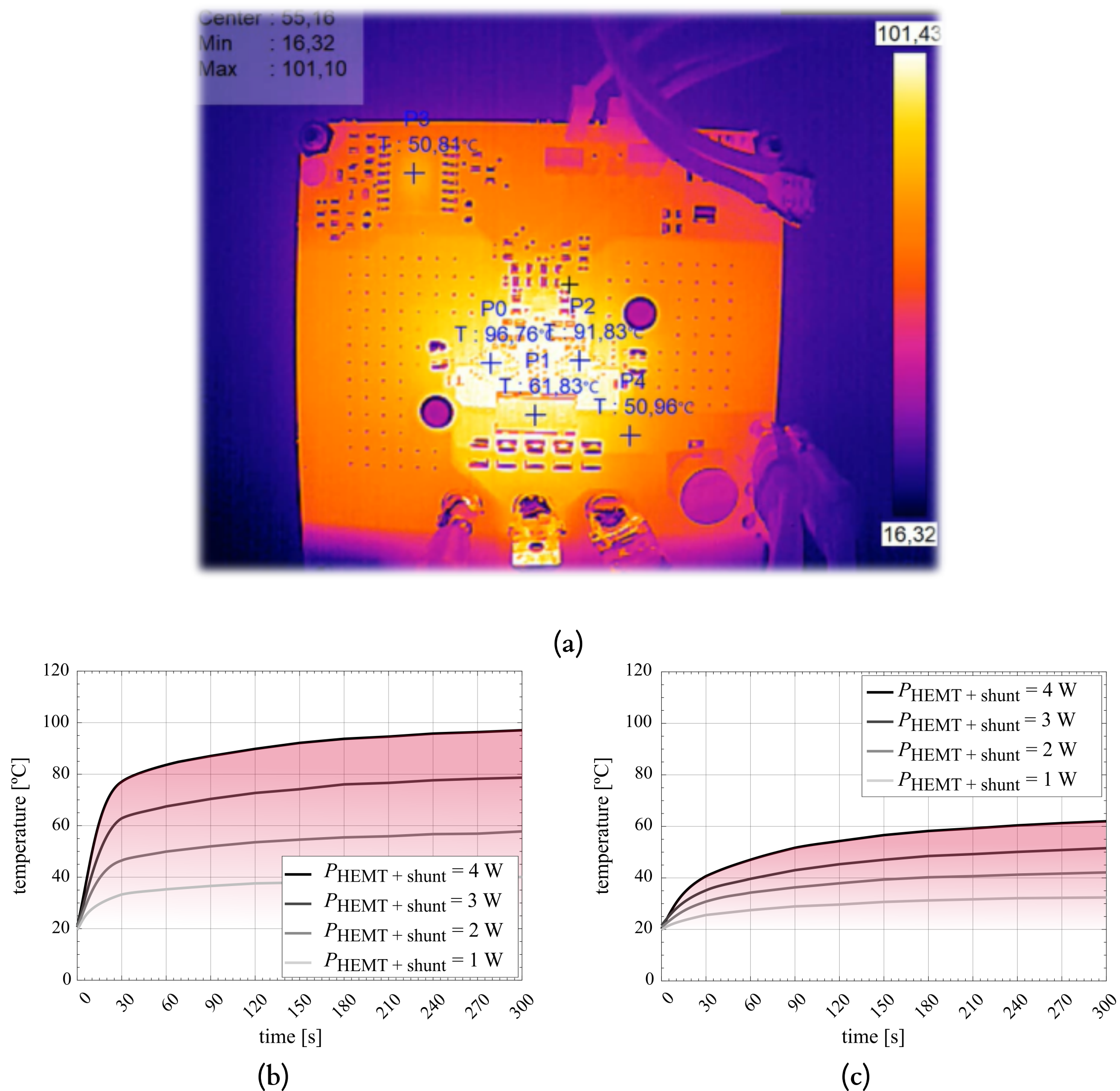


Figure 5.26: (a) Thermal capture, (b) temperature evolution of active switches, and (c) temperature evolution of shunt resistor, dissipating power in both elements ranging from 1 W to 4 W.

important to understand that due to the low $R_{\text{DS(on)}}$ of the active switches, now the voltage drop is divided proportionally between the switches and the shunt resistor. 68% of the voltage drop is produced in the shunt resistor, (R_{shunt} = 5 mΩ in series with 2 switches of $R_{\text{DS,on, 100°C}}$ = 4.8 mΩ in parallel), see Fig. 5.26.

Lastly, the transformer's PCB is thermally characterized. For that, a current source is connected to the primary winding, and a second current source to the secondary winding. The secondary current is configured to be 1:10 of the primary current, trying to emulate the current ratio of the designed transformer, Fig. 5.28.

Once each section of the converter is characterized separately, the converter is operated under nominal operating conditions, and the temperature of each element is monitored.

The thermal image of the prototype, shown in Fig. 5.29, illustrates the temperature distribution among the components. The highest measured temperature reaches 94.1 °C at the switches under steady-state operation.

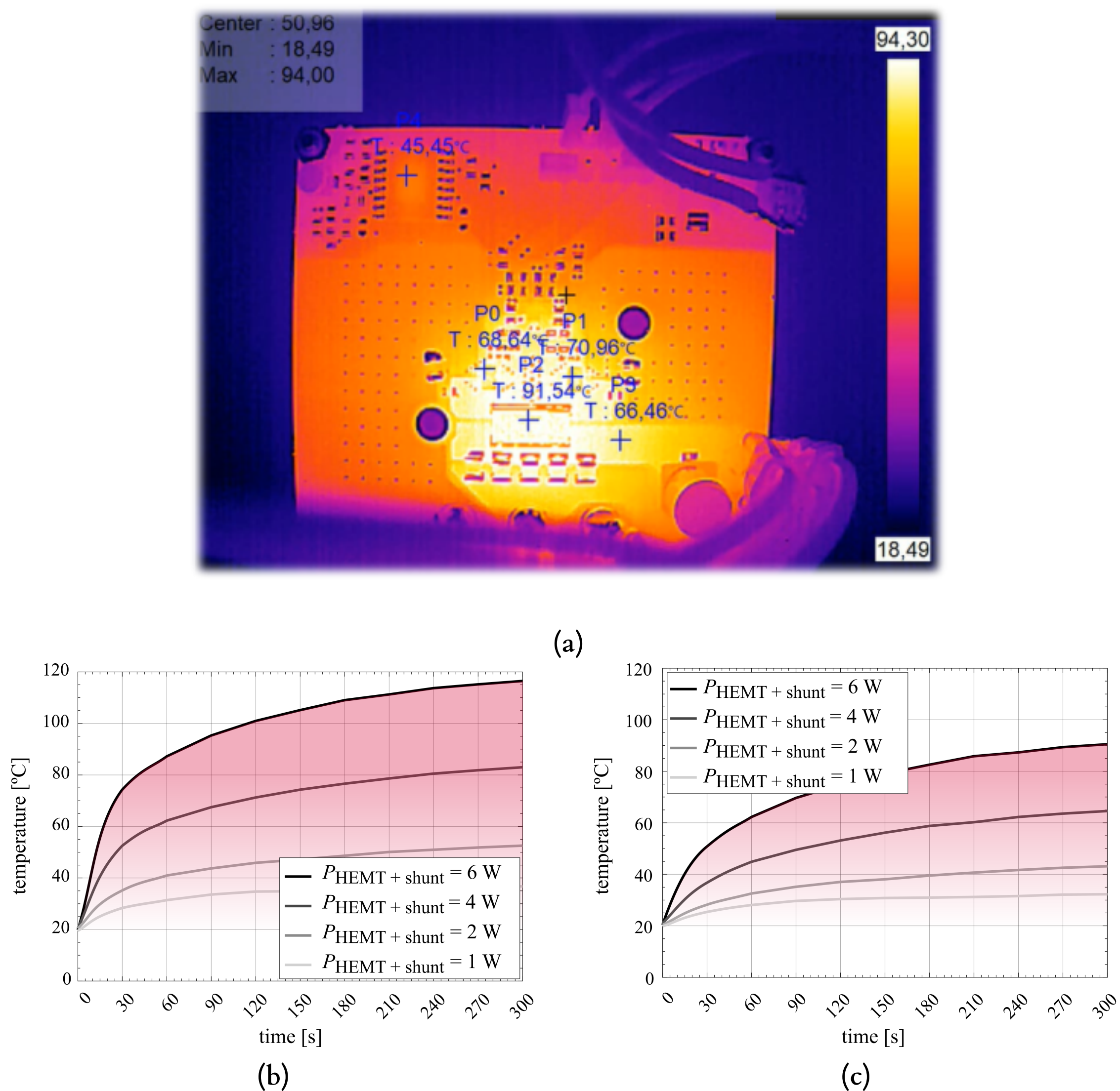


Figure 5.27: (a) Thermal capture, (b) temperature evolution of shunt resistor, and (c) temperature evolution of one HEMT, dissipating power in both elements ranging from 1 W to 6 W.

The thermal evolution of each element can be used to estimate the distribution of the power losses of the converter. These results are gathered in the following Table 5.9.

Focusing on the primary-side losses, the thermally estimated losses in the switches and snubbers are approximately 30% higher than those estimated analytically. In contrast, the remaining primary-side losses (shunt and PCB traces) show very good agreement between both methods. When looking into the transformer's winding losses (primary and secondary) with calorimetric testing, they are calculated to be 33% higher than the analytical estimates. Although the individual comparison reveals significant discrepancies between the two approaches, it is important to note that the thermal analysis does not account for the thermal coupling between the transformer's PCB-integrated windings and the rest of the board, which could partly explain the observed differences. The total losses determined by the calorimetric method, excluding the transformer's core losses, sum up to 15 W, compared to 13.65 W from the analytical method, resulting in a deviation of less than 10%. Including the core losses, which are calculated analytically, and verified with MagNet Challenge data [120], the overall thermal

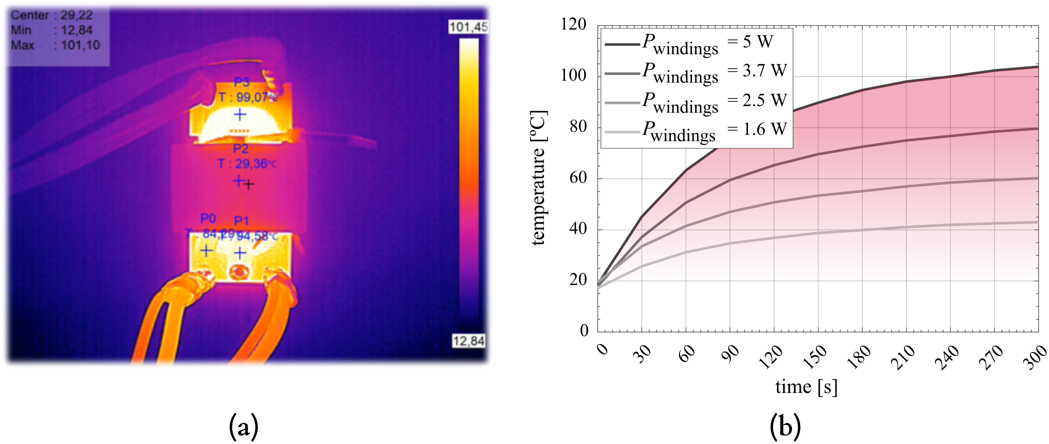


Figure 5.28: (a) Thermal capture and (b) temperature evolution of PCB windings dissipating total power ranging from 1.5 W to 5 W.

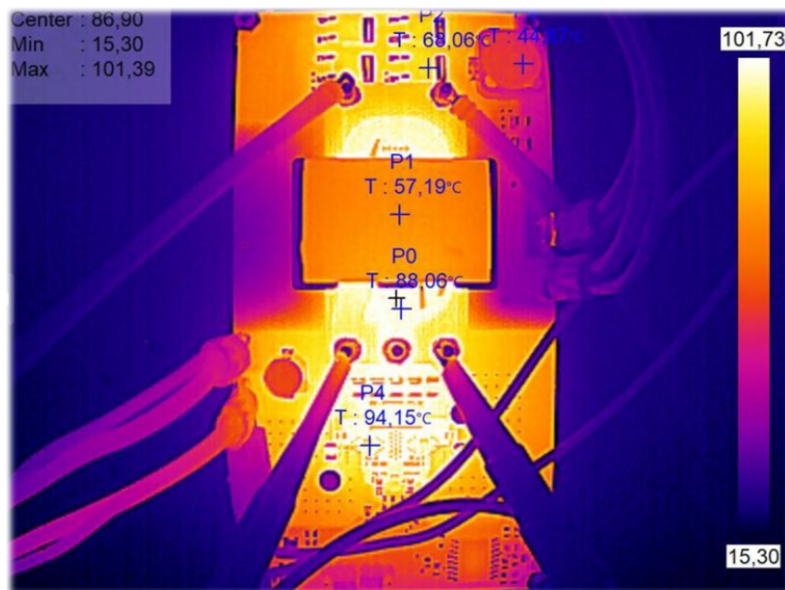


Figure 5.29: The 300 W GaN-based push-pull converter's steady-state thermal capture obtained with a TE-Q1 thermal camera. The converter is working at 250 kHz, 48% duty cycle, and 300 W output power, [112].

estimation results in total power losses, P_{tot} of 20.5 W. Meanwhile, the analytical estimations predicted a P_{tot} of 19.15 W, and by measuring input and output power, the wattmeter results in a total power loss of 21.4 W.

5.3.7. Discussion

Starting from the behavioural study of the Silicon-based push-pull converter and implementing the presented analytical model, a GaN-based push-pull converter design is implemented, targeting reduced cost, volume, and improved efficiency. The use of a PCB winding and a planar transformer, the minimization of parasitics in the layout, and the use of snubbers offer the right combination to use GaN switches in this topology, moving above 200 kHz switching

Table 5.9: Results for the GaN-based push-pull prototype, working at 300 W, 24 V (δ = 48%), and 250 kHz.

Variable	Loss type	Analytical	Calorimetric	**Experimental**
Transistor, $P_{sw} + P_{cond}$	DC	(2x) 0.636 W	3 W	
	AC	(2x) 0.34 W		
Snubber, P_{sn}	AC	(2x) 0.19 W	-	
Transformer core, P_c	AC	5.5 W	-	
Transformer winding, P_w	DC	0.75 W	4.5 W	
	AC	2.614 W		
Rectifying diode, P_D	DC	(4x) 0.836 W	3 W	
	AC	0 W		
Primary resistance, P_{pri}	DC	2.8911 W	4 W	
	AC	1.112		
Output inductance, P_{Lout}	DC	0.1365 W	0.5 W	
	AC	0.4784 W		
Total losses, P_{tot}		**19.15 W**	**20.5 W**	**21.4 W**

frequencies, and minimizing the cost and volume of most components.

To achieve this, an operating frequency range between 200 kHz and 500 kHz is selected, and the passive components are dimensioned accordingly. From the outset of the design, special attention is paid to minimising the transformer's leakage inductance, as it critically affects both the switching losses and the overvoltage stress experienced by the semiconductors. Consequently, the transformer and semiconductor selection are coordinated to ensure optimal system-level performance. Once the transformer is characterised and switch models are defined, the presented modelling tool is used to evaluate the switching behaviour and to size the snubber networks appropriately, selecting a well-balanced operating point in terms of losses, volume, and cost. A 20 nH leakage inductance PCB winding is constructed, which enables the design of a 300 W GaN-based push-pull prototype, working with EPC2218 devices at 250 kHz, validating the analytical estimations.

The calorimetric characterisation of individual sections of the converter, followed by comparison with both analytical estimations and experimental measurements, highlights the complexity of accurately isolating and quantifying power losses on a per-component basis. The results indicate that the primary-side losses and winding losses were underestimated in the analytical approach. Calorimetric testing further reveals significant thermal coupling among several key components, including the GaN HEMTs, shunt resistors, windings, and input PCB traces. Moreover, discrepancies between measured and estimated losses can be attributed to factors not included in the analytical model, such as the dynamic variation of the GaN HEMTs' $R_{DS(on)}$ and the parasitic resistances of electrical interconnections, as well as the high-frequency effects present in the PCB traces and components.

The efficiency measured experimentally with the GaN-based converter reaches 93% working under nominal conditions (V_{in} = 24 V, V_{out} = 230 V). The efficiency slightly drops when output regulation is enabled, where the constructed prototype reaches 91.8% for the analysed worst conditions (V_{in} = 24 V, V_{out} = 197 V). This trend suggests that the GaN-based converter performs better than the Silicon-based converter under output regulation requirements. In terms of volume, the constructed prototype is approximately 125 cm^3. The cost of the main components (power switches, transformer, and passives) is around €12 per unit in a 1000-unit batch.

The GaN-based converter is also benchmarked against two recently reported low-voltage input isolated DC/DC converter designs from the literature [121], using nominal operating conditions to ensure a fair comparison. According to [121], an interleaved flyback converter based on Silicon devices achieves an efficiency of 92.3%, a power density of 1.97 W/cm^3, and a combined cost of approximately €38 per 1000 units for magnetics, semiconductors, and capacitors. The same work also presents a full-bridge topology, which increases efficiency to 94.9% under nominal conditions but at the expense of a higher cost (around €47 per 1000 units) and a reduced power density of 1.78 W/cm^3. In comparison, the proposed GaN-based push-pull converter demonstrates a 0.7% improvement in efficiency over the interleaved flyback design, while simultaneously reducing the cost by 54% and increasing power density by 14%. Although the Silicon-based full-bridge achieves slightly higher efficiency, the increased number of switches results in greater cost and lower power density. Overall, the GaN-based push-pull converter offers a compelling trade-off, achieving a well-balanced optimisation of efficiency, volume, and cost among the evaluated solutions.

5.4. LLC Half-bridge Converter Design

The hard-switching push-pull converter presented in this work has already demonstrated significant improvements in cost, volume, and efficiency when compared to the Silicon-based reference design. By preserving the same converter topology and simply replacing the Silicon MOSFETs with GaN HEMTs, a fair and unbiased comparison was ensured, isolating the influence of the semiconductor technology from any topological advantages. In this hard-switching context, GaN devices exhibit improved dynamic performance, particularly in terms of fast switching transitions and reduced switching losses; however, the influence of the planar transformer should also be considered here. These results strongly support the claim made in the State of the Art chapter that GaN offers clear advantages over Silicon in hard-switching applications. The comparative analysis of Figure of Merit (FOM) also revealed that the benefits of GaN are less pronounced in soft-switching converters. In such topologies, the impact of improved switching speed is inherently reduced due to the near ZVS or ZCS transitions during switching events. Moreover, for the power level and performance targets of the application considered, the required $R_{\mathrm{DS,on}}$ values are so low that suitable GaN devices are not widely available, whereas Silicon MOSFETs, benefiting from greater commercial maturity, can offer lower conduction resistance at competitive cost and higher availability. This limitation suggests that, in soft-switching applications, the advantages of GaN over Silicon are less straightforward, and additional parameters must be evaluated to determine the most suitable technology. It is worth noting, however, that the inherently fast-switching nature of GaN devices could still offer benefits even in soft-switching scenarios. For instance, the reduction of deadtime, often necessary to ensure ZVS in resonant converters, may be facilitated by the faster transitions of GaN devices, potentially improving overall system performance. This hypothesis remains to be thoroughly investigated.

To further investigate the benefits and trade-offs between semiconductor technologies in a soft-switching environment, a resonant half-bridge LLC converter is proposed. This topology enables zero-voltage switching (ZVS), offering an ideal environment to exploit the performance of semiconductor devices while mitigating switching losses. By employing the latest generation of switching devices in the resonant converter, a comparative study can be conducted to analyse how GaN and Silicon (Si) technologies perform under fundamentally different switching conditions, thereby providing deeper insights into their respective suitability for isolated DC/DC converter applications.

The half-bridge LLC converter is designed for the same application as the push-pull converter; however, as was done with the push-pull converter, the design requirements are adjusted to facilitate the design of the LLC. One of the main challenges when working with a soft-switching topology is its limited regulation capacity, maintaining the soft-switching conditions. When regulation is required, the working conditions often change, and the soft-switching is no longer achieved. The standard half-bridge LLC configuration is prone to this behaviour, and for this reason, the regulation requirements for this application are left out for the resonant stage. As a result, regulation in this solution is not handled by the resonant stage. Instead, an additional regulation stage is introduced in the following subchapter to meet output control requirements.

Following the steps for the push-pull converter design, the half-bridge converter is first studied, addressing its main waveforms and characteristics. Later, the passive components are sized for the desired application, including the resonant components. Using the analytical model, various generic semiconductors are compared. In this context, Silicon- and GaN-based switches are compared, discussing their differences and advantages for this application. Lastly,

Table 5.10: Requirements for the designed Si-based step-up LLC converter

Parameter	Symbol	Value
Input voltage	V_{in}	20 V ... 28 V
Output voltage	V_{out}	200 V ... 280 V **(non-regulated)**
Output power	P_{out}	**300 W**
Maximum input voltage ripple	ΔV_{in}	$<$ **10%** of V_{in}
Maximum output voltage ripple	ΔV_{out}	$<$ **10%** of V_{out}
Switching frequency	f_{sw}	50 - 300 kHz

a comprehensive optimisation process is carried out to select the most appropriate devices and finalise the converter architecture. As a result, a Silicon-based half-bridge LLC converter is designed and experimentally validated.

5.4.1. LLC resonant half-bridge converter with split capacitor

The LLC resonant converter is widely recognised for its minimal component count among resonant isolated DC/DC topologies. It consists of a primary and a secondary stage separated by a high-frequency isolation transformer, Fig. 5.30. On the primary side, the series connection of the resonant inductor and capacitor is excited by two switching devices, generating a near-sinusoidal current at the tank's resonant frequency. Under nominal conditions, the switches operate at this resonant frequency, enabling soft-switching, either zero-voltage switching (ZVS) or zero-current switching (ZCS), thanks to the sinusoidal nature of the waveforms. This soft-switching capability, achieved with relatively low complexity, makes the LLC topology a well-established industrial standard, offering some of the highest efficiencies among isolated converter architectures, [122], [123], [124].

The resonant tank, composed of the resonant inductance L_r, magnetizing inductance L_m and resonant capacitance C_r, can be driven by either a half-bridge or full-bridge configuration. In the half-bridge arrangement, the use of a split-capacitor input reduces the input current i_{pri} and doubles the ripple frequency, although it typically requires additional passive components, [125]. Given that the targeted application involves low voltage and high current, this structure is selected as the most appropriate. Fig. 5.31 presents the key waveforms of the LLC resonant half-bridge converter with split capacitors, operating in $f_{sw} \approx f_r$.

$$I_{in(max)} = \frac{I_{D(max)}}{2}, \tag{5.22}$$

where, $I_{D(max)}$ is equal to $I_{pri(max)}$. Additionally, the RMS current of circulating through the resonant tank can be approximated as follows:

$$I_{pri(RMS)} \approx \frac{P_{out}}{V_{in}\delta}. \tag{5.23}$$

The half-bridge is formed by switches S_1 and S_2, typically operating with a maximum duty cycle $\delta \approx 0.5$, and a defined deadtime dt to prevent shoot-through. The current flowing through the resonant tank, i_{pri}, is approximately sinusoidal and consists of two components: the resonant current i_r and the magnetising current i_m. The magnetising current sustains the transformer's flux and facilitates soft-switching by ensuring that current is present at the instant of switching transitions.

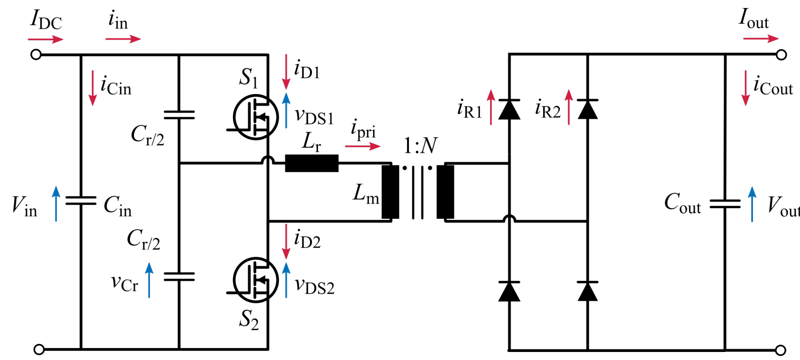


Figure 5.30: The studied LLC resonant converter topology, with the main primary switches S_1 and S_2, the input capacitance C_{in}, transformer, output rectifying diodes, and output filter with C_{out}.

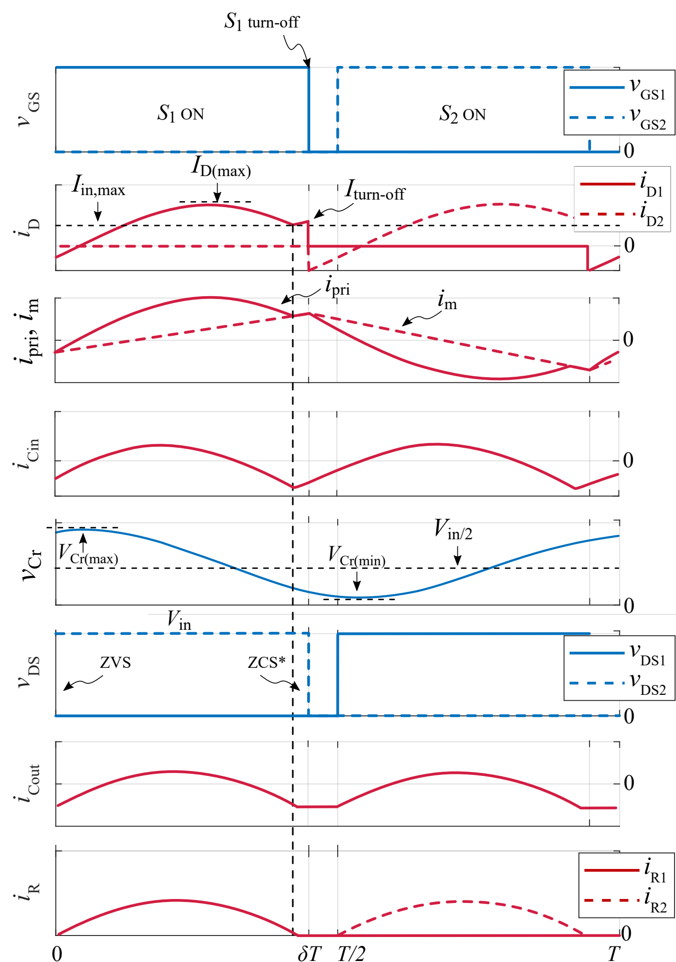


Figure 5.31: LLC resonant half-bridge converter's ideal waveforms, using split capacitors, with $\delta = 45\%$ for each switch, showing gate-source voltage (v_{GS}), drain current (i_D), resonant current (i_{reso}), magnetizing current (i_m), input capacitor's current (i_{Cin}), resonant capacitor's voltage (v_{Cr}), drain-source voltage (v_{DS}), output capacitor's current (i_{Cout}), and output rectifiers' current (i_R).

As illustrated in the waveforms, each switch conducts one half-cycle of the sinusoidal current. When the complementary switch (e.g., S_2) turns off, the circulating current commutates naturally through the body diode of the opposite switch (S_1), thereby discharging its drain-source voltage with minimal losses. This negative current allows S_1 to turn on under zero-

voltage switching (ZVS) conditions. Once the half-cycle is completed, the switch is turned off while its drain current approaches zero. Although this resembles a zero-current switching (ZCS) transition, complete turn-off at zero current is not achievable due to the continuous presence of the magnetising current, which limits the minimum value of i_{pri}.

5.4.2. Resonant tank analysis and optimization

The design of the LLC resonant converter has been extensively addressed in the literature, [125–127]. The most common approach is based on Frequency Domain Analysis (FDA), where the resonant tank components are dimensioned for a given resonant frequency f_{r} and with the desired voltage gain spectrum. This analysis is often fulfilled with the First Harmonic Approximation (FHA), which simplifies the analysis by considering purely sinusoidal waveforms at the fundamental frequency in the primary side, neglecting the rest of the switching harmonics.

While the FHA offers an intuitive starting point for analysis near the resonant frequency, its inherent simplifications can lead to notable inaccuracies when operating across a wider range of the voltage gain curve. Away from the resonant point, current and voltage waveforms progressively deviate from pure sinusoidal shapes, making it increasingly difficult to achieve ZCS and ZVS.

Several Time Domain Analysis (TDA) methods have been proposed, [128–130], enabling more precise waveform estimation and facilitating converter optimization that takes into consideration critical factors such as deadtime and magnetizing current. In the presented study, both methods are analysed and used to design the resonant tank, considering deadtime minimum magnetizing current constraints for the desired application. Overall, the resonant components are selected based on the following targets:

- Maximize magnetizing inductance, L_{m}, to reduce the primary RMS current and the turn-off current, thus reducing conduction and switching losses.
- Minimize resonant inductance, L_{r}, to integrate it within the transformer, and avoid using an extra inductor, reducing cost and improving power density.
- Maximize resonant capacitance, C_{r}, to reduce the voltage stress on individual capacitors.

Frequency Domain Analysis (FDA)

To simplify circuit analysis, the resonant tank of the LLC converter is typically analysed considering only the fundamental harmonic comprising the resonant components L_{m}, L_{r}, and C_{r}. To perform the FHA analysis, the following equivalent simplified circuit is analysed:

The voltage gain K of the full equivalent circuit is extracted and defined in the following equation:

$$K(Q,m,F_{\mathrm{x}}) = |\frac{V_{\mathrm{out,ac}}(s)}{V_{\mathrm{in,ac}}(s)}| = \frac{F_{\mathrm{x}}^2(m-1)}{\sqrt{(mF_{\mathrm{x}}^2-1)^2 + F_{\mathrm{x}}^2(F_{\mathrm{x}}^2-1)^2(m-1)^2Q^2}} \tag{5.24}$$

where,

$$Q = \frac{\sqrt{L_{\mathrm{r}}/C_{\mathrm{r}}}}{R_{\mathrm{ac}}}, \text{ is the quality factor,} \tag{5.25}$$

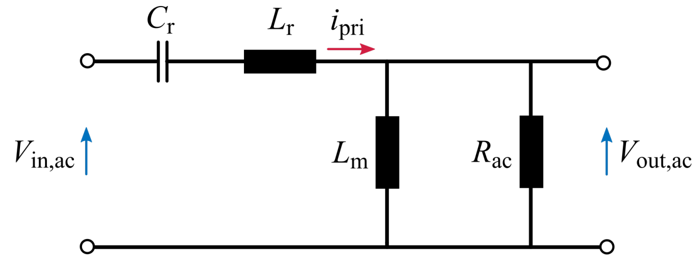


Figure 5.32: The simplified circuit of the LLC resonant converter, comprising the resonant capacitor C_r, resonant inductor L_r and magnetizing inductor L_m.

$$R_{ac} = R_{out} \frac{8N_p^2}{\pi^2 N_s^2}, \text{ is the reflected load resistance,} \tag{5.26}$$

$$F_x = \frac{f_{sw}}{f_r}, \text{ is the normalized switching frequency,} \tag{5.27}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}, \text{ is the resonant frequency,} \tag{5.28}$$

$$m = \frac{L_r + L_m}{L_r}, \text{ is the ratio of total primary inductance to resonant inductance.} \tag{5.29}$$

By defining L_r, L_m and C_r, the converter's gain spectrum is determined. The converter can operate at the same switching frequency as the resonant frequency ($f_{sw} = f_r$), below the resonant frequency ($f_{sw} < f_r$) or above the resonant frequency ($f_{sw} > f_r$), modifying the voltage gain of the converter and therefore achieving output voltage regulation. In case output voltage regulation is required, the gain curve, and therefore, the resonant components, have to be selected accordingly.

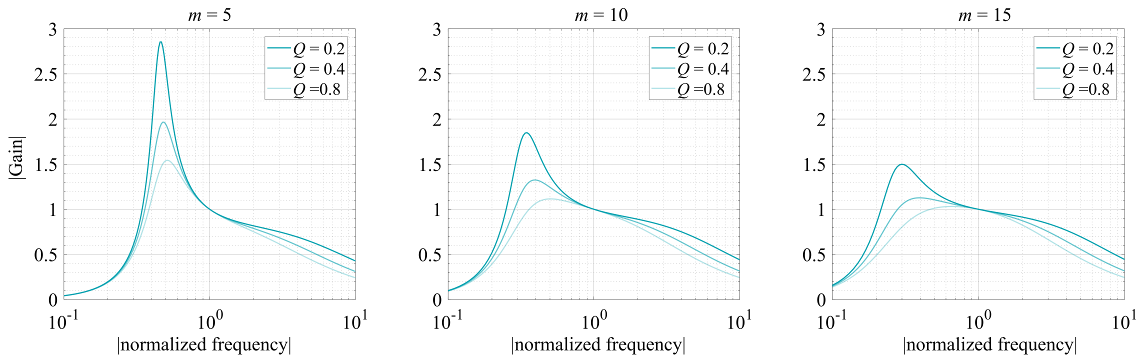


Figure 5.33: Gain spectrum for inductance ratio (m) ranging from 5 to 15, and quality factor (Q) ranging from 0.2 to 0.8.

For this application, where the regulation capability is not the main focus (external regulation by an additional DC/DC converter will be discussed in the future), the converter is designed for $f_{sw} \approx f_r$, optimizing the operation of the switches. For that reason, a tight and unity value gain curve is desired, and the maximization of magnetizing inductance is sought to minimize the magnetizing current, and therefore, the losses. In an ideal scenario with perfect switches, the magnetizing inductance could be maximized to a level just sufficient for the magnetizing current to maintain the flux in the transformer core. However, in practical

implementations with non-ideal switches, the magnetising current assumes a more critical role, particularly in enabling soft-switching conditions. Specifically, it facilitates ZVS during turn-on transitions by generating a negative current that discharges the drain-source voltage of the incoming switch before its turn-on. This negative current mirrors the turn-off current of the complementary switch, flowing in the opposite direction. When the turn-off current is too low, the output capacitance C_{OSS} of the switch cannot be fully discharged within the available deadtime, compromising the ZVS condition.

Consequently, a minimum turn-off current is necessary to ensure that the drain-source voltage reaches zero before the gate signal is applied, [131]. The deadtime dt between the switching events of S_1 and S_2 also plays a crucial role. It must be sufficiently long to allow the complete discharge of the drain-source voltage through the magnetising current, but not so long as to permit the reverse current to reach 0 A and start charging the drain-source voltage again before turn-on. Therefore, achieving reliable ZVS operation requires a careful balance between the magnetising current magnitude and the dead time duration.

Time Domain Analysis (TDA)

The TDA method is employed to facilitate a more detailed optimisation of both the deadtime and the magnetising inductance. The goal of this optimisation is to minimise switching and conduction losses, considering that the primary current is the sum of the resonant and magnetising currents, $i_{\text{pri}} = i_{\text{r}} + i_{\text{m}}$. Assuming that switching occurs when the magnetising current reaches its peak and coincides with the resonant current, the turn-off current can be considered proportional to the magnetising current. The turn-off current must be sufficiently high to discharge the output capacitance of the semiconductors during the deadtime (dt) to achieve ZVS. As a result, the necessary deadtime duration can be considered inversely proportional to the magnitude of the turn-off current. Two boundaries for defining the minimum turn-off current can be identified:

- Lower Boundary: Determined by the need to discharge the output charge of the selected semiconductors, this sets a minimum magnetising current based on the required turn-off current and deadtime.
- Upper Boundary: A large deadtime clips a portion of the resonant current waveform, imposing a second constraint. Below this boundary, the turn-off current is no longer dictated by the magnetising current but rather by the duration of the deadtime itself. This second boundary depends on the clipped portion of the sine wave, therefore, on the switching period.

The first boundary can be calculated using several approximations, and in this case, derived from [126], is calculated by the following equation, which also considers the parasitic capacitances of the output rectifying diodes C_{jd} reflected in the primary side:

$$i_{\text{off(min)}} = 2V_{\text{in}}(C_{\text{OSS}} + 2C_{\text{jd}}N^2)/dt \tag{5.30}$$

The second boundary can be calculated by simply considering a sinusoidal current with the calculated RMS value for the application's requirements, and obtaining the current at which the deadtime clips the waveform:

$$i_{\text{off(min)}} = I_{\text{pri(RMS)}}\sqrt{2}\sin(2\pi f_{\text{r}}t - 4\pi f_{\text{r}}dt) \tag{5.31}$$

This relationship is more intuitively understood with the aid of the following illustration, Fig. 5.34.

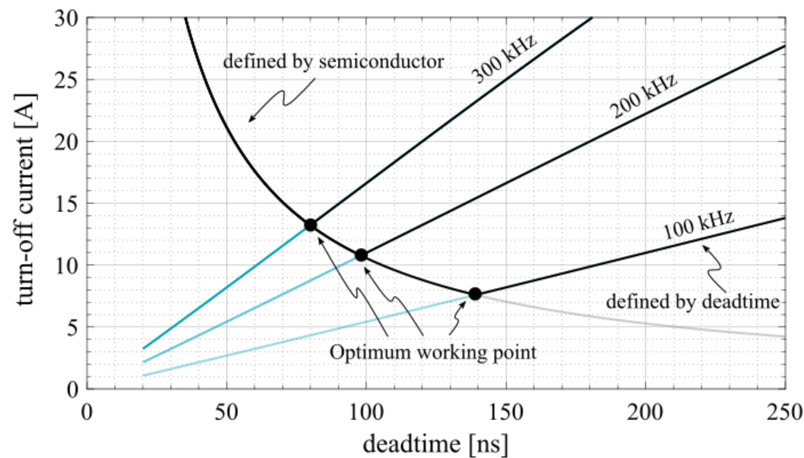


Figure 5.34: Turn-off current definition by semiconductor and deadtime constraints, showing the optimum working conditions for the desired application switching at 100 kHz, 200 kHz, and 300 kHz

The figure illustrates the minimum achievable turn-off current, and consequently the peak magnetising current, at three different switching frequencies for the intended application. Although increasing the deadtime reduces the current required to discharge the semiconductor's output capacitance, it also clips the sine waveform, creating a positive slope that leads to an optimal point where both effects intersect. This clipping is more pronounced as the resonant frequency increases, additionally increasing the minimum turn-off current. At this intersection, the peak magnetising current is known, allowing the maximum magnetising inductance to be calculated as:

$$L_{\mathrm{m(max)}} = \frac{N V_{\mathrm{out}}}{4 i_{\mathrm{off(min)}} f_{\mathrm{sw}}}. \tag{5.32}$$

This inductance is computed individually for each switching frequency and, as discussed in the following section, for each semiconductor under study. Once the minimum required magnetising inductance is determined, the resonant inductance and capacitance are calculated using the FHA. An inductance ratio $m = 16$ is selected as suitable for integrating the resonant inductance as part of the transformer ($L_{\mathrm{r}} < 200$ nH for all switching frequency range). From the selected inductance ratio, the resonant inductance L_r is derived. Subsequently, the quality factor Q and the resonant capacitance C_r are calculated to achieve the desired resonant frequency.

5.4.3. Semiconductor selection

Following the analysis of the maximum allowable magnetising inductance and the required deadtime, various semiconductor models are compared using the modelling framework developed in Chapter 3. In this half-bridge configuration, high RMS currents are expected, suggesting that conduction losses will dominate the overall loss profile. Consequently, even small differences in $R_{\mathrm{DS(on)}}$ (in the milliohm range) can significantly influence device selection, favouring chips with the lowest on-state resistance. However, low-ohmic GaN HEMTs

remain limited in availability and are not yet as commercially widespread as Silicon MOSFETs. Additionally, even within Silicon technologies, $R_{DS(on)}$ values are not fully standardised across manufacturers. To enable a fair comparison between different device technologies for the intended application, generic semiconductor models have been created following the procedure described in Chapter 3.

The selected generic models are 80 V Silicon MOSFETs, and 100 V GaN HEMTs, with $R_{DS(on)}$ values ranging from 1 mΩ up to 3 mΩ. First, the minimum turn-off current for each semiconductor is approximated by equation 5.30, where the output rectifiers' parasitic capacitance (C_{jd}) is considered to be 30 pF. The data for these semiconductors is listed in the following table 5.11.

Table 5.11: Transistor comparison for the presented LLC resonant converter

	Tech.	$R_{DS(on)}$	C_{OSS}	Package	u. cost per 1000u
Case 1A	Si MOSFET	1 mΩ	2660 pF	QFN	1.69 €
Case 2A	Si MOSFET	2 mΩ	1550 pF	QFN	1.08 €
Case 3A	Si MOSFET	3 mΩ	913 pF	QFN	0.702 €
Case 1B	GaN HEMT	1 mΩ	940 pF	QFN	5 €
Case 2B	GaN HEMT	2 mΩ	690 pF	QFN	3 €
Case 3B	GaN HEMT	3 mΩ	514 pF	QFN	1.5 €

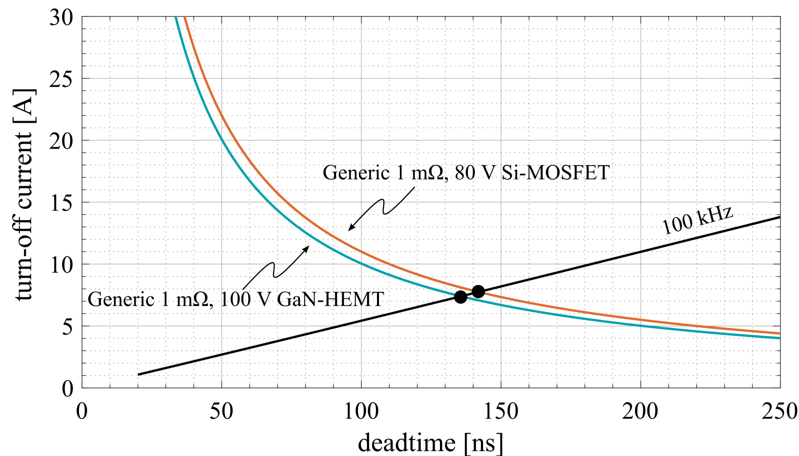


Figure 5.35: Turn-off current definition by semiconductor and deadtime constraints, showing the optimum working conditions for an 80 V generic Si-MOSFET, and a 100 V generic GaN HEMT, application switching at 100 kHz.

It can be observed in Fig. 5.35 that the difference in the minimum allowable turn-off current between the two technologies is not particularly significant. The GaN HEMT allows for a slightly lower turn-off current, and consequently a reduced magnetising current, due to its smaller output capacitance, C_{OSS}. As stated before, the switching frequency also affects the minimum achievable turn-off current, increasing with it, Fig. 5.36. But the difference between GaN and Silicon is still very small.

However, to accurately capture the technological advantage, the switching losses associated with this turn-off current must also be assessed. This aspect is expected to further widen the performance gap between GaN HEMTs and Silicon MOSFETs. After calculating the optimum working point for each generic semiconductor listed in Table 5.11, their models are generated, and the Double Pulse Test (DPT) model is employed to obtain their switching losses for all the

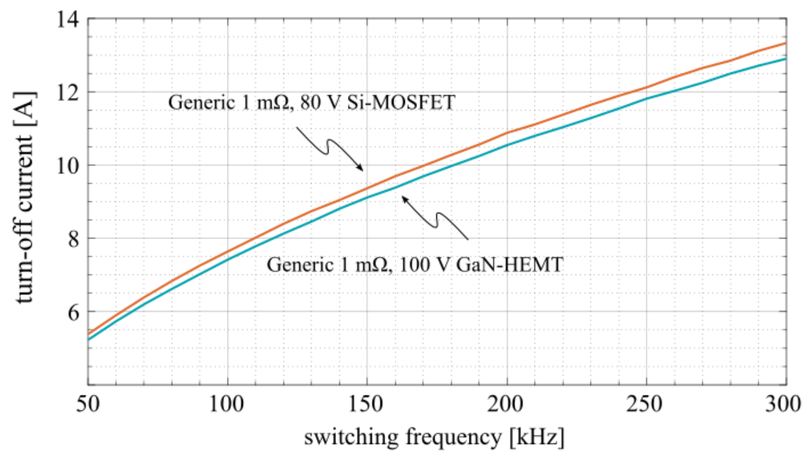


Figure 5.36: Minimum turn-off current by semiconductor and deadtime constraints, showing the optimum working conditions for an 80 V generic Si-MOSFET, and a 100 V generic GaN HEMT, at different switching frequencies.

desired switching frequency range. Besides the switching and conduction losses, the deadtime losses are also included. As the optimum deadtime period for each case is known, the nominal reverse voltage drop is estimated (body diode drop for Si-MOSFETs, threshold voltage for GaN HEMTs), and multiplying it by the current shape during the deadtime, the losses of this period are calculated. In this context, the GaN HEMTs are expected to generate more losses than Si-MOSFETs during the deadtime. Therefore, the optimization of deadtime for GaN devices is critical.

Once the semiconductor losses are calculated, the corresponding area for heat dissipation via PCB is calculated, following the same steps as in the case of the GaN-based push-pull converter, equation 5.15.

5.4.4. Transformer design

The high-frequency transformer in the resonant LLC converter must be designed to meet the specified values of the resonant inductance L_r and the magnetising inductance L_m. Among these, the magnetising inductance is determined first, as it directly influences the minimum achievable turn-off current. This inductance depends primarily on the magnetic core material and the number of primary turns. To facilitate its calculation, ferrite core manufacturers typically provide the inductance factor A_L, allowing L_m to be estimated using:

$$L_\mathrm{m} = A_\mathrm{L} N_\mathrm{p}^2 \tag{5.33}$$

In this design, high primary currents are expected, which would result in significant conduction losses due to winding resistance. To minimise these losses, the number of primary turns N_p is kept as low as possible. However, a minimum number of turns must be maintained to prevent magnetic core saturation. For ferrite cores, the peak magnetic flux density B_max is generally maintained within the range of 50 mT to 200 mT. The peak flux density can be estimated as follows, [116]:

$$B_\mathrm{max} = \frac{V_\mathrm{in}\delta}{4 N_\mathrm{p} A_\mathrm{e} f_\mathrm{sw}}. \tag{5.34}$$

Here, A_e is the effective cross-sectional area of the core, which depends on its geometry. Considering the application constraints, a fixed number of primary turns, $N_p = 3$, is selected for all analysed cases. For each core size under consideration, the magnetic flux is evaluated under worst-case conditions, specifically, the highest input voltage ($V_{\text{in}} = 28$ V), and across the range of switching frequencies. In some cases, particularly at lower switching frequencies and small A_e values, the resulting peak flux density exceeds the allowable limit. These frequency values are therefore discarded for the corresponding core size. This approach simplifies the design process while ensuring the maximum flux density remains safely below 200 mT. With the number of turns fixed, the desired magnetising inductance L_m is achieved by selecting a core with a suitable A_L value. Many ferrite core families offer a wide range of A_L values, typically adjusted by varying the air gap between the core halves. Following a comprehensive market survey, the N87 material from TDK/EPCOS has been selected as the most suitable option for this application, given its favourable magnetic properties and availability across a broad range of A_{L} values.

From the specification datasheet of the material, the coefficients K, α, and β are obtained to calculate the core losses in kW, given by

$$P_{\text{c}} = VP_{\text{cv}} = VKB_{\text{max}}^{\beta} f_{\text{sw}}^{\alpha} \quad (5.35)$$

where, V is the volume of the transformer's core. The results are further verified with MagNet Challenge data [120]. In contrast to hard-switching converters, this soft-switching topology produces near-sinusoidal waveforms with minimal ringing and high-frequency oscillations, which significantly reduces the potential for high-frequency AC winding losses. Consequently, only winding losses related to fundamental frequency are considered in the calculation of primary winding losses.

$$P_{\text{w}} = P_{\text{w-dc}} + P_{\text{w-ac}}. \quad (5.36)$$

To further ensure that the AC effects (proximity, skin effect) generate minimal losses, Litz wire is used for the winding construction. The wire's characteristics, including the number of strands, optimal strand diameter, and DC and AC losses, are determined according to the guidelines in [132], ensuring that approximately 25% of the core's window area is occupied by copper.

The core and winding losses are calculated for the entire studied frequency range, considering various transformer sizes. They are listed in the following table, also with their volume and cost as of June 2025.

Table 5.12: Candidate cores for the resonant LLC converter

	Effective area, A_{e}	Effective volume, V	Material	u. cost per 1000u
EFP 20/10/7	31 mm^2	1460 mm^3	N87	0.39 €
EFP 25/13/9	58 mm^2	3310 mm^3	N87	0.6 €
EFP 30/15/9	69 mm^2	4690 mm^3	N87	0.73 €
E 20/10/6	32.1 mm^2	1490 mm^3	N87	0.33 €
E 25/13/7	60 mm^2	4000 mm^3	N87	0.33 €
E 30/15/7	130 mm^2	5390 mm^3	N87	0.54 €

The unit cost is updated from Octopart (June, 2025).

5.4.5. Multi-objective design

Once the transformer design and the switching behaviour of the power devices have been addressed, the power losses, cost, and volume of the transformer and primary switches are estimated across the considered switching frequency range. The input and output capacitors are dimensioned by calculating the charge required to meet the voltage ripple specifications of the application (see waveforms in Fig. 5.31). The resonant capacitor values are derived using FHA, based on the selected magnetising inductance, inductance ratio m, and target resonant frequency f_r. As in the push-pull converter analysis, cost and volume models are generated for both ceramic and film capacitors. For the resonant capacitors, 63 V-rated film capacitors are considered. The magnetising and resonant inductors are assumed to be integrated into the transformer, and therefore do not contribute additional cost or volume. The results for minimum input voltage conditions $V_{in} = 20$ V (which is considered the worst-case in terms of total losses), are presented in Fig. 5.37, showing power losses versus volume (a) and power losses versus cost (b).

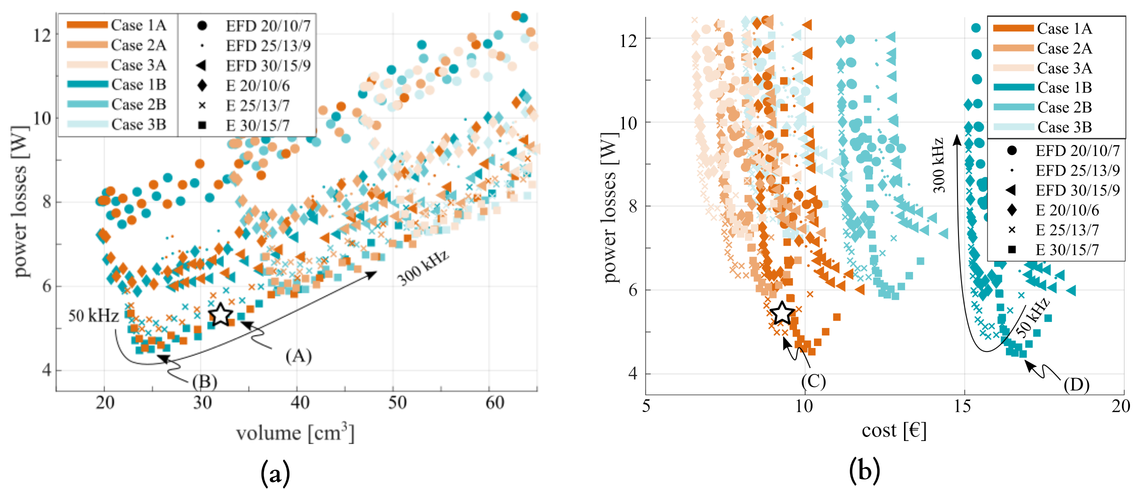


Figure 5.37: Power losses vs volume (a) and power losses vs cost (b) for six different core sizes, and six different GaN and Si generic semiconductors. Volume and cost of resonant, input, and output capacitors are also included in the analysis.

The analysis of power losses versus volume indicates that the advantages offered by GaN HEMTs in the considered application are limited, as shown by point (B ≡ D). In this specific use case, power losses are predominantly resistive, while switching losses represent only a minor fraction. As such, the benefits of GaN technology, higher switching speed and reduced switching losses, are marginal and do not justify their integration. Even if turn-off losses are smaller than with Silicon MOSFETs, this advantage is offset by increased deadtime-related losses. Moreover, the minimum allowable deadtime (stated by equation 5.30) limits further reduction, and, as a result, the estimated optimum switching frequency is similar for both technologies. Furthermore, the power losses versus cost comparison highlights that leveraging the minor efficiency improvements offered by GaN HEMTs comes at a substantial cost increase, as illustrated in point (D ≡ B). In addition, low-resistance GaN HEMTs (e.g., 1 mΩ) are rarely available on the market, whereas Silicon MOSFETs with comparable $R_{DS(on)}$ values are widely accessible.

Among the evaluated core geometries, the best results are achieved using E30/15/7 core sets, indicated with points (A) and (C ≡ A). Based on these findings, the half-bridge LLC

converter is constructed using 80 V Silicon MOSFETs and E30/15/7 cores made of N87 ferrite material. One available Silicon MOSFET with $R_{DS(on)} \approx 1$ mΩ is the IAUCN08S7N013 from Infineon, which offers 1.16 mΩ typical, 1.3 mΩ maximum conduction resistance. The chosen switching frequency is approximately 130 kHz. At the targeted design point, the total power losses of the analysed components, including GaN switches, passive elements, and magnetic components, are estimated to be 5.2 W, with a compact volume of 32 cm^3 and an approximate cost of 9.5 €.

To achieve the required magnetising and leakage inductances, the transformer is built using a B66319G500X187 gapped half and a B66319G0000X187 ungapped half, resulting in an A_L value of 145 nH/n^2. With $N_p = 3$ turns, this yields an estimated magnetising inductance of 1.3 μH. To maintain an inductance ratio of $m = 16$, the resonant inductance must be approximately 86 nH. Accordingly, the resonant capacitor required to achieve a resonant frequency of 130 kHz, based on FHA, is around 16 μF.

5.4.6. 300 W prototype design validation

To validate the design method of the resonant LLC half-bridge converter, a prototype is constructed based on the requirements established in Table 5.10. First, the high-frequency transformer is constructed, and its main parameters are validated. For the primary and secondary windings, Litz wire is used. The magnetizing inductance and leakage inductance are measured and validated with Bode 100 VNA. Main specifications of the constructed converter are presented in Table 5.13.

Table 5.13: Si-based resonant LLC prototype specifications and main components

Component	Name	Specifications
Transistors	IAUCN08S7N013	100 V, 1.3 mΩ max. Si MOSFET
Output diodes	C6D04065E	600 V, 4 A SiC Schottky
Transformer core	E38/8/25, N87	1.44-1.35 μH @ 100 kHz-10 MHz
Transformer wind.	38 AWG Litz wire	90-80 nH @ 100 kHz-10 MHz
Controller	ICE2HS01G	1 MHz resonant mode controller
Thermal pad	-	900 mm^2, 30 vias per transistor
Input capacitor	C1206X105K1RACAUTO	50 V rated 2.2 μF x10
Resonant capacitor	B32529C105K189	63 V rated 1 μF x16
Output capacitor	C1210X104KBRACAUTO	630 V rated 0.1 μF x2

The constructed prototype is shown in Fig. 5.38, with a total footprint of 130 × 60 mm and a height of 20 mm, constrained by the transformer. The resulting power density is 1.92 W/cm^3. The total cost of the magnetic components, capacitors, and semiconductors, including the MOSFETs and rectifier diodes, is estimated at 9.5€. The control of the converter is performed by ICE2HS01G controller, which has a minimum deadtime of around 120 ns.

Main waveforms of the converter have been measured working under the most critical conditions (V_{in} = 20 V, P_{out} = 300 W). The measured waveforms are shown in Fig. 5.39. The primary current is measured with a Rogowski coil surrounding the primary winding of the transformer. The sinusoidal waveform demonstrates that the converter is working very close to the resonant frequency of 130 kHz.

If the waveform is zoomed in, the switching transition can be observed. The deadtime of the controller is configured to the minimum value of 120 ns. Fig. 5.40 shows how the deadtime is just sufficient to avoid cross conduction and to achieve soft-switching. The turn-off current is between 8 to 10 A, as estimated.

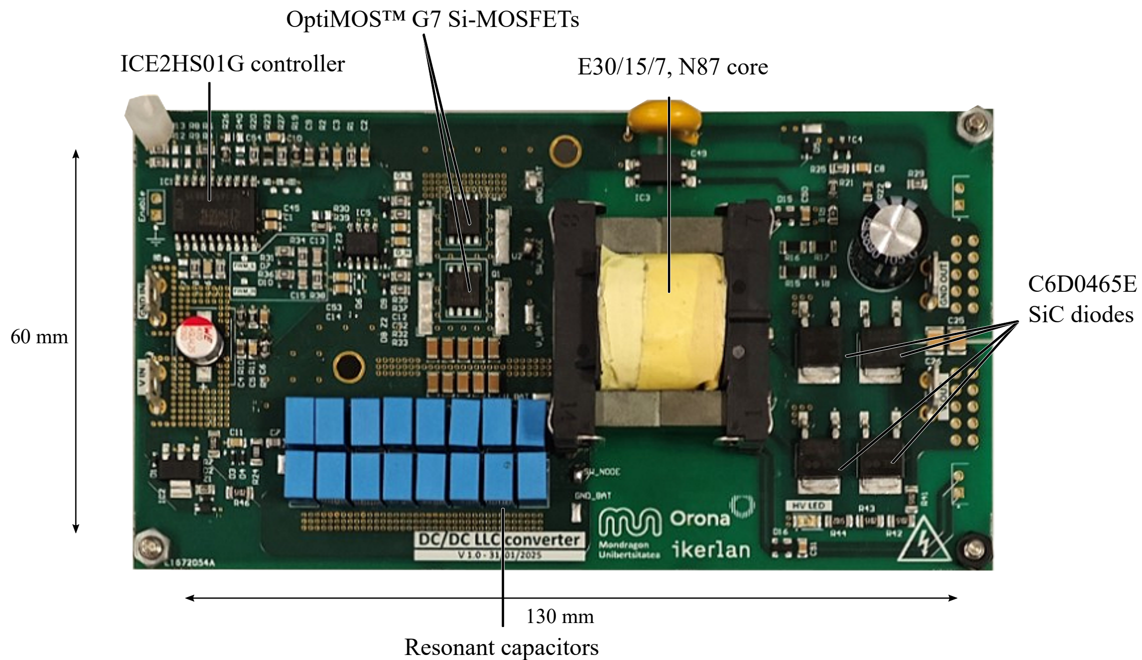


Figure 5.38: The 300 W Si-based resonant LLC prototype. The prototype is 130 mm in length and 60 mm in width. The core is 20 mm in height.

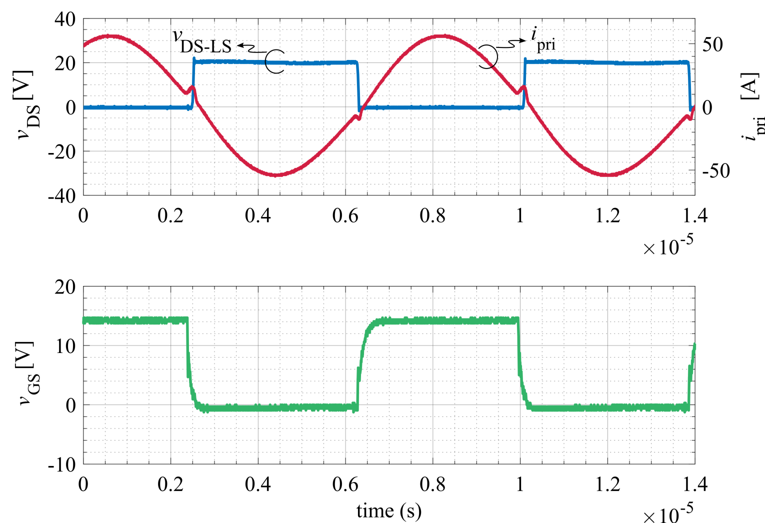


Figure 5.39: Experimental waveforms of drain-source voltage v_{DS} and drain current i_D of a single switch, and the gate-source voltage v_{GS}, working at 130 kHz and 300 W output power.

The efficiency of the converter was measured using a YOKOGAWA wattmeter, and the results are presented in Fig. 5.41. Measurements were carried out at three different input voltages: 20 V, 24 V, and 28 V. The lowest efficiency, 93.7%, was recorded at an input voltage of 20 V, under nominal load conditions ($P_{out} = 300$ W). This result is attributed to increased conduction losses, which dominate at high power levels and become more pronounced when the input voltage is reduced. Conversely, the highest efficiency of 95.7% was achieved at the maximum input voltage of 28 V. As previously observed in the GaN-based push-pull converter, at lower output power levels, core losses become a more significant contributor to

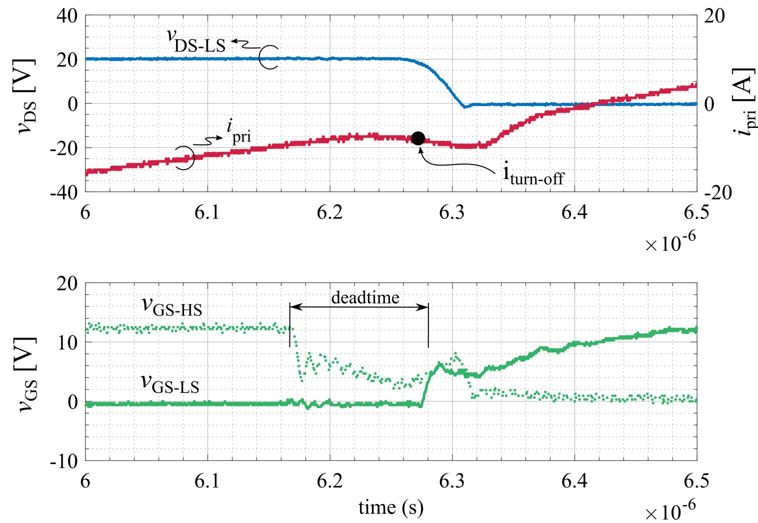


Figure 5.40: Experimental waveforms of drain-source voltage v_{DS} and drain current i_D of a single switch, and the gate-source voltage v_{GS} of both switches, during turn-on of low-side switch.

the total losses. In such cases, maximum efficiency tends to occur at lower input voltages.

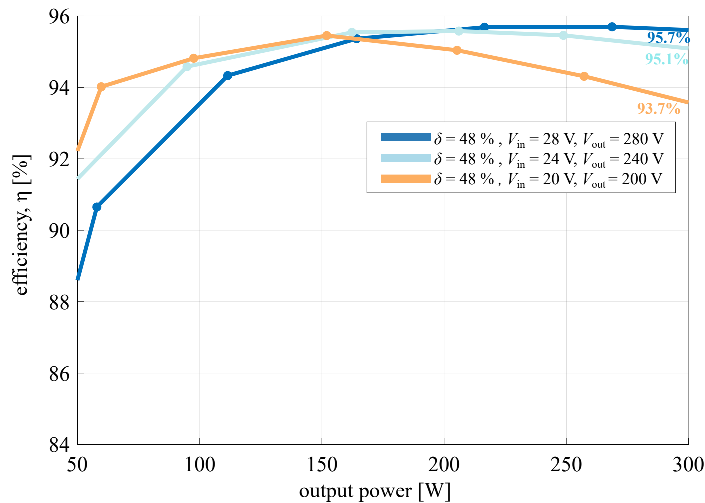


Figure 5.41: Measured efficiency of the experimental prototype, working at different input voltages, and power ranging from 50 W to 300 W. The operating frequency is 130 kHz and 48% duty cycle.

Compared to the GaN-based push-pull converter, the designed Si-based resonant LLC converter achieves approximately 2% higher efficiency under nominal operating conditions ($V_{in} = 24$ V, $P_{out} = 300$ W). This improvement is primarily attributed to the soft-switching nature of the LLC topology, along with the carefully tuned deadtime and magnetising current, which provide notable advantages when operating close to the resonant frequency. However, it is important to note that the regulation capability of the LLC converter has been intentionally excluded from this study. In this context, the GaN-based push-pull converter could potentially outperform the Si-based counterpart due to its better performance under hard-switching conditions when regulation is required. In terms of volume and cost, the Si-based LLC converter comprises 25% higher volume due to the non-planar high-frequency transformer's

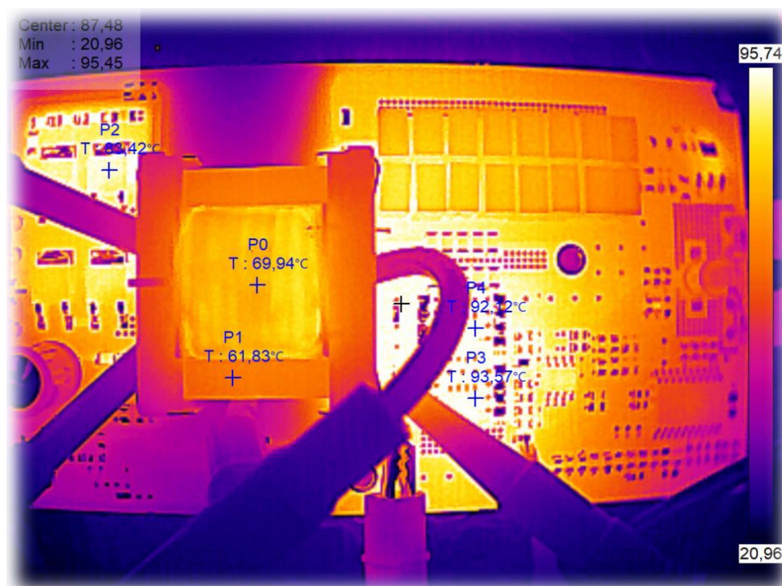


Figure 5.42: The 300 W Si-based resonant LLC half-bridge converter's steady-state thermal capture obtained with a TE-Q1 thermal camera. The converter is working at 130 kHz, 24 V input voltage, and 300 W output power.

height. But considering the cost, the LLC converter is 25% cheaper than its GaN-based push-pull counterpart.

The thermal image of the prototype, shown in Fig. 5.42, illustrates the temperature distribution among the components. The highest measured temperature reaches 93.57 °C at the switches under steady-state operation.

5.4.7. Discussion

To enable a broader comparison of semiconductor technologies and DC/DC converter topologies within the context of the target application, a resonant LLC half-bridge converter with split-capacitor configuration is analysed. This topology, known for its sinusoidal waveforms and intrinsic soft-switching capability, offers an interesting alternative to the previously studied hard-switched push-pull converter, particularly for evaluating the integration of GaN devices. At the specified power and performance levels, the required low $R_{DS(on)}$ values are challenging to find with commercially available GaN HEMTs. In contrast, Silicon MOSFETs, benefiting from their technological maturity, offer wider availability for those resistance values, and more competitive pricing. As a result, the advantages of GaN in soft-switching applications are not always decisive, and a more comprehensive evaluation of performance, availability, and cost is essential for optimal technology selection.

The LLC converter is first analysed in the frequency domain using FHA to size the resonant components. However, due to the limited accuracy of this method in capturing non-ideal effects, a complementary time-domain analysis is performed. This analysis focuses on optimising the magnetising inductance and deadtime over a switching frequency range of 50–300 kHz. Generic GaN and Si devices with low $R_{DS(on)}$ values (1 mΩ, 2 mΩ, and 3 mΩ) are evaluated. The study reveals the existence of an optimal operating point where the trade-off between turn-off current and deadtime minimises overall losses. Using the

DPT-based modelling tool presented earlier, a multi-objective comparison is conducted across passive components, semiconductors, and transformer geometries. Results show that Silicon MOSFETs not only deliver performance comparable to GaN HEMTs in terms of power losses but also represent a significantly more cost-effective solution. Furthermore, the limited market availability (at the time analysis was carried out, June 2025) of sub-1 mΩ GaN devices reinforces the decision to proceed with a Silicon-based implementation.

A resonant LLC half-bridge prototype is therefore developed using 80 V Silicon MOSFETs (Infineon IAUCN08S7N013, $R_{DS(on)} = 1.16$ mΩ) and E30/15/7 cores with N87 ferrite material. The transformer is constructed using a B66319G500X187 gapped half and a B66319G0000X187 ungapped half, yielding an A_L of 145 nH/n^2, which results in a magnetising inductance L_m of 1.3 μH for $N_p = 3$. To maintain an inductance ratio $m = 16$, the resonant inductance is set to 86 nH, and the required resonant capacitor (calculated for a resonant frequency of 130 kHz) is approximately 16 μF. Experimental validation confirms the design methodology, resonant tank sizing, and optimal operating conditions. The prototype achieves 95.1% efficiency under nominal conditions (V_{in} = 24 V, V_{out} = 240 V, P_{out} = 300 W), with measured waveforms closely matching estimated results and demonstrating successful deadtime and turn-off current minimisation. The total cost of the main components is estimated at 9.5€, while the measured volume of the prototype is approximately 156 cm^3. The benefits of the present design also leave open the possibility of adding a secondary, non-isolated DC/DC stage to introduce regulation functionality if required.

The converter is driven by the Infineon ICE2HS01G controller, which supports a minimum deadtime of 120 ns. While suitable for Silicon MOSFETs, this deadtime limit poses a constraint when operating at higher frequencies or when integrating faster GaN devices. The analysis confirms that optimal deadtime values for GaN can fall below 100 ns thresholds, which are beyond the capability of most commercial controllers, thus limiting potential performance improvements. Although GaN devices currently face limitations in cost and availability for studied $R_{DS(on)}$ sizes, ongoing developments suggest that more affordable and available GaN solutions will soon enter the market. These emerging devices could enable further magnetising current optimisation and offer substantial advantages in scenarios requiring hard-switching performance or regulated outputs.

5.5. Buck Converter Design

The cost and efficiency benefits demonstrated by the proposed silicon-based resonant LLC converter, in comparison with the baseline silicon-based push-pull converter, offer sufficient headroom to incorporate an additional non-isolated step-down stage. This auxiliary converter enhances the overall system functionality by enabling flexible output regulation, reduced voltage stress on downstream components, and improved compatibility with varying load conditions. When integrated alongside the LLC converter, this additional stage provides significant performance gains within the target application, surpassing the baseline architecture.

Among the various non-isolated step-down topologies available, the buck converter stands out due to its simplicity, robustness, and high efficiency. Two configurations are considered: the single-switch (asynchronous) buck and the synchronous buck converter. While the single-switch design offers minimal component count and reduced control complexity, the synchronous version achieves superior efficiency by eliminating the freewheeling diode losses. For this reason, the synchronous buck converter is selected for this design.

The converter is designed to regulate the LLC output voltage (200 ... 280 V) within a range of 100 V to 200 V. To guarantee reliable performance under all operating conditions, it is dimensioned based on worst-case scenarios. This design strategy ensures predictable thermal behaviour, which is essential for operation in high-reliability environments.

The key design specifications for the synchronous buck converter are summarised in Table 5.14.

Table 5.14: Requirements for the designed Si-based Buck converter

Parameter	Symbol	Value
Input voltage	V_{in}	200 V ... 300 V
Output voltage	V_{out}	100 V ... 190 V
Output power	P_{out}	**300 W**
Maximum inductor ripple	ΔI_{out}	$<$ **70%** of I_{out}
Maximum input voltage ripple	ΔV_{in}	$<$ **10%** of V_{in}
Maximum output voltage ripple	ΔV_{out}	$<$ **10%** of V_{out}
Switching frequency	f_{sw}	100 - 300 kHz

5.5.1. Continuous Conduction Mode buck converter

Buck converters can be configured to operate either in Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM), depending on the current ripple through the output inductor, L_{out}. The configuration of a synchronous switch is shown in Fig. 5.43.

In DCM, the inductor current decreases to zero during part of the switching cycle, typically when the low-side switch is reverse conducting (or its body diode is conducting in the case of asynchronous topologies). This results in the high-side switch turning on under ZCS conditions, which reduces switching losses and EMI.

During DCM operation, the low-side switch (or diode in case of asynchronous configuration) conducts in reverse direction once the high-side switch turns off, allowing the inductor to transfer its stored energy to the load. This condition persists until the inductor current naturally decays to zero, after which a brief idle period may occur before the next switching cycle begins.

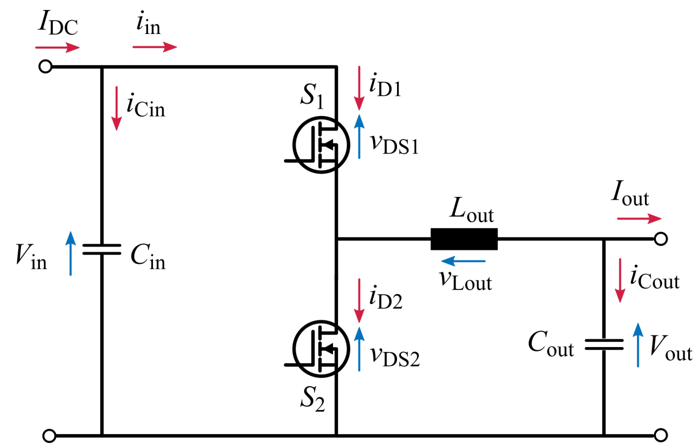


Figure 5.43: The simplified circuit of the Buck converter, with the main primary switches S_1 and S_2, the input capacitor C_{in}, the output inductor L_{out}, and the output capacitor C_{out}.

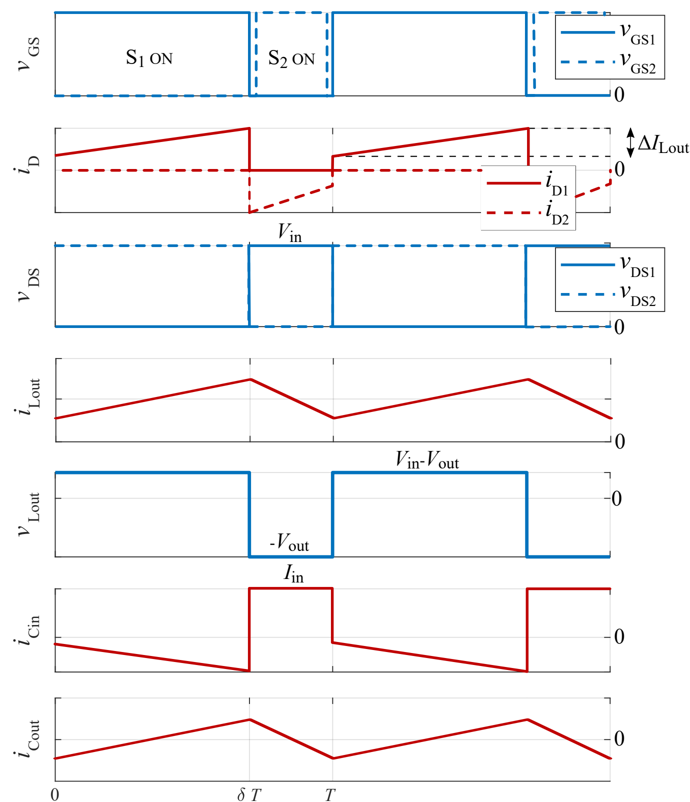


Figure 5.44: Buck converter's ideal waveforms in CCM operation, with $\delta = 70\%$ for each switch, showing gate-source voltage (v_{GS}), drain current (i_D), drain-source voltage (v_{DS}), output inductor's current (i_{Lout}), voltage (v_{Lout}), input capacitor's current (i_{Cin}), and output capacitor's current (i_{Cout}) .

In contrast, when the converter operates in CCM, the inductor current never reaches zero, ensuring continuous energy transfer throughout the entire switching cycle. In this mode, the ZCS advantage for the top-side switch is lost, as it must always turn on under a non-zero current. However, CCM operation offers several important benefits: it leads to reduced peak currents, smaller current ripple, and lower core losses in the magnetic components. Most notably, it simplifies the control design, especially under varying load conditions, by avoiding the need for mode transition management and ensuring predictable dynamic behaviour. The

typical voltage and current waveforms of a synchronous buck converter operating in CCM are illustrated in Fig. 5.44. These waveforms correspond to the steady-state regime.

For the aforementioned reasons, and taking into account the worst-case operating conditions of the target application, the buck converter is intentionally designed to operate in CCM across the entire load range. This decision ensures stable dynamic behaviour, avoids the complexities associated with mode transitions, and facilitates simplified control implementation.

The relationship between the input and output voltages of an ideal buck converter, following the nomenclature adopted in Fig. 5.43, is directly determined by the duty cycle δ, as described by:

$$V_{\text{out}} = \delta V_{\text{in}}, \tag{5.37}$$

This expression reveals that the output voltage is linearly proportional to the input voltage, scaled by the duty cycle. Consequently, the minimum required duty cycle occurs under the condition of maximum input voltage and minimum output voltage. For the present application, the worst-case combination corresponds to an input voltage of 280 V and an output voltage of 100 V, yielding a duty cycle of approximately $\delta = 0.357$.

5.5.2. Multi-objective design

Once the operation mode of the buck converter is defined, various power switches are compared, and along with the analysis of the passive components, the most suitable switching frequency is selected, considering losses, volume, and cost. All passives are sized to fulfil the requirements in the worst-case scenario, and their cost and volume are calculated following the same procedure as employed with the push-pull and the half-LLC converters. For the power switches, three 650 V GaN Schottky Gate Transistor (SGT)s and a SiC MOSFET are considered, which are listed in the following table with their estimated cost.

Table 5.15: Transistor comparison for the presented LLC resonant converter

	Tech.	$R_{\text{DS(on)}}$	C_{OSS}	Package	u. cost per 1000u
GS-065-018-2-L	GaN HEMT	78 mΩ	34 pF	QFN	4.19 €
GS-065-011-6-L	GaN HEMT	125 mΩ	20 pF	QFN	1.98 €
GS-065-011-1-L	GaN HEMT	150 mΩ	20 pF	QFN	2.23 €
IMT65R107M1H	SiC MOSFET	107 mΩ	58 pF	QFN	3.17 €

For this application, where the high-side switch works under hard-switching conditions, WBG can provide clear advantages over silicon semiconductors, improving efficiency and thermal performance. The power losses for the listed semiconductors are calculated using the developed analytical model in Chapter 4. The required PCB area to dissipate the losses, including the low-side (soft-switching) switch losses, is calculated based on the same principle followed in previous designs. The sum of power losses, volume, and cost of both power switches, input and output capacitors, and output inductor, are shown in Fig. 5.45.

Based on the results, the best performance in terms of power losses and converter volume is achieved with the GaN HEMT featuring the highest $R_{\text{DS(on)}}$ among the evaluated devices, that is, the GS-065-011-1-L from Infineon. Interestingly, the next chip size in the series delivers comparable results, suggesting that the optimal $R_{\text{DS(on)}}$ for this application lies within the tested range. From a power loss and cost perspective, the 125 mΩ_{typ} GaN HEMT emerges as

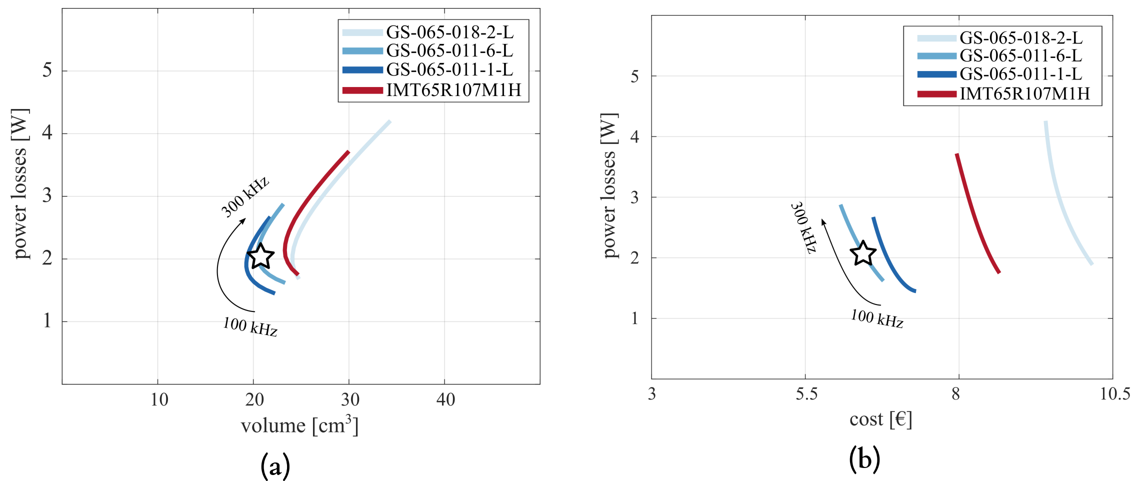


Figure 5.45: Power losses vs volume (a) and power losses vs cost (b) for three different GaN HEMTs and a SiC MOSFET. Volume and cost of input, output capacitors, and output inductor are also included in the analysis.

a more cost-effective option. However, this cost figure should be interpreted with caution, as GaN HEMT pricing continues to evolve rapidly with the introduction of newer generations.

The device with the lowest $R_{DS(on)}$ demonstrates that further reduction in this parameter does not lead to better performance in this application, neither in terms of cost nor the combined losses-volume trade-off. While the SiC MOSFET also offers competitive performance regarding losses and volume, its cost-effectiveness remains inferior to that of the GaN-based solutions.

Finally, the design based on 125 $m\Omega_{typ}$ GaN HEMTs is selected. Operating at approximately 170 kHz, the total power losses of the switching devices remain around 2 W under the defined worst-case scenario, corresponding to an overall efficiency of roughly 99%. The total volume of the power stage is estimated at around 20 cm^3 ($\approx$ 4 cm length, 5 cm width, and 1 cm height), with a semiconductor and passive component cost close to 6€. To further enhance robustness, the use of GaN Gate Injection Transistor (GIT)s, available with comparable $R_{DS(on)}$ values, emerges as a promising alternative. As analysed in Chapter 3, these next-generation devices could not only improve reliability but also reduce the overall cost of the buck converter design.

5.5.3. Discussion

Following the design of the silicon-based resonant LLC converter, regulation functionality is studied by integrating a GaN-based buck converter into the overall solution. This non-isolated stage enables output voltage control within the range of 200 V to 100 V. For this application, 650 V GaN and SiC switches are evaluated through a multi-objective analysis. Among the candidates, 125 mΩ GaN HEMTs demonstrate superior performance in terms of efficiency, volume, and cost. A switching frequency of 170 kHz is selected as the optimal design point.

The GaN devices under evaluation, based on the SGT structure, could be replaced by GaN GITs with comparable $R_{DS(on)}$ values. From a technological standpoint, GaN GITs provide enhanced robustness while maintaining the characteristics of pure GaN HEMTs. As discussed in Chapter 3, next-generation GaN technologies could offer further improvements

in reliability and, as observed in the current market landscape, also contribute to a more cost-effective implementation of the buck stage.

In overall terms, combining the results obtained from the GaN-based buck converter with the experimental data from the resonant LLC stage indicates that the total power losses, considering all semiconductors and main passive components, remain below 17 W under nominal conditions (V_{in} = 24 V, V_{out} = 200 V, P_{out} = 300 W), and below 21 W under worst-case scenarios (V_{in} = 20 V, V_{out} = 100 V, P_{out} = 300 W). These figures correspond to theoretical efficiencies of approximately 94.3% for the application's nominal conditions and 93% under worst-case scenarios.

Regarding cost, the total estimated expense for the main components of the combined converter is around 15.5 €. However, this cost differential is expected to decrease with the ongoing reduction in GaN device prices as newer generations are commercialised. Furthermore, alternative configurations such as an asynchronous buck stage may offer opportunities to further reduce system cost while preserving most of the benefits of the combined approach, although with a slight reduction in efficiency.

In terms of volume, the proposed solution is relatively compact, achieving a combined volume of 176 cm^3. Thanks to the lower thermal dissipation requirements, the bulky heatsink needed in the baseline converter can be eliminated. As a result, the total volume could be reduced, enabling easier integration in space-constrained applications.

Finally, it should be noted that the proposed experimental design for the buck stage has not yet been materialized. It is included in the future lines of the project.

5.6. Solution Comparison

To conclude this chapter, the key performance indicators of the proposed solutions for the studied low-power DC/DC case study are gathered and compared to provide a concise summary of the results. This comparative analysis aims to highlight the respective advantages and limitations of each converter solution, offering a final assessment of the most suitable technologies and topologies for the application.

5.6.1. Si-based push-pull converter (Baseline)

The baseline converter, analysed in Chapter 3 and employed to validate the developed modelling tool, was designed before the work presented in this thesis. This push-pull converter operates over a variable input voltage, V_{in}, range of 20 V to 28 V (nominal value of 24 V) and regulates the output voltage, V_{out}, between 200 V and 100 V.

Under nominal conditions (V_{in} = 24 V, V_{out} = 200 V, P_{out} = 300 W), the converter achieves an efficiency of 91%. However, when output regulation is required, the efficiency drops significantly, down to 89% in light regulation conditions (V_{in} = 24 V, V_{out} = 170 V, P_{out} = 300 W), and to 79.5% in worst-case conditions (V_{in} = 20 V, V_{out} = 100 V, P_{out} = 300 W). The total volume of the converter, excluding the EMI filter, is approximately 725 cm^3, and the estimated cost of key components (power switches, heatsink, transformer, and passive elements) amounts to approximately €11.50.

- **Advantages:** Simple architecture with a low component count.
- **Limitations:** Not optimised for output regulation; the significant efficiency drop under regulated conditions can compromise the thermal reliability of critical components during prolonged operation.

5.6.2. GaN-based push-pull converter

The next converter, a GaN-based push-pull topology developed as part of this work, demonstrated notable improvements over the baseline design, particularly in terms of efficiency and volume. The prototype was designed for a nominal input of 24 V and an output of 230 V at 300 W.

Under nominal conditions (V_{in} = 24 V, V_{out} = 230 V, P_{out} = 300 W), the converter reaches an efficiency of 93%. In a lightly regulated scenario (V_{in} = 24 V, V_{out} = 197 V, P_{out} = 300 W), the efficiency decreases slightly to 91.5%, widening the performance gap concerning the baseline (equivalent to V_{in} = 24 V, V_{out} = 170 V, P_{out} = 300 W). The prototype has not been tested under full regulation conditions. The converter's volume is approximately 125 cm^3, and the estimated cost of key components, including power switches, transformer, and passive elements, is around €12.

- **Advantages:** Compact and efficient design with a minimal component count.
- **Limitations:** Despite improved efficiency, performance under regulated conditions still declines, potentially affecting the thermal reliability of key components during extended operation.

5.6.3. Si-based LLC converter with GaN-based buck converter

To address the limitations associated with output voltage regulation, a two-stage solution is proposed. The first stage consists of an unregulated resonant converter, while the second stage is a non-isolated buck converter responsible for voltage regulation.

The resonant converter is implemented as an LLC topology with a split-capacitor configuration, which enables isolation while decoupling it from the regulation functionality. Under nominal conditions ($V_{in,LLC}$ = 24 V, $V_{out,LLC}$ = 280 V, $P_{out,LLC}$ = 300 W), the LLC stage achieves an efficiency of 95.1% at full load. The use of the LLC stage alone for regulation was discarded to simplify the control design. The converter occupies approximately 156 cm^3, with an estimated cost of €9.5 for key components such as power switches, transformer, and passive elements.

The second stage, a buck converter, is introduced to enable full output regulation. Although not physically implemented in the prototype, the GaN-based synchronous buck stage is considered a simple and robust solution. Its worst-case efficiency ($V_{in,buck}$ = 200 V, $V_{out,buck}$ = 100 V, $P_{out,buck}$ = 300 W) is estimated to exceed 99%, with a volume of approximately 20 cm^3 and a component cost of around 6€.

The combined two-stage architecture results in an overall efficiency of 94.3% under nominal conditions (V_{in} = 24 V, V_{out} = 200 V, P_{out} = 300 W) and 93% under worst-case conditions (V_{in} = 20 V, V_{out} = 100 V, P_{out} = 300 W). The total volume is approximately 176 cm^3, and the combined cost of the main components is estimated at 15.5€.

- **Advantages:** High efficiency and full output regulation capability. The separation of stages offers design flexibility and potential for functional enhancement.
- **Limitations:** Increased complexity and cost. The number of power switches is doubled compared to the baseline, which, despite the performance improvements, raises the overall system cost.

The efficiency, cost, and volume indicators for the three converter solutions are compared in Fig. 5.46. In terms of nominal efficiency, the two-stage converter achieves the highest value, followed by the GaN-based push-pull converter. However, this improved performance comes at the expense of a higher component cost.

Regarding volume, both converters developed in this work demonstrate a significant reduction compared to the baseline. Nonetheless, the compact size of the GaN-based push-pull converter should be interpreted with caution, as its thermal design was optimised for light regulation conditions rather than full regulation, as considered in the baseline and two-stage solutions.

For regulation efficiency, a distinction is made between the test conditions: the Si- and GaN-based push-pull converters are evaluated under light regulation (V_{in} = 24 V, P_{out} = 300 W, V_{out} = 170 V for Si, and V_{out} = 197 V for GaN), whereas the two-stage converter is assessed under full regulation (V_{in} = 24 V, P_{out} = 300 W, V_{out} = 100 V). Despite this disadvantageous scenario, the two-stage architecture still delivers the highest efficiency, highlighting its suitability for applications requiring wide output voltage regulation.

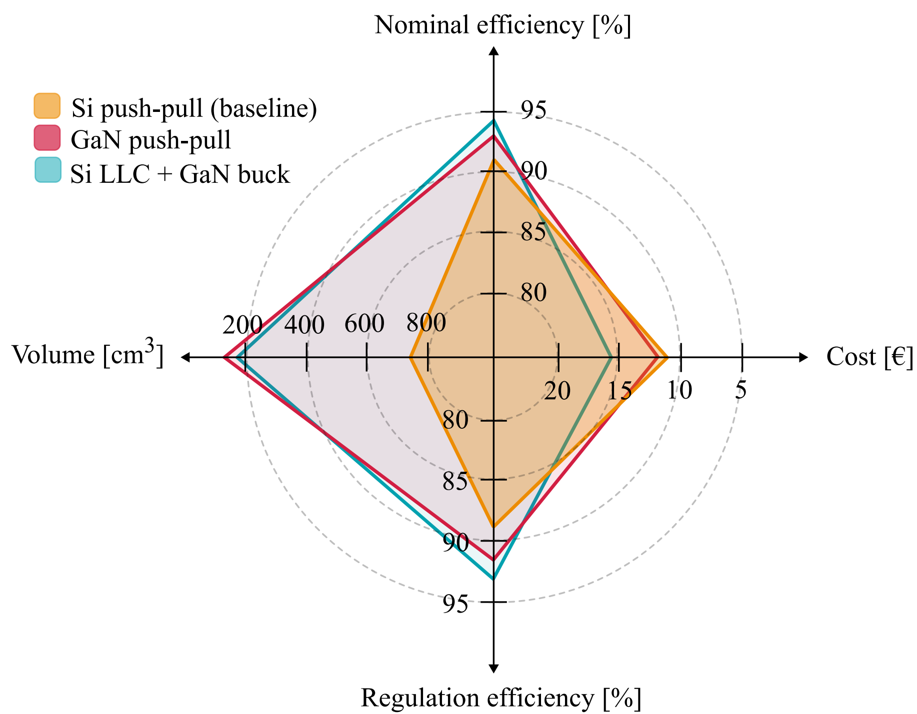


Figure 5.46: Comparison of efficiency, cost, and volume indicators for the proposed DC/DC case study. Three solutions are evaluated: (i) the baseline Silicon-based push-pull converter, (ii) the GaN-based push-pull converter developed in this work, and (iii) the two-stage solution comprising a Silicon-based LLC converter and the GaN-based push-pull converter, both presented in this work.

Chapter 6

OUTLOOK AND CONCLUSIONS

This thesis has explored the integration and performance enhancement of advanced power electronic solutions employing Wide BandGap (WBG) semiconductors, specifically Gallium Nitride (GaN) and Silicon Carbide (SiC) devices, within the context of vertical traction systems and low- to medium-power DC/DC converter applications. Through a structured approach following theoretical modelling, simulation, experimental validation, and comparative analysis, this work has demonstrated the potential of WBG technologies to improve efficiency, reduce volume, and optimise cost in modern power conversion systems.

After defining the scope of this thesis in Chapter 1, Chapter 2 established a solid foundation by reviewing the State of the Art in WBG devices, including their technological advantages, packaging trends, and market scope. SiC Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and diodes were identified as optimal for high-voltage applications due to their robustness and thermal capabilities, while GaN High Electron Mobility Transistor (HEMT) devices offered superior switching speed and integration potential in compact, high-frequency designs. However, the chapter also highlighted challenges such as gate voltage sensitivity and reverse conduction losses, especially noticed in some GaN structures. Figure of Merit (FOM) revealed that GaN devices outperform their Silicon (Si) and SiC counterparts in hard-switching conditions, but under soft-switching scenarios, the performance gap narrows, reinforcing the need for application-specific investigation.

Chapter 3 extended the device-level analysis by addressing three critical aspects of GaN HEMTs: saturation current, dynamic on-resistance, and short-circuit robustness. Experimental evaluations performed with 650 V devices revealed that the saturation current in GaN HEMTs is highly dependent on switching conditions and gate control, with significantly higher (above 50% higher) limits achievable under Zero-Current-Switching (ZCS) operation. GaN Gate Injection Transistor (GIT) devices, especially the latest generation ones, demonstrated superior performance in achieving higher saturation currents than equivalent GaN Schottky Gate Transistor (SGT) devices. The developed study, performed with a customized On-state Voltage Measurement Circuit (OVMC), also confirmed that GaN GITs exhibit improved consistency in dynamic $R_{DS(on)}$ compared to other GaN variants, making them more suitable for high-performance applications. Short-circuit testing further validated the ability of GaN devices to withstand short-circuit periods over 100 μs at reduced drain voltages (320 V in the tested case), contributing to the design of more robust converters.

In Chapter 4, an analytical model of the Double Pulse Test (DPT) was developed to characterise switching behaviour of semiconductor devices using only datasheet parameters. The model, which was based on state-space equations and simulated with MATLAB's ode23s solver, incorporated key parasitics comprising the gate loop and power loop, such as gate inductance (L_G), power loop inductance (L_{loop}), and common source inductance(L_S), and an study was

performed about the impact of these parasitics on the switching losses. The analysis highlighted the importance of minimizing the L_S to reduce switching losses, but also minimizing the L_G and L_{loop} to reduce the overvoltage at the *Gate* and the *Drain* terminals, respectively. The model was validated experimentally on a Silicon-based push-pull converter, which was characterized with a 200 to 350 nH power loop inductance caused by the transformer's winding. The analytical predictions correlated with the experimental measurements, maintaining an error margin within 10% for both switching waveforms and calorimetrically derived loss estimations. The proposed modelling method demonstrated high computational efficiency, requiring less than 5 seconds to simulate a complete switching period. It also proved to be flexible and broadly applicable, enabling the analysis of various semiconductor technologies and converter topologies. As such, it offers a valuable tool for comparing different power switches in terms of switching losses and sensitivity to external parasitics.

In the final chapter, Chapter 5, the insights gained throughout the thesis are translated into practical design implementations, with a focus on elevator system applications and their associated DC/DC converter topologies.

The chapter begins by identifying several opportunities for integrating WBG semiconductors into modern elevator systems, particularly within auxiliary converters operating below 1 kW. While SiC MOSFETs emerge as strong candidates for the main traction drive due to their voltage-handling capability and thermal performance, GaN devices demonstrate clear advantages in compact, high-frequency auxiliary systems where power density and integration are key. Within this context, a comparative review of isolated DC/DC topologies is conducted, considering flyback, forward, push-pull, and half-bridge architectures, where the push-pull converter is highlighted as a particularly favourable solution for mid-power applications, thanks to its efficient transformer utilisation and high effective duty cycle. Compared to the half-bridge alternative, the push-pull configuration shows lower conduction losses at higher step-up ratios, although it demands careful consideration of switch voltage stress.

Focusing on the selected application, a high-frequency GaN-based push-pull converter is designed, optimised, and experimentally validated. Employing the previously developed modelling tool, a multi-objective analysis is carried out in terms of losses, volume, and cost, addressing main components such as power semiconductors, passive, and magnetic components. Focusing on a switching frequency range between 200 and 500 kHz, a well-balanced design was selected, operating at 250 kHz, with EPC2218 GaN HEMTs, and ELP 38/5/25 cores. The snubber circuit was further adjusted employing the modelling tool to limit the overvoltage produced by the leakage inductance to below 80 V. The constructed prototype achieved a peak efficiency of 93% (V_{in} = 24 V, V_{out} = 230 V, P_{out} = 300 W) and a minimum efficiency of 91.8% (V_{in} = 24 V, V_{out} = 197 V, P_{out} = 300 W), with a compact volume of 125 cm^3 and an estimated cost of €12 for main components (including only GaN switches, transformer, and passive components). Compared to the baseline Silicon-based push-pull converter, this represents a fourfold reduction in volume and an efficiency improvement of 2% for nominal conditions (V_{in} = 24 V, V_{out} = 200 V, P_{out} = 300 W) and around 2.8% under light regulation conditions (V_{in} = 24 V, V_{out} = 170 V, P_{out} = 300 W), while maintaining its competitive cost. Calorimetric characterisation of the GaN-based push-pull converter confirms the accuracy and robustness of the analytical modelling tool. When benchmarked against recent literature, the proposed converter demonstrates a strong trade-off profile, offering increased power density and reduced cost while maintaining competitive efficiency levels.

The chapter continues with the development of a resonant LLC half-bridge converter designed for the same target application. This topology enables soft-switching operation and smooth voltage and current waveforms, making it particularly suitable for high-efficiency

designs. Both Frequency Domain Analysis (FDA) and Time Domain Analysis (TDA) are employed to accurately size the resonant tank, while an optimum deadtime and minimum magnetising current approach is adopted to enhance performance. Using the developed modelling tool, both GaN and Silicon devices are evaluated. Results indicate that, under current market availability, Silicon MOSFETs represent a more cost-effective and readily available solution, particularly in soft-switching applications. Following a multi-objective analysis, a well-balanced design is selected, featuring IAUCN08S7N013 Silicon MOSFETs operating at 130 kHz and E 30/7/15 magnetic cores. The fabricated prototype achieves a peak efficiency of 95.7% in most favourable conditions (V_{in} = 28 V, V_{out} = 280 V, P_{out} = 300 W), and 95.1% and 93.7% with nominal (V_{in} = 24 V, V_{out} = 240 V, P_{out} = 300 W) and worst analysed conditions (V_{in} = 20 V, V_{out} = 200 V, P_{out} = 300 W), respectively. Experimental waveforms show excellent agreement with simulations, particularly in terms of deadtime tuning and turn-off current optimisation. The final prototype has a compact volume of 156 cm^3 and an estimated cost of €9.5 for the main components (including only Silicon switches, transformer, and passive elements). As GaN technology continues to mature, with ongoing improvements in device availability and controller compatibility, the potential of GaN within this framework is expected to grow further. However, the analysis also highlights deadtime limitations of commercial controllers as a bottleneck for fully exploiting GaN performance at high switching frequencies with this topology.

The chapter concludes with the analysis and design of a non-isolated step-down buck stage, intended to complement the resonant LLC converter in applications where output voltage regulation is required. A comparison between 650 V GaN SGTs and SiC MOSFETs is conducted for implementing a synchronous buck converter, where the 125 $m\Omega_{typ}$ GaN devices are identified as the most suitable choice for this application. The integration of this additional stage reduces the overall efficiency of the combined system by only 0.7% under worst-case scenarios, while increasing the component cost by approximately €6 per unit for a production batch of 1000 units. This stage provides the required output voltage regulation, complementing the LLC converter's performance. The combined performance of the synchronous buck and the LLC converter results in total power losses of 17 W under nominal conditions (V_{in} = 24 V, V_{out} = 200 V, P_{out} = 300 W) and 21 W under worst-case scenarios (V_{in} = 20 V, V_{out} = 100 V, P_{out} = 300 W), corresponding to overall efficiencies of 94.3 and 93%, respectively. When evaluated at the nominal and worst-case operating points, the combined solution outperforms the Silicon-based push-pull baseline by over 2% in efficiency under nominal conditions (V_{in} = 24 V, V_{out} = 200 V, P_{out} = 300 W) and by more than 13% in worst-case scenarios (V_{in} = 20 V, V_{out} = 100 V, P_{out} = 300 W).

In terms of cost, the total estimated expense for the main components of the combined solution is approximately €15.5, compared to €11.5 for the baseline design, representing an increase of roughly 25–30%. However, this cost gap is expected to narrow as GaN device prices continue to decline with the commercialisation of newer generations. Additionally, alternative configurations, such as replacing the synchronous buck stage with an asynchronous counterpart, could further reduce system costs while retaining most of the benefits of the combined architecture.

From a volumetric perspective, the proposed solution offers a substantial size reduction. Due to lower thermal dissipation requirements, the large heatsink used in the baseline converter can be eliminated. As a result, the overall volume can be reduced by more than 50%, facilitating integration in space-constrained environments. Moreover, the combined solution of LLC and buck configuration is scalable and can be adapted to address increased output power requirements, thus expanding its applicability to a wider range of lift system architectures and

subsystems.

From a broader perspective, the findings suggest that both purely WBG-based and hybrid WBG–Si solutions offer significant advantages for elevator systems. These include enhanced efficiency, reduced volume, and potential cost optimisation. GaN devices, in particular, demonstrate strong suitability for high-frequency, compact designs, while SiC technology, less studied in this thesis, remains advantageous for high-voltage and thermally demanding applications. By strategically combining these technologies, converter designs can be tailored to specific performance and reliability targets, offering a high degree of design flexibility.

In summary, this thesis has provided a comprehensive evaluation of WBG integration in power converters, from device-level characterisation to system-level implementation. The proposed solutions not only improve the technical performance of the studied application but also contribute to broader industrial adoption by enhancing product competitiveness. As device technologies continue to evolve and controller ecosystems become increasingly compatible with high-speed switching, the relevance and impact of these findings are expected to grow, reinforcing the role of WBG semiconductors in next-generation power conversion systems.

FUTURE LINES

Building on the insights and contributions presented in this thesis, several promising directions for future research are identified:

First, further validation of the analytical loss model developed in Chapter 4 is recommended, with an emphasis on separating turn-on and turn-off energy contributions. Extending the model to cover all GaN-based devices, including GITs and Hybrid Normally-off Structures (HNO) structures, would significantly enhance its generality. A first approach has been developed for GaN GITs, but further verification and experimental validation is required. Incorporating advanced calorimetric techniques for experimental validation and adjustment would also improve the accuracy of the model, helping with WBG adoption in power electronics.

Second, future work should explore layout parasitics in more detail. Developing comprehensive design criteria and optimisation strategies for PCB and packaging layouts, using electromagnetic field simulation tools such as ANSYS Q3D or FastFieldSolvers, would enable more precise estimation of behaviour and overall converter optimization. These insights would complement the analytical modelling framework by closing the gap between theoretical losses and real-world implementation.

Another important research path is the characterisation and quantification of AC losses in magnetic and passive components. The high-frequency effects harden the sizing and fining of suitable components, complementing WBG devices. Experimental validation of these losses, under realistic switching conditions and waveform shapes, remains an open challenge. Addressing this would refine the understanding of total system efficiency and support more accurate thermal design and component sizing.

Additionally, GaN GITs and SGTs should be further investigated under fault conditions to evaluate their short-circuit robustness in detail. Experimental testing and research could validate their practical viability in demanding environments and enable safe design margins for commercial deployment.

In the context of experimental prototypes and validation, Electromagentic Interference (EMI)/Electromagentic Compatibility (EMC) performance should be carefully evaluated. This includes proper sizing of input and output filters to ensure compliance with relevant standards and regulations, particularly when comparing hard-switched and soft-switched converter topologies. Furthermore, the integration of WBG devices may significantly influence EMI/EMC behaviour, potentially impacting the choice of semiconductor technology and converter architecture.

Finally, the construction of the resonant LLC converter has been partially validated; however, GaN HEMT devices have not yet been experimentally tested. While theoretical estimations have already highlighted the practical limitations of this topology, experimental evaluation using GaN HEMTs could offer deeper insight and further validate the theoretical analysis. Such results may also provide a clearer definition of operational constraints.

Regarding the regulation stage, the physical implementation of the proposed GaN-based buck converter remains. Building and testing this converter would allow for a direct comparison with simulated performance, while also verifying the proposed design methodologies. Moreover, integrating GaN GITs in this prototype would provide a valuable opportunity to experimentally investigate their short-circuit robustness within a practical application context. This prototype could serve as a platform for evaluating dynamic behaviour, integration

challenges, and cost-performance trade-offs in compact, high-frequency power systems.

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