Experimental verification of the AC resistance effect in Insulated Metal Substrate based Power Converters

Iosu Aizpuru [1], Miguel Lajas [1], Asier Arruti [1], Eneko Agirrezabala [1], José Miguel Sanz-Alcaine [2], Francisco Jose Perez-Cebolla [2], Mikel Mazuela [1]

[1] Mondragon Unibertsitatea, Galarreta Campus, Hernani, Spain
[2] Group of Power Electronics and Microelectronics (GEPM), Aragón Institute of Engineering Research (I3A), University of Zaragoza, Zaragoza, Spain
Main Author e-Mail: iaizpuru@mondragon.edu

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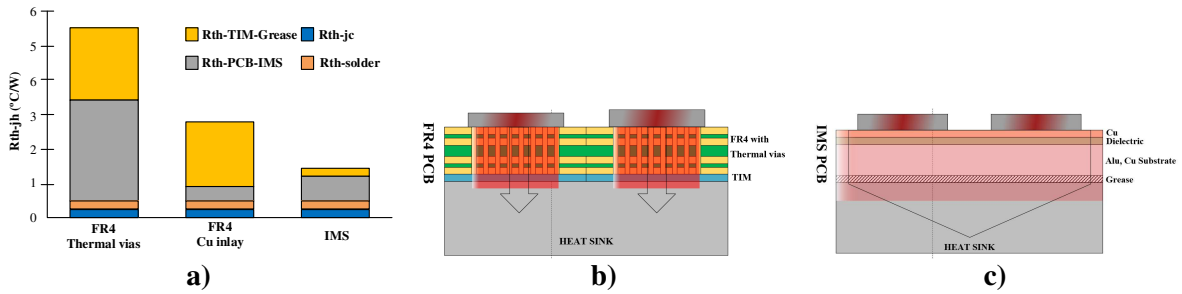
***Abstract*— Insulated Metal Substrate (IMS) based power converters are an excellent solution for thermal dissipation of power converters, but they suffer for limited layer options generating parasitic elements specially in High Frequency. The paper analyses and proposes experimental verification of IMS AC resistance in High Frequency power converter applications. The developed test bench can generate high current high frequency electrical signals in order to excite the IMS board parasitic AC resistances. The experimental validation highlights the importance of PCB lay-out in high frequency IMS boards where big area current loops and low copper areas increase significantly the resistance of the board. The developed tests verify a significant AC resistance effect in IMS boards with a temperature increase 4 times bigger at 500 kHz switching frequency than the equivalent DC current.**

I. Introduction

Insulated Metal Substrate (IMS) technology has become a popular choice in many LED applications due to its high thermal conductivity and excellent heat transfer properties [1]–[3]. The use of IMS technology has allowed LED manufacturers to design more efficient and reliable LED products. The exceptional thermal properties of IMS technology have generated interest in its application for heat dissipation in power converters [4]–[6]. In recent years, with the emergence of new technologies such as WBG SiC and GaN devices, power converters have been capable of operating at multi-Megahertz switching frequencies [7]–[9]. High-frequency (HF) operation can complicate the use of IMS technology in power converter applications [10]–[12]. IMS technology is limited to single or double-layer construction, and these constraints in PCB layout can make it challenging to implement flux cancellation techniques. Due to this fact, the use of IMS technology in HF power converter applications



a) b) c)

Fig. 1: a) Thermal Resistance decrease thanks to better PCB substrate adoption from classical FR4 PCBs, to Cu-inlay PCBs and IMS technology (adopted from [6]). b) Localized and straight thermal flow in classical FR4 PCB, c) IMS distributed heat dissipation where all the heat dissipation area of the IMS substrate is used, even to cool-down the PCB traces.

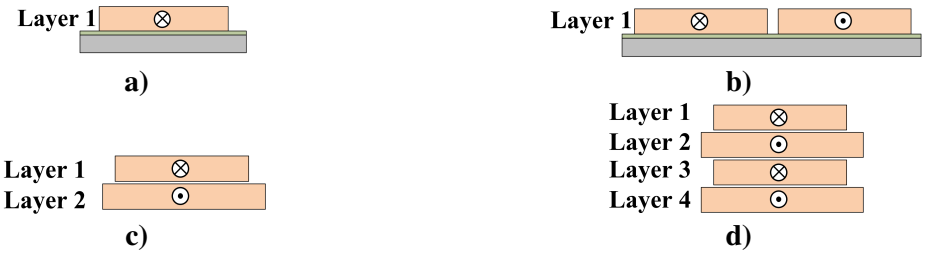


Fig. 2: a) Bad IMS design where the backward current path is not near the forward one b) Good IMS trace lay-out with near backward-forward traces. c) Good 2 layer FR4 design where the backward layer is down the forward layer and with wider copper area (GND plane concept) d) Multilayer PCB concept where backward and forward layers/traces are simultaneously intercalated (Flux cancelling "sandwich" concept).

can result in increased AC resistance, primarily due to skin effect.

This paper aims to contribute to the understanding of IMS technology in high-frequency power converter applications by analyzing the AC resistance of IMS technology in DCDC converters. The main contributions of the paper are:

- Experimental analysis of high-frequency AC resistance in IMS technology applications.
- Development of a thermal testing method for IMS converter testing by incorporating the converter as a DUT.

II. IMS TECHNOLOGY OVERVIEW

The IMS technology enables a substantial reduction in the thermal dissipation path for power converters, particularly in high-frequency designs such as those employing GaN-based devices. In the case of small package devices, despite the limited heat generation, the dissipation of thermal energy through the pad is not sufficiently efficient. Therefore, IMS technology plays a pivotal role in enhancing the benefits of high-frequency power converters by augmenting the thermal pad's dissipation capabilities. As depicted in **Fig. 1** a), the utilization of IMS-based semiconductor dissipation results in a reduction of the overall thermal pad from the junction to the heat sink. This reduction is approximately **4** times greater compared to a FR4-based thermal vias design and roughly **2** times greater than a Cu-inlay counterpart. One additional advantage of utilizing the IMS-based converter is the provision for efficient dissipation of heat from the current-carrying paths. In designs with high current densities, this feature is particularly crucial. This is owing to the favorable coefficient of copper tracks, which has a positive correlation with temperature, resulting in an increase in efficiency when the tracks are maintained at lower temperatures.

Notwithstanding the advantages of IMS technology, the design layout poses certain limitations. Mainly, IMS designs are predominantly single-layered, which does not facilitate the implementation of current cancellation techniques that are commonly utilized in two-layer or multilayer FR4 designs.

In IMS technology, the forward and backward current paths must be kept in close proximity to minimize the skin effect. Moreover, the metallic substrate in IMS technology needs to be scrutinized to assess its potential impact on the AC resistance in high-frequency applications.

The skin depth effect in copper traces/conductors is defined by:

$$\delta = \sqrt{\frac{1}{\sigma \pi \mu_0 \mu_r f}} \sim 2\mu m \sqrt{\frac{1}{f\ [GHz]}} \qquad (1)$$

Where is mainly given by a skin depth of 2 microns at 1 GHz and it just scales inversely respect to the square rot of the working frequency.

Table I: Approximation of High Frequency power converter skin depth in function of the working frequency.

Frequency [MHz]	Skin depth [µm]
0.1	200
0.5	89.44
1	63.24
2.5	40
5	28.28

Power converters are reaching switching frequencies above the MHz frequency range.

Considering that 1-3oz (35-105µm) are usual copper thickness in classical designs the skin depth effect could appear in PCB based power converters.

III. RAC TESTING METHODOLOGY IN IMS BASED POWER CONVERTERS

The AC resistance of copper traces/tracks is very difficult to measure. Small signal measurement equipment as LCR and impedance analyzers do not excite the circuit with application current (not provoking same flux levels) and are prepared to measure high impedance/resistance values (10s to 100s of Ω), so they are not suitable to check the AC resistance of IMS based copper tracks.

It is clear that the IMS power tracks AC resistance measurement is a big challenge, mainly due to the need of inserting application current levels and relatively low resistance track values.

Due to these issues, this paper proposes a methodology where the AC resistance effect is measured by thermal measurements.

One option could be to measure the temperature of the tracks while the converter is working. However this method could have several drawbacks. The switching frequency may not be varied due to converter control/HW limitations. Another drawback is that the current amplitude may not be also controlled. And finally the main drawback is that the semiconductor losses (switching and conduction) and temperature increase could not be decoupled from the track temperature increase.

In order to correctly measure the temperature increase of IMS based power tracks the next test setup with some important characteristics is proposed:

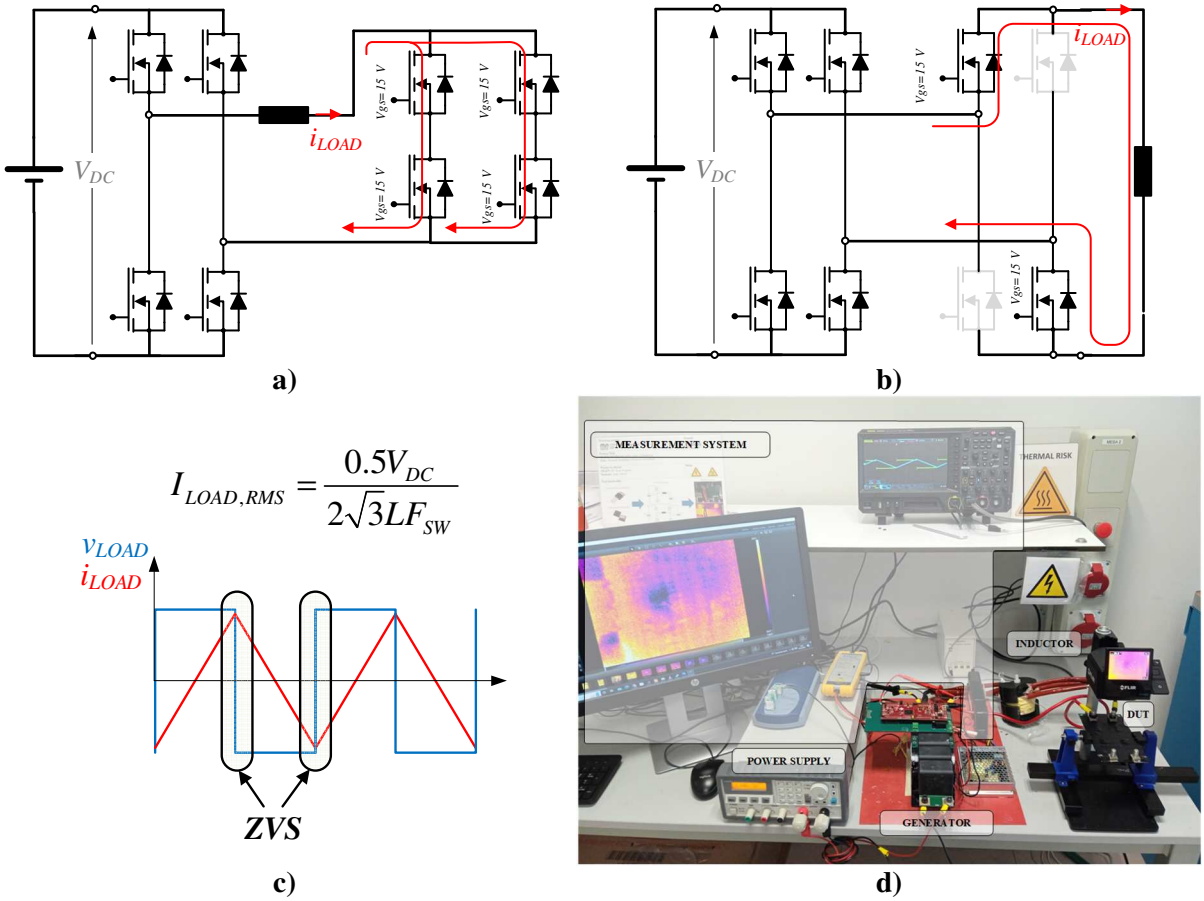


Fig. 3: a) Test setup analysis for the determination of AC resistance in IMS based power PCBs. A) Test setup to determine the AC resistance of the half bridges of an IMS based H-bridge. B) test setup to determine the positive sequence pad for an IMS based H-bridge converter. C) Expected triangular waveforms where the load RMS current $I_{LOAD,RMS}$ is a function of the inductor L, DC voltage V_{DC} and the switching frequency F_{SW}. d) Test setup photography with the lay-out description of the equipment used for IMS AC resistance board testing.

- A power converter that generates a 50% duty square voltage wave will be used to excite the IMS board at different frequency values and current levels. During this paper the converter will be known as GENERATOR.
- The converter under test is the main converter IMS board, with the semiconductor pads short circuited, avoiding any switching and losses effect of the semiconductors, and only focusing on the IMS board traces temperature increase. This converter will be known as DUT.
- The current that will flow through the DUT will be set as triangular with zero DC/average current. The harmonic content of a triangular waveform is low and could be approximated that the F_{SW} is mainly the fundamental and dominant frequency of the AC signal.
- In order to analyze the AC resistance effect, a triangular AC current with controlled RMS value is generated in function of the DC bus voltage V_{DC}, the switching frequency F_{SW} and the inductor load L value. This current RMS value is compared to an equivalent DC current.

The test RMS current $I_{LOAD,RMS}$ is described by equation (2) due to its triangular nature.

$$I_{LOAD,RMS} = \frac{0.5V_{DC}}{2\sqrt{3}LF_{SW}} \quad (2)$$

The GENERATOR could be able to reach high ILOAD,RMS / FSW ratios due to that all the semiconductors will be working in a soft switching ZVS region Fig. 3 c).

The DUT can be configured in different ways in order to test different IMS traces pads. For example Fig. 3 a) presents a configuration where both half-bridges are short circuited (Vgs=15V in all 4 semiconductors). With this configuration the IMS AC resistance of the half bridges paths could be analyzed, even the asymmetries between the different half-bridges lay-outs.

On the other side, Fig. 3 b) represents an analysis path of the positive sequence of a classical H-bridge configuration. With this configuration the positive sequence AC resistance could be evaluated only switching on (Vgs=15V in 2 semiconductors) in the DUT.
The test setup could be visualized in Fig. 3 d) and resumed in Table II. The test setup is divided in 5 main parts: GENERATOR, DUT, INDUCTOR (L), POWER SUPPLY and MEASURE EQUIPMENT.

IV. EXPERIMENTAL RESULTS

To verify the proposed methodology and test bench, an IMS-based power board will undergo testing. The power board under test (DUT) is an H-bridge with the following characteristics.

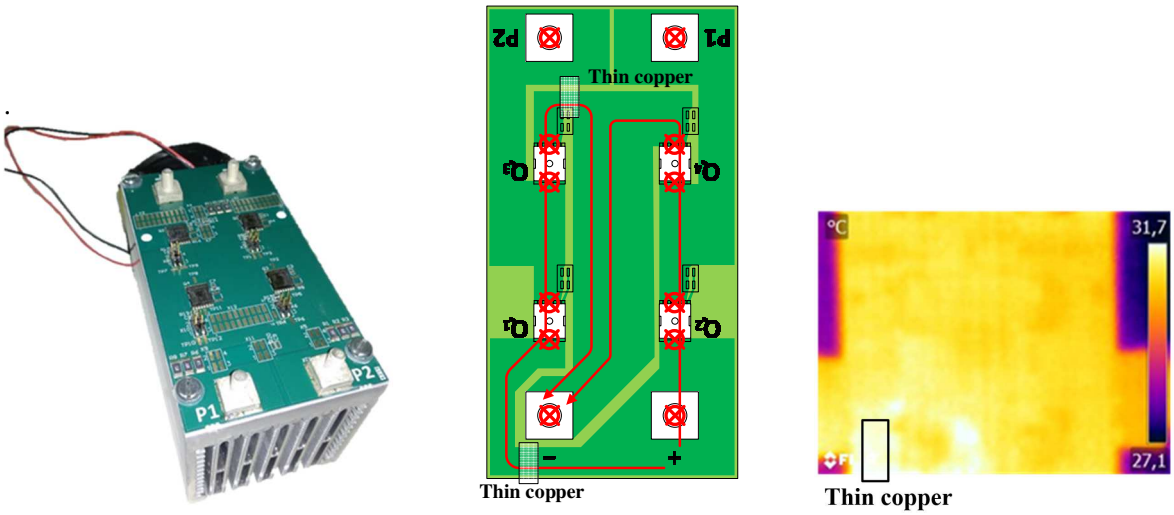
Table III: Specifications of the Device Under Test DUT.

Parameter	Value/Description
PCB technology	IMS
Nº of layers	1
Copper Thickness	2 oz / 70 µm
Converter Topology	H-Bridge

In order to produce a quantifiable temperature rise within the IMS board, the RMS current supplied will be adjusted to a range of

Table II: Test equipment description.

	Equipment	Description
	GENERATOR	H-BRIDGE IPT026N10N5 100V 2.6 mΩ 202 A $F_{SW,max}$ = 1 MHz
	DUT	IMS BOARD: Different ranges from 1 oz to 3 oz.
	INDUCTOR	High current inductor range from 470 nH 150A to 5 µH 70 A.
	POWER SUPPLY	IT6723G power supply, 660V, 5A, 850W
MEASURE EQUIPMENT	THERMAL CAMERA	Flir ETS320 -20ºC-250ºC 320x240 Resolution +-3ºC
	THERMAL LOGGER	Picolog USB TC-08 8 Channel temperature datalogger 10S/s
	OSCILLOSCOPE	Rigol MSO5204 200MHz BW,4 Channel+ 16 digital Channel,8GSa/s
	CURRENT PROBE	Hioki 3274 DC to 10 MHz, 150 Arms
	VOLTAGE PROBE	TA 041 25 MHz 700 V differential oscilloscope probe
	MAIN CONTROLLER	Windows based PC with Labview based control SW for equipment control



a) b) c)

Fig. 4: a) Photo of the IMS based H-bridge under test (During the AC resistance test, the heat sink is not utilized). b) PCB lay out of the different components of the IMS based H bridge. Special check to the thin copper area when the DC + current flows to Q1. c) Thermal camera image of the DC test where it is clearly measured that there is an unbalance on temperature distribution due to the thin copper area.

approximately 20-25 Arms. This range of selected current level aims to induce a detectable thermal effect within the IMS board, enabling reliable and precise measurement of the temperature increase.

In order to assess the impact of AC resistance in the typical operating range of power conversion systems, the switching frequency will be varied systematically between 50 kHz and 500 kHz. This range represents the classical nowadays switching frequency utilized in such systems. However, it is worth noting that future research will explore higher switching frequencies beyond the MHz range, made feasible by the implementation of Gallium Nitride (GaN) and Silicon Carbide (SiC) Wide Bandgap (WBG) devices.

The inductance value is measured with an LCR meter. This measurement accounts for not only the inherent inductance of the device but also measures the additional inductance contributed by the connecting cables. The total inductance utilized in the test bench is of 0.866 µH = 866 nH.

The final test specifications are summarized in **Table IV**.

In order to analyze the AC resistance in IMS boards the configuration presented in **Fig. 3** a) will be evaluated. The test will be carried with the 4 semiconductors of the H bridge shorted (Vgs = 15 V constant) in order to analyze the AC resistance effect in the current pads of the IMS based H-bridge.

The reference test (Test 0) is developed by a DC power supply and with a controlled DC current of 23 A. The IMS board is tested without the heat-sink to obtain bigger temperature sensitivity.

The lay-out of the IMS board is presented in **Fig. 4** b) where the current paths as in **Fig. 3** a) are represented. There are pad/trace lay-out limitations, due to the limitations of a single layer IMS board design. In this design copper traces have different width, where PCB zones with thin copper have higher effective copper resistance. The thin copper areas are highlighted and the effect on the thermal unbalance of the thin copper of the down side is presented in **Fig. 4** c). The thermal camera analysis concludes that the thin copper area has a maximum temperature of 31,7 ºC during the DC test.

Table IV: Test specifications. The values that are in the table are exact values of the developed tests.

Test	V_{DC} [V]	F_{SW} [kHz]	$I_{LOAD,RMS}$ [A]	L [µH]
0	DC	DC	23	0.866
1	7	50	23	0.866
2	14	100	23	0.866
3	28	200	23	0.866
4	42	300	23	0.866
5	56	400	23	0.866
6	70	500	23	0.866

a) **b)** **c)**

Fig. 5: Flir ETS320 thermal camera images for different AC resistance evaluation tests. a) Test 1 50 kHz b) Test 3 200 kHz c) Test 6 500 kHz.

After DC test (Test 0) is performed, frequency tests are developed with the same equivalent RMS current of 23 A. (Test 1-6).

The experimental triangular waveforms of Test 1 (50 kHz) and test 6 (500 kHz) are presented in **Fig. 6** (a and b) respectively. The presence of parasitic capacitance and inductance resulting from single-layer routing is responsible for the observed ringing effect in the voltage waveform. However, in this context, the significance lies in the fact that the current waveform maintains a complete triangular shape, rendering the impact of the ringing effect negligible. So the results presented in **Fig. 6** permits to validate the developed GENERATOR as a high frequency triangular current source.

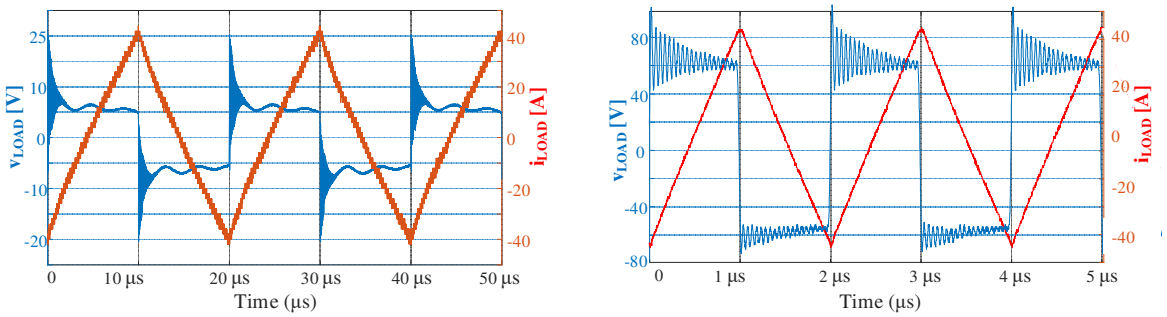
The thermal camera images of tests 1, 3 and 6 are presented in Fig. 5. These images validate the developed test bench as an AC resistance analysis test bench.

The results presented in **Fig. 5** confirm that there is a temperature increase in the IMS PCB due to the increase in F_{SW}, certifying an AC resistance increase in IMS based power converters.

The hot spot that was in the down side of the PCB thin copper area of **Fig. 4** b) now is moved to the upper side thin copper area due to the increase of the AC resistance in that zone. This increase is mainly due to higher distance with the opposite current path. The current flowing loop area is increased increasing the AC parasitic effects and increasing the losses in the high side PCB zone.

In order to simplify the analysis of the results, **Table V** resumes the main results of the developed tests. The MAX, MIN and AVERAGE temperature are calculated with the total measuring area of 320x240 given by the Flir ETS320 thermal camera.

The results are also plotted in **Fig. 7** analyzing the temperature variation of the PCB respect to the ambient temperature T_{AMB} of 25ºC. The baseline temperature is the DC Test (Test 0). A maximum temperature variation of 20º respect to the DC Test is measured in the IMS board with a switching frequency F_{SW} of 500 kHz. Compared to a maximum temperature increase of 5ºC in the DC scenario, a temperature rise of 20ºC at 500 kHz is four times larger, providing further confirmation of the significant impact of the AC resistance effect.



a) **b)**

Fig. 6: Experimental load current i_{LOAD} and load square voltage v_{LOAD} for tests 1 and tests 6. a) Test 1 50 kHz b) Test 6 500 kHz.

Table V: Steady state thermal results. Maximum PCB temperature, average PCB temperature and minimum PCB temperature

Test	T_{MAX} PCB [ºC]	T_{AV} PCB [ºC]	T_{MIN} PCB [ºC]
0	30.98	30.17	29.23
1	34.47	33.78	32.33
2	35.83	34.87	33.1
3	38.26	36.82	34.49
4	40.69	38.67	35.87
5	42.51	40.35	37.23
6	44.35	41.93	38.47

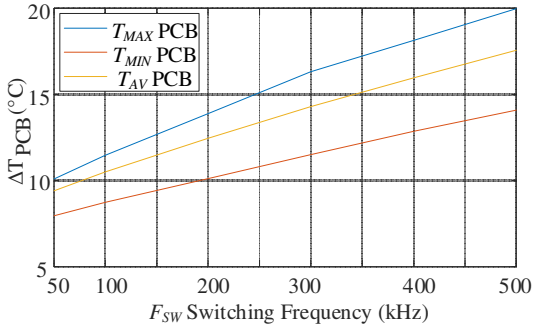


Fig. 7: Variation of the IMS PCB temperature ΔT PCB respect to an ambient temperature T_{AMB} =25 ºC. maximum minimum and average temperature variation in PCB.

V. Conclusion

An experimental validation methodology in order to analyze the AC resistance effect in IMS boards is presented.

The developed test bench can analyze the AC resistance effect in IMS boards, for different F_{SW}, IMS board pads/traces, $I_{LOAD;RMS}$ levels, for a range from DC to 500 kHz-1MHz. The analysis is developed by thermal camera analysis where the critical pads/traces in an IMS board can be determined.

A temperature increase of a factor of 4 (4x) has been measured for the same RMS current in a 500 kHz current RMS analysis respect to an equivalent DC.

Future lines will be the theoretical analysis of AC resistance in IMS boards in order to minimize AC resistance effect during the PCB design process. This theoretical approach will be validated by experimental measurements developed in the proposed test bench.

References

[1] G. Elger, A. Hanss, M. Schmid, and T. Wipiejewski, "Application of thermal analysis for the development of reliable high power LED modules," in 2014 11th China International Forum on Solid State Lighting (SSLCHINA), 2014, pp. 158–164, doi: 10.1109/SSLCHINA.2014.7127246.

[2] G. Elger, H. Willwohl, and J. Schug, "Thermal analysis of high power LED subassemblies for automotive front light application," in 2012 4th Electronic System-Integration Technology Conference, 2012, pp. 1–8, doi: 10.1109/ESTC.2012.6542062.

[3] J. Freisleben, T. Dzugan, and A. Hamacek, "Comparative study of printed circuit board substrates used for thermal management of high power LEDs," in 2015 38th International Spring Seminar on Electronics Technology (ISSE), 2015, pp. 80–84, doi: 10.1109/ISSE.2015.7247967.

[4] M. P. Sayani, "DC-DC converter using all surface-mount components and insulated-metal substrate," in [Proceedings] APEC '92 Seventh Annual Applied Power Electronics Conference and Exposition, 1992, pp. 639–646, doi: 10.1109/APEC.1992.228351.

[5] G. Aime, J. Barbaroux, and J.-P. Ferrieux, "Power factor corrector on insulated metal substrate," in IAS '95. Conference Record of the 1995 IEEE Industry Applications Conference Thirtieth IAS Annual Meeting, 1995, vol. 2, pp. 1026–1030 vol.2, doi: 10.1109/IAS.1995.530414.

[6] J. L. Lu, R. Hou, and D. Chen, "Opportunities and design considerations of GaN HEMTs in ZVS applications," in Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2018, vol. 2018-March, pp. 880–885, doi: 10.1109/APEC.2018.8341117.

[7] Y. Gao and A. Q. Huang, "Feasibility Study of AlGaN/GaN HEMT for Multi-megahertz DC/DC Converter Applications," in 2006 CES/IEEE 5th International Power Electronics and Motion Control Conference, 2006, vol. 2, pp. 1–3, doi: 10.1109/IPEMC.2006.4778172.

[8] Y. Li, X. Ruan, L. Zhang, and J. Dai, "Optimized Parameters Design for a 20MHz Class E DC-DC Converter With ON-OFF Control," in 2018 IEEE Energy Conversion Congress and Exposition (ECCE), 2018, pp. 2164–2170, doi: 10.1109/ECCE.2018.8558018.

[9] S. Guo, P. Liu, R. Yu, L. Zhang, and A. Q. Huang, "Analysis and loss comparison of

megahertz high voltage isolated DC/DC converters utilizing integrated SiC MOSFET module," in 2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2016, pp. 291–296, doi: 10.1109/WiPDA.2016.7799955.

[10] H. Huillet, C. Zardini, S. Catrou, F. Manns, C. Martin, and I. L. Aucouturier, "High frequency quasi-resonant buck converter on insulated metal substrate for avionics distributed power systems," in [Proceedings] APEC '92 Seventh Annual Applied Power Electronics Conference and Exposition, 1992, pp. 647–653, doi: 10.1109/APEC.1992.228350.

[11] R. Samani, J. Lu, and I. G. Zurbriggen, "Next Generation of GaN Single-Board High Power Stages," in 2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA), 2022, pp. 233–237, doi: 10.1109/WiPDA56483.2022.9955306.

[12] E. Gurpinar, S. Chowdhury, B. Ozpineci, and W. Fan, "Graphite-Embedded High-Performance Insulated Metal Substrate for Wide-Bandgap Power Modules," IEEE Trans. Power Electron., vol. 36, no. 1, pp. 114–128, 2021, doi: 10.1109/TPEL.2020.3001528.