

System Level Optimization of 5 MW Wind Converter using 3L-NPC Topology in Medium Voltage with 1.7 kV IGBT

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Abstract—Market competitiveness is the main driver in the massive adoption of wind energy, and the optimization of the power converter is crucial for this purpose. Because it has higher efficiency than the two level Voltage Source Converter (2L-VSC), the three level Neutral Point Clamped (3L-NPC) topology is considered for the converter optimization. Due to reduced voltage stress in 3L-NPC, the system voltage can be increased up to Medium Voltage while keeping the same 1.7 kV semiconductors used for 2L-VSC. Potential extra efficiency due to the increased voltage, cooling system and filter volume reduction are studied by simulation. Commercial cooling systems and capacitors are analyzed to calculate volumes, while analytical expressions are used for the inductors. A system level optimization is proposed achieving filter and combined volume reduction, as well as efficiency increment. The benefits of using three level converters to increase the application voltage, without increasing the semiconductors voltage range are shown at system level.

Keywords—Wind energy, Modeling, 3L-NPC, Multilevel, Medium Voltage.

I. INTRODUCTION

Renewable energy generation has been receiving increasing attention from scientific community since the 2000s [1], [2]. According to [3], for example, wind energy installed capacity has grown exponentially the last three decades. By the end of 2018, the renewable energies represented the 26.2 % of the world energy mix, having experienced a growth of the 33 % in the year 2018 [4]. As market competitiveness is the main driver for renewable energies high penetration into the energy mix, the system cost must be optimized in wind and solar energy generation systems. Power converters are used to interface renewable energy systems with the distribution grid [3], [5], [6], so improving this component is key to achieve a reduction in the system cost. Fig. 1, shows a Wind Generation System (WGS) with a back to back converter. These author focus on the optimization of the power converter to make a contribution to the renewable energies market competitiveness.

Increasing the efficiency of the grid interfacing power converter, as well as an increased power density of WGS, are cited as important contributions in [3], while [7] proposes SiC semiconductors to achieve those objectives. Safety in form of reliability and strict grid code compliance, reactive power compensation, grid fault ride-through and voltage regulation are mentioned in [8]–[12], even if massive power electronics

integration is needed for this purpose. In addition, the importance of the control of the generator and power converter

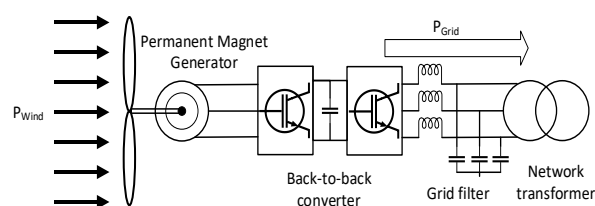


Fig. 1. WGS with PM and back to back converter.

in the grid integration of Wind Farms (WF) as a global unit, together with strict protection standards was underlined even before the year 2000 [13], and more recently in [14], [15].

In [14] the need to focus on reliability, efficiency and cost of the power converter is highlighted, leading to an important amount of research looking for the best topology and design. Back to back converters, symmetrical converters in both sides of the dc link, Fig. 1, have been selected by the main manufacturers up to date [3], [6]. These power converters need to ensure the grid connection complies strict grid codes. In addition, these regulations are being updated and getting more and more demanding [16], [17]. The voltage ride-through requirements of the German Transmission and Distribution Utility (E.On) regulation are explained in [18]. This regulation was introduced in 2003 but seems to set the standard according to [3].

Various power converter topologies can be implemented in wind turbines. The most common up to date is the two level (2L) back to back [3], [6]. However, if bidirectional power is not required, diode rectification can be applied, with a cascaded step-up converter to perform dc bus control and a 2L-Voltage Source Converter (VSC), Fig. 2 (a), in the inverter stage [3]. According to [7], 1.7 kV semiconductors are preferred in Full Converter (FC) configurations. However, if 2L-VSC converter is used with 1.7 kV semiconductors, the dc bus voltage is limited to 1.2 kV [19], only being able to create a line to line voltage of 690 V in the output. Multilevel converters have been introduced to achieve higher operation voltages as well as a reduction in the line filter [3], [20]. Many three level (3L) topologies can be used depending on the application and goal [21], designing 3L back to back converters, as suggested in [3], [20].

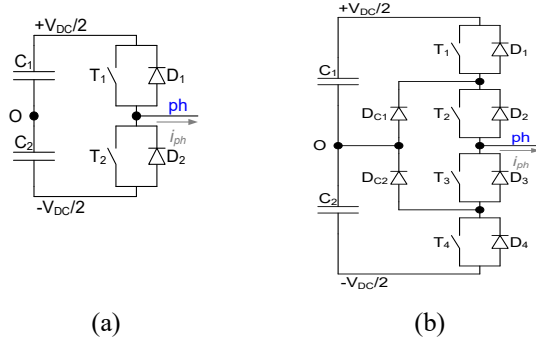


Fig. 2. Compared topologies, (a) 2L-VSC, (b) 3L-NPC.

TABLE I. REGIONAL CLASSIFICATION OF LOW AND MEDIUM VOLTAGE IN THREE PHASE AC LINES

Region	Standard	LV	MV
Europe [50 Hz]	IEC60038	<1000 V	1-35 kV
USA [60 Hz]	ANSI C84.1	<600 V	600 V-35 kV

WGS configurations can be classified depending on the voltage level of the application, however, this classification varies depending on the region [22], TABLE I. Although Low Voltages (LV) are preferred due to reduced installation and maintenance cost as well as more flexible regulations, Medium Voltage (MV) and High Voltage (HV) applications are gaining interest nowadays due to the reduced currents and higher efficiencies, being specially interesting in off-shore wind farms due to reduced transport losses [23]. The limit between MV and LV will be considered 1 kV for the rest of this paper, according to the IEC60038 standard.

The benefits of the efficiency improvement achieved by using 3L-NPC topology in MV applications, compared to the 2L-VSC in LV are analyzed in a 5 MW Permanent Magnet (PM) WGS with a back to back converter, Fig. 1. In addition, the possible system level improvements in the line filter and Cooling System (CS) volumes are also considered. A system optimization is finally performed, taking advantage of 3L-NPC topology and its capability to work in MV without changing the widely used 1.7 kV semiconductors. This system level optimization can influence directly the before mentioned market competitiveness, helping the integration of more renewable energies into the energy mix.

II. PROPOSED SYSTEM

In order to achieve a low semiconductor price, and ensure a reliable supply chain, keeping the widely used 1.7 kV semiconductors is identified as a key factor. The possibility to increase the applications voltage level until MV without serializing any 1.7 kV semiconductor is opened using 3L topologies, because only half of the dc link voltage needs to be blocked [19], allowing to create a 2.4 kV dc link. With this dc voltage, assuming a possible grid voltage variation of $\pm 10\%$ and keeping the modulation index below 0.9, an optimum line to line voltage of 1375 V is estimated for exploiting to the maximum the voltage rating of 1.7kV semiconductors. This will be the MV reference considered henceforth in this paper. 3L Neutral Point Clamped (3L-NPC) topology, Fig. 2 (b), is successfully used in PV applications achieving high efficiency [24]. The same topology is adopted for evaluation in LV and MV, and being compared to state of the art 2L-VSC, Fig. 2 (a), converter in LV.

TABLE II. SEMICONDUCTOR NUMBER USED IN EVERY TOPOLOGY

Topology	Voltage level	Total component count
2L-VSC	LV	96
3L-NPC	LV	188
3L-NPC	MV	144

III. SYSTEM MODEL

A. Wind Generator System Model

First, the power curve of a 2 MW wind turbine presented in [6] is adapted by lineal extrapolation to obtain a 5 MW power curve. Next, the mechanical power extracted from the power curve is converted into electrical power by using the PM model used in [25]. If a unity PF is assumed, currents and voltages in the PM can be calculated in dq rotating coordinate system using basic PM generator theory. Output voltage as well as line current are calculated with the presented PM generator model in order to supply electrical input variables to the power loss models of 2L-VSC and 3L-NPC converters.

B. Power Loss Models

Power losses of the two analyzed converter topologies are modeled by analytical expressions in this section. First, the equations representing 2L-VSC converter power losses are shown. Next, the equations modeling 3L-NPC converter losses are presented. Both conduction and switching losses are considered.

Same semiconductor is used in order to compare the topologies and voltage levels in a fair way. The selected semiconductor is a generic IGBT in a half bridge stack. It has a blocking voltage rating of 1.7 kV, as well as 600 A capability. TABLE II summarized the semiconductor use in every analyzed topology and voltage level combination. IGBT diodes data is used for diodes, for the sake of simplicity.

As observed in TABLE II, the component count in the 3L-NPC is higher than in the 2L-VSC. However, the number of semiconductors required is reduced when moving to MV, due to the current reduction. In addition, the simulations performed will show extra benefits at system level.

1) 2L-VSC

The following equations for 2L-VSC converters are presented in [26], being (1) the conduction losses of the IGBTs and (2) of the diodes. m_a represents the modulation index, and it is calculated using (3).

$$P_{\text{Cond_IGBT}} = \frac{1}{2} \cdot \left(V_{\text{th}} \cdot \frac{I_{\text{max}}}{\pi} + R_{\text{ON}} \cdot \frac{I_{\text{max}}^2}{4} \right) + m_a \cdot \cos(\varphi) \cdot \left(V_{\text{th}} \cdot \frac{I_{\text{max}}}{8} + \frac{R_{\text{ON}} \cdot I_{\text{max}}^2}{3 \cdot \pi} \right) \quad (1)$$

$$P_{\text{Cond_DIODE}} = \frac{1}{2} \cdot \left(V_{\text{th}} \cdot \frac{I_{\text{max}}}{\pi} + R_{\text{ON}} \cdot \frac{I_{\text{max}}^2}{4} \right) - m_a \cdot \cos(\varphi) \cdot \left(V_{\text{th}} \cdot \frac{I_{\text{max}}}{8} + \frac{R_{\text{ON}} \cdot I_{\text{max}}^2}{3 \cdot \pi} \right) \quad (2)$$

$$m_a = \sqrt{2} \cdot \frac{V_{ll}}{V_{dc}} \quad (3)$$

Switching losses in the IGBTs are calculated using (4). a_T , b_T and c_T refer to the coefficients of the second order polynomial that approaches the switching energy losses of the

IGBTs, provided in the datasheets. Switching losses in the diodes are calculated using (5), being a_D , b_D and c_D the switching energy coefficients referring to the diodes.

$$P_{Sw_IGBT} = f_{sw} \cdot \frac{V_{dc}}{V_{100FIT}} \cdot \left(\frac{a_T}{2} + \frac{b_T \cdot I_{max}}{\pi} + \frac{c_T \cdot I_{max}^2}{4} \right) \quad (4)$$

$$P_{Sw_DIODE} = f_{sw} \cdot \frac{V_{dc}}{V_{100FIT}} \cdot \left(\frac{a_D}{2} + \frac{b_D \cdot I_{max}}{\pi} + \frac{c_D \cdot I_{max}^2}{4} \right) \quad (5)$$

2) 3L-NPC

As the semiconductors in 3L-NPC converters do not perform equally, each semiconductor must be analyzed. First, conduction losses are modeled in equations (6), (7) for IGBTs, (8), (9) for diodes, and (10) for clamping diodes, [19]. Semiconductor naming is the one used in Fig. 2(b). The 3L-NPC is symmetrical, so semiconductors are organized in pairs.

$$P_{Cond_{T_1, T_4}} = \frac{m_a \cdot I_{max}}{12\pi} \cdot \{3V_{th} \cdot [(\pi - \varphi) \cdot \cos(\varphi) + \sin(\varphi)] + 2R_{ON} \cdot I_{max} \cdot [1 + \cos(\varphi)]^2\} \quad (6)$$

$$P_{Cond_{T_2, T_3}} = \frac{I_{max}}{12\pi} \cdot \{V_{th} \cdot [12 + 3m_a(\varphi \cdot \cos(\varphi) - \sin(\varphi))] + R_{ON} \cdot I_{max}[3\pi - 2 \cdot m_a \cdot (1 - \cos(\varphi))^2]\} \quad (7)$$

$$P_{Cond_{D_1, D_4}} = \frac{m_a \cdot I_{max}}{12\pi} \cdot \{3V_{th} \cdot [-\varphi \cos(\varphi) + \sin(\varphi)] + 2R_{ON} \cdot I_{max} \cdot [1 - \cos(\varphi)]^2\} \quad (8)$$

$$P_{Cond_{D_2, D_3}} = \frac{m_a \cdot I_{max}}{12\pi} \cdot \{3V_{th} \cdot [-\varphi \cos(\varphi) + \sin(\varphi)] + 2R_{ON} \cdot I_{max} \cdot [1 - \cos(\varphi)]^2\} \quad (9)$$

$$P_{Cond_{D_{C1}, D_{C2}}} = \frac{I_{max}}{12\pi} \cdot \{V_{th} \cdot [12 + 3 \cdot m_a \cdot [(2\varphi - \pi) \cdot \cos(\varphi) - 2 \sin(\varphi)]] + R_{ON} \cdot I_{max} \cdot [3\pi - 4 \cdot m_a \cdot (1 + \cos^2(\varphi))]\} \quad (10)$$

Finally, the switching performance of 3L-NPC is evaluated using the series of equations presented in [27]. Equations (11), (12) refer to the IGBTs, (13) is used for diodes 1 to 4, while (14) is used for the clamping diodes. Note that coefficients b_T and c_T refer to the coefficients of the second order polynomial that approaches the switching energy losses of IGBTs, while b_D and c_D refer to the diode ones. Again, the semiconductors are organized in pairs, and the naming of Fig. 2(b) is used.

$$P_{Sw_{T_1, T_4}} = \frac{V_{dc}}{4\pi} I_{max} \cdot f_{sw} \cdot [b_T \cdot (1 + \cos(\varphi)) + \frac{1}{2} \cdot c_T \cdot I_{max} \cdot (\frac{1}{2} \cdot \sin|2\varphi| + \pi - |\varphi|)] \quad (11)$$

$$P_{Sw_{T_2, T_3}} = \frac{V_{dc}}{4\pi} I_{max} \cdot f_{sw} \cdot [b_T \cdot (1 - \cos(\varphi)) + \frac{1}{2} \cdot c_T \cdot I_{max} \cdot (|\varphi| - \frac{1}{2} \cdot \sin|2\varphi|)] \quad (12)$$

$$P_{Sw_{D_{1-4}}} = \frac{V_{dc}}{4\pi} I_{max} \cdot f_{sw} \cdot [b_D \cdot (1 - \cos(\varphi)) + \frac{1}{2} \cdot c_D \cdot I_{max} \cdot (|\varphi| - \frac{1}{2} \cdot \sin|2\varphi|)] \quad (13)$$

$$P_{Sw_{D_{C1}, D_{C2}}} = \frac{V_{dc}}{4\pi} I_{max} \cdot f_{sw} \cdot (2b_D + \frac{\pi}{2} \cdot c_D \cdot I_{max}) \quad (14)$$

C. Cooling System Model

The equivalent average thermal circuit is used to calculate the maximum allowable thermal resistance to keep junction temperature in the semiconductors under the safe thresholds. However, a calculation to relate the maximum allowable thermal resistance with the required CS volume needs to be added.

To do so, commercial CSs with forced air are analyzed in order to identify the volume required to obtain a certain thermal resistance value. The required volume and the achieved thermal resistance are plotted for each product and manufacturer, obtaining a trend that can be approximated with an exponential curve, shown with a black line in Fig. 3.

Each topology and voltage level has different power losses, and as the switching frequency also affects the power losses, each topology and voltage level, as well as each selected switching frequency combination will require a certain and unique maximum thermal resistance. Using the exponential approximation of the available commercial CSs, Fig. 3, the cooling system model is capable to calculate the volume required by the cooling system for each topology, voltage level and switching frequency combination.

D. Line Filter Model

A line filter shapes the output current of the converter, as shown in Fig. 1. The inductance and capacitance values in the filter are calculated using expressions (15) and (16) presented in [28] and [29] respectively. V_{dc} is selected 1.2 kV for LV applications, and 2.4 kV for MV applications, ΔI_{out} is defined as 10 % of the I_{out} . m is the number of voltage levels of the converter, being 2 for 2L and 3 for 3L. Att_{req} , which refers to the required attenuation of the filter, is set to 0.01 to have enough damping in the switching frequency for both LV and MV, [29].

$$L_f = \frac{V_{dc}}{6(m-1) \cdot \Delta I_{out} \cdot f_{sw}} \quad (15)$$

$$C_f = \frac{1}{(2\pi f_{sw})^2 \cdot L_f \cdot Att_{req}} \quad (16)$$

To calculate the volume of the inductor, the area product A_p technique proposed in [30] is used. Equation (17) uses the factor k_L to relate the area product and inductor volume, approximated by a polynomial expression [31]. [29] identifies a linear relation between volume, the rated voltage and capacitance for every capacitor technology. This characteristic can be highly important in the comparison of LV

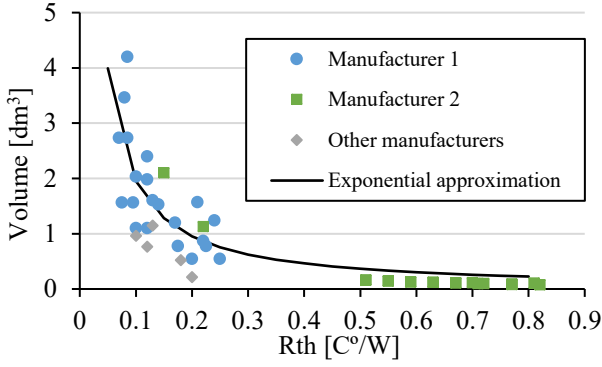


Fig. 3. Commercial CSs volumes and the calculated exponential approximation, depending on the thermal resistance.

and MV applications. To have a fair volume approximation, commercial polypropylene capacitors are analyzed, considering their volume and rated voltage, Fig. 4. 1.2 kV series is selected for the LV applications, while 3 kV is selected for MV applications. The linear expressions relating volume and capacitance are shown in, (18) for 1.2 kV rated voltage, and in (19) for 3 kV. It can be seen that capacitors used in MV require more volume, Fig. 4. This difference is even more important when high capacitance is required, because the slope of the linear approximation is higher for MV capacitors.

$$Vol_{L_f} = k_L \cdot A_p^{\frac{3}{4}} \quad (17)$$

$$Vol_{C_{fLV}} = 0.0345C_f + 0.0037 \quad (18)$$

$$Vol_{C_{fMV}} = 0.158C_f + 0.0026 \quad (19)$$

IV. SIMULATION

The simulation of the system is done for wind speeds from 2.5 to 25 m/s, which is the operation range of the turbine presented in [6]. Different switching frequencies are also considered, keeping the wind speed constant at nominal wind speed, 12.5 m/s. Semiconductors junction temperature is kept under 150 °C, while ambient temperature is assumed to be 20 °C. Line voltages of 690 V and 1375 V are considered for LV and MV respectively.

At the first section, the efficiency of the system is studied, calculating the volume required for the CS for different topologies and voltage levels. In the second section, the volume of the line filter is analyzed, for different voltage levels and switching frequencies. Finally, system level optimization is proposed.

A. Efficiency Analysis and Cooling System Volume

First, the converter efficiency is calculated in the whole operation range for 2L-VSC, 3L-NPC in LV and 3L-NPC in MV, Fig. 5. For this simulation, 2.5 kHz frequency has been selected. It is observed that 3L-NPC has slightly better efficiency than the state of the art 2L-VSC topology, even in LV, however, if the full voltage potential of the semiconductors is used, moving to MV, the efficiency difference is higher, being over 98.7 % in nominal wind conditions, 12.5 m/s, Fig. 5.

Next, the efficiency of the converter is analyzed in different switching frequencies and shown in Fig. 6. To do so, nominal wind conditions (12.5 m/s) are selected, because it is

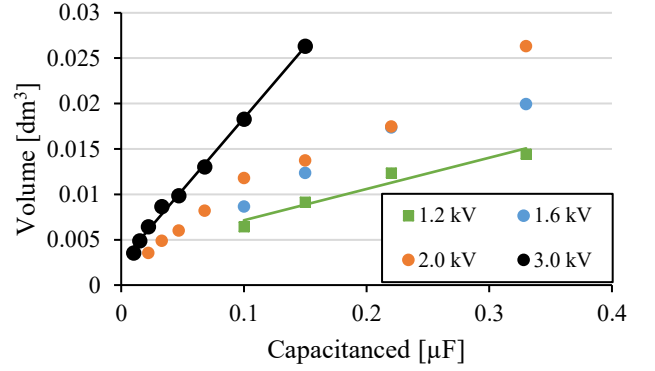


Fig. 4. Commercial polypropylene capacitors volumes for different rated voltages, and the linear approximations for 1.2 kV (green) and 3 kV (black).

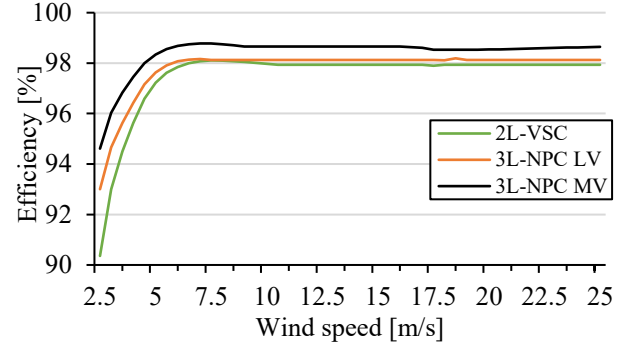


Fig. 5. Converter efficiency for different topologies, voltage levels, and wind speeds.

the operation point in which most energy is generated, as well as maximum losses are generated in the system. Fig. 6 shows 3L-NPC converters decrease in efficiency at nearly the same rate, being the main difference between them the conduction losses. Looking at equations (6)-(10), it can be seen they are proportional to I_{max} , which is reduced in MV applications, also reducing the conduction losses of the application.

Analyzing switching losses of the 3L-NPC topology, equations (11)-(14), it is observed that switching losses are nearly proportional to both V_{dc} and I_{max} . As the power of the application is the same, these two parameters keep a constant relation in between them when increasing voltage, forcing the efficiency to decrease at very similar rate for LV and MV applications, in this particular case. Fig. 6 also shows the efficiency decrease in relation to frequency of the 2L-VSC topology is greater than the one of the 3L-NPC. This characteristic opens up the possibility to increase the switching frequency in 3L-NPC topology, reducing the volume of the filter, but not so much in 2L-VSC topology, because the efficiency would drop drastically.

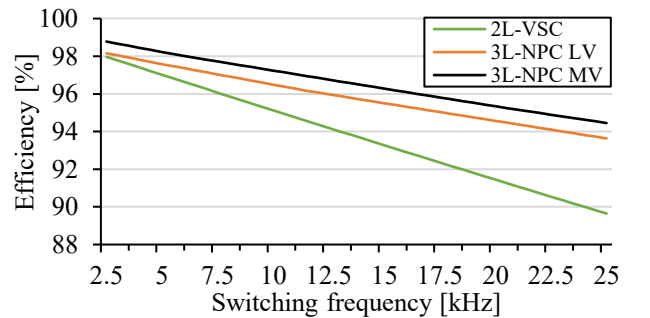


Fig. 6. Converter efficiency for different topologies, voltage levels, and switching frequencies.

Fig. 7 analyses the evolution of the required volume for the CS, in order to keep the semiconductors junction temperature under 150 °C. This volume is calculated at nominal wind speed condition (12.5 m/s), being the operation point with maximum losses, and the one selected to design the cooling requirements. As expected, the 3L-NPC topology in MV configuration requires less volume than the other two configurations. In addition, 3L-NPC topology increases its CS volume requirements less than the 2L-VSC when frequency is increased.

B. Filter Volume

In this section, the volume of the filter is analyzed for different applications. The effect of switching frequency as well as the level of the topology are studied, in order to define the benefits and drawbacks of increasing switching frequency and working in MV.

Fig. 8 shows how the volume required for the filter is reduced if the switching frequency of the converter is increased. The higher the number of voltage levels, the greater the reduction in the filter inductor can be (15). This is why 3L topologies achieve lower volumes in the filter, Fig. 8. No difference in volume is identified when using LV or MV, because the current is reduced at the same rate as the voltage is increased. It is also seen the extra volume required in the capacitor of the filter in MV, Fig. 4, is widely out-weighted by the inductor volume.

Two methods to reduce the volume of the filter for the same power applications are identified. The first approach is to increase the switching frequency, with the already analyzed efficiency penalty, shown in Fig. 6. The other is increasing the voltage levels of the converter topology, applying multilevel converters.

C. Proposed System Level Optimization

The CS, Fig. 7, and filter, Fig. 8, volumes are combined and computed in Fig. 9. It is seen that the CS volume is dominant in every switching frequency in all the applications, so a combined volume optimization cannot be performed by changing the switching frequency. However, it is possible to obtain benefits at system level by increasing frequency.

To achieve this, it is defined that the filter volume is being reduced 50 % respect to the 2L-VSC converter. This can be achieved by just increasing the switching frequency 1 kHz, up to 3.5 kHz in 3L converters, Fig. 8. Even if very close efficiency to 2L-VSC topology is achieved at this switching frequency with 3L-NPC at LV, the reduced volume in the filter leads to a reduced combined volume, Fig. 9. The main

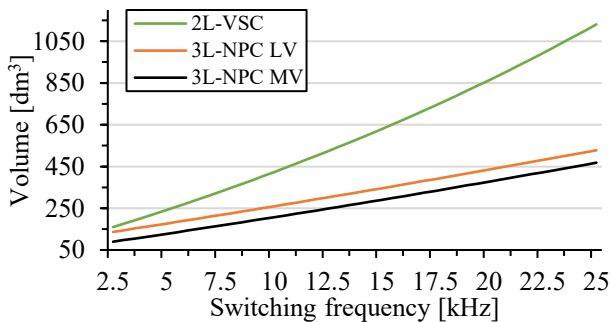


Fig. 7. Calculated cooling system volume for different topologies, voltage levels, and switching frequencies.

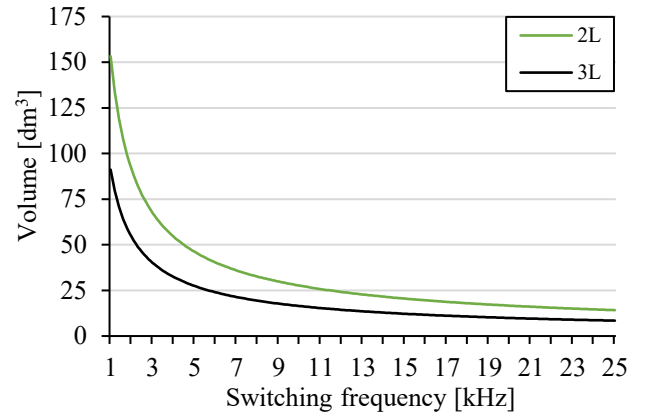


Fig. 8. Calculated filter volume for 2L and 3L topologies as well as switching frequency.

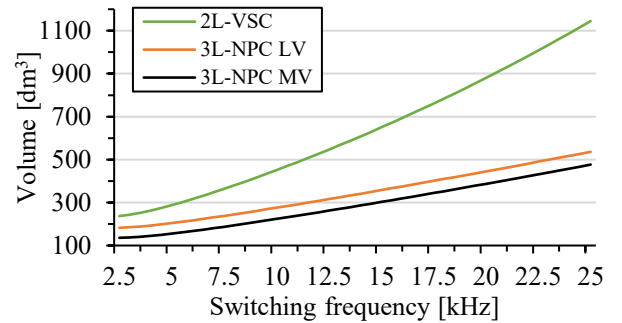


Fig. 9. Combined volume for different topologies, voltage levels, and switching frequencies.

benefits are achieved with 3L-NPC topology in MV, reducing the filter and combined volume while still increasing efficiency at nominal wind speed respect to 2L-VSC topology. It should be noted that this system level optimization is achieved with the same 1.7 kV IGBTs that are widely used nowadays in 2L-VSC and LV applications. TABLE III summarizes the benefits of using the optimized 3L-NPC topology at MV.

V. CONCLUSION

This simulation work shows the possibilities of improving the converter of wind generation systems at system level, with the use of 3L topologies, even with the conventional 1.7 kV IGBTs used in 2L-VSC converters. By using 3L-NPC topology in LV, the volume of the output filter can be reduced 50 %, without penalizing efficiency. However, if the characteristics of the 1.7 kV IGBT blocking voltage in 3L-NPC are fully used, a MV approach can be adopted. This voltage increment leads to the already mentioned 50 % filter reduction, but also increasing the efficiency of the converter, leading to a volume reduction in the CS of nearly 35 %. Final combined volume is reduced over 40 % using 3L-NPC topology in MV.

The volume required for the dc link, control board, connections and semiconductors should also be considered in the future, in order to compute and compare power densities. Although the proposed system uses commonly selected 1.7 kV IGBTs, with secured supply chain and competitive market prices, cost functions should be included regarding efficiency increment, CS and filter reduction and semiconductor number, in order to achieve the most price-competitive system. This last analysis is out of scope of this work.

TABLE III. OPTIMIZED SYSTEMS CHARACTERISTICS COMPARED TO 2L-VSC

Characteristic	2L-VSC	3L-NPC LV	3L-NPC MV	Unit
Switching frequency	2.5	3.5	3.5	kHz
Efficiency at nominal wind speed	97.92	97.96	98.55	%
Filter volume	77.26	35.85	35.85	dm ³
Filter volume reduction	/	53	53	%
Required CS volume	159.8	157.6	104.8	dm ³
Required CS volume reduction	/	1.37	34.41	%
Combined volume	237	193.45	140.65	dm ³
Combined volume reduction	/	18.37	40.65	%

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