





Review

Short-Circuit Detection and Protection Strategies for GaN E-HEMTs in High-Power Applications: A Review

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Abstract

Gallium nitride (GaN) enhancement-mode high-electron-mobility transistors (E-HEMTs) deliver superior performance compared to traditional silicon (Si) and silicon carbide (SiC) counterparts. Their faster switching speeds, lower on-state resistances, and higher operating frequencies enable more efficient and compact power converters. However, their integration into high-power applications is limited by critical reliability concerns, particularly regarding their short-circuit (SC) withstand capability and overvoltage (OV) resilience. GaN devices typically exhibit SC withstand times of only a few hundred nanoseconds, needing ultrafast protection circuits, which conventional desaturation (DESAT) methods cannot adequately provide. Furthermore, their high switching transients increase the risk of false activation events. The lack of avalanche capability and the dynamic nature of GaN breakdown voltage exacerbate issues related to OV stress during fault conditions. Although SC-related behaviour in GaN devices has been previously studied, a focused and comprehensive review of protection strategies tailored to GaN technology remains lacking. This paper fills that gap by providing an in-depth analysis of SC and OV failure phenomena, coupled with a critical evaluation of current and next-generation protection schemes suitable for GaN-based high-power converters.

Keywords: GaN E-HEMT; short-circuit protection; overvoltage; reliability; power electronics



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1. Introduction

Power electronic converters play a fundamental role in modern society by enabling efficient energy conversion across a wide range of applications, including renewable energy systems, electric vehicles, and data center power supplies [1]. Historically, these systems have relied on silicon (Si)-based semiconductor devices, which have undergone continuous improvements in current handling capability, voltage blocking, thermal performance, and switching speed. However, Si technology is now approaching its fundamental material limits, as it can be manufactured without defects, leaving limited room for further performance enhancements [2].

To address these limitations, wide-bandgap (WBG) semiconductors such as gallium nitride (GaN) and silicon carbide (SiC) have attracted considerable attention due to their superior electrical properties [3]. Among them, GaN-based high-electron-mobility transistors (HEMTs) have emerged as a promising alternative to conventional Si and even SiC devices in high-performance power electronic systems [4]. GaN HEMTs exhibit several advantages, including faster switching dynamics, lower on-state resistance, and enhanced

high-frequency performance [3]. These characteristics enable the development of power converters with higher efficiency and increased power density.

Initially, GaN technology gained commercial traction through its use in low-power applications [5]. However, recent improvements in voltage ratings and current capabilities have significantly expanded its potential in high-power applications such as automotive and aerospace. These fields require compact, lightweight, and highly efficient power solutions, where the superior performance of GaN devices can directly contribute to extended operational range [6,7].

Despite these promising attributes, the widespread adoption of GaN technology in high-power applications remains constrained by several critical reliability concerns. One of the primary challenges is the inherently normally on nature of conventional GaN HEMTs, which poses safety risks, as the device may remain conductive in the absence of a gate signal or during power loss. In contrast, normally-off devices are preferred, as they inherently revert to a non-conductive state under such conditions [8]. To fulfill this requirement, enhancement-mode GaN HEMTs (E-HEMTs) have been developed. The most prevalent commercial implementations include the Schottky-type p-gate HEMT (SP-HEMT) and the gate-injection transistor (GIT) [9].

Nevertheless, even with the adoption of E-HEMT architectures, applying GaN devices in high-power systems remains difficult due to their limited short-circuit (SC) tolerance. In high-power systems, robust SC performance is essential for ensuring safe operation under fault conditions. Conventional Si-based insulated-gate bipolar transistors (IGBTs) can typically withstand SC events for up to $t_{sc} = 10 \mu\text{s}$ and SiC MOSFETs up to around $t_{sc} = 2 \mu\text{s}$ [10,11]. In contrast, 600–650 V GaN E-HEMTs—commonly used in applications above 400 V—can typically tolerate SC conditions for only a few hundred nanoseconds [12–14].

This extremely short SC withstand time places stringent demands on the protection and detection circuits. Traditional detection schemes, such as the desaturation (DESAT) technique—widely used with Si and SiC power transistors—are too slow for GaN-based systems. Commercial DESAT gate drivers generally require more than $2.5 \mu\text{s}$ to respond [15], far exceeding the failure threshold of GaN HEMTs. Furthermore, the very fast switching transitions of GaN devices increase susceptibility to electromagnetic interference (EMI) and noise, which may result in false activation events and further compromise system reliability [16].

Moreover, when an SC event is detected and the protection circuit rapidly turns off the GaN device, the sudden current interruption generates a high rate of change in the current (di/dt). This excites parasitic inductances in the circuit, causing significant overvoltage (OV) spikes across the device terminals. Unlike Si and SiC devices, which can often endure such transients via avalanche breakdown or active clamping mechanisms, GaN HEMTs lack avalanche ruggedness, making them unable to safely dissipate the resulting energy or effectively clamp OV. Instead, their deactivation behaviour is dominated by resonant oscillations between the device's output capacitance and parasitic inductances. Notably, GaN devices exhibit a wide dynamic breakdown voltage margin, allowing them to temporarily withstand voltages beyond their static ratings [17]. However, this dynamic margin is highly dependent on operating conditions, trap states, and device architecture, making OV tolerance unpredictable and uncontrolled for reliable protection [18]. Consequently, it is difficult to effectively apply conventional protection techniques such as transient voltage suppressors (TVS), as the variable and condition-dependent breakdown voltage (BV) complicates the design of fixed voltage clamping solutions.

Given these challenges, there is a pressing need for advanced detection and protection strategies that combine ultrafast detection and high noise immunity circuits to safeguard

GaN devices during SC events. Although prior research has examined various aspects of GaN SC and OV behaviour, to the best of the authors' knowledge, this work is the first comprehensive review specifically focused on SC detection and protection strategies tailored to GaN E-HEMTs in high-power applications. This paper aims to bridge that gap by providing an in-depth analysis of the following:

- **Short-circuit:** A comprehensive examination of the SC reliability of GaN devices is presented, highlighting critical factors such as gate–source voltage (V_{gs}), ambient temperature (T_{amb}), and bus voltage (V_{bus}), and their significant influence under both single-pulse and repetitive stress conditions. The root causes of device failure during SC stress are also analysed.
- **Overvoltage:** A focused analysis of avalanche and non-avalanche devices is provided, with special emphasis on the dynamic breakdown behaviour of GaN HEMTs. The study highlights the key factors—such as device architecture, trap dynamics, and operating conditions—that cause variations in breakdown voltage across different GaN structures.
- **Emerging protection and detection techniques for SC events in GaN power devices:** A state-of-the-art review of protection and detection methods currently implemented in Si and SiC technologies is presented, offering valuable insights into their applicability and adaptation to GaN systems, alongside solutions proposed in recent academic literature.

The paper is structured as follows: first, the types of SC faults are examined in detail; second, the behaviour of E-HEMT GaN devices under SC conditions is analysed; third, the OV characteristics of GaN devices are explored; and finally, the detection and protection circuits currently used or proposed for GaN applications are reviewed.

2. Short Circuit

An SC event occurs when a low-impedance path is established between the transistor and the power supply. This condition forces the device into its active region, resulting in significant current and voltage combined stress. SC faults in a single device are typically classified into two main types: hard switching faults (Type I) and faults under load (Type II) [19].

2.1. Type I SC

Type I SC occurs when Q_2 is activated while its complementary switch Q_1 remains in an SC state, as illustrated in Figure 1a within Loop 1.

In Figure 1b, the different intervals of a Type I SC event can be distinguished following the transfer (Figure 1c) and output (Figure 1d) characteristics:

- $t_0 - t_1$: At instant t_0 , the driver of transistor Q_2 receives the activation command and begins injecting gate charge, charging the input capacitance of the transistor and increasing V_{gs} . At instant t_1 , as shown in Loop 2, V_{gs} reaches the threshold voltage ($V_{gs_{th}}$), and transistor Q_2 begins conducting the drain to source current (I_{ds}). At this point, Q_2 blocks the entire V_{bus} , meaning the drain to source voltage (V_{ds}) remains high as the channel begins to form.
- $t_1 - t_2$: During this interval, I_{ds} experiences a rapid increase towards its steady-state short-circuit value (I_{sc}), following a di/dt transition predominantly determined by V_{bus} and the total parasitic inductance (L_σ) of the circuit:

$$\frac{di}{dt} = \frac{V_{bus}}{L_\sigma} \quad (1)$$

Concurrently, the drain-to-source voltage V_{ds} of Q_2 decreases as a result of the voltage drop across the parasitic inductance:

$$V_{ds} = V_{bus} - L_{\sigma} \cdot \frac{di}{dt} \tag{2}$$

As V_{gs} continues to rise towards the driver supply voltage (V_{DR}), the channel conductivity increases, and the device operates in the active region, where the transfer characteristic governs its behaviour. Consequently, V_{gs} defines the final value of I_{sc} . This interval concludes at t_2 , when the current slope (di/dt) reaches zero, the drain current stabilizes at I_{sc} , and V_{ds} returns close to V_{bus} .

- $t_2 - t_3$: During this interval, the device remains in the active region, sustaining both V_{bus} and I_{sc} , leading to high power dissipation and severe thermal stress. Once the short-circuit event is detected at t_3 , the driver initiates the deactivation process for Q_2 by applying the deactivation voltage (V_{DR}). As a result, V_{gs} starts to decrease, and when it falls below $V_{gs_{th}}$, the transistor ceases conduction.
- $t_3 - t_4$: The current derivative occurring in the $t_3 - t_4$ interval excites the parasitic inductances, causing an OV across the transistor terminals. The faster the transistor turns off, the greater the di/dt , and therefore, the higher the OV, which could exceed BV and lead to its destruction.

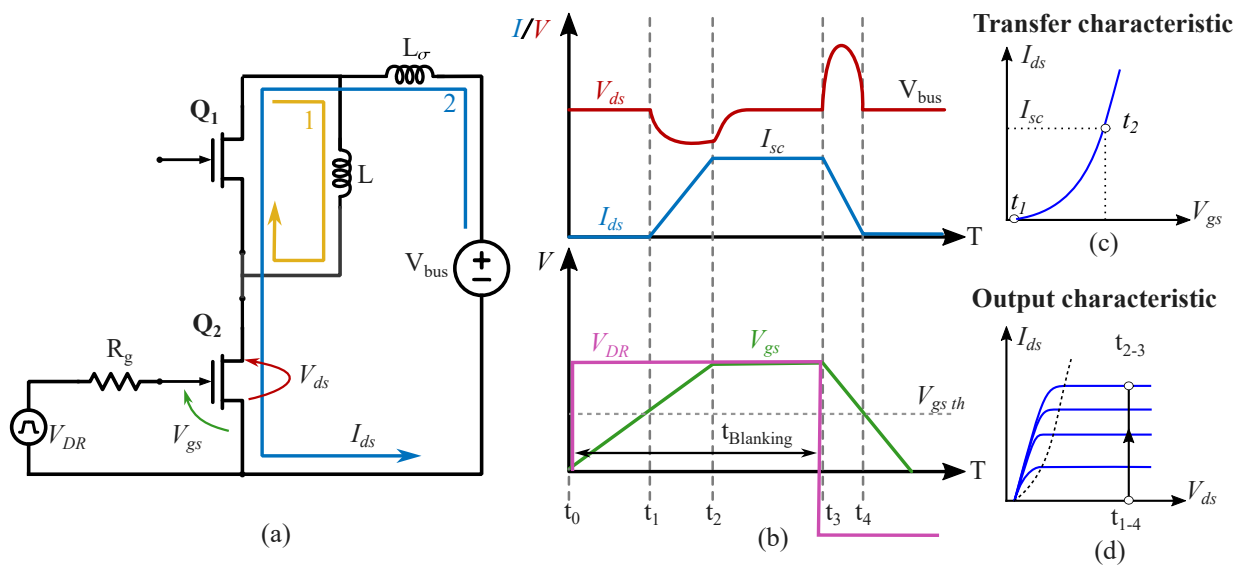


Figure 1. Type I short-circuit event: (a) half-bridge configuration; (b) corresponding voltage and current waveforms; (c) transfer characteristic; and (d) output characteristic of the transistor.

2.2. Type II SC

Type II SC occurs when the transistor Q_2 conducts the load current, while Q_1 is off and blocking voltage (see Figure 2a, Loop 2).

In Figure 2b, the different intervals of the Type I SC event can be distinguished following the transfer (Figure 2c) and output (Figure 2d) characteristics:

- $t_1 - t_2$: At instant t_1 , the fault occurs at Q_1 , and the drain-to-source voltage of transistor Q_2 suddenly rises to V_{bus} (Loop 2). The voltage derivative across transistor Q_2 causes the gate-drain capacitance (C_{gd}), also known as the Miller capacitance, to inject current into the gate terminal (I_M), increasing V_{gs} , which was initially at V_{DR} .

$$I_M = C_{gd} \cdot \frac{dV_{ds}}{dt} \tag{3}$$

Since V_{bus} is applied between the drain and source terminals of Q_2 , it operates in the active region. In this region, the transfer characteristic is fulfilled, meaning that an increase in V_{gs} results in a higher I_{sc} .

As long as V_{gs} remains higher than V_{DR} , during the $t_1 - t_2$ interval, current flows from the gate to the driver, reducing V_{gs} . At instant t_2 , V_{gs} stabilises at V_{DR} , and the gate current ceases. At this moment, I_{sc} is established.

- $t_2 - t_3$: During this interval, the device remains in the active region, sustaining both V_{bus} and I_{sc} , leading to high power dissipation and severe thermal stress.

Finally, when the SC is detected at instant t_3 , the driver initiates the turn-off process for Q_2 by applying the V_{DR} turn-off voltage. At this moment, V_{gs} begins to decrease.

- $t_3 - t_4$: The current derivative during this interval excites the parasitic inductances of the power circuit, resulting in an OV at the transistor terminals, which could exceed the BV and lead to device failure.

The thermal stress experienced by a transistor during a Type II SC is higher than in a Type I SC as I_{sc} is greater in a Type II event. Additionally, if V_{gs} exceeds the maximum limit specified in datasheets ($V_{gs\ MX}$), it can lead to device failure.

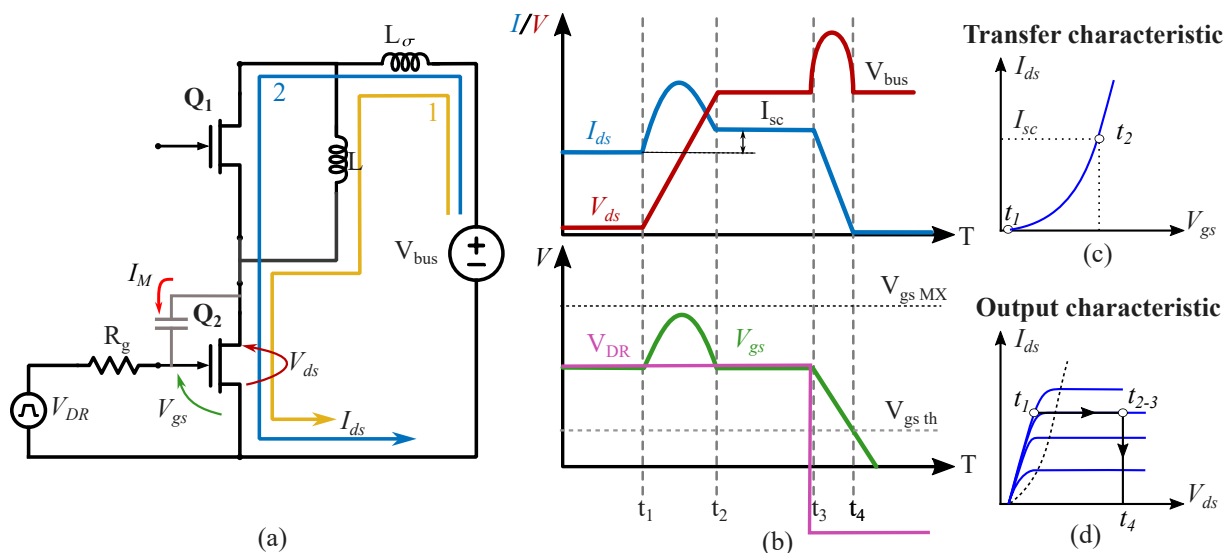


Figure 2. Hard-switching or Type II short-circuit event in (a) half-bridge configuration; (b) associated waveforms; (c) transfer characteristic; and (d) output characteristic of the transistor.

3. Behaviour of GaN E-HEMTs Under Short Circuit

Several studies have examined the performance of commercial GaN devices under SC conditions [12,13,20–22]. As mentioned above, the two main commercial GaN E-HEMT structures are SP-HEMT and GIT [23]. Both are based on the conventional HEMT architecture, which relies on a high-mobility two-dimensional electron gas (2DEG) formed at the AlGaN/GaN interface that serves as the conduction channel (see Figure 3). These HEMT structures are modified by introducing a p-type semiconductor layer beneath the gate, which depletes electrons from the channel and thereby enables normally off operation of the E-HEMT [24].

The key difference between these two normally off structures lies in the nature of the interface between the p-type semiconductor layer and the gate electrode. In SP-HEMT structure a lightly doped p-type layer forms a Schottky junction with the gate, creating a rectifying contact which prevents carrier injection (see Figure 4).

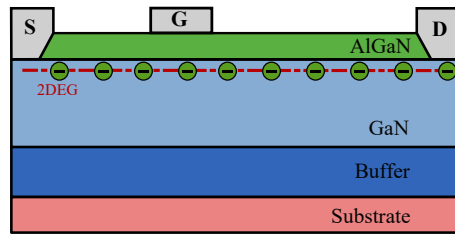


Figure 3. Schematic representation of HEMT normally on device.

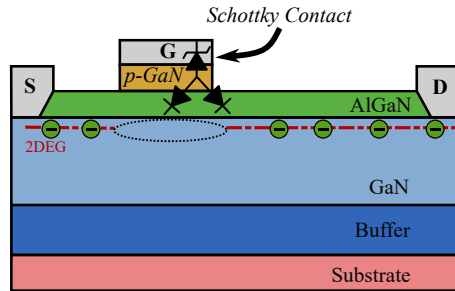


Figure 4. Schematic representation of E-HEMT normally off SP-HEMT, highlighting the nature of the gate-to-p-type semiconductor interface.

In the GIT structure, the p-type layer is heavily doped, resulting in an ohmic contact at the interface that enables direct carrier injection from the gate into the channel (see Figure 5a). As can be observed in Figure 5b, adding another p-type layer of the same doping to the drain region yields the HD-GIT structure, which could further enhance carrier injection.

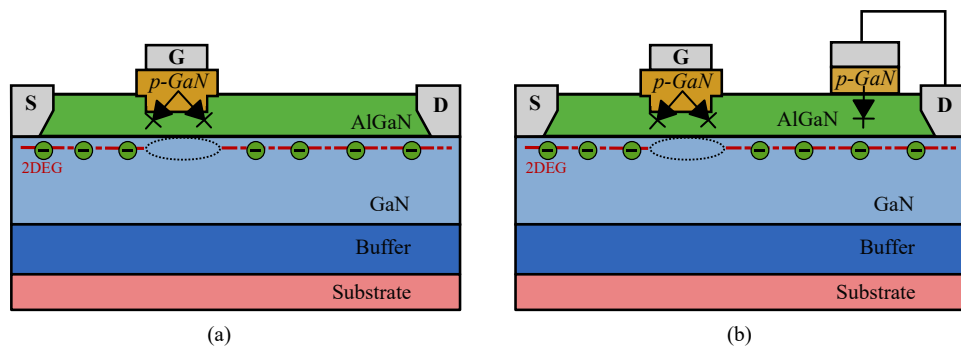


Figure 5. Schematic representation of E-HEMT normally off (a) GIT gate and (b) HD GIT structures, highlighting the nature of the gate-to-p-type semiconductor interface.

Short-circuit performance of both structures has been extensively investigated under single-event [12,20–22,25,26] and repetitive SC stress tests [14,27], with a primary focus on Type I SC conditions, providing valuable insights into device robustness and failure mechanisms.

3.1. Behaviour Under a Single Test

According to JEDEC reliability standards, a device under test (DUT) must withstand a 10 μ s SC pulse under typical operating conditions [28]. Experimental data for 600–650 V GaN E-HEMTs show that their SC withstand capability deteriorates significantly with increasing V_{ds} (see Table 1). At $V_{ds} < 300$ V, devices can typically survive SC pulses exceeding 10 μ s [12,29]. However, above 350 V, the withstand time (T_{sc}) drops below 700 ns [13], falling short of the standard by an order of magnitude.

Table 1. Single-pulse degradation parameters for different devices.

Ref.	V_{ds} (V)	V_{gs} (V)	V_{bus} (V)	T_{amb} (°C)	t_{sc} (s)	I_n (A)	I_{sc}^{peak} (A)	Device
SP-HEMT Devices								
[12]	650	6	<300	25/125	10 μ s	60 A	235 A	-
[25]	650	5	300	25	308 μ s	7.5 A	28 A	GS66502BD
[12]	650	6	350	25/125	700 ns	60 A	233 A	-
[21]	650	6.5	400	25	600 ns	60 A	130 A	GS66516T
[22]	600	4	400	23	400 ns	10 A	35 A	-
[25]	650	5	350	25	700 ns	7.5 A	35 A	GS66502BD
[20]	650	4.5	470	25	209–550 ns	7.5 A	20.6 A	GS66502BD
[20]	650	5	360	25	450–890 ns	7.5 A	24.9 A	GS66502BD
[20]	650	6	320	-	440–860 ns	7.5 A	32.3 A	GS66502BD
GIT Devices								
[26]	600	6	350	-	<10 μ s	26 A	55 A	PGA26E07BA
[26]	600	6	360	-	>500 ns	26 A	63 A	PGA26E07BA

This presents a reliability concern, especially as most GaN E-HEMTs are discrete components and their datasheets do not include SC ratings—unlike Si IGBTs and SiC MOSFET modules, where parameters like I_{sc} and T_{sc} are typically specified. Although GaN modules are beginning to emerge, the lack of standardised SC information complicates robust system design. Despite the growing adoption of GaN E-HEMTs in demanding applications, most commercial datasheets still omit explicit SC ratings. Including these ratings would significantly improve the reliability and predictability of GaN-based systems under fault.

Under an SC event, the simultaneous presence of high voltage and current induces substantial thermal stress, especially in the gate and channel regions. As the temperature rises, the electron mobility in the 2DEG degrades, leading to an increase in the drain-source resistance (R_{ds}) and, consequently, a reduction in I_{sc} . Riccio et al. [30] reported an 8% increase in R_{ds} relative to a fresh device, confirming the presence of a strong positive temperature coefficient.

The extent of these thermal effects depends not only on the 2DEG properties but also on the device structure. In particular, SP-HEMTs exhibit additional mechanisms under SC stress. The increase in temperature significantly raises the gate leakage current, which in turn induces a voltage drop across the external gate resistor (R_g). This voltage drop reduces the gate–source voltage (V_{gs}), further limiting I_{sc} . Heli et al. [12] reported a decrease in V_{gs} from 6 V to 4 V during an SC event, accompanied by a dramatic rise in gate–source current (I_{gs}) from 320 μ A to 30–37 mA.

These combined effects underscore the critical role of thermal stress in decreasing I_{sc} value by up to 70–82% [12,27,30]. This reduction in I_{sc} is more pronounced at higher V_{Bus} and T_{amb} , effectively reducing the SC energy (E_{sc}) [14,27].

The SC energy is defined as follows:

$$E_{sc} = \int_0^{T_{DUT}} V_{ds}(t) \cdot I_{ds}(t) dt, \quad (4)$$

where T_{DUT} is the SC duration.

In long SC duration tests, the DUT is subject to two distinct failure mechanisms. The first occurs at lower voltages ($V_{\text{Bus}} < 350 \text{ V}$) [13,26]. In this regime, failure is characterised by a prolonged time to failure ($t_{\text{sc}} > 10 \mu\text{s}$) and higher E_{sc} . In this regime devices typically fail due to thermal effects [26,29]. The cause of failure is the rise in junction temperature, which can exceed $727 \text{ }^\circ\text{C}$ [14,29].

The second failure mechanism is observed at higher voltages ($V_{\text{Bus}} > 350 \text{ V}$) and significantly shorter SC durations ($t_{\text{sc}} < 1 \mu\text{s}$). Here, failure occurs rapidly, and its causes are less clearly defined. Several studies suggest an electrical failure mechanism [12,26,27,29]. During hard-switching conditions, a high concentration of electrons in the channel combined with a strong electric field in the drain region leads to the generation of high-energy carriers, commonly referred to as “hot electrons” [2]. These carriers can become trapped in pre-existing or stress-induced defect states, resulting in negatively charged ions that locally enhance the electric field. This field enhancement can accelerate degradation mechanisms and ultimately trigger electrical breakdown. The density of such hot electrons increases with higher drain-source voltage (which raises carrier energy) and larger channel current (which increases carrier population) [31,32]. The corresponding trap sites are generally located in the GaN layer between the drain and the gate terminals and in the passivation layer next to the gate terminal [2] (Figure 6).

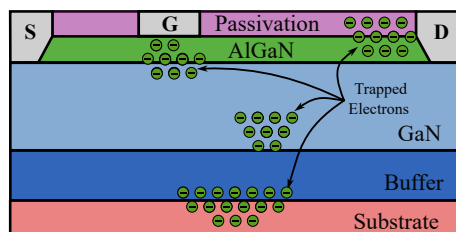


Figure 6. Trapped electron positions in a HEMT transistor. Adapted from [2].

Castellazzi et al. further suggested that SC-induced breakdown may originate within the AlGaN barrier layer of the gate stack [26]. Similarly, Huang et al. reported that device temperatures during SC events remain below $150 \text{ }^\circ\text{C}$, thus ruling out thermal breakdown and attributing failure to the high electric field stresses experienced within the device [33].

In contrast, Abbate et al. and Fernández et al. argued that the failure mechanism in GaN HEMTs is primarily driven by high power density due to current localisation, rather than charge–electric field interactions [14,20,22]. Experimental observations indicate that damage is primarily localised near the gate edge on the drain side. Complementary simulations reveal the formation of localised hot spots, with peak temperatures exceeding $827\text{--}1227 \text{ }^\circ\text{C}$. Abbate et al. also highlight that current focalization, exacerbated by device layout asymmetries, reduces the active area by up to 15% at high drain voltages (e.g., $V_{\text{ds}} = 485 \text{ V}$), intensifying localised heating and leading to thermal failure [20].

In Figure 7, Abbate et al. [20] show that the failure consistently localises at the gate edge on the drain side, directly beneath the source metal stripe. This region acts as a critical hotspot where the combined effects of high power density and current crowding induce localised thermal runaway, ultimately leading to device destruction during a single SC event.

Current studies do not provide a clear consensus on which mechanism prevails. Therefore, more detailed tests are still needed to unify these perspectives and develop robust design guidelines.

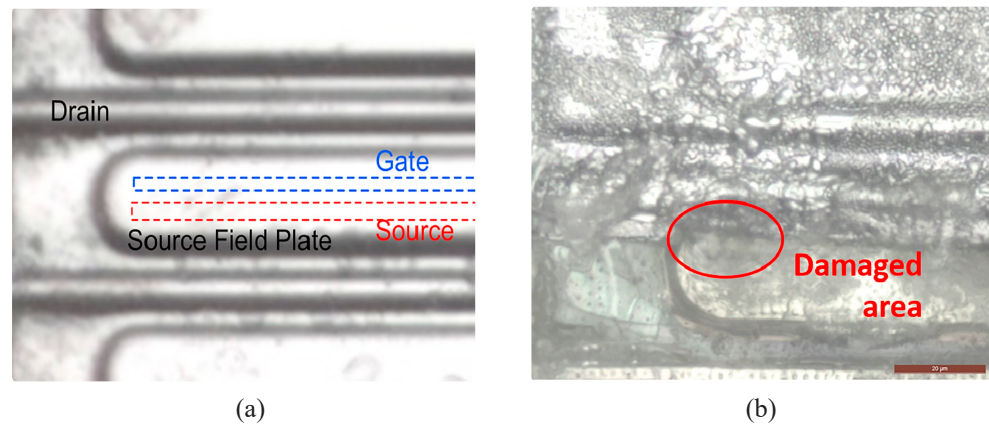


Figure 7. (a,b) Microscope image of the localised failure region in a GaN HEMT after a single short-circuit test, showing damage at the gate edge on the drain side [20].

3.2. Behaviour Under Repetitive SC Test

The repetitive SC test is a key method for evaluating transistor durability, as it assesses their capacity to withstand repeated electrical and thermal stress without performance degradation or failure. Understanding how GaN transistors respond under repetitive conditions is essential for verifying their reliability in demanding applications.

A summary of published results is provided in Table 2, detailing the conditions and number of SC pulses tolerated before degradation. Degradation is defined as the point at which the device cannot longer safely withstand the applied stress voltage [14,27].

Table 2. Repetitive test degradation for SP-HEMT devices.

Ref.	V_{ds} (V)	V_{gs} (V)	V_{bus} (V)	R_g (Ω)	I_n (A)	I_{sc}^{peak} (A)	T_{amb} ($^{\circ}$ C)	Pulses	t_p	Device
SP-HEMT										
[27]	650	6	400	16	15	73.8	23	2	1 μ s	GS66504B
[27]	650	6	200	38	15	65	23	4000	1 μ s	GS66504B
[27]	650	6	400	16	15	80	23	13	45 ns	GS66504B
[27]	650	3	400	38	15	15	23	2000	1 μ s	GS66504B
[14]	650	6/−3	200	2*	60	325	85	60	5 μ s	GS66516T
[14]	650	6/−3	200	2*	60	325	25	10	5 μ s	GS66516T
[14]	650	6/−3	200	2*	60	350	−35	5	5 μ s	GS66516T
[14]	650	6/−3	200	2*	60	−	25	10	5 μ s	GS66516T
[14]	650	6/−3	200	2	60	−	25	5	5 μ s	GS66516T
GIT Devices										
[34]	600	6	400	−	−	−	150 *	30,000	150 μ s	PGA26E07BA
[26]	600	3.5	300	−	−	−	127 *	4000	60 μ s	PGA26E07BA
[26]	600	3.5	300	−	−	−	152 *	5000	70 μ s	PGA26E07BA
[26]	600	3.5	300	−	−	−	152 *	7000	100 μ s	PGA26E07BA
[26]	600	3.5	300	−	−	−	152 *	9500	140 μ s	PGA26E07BA

The notation 2* indicates that a ferrite bead is added to the gate resistance R_g . For * GIT devices, the temperature (T_{amb}) refers to the fixed case temperature (T_{case}) during stress testing, not the peak junction temperature at failure.

For SP-HEMTs, the endurance to repetitive SC stress is highly dependent on parameters such as V_{ds} , V_{gs} , T_{amb} , and R_g . An increase in the applied V_{bus} leads to a higher E_{sc} , which in turn accelerates the onset of degradation. On the other hand, reducing V_{gs} lowers the I_{sc} peak and thus decreases the E_{sc} , allowing the device to withstand a greater number of pulses. In fact, it has been reported that adjusting V_{gs} is a more effective strategy for improving SC endurance than simply shortening the pulse duration [27].

Temperature also plays a significant role. As T_{amb} increases, the I_{sc} decreases, which helps to reduce E_{sc} and delays thermal degradation. Under identical electrical conditions, devices tested at elevated T_{amb} have shown the ability to withstand significantly more SC pulses than those tested at room temperature [14].

The gate driver impedance ($R_{\text{gon/off}}$) influences SC behaviour. In [29,35] used a large R_{gon} during activation, which prolonged device activation and lowered the I_{sc} peak. The resulting temperature rise increases gate leakage current, and when combined with a high R_{gon} , this significantly reduces V_{gs} , further limiting I_{sc} and thermal stress [13,22,35]. However, a large R_{gon} also slows activation, increasing switching losses under normal operation.

During deactivation, Galindos et al. [14] identified two failure modes depending on R_{goff} . A low value ($2\ \Omega$) caused electrical failure due to OV. Introducing a ferrite bead to increase R_{goff} mitigated OV but slowed deactivation transients, raising switching losses and shifting failure mode to thermal destruction from excessive heat.

Regarding GITs, their behaviour under repetitive SC stress differs significantly from that of SP-HEMTs. In the work by Castellazzi et al., 600 V-rated GITs were subjected to thousands of SC pulses at $V_{\text{bus}} = 300\ \text{V}$, under controlled case temperatures and pulse durations [26,34].

Under mild conditions—specifically, a pulse width of $40\ \mu\text{s}$ and a case temperature of $127\ ^\circ\text{C}$ —no signs of degradation were detected after 1000 pulses. When the pulse width was increased to $60\ \mu\text{s}$, the devices withstood at least 4000 pulses without measurable degradation. However, under more severe stress, with a pulse width of $70\ \mu\text{s}$ and an elevated case temperature of $152\ ^\circ\text{C}$, the onset of degradation was observed between 4500 and 5000 pulses. Further increasing the pulse width to values between 100 and $140\ \mu\text{s}$, while maintaining the same temperature, led to progressive performance deterioration after approximately 7000 pulses [26].

Notably, this degradation did not involve abrupt electrical failure but rather accumulated gradually due to thermal stress. Electrothermal simulations estimated that the peak junction temperature during the tests reached approximately $397\ ^\circ\text{C}$ —well below the critical thermal limit for GaN devices, typically between 577 and $627\ ^\circ\text{C}$. Nonetheless, this temperature was sufficient to initiate structural degradation. The authors attributed the observed failure to thermo-mechanical stress concentration near the gate edge, potentially leading to interlayer dielectric cracking and aluminium extrusion, which compromise device integrity over time [26].

4. Overvoltage and Surge Energy

Once the driver detects the SC, it proceeds to shut it down. During the shutdown process, OVs occur at the terminals of the device due to fast deactivation di/dt . If these OVs exceed the BV of the device, it may lead to catastrophic failure.

Some Si and SiC power devices, such as MOSFETs and IGBTs, rely on avalanche capability to withstand high currents under elevated V_{ds} . This mechanism is fundamental for circuit protection during OV or surge events. The avalanche effect, driven by impact ionisation and carrier multiplication, occurs at the pn junction of a semiconductor device [36]. During a surge event, V_{ds} rapidly increases and clamps at BV_{AV} , preventing further voltage rise (see Figure 8a). Simultaneously, I_{ds} drops to zero as the surge energy is dissipated resistively within the device. This process is crucial because it limits the electric field peak, minimising the risk of electrical breakdown. However, excessive avalanche currents, combined with high blocking voltages, can push the device beyond its thermal limits, ultimately leading to failure.

A key parameter in assessing the robustness of the avalanche device is its avalanche energy (E_{AVA}), which represents the maximum energy a device can safely dissipate without triggering thermal failure [37].

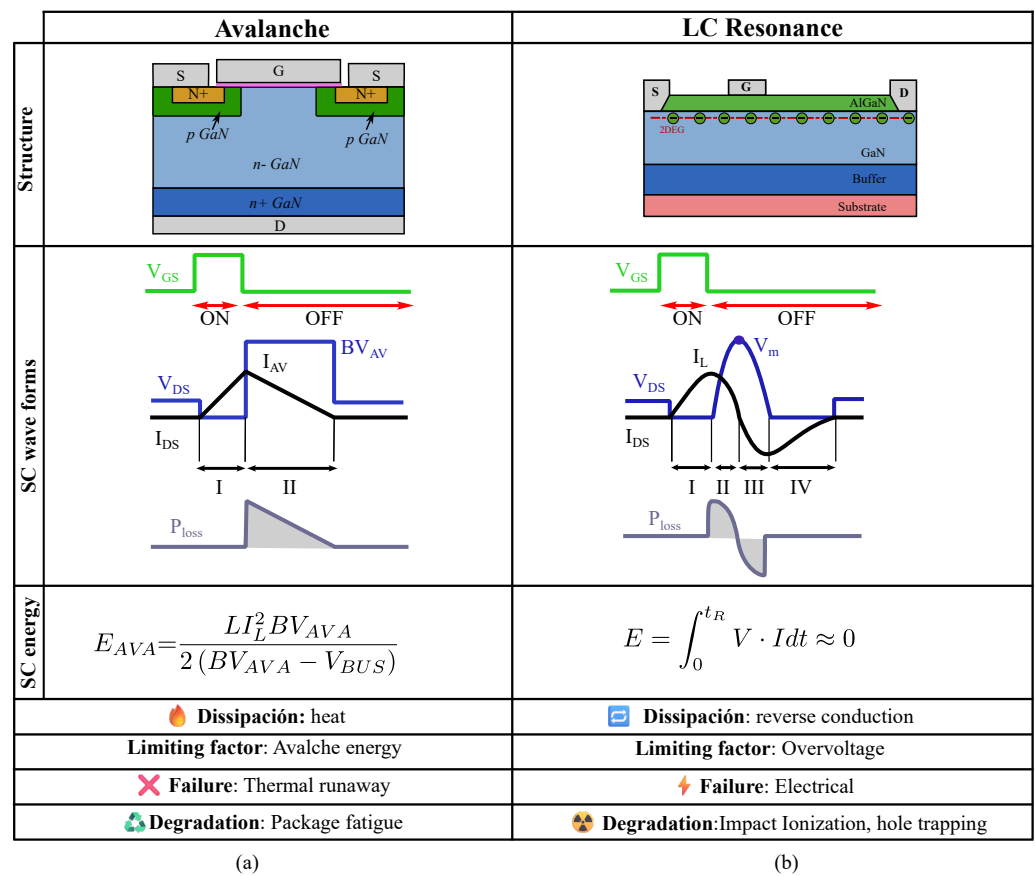


Figure 8. Cross-sectional structures of (a) vertical MOSFET devices and (b) GaN E-HEMT, with their overvoltage behaviour. Adapted from [13].

In the case of GaN HEMTs, the absence of a pn junction structure means that they lack intrinsic avalanche capability [5,13,36]. As shown in Figure 8b, unlike avalanche devices, GaN devices do not reach a fixed BV. Instead, GaN devices exhibit a rapid increase in V_{ds} . This behaviour is due to the HEMT structure, which causes resonance between its output capacitance of the device (C_{OSS}) and the parasitic inductance of the circuit.

Four distinct intervals can be identified in the waveform: during time interval I, the transistor is switched on, and the inductance stores energy (E_L). Interval II begins when the transistor switches off, transferring E_L and the source energy to C_{OSS} . Unlike avalanche devices, which dissipate this energy as heat, in this case, the transferred energy is stored. Therefore, the only power loss in this interval occurs during the charging of C_{OSS} , which is practically negligible [38]. When V_{ds} reaches its peak value, V_m , it is assumed that all the stored energy has been transferred to C_{OSS} , marking the beginning of interval III. At this stage, the current reverses direction, and the inductance starts recharging. From interval IV onwards, V_{ds} gradually becomes negative, causing the GaN device to conduct in reverse. This mechanism results in significant energy dissipation [13].

The BV ratings provided for GaN devices in datasheets typically include both dynamic and static values [39], unlike those of conventional Si and SiC devices. These ratings are conservative compared to the experimental findings in the literature. For instance, 600–650 V-rated E-HEMTs have demonstrated static breakdown voltages as high as 920 V and 1020 V, respectively [13], whereas manufacturers typically specify BV ratings between

750 V and 800 V [39]. This discrepancy reveals a substantial margin, with BV exceeding rated values by over 400 V.

The dynamic BV characteristic is influenced by pulse duration, frequency, and circuit layout [18]. For example, a 650V SP-HEMT GaN transistor exhibits a dynamic BV ranging from 1270 V to 1480 V for pulse durations between 25 ns and 500 ns, during which the device is turned off and solely withstanding the overvoltage generated by a resonant LC discharge [18]. This increase is attributed to reduced electron trapping, which mitigates local electric field enhancement. As the pulse width increases, more electrons become trapped in buffer layers or at interfaces, leading to stronger field localisation and earlier breakdown. For pulses of 2 s, the BV drops back to 950 V, confirming the time-dependent nature of the effect [13,18].

Gate Injection Transistors (GITs), particularly hybrid-drain GITs (HD-GITs), exhibit significantly more stable dynamic breakdown characteristics compared to conventional SP-HEMTs. This improvement is attributed to structural enhancements, including an ohmic-type p-gate and a p-GaN region connected to the drain, which facilitates hole injection into the 2DEG channel and buffer layers (see Figure 9). The injected holes help neutralise trapped electrons and mitigate local electric field peaks near the drain edge, a common failure initiation site in SP-HEMTs.

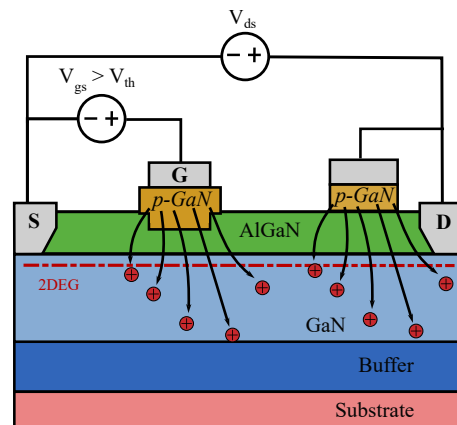


Figure 9. Hole injection in an HD-GIT transistor.

As a result, HD-GITs display a much narrower dynamic BV variation under pulsed conditions—for example, from 1180 V (25 ns) to 1095 V (500 ns) [18]—and exhibit minimal sensitivity to temperature and prolonged electrical stress. This enhanced control over transient breakdown behaviour also leads to reduced localised thermal and electrical overstress during repetitive short-circuit events. Consequently, GITs tend to sustain a higher number of SC withstand cycles compared to SP-HEMTs (see Table 2). However, meaningful endurance comparisons require consistent test conditions—including gate-source voltage, bus voltage, and PCB parasitics—to ensure that observed differences are attributable to device structure rather than circuit-level factors.

In both SP-HEMTs and GITs, if transient pulses are applied repetitively without sufficient time for detrapping, trapped charge accumulates. This results in progressive degradation of the BV. Experimental evidence confirms that both devices can survive thousands of 25 ns pulses when spaced by at least 1 ms, but shorter intervals lead to dynamic BV reduction and eventual failure [18].

Ultimately, Zhang et al. conclude that the breakdown in GaN HEMTs is not defined by intrinsic avalanche energy, but by the peak electric field generated by resonance [37]. The voltage peak V_m can be estimated as follows:

$$V_m = I_L \sqrt{\frac{L}{C}} = \sqrt{\frac{2E_L}{C}} \quad (5)$$

where L and C denote the parasitic inductance and capacitance within the switching loop.

Equation (5) suggests that surge energy alone is no longer a direct indicator of the intrinsic ruggedness of GaN HEMTs. Unlike E_{AVA} , which characterises the device's inherent and thermal robustness, failure of GaN HEMT under E_L is influenced not only by the device's capacitance and OV margin but also by the parasitic elements of the switching circuit, including stray inductances and capacitances [37].

5. Detection Systems for Short Circuit Events in GaN Transistors

In this section, several methods of SC detection systems will be briefly explained and evaluated in terms of their suitability for GaN devices.

5.1. Desaturation Detection (DESAT)

The DESAT detection technique is widely used in power electronics for SC detection, especially in Si power devices [40]. It operates by monitoring V_{ds} of a switching device after a predefined blanking time ($t_{Blanking}$), allowing the device to fully turn on and enter the ohmic region. Under normal operation, V_{ds} drops to a low value proportional to $I_{ds} \cdot R_{ds(on)}$. However, if an SC or overcurrent (OC) fault occurs, the device enters saturation and V_{ds} increases rapidly. If V_{ds} exceeds a preset threshold V_{DESAT} , the driver interprets this as a fault and initiates a deactivation sequence to protect the system.

As shown in Figure 10a, a typical DESAT protection circuit includes a high-voltage diode, a current-limiting resistor, and a capacitor connected to a comparator input. The simplicity and robustness of this approach have led to its widespread adoption in Si-based systems.

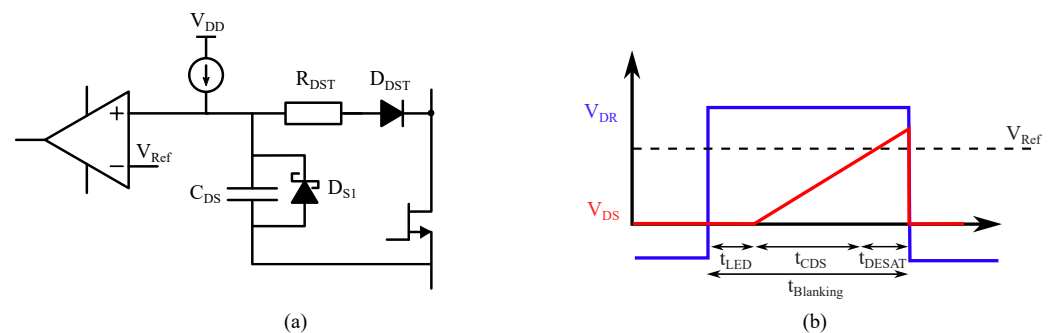


Figure 10. (a) Schematic and (b) waveforms of a DESAT short-circuit detection system

However, GaN devices present unique challenges for DESAT-based protection due to two key factors: (1) extremely short short-circuit withstand times (t_{SC}), and (2) high switching speeds with steep dv/dt . These characteristics require ultra-fast and noise-immune protection schemes to prevent device destruction or false triggering.

Standard DESAT implementations typically involve intrinsic delays that become problematic for GaN-based systems. As can be seen in Figure 10b, the driver response comprises two main delays: the leading-edge blanking time (t_{LEB}), which is the delay before the DESAT detection circuitry begins to source current (typically around 400 ns), and the DESAT response time t_{DESAT} , which is the delay from comparator threshold crossing (V_{Ref}) to gate turn-off initiation (often around 415 ns at 10% gate voltage level) [41]. These combined delays can approach or exceed the SC withstand time of GaN HEMTs, which may be in the range of nanoseconds, rendering conventional DESAT protection insufficiently fast.

Unlike conventional implementations, the architectures proposed in [15,42,43] effectively eliminate both major sources of delay in DESAT-based protection. First, t_{LEB} is inherently avoided, as the detection circuit is powered by the gate supply and does not rely on a current source with delayed activation. Second, t_{DESAT} —which in traditional drivers corresponds to the delay from comparator output to gate turn-off—is also removed. In these approaches, the detection circuit is directly connected to the GaN gate terminal and actively initiates the protection sequence, bypassing the internal logic and propagation delays of the gate driver. As a result, the total fault response time is significantly reduced, reaching values compatible with the nanosecond-scale SC withstand capability of GaN E-HEMTs.

Although reducing response time was the main objective of these studies, alternative approaches have placed greater emphasis on enhancing noise immunity under high dv/dt conditions. For instance, in [44], the authors introduced a discharge capacitor to suppress false triggering caused by high dv/dt transients. Their solution achieves a response time of 110 ns and can withstand dv/dt noise levels of up to 84 V/ns, significantly enhancing the reliability of GaN devices under SC conditions.

Further improvements are presented in [45], where Schmitz et al. eliminated the high-voltage DESAT diode and implemented an RC voltage divider to directly monitor V_{ds} . This approach reduced the overall fault detection time to less than 56 ns and enhanced noise immunity, making it highly suitable for GaN-based applications.

5.2. Shunt Resistor-Based Detection

A common method for detecting SC or OC conditions involves placing a low-value resistor in series with the transistor and monitoring the voltage drop across it (see Figure 11a). If this voltage exceeds a predefined threshold, a fault detection mechanism is triggered. However, this approach has notable drawbacks for power converters in practical applications: it introduces additional conduction losses and, more critically, adds stray inductance to the commutation loop, which deteriorates switching performance, increases EMI, and aggravates OV issues [16,46].

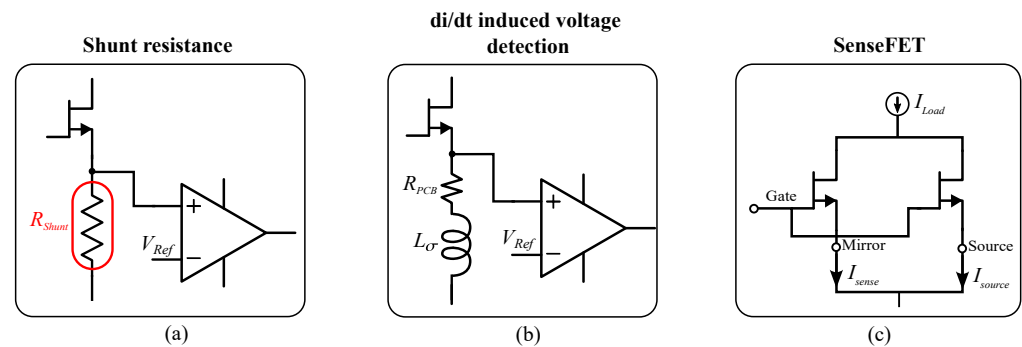


Figure 11. Schematic comparison of short-circuit detection strategies: (a) shunt resistor sensing, (b) di/dt -induced voltage detection, and (c) SenseFET-based sensing

5.3. di/dt -Induced Voltage Detection

SC detection based on di/dt -induced voltage monitoring exploits the voltage drop across parasitic inductances in the current path to sense rapid changes in current (see Figure 11b). When an SC event occurs, the drain current I_{ds} increases extremely quickly, leading to a substantial di/dt that induces a voltage across the parasitic inductance L_{σ} according to Faraday's law:

$$V_{\text{ind}} = L_{\sigma} \cdot \frac{di}{dt} \quad (6)$$

This induced voltage can be sensed directly on the PCB traces or across purposely introduced low-inductance measurement points to infer the occurrence of a fault.

Ozturk et al. [16] proposed a detection scheme for GaN HEMTs based on sensing the voltage drop across the combined parasitic inductance and resistance of PCB traces. This method detects high slew-rate SC faults using the inductive voltage drop and slower OC faults using the resistive voltage drop. However, it faces challenges such as temperature sensitivity, complex signal processing, and stringent PCB layout constraints, which increase design complexity. Similarly, Acuña et al. [47] proposed a PCB-integrated current sensor that measures the magnetic stray field generated by the current of the transistor. This method eliminates the need for blanking times, enabling ultra-fast SC detection with response times as low as 30 ns.

Other approaches, proposed by He et al. and Kim et al., are based on detecting the voltage drop across the phase-leg DC bus caused by di/dt and parasitic inductances [48,49]. This method leverages the voltage fluctuations in the DC bus to detect SC faults, providing an alternative to PCB trace measurements. However, sensing the voltage across parasitic inductance is not always practical for GaN devices due to their minimized stray inductance, which reduces the measurable voltage signal [15].

5.4. SenseFET-Based Detection

Another approach involves integrating a senseFET into the power module, connected in parallel with the main device to scale down the device current [50]. As can be seen in Figure 11c, the senseFET is embedded within the power module and it generates minimal noise due to its reduced parasitic inductance. The scaled-down current is then measured using a precision shunt resistor. This configuration allows for rapid fault detection, as the sensed current remains synchronized with the device current, ensuring a fast response time under fault conditions [46]. For instance, the Texas Instruments LMG341X series of GaN power stage ICs can turn off the GaN FET in less than 100 ns during an OC or SC event [46]. Despite its advantages, the higher cost and manufacturing complexity of integrating a senseFET into the power module remain significant drawbacks, limiting its widespread adoption.

5.5. Gate Charge Monitoring

Gate charge monitoring is an SC detection technique based on analyzing the behaviour of the gate–source voltage V_{gs} and the corresponding gate charge during the switching process. Under normal operating conditions, the device exhibits a characteristic Miller plateau in the V_{gs} waveform. This plateau occurs due to the charging of the gate–drain capacitance C_{gd} while the drain–source voltage V_{ds} transitions, effectively clamping V_{gs} during this interval.

In the event of a SC, V_{ds} remains high because the load current cannot commutate. As a result, the voltage across C_{gd} , and the current required to charge it is minimal. This causes the Miller plateau to reduce or disappear entirely. By evaluating the shape and timing of the V_{gs} curve—particularly after a defined blanking time t_b —the gate driver can distinguish between normal switching and a fault condition. The absence of a plateau is indicative of a potential SC event.

This method has proven effective for IGBTs, where the large C_{gd} results in a well-defined Miller plateau that can be reliably detected. However, its applicability to WBG devices is significantly limited—as illustrated in Figure 12, which compares an IGBT with a SiC MOSFET. The limitation is even more pronounced in GaN HEMTs, due to their inherently low C_{gd} and extremely fast switching behaviour. These characteristics lead to a minimal Miller plateau even during normal operation. Consequently, the difference

between a normal turn-on and an SC event becomes nearly indistinguishable when observing V_{gs} or Q_g , severely reducing the reliability of this detection approach in GaN-based systems [40].

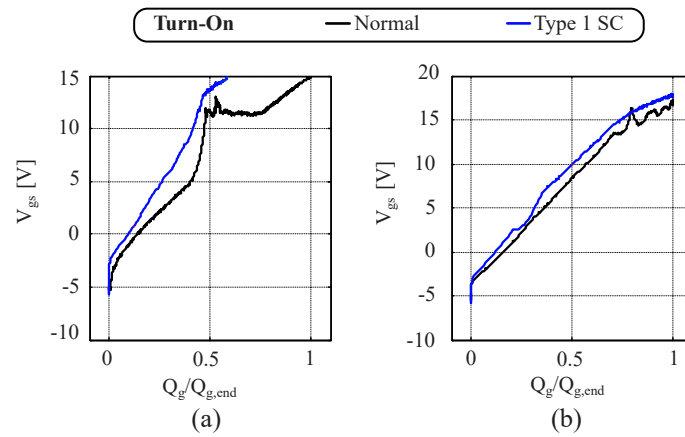


Figure 12. Measured gate charge characteristic for normal activation and under HSF of (a) IGBT and (b) SiC MOSFET. Adapted from [40].

5.6. Emerging Techniques

In addition to the methods discussed above, Jones et al. [51] propose an SC protection scheme tailored specifically for GIT transistors. This method exploits the near-linear relationship between the steady-state gate–source voltage V_{gs} and the drain current I_{ds} , enabling V_{gs} to act as an indirect sensor for current magnitude.

The operating principle relies on the fact that, in GaN GITs (see Figure 13), a steady-state gate current I_{gs} (typically 10–50 mA) is required to maintain the 2DEG channel. The external gate voltage $V_{gs,ext}$, which includes the voltage drop across the internal resistance r_1 , varies proportionally with I_{ds} according to Ohm’s law:

$$V_{gs,ext} = V_{ac} + r_1 \cdot (I_{ds} + I_{gs}) \tag{7}$$

where V_{ac} represents the voltage drop across the clamping diode and r_1 is the resistance in the measured channel region.

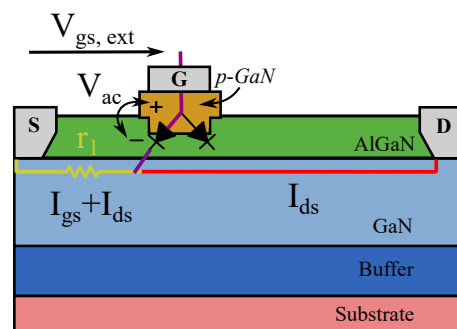


Figure 13. Detection method with internal architecture for GIT.

By continuously monitoring $V_{gs,ext}$, the circuit detects when the current exceeds a predefined threshold, indicating an overcurrent or SC condition. Once the sensed voltage surpasses a reference level, a high-speed comparator triggers the gate driver to turn off the device.

This circuit achieves a fault response time of less than 70 ns. [51]. Additionally, it avoids direct interaction with high-voltage drain terminals, reducing parasitic effects and switching losses.

However, this approach is limited to GaN GITs and cannot be applied to voltage-driven enhancement-mode GaN devices such as SP-HEMTs, which do not require steady-state gate current and lack the V_{gs} - I_{ds} correlation utilized in this technique.

Table 3 reviews and compares the suitability of the main short-circuit detection schemes for GaN E-HEMTs. It summarises their key advantages and limitations, as well as typical response times, implementation complexity, and cost considerations.

Table 3. Comparative summary of short-circuit detection schemes for GaN E-HEMTs [40,52].

Detection Scheme	Pros	Cons	Response Time	Complexity	Cost
DESAT	Simple, widely used	Poor noise immunity	+	Low	Low
Shunt Resistor	Direct current sensing	Adds losses, stray inductance	++	Medium	Low
di/dt	Fast response, no extra resistor	Layout sensitive, susceptible to noise	++	Medium	Low
SenseFET	Accurate	Requires module-level integration	++	High	High
Gate Charge	Uses existing gate signal	Unreliable for GaN due to low C_{gd} , SNR	++	Low	Low
GIT V_{gs} Monitoring	Fast	Only suitable for GITs, SNR	++	Medium	Medium

+ fast and ++ very fast response time .

This comparative overview underscores that, although techniques such as DESAT remain widely adopted due to their simplicity and ease of integration, they often fall short in terms of speed and robustness for modern GaN applications. In contrast, high-speed alternatives like di/dt sensing and SenseFET-based approaches offer significantly faster response times but typically involve added circuit complexity or cost. Gate charge monitoring provides a more cost-effective solution; however, its effectiveness is limited in GaN devices due to their inherently low C_{gd} and poor signal-to-noise ratios (SNR). Meanwhile, techniques based on gate current or voltage monitoring in GIT devices have demonstrated their feasibility, although their applicability is restricted to specific GaN architectures and this method also suffers from SNR.

6. Mitigation Strategies for Short Circuit Events in GaN Transistors

Once SC is detected, the protection circuitry initiates a turn-off sequence to terminate the fault condition. However, a rapid interruption can induce OVs due to high di/dt and parasitic inductance in the circuit. These transient OVs may exceed the device's BV, thereby posing a risk of failure.

For Si and SiC devices, especially those lacking avalanche capability, OV protection typically involves active clamping. This is triggered when the drain to source voltage exceeds a set threshold and acts on the gate terminal to limit the transient. As shown in Figure 14, the feedback branch generally includes one or more transient voltage suppressors (TVS) that define the clamping level.

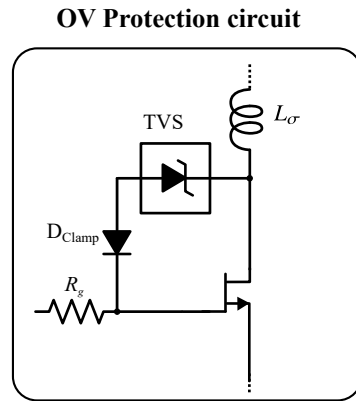


Figure 14. Schematic of overvoltage (OV) protection circuit using TVS clamping.

In contrast, using external TVS devices for GaN HEMTs is not straightforward. The effective BV of GaN devices is dynamic—it depends on temperature, traps, and manufacturing tolerances—making it difficult to set a fixed threshold for an external clamp. If the clamping level is too low, the circuit may trigger unnecessarily and reduce system efficiency; if it is too high, the device may already be damaged by the time clamping occurs. For these reasons, conventional TVS-based solutions are often ineffective for GaN.

Instead, recent approaches for GaN OV protection focus on internal active clamping, where the device is intentionally turned on during an OV event to safely conduct the excess energy and avoid breakdown [53]. Despite this, most commercial GaN implementations still prioritize SC detection and fast turn-off over dedicated OV management [43,54]. This is partly because GaN transistors are usually designed with larger voltage margins to tolerate transients passively, but if the critical electric field is exceeded, failure is immediate and irreversible. Therefore, it remains unclear whether OV should be actively limited or tolerated. Moreover, under SC conditions, for a given peak current and parasitic inductance, it is uncertain whether allowing LC resonance—risking breakdown—or clamping the voltage—risking trap generation—is the safer approach.

Unlike Si and SiC devices that can be safely disabled by simply removing the gate drive voltage, GaN transistors require more sophisticated, multi-stage mitigation strategies due to their ultra-short SC withstand times and vulnerability to deactivation-induced OVs. Table 4 presents a comparison of detection, extinction, and total times reported for different short-circuit protection techniques.

Table 4. Comparison of detection and extinction times for different protection methods.

Ref.	Det. (ns)	Ext. (ns)	Total (ns)	I_n (A)	I_{sc}^{peak} (A)	V_{DSS} (V)	V_{br}^{sc} (V)	V_{bus} (V)	V_{gs} (V)	Device
DESAT Detection										
[45]	56	95	151	60	280	650	444	400	5.5	GS66516T
[54]	82	44	126	30	147	650	520	400	5	GS66508B
[55]	120	83	203	12	38	200	-	50	5	EPC2010
[44]	110	150	-	30	110–120	650	-	270	6	GS66508P
[42]	160–250	150	310–400	120	500	650	-	400	6	-
[43]	276	817	1000	50	-	650	-	400	-	TPH3207WS
Shunt										
[56]	-	-	100	22.5	-	650	-	200	6	GS66506T

Table 4. Cont.

Ref.	Det. (ns)	Ext. (ns)	Total (ns)	I_n (A)	I_{sc}^{peak} (A)	V_{DSS} (V)	V_{br}^{sc} (V)	V_{bus} (V)	V_{gs} (V)	Device
<i>di/dt</i> Induced Voltage Detection										
[16]	30	340	370	90	70.7	100	-	48	6	GS61008T
[57]	40	210	250	30	-	650	-	400	6	GS66508T
[47]	20	40	60	30	50	650	250	200	6.5	GS66506T
[48]	100	181	281	60	-	650	-	400	6	-
[49]	-	-	257	11	-	650	-	400	6	GS0650111L
[58]	100–150	250	400	15	45	650	-	400	6	GS66504B
SenseFET Detection										
[52]	-	-	100	-	-	-	-	-	-	-
GIT Detection										
[51]	>70	-	>70	19	37.5	600	622	400	-	PGA26E19BA

Most of the protection strategies proposed in the literature [16,43,45,47,48,54], follow a common approach: once the SC event is detected, a resistive voltage divider is temporarily applied to the gate to reduce V_{gs} . This reduction forces the transistor into its active region, thereby lowering I_{sc} and consequently reducing E_{sc} . By minimising V_{gs} in this manner, the device can tolerate the fault for a longer duration before catastrophic failure, compensating for inherent delays in the driver core that could otherwise result in late turn-off.

In this context, Derkacz and Musznicki [43] introduced a gate driver incorporating a two-stage protection circuit specifically designed for GaN transistors. This circuit employs an integrated driver for fast and reliable operation. The first stage involves a fast comparator that triggers a switch to quickly lower V_{gs} , initiating a soft turn-off. The second stage completes a hard turn-off by fully disengaging the driver. This two-stage mechanism achieves a response time of 281 ns. Experimental results validate the effectiveness of this driver in protecting GaN transistors in high-frequency applications, with a blanking time of 330 ns to ensure safe operation during standard switching transients.

Similarly, Hou et al. [54] propose a two-stage protection mechanism. Unlike the integrated driver approach in [43], this circuit is implemented using discrete components, providing greater design flexibility and cost-effectiveness. The first stage involves a soft turn-off, where V_{gs} is gradually reduced to limit OV. The second stage enforces a hard turn-off, completely disabling the transistor. This method achieves a response time of 85 ns for the first stage and 125 ns for the second stage.

7. Future Trends in Short-Circuit Detection and Protection for GaN E-HEMTs

Based on the findings reviewed in this work, several promising trends and research directions can be identified to address the persistent challenges associated with SC detection and OV protection in GaN E-HEMTs for high-power applications.

As shown in Table 4, recent research efforts in GaN SC detection predominantly focus on two strategies: optimised DESAT implementations and *di/dt*-induced voltage detection. Although DESAT circuits were initially too slow for GaN applications, recent improvements have significantly reduced their response times—often below 100 ns—while preserving simplicity and ease of integration [15,42,43]. In parallel, *di/dt*-based schemes offer ultra-fast detection without intrusive current sensors, making them well suited for high-speed GaN switching where minimal additional parasitics are critical.

These two approaches currently dominate the landscape of SC detection research. DESAT remains the preferred solution in industrial settings where cost-effectiveness and mature integration are priorities. Conversely, di/dt detection is increasingly adopted in experimental and high-performance applications due to its faster transient response and ability to detect faults at the nanosecond timescale. Nevertheless, both methods present trade-offs: DESAT circuits are still vulnerable to false triggering under high dv/dt conditions, while di/dt sensing is highly sensitive to PCB layout and parasitic elements, which can compromise detection reliability if not carefully managed.

Most protection strategies, once a fault is detected, proceed to shut down the device as quickly as possible, often by lowering V_{gs} to limit the fault current before fully turning the switch off [16,43,45,47,48,54]. This approach effectively minimises driver-related delays and reduces SC energy. The protection strategy must be carefully designed to avoid degrading system performance. Improperly implemented protection schemes can introduce additional parasitic capacitance and resistance at the gate node, which increases the effective gate charge (Q_g) and slows down switching transitions. This leads to longer overlap periods of voltage and current, directly reducing conversion efficiency. Moreover, abrupt gate discharging or poorly damped switching events can generate excessive dv/dt and di/dt , becoming significant sources of EMI. Therefore, protection circuits for GaN switches must be designed to shut down the device quickly and safely during faults, but without introducing parasitic elements that increase electromagnetic noise or reduce converter efficiency.

However, nearly all actual solutions focus exclusively on current extinction and largely overlook the associated OV spikes generated during the rapid deactivation process. As can be seen in Table 4, very few studies provide detailed information on the magnitude of these voltage transients, despite their critical role in device failure.

A promising future direction is therefore the development of detection and protection schemes that simultaneously manage quick response, high noise immunity, and minimal sensitivity to layout variations. Future research should address the overlooked OV aspect equally to ensure safe and robust deployment of GaN devices in demanding high-power applications.

8. Conclusions

This review has comprehensively examined the SC and OV failure mechanisms of GaN enhancement-mode high-electron-mobility transistors (E-HEMTs), as well as the protection strategies developed to address these critical reliability challenges. While GaN technology offers significant performance benefits—such as high switching speed, low on-state resistance, and compact device size—its intrinsic limitations in fault tolerance remain a primary obstacle to deployment in high-power applications.

Firstly, GaN devices exhibit extremely limited SC withstand times—typically below 700 ns—making them highly vulnerable to thermal and electrical overstress. The lack of avalanche capability and the dominance of resonant turn-off behaviour render conventional Si and SiC protection approaches ineffective. Unlike robust avalanche-clamped Si or SiC devices, GaN transistors cannot safely dissipate the energy associated with fault-induced voltage spikes, and their breakdown voltage varies dynamically with operating conditions, pulse width, and charge trapping.

Secondly, device architecture plays a decisive role in failure dynamics. SP-HEMTs suffer from severe gate leakage, thermal degradation, and localised hot-spot formation, especially under repetitive stress. In contrast, GITs—and particularly HD-GITs—demonstrate greater resilience to both SC and OV events, attributed to improved hole injection and trap neutralisation mechanisms that mitigate electric field crowding and charge accumulation.

These structural features confer a narrower and more predictable dynamic breakdown voltage profile, enhancing their suitability for repetitive high-stress conditions.

Thirdly, conventional DESAT-based fault detection methods are generally inadequate for GaN due to slow response times and poor noise immunity. However, recent advancements have achieved detection times under 150 ns with improved dv/dt robustness. Alternative approaches—such as di/dt -induced voltage sensing, integrated SenseFETs, and gate charge monitoring—offer faster and more reliable detection, although they require more complex circuitry than the classic DESAT technique.

Finally, two-stage protection circuits have emerged as one of the most effective mitigation strategies. These typically consist of an initial soft turn-off phase—achieved by lowering the gate–source voltage to reduce fault current—followed by a hard turn-off to fully disable the device. However, during the second stage, the di/dt cannot be directly controlled since the turn-off speed is dictated solely by the gate voltage, potentially leading to hazardous overvoltage conditions.

In conclusion, improving the reliability of GaN E-HEMTs in high-power systems requires high-speed detection and advanced fault mitigation techniques. Future research should focus on developing protection solutions with fast response and strong noise immunity, as well as on establishing standard SC and OV robustness metrics to support the safe and scalable adoption of GaN technology.

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