Silicon Application Extension Versus WBG Due to Partial Power Processing

Jon Anzola├, Shrivatsal Sharma┤, Iosu Aizpuru├ and Subhashish Bhattacharya┤

├Mondragon Unibertsitatea, Hernani, Spain. Email: *janzola@mondragon.edu, iaizpuru@mondragon.edu*

┤North Carolina State University, Raleigh, USA. Email: *ssharm39@ncsu.edu, sbhatta4@ncsu.edu*

***Abstract*— This paper discusses the new possibilities that partial power processing offers to implement silicon semiconductors compared to wide-bandgap technologies. With this purpose, an on-board charger application is presented as a case study in which wide-bandgap semiconductors based full power converters are compared with silicon semiconductors based partial power converters. The comparison is made using the total energy loss over a complete charge cycle. The total energy loss is calculated using the switching loss and conduction loss of the devices. The zero-voltage switching regions for both full power and partial power topologies are also considered while calculating switching losses. Using circuit simulations, it is concluded that the partial power processing converters with silicon based devices have better efficiency and reduced cost than full power converters with wide-bandgap based devices.**

Keywords—Silicon, wide-bandgap, partial power processing, dual active bridge

I. INTRODUCTION

Higher energy efficiency, reduced power converter size and prolonged reliability are the main benefits that wide-bandgap (WBG) devices present against conventional Silicon (Si) based semiconductors [1], [2]. Furthermore, these WBG semiconductors permit devices to operate at much higher voltages (typical application of Silicon Carbide, SiC), higher frequencies (typical application of Gallium Nitride, GaN), and temperatures than the conventional Si semiconductors [3]. Consequently, crucial applications such as solar, traction, and electric vehicles (EV) are already implementing power converters with WBG-based devices [4]. On the other hand, Si-based devices have matured, and so they still dominate the market of power devices due to their reduced cost and ruggedness. However, their performance has reached its theoretical limitations in terms of power density and switching capability [5].

Recent literature around power converter designing presents partial power processing (PPP) based strategies as promising solutions that help reduce the power converter's footprint and improve system efficiency [6]. The PPP strategies improve efficiency by reducing the power processed by the power converter. To explain this, Fig. 1 presents a power flow comparison between a full power processing (FPP) solution and a PPP one. As it can be observed, an FPP converter (Fig. 1a) processes the 100% of the source power. However, a PPP (Fig. 1b) converter only processes a fraction of the power flowing from the source to the load. According to the literature, three different types of PPP strategies exist for DC-DC applications [7]: differential power converters (DPC), partial power converters (PPC), and mixed strategies. DPCs are aimed to correct the current imbalances that exist between different elements connected in series to a common voltage bus [8], [9]. The main goal of

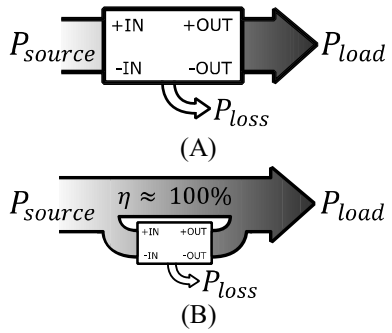

Fig. 1. Power flow diagram. A) FPP. B) PPP.

PPCs is to control the power flow between a source and a load with a different voltage or current level [10], [11]. Finally, the mixed strategies group contains other solutions that offer better performance than DPCs and PPCs at specific conditions.

Focusing on PPC architectures, many recent works have achieved the reduced size and more efficient solutions than FPP architectures. For example, authors in [12] prove that PPP can be achieved with a PPC architecture if an adequate isolated topology is implemented, for example, a phase-shifted full-bridge (PSFB). Also, [13] concludes that a dual active bridge (DAB) topology implemented on a PPC architecture achieves a reduced electrical stress and efficiency improvement compared to its FPP architecture due to the reduction of the power processed by the converter. The reduced power processed by the converter can help conventional Si -based devices to compete with upcoming SiC-based devices. Si-based devices are a very mature technology, and their market offers highly competitive semiconductors in terms of conduction resistance and current capability. So, if these advantages are combined with the benefits that PPP presents, Si semiconductors may provide better solutions than WBG-based FPP solutions. For this reason, the present paper aims to analyze the benefits that PPP can bring to the life extension of Si-based technology.

The paper is organized as follows. Section II describes the basis of PPC architectures. In Section III, details of the application and the devices selected for the analysis are presented. Section IV presents simulation results and, finally, Section V summarizes the main conclusions.

II. PPC ARCHITECTURES DESCRIPTION

There exist two main PPC architectures: Input-Parallel-Output-Series (IPOS, Fig. 2a) and Input-Series-Output-Parallel (ISOP, Fig. 2b). Depending on the operating conditions, each architecture achieves a different reduction of the power processed by the converter (P_{conv}). This can be compared by calculating the partial power ratio (K_{pr}), which consists of the ratio of the converter power to the system

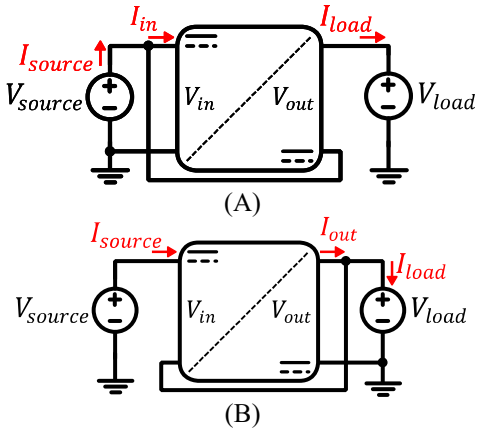

Fig. 2. PPC architectures. (A) IPOS. (B) ISOP.

$$K_{pr} = \frac{P_{conv}}{P_{source}} \quad (1)$$

$$K_{pr_{IPOS}} = 1 - \frac{\eta}{G_V} \quad (2)$$

$$K_{pr_{ISOP}} = 1 - G_V \quad (3)$$

$$G_V = \frac{V_{load}}{V_{source}} \quad (4)$$

power (1). Applying Kirchhoff's laws on both architectures, their corresponding K_{pr} curves are obtained in function of the static voltage gain (G_V), see (2), (4). Where η is the efficiency of the system and $K_{pr_{IPOS}}$ and $K_{pr_{ISOP}}$ are the processed power ratios of the IPOS and ISOP architectures. In this study, it is considered as ideal (η=1). Fig. 3 shows the resulting curves.

From Fig. 3, several conclusions can be obtained. First, it is observed that as G_V approaches 1, K_{pr} decreases for both IPOS and ISOP architectures. This means that the smaller the difference between the output and input voltage, the less power the converter will process. Secondly, if the application requires only voltage boost ($G_V > 1$), the architecture that obtains lower K_{pr} values is IPOS. In fact, its K_{pr} curve never exceeds the value of 1 when working in boost mode. On the contrary, the ISOP architecture obtains K_{pr} values less than -1 when G_V is greater than 2. When G_V is greater than 2, the converter does not operate in the partial power range, thus losing all advantages. Thirdly, if the application requires only to reduce the voltage ($0 < G_V < 1$), the architecture that obtains lower K_{pr} values is the ISOP. As in the previous case, in buck mode, the ISOP architecture never exceeds the value of 1 for K_{pr}. However, the IPOS architecture does when G_V is less than 0.5. Finally, if the application requires buck-boost functionality, the power converter will enter in the shaded blue (IPOS case) and red (ISOP case) areas from Fig. 3. At these regions, the K_{pr} curve achieves negatives values, which means that the power flow inside the converter is reversed [11], [14], [15]. In the case of the IPOS, the polarization of V_{out} is inverted and the flow of I_{in} changes its direction to the opposite way. Same thing occurs with the ISOP step-down (Fig. 2b) for step-up applications. In this case, the polarity of V_{in} and the direction of I_{out} must be inverted. To sum up, the IPOS architecture is the optimal solution for purely boost applications and the ISOP for purely buck applications. If the application consists of a buck-boost, the selection between the IPOS and the ISOP is not that evident and it requires a more complex comparison.

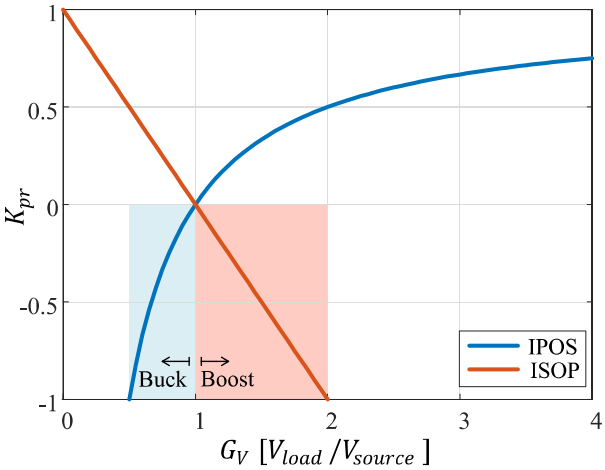

Fig. 3. K_{pr} curves of IPOS and ISOP architectures.

Table 1. Main electrical parameters of the concerned OBC application.

Parameter	Value
V_{DC} [V]	340
V_{EV} [V]	195÷320
P_{DC} [kW]	20

Table 2. Design parameters of the DAB-FPC and the DAB-PPC.

Parameter	DAB-FPC	DAB-PPC
V_{in} [V]	340	146÷20
V_{out} [V]	195÷320	195÷320
n (turns ratio)	1.12	0.2
L [µH]	15.3	2.72
C [µF]	300	300
$P_{conv_{MAX}}$ [kW]	20	5.2
f_{sw} [kHz]	50	50

III. System Description

A. Application definition

This paper focuses on an on-board charger (OBC) application. Usually, an OBC is divided in two main stages [16]: AC-DC rectification stage and DC-DC stage. The first one operates as power factor corrector (PFC) and it is in charge of supplying the DC link between both stages. Whereas, the second one supplies the battery of the EV. This work is focused on the design of the DC-DC converter. In relation to the normative around EV charging systems, at present, the majority of countries implement isolated DC-DC converters. This negatively affects the implementation of the PPC architectures as they proved non-isolated solutions. However, the requirement of galvanic isolation for OBC application is not a mandate, and the application of non-isolated supply equipment is allowed for EV charging [17]. To be more precise, the only countries that are included at the corrigendum of the IEC 61851-23 normative are the United States and Canada. Table 1 presents the main electrical

Table 3. Selected MOSFETs for the analysis.

ID	Semiconductors	Technology	V_{DS} [V]	I_D [A]	R_{DS} [mΩ] @ 25ºC	Cost [$/unit]
UF3SC065007K4S	Q_{1-8} (DAB-FPC)	SiC	650	120	6.70	59.52
C3M0015065D	Q_{1-8} (DAB-FPC)	SiC	650	120	10.5	28.18
TP65H015G5WS	Q_{1-8} (DAB-FPC)	GaN	650	95	15	25.53
IPT111N20NFD	Q_{1-4} (DAB-PPC)	Si	200	96	9	8.78
IPT65R033G7	Q_{5-8} (DAB-PPC)	Si	650	69	29	11.04

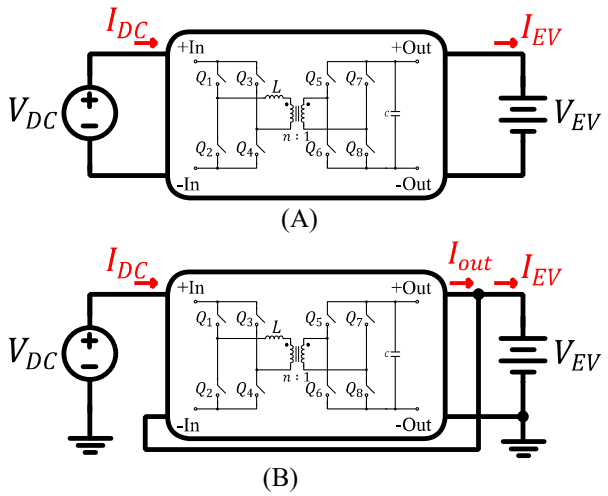

Fig. 4. Simplified electrical diagram. A) WBG-based DAB-FPC. B) Si-based DAB-PPC.

parameters of the application. According to the SAE J1772 standard, the DC bus voltage can be established at 340 V (peak value of a rectified 240 V single phase). Typically, the maximum voltage of ESS also does not exceed 380 V [18] For the considered system, the maximum voltage level of the EV is defined at 320 V (which corresponds to the VW e-Golf) and the maximum power is stablished at 20 kW.

Fig. 4 shows the schematic of the two topologies which are compared. Fig. 4a shows the schematic of a WBG based dual active bridge full power converter (DAB-FPC), and Fig. 4b Si based dual active bridge partial power converter (DAB-PPC). Regarding the DAB-PPC, since the application consists of a voltage step-down, an ISOP architecture is implemented. This way, reduced voltage level is expected at the primary side ($V_{in} = V_{DC} - V_{EV}$) and reduced current at the secondary side ($I_{out} = I_{EV} - I_{DC}$). Topology wise, the DAB is selected for its bi-directionality and zero voltage switching (ZVS) operation. In this work, DAB is controlled with single phase-shift modulation (PSM) [19].

Table 2 specifies the design parameters of the DAB-FPC and the DAB-PPC. As it can be observed, the maximum input voltage of the DAB-PPC is expected around 140V. Therefore, lower voltage rated Si-based devices which offer much less on-state resistance than the higher voltage rated WBG-based devices can be implemented. This will result in lower conduction losses in the primary bridge of the converter. A detailed comparison of the semiconductors that will be implemented for the analysis is presented in Table 3.

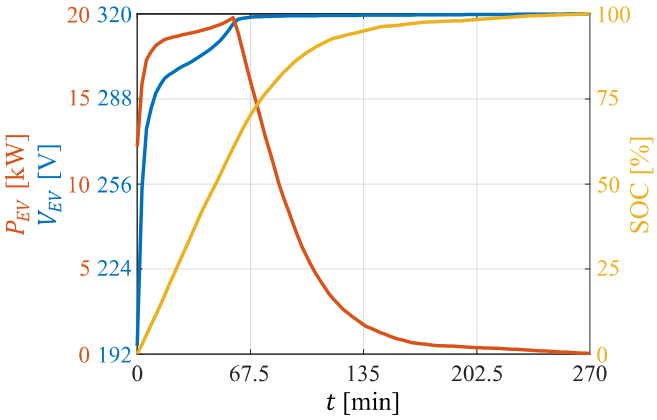

Fig. 5. Modelled EV's charging curves.

Based on the application presented in Table 1, it can be observed that the DAB-FPC will work with a fixed input voltage ($V_{in} = V_{DC}$) and a variable output voltage ($V_{out} = V_{EV}$). Whereas, the DAB-PPC contains a variable input voltage ($V_{in} = V_{DC} - V_{EV}$) and a variable output voltage ($V_{out} = V_{EV}$). In consequence, the voltage gain observed by the converter ($M = \frac{V_{in}}{V_{out} \cdot n}$) extends its operation range and the ZVS region of the PPC is affected. This is discussed later in this section.

The comparison of the two topologies is made by considering the open-circuit voltage (OCV) vs. state of charge (SOC) of the traction battery. The typical OCV vs. SOC characteristics are shown in Fig. 5 [20]. Focusing on the OCV curve, it is observed that it varies from 195 V to 320 V and it completes a charging range up to 100 %.

B. Energy losses calculation

The total energy losses produced by the power converter through the charging process from Fig. 5 are computed by applying (5) and (6). The energy loss at the i^{th} time is given by E_{loss_i} and it is obtained by using (5). Here, P_{loss_i} is the power loss at the i^{th} time instant and $P_{loss_{i-1}}$ is the power loss at the $i-1^{\text{th}}$ time instant. The total energy loss over the complete cycle is obtained by summing the energy loss at each time instant and it is given by (6).

$$E_{loss} = \frac{P_{loss_i} + P_{loss_{i-1}}}{2} \cdot (t_i - t_{i-1}) \quad (5)$$

$$E_{loss_{total}} = \sum_{i=1}^{k} E_{loss_i} \quad (6)$$

Where k is the total number of time instants.

The total P_{loss} is given by (7) and is the sum of the switching and conduction losses. The conduction loss, P_{cond}

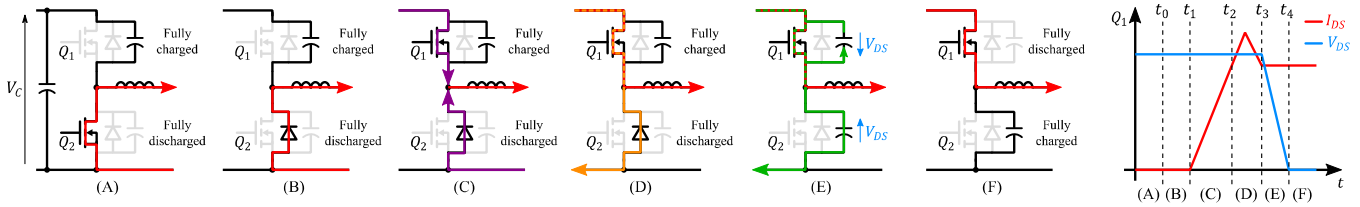

Fig. 6. Switching states during the turn on of a hard switched semiconductor.

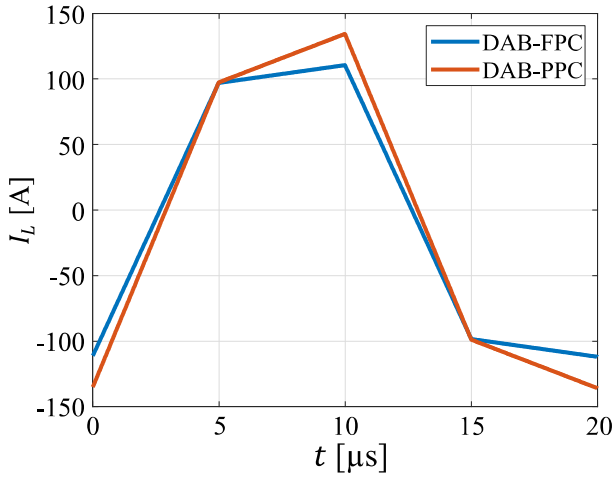

Fig. 7. Steady-state inductor current waveform.

is given by (8). It is obtained using the RMS of the current and the on-state resistance of the devices.

$$P_{loss} = P_{cond} + P_{sw} \quad (7)$$

$$P_{cond} = R_{DS} \cdot I_{Q_{RMS}}^2 \quad (8)$$

Where, R_{DS} is the on resistance of the semiconductor and $I_{Q_{RMS}}$ its RMS current.

Estimation of switching loss requires inclusion of the ZVS boundary for both of the architectures. For this analysis, turn-off losses are neglected [21], [22] and only turn on switching losses that occur out of the ZVS region will be taken into account. Therefore, as a first step, the boundaries of the ZVS regions of each solution are calculated following the steps described in [23]. Fig. 6 shows the characteristic switching states and waveforms during the turn on of a hard switched semiconductor. At the beginning of the transition (interval A), the inductor current is free-wheeling through Q_2 and the output capacitor of Q_1 is fully charged to the capacitor voltage (V_C). At t_0, the gate signal of Q_2 is turned off and, consequently, the inductor current flows through its body diode until t_1 (interval B). At this point, the gate signal of Q_1 reaches the threshold voltage and its drain current rises to I_L (interval C). However, the drain current of Q_1 continues increasing due to the reverse recovery effect of the body diode of Q_2 (interval D). Once the body diode of Q_2 starts blocking the voltage, its output capacitor charges to V_C (interval E). Here it ends the switching process. To sum up, the power losses that will be considered when hard switching occurs are calculated using (9). There, the next losses are considered: the conduction losses of the body diode (10), the losses related to the coexistence of the drain-source voltage and current (11), the reverse recovery losses (12) and the resonant transition (13).

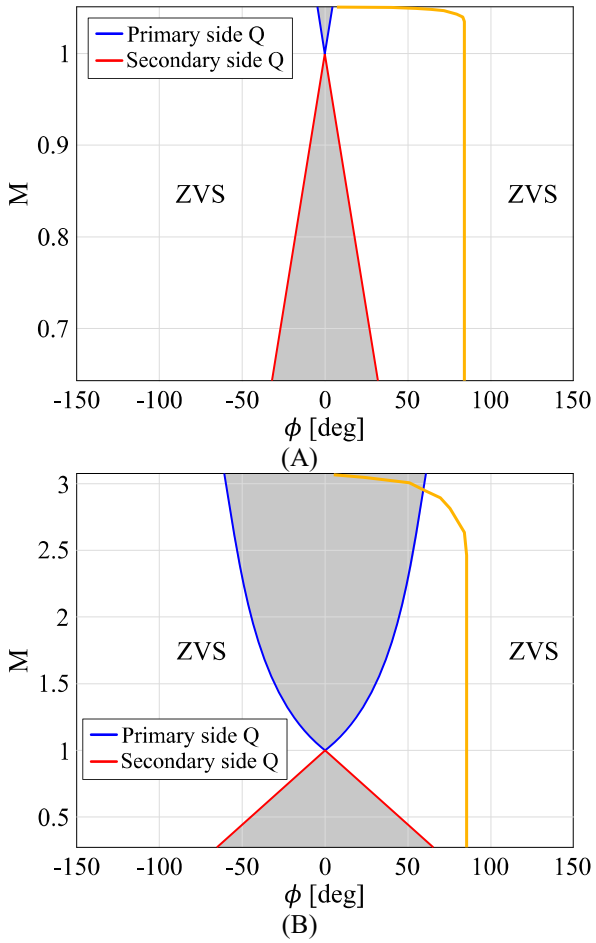

Fig. 8. ZVS regions and boundaries for primary and secondary side semiconductors using PSM. (A) DAB-FPC. (B) DAB-PPC.

$$P_{sw} = P_{diode} + P_{VI} + P_{rr} + P_{oss} \quad (9)$$

$$P_{diode} = (V_{SD} \cdot I_{SD} + R_{SD} \cdot I_{SD}^2) \cdot \frac{t_{db}}{T_S} \quad (10)$$

$$P_{VI} = \frac{1}{2} \cdot I_L \cdot V_{DC} \cdot \frac{t_{ri} + t_{fv}}{T_S} \quad (11)$$

$$P_{rr} = Q_{rr} \cdot V_{DC} \cdot f_{sw} \quad (12)$$

$$P_{oss} = \left(E_{oss_{Q1}} + E_{oss_{Q2}}\right) \cdot f_{sw} \quad (13)$$

Where, t_{db} is the dead band time (3% of the period), t_{ri} is the rise time of the current (14) and t_{fv} is the fall time of the voltage (15).

$$t_{ri} = \frac{Q_i}{I_{gate}} = \frac{Q_i \cdot R_{gate}}{V_{driver} - \frac{(V_{th} + V_{pl})}{2}} \quad (14)$$

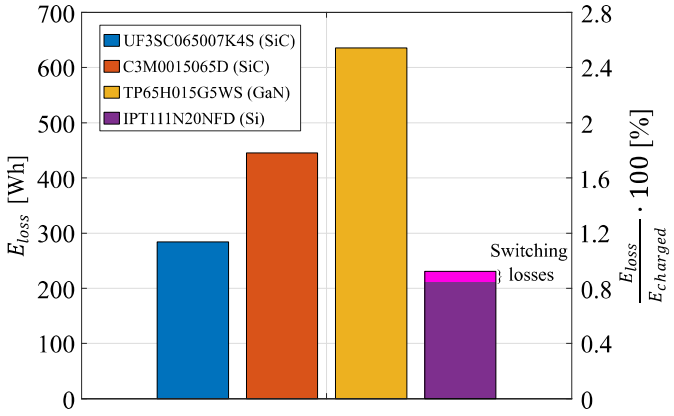

Fig. 9. Total energy losses due to semiconductors.

$$t_{fv} = \frac{Q_v}{I_{gate}} = \frac{Q_v \cdot R_{gate}}{V_{driver} - V_{pl}} \qquad (15)$$

Q_i from (14) is the amount of charge that must be supplied while the gate voltage increases from the threshold voltage to the plateau voltage. Q_v from (15) is the amount of charge that must be supplied through the plateau. Both values can be extracted from the datasheet of the semiconductor [24]–[28].

IV. Simulation Results

An analytical model of the DAB is developed to obtain the current waveforms of the power devices. As example, Fig. 7 shows the steady-state waveforms of the inductor's current at initial charging conditions.

In the first place, Fig. 8 presents the ZVS regions of each solution in function of M and the phase-shift (ϕ). The yellow line represents the working points of the converter through a complete charging process. As it can be observed, at both solutions, this line maintains a constant ϕ value at 90º through great part of the charging process. This corresponds to the constant current region from Fig. 5. Then, the value of ϕ starts decreasing as the power consumed by the EV decreases (constant voltage region). In the case of the DAB-FPC (Fig. 8a), the yellow line never enters in to the grey area, which means that the semiconductors will always work inside the ZVS region. However, the DAB-PPC (Fig. 8b) does enter at the end of the charging process. At this moment, the semiconductors from the primary side do not commute in ZVS and their switching losses must be quantified. Nevertheless, these switching losses are expected to be very low due to the reduced switched voltage and current. Indeed, since the battery is at the constant voltage region, its voltage value (V_{EV}) is at its maximum, 320 V. Consequently, the voltage commuted by the primary side semiconductors will only be 20 V.

Finally, Fig. 9 presents the total energy losses generated over one charge with each semiconductor and the energy loss in percentage. In the case of the Si-based DAB-PPC, the energy losses due to the hard switching that occurs at the end of the charging process are differentiated with a lighter color. As it can be observed, they only represent an 8.2% of the total result. This is because they occur when the K_{pr} and V_{in} (voltage switched by the primary semiconductors) are at their lowest values. Then, it can be concluded that the Si-based DAB-PPC is the most efficient solution. Compared to the most efficient SiC device (UF3SC065007K4S), the Si-based DAB-PPC solution achieves an energy loss reduction of 18.37 %. When it comes to the WBG devices, it is observed that SiC semiconductors offer better performance than GaN for the considered application.

V. Conclusion

This paper presents an efficiency comparison between a WBG-based DAB-FPC and a Si-based DAB-PPC for an OBC application. Using simulations, it has been validated that the lower power rated DAB-PPC topology significantly reduces the converter losses by a 18.37 %. This is mainly due to the low conduction losses achieved by the DAB-PPC due to the reduced on-state resistance of the primary side Si semiconductors. Also, the hard switching losses that are computed for the DAB-PPC (Fig. 8b), are not significant, due to the low power level conditions and reduced switched voltage. Additionally, Si-based devices are considerably cheaper than SiC semiconductors, which reduces the final cost of the converter. So, it can be concluded that by combining PPP strategies and Si technology, highly efficient and reduced cost converters can be achieved. Hence, PPP strategies are attractive solutions to life extension of Si power devices.

References

[1] K. Shenai, "Future prospects of widebandgap (WBG) semiconductor power switching devices," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 248–257, 2015.

[2] A. Jafari *et al.*, "Comparison of Wide-Band-Gap Technologies for Soft-Switching Losses at High Frequencies," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12595–12600, 2020.

[3] "Shyh-Chiang Shen, Ph.D. // Research – Shyh-Chiang Shen." [Online]. Available: https://shensc.ece.gatech.edu/research/. [Accessed: 16-Nov-2021].

[4] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, 2017.

[5] L. Zhang, Z. Zheng, and X. Lou, "A review of WBG and Si devices hybrid applications," *Chinese J. Electr. Eng.*, vol. 7, no. 2, pp. 1–20, 2021.

[6] J. Anzola, I. Aizpuru, and A. Arruti, "Partial power processing based converter for electric vehicle fast charging stations," *Electron.*, vol. 10, no. 3, pp. 1–17, 2021.

[7] J. Anzola *et al.*, "Review of Architectures Based on Partial Power Processing for DC-DC Applications," *IEEE Access*, vol. 8, pp. 103405–103418, 2020.

[8] P. S. Shenoy, K. A. Kim, and P. T. Krein, "Comparative analysis of differential power conversion architectures and controls for solar photovoltaics," *IEEE 13th Work. Control Model. Power Electron. COMPEL*, 2012.

[9] M. Kasper, D. Bortis, and J. W. Kolar, "Classification and comparative evaluation of PV panel-integrated DC-DC converter concepts," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2511–2526, 2012.

[10] J. R. R. Zientarski, J. R. Pinheiro, M. L. D. S. Martins, and H. L. Hey, "Understanding the partial power processing concept: A case-study of buck-boost dc/dc series regulator," *2015 IEEE 13th Brazilian Power Electron. Conf. 1st South. Power Electron. Conf. COBEP/SPEC 2016*, no. 1, 2015.

[11] J. R. R. Zientarski, M. L. Da Silva Martins, J. R. Pinheiro, and H. L. Hey, "Series-Connected Partial-Power Converters Applied to PV Systems: A Design Approach Based on Step-Up/Down Voltage Regulation Range," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7622–7633, 2018.

[12] J. R. R. Zientarski, M. L. da S. Martins, J. R. Pinherio, and H. L. Hey, "Evaluation of Power Processing in Series-connected Partial-power Converters," *J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 1, pp. 343–352, 2019.

[13] V. M. Iyer, S. Gulur, S. Bhattacharya, and R. Ramabhadran, "A Partial Power Converter Interface for Battery Energy Storage Integration with a DC Microgrid," *IEEE Energy Convers. Congr.*

Expo. ECCE, pp. 5783–5790, 2019.

[14] A. Diab-Marzouk, “Lightweight DC-DC Converter with Partial Power Processing and MPPT for a Solar Powered Aircraft,” 2015.

[15] M. Pape and M. Kazerani, “An Offshore Wind Farm with DC Collection System Featuring Differential Power Processing,” *IEEE Trans. Energy Convers.*, vol. PP, no. c, pp. 1–1, 2019.

[16] S. Rivera, S. Kouro, S. Vazquez, S. M. Goetz, R. Lizana, and E. Romero Cadaval, “Electric Vehicle Charging Infrastructure,” *IEEE Ind. Electron. Mag.*, pp. 517–543, 2021.

[17] J. Buck, “International electrotechnical commission,” *Handb. Transnatl. Econ. Gov. Regimes*, pp. 573–584, 2016.

[18] D. Christen, “Analysis and Performance Evaluation of Converter Systems for EV-Ultra-Fast Charging Stations with Integrated Grid Storage,” no. 24577, p. 195, 2017.

[19] A. Rodríguez, A. Vázquez, D. G. Lamar, M. M. Hernando, and J. Sebastián, “Different purpose design strategies and techniques to improve the performance of a dual active bridge with phase-shift control,” *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 790–804, 2015.

[20] “BU-409: Charging Lithium-ion - Battery University.” [Online]. Available: https://batteryuniversity.com/article/bu-409-charging-lithium-ion. [Accessed: 04-Aug-2021].

[21] D. Bortis, O. Knecht, D. Neumayr, and J. W. Kolar, “Comprehensive evaluation of GaN GIT in low- and high-frequency bridge leg applications,” *2016 IEEE 8th Int. Power Electron. Motion Control Conf. IPEMC-ECCE Asia 2016*, pp. 21–30, 2016.

[22] D. Christen and J. Biela, “Analytical Switching Loss Modeling Based on Datasheet Parameters for mosfets in a Half-Bridge,” *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3700–3710, 2019.

[23] S. S. Shah, V. M. Iyer, and S. Bhattacharya, “Exact Solution of ZVS Boundaries and AC-Port Currents in Dual Active Bridge Type DC-DC Converters,” *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5043–5047, 2019.

[24] “C3M0015065D Wolfspeed | Mouser España.” [Online]. Available: https://www.mouser.es/ProductDetail/Wolfspeed/C3M0015065D?qs=sGAEpiMZZMv0NwlthflBi5kUgygwZBxUZdhKhXathFE%3D. [Accessed: 19-Nov-2021].

[25] “IPT65R033G7 - Infineon Technologies.” [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/n-channel/500v-950v/ipt65r033g7/?redirId=144495. [Accessed: 19-Nov-2021].

[26] “IPT111N20NFD - Infineon Technologies.” [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/n-channel/ipt111n20nfd/. [Accessed: 19-Nov-2021].

[27] “TP65H015G5WS 650V Cascode GaN FET - Transphorm.” [Online].Available:https://www.transphormusa.com/en/product/tp65h015g5ws/. [Accessed: 19-Nov-2021].

[28] “UnitedSiC UF3SC065007K4S - UnitedSiC.” [Online]. Available:https://unitedsic.com/products/sicfets/uf3sc065007k4s/. [Accessed: 19-Nov-2021].