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Static Current Unbalance of Paralleled SiC MOSFET Modules in the Final Layout

Ander Jauregi*, David Garrido†, Igor Baraia-Etxaburu†, Asier Garcia-Bediaga* and Alejandro Rujas*
*Ikerlan Technology Research Centre
Basque Research and Technology Alliance (BRTA)
Arrasate-Mondragon, Basque Country, Spain
Email: arujas@ikerlan.es
†Electronics and Computer Science department
Mondragon Unibertsitatea - Faculty of Engineering
Arrasate-Mondragon, Basque Country, Spain
Email: ibaraia@mondragon.edu

***Abstract*— Silicon Carbide (SiC) MOSFETs enable enhanced performance of power converters in several applications. Parallel connection of SiC MOSFETs become mandatory for medium power applications due to the current rate of existing modules. A balanced current sharing between paralleled MOSFETs is desired to maximize the power capability of each device, maximizing the power capability of the whole system. This work studies the static current unbalance of two paralleled 1200V-400A SiC MOSFET modules with individual gate driver. Experimental measurements are done focused on parasitic inductance caused by electromechanical layout.**

***Index Terms*—Sicilon Carbide, Parallel connection, Current sharing.**

I. Introduction

The Silicon Carbide (SiC) MOSFET has superior characteristics compared to traditional Silicon (Si) MOSFETs and IGBTs [1]. It can switch voltages in excess of 1kV and operate at hundreds of kHz due to the lack of tail current and its small gate charge. Thus, the SiC-MOSFET offers notorious benefits in terms of high voltage and high switching frequency capabilities. In consequence, it has become in a real alternative to the Si-IGBT for Medium Voltage and Medium Power applications.

1.2kV and 1.7kV SiC-MOSFET modules are commercially available (and up to 3.3kV and 6.5kV devices are expected in the near future [2]) with current rating of 800A and 225A [3], [4] that are suitable for Medium Voltage and Medium Power Applications. For higher power applications, the parallel connection of multiple SiC-MOSFET devices is often necessary to increase the current capability of a single switch and to improve the efficiency of the converter.

However, the balanced current sharing during the conduction time (static behavior) interval and the switching transients (dynamic behavior) is not trivial [5]. Static current unbalances lead to power loss and operation temperature differences between the parallel connected devices. Consequently, a current derating must be considered to guarantee that all devices operate under their maximum rated current and temperature. Although the temperature coefficient of the on-resistance of SiC-MOSFETs (R_{dson}) is positive, it is less sensitive to temperature than their Si counterparts [5] so this feedback mechanism is not a current balance guarantee.

Current unbalances during the switching transients lead to different switching losses or to exceed the maximum current switching capability of a parallel-connected device. Thus, again, a current derating results mandatory.

It is known [6] that the static current distribution is dependent on differences between the R_{dson} of the parallel connected devices, the operation temperature, the gate driver voltage and layout asymmetries in the power loop.

Similarly, the current unbalance during the switching transient is related to asymmetries between gate drivers, SiC-MOSFET [6] and free-wheeling diodes [7] parameters. In addition, differences in stray inductances on the switching loops have also negative influence on the transient behavior of parallel-connected devices.

In [8], the author proposes the use of matched devices and the proper current distribution is achieved by means of adjusting the source kelvin connection length. In [5] and [9], passive balancing techniques are used to balance the current during the switching transients, while in [10] active gate driver solutions are proposed. Thus, it is not clear how the unbalance problem of parallel-connected devices must be approached. Different balance techniques can be found where additional passive components are introduced, leading to bulky and less efficient solutions (adding stray inductance) or active gate driver techniques which become complex when paralleling more than two devices. In addition, the effectiveness of these active balance control methods are limited by the stray inductance differences between the parallel connected devices [11]. So further research must be done, in order to fully understand which are the major causes that influence on the unbalance problem.

Generally speaking, the use of a compact and cost-effective single driver to operate all the parallel connected devices is preferred because it eliminates problems related to signals

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propagation delays and applied different driver voltages [12]. However, this solution requires the use of emitter resistors to damp the coupling effects between the common emitter inductances of the parallel-connected devices. When the parallel-connected modules are large and the distances between the emitters is large, individual gate drivers for the parallel-connected modules become mandatory [12].

As a first step, this short paper evaluates the influence of parasitic inductance mismatch on the static current unbalance between two parallel-connected 1200V/400A SiC-MOSFET modules with individual gate driver. Section II studies the real impact of possible static unbalance sources on the studied scenario. Section III shows a study of the influence of electromechanical layout on static current balance. Finally, the conclusions of the work are presented. The factors that influence dynamic current balance will be analyzed in future works.

II. Evaluation of current unbalance sources

One of the main unbalance sources when paralleling semiconductors is the gate circuit [12]. The studied power stack depicted in Fig. 1 shows that each SiC module has an individual gate driver based on a 2SC0435T2H0-17 driver core from Power Integrations [13]. Considering individual gate drivers, special attention is required in order to design a circuit that provides equal propagation time, equal gate-emitter voltage and minimum jitter for the paralleled devices. In the case under study, a common PWM signal goes from the control unit to both SiC module gate driver cores (of the same phase leg). Each gate driver core drives its own SiC module, with two independent driver output signals and gate resistances.

Experimental results of the gate circuit signals, depicted in Fig. 2, demonstrate that the analyzed gate circuit is not a considerable unbalance source. In that figure, the PWM control signal is plotted in blue. This signal is a common input for both driver cores. The outputs of these driver cores are plotted in yellow and red. Each device has its own gate circuitry after

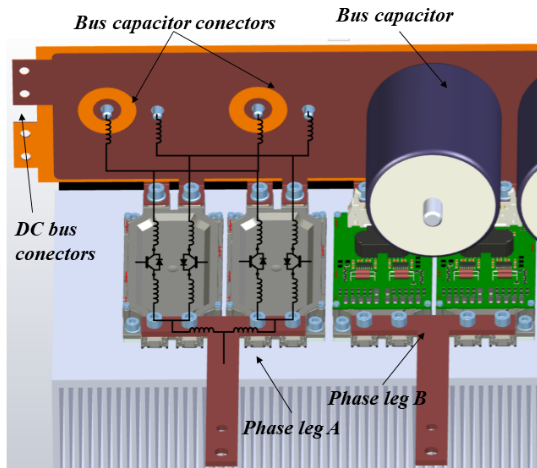

Fig. 1: Power stack with BSM400D12P3G002 SiC-MOSFET modules used on this work.

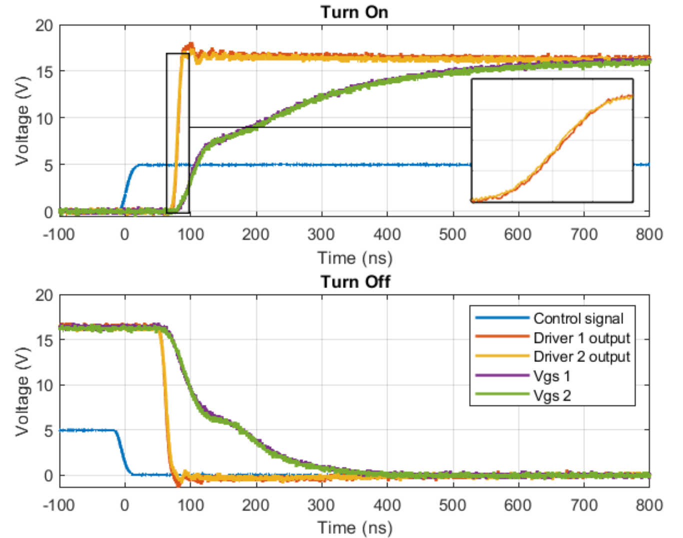

Fig. 2: Gate circuit signals for turn-on and turn-off transients. The zoom area shown on the turn on event has 10ns/div.

these two signals, what results in two independent gate-source voltages plotted on green and purple. It can be seen that no critical delays are obtained, so gate circuit is discarded as a current unbalance source in the experimental tests developed in Section III.

Another unbalance source is the semiconductor parameter dispersion. The on-state resistance difference of the modules leads to a static current sharing mismatch. This difference can be reduced by using modules of the same production lot or preselecting them based on R_{dson}. It is known [14] that this R_{dson} difference can cause a current unbalance up to 5% for random picked unselected modules. This figure can be decreased to 2% when the parallel connected modules are selected to have conduction voltages with differences up to 100mV [15]. This work studies the current unbalance with two BSM400D12P3G002 modules from Rohm [16], paralleled in a double-pulse scenario. The modules are of the same production lot so differences on R_{dson} are minimized.

The main unbalance source studied in this work is the parasitic inductance of the current loop due to electromechanical layout. To understand this effect, the electrical diagram of the double-pulse test in introduced in Fig. 3.

L_{s1} and L_{s2} represent the stray inductances of the DC side electromechanical connection, while L_{d1} and L_{d2} represent the stray inductances of the AC side. V_{ds1} and V_{ds1} represent the voltage drop caused by currents i_1 and i_2 in each SiC-MOSFET. Both paralleled modules share a common $V_{D'S'}$ voltage in the electromechanical connection point, which leads to:

$$V_{ds1} + \frac{di_1}{dt} L_{\sigma 1} = V_{ds2} + \frac{di_2}{dt} L_{\sigma 2}, \tag{1}$$

$$L_{\sigma 1} = L_{s1} + L_{d1}, \tag{2}$$

$$L_{\sigma 2} = L_{s2} + L_{d2}, \tag{3}$$

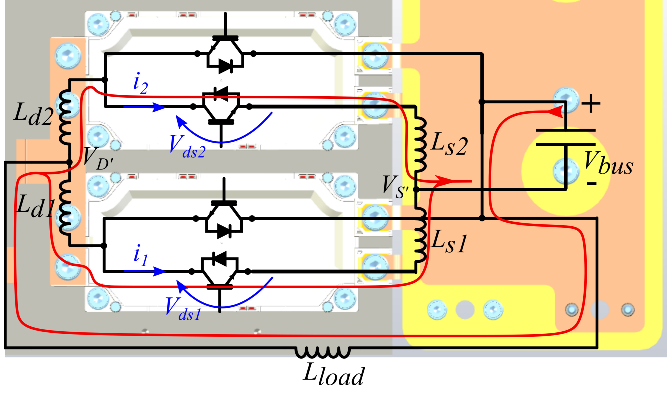

Fig. 3: Electrical diagram and static current loop for two paralleled SiC-MOSFET modules in a double pulse scenario.

Considering the output characteristic of SiC-MOSFETs, $V_{ds1} = V_{ds2}$ is desired in order to obtain a perfect current balance if device parameter dispersion is neglected. For that reason, any mismatch on the total parasitic inductance of the paralleled devices $L_{\sigma 1} \neq L_{\sigma 2}$ will lead to $V_{ds1} \neq V_{ds2}$ and generate a current unbalance.

The V_{ds} difference is accentuated for a certain parasitic inductance mismatch if the di/dt increases. The inductance value of the test (L_{load}) together with parasitic inductances and DC bus voltage (V_{bus}) define the di/dt of the load current when R_{dson} is neglected:

$$\frac{di}{dt} = \frac{V_{bus}}{(L_{load} + L_{\sigma 1}//L_{\sigma 2})}, \tag{4}$$

Low load inductance values lead to high di/dt and current unbalance is increased. It is concluded that load inductance determines the current unbalance as well.

Considering that gate circuit, device parameter mismatch and thermal effects have minor influence on the studied scenario compared to the 30% unbalance presented in Section III, the experimental tests focus on the electromechanical symmetry study.

III. Electromechanical Layout Study

Parasitic inductance is identified as the main current unbalance source in Section II. The influence of electromechanical layout on stray inductance is cuantified in this section for two paralleled SiC-MOSFET modules.

Parasitic inductance is a consequence of the energy stored in the magnetic field generated by any current flowing through a current loop. In the case of the static current loop in a double pulse scenario, there are some fixed stray inductances defined by the design such as the DC bus capacitors and busbar parasitic inductance or SiC-MOSFET modules internal stray inductances. However, parasitic inductance generated by the power loop enclosed between L_{load}, its conection points and the return cable can be modified to evaluate its impact. The importance of symmetric and compact L_{load} electromechanical connection is studied for paralleled SiC-MOSFET modules.

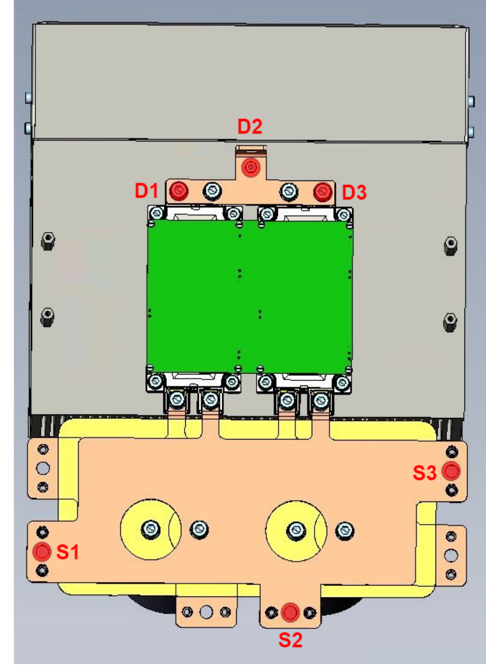

Fig. 4: Power stack with load connection points to force electromechanic asymmetries on drain and source parasitic inductance.

Electromechanical layout asymmetries can be found both on the DC and AC side of the SiC-MOSFET modules. The different AC and DC connection points presented in Fig. 4 are combined with L_{load} inductance position and return cable routing to study the influence of electromechanical layout on current balance. Connection asymmetries are forced to generate drain inductance (L_{d1} and L_{d2}) and source inductance (L_{s1} and L_{s2}) mismatch. Three different connection points are tested for both drain and source connection. For the DC connection, the left side point (S_1) forces $L_{s1} < L_{s2}$, the center point connection (S_2) equals $L_{s1} = L_{s2}$ and the right point (S_3) forces $L_{s1} > L_{s2}$. In the same way, D_1, D_2 and D_3 are the connection points for the AC side.

Some examples of the studied electromechanical layout combinations are depicted in Fig. 5. The connection with the highest balance possible on the analyzed power stack is shown in Fig. 5(a). The symmetric DC and AC points (S_2 and D_2) are connected to L_{load} with a return cable that goes below the SiC-MOSFET modules, just between both modules, with the aim of matching as much as possible the enclosed area of each SiC-MOSFET module (DUT_1 and DUT_2). The resulting current unbalance of this electromechanical layout is 1.73% as presented in Table I, where the current unbalance is calculated as:

$$\Delta I[\%] = \frac{i_1 - i_2}{i_1} \times 100 \tag{5}$$

In Fig. 5(b) symmetric AC connection point D_2 is connected with the asymmetric S_3 DC point. This connection in

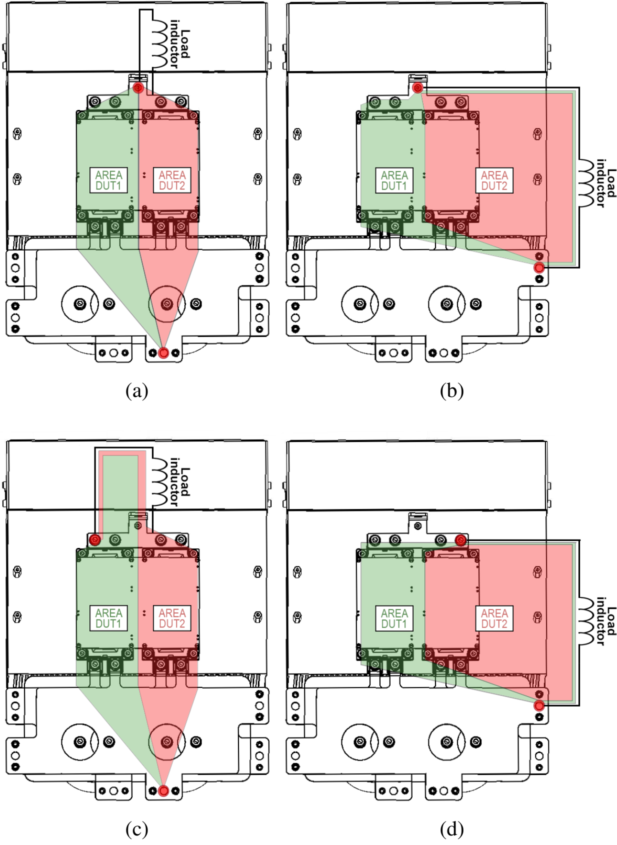

Fig. 5: Example of electromechanical layouts. (a) S_2 and D_2 connection points with symmetric L_{load} position. (b) S_3 and D_2 connection points with asymmetric L_{load} position. (c) S_2 and D_1 connection points with symmetric L_{load} position. (d) S_3 and D_3 connection points with asymmetric L_{load} position.

combination with an asymmetric L_{load} position forces different parasitic inductances. The module with smaller enclosed area to L_{load} (DUT_2) has smaller parasitic inductance and therefore conducts more static current. This results in a static current unbalance of $-21,78\%$ as shown in Table I.

Fig. 5(c) represents a symmetric L_{load} position with asymmetric AC connection point to D_1. The added current loop area of DUT_2 due to de AC connection point increases the current unbalance to $12,27\%$ compared to Fig. 5(a).

Finally, Fig. 5(d) represents the electromechanical layout in which the biggest current unbalance is measured. Asymmetric DC and DC connections to S_3 and D_3 combined with an asymmetric L_{load} position generates a $-30,48\%$ current unbalance.

All the current unbalance results for the tested DC and AC connections points combined with L_{load} position are presented in Table I. Some examples of the measured i_1 and i_2 currents are depicted in Fig. 6. The tests have been obtained with $L_{load} = 150\mu H$, with an on-time pulse test of 60µs. Results show that layout is the main unbalance source in the studied scenario. For the maximum symmetry case with S_2 and D_2 connection points and symmetric L_{load} position ($L_{s1} = L_{s2}$ and $L_{d1} = L_{d2}$) the current unbalance is just 1.73%. That mismatch can be attributed to the combined effect of the previously analyzed minor unbalance sources: gate circuit, semiconductor parameter mismatch and temperature effects.

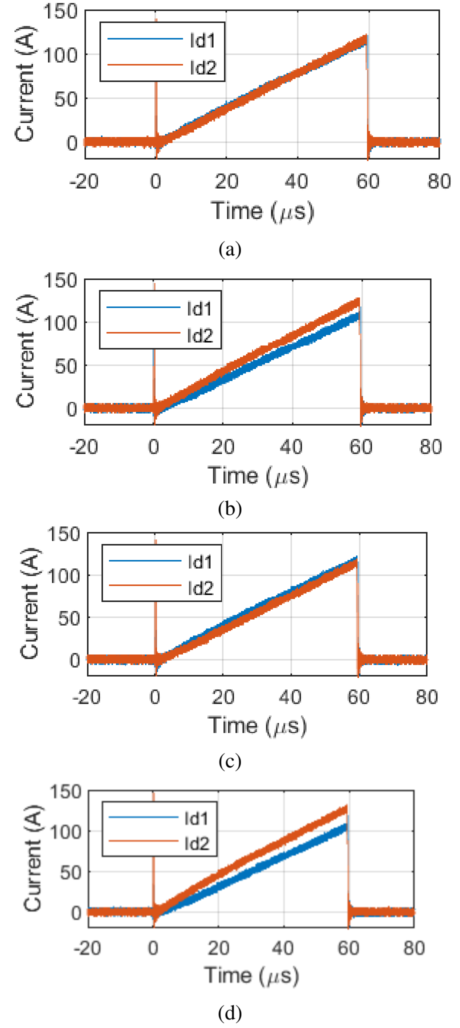

Fig. 6: Static current unbalance at $V_{bus} = 600V$ with $150\mu H$ load inductance for the corresponding electromechanical layout examples depicted in Fig. 5.

TABLE I:
UNBALANCE RESULTS WITH $L_{load} = 150\mu H$

Source	Load position	Drain	$\Delta I[\%]$
S_1	Asymmetric left	D_1	24.47%
S_1	Asymmetric left	D_2	10.14%
S_1	Asymmetric left	D_3	-3.72%
S_2	Symmetric	D_1	12.27%
S_2	Symmetric	D_2	1.73%
S_2	Symmetric	D_3	-12.41%
S_3	Asymmetric right	D_1	-11.62%
S_3	Asymmetric right	D_2	-21.78%
S_3	Asymmetric right	D_3	-30.48%

TABLE II:
UNBALANCE WITH $L_{load} = 150\mu H$ AND $L_{load} = 625\mu H$

Source	Load position	Drain	$\Delta I[\%]$	L_{load}
S_3	Asymmetric rigth	D_3	-20.42%	$625\mu H$
S_3	Asymmetric right	D_3	-30.48%	$150\mu H$

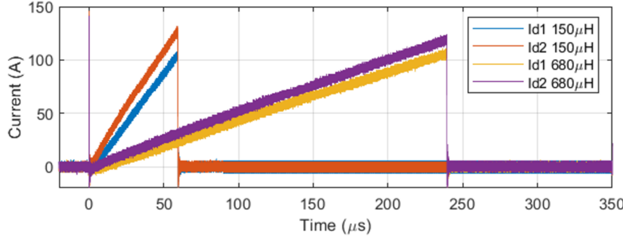

Fig. 7: Influence of load inductance at $V_{bus} = 600V$ with different load inductance values: $150\mu H$ and $625\mu H$. Asymmetric parasitic inductances $L_{\sigma 1} > L_{\sigma 2}$

As it has been commented previously, the load inductance of the converter also affects the current sharing. Higher di/dt caused by low load inductance value accentuates the current unbalance. This effect is depicted in Fig. 7 where two different load inductance values ($L_{load} = 150\mu H$ and $L_{load} = 625\mu H$) are tested with the forced electromechanical asymmetry of Fig. 5(d). Load inductance is connected to points D_3 and S_3 with asymmetric load position to force $L_{\sigma 1} > L_{\sigma 2}$.

On the one hand, the high inductance value ($625\mu H$) generates around $0.96A/s$ dynamic per module and results in a -20.42% current unbalance. On the other hand, the low inductance value ($150\mu H$) increases the dynamic to $2A/s$ and current unbalance therefore increases to -30.48%. The on-time has been selected with the aim of reaching the same current level.

It is concluded that load inductance value is a key factor that determines the magnitude of the current unbalance problem with paralleled SiC-MOSFETs. $V_{ds1} \neq V_{ds2}$ mismatch is accentuated due to the increased di/dt generated by low L_{load}.

IV. CONCLUSIONS

The static current sharing between paralleled 1200V-400A SiC-MOSFET modules has been evaluated in the final converter layout. It has been proved that typical semiconductor parameter variation reported in literature has minor influence on the static current sharing compared to the unbalance forced by layout asymmetries. Regarding gate circuit, it is demonstrated the viability of good parallelization with individual gate drivers. The combined effect of gate circuit and parameter mismatch generates a static current unbalance around 1.73% in the evaluated scenario. Electromechanical layout is identified as the major influence on static current sharing between paralleled modules. Asymmetries on both DC and AC side of the module generate severe static current unbalance (up to 30%).

Finally, the influence of load inductance value is studied. It is proved that high di/dt generated by low load inductance increases the current unbalance problem. This fact gets great importance with SiC semiconductors. It is common to take advantage of the high switching frequency capabilities of SiC technology to reduce inductor volume (inductance value) in certain applications. Designs with paralleled semiconductors and low load inductances need to take special care of electromechanical layout in order to achieve a good current sharing.

The parameters affecting dynamic current balance for paralleled 1200V-400A SiC-MOSFET modules will be analyzed in future work.

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