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Current References Limitation Method Considering Voltage and Current Maximums for STATCOMs Providing Simultaneously Reactive Power and Current Harmonics

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***Abstract*— The present paper focuses the analysis on a Static Synchronous Compensator (STATCOM) that operates simultaneously providing reactive power and several current harmonics of different frequencies (active power filter or active impedance functionalities). Being more specific, this paper proposes a general limitation method that reduces the current references of the STATCOM, whenever the current or voltage limit of the converter is exceeded. In a realistic operation scenario, the STATCOM's operator may ask for certain reactive power and harmonic current reference signals and depending on the actual grid voltage conditions (unbalances and harmonics), the required converter voltage and current may exceed their limit. Consequently, the proposed limitation method protects the STATCOM system from malfunctioning when the voltage limit is exceeded and from damages when the current limit is exceeded. Hence, the paper first proposes a limitation method oriented to a STATCOM that operates solely exchanging reactive power. Secondly, the limitation method is generalized for a STATCOM that controls reactive power as well as several current harmonics. Then, simulation and experimental results are provided to validate the proposed limitation method, under a rich variety of working conditions. Finally, a conceptual analysis of the method is carried out confronting it against several possible limitation alternatives.**

***Index Terms*—STATCOM, active filter, current harmonic control, limitation method, voltage and current maximums, current loops.**

I. Introduction

THE Static Synchronous Compensator (STATCOM) is becoming an essential device in power grid applications. It is used to facilitate the integration of large power consuming loads [1] or renewable energy-sources (RES) [2], by meeting the requirements imposed by grid operators. STATCOMs are typically used in the improvement of the power system stability, power factor correction, regulation of line voltages, active power filtering, mitigation of voltage flicker, unbalanced load compensation, and low-voltage ride-through (LVRT) applications [3].

In recent years STATCOM devices are starting to be required to operate with several functionalities simultaneously such as harmonic and reactive power compensation, or grid unbalance compensation, sharing the same converter hardware limits [4]-[8]. The simultaneous operation under unbalanced voltages and currents together with several harmonic voltages and currents can involve problems, due to the complexity of having to predict if the converter's voltage and current is going to exceed its maximum allowed value. Hence, the use of reference limiting algorithms has become necessary in order not to disconnect the converter due to exceeding any of these boundaries.

For STATCOMs, or in general for converters connected to the grid, there already exist several proposals in the literature to limit the references, so that they do not exceed the maximum permitted value in any of the three phases of the current [9]-[11].

In addition, perhaps oriented to more specific applications, there are several limiters already proposed for grid connected converters in the context of faults [12]-[15]. In general, they develop limitation algorithms not to exceed the maximum allowable current limit. These algorithms are based on space vector theory, combined with the sequence decomposition methods to cope with the unbalances of the grid. Often, for instance in [12]-[13], the limitation control rule is based on generating limited current reference signals, in function on the measured currents.

In a similar direction, there are also a family of contributions clearly more oriented to analysis around limiters for grid connected converters in distribution generation applications [16]-[22]. Thus, for instance [17]-[21] study grid-forming converter control during grid fault conditions and propose a controller which keeps the voltage-mode characteristics of the grid-forming structure while simultaneously limiting the converter currents.

There are also more innovative conceptualizations, which propose 'resiliency' to power converters via Multi-Timescale Current Limiting techniques such as in [23].

Nevertheless, the above-mentioned limitation methods are focused only on converters which operate at fundamental component of voltage and current. In specialized literature, it is not easy to find many limitation methods that also contemplate a grid-connected converter that operates controlling current harmonics. One of the few examples that the authors have found is [24], which directly truncates the sinusoidal current references when one of the phases exceeds the current limit, therefore deteriorating the quality of the obtained current waveforms. Probably, one of the main reasons why there is an absence of literature on this matter, is the mathematical complexity in the peak calculation of a signal composed by several harmonics.

Hence, trying to contribute to a lack of limiters in specialized literature oriented to converters that operate under unbalanced

voltage conditions providing reactive power and providing controlled current harmonics, this paper proposes a general limitation method that is conceived into two steps. The paper first proposes a limitation method oriented to a STATCOM that operates solely exchanging reactive power. Secondly, the limitation method is generalized for a STATCOM that controls reactive power as well as several current harmonics. The main characteristics of the limitation method that go beyond the state of the art are:

- Limitation of demanded current reference signals of the converter, in a priority order that can be re-programmed by the user, when any of both, the converter current or voltage limit, is exceeded. Since the current references are limited, the current waveforms are not deteriorated and therefore, it provides good current qualities. The limitation method is flexible and re-adaptable to the needs of a specific STATCOM operator, since the order in which the converter current references are limited can be prioritized as required by the specific application.

- Consideration of both voltage and current constraints (both voltage and current limits of the converter). By means of a pre-defined prioritization criterion, it coordinates how to reduce the current references of the converter, when both current and voltage limits are exceeded.

- Conceptualization of the method in such a generalized way that it is applicable to a converter exchanging reactive power, under unbalanced grid scenario and/or as providing certain harmonic currents (active power filter function for instance). The method is generalized in so that it can work providing one single service (solely providing reactive power) or combining more than one simultaneously (providing reactive power and several current harmonics at the same time).

As will be later explained under detail, the proposed limitation method when applied to a scenario exchanging current harmonics is based on a simple but practical mathematical calculation based on a worst-case assumption, combined with a correction feedback-loop. In a similar manner, the limitation method also supervises that the voltage limit is not exceeded, based on a feedback loop.

In addition, it has to be highlighted that the limitation method proposed in this article is valid basically at steady-state operation conditions.

II. CURRENT REFERENCES LIMITATION METHOD IN A STATCOM EXCHANGING REACTIVE POWER

A. General control block diagram

The general control block diagram where the proposed limitation method is implemented is depicted in Fig. 1. It is a STATCOM device, which is already well studied and analyzed in the technical literature [1], [2], [25], [26]. The control presents two references, i.e., Q^* and V_{bus}. Q is the reactive power at the point of common coupling (PCC) and V_{bus} the DC bus voltage. Then, the control is prepared to operate under unbalanced grid voltage conditions, since it incorporates two pairs of *dq* current controls, one dedicated for the positive sequence while the other, to the negative sequence [27]. The connection to the grid of the power electronic converter is made through a *LC* filter (R_f-L_f and R_c-C_c). Then, the voltage levels are adapted to the PCC by means of a transformer, which is modelled in the power circuit as R_{TF}-L_{TF}. Finally, the equivalent impedance of the grid is modelled as R_g-L_g.

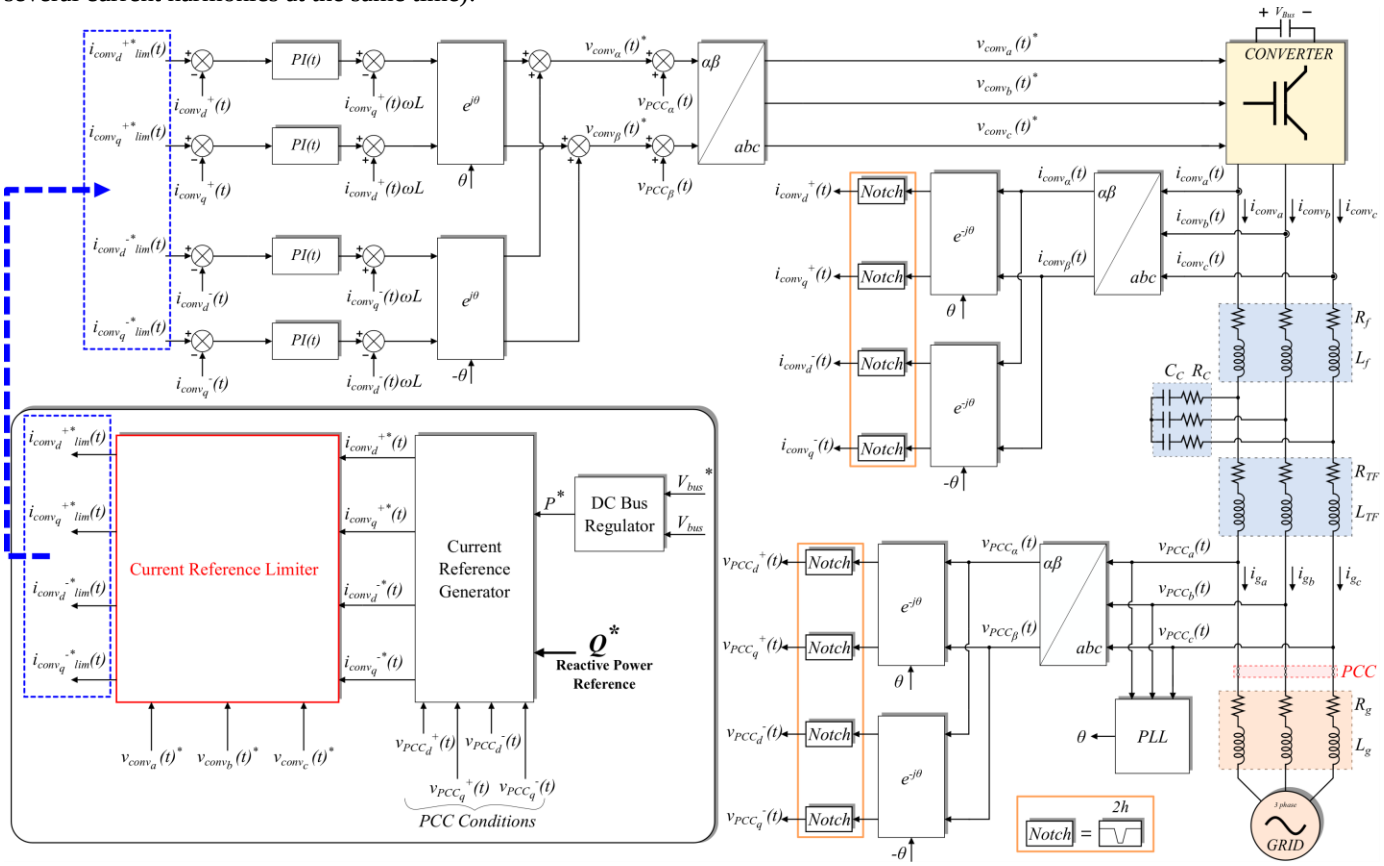

Fig. 1. Power circuit of the STATCOM and general control block diagram with the current reference limiter (L=L_{TF}+L_f).

B. Current references generation

From the DC bus voltage controller, the active power reference P^* is created. In a STATCOM device, this active power exchange is the one required to maintain constant the average DC bus voltage, compensating the effect of the power losses. Then, as depicted in Fig. 1, one block called 'Current Reference Generator' is incorporated. This block is divided into two subblocks, as illustrated in Fig. 2. As can be noticed, at a first stage, the positive and negative grid side current references are calculated. Then, as the current loops are controlling the converter currents, a second stage of calculation is needed to generate the positive and negative converter side current references, from the calculated grid side current references (at the PCC). Note that there is an alternative possibility, which is to directly control the grid side currents. However, in this article, the converter current control has been chosen. Nevertheless, this choice does not affect the conceptual usefulness of the proposed current references limitation method.

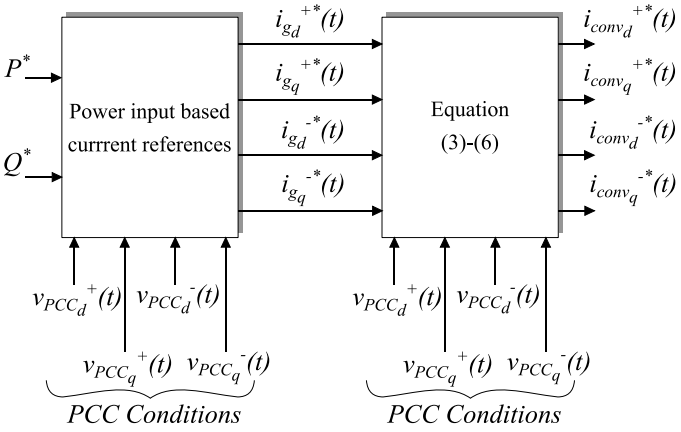

Fig. 2. Converter current references generation.

Hence, as depicted in Fig. 2, the positive and negative grid side current references are calculated according to well known equations which seek to reduce the active power oscillations at the DC bus voltage. The actual mathematical expression can be found for instance in [9].

Then, based on the steady-state phasor equations that relate the grid and converter currents, together with the PCC voltages:

$$V_{PCC}^{+} + I_g^{+}\left(R_{TF} + j\omega L_{TF}\right) - \left(\left(I_{conv}^{+} - I_g^{+}\right)\left(R_c + \frac{1}{j\omega C_c}\right)\right) = 0 \quad (1)$$

$$V_{PCC}^{-} + I_g^{-}\left(R_{TF} - j\omega L_{TF}\right) - \left(\left(I_{conv}^{-} - I_g^{-}\right)\left(R_c - \frac{1}{j\omega C_c}\right)\right) = 0 \quad (2)$$

It is possible to derive the converter side current references as follows (with ω the grid frequency in rad/s):

$$i_{conv_d}^{+*} = \left[\frac{i_{g_d}^{+*} - \omega C_C v_{PCC_q}^{+} - \omega^2 C_C L_{TF} i_{g_d}^{+*} + \omega^2 C_C^2 R_C v_{PCC_d}^{+}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} + \ldots \right.$$
$$\left. \frac{\omega C_C R_{TF} i_{g_q}^{+*} + \omega^2 C_C^2 R_C^2 i_{g_d}^{+*} - \omega^3 C_C^2 L_{TF} R_C i_{g_q}^{+*}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} + \frac{\omega^2 C_C^2 R_C R_{TF} i_{g_q}^{+*}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} \right] \quad (3)$$

$$i_{conv_q}^{+*} = \left[\frac{i_{g_d}^{+*} - \omega C_C v_{PCC_q}^{+} - \omega^2 C_C L_{TF} i_{g_d}^{+*} + \omega^2 C_C^2 R_C v_{PCC_d}^{+}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} - \ldots \right.$$
$$\left. \frac{\omega C_C R_{TF} i_{g_q}^{+*} + \omega^2 C_C^2 R_C^2 i_{g_d}^{+*} - \omega^3 C_C^2 L_{TF} R_C i_{g_q}^{+*}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} + \frac{\omega^2 C_C^2 R_C R_{TF} i_{g_q}^{+*}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} \right] \quad (4)$$

$$i_{conv_d}^{-*} = \left[\frac{i_{g_d}^{-*} + \omega C_C v_{PCC_q}^{-} - \omega^2 C_C L_{TF} i_{g_d}^{-*} + \omega^2 C_C^2 R_C v_{PCC_d}^{-}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} + \ldots \right.$$
$$\left. \frac{\omega C_C R_{TF} i_{g_q}^{-*} + \omega^2 C_C^2 R_C^2 i_{g_d}^{-*} + \omega^3 C_C^2 L_{TF} R_C i_{g_q}^{-*}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} + \frac{\omega^2 C_C^2 R_C R_{TF} i_{g_q}^{-*}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} \right] \quad (5)$$

$$i_{conv_q}^{-*} = \left[\frac{i_{g_q}^{-*} - \omega C_C v_{PCC_d}^{-} - \omega^2 C_C L_{TF} i_{g_q}^{-*} + \omega^2 C_C^2 R_C v_{PCC_q}^{-}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} - \ldots \right.$$
$$\left. \frac{\omega C_C R_{TF} i_{g_q}^{-*} + \omega^2 C_C^2 R_C^2 i_{g_q}^{-*} - \omega^3 C_C^2 L_{TF} R_C i_{g_d}^{-*}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} + \frac{\omega^2 C_C^2 R_C R_{TF} i_{g_q}^{-*}}{\left(C_C^2 R_C^2 \omega^2 + 1\right)} \right] \quad (6)$$

C. Current references limitation method

Once the converter current reference generation has been described, in this subsection the current limitation method is presented. This limiter arises on the following realistic context [5], [28]: it is supposed that the STATCOM device is connected to a grid, where it can be affected by any type or degree of unbalanced voltages. Then, it is supposed that the 'user' of the STATCOM or 'grids system operator' demands a reactive power reference Q^*, without knowing which the actual voltage unbalance of the grid is (which can change an unknown number of times during the day). This means that, although it knows the maximum current and voltage limits of the STATCOM(current and voltage constraints, I_{max} and V_{max}), it does not really know if the reference Q^* can be fully provided or not, without exceeding the limits. Consequently, under this described context, which is quite typical and very realistic, the current references limitation method is specifically designed to limit the converter's current references as shown in Fig. 1. This way, the current and/or voltage (the exceeded one in every case, or even both) of the converter is set at its maximum, taking advantage of the full capabilities of the converter. In this manner, in an indirect way, an exact amount of Q is reduced to reference Q^*, so the converter operates at its maximum current or voltage (or both) in a safe manner.

Hence, the conceptual block diagram of the current reference limiter is depicted in Fig. 3. It is comprised by two blocks that perform two main tasks. One block supervises if the current limit is not exceeded, while the other supervises that the voltage limit is not exceeded.

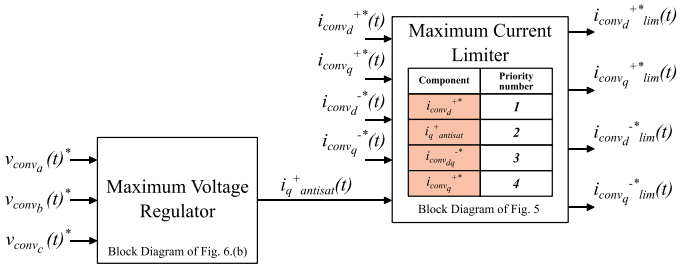

Fig. 3. Current reference limitation method.

1) Maximum phase peak calculations

The criteria used for the limitation of the current references is based on the well-known space vector theory. Thus, one

basic but important calculation that must be performed is the instantaneous peak calculation of each *abc* phase of the converter's current and voltage [9]-[29]. This fact is graphically represented at Fig. 4 only for the converter's currents (the resulting graphical representation of the voltage would be equivalent). It is seen that under the presence of unbalances, i.e., under the presence of positive and negative sequence currents, the space vector shows an ellipsoidal trajectory.

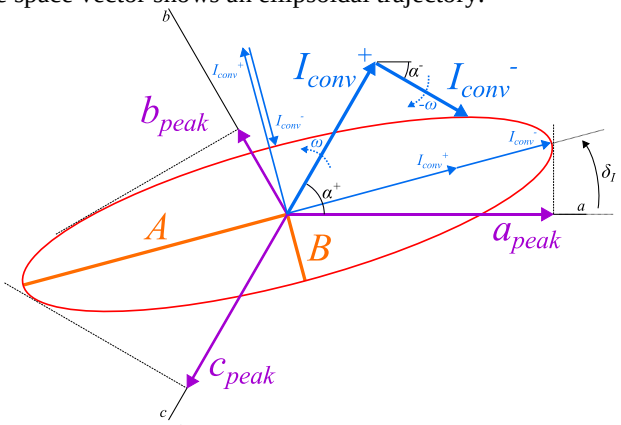

Fig. 4. Ellipse method for phase peak calculations

Thus, according to this geometrical ellipsoidal representation, the *abc* phase peaks of currents (voltages would be equivalent) can be calculated according to the following expressions [9]:

$$a_{peak} = \sqrt{A^2 cos^2(\delta_I) + B^2 sin^2(\delta_I)} \tag{7}$$

$$b_{peak} = \sqrt{A^2 cos^2(\delta_I - 120^o) + B^2 sin^2(\delta_I - 120^o)} \tag{8}$$

$$c_{peak} = \sqrt{A^2 cos^2(\delta_I + 120^o) + B^2 sin^2(\delta_I + 120^o)} \tag{9}$$

Being the magnitudes *A*, *B* and δ_I of the ellipse, in function of the positive and negative sequences as follows:

$$A = \left|I_{conv}^+\right| + \left|I_{conv}^-\right| \qquad B = \left|I_{conv}^+\right| - \left|I_{conv}^-\right| \tag{10}$$

$$\delta_I = \frac{\alpha_I^+ + \alpha_I^-}{2} \tag{11}$$

$$\alpha_I^+ = atan\left(\frac{i_{conv_q}^+}{i_{conv_d}^+}\right) \qquad \alpha_I^- = atan\left(\frac{i_{conv_q}^-}{i_{conv_d}^-}\right) \tag{12}$$

Therefore, by substituting positive and negative sequence *dq* currents in expressions (7)-(9), the peak phase values can be calculated according to:

$$I_{peak_a}^{\ 2} = \left(i_{conv_d}^+\right)^2 + \left(i_{conv_q}^+\right)^2 + \left(i_{conv_d}^-\right)^2 + \left(i_{conv_q}^-\right)^2 + \ldots$$
$$\ldots 2\left(i_{conv_d}^{\ +} i_{conv_d}^{\ -} - i_{conv_q}^{\ +} i_{conv_q}^{\ -}\right) \tag{13}$$

$$I_{peak_b}^{\ 2} = \left(i_{conv_d}^+\right)^2 + \left(i_{conv_q}^+\right)^2 + \left(i_{conv_d}^-\right)^2 + \left(i_{conv_q}^-\right)^2 + \ldots$$
$$i_{conv_q}^{\ +} i_{conv_q}^{\ -} - i_{conv_d}^{\ +} i_{conv_d}^{\ -} - \sqrt{3}\left(i_{conv_q}^{\ +} i_{conv_d}^{\ -} + i_{conv_d}^{\ +} i_{conv_q}^{\ -}\right) \tag{14}$$

$$I_{peak_c}^{\ 2} = \left(i_{conv_d}^+\right)^2 + \left(i_{conv_q}^+\right)^2 + \left(i_{conv_d}^-\right)^2 + \left(i_{conv_q}^-\right)^2 + \ldots$$
$$i_{conv_q}^{\ +} i_{conv_q}^{\ -} - i_{conv_d}^{\ +} i_{conv_d}^{\ -} + \sqrt{3}\left(i_{conv_q}^{\ +} i_{conv_d}^{\ -} + i_{conv_d}^{\ +} i_{conv_q}^{\ -}\right) \tag{15}$$

2) Prioritized limitation of current references

Once the mathematical expressions to derive the peak phase currents in function of i_{convd}^+, i_{convq}^+, i_{convd}^- and i_{convq}^- are obtained, they are applied to perform the current references limitation which is schematically represented within block from the right of Fig. 3. The general idea is that when the required current references cause the peak current of any phase to exceed its maximum constraint, the current references (i_{convd}^+, i_{convq}^+, i_{convd}^-, i_{convq}^-) are limited until the exceeded phase current operates at the maximum current I_{max}. This general idea is carried out according to the sequential procedure shown in Fig. 5. A certain priority order is assigned to each current component (i_{convd}^+, i_{convq}^+, i_{convd}^-, i_{convq}^-) and the idea is to add current components in order of prioritization until the limit current is reached (if it is reached). Thus, the adopted prioritization order in this article firstly prioritizes i_{convd}^+ to guarantee a stable value in DC bus voltage. Secondly, an inductive $i_{convq}^{+}{}_{antisat}$ sequence is prioritized to avoid exceeding the maximum AC voltage limit of the converter. Thirdly, the negative sequence current is prioritized. While, finally, the lastly prioritized current is i_{convq}^+ that is employed to provide the demanded *Q**. Specific details of the prioritization process are provided next:

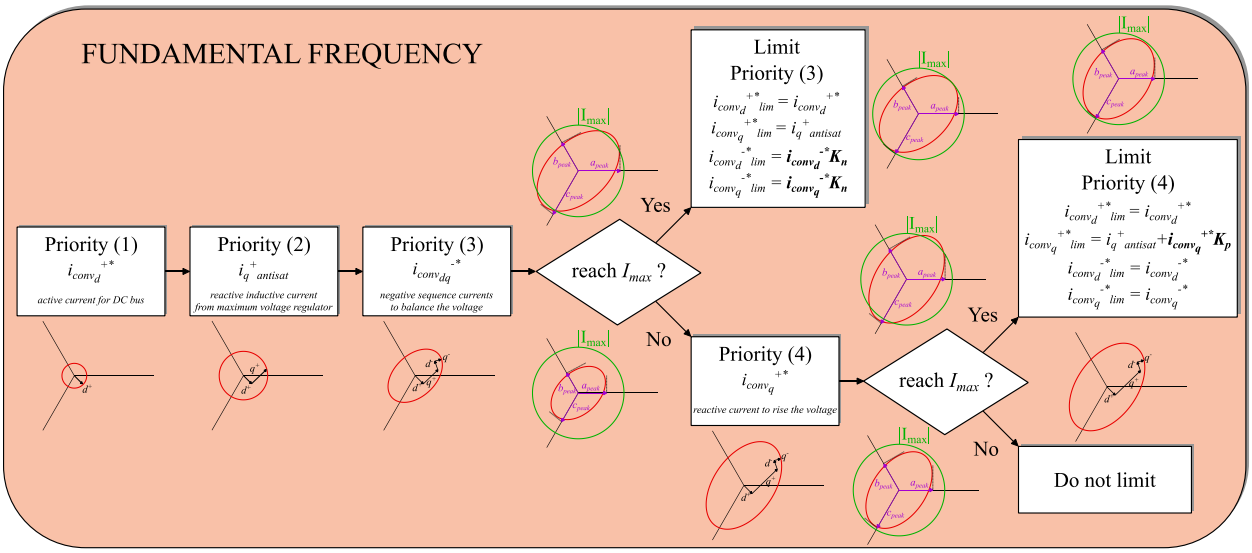

Fig. 5. Maximum current limitation procedure (implemented within right hand block of Fig. 3). Current components are sequentially added in a specific order of prioritization, until the limit (I_{max}) is reached (if is reached).

a) Priority (1)

The current component with the highest priority is i_{convd}^{+}. This current is an image of the active power exchanged by the converter with the grid. It is used to maintain the DC bus voltage of the converter (V_{bus}) to the required value, so the converter can operate properly [27]. In a practical STATCOM design, the i_{convd}^{+} in normal operation is far from the maximum current limit (I_{max}).

b) Priority (2)

In general, there is always some margin to include the second most prioritized current, i.e. $i_{\text{convq}}^{+}\text{antisat}$. This current component is created by the Maximum Voltage Regulator of Fig. 3 (left hand block). It is an inductive reactive current of positive sequence, used to ensure that the converter does not exceed the maximum voltage constraint. This fact is graphically explained in Fig. 6 (a) by means of space vectors. In addition, Fig. 6 (b) shows the block diagram of the Maximum Voltage Regulator needed to adjust the appropriate 'anti-saturation' current ($i_{\text{convq}}^{+}\text{antisat}$) at any moment. It is seen that this regulator first calculates the converter's reference voltage phase *abc* peaks. Then, if at least one of the calculated peaks exceeds the V_{max} limit, the $i_{\text{convq}}^{+}\text{antisat}$ current is progressively increased through a PI regulator, until the exceeded phase voltage equals the voltage limit V_{max}. Note that the output of the PI regulator presents a minimum saturation limit at zero, so when the error is negative (voltage limit V_{max} not exceeded) the output signal is zero as well.

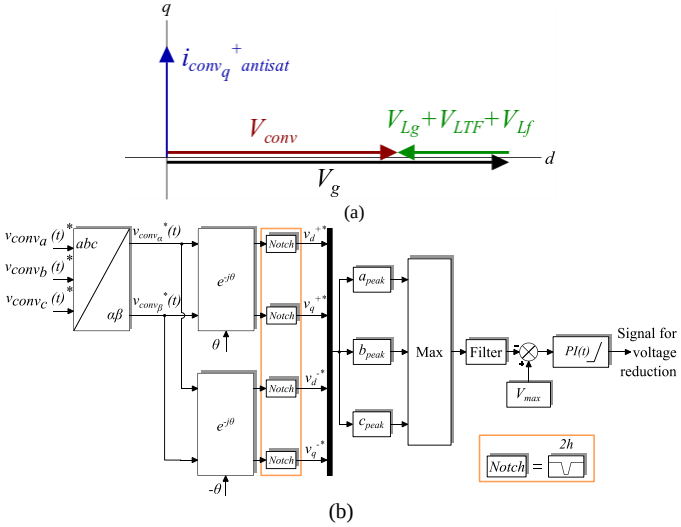

Fig. 6. (a) Graphical representation showing that the current $i_{\text{convq}}^{+}\text{antisat}$ helps reducing the converter's voltage for a given grid voltage (approximated analysis), (b) Maximum voltage regulator that is implemented in Fig. 3.

Table I Reduction constants K_n, for negative sequence.

$$I_{max}^{\ 2} = \left(i_{conv_d}^{\ +}\right)^2 + \left(i_{conv_q}^{\ +}{}_{antisat}\right)^2 + \left(i_{conv_d}^{\ -}K_{n_a}\right)^2 + \left(i_{conv_q}^{\ -}K_{n_a}\right)^2 + 2\left(i_{conv_d}^{\ +}i_{conv_d}^{\ -}K_{n_a} - i_{conv_q}^{\ +}{}_{antisat}i_{conv_q}^{\ -}K_{n_a}\right) \quad (16)$$

$$I_{max}^{\ 2} = \left(i_{conv_d}^{\ +}\right)^2 + \left(i_{conv_q}^{\ +}{}_{antisat}\right)^2 + \left(i_{conv_d}^{\ -}K_{n_b}\right)^2 + \left(i_{conv_q}^{\ -}K_{n_b}\right)^2 + i_{conv_q}^{\ +}{}_{antisat}i_{conv_q}^{\ -}K_{n_b} - i_{conv_d}^{\ +}i_{conv_d}^{\ -}K_{n_b} - \sqrt{3}\left(i_{conv_q}^{\ +}{}_{antisat}i_{conv_d}^{\ -}K_{n_b} + i_{conv_d}^{\ +}i_{conv_q}^{\ -}K_{n_b}\right) \quad (17)$$

$$I_{max}^{\ 2} = \left(i_{conv_d}^{\ +}\right)^2 + \left(i_{conv_q}^{\ +}{}_{antisat}\right)^2 + \left(i_{conv_d}^{\ -}K_{n_c}\right)^2 + \left(i_{conv_q}^{\ -}K_{n_c}\right)^2 + i_{conv_q}^{\ +}{}_{antisat}i_{conv_q}^{\ -}K_{n_c} - i_{conv_d}^{\ +}i_{conv_d}^{\ -}K_{n_c} + \sqrt{3}\left(i_{conv_q}^{\ +}{}_{antisat}i_{conv_d}^{\ -}K_{n_c} + i_{conv_d}^{\ +}i_{conv_q}^{\ -}K_{n_c}\right) \quad (18)$$

$$K_{n_a} = \frac{\sqrt{\left(i_{conv_d}^{\ -}\right)\left(I_{max}\right)^2 - \left(i_q^{\ +}{}_{antisat}\right)^2\left(i_{conv_q}^{\ -}\right)^2 + \left(I_{max}\right)^2\left(i_{conv_q}^{\ -}\right)^2} - \left(i_{conv_d}^{\ -} - i_{conv_d}^{\ +}\right)}{\left(i_{conv_d}^{\ -}\right)^2 + \left(i_{conv_q}^{\ -}\right)^2} \quad (19)$$

$$K_{n_b} = \frac{\sqrt{3\left(i_{conv_d}^{\ -}\right)^2\left(i_{conv_d}^{\ +}\right)^2 + 4\left(i_{conv_d}^{\ -}\right)^2\left(I_{max}\right)^2 + 2\sqrt{3}\left(i_{conv_d}^{\ -}\right)\left(i_{conv_d}^{\ +}\right)^2\left(i_{conv_q}^{\ -}\right) - \left(i_{conv_d}^{\ +}\right)^2\left(i_{conv_q}^{\ -}\right)^2 + 4\left(I_{max}\right)^2\left(i_{conv_q}^{\ -}\right)^2} + \left(i_{conv_d}^{\ -}\right)\left(i_{conv_d}^{\ +}\right) + \sqrt{3}\left(i_{conv_d}^{\ +}\right)^2\left(i_{conv_q}^{\ -}\right)}{2\left(\left(i_{conv_d}^{\ -}\right)^2 + \left(i_{conv_q}^{\ -}\right)^2\right)} \quad (20)$$

$$K_{n_c} = \frac{\sqrt{3\left(i_{conv_d}^{\ -}\right)^2\left(i_{conv_d}^{\ +}\right)^2 + 4\left(i_{conv_d}^{\ -}\right)^2\left(I_{max}\right)^2 - 2\sqrt{3}\left(i_{conv_d}^{\ -}\right)\left(i_{conv_d}^{\ +}\right)^2\left(i_{conv_q}^{\ -}\right) - \left(i_{conv_d}^{\ +}\right)^2\left(i_{conv_q}^{\ -}\right)^2 + 4\left(I_{max}\right)^2\left(i_{conv_q}^{\ -}\right)^2} + \left(i_{conv_d}^{\ -}\right)\left(i_{conv_d}^{\ +}\right) - \sqrt{3}\left(i_{conv_d}^{\ +}\right)^2\left(i_{conv_q}^{\ -}\right)}{2\left(\left(i_{conv_d}^{\ -}\right)^2 + \left(i_{conv_q}^{\ -}\right)^2\right)} \quad (21)$$

c) Priority (3)

In a normal STATCOM design, in general, there is always margin to include the third most prioritized current, i.e. the negative sequence current (both i_{convd}^{-} and i_{convq}^{-}). This current is employed to assist to the voltage balancing of the grid at the PCC. After adding this negative sequence current (both *d* and *q* components), the peak phase currents are calculated according to expressions (13)-(15). If at any phase the maximum current limit I_{max} is exceeded, as shown in Fig. 5, the negative sequence current is limited. In order to do so, a reduction constant K_n is applied to the negative sequence components *d* and *q*. The mathematical development is shown in equations (16)-(21). First, we incorporate the reduction constants for the negative sequence (K_{na}, K_{nb}, K_{nc}) to expressions (13)-(15). This way, we obtain expressions (16)-(18), where we assume that each phase reaches the maximum current limit and making zero the last prioritized current i_{convq}^{+}. Then, directly from these last expressions, the reduction constants are isolated. Thus, in order to limit the negative sequence, the reduction constant (K_{na}, K_{nb}, K_{nc}) of the phase with the biggest current peak is taken as K_n, as illustrated in the block of Fig. 5. On the contrary, if the current limit is not exceeded by any phase, the next prioritized current is tried to be included.

d) Priority (4)

Finally, the lastly prioritized current is i_{convq}^{+}, which is employed to provide the demanded *Q**. Thus, this current component is added and again the phase current peaks are calculated by applying equations (13)-(15). If any of the phases exceeds the maximum current limit (I_{max}), then in a similar manner as before, a reduction constant K_p is defined to calculate exactly how much current has to be reduced. This constant is derived as mathematical development shown in equations (22)-(27) (the procedure for obtaining the reduction coefficients is equivalent to the one followed in negative coefficients, but in

this case, the last prioritized current i_{convq}^{+} must be included at the expressions, and limited if necessary). By applying these reduction constants, the phase peak that exceeds its limit is reduced up to the maximum current limit (I_{max}). On the contrary, if the current limit is not exceeded, no reduction constant is necessary and the reference currents required by the user are left unmodified. It has to be remarked that following this general limitation method, different order of priorities can be defined depending of the specific needs of the grid where the STATCOM is going to be used. For practical reasons, in this article the presented order of priorities is only analyzed.

Table II Reduction constants K_p, for positive sequence.

$$I_{max}^{2} = \left(i_{conv_d}^{+}\right)^2 + \left(i_{conv_q}^{+}{}_{antisat} + i_{conv_q}^{+} K_{p_a}\right)^2 + \left(i_{conv_d}^{-}\right)^2 + \left(i_{conv_q}^{-}\right)^2 + 2\left(i_{conv_d}^{+} i_{conv_d}^{-} - \left(i_{conv_q}^{+}{}_{antisat} + i_{conv_q}^{+} K_{p_a}\right) i_{conv_q}^{-}\right) \quad (22)$$

$$I_{max}^{2} = \left(i_{conv_d}^{+}\right)^2 + \left(i_{conv_q}^{+}{}_{antisat} + i_{conv_q}^{+} K_{p_b}\right)^2 + \left(i_{conv_d}^{-}\right)^2 + \left(i_{conv_q}^{-}\right)^2 + \left(i_{conv_q}^{+}{}_{antisat} + i_{conv_q}^{+} K_{p_b}\right) i_{conv_q}^{-} - i_{conv_d}^{+} i_{conv_d}^{-} - \sqrt{3}\left(\left(i_{conv_q}^{+}{}_{antisat} + i_{conv_q}^{+} K_{p_b}\right) i_{conv_d}^{-} + i_{conv_d}^{+} i_{conv_q}^{-}\right) \quad (23)$$

$$I_{max}^{2} = \left(i_{conv_d}^{+}\right)^2 + \left(i_{conv_q}^{+}{}_{antisat} + i_{conv_q}^{+} K_{p_c}\right)^2 + \left(i_{conv_d}^{-}\right)^2 + \left(i_{conv_q}^{-}\right)^2 + \left(i_{conv_q}^{+}{}_{antisat} + i_{conv_q}^{+} K_{p_c}\right) i_{conv_q}^{-} - i_{conv_d}^{+} i_{conv_d}^{-} + \sqrt{3}\left(\left(i_{conv_q}^{+}{}_{antisat} + i_{conv_q}^{+} K_{p_c}\right) i_{conv_d}^{-} + i_{conv_d}^{+} i_{conv_q}^{-}\right) \quad (24)$$

$$K_{p_a} = \frac{\left(i_{conv_q}^{-}\right) + \sqrt{\left(-\left(i_{conv_d}^{-} + i_{conv_d}^{+} + I_{max}\right)\left(i_{conv_d}^{-} + i_{conv_d}^{+} - I_{max}\right)\right)}}{\left(i_{conv_q}^{+}\right)} \quad (25)$$

$$K_{p_b} = -\left(\frac{i_{conv_q}^{-} - \sqrt{3}\left(i_{conv_d}^{-}\right) + \sqrt{-\left(i_{conv_d}^{-}\right)^2 + 4\left(i_{conv_d}^{-}\right)\left(i_{conv_d}^{+}\right) - 2\sqrt{3}\left(i_{conv_d}^{-}\right)\left(i_{conv_q}^{-}\right) - 4\left(i_{conv_d}^{+}\right)^2 + 4\sqrt{3}\left(i_{conv_d}^{+}\right)\left(i_{conv_q}^{-}\right) + 4\left(I_{max}\right)^2 - 3\left(i_{conv_q}^{-}\right)^2}}{2\left(i_{conv_q}^{+}\right)}\right) \quad (26)$$

$$K_{p_c} = -\left(\frac{i_{conv_q}^{-} - \sqrt{3}\left(i_{conv_d}^{-}\right) + \sqrt{-\left(i_{conv_d}^{-}\right)^2 + 4\left(i_{conv_d}^{-}\right)\left(i_{conv_d}^{+}\right) + 2\sqrt{3}\left(i_{conv_d}^{-}\right)\left(i_{conv_q}^{-}\right) - 4\left(i_{conv_d}^{+}\right)^2 - 4\sqrt{3}\left(i_{conv_d}^{+}\right)\left(i_{conv_q}^{-}\right) + 4\left(I_{max}\right)^2 - 3\left(i_{conv_q}^{-}\right)^2}}{2\left(i_{conv_q}^{+}\right)}\right) \quad (27)$$

III. CURRENT REFERENCES LIMITATION METHOD IN A STATCOM OPERATING SIMULTANEOUSLY PROVIDING REACTIVE POWER AND HARMONIC CURRENTS

A. General control block diagram

In this section, the references limitation method presented at the previous section, is extended to a more complex operation of the STATCOM. The basic idea of the limiter is now applied to a STATCOM that can simultaneously operate as a reactive power compensator and as an active power filter that controls several current harmonics. STATCOMs with this simultaneous operation capacities are being demanded more and more nowadays [4], [5], [30], in order to solve anomalies or problems arising is weak grids with strong penetration of power converters. Thus, the general control block diagram where the proposed limitation method is implemented, is depicted in Fig. 7.

Hence, for the specific case that has been analyzed in this article, the control contains 12 current control loops, being 4 of them used to control the *dq* positive and negative sequences of the fundamental current (h). Then, 4 more loops dedicated for controlling one specific harmonic (h_1), while finally, 4 more loops are dedicated for controlling a second specific harmonic (h_2). Since several frequencies of currents are simultaneously being controlled, it is seen that a specific notch filter combination must be used at each sequence decomposition [31]. Note that depending on the specific application where this STATCOM is going to be used, it could be also possible to use a greater number of loops, dedicated to control a greater number of harmonics. However, in this article, for simplicity in the exposition, two harmonics (h_1) and (h_2) are controlled, together with the fundamental component current (h).

Regarding the current references generation, the control system studied at this section, in comparison with the control presented at previous section (Fig. 1), maintains how the fundamental frequency current reference generation is carried out. In addition, it is also necessary to create the references for the rest of the loops dedicated for controlling the current harmonics (h_1) and (h_2). There are several possibilities for doing this [5], [32], [33], but in this article, this fact is not considered and is supposed that these current references are created externally. Nevertheless, the limiter proposed in this section is useful no matter how the current references are created.

B. Current references limitation method

Before proceeding to describe the working principle of the limiter, a realistic context that justifies its needs is firstly proposed [5]: it is assumed that the STATCOM device is connected to a weak grid, where it might be affected by any type or degree of unbalanced voltages and any type of voltage harmonics. Then, in a very similar way as in previous section, it is supposed that the 'user' of the STATCOM has programmed a certain fixed active impedance for each voltage harmonic that wants to be corrected (Z_{h1} and Z_{h2}). Simultaneously, the user can demand a reactive power reference Q^*, without knowing which is the current state of the grid (unbalance level and harmonic levels, that change continuously during the day). This means that although it knows the maximum current and voltage limits of the converter (current and voltage constraints, I_{max} and V_{max}), it does not really know if the reference Q^* and the programmed active impedances can be fully provided or not, without exceeding the voltage or current limits, or even both. Thus, in an equivalent way as done in previous section, if the actual Q^* demand, combined with the actual unbalance and harmonics levels of the grid voltage, exceed the current and/or voltage constraint, the limiter will limit the current references as shown in Fig. 7.

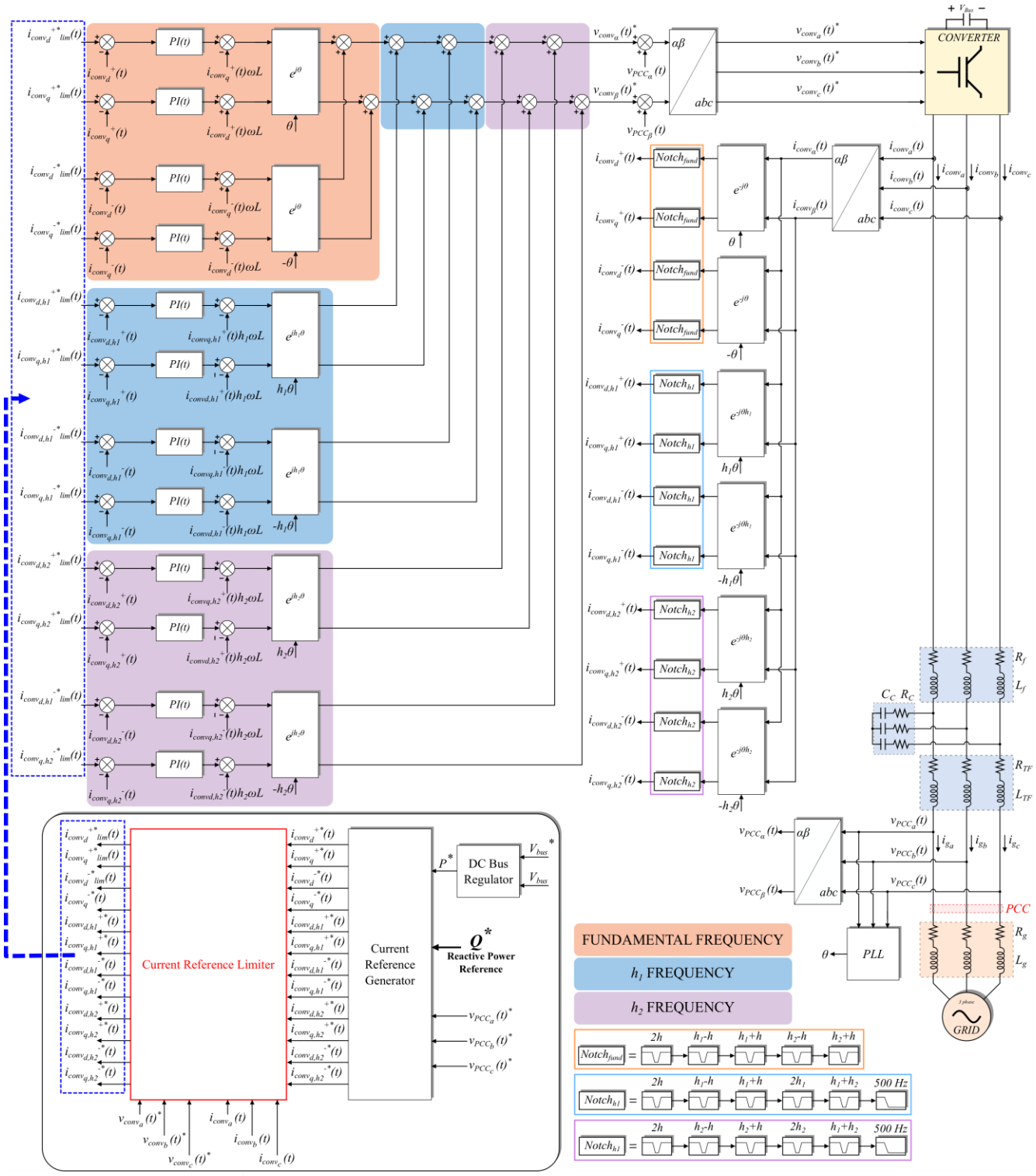

Fig. 7. Control strategy and current references limitation in a STATCOM that can simultaneously provide reactive power and current harmonics (L=L_f+L_{TF}).

In this way, the converter's current and/or voltage (the exceeded one in every case, or even both) of the converter will be set at its maximum value.

The conceptual block diagram of the current reference limiter is depicted in Fig. 8. It is composed by three main blocks that perform three main tasks. One block is dedicated to performing the 'maximum current limiter', then a second block is a 'correction loop' associated to the 'maximum current limiter', while the third block is oriented to ensure that the 'maximum voltage limit' is not exceeded.

1) Phase maximum calculations

The criteria used for the limitation of the current references is based again on the space vector theory. The calculation that must be performed is the peak of each phase *abc*, at the converter's current. Since in general the converter is operating with three current frequencies (h), (h_1) and (h_2), the accurate peak current calculation by a mathematical equation becomes not trivial (see next section VI for further discussion).

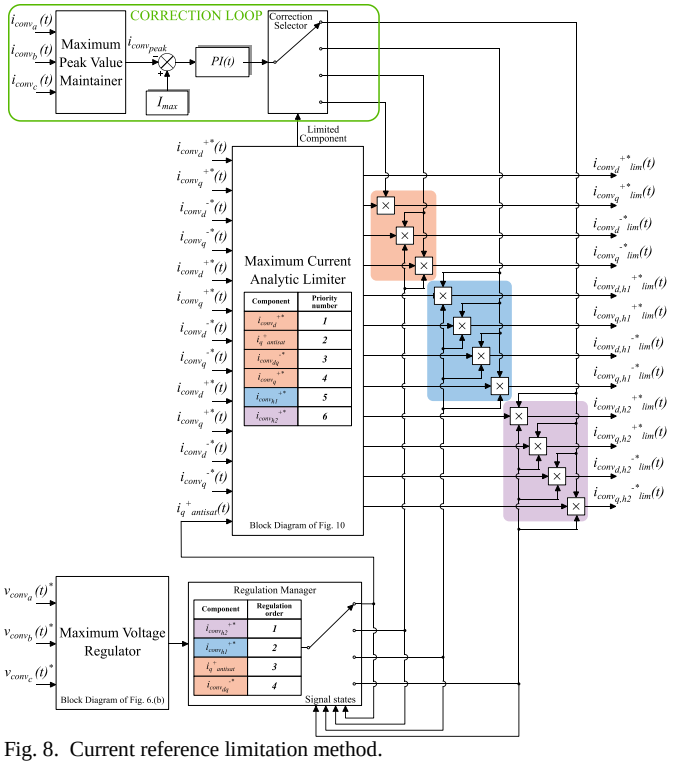

Fig. 8. Current reference limitation method.

A practical solution adopted in this article, works as follows: from the current references for each current harmonic (including the fundamental component *h*), the peak *abc* current of each harmonic is calculated separately according to expressions (13)-(15). Then, the approximated total current *abc* current peak is calculated, by adding directly the three pre-calculated peaks for each harmonic:

$$I_{peak_a} \simeq |I_{a_h}| + |I_{a_{h1}}| + |I_{a_{h2}}| \quad (28)$$

$$I_{peak_b} \simeq |I_{b_h}| + |I_{b_{h1}}| + |I_{b_{h2}}| \quad (29)$$

$$I_{peak_c} \simeq |I_{c_h}| + |I_{c_{h1}}| + |I_{c_{h2}}| \quad (30)$$

Note that these equations perform a worst-case peak calculation, which means that the actual current peak will be always smaller (or equal only in a unique case) than this approximation. As graphically represented in Fig. 9, the peak current will depend on the phase shift between the current harmonics and their amplitudes. So, for given amplitudes of currents, there is a worst-case phase shift that produces the maximum current peak. That particular phase shift is the direct summation of the currents provided by expressions (13)-(15). Thus, performing this simple peak calculation, we are approximating the calculation to the worst current peak. In addition, this approximated calculation of the total *abc* current peak allows to implement the 'Maximum current limitation' procedure according to the block diagram of Fig. 10, which reasonably follows the limitation philosophy seen in the previous section. The different current components are added sequentially according to a pre-defined priority order. If at every current addition the current limit I_{max} is reached, the last current component is limited; otherwise, the next prioritized current component is added.Then, in order to correct the error assumed at this simplified calculation, a second block is added to the limiter depicted in Fig. 8 (block located at the top of the figure). This block mainly corrects this error by means of a feedback loop. In this loop, the *abc* currents are measured and the biggest peak (can be at phase *a*, *b* or *c*, depending on the instantaneous state of the grid voltage) is compared to the limit of the current I_{max} (same idea as the voltage regulator seen in previous section, Fig. 6, but with currents as inputs instead of voltages). If the error is positive, the PI regulator increases a correction signal that is multiplied by the last limited (prioritized) current component, leading to the biggest peak phase current to the limit I_{max}.

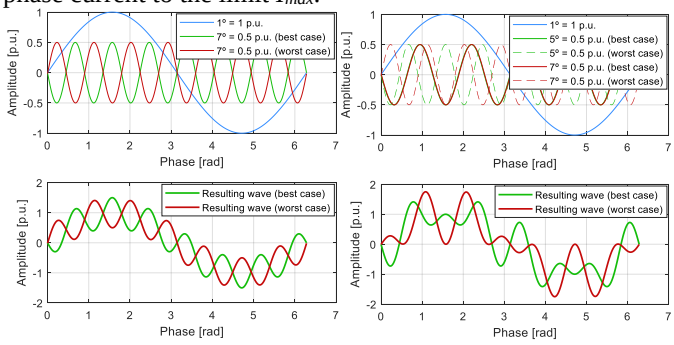

Fig. 9. Two illustrative examples of current summations of different frequencies and their dependence on the phase shift. (a) fundamental component added to a 7th harmonic, (b) fundamental component added to a 5th and a 7th harmonic.

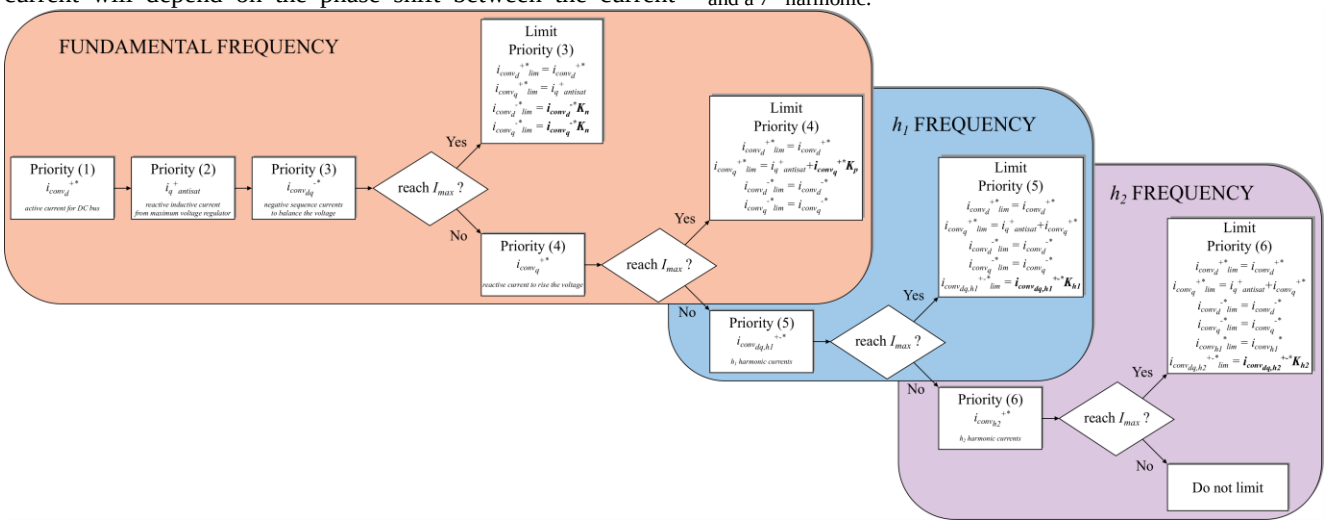

Fig. 10. Maximum current limitation procedure (implemented within central block of Fig. 8). Current components of different harmonic currents are sequentially added in order of prioritization, until the limit (I_{max}) is reached (if is reached).

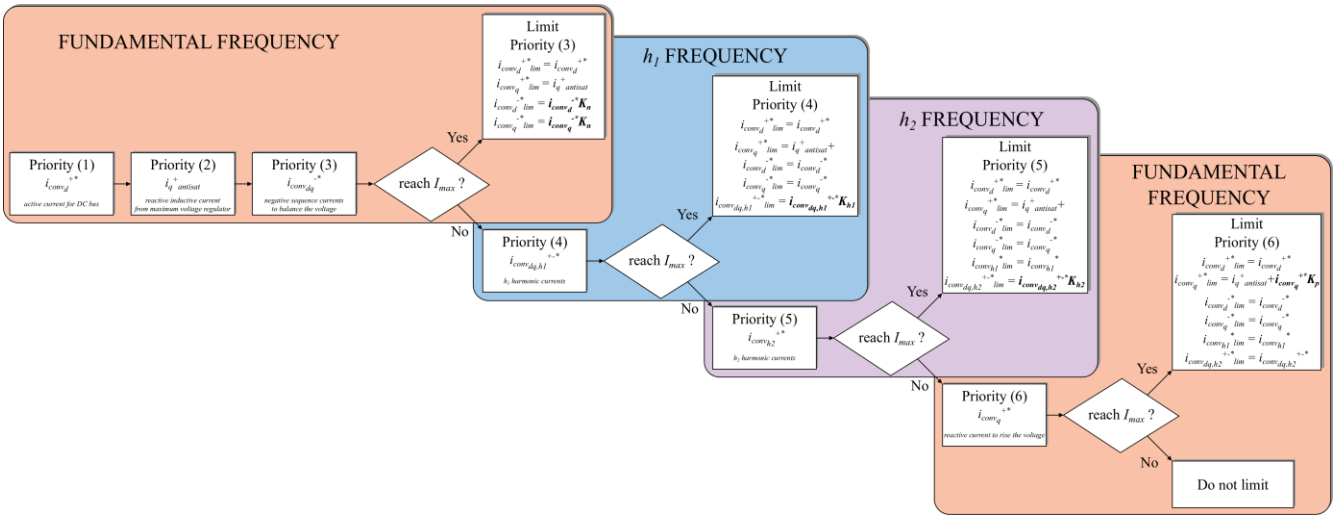

Fig. 11. Illustrative example of maximum current limitation procedure, with a different prioritization order to the one followed in Fig. 10 (not implemented at the validation sections).

This correction loop is normally tuned to be dynamically 'slower than the current control loops'. It is important to remark that the correction loop is only enabled when the system operates at steady-state, so if a variation of current references is detected, it is disabled.

Once the limiter ensures that the reference signals passed to the vector control loops do not exceed the current limit (I_{max}), it is necessary to supervise that the synthesized voltage does not exceed the voltage limit V_{max}. For that purpose, the same philosophy as used in the previous section is followed. It is graphically represented in the block at the bottom of Fig. 8 (same idea as voltage regulator seen in previous section, Fig. 6). This new loop acts either by injecting an inductive reactive current, or by reducing the harmonic references. This order of action can be adapted to the specific needs in each context. When the voltage regulation loop is operating, the value of the regulator of the current correction loop is frozen, so that it does not interfere in the reduction of the current references.

Finally, as an illustrative example, Fig. 11 shows an alternative sequence order of prioritizations compared to the one shown in Fig. 10. Note that, if desired, it would be even possible to prioritize harmonic components to certain components of the fundamental frequency component.

IV. Simulation Based Validation of the Limitation Method

In this section the previously defined two limiters are validated by means of simulation results. The simulation-based analyses are developed in Matlab-Simulink models. The converter and filter characteristics are summarized in Table III. Note that the first limiter presented in this article can be understood as a particular case of the second limiter, when the converter is not operating with current harmonics (i.e., only with fundamental components). Taking this fact in mind, only the second limitation method is implemented in this validation, but the validation includes operating condition ranges where no harmonics are present, representing the operating conditions of the first limiter.

TABLE III. SYSTEM CHARACTERISTICS FOR SIMULATION BASED VALIDATION

Variable	Value
S	24 MVA
V_{PCC}	3650 $V_{LL\text{-}RMS}$
V_{bus}	6900 V
V_{max} (converter)	3984 $V_{peak\ phase}$
I_{max} (converter)	2121 A_{RMS}
R_f	3.5 mΩ
L_f	375μH
R_c	100 mΩ
C_c	3120 μH
R_{TF}	1 mΩ
L_{TF}	28 mH
R_g	175 mΩ
L_g	7.85μH

Hence, the validation that is carried out performs a time domain simulation that passes through different operating conditions. The programmed reactive power reference Q^* together with 5th and 7th harmonics current reference profiles are represented in Fig. 12. These profiles are chosen in order to check different operation conditions for the limiter, so during some time ranges voltage limit and/or current limits are exceeded, and the limiter curtails the current references. Note that any other pair of harmonic order could be chosen for the validation instead of the 5th and 7th.

Fig. 13 shows the performance of the implemented 12 current loops (Fig. 7) under the programmed reference profiles. In addition, it must be remarked that a grid voltage unbalance is also programmed during time intervals 1.5-1.7 s and 2.7-2.9 s. This unbalance corresponds to a Type C fault of 0.6 [p.u.] depth between *b* and *c* phases. Thus, in Fig. 13 it is seen that, depending on the state of the references, the necessary converter's voltage and current differs and therefore, the limiter needs to limit in some cases some of the converter's current references, according to the programmed prioritization criteria (Fig. 10) so as to operate within the voltage and current limits. Fig. 14 shows the *abc* waveform of the converter current and voltages, together with the voltage at the PCC (Fig. 14 (a), (b) and (c)). Fig. 14 (d), (e) and (f) illustrate the time interval where the Q^* is capacitive and at the beginning, the converter operates

at the maximum voltage limit V_{max}, with current references of the 5th and 7th harmonics limited. When suddenly the voltage unbalance appears, with actual state of the references, the converter starts operating at the current limit I_{max}, being necessary to completely eliminate the harmonic current references. All these current reference limitations are automatically created by the limiter.

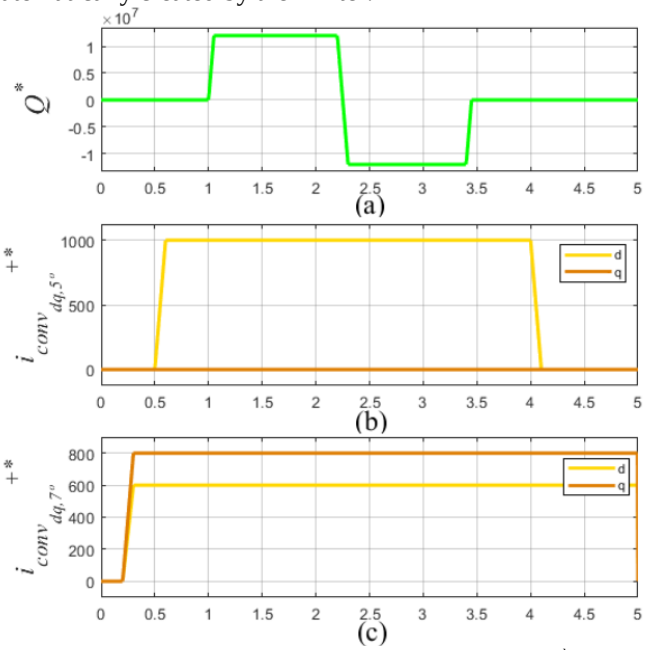

Fig. 12. Reference variations programed in (a) reactive power, (b) 5th harmonic, (c) 7th harmonic.

Fig. 14 (g), (h) and (i) illustrate the time interval where the Q^* is inductive and at the beginning, the converter operates at the maximum current limit I_{max}, with current references of the 5th and 7th harmonics limited. When suddenly the voltage unbalance appears, the converter continues operating at the current limit I_{max}, being necessary to completely eliminate the harmonic currents for a proper operation within the constrains. Finally, Fig. 14 (j), (k) and (l) show the time interval where the Q^* is inductive and the phase *b* exceeds the current limit I_{max} operating with 5th and 7th harmonics. At the initial moment (at second 3 approximately) the limiter analytically limits the references 'in excess', while after some few periods, the correction loop progressively increases the corresponding current reference, reaching phase *b* the current limit I_{max}.

It must be remarked that there are many other different cases where the limiter could operate under different circumstances, but they have not been included in the results for the sake of simplicity. It is worth to mention that in all tests that the authors have done the limiter has operated successfully.

Finally, note that the oscillations seen at the different *dq* current components when only one current changes, are due to the coupling of the different harmonics and sequences among the loops [31]. Nevertheless, these oscillations are due to the transient response of notch filters used for sequence decompositions (Fig. 7), but are not seen at the real *abc* currents of the converter as shown in Fig. 14.

V. Experimental Validation of the Limitation Method

A. Maximum Current Limiter and Correction-Loop

This section validates the performance of the proposed limitation method (Fig. 8 and 11, with only one harmonic control instead two) under a downscaled experimental platform. The converter and filter characteristics are summarized in Table IV. In this case, only a pure inductive filter is available for the experimental results in the laboratory and only one harmonic is controlled for the sake of simplicity. However, the conclusions can be extended to a more complex scenario as the one analyzed in the previous sections.

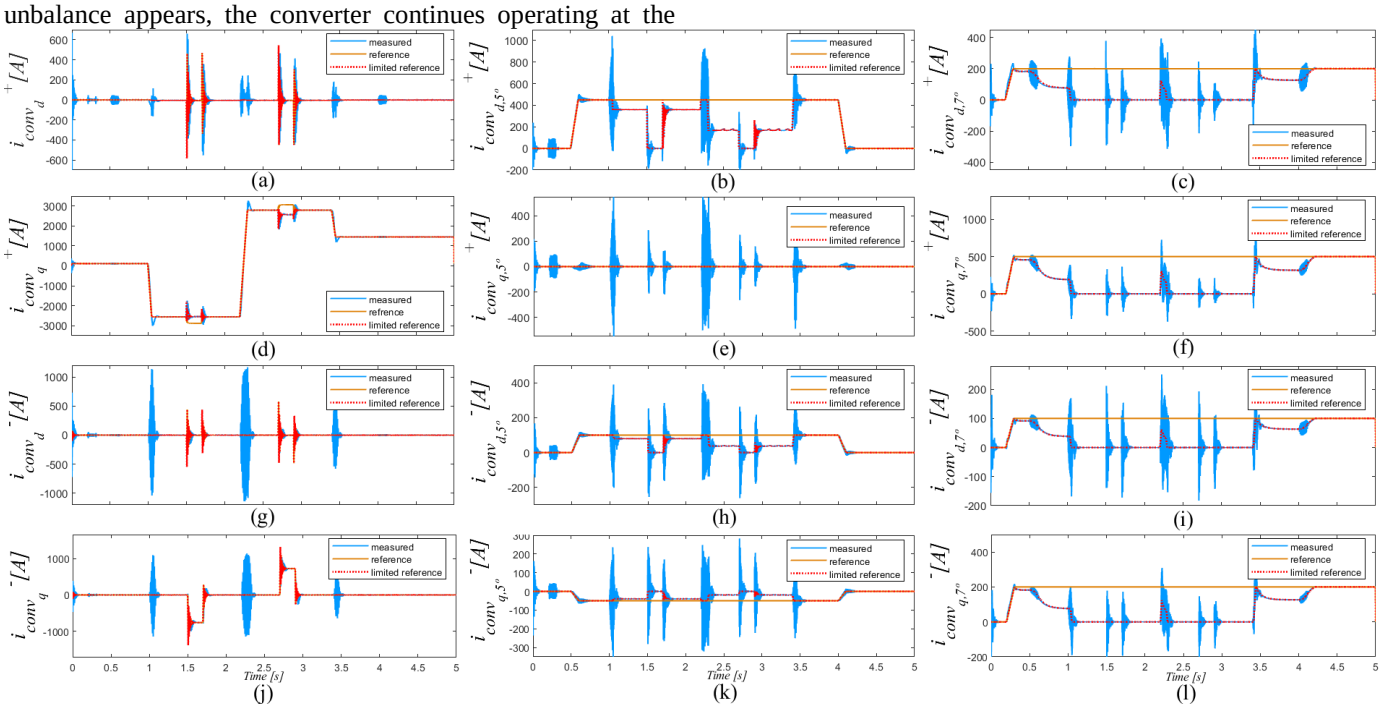

Fig. 13. Time domain simulation where the proposed limitation method of this article (Fig. 8 and Fig. 10), limits whenever is necessary the corresponding converter's current references. Performance of the 12 current loops implemented (Fig. 7), under the programmed reference profiles of Fig. 12.

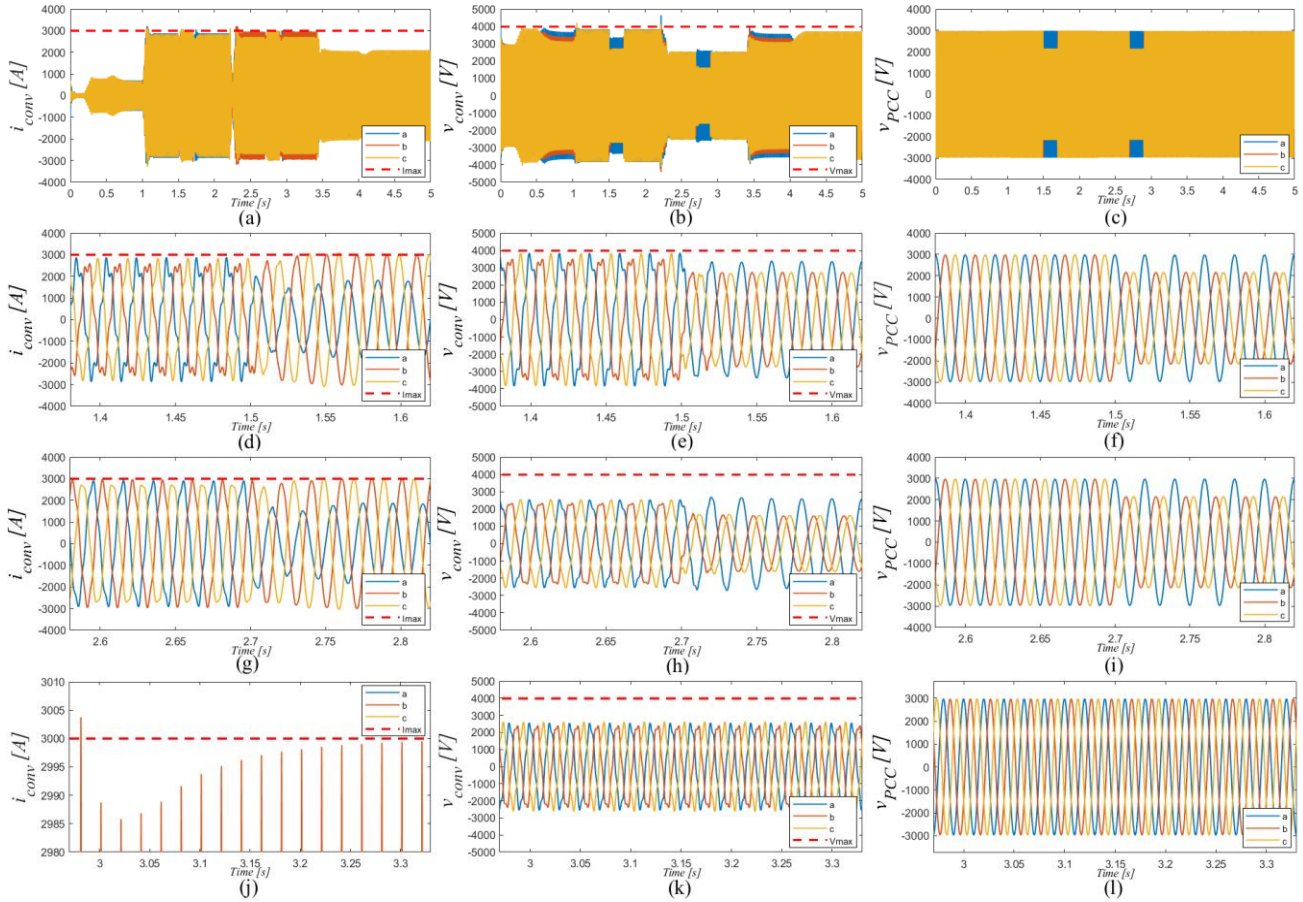

Fig. 14. Time domain simulation where the proposed limitation method of this article (Fig. 8 and Fig. 10), limits whenever is necessary the corresponding converter's current references. Performance of the *abc* converter's current and voltages together with the PCC voltage, under the programmed reference profiles of Fig. 12.

In addition, a simulation-based model is developed that reproduces the characteristics and operating conditions of the experimental platform. The simulation-based results of this model are superposed to the experimental based results, in order to detect any possible mismatch.

TABLE IV. SYSTEM FOR EXPERIMENTAL VALIDATION

Variable	Value
V_{PCC}	25 $V_{peak\ phase}$
V_{bus}	75 V
V_{max} (converter)	35 $V_{peak\ phase}$
I_{max} (converter)	9 A_{peak}
R_f	1 mΩ
L_f	4 mH
Control task time	250μs
Switching frequency	8 kHz
Power Converter Topology	2 Level

As in the previous section, only the second limiter is implemented in this experimental validation. A switching frequency of 8 kHz is chosen in order to have sufficiently good quality of waveforms. On the other hand, a control task time of 250μs (4 kHz) is selected for the controller, since the control hardware where the algorithm is implemented cannot go faster.

The validation that is carried out performs several experiments that pass through different operating conditions. Different reactive power reference Q^* together with 7th current reference harmonic profiles are programmed. Thus, Fig. 15 shows the *abc* currents and voltages of the converter, together with the performance of the implemented 8 loops (4 loops for the fundamental component and 4 more loops for 7th harmonic). At the beginning of the test, an increase of i_{convq}^+ is programmed, forcing the limiter to reduce the harmonic reference not to exceed the current limit I_{max}. At the first stage, the analytical limiter (central block at Fig. 8) reduces the current references in excess (equations (28)-(30)). Then, the correction loop (block at the top of Fig. 8) progressively increases the harmonic current reference (activated at second 1.5 for a clearer visualization) until the converter ends operating exactly at the current limit I_{max}. Note that thanks to this method, although the analytical limiter is not exact (equations (28)-(30) limit more than needed) it guarantees that the currents at steady state will never go beyond the current limit I_{max}. Then, in Fig. 15 (b) and (c) a zoom of the current is shown, illustrating the converter's *abc* currents before and after, the correction loop is activated. During this experiment, the voltage limit is not reached. After this first experiment, in Fig. 16 a second experiment is presented which is a continuation of the previous one. In this case, at the beginning of the experiment the current component i_{convq}^+ is further ramped from 7 to 10 A. Under these circumstances, the limiter must reduce the harmonic current reference until completely eliminating it. In this case, since the harmonic has been fully eliminated (only the fundamental current component is remaining), the analytical limiter is precise and therefore limits the reference currents exactly at the limit I_{max}. This means that the correction loop does not actuate in this case. Finally, it can be highlighted that in all the results, the simulation based performances and the experimental based performances coincide reasonably well.

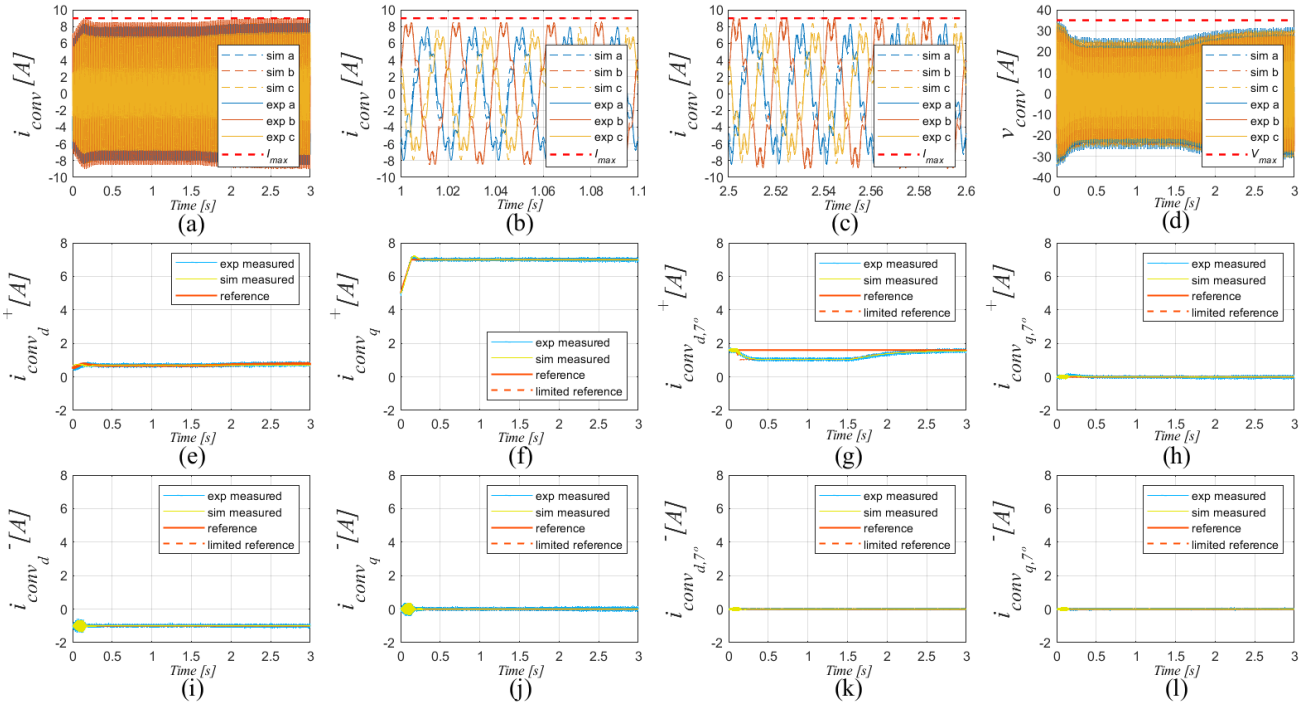

Fig. 15. Experimental and simulation based *abc* currents and voltages of the converter, together with the performance of the 8 loops implemented (4 loops for the fundamental component and 4 more loops for 7th harmonic), with an increase of the i_{convq}^{+} from 5 to 7 A, showing that the limiter guarantees the operation at the maximum current I_{max}.

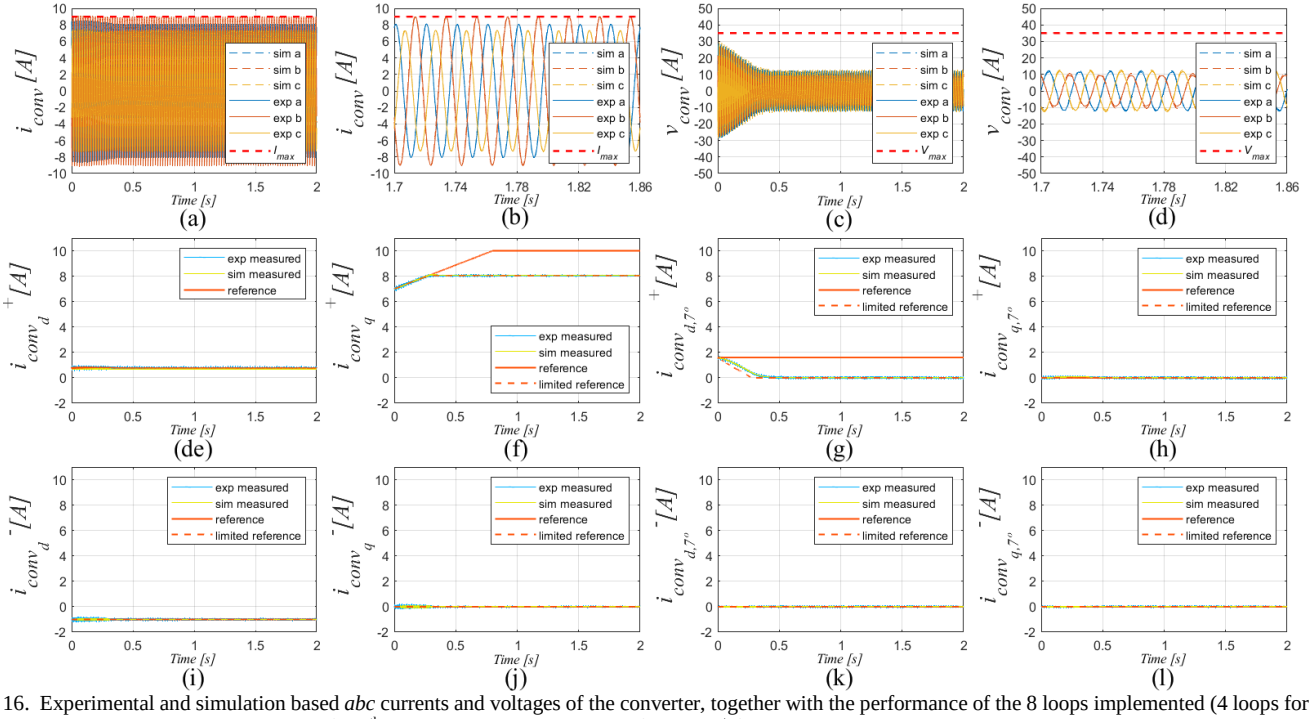

Fig. 16. Experimental and simulation based *abc* currents and voltages of the converter, together with the performance of the 8 loops implemented (4 loops for the fundamental component and 4 more loops for 7th harmonic), with an increase of the i_{convq}^{+} from 7 to 10 A, showing that the limiter guarantees the operation at the maximum current I_{max}.

VI. Further Discussions

A. Necessity of the proposed limitation method

This section contains a brief discussion about some important issues that can clarify many related questions that might have arisen from the proposed limitation method.

First of all, it has to be highlighted that in a STATCOM application the current limiter is very necessary. Depending on the characteristics of the grid (PCC) where it is going to be connected, if the unbalance changes regularly (e.g. in weak grids), the 'user' who is programing the Q^* does not know how much can Q can the converter really provide. Thus, with help of the proposed limiter, it will be possible to always provide the maximum amount of Q if necessary. This fact is illustrated in Fig. 20 with a graphical example (system of Table III). In Fig. 17 (a) and (b), when the grid voltage is not unbalanced, the converter can provide more Q than when there is a certain unbalance at the grid, as illustrated in Fig. 17 (c) and (d). Note that the maximum voltage regulator is necessary specially

depending on the converter design, in relation to the characteristics of the grid (PCC) where it is going to be connected. More specifically, it strongly depends on the voltage of the DC bus as can be seen in Fig. 17 (b) and (d).

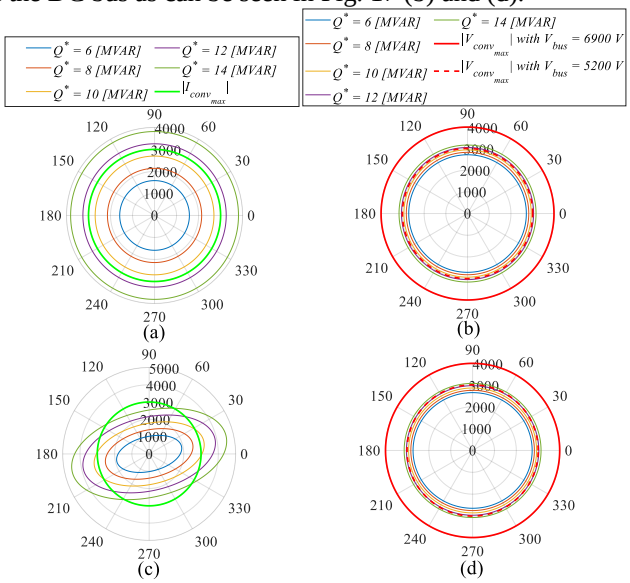

Fig. 17. I_{conv} (a) V_{conv} (b) with a balanced grid voltage. I_{conv} (c) V_{conv} (d) with unbalance at the grid voltage (40% of voltage drop at phase *a*, and 15% of voltage drop at phase c).

On the other hand, when the STATCOM operates simultaneously providing reactive power *Q* and certain number of harmonics, the necessity of the limiter is probably more obvious, because the combination of different harmonics yields to a more complex coupling scenario and the maximum voltage and current limits are reached 'easier'. It must be remarked that when there is a presence of harmonics of higher frequency, the voltage limit is reached easier, since the voltage needed to feed each harmonic depends on the frequency as $(L_{TF}+L_f)\cdot\omega\cdot h\cdot|I_h|$. This means that more converter voltage is needed with higher order of harmonic *h* to feed the equivalent inductance of the filter and transformer. This fact is numerically represented in a simplified manner in Table V. Thus, it is represented that the converter is only providing one harmonic (without providing reactive power) and it is shown which is the maximum current that can be controlled without exceeding the voltage limit. As can be seen, in every case the maximum current that can be exchanged is strongly reduced from the maximum current in which the converter has been designed I_{max}=2121A$_{rms}$.

TABLE V. MAXIMUM CURRENT THAT CAN BE PROVIDED AT EACH HARMONIC WITH THE SYSTEM PARAMETERS OF TABLE III AND V_{bus}=6900V.

Harmonic order	Maximum Harmonic Current due to Voltage Limit
3	1868 A$_{rms}$
5	1121 A$_{rms}$
7	801 A$_{rms}$
9	622 A$_{rms}$
11	509 A$_{rms}$
13	431 A$_{rms}$

Hence, it can be concluded that for a manufacturer that is going to install a STATCOM with various functionalities in a weak grid, it is almost compulsory to implement these type of limiters to ensure that it takes advantage of all the voltage and current which has 'invested' in its converter design.
In the practical experiences of this manufacturer, it has been seen that is very necessary.

B. Problem of the voltage limit overshoot of the maximum voltage regulator.

The maximum voltage regulator proposed in this paper (Fig. 6 (b)) operates when the converter voltage exceeds the maximum voltage limit V_{max}. Depending on how quick is this regulator dynamically tuned, and depending on how the V_{max} is chosen, this fact can be a problem because it can demand to the converter to operate with a voltage that it cannot provide.

For a general case, the authors propose to choose V_{max} at the modulation index, in the limit of the linear modulation of the converter. This means that when the maximum voltage regulator starts operating it will work at the over-modulation region [35]. During the operation under this over-modulation region when the regulator is correcting the current references, the quality of the synthetized converter voltage would be poorer than in linear modulation region. However, this is not a problem if the system is able to ensure the controllability. Then, obviously, the regulator must be carefully tuned so it quickly corrects the error and quickly tends to reduce the converter voltage needed, in order to avoid reaching the upper limit of the over-modulation that means loss of control.

Therefore, by following this strategy (choice of V_{max} at the maximum modulation index of the linear region), the converter will always operate within the limits of the linear modulation region at steady-state, while during transients where the maximum voltage regulator operates, the converter could work in the over-modulation region.

On the other hand, an alternative solution could be to reduce the limit V_{max} to a modulation index below 1 and therefore make the converter to always operate in the linear regulation region when the maximum voltage regulator operates. However, in this case, obviously the steady-state voltage operation of the converter would be reduced, also reducing its maximum *Q* and harmonics compensation capacity.

C. Exact mathematical expression for calculation of the peak phase current when operating with harmonics

Finally, in this subsection a short discussion of the most evident possible methods for the calculation of the peak phase current is carried out. The advantages and disadvantages of the methods studied are summarized in Table VI. The first studied method, which is the one proposed and implemented in this article, is based on the approximated calculation of peak phase currents, using equations (28)-(30). This method requires a correction loop that after a few milliseconds reaches the exact limitation. This delay in achieving 'the exactness' is not a problem in requirements of most STATCOM applications, since they often do not demand extremely fast dynamic responses. As advantages, it is simple and easy to adapt to different converter and harmonic mitigation needs. In addition, the method guarantees not exceeding the current limit I_{max} at steady-state, since the correction loops always tends to increase the current references to reach the limit.

Then, the second method that has been studied consist of a time-domain-based prediction of the current phase peaks. By

defining a sufficiently small sample time (microseconds), the phase peak currents are reconstructed from the current references in *dq* frame every half of the period of the grid, by using the Clarke and rotational transformations [31]. In this way, 'when' the maximum peak will occur can be predicted, and obviously how much is in amplitude. However, after several trials made by the authors, it has been concluded that although the method conceptually is easy to understand, it is computationally too expensive computationally and impossible to be implemented in today's standard control hardware.

Then, in relation to the previous method, it has been also studied a conceptually similar method. The idea is to avoid the online computation needs by using pre-calculated look up tables. Thus, by an exhaustive off-line pre-calculation exercise of all possible current reference values, the peaks are calculated for all the combinations of possible reference values and stored in memory tables . Unfortunately, if a reasonably good precision is desired, today's standard control hardware is not prepared to store such high amount of data on memory in a practical way.

Many efforts have also been carried out to find exact mathematical expressions of the peaks. Several methods have been tried, and although some nice solutions have been found for combinations of harmonics of order 1, 3 and 5, it has not been possible to find a mathematical general solution that covers all the typical harmonics: 3, 5, 7, 9, 11 and 13. Due to this fact, this method has been discarded since in practical applications, harmonics 7 to 13 are often demanded to be corrected and a solution to limit them is compulsory.

TABLE VI. ADVANTAGES AND DISDVANTAGES OF THE PEAK PHASE CURRENT CALCULATION METHODS STUDIED

Method	Advantages	Disadvantages
Direct addition of amplitudes	Easy to implement and adaptable to different priorities	A correction loop is needed to reach exactness in few milliseconds
Time-domain-based prediction based on computations	Conceptually is easy to understand and accurate. It does not need correction loop.	Computationally unaffordable
Pre-calculated look up tables	Conceptually is easy to understand and accurate. It does not need correction loop.	Unaffordable due to a large memory need
Exact mathematical expressions	Accurate and implementable	Solution has not been found for all the possible combination of harmonics
Calculation of the phase peaks from the measured currents	Easy to implement	The limit I_{max} is exceeded, a correction loops is needed and the 'sample time' of the limiter is reduced to one cycle of the grid

Finally, there is also another method that has been studied. The idea is 'to limit afterwards'. The limiter would be based on the calculation of the phase peaks from the measured currents, which is reasonably easy to implement, once per cycle of the grid voltage. Then, if it is detected that the limit is exceeded, the current references are reduced progressively until the maximum peak current is at the limit I_{max}. This would be an exactly equivalent method to the one used for the maximum voltage regulation (Fig. 6(b)) but applied to the current. Note that this method forces the converter to work above the current limit for some periods of time, which thermally perhaps could be possible, but is a 'non-comfortable' and 'risky' solution from a manufacturer point of view. Note that the stress of the converter suffered along the cycle of life of the converter could be penalized.

Consequently, it can be concluded that the proposed peak calculation method of the article is the best method from the studied and compared ones.

To conclude, Table VII provides a quantification of the error produced by the method proposed (equations (28)-(30)) with some different harmonic combinations. As can be noticed, the correction loop for instance when harmonics 7 and 11 are combined, will never need to correct an error bigger than 21%. Note that this error is quickly corrected after few milliseconds by the correction loop.

TABLE VII. AMPLITUDE ERRORS PRODUCED FROM THE MAXIMUM AMPLITUDE CASE (EQUATIONS (28)-(30)) TO MINIMUM AMPLITUDE CASE (NOTE THAT THE ERROR IS CORRECTED AFTER FEW MILLISECONDS BY THE CORRECTION LOOP).

Harmonics	Amplitude of the harmonics respect the fundamental component				
	10%	25%	50%	75%	100%
1, 3, 5	21,52	33,83	39,68	40,71	42,02
1, 3, 7	18,55	29,36	34,89	38,78	35,38
1, 3, 11	17,18	26,44	29,07	24,72	21,99
1, 3, 13	17,01	26,37	24,47	23,23	22,68
1, 5, 7	17,83	30,18	37,77	33,21	30,98
1, 5, 11	14,63	21,29	28,42	28,17	28,37
1, 5, 13	14,03	28,28	28,42	19,16	20,37
1, 7, 11	14,31	21,94	20,12	19,11	18,75
1, 7, 13	12,04	18,43	25,39	27,07	27,51
1, 11 13	16,53	26,98	30,58	29,51	27,16

VII. CONCLUSIONS

In the practical experience of the manufacturer, in such applications of STATCOM devices applied to weak grids where the grid voltage can vary repeatedly, a limiter like the proposed in this article is very necessary in order to get the most of every single Volt and Amp invested at the converter.

On the other hand, simulation and experimental validations have demonstrated that the limitation method has successfully worked in a wide variety of tests, limiting the current references in order to cope with the objective of not exceeding the converter's current and voltage limits. In addition, since the method is not computationally expensive, it can be implemented in a standard hardware at a sample time equal as the sample time of the controller (micro-seconds).

Added to this, under the performed multiple tests, the proposed limitation method has resulted in a flexible limiter that can be easily reconfigured to the needs of the specific application, is aspects such as:

- Number and order of harmonics that the STATCOM is going to compensate (for instance simultaneous compensation of harmonics 3, 7 and 13, or 5, 7 and 11, etc…),
- The priority order in which the harmonics are limited when V_{max} or I_{max} is exceeded, can be easily modified.
- It can be easily adapted to different converter designs, with different V_{max} and I_{max}, and it is useful for any converter topology.

Furthermore, the correcting loops included at the limitation method can be easily tuned by a successive set of time domain simulations. Finally, it can be remarked that this limitation method can be also useful and directly extended to grid connected converters with batteries connected to the DC source

(not only STATCOM devices).

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