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Design of a Solid-State Circuit Breaker for a DC Grid-Based Vessel Power System

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Abstract: Electric propulsion and integrated hybrid power systems can improve the energy efficiency and fuel consumption of different kinds of vessels. If the vessel power system is based on DC grid distribution, some benefits such as higher generator efficiency and lower volume and cost can be achieved. However, some challenges remain in terms of protection devices for this kind of DC grid-based power system. The absence of natural zero crossing in the DC current together with the fast and programmable breaking times required make it challenging. There are several papers related to DC breaker topologies and their role in DC grids; however, it is not easy to find comprehensive information about the design process of the DC breaker itself. In this paper, the basis for the design of a DC solid-state circuit breaker (SSCB) for low voltage vessel DC grids is presented. The proposed SSCB full-scale prototype detects and opens the fault in less than 3 µs. This paper includes theoretical analyses, design guidelines, modeling and simulation, and experimental results.

Keywords: breakers; circuit breaker; fault current limiter; direct current; DC power grids; solid-state DC circuit breaker

1. Introduction

Electric propulsion, together with integrated hybrid power systems, is already a widely demonstrated solution for improving energy efficiency and fuel consumption in marine applications [1–4]. Among hybrid power systems, DC distribution-based shipboard power systems (DCSPS) can increase the efficiency of the diesel generators, reduce the volume and weight of the electric power system, and avoid frequency coupling problems [5–8].

Despite its benefits, the use of DCSPSs faces a technical challenge concerning fault protection. The interruption and extinction of a fault in a DCSPS is difficult due to the absence of a natural zero-crossing of the DC currents. Consequently, the DC circuit breakers (DCCBs) must force the current to fall to zero during the fault breaking process [9–11].

DCCBs are usually divided in three main groups: mechanical (electro-mechanical switch), solid-state (power semiconductors), and hybrids (electro-mechanical + semiconductors) [12].

Electro-mechanical DCCBs offer low contact resistivity while conducting the current; therefore, they have lower conduction power losses. On the contrary, their breaking operation times are large (tens of milliseconds for managing the internal electric arc); therefore, they cannot rapidly clear short circuit faults [13].

Modern DCSPSs require very fast fault clearing times for safety reasons, especially in vessels performing risky and critical operations [14,15]. The use of power semiconductors provides response times lower than 7–8 µs to the solid-state circuit breakers (SSCBs), thus obtaining the shortest fault breaking times [12]. As the main drawback, due to the semiconductors' higher on-state voltage drop,

the conduction power losses are greater than in mechanical DCCBs. Although pure SSCBs do not offer galvanic isolation in the open state, a switch disconnector can be easily connected in series, which can be operated once the SSCB has interrupted the current to achieve the required isolation [11].

Hybrid DCCBs make use of semiconductors and fast mechanical switches, thus offering galvanic isolation and low conduction power losses [10]. Their breaking times are lower than those of pure electro-mechanical DCCBs (1–5 ms), but are considerably larger than in the SSCBs [16]. Despite their complexity and large number of components, hybrid breakers provide a good trade-off between reaction times and low conduction power losses.

In the literature, several different, promising, and very new conceptualizations of DC breakers have been proposed [17–20] that are not addressed in this paper.

The SSCBs are becoming the preferred choice to protect DC systems with fast fault current clearing requirements. Insulated Gate Bipolar Transistors (IGBTs) and diodes are the preferred semiconductor devices for SSCBs due to their easier control. However, the relatively low thermal i^2t capability of the IGBTs makes the management of the stored line energy mandatory to guarantee their safe operation during fault clearance.

There are several papers related to DC breaker topologies and their role in DC grids. However, it is not easy to find comprehensive information about the basic behavior of the breaker, its functional requirements, and the design and sizing of its components. Therefore, in real electronic applications where a DC breaker must be included and its design must be addressed, the selection of the breaker topology and the sizing of its components are not trivial.

This paper evaluates the requirements of a fast solid-state DC breaker, proposes a breaker topology, and accomplishes the design process of the DC breaker in a simple and straightforward way. The design procedure includes calculations and model- and simulation-based techniques for the sizing of the main components. The design procedure is applied and discussed for a case study and is finally validated with experimental results for a 1.1 kV DC bus voltage and 1 kA fault current case.

In Section 2, we present that basic concepts of a SSCB. Section 3 gives the design guidelines of a SSCB. Sections 4 and 5 present the proposed circuit breaker topology and its evaluation and control. Finally, Sections 6 and 7 provide simulation and full-scale experimental results.

2. Evaluation of an Ideal SSCB

In order to understand the behavior of an SSCB, in this section an ideal SSCB is discussed and evaluated under a simple short-circuit scenario [21]. The ideal SSCB is composed of an IGBT (IGBT & D2) together with an ideal clamp circuit formed by a capacitor (C) and a blocking diode (D1), see Figure 1. The clamp circuit stores all the energy coming from the line inductance (L) and the power supply (V_{DC}) during the breaking transient. In this transient, the clamp circuit determines the maximum collector–emitter voltage applied to the IGBT. For the analysis, it is assumed that the capacitor C is charged at the desired clamping voltage while the capacitor is large enough to keep its voltage constant even after absorbing the energy coming from the line.

Before the SSCB detects the fault current (green line in Figure 1), the voltage drop in the DC breaker is equal to the voltage drop of the IGBT. Consequently, the DC bus voltage is fully applied to the short circuit impedance (L in Figure 1).

After the fault detection, during the turn off process of the IGBT, the line current is deviated to the clamp circuit (red line in Figure 1). Hence, the voltage drop in the DC breaker is the voltage of the clamp capacitor. Considering the voltage of the clamp capacitor (clamping voltage) greater than the DC bus voltage, the line inductance voltage ($V_L = V_{DC} - V_C < 0$) becomes negative so the current starts falling to zero (1).

$$\frac{di}{dt} = \frac{V_L}{L} = \frac{V_{DC} - V_C}{L} \quad (1)$$

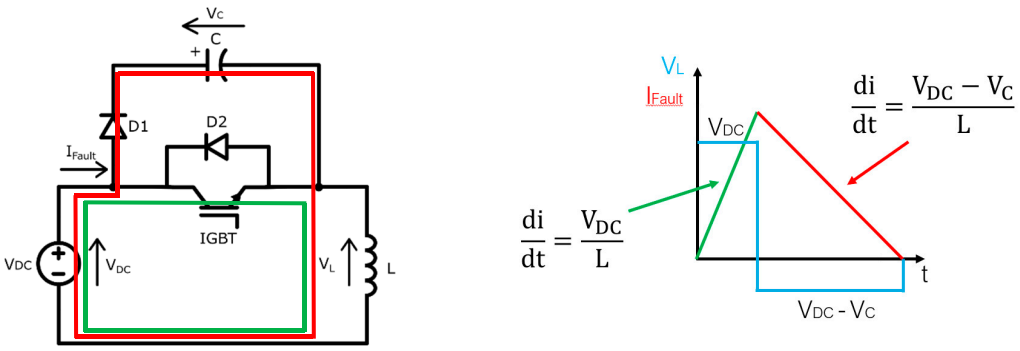

Figure 1. Ideal solid-state circuit breaker (SSCB) under a simple short-circuit scenario. Green line: current loop before breaking transient. Red line: current loop during breaking transient.

2.1. Extinction Time of the Fault Current

The time required to have zero DC current is called the extinction time (t_{ext}). Considering the clamping voltage constant, from Equation (1), the extinction time of the line current (I_{max}) can be estimated in Equation (2).

$$t_{ext} = \frac{L}{V_L} \cdot I_{max} = \frac{L}{V_C - V_{DC}} \cdot I_{max} \quad (2)$$

As an example, Figure 2 shows the extinction times for a 1.1 kV DC bus voltage for different line inductance values and clamping voltages, V_C. In order to obtain finite extinction times during a fault opening, the clamping voltage must exceed the DC bus voltage. The higher the clamping voltage is, the lower the extinction time will be.

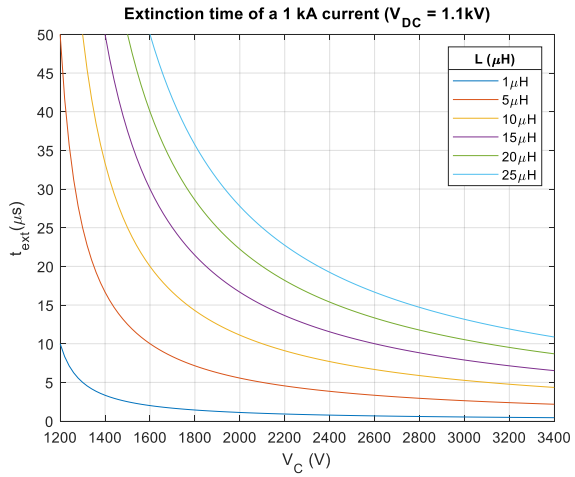

Figure 2. Extinction time of the fault current in an ideal SSCB.

2.2. Capacitance of the Clamping Capacitor

The energy stored in the capacitor (E_C) during the current extinction time is the product of the capacitor current, the capacitor voltage, and the extinction time (3), see Figure 3.

$$E_C = \frac{P_{C_{max}} \cdot t_{ext}}{2} = \frac{I_{C_{max}} \cdot V_C \cdot t_{ext}}{2}. \quad (3)$$

Adding Equation (2) to Equation (3), it can be observed that the energy stored in the capacitor is higher than the energy contained in the line inductance (4). During the extinction time interval, the DC voltage source continues supplying energy. It can also be deduced that the higher the difference between the clamping voltage and the DC bus voltage, the lower the energy supplied by the DC bus:

$$E_C = \frac{1}{2} \cdot L \cdot {I_{C_{max}}}^2 \cdot \frac{V_C}{V_C - V_{DC}} \tag{4}$$

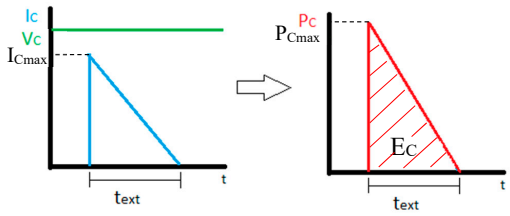

Figure 3. Capacitor voltage and current waveforms during a fault opening.

The increase of energy in a capacitor causes a voltage variation in its terminals (5), where C is the capacitance and V_{C1} and V_{C2} are the capacitor voltages before and after absorbing the energy, respectively.

$$\Delta E_C = \frac{1}{2} \cdot C \cdot \left(V_{C_2}^2 - V_{C_1}^2 \right) \tag{5}$$

Hence, by using Equations (4) and (5), the required capacitance value can be obtained to limit its voltage variation (Equation (6)).

$$C = \frac{L \cdot {I_{C_{max}}}^2 \cdot \frac{V_{C_1}}{V_{C_1} - V_{DC}}}{\left(V_{C_2}^2 - V_{C_1}^2 \right)} \tag{6}$$

Figure 4 shows the capacitor values required to limit the voltage swing of the clamp. The capacitor value can be estimated depending on the allowed voltage swing and the stored energy, see Equation (6). A low capacitor value reduces its size but increases the voltage variation. Consequently, if the stored energy is higher than the expected, the maximum voltage of the IGBT and the capacitor itself could be exceeded. For safety reasons, it is then convenient to oversize the capacitor to limit the maximum voltage in the worst-case scenario.

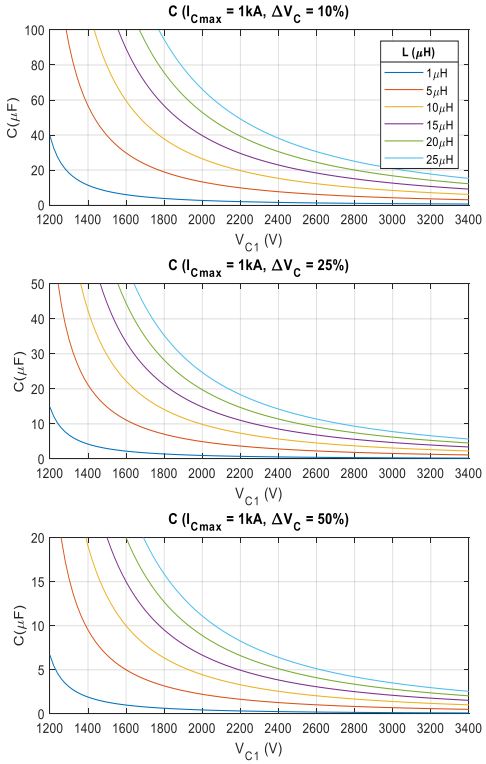

Figure 4. Capacitance value of the clamping capacitor in an ideal SSCB.

2.3. Design Discussion

The extinction time for line inductances of 15 μH or bigger is high if the clamping voltage is lower than 2–2.5 kV, see Figure 2. In consequence, the minimum value of the clamping capacitor is obtained from this voltage onwards. Therefore, for fault scenarios with short circuit inductances of 15 μH or bigger, a clamping capacitor of 30 μF or bigger is needed (see Figure 4, where ΔV_C = 10% and V_{C1} = 2.2 kV).

A capacitor of tens of microfarads and 2–2.5 kV, whose inductance in series is low (to allow a fast opening of the IGBT and to reduce the overvoltage caused by L·di/dt), supposes a very large volume and weight. Furthermore, this ideal clamp topology requires an external circuit to maintain the capacitor voltage to a determined voltage level, which adds complexity, additional volume and extra costs. Consequently, a more optimized option could be the dissipation of the short circuit line stored energy by using DC choppers or Metal Oxide Varistors (MOV). Since the use of a DC chopper implies complexity the use of a MOV is the simplest solution for a DC breaker.

3. Proposed SSCB

The proposed SSCB scheme for low voltage DCSPSs is shown in Figure 5 [9]. Two IGBT semiconductors are placed in anti-series connection to get bi-directional operation. A Metal Oxide Varistor (MOV) is used to dissipate the energy coming from the line. The proposed SSCB also includes RCD snubbers that reduce the stress on the IGBTs during the fault breaking process, Figure 5.

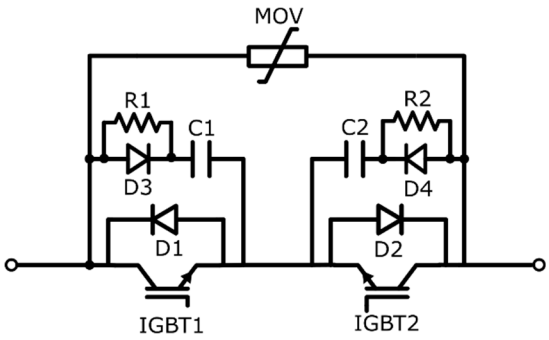

Figure 5. Proposed SSCB.

During normal operation and depending on the sense, the current flows through the IGBT1 and D2 or through the IGBT2 and D1, Figure 6a. When the control detects a fault, both IGBTs are commanded to open and the current flows through D3, C1 and D2 or trough D4, C2 and D1 depending on the sense of the current, Figure 6b. After RCD snubber capacitor (C1 or C2) is charged up to the MOVs clamping voltage, fault current flows through the MOV, Figure 6c.

The use of a snubber is optional for this application. If the switching loop between the IGBT module and the MOV presents a high stray inductance (cents of nanohenrys) the IGBT must withstand the clamping voltage of the MOV plus the voltage impressed by the stray inductance during the turn off process of the IGBT. This overvoltage could lead to the destruction of the IGBT if its breakdown voltage is exceeded. If a RCD snubber is placed close to the IGBT, the voltage derivative of the IGBT after its turn off is controlled by the snubber capacitor and the line current. Therefore, using a large enough capacitor, the overvoltage applied to the IGBT is reduced.

The MOV imposes a voltage (V_{MOV}) that depends on the value of the current through it. This voltage has to be greater than the working voltage (V_{DC}) so that a negative voltage drops in the inductance that crosses the fault current ($V_L = V_{DC} - V_{MOV}$, see Figure 6c), causing the extinction of the fault current. Once the current has been extinguished, the MOV must prevent the circulation of any residual current. To do this, the MOV must conduct a minimum leakage current when the voltage

applied to it is the bus voltage. When galvanic isolation is also required for the SSCB, a mechanical switch disconnector can be used in series with the SSCB to open the circuit at zero or minimal current.

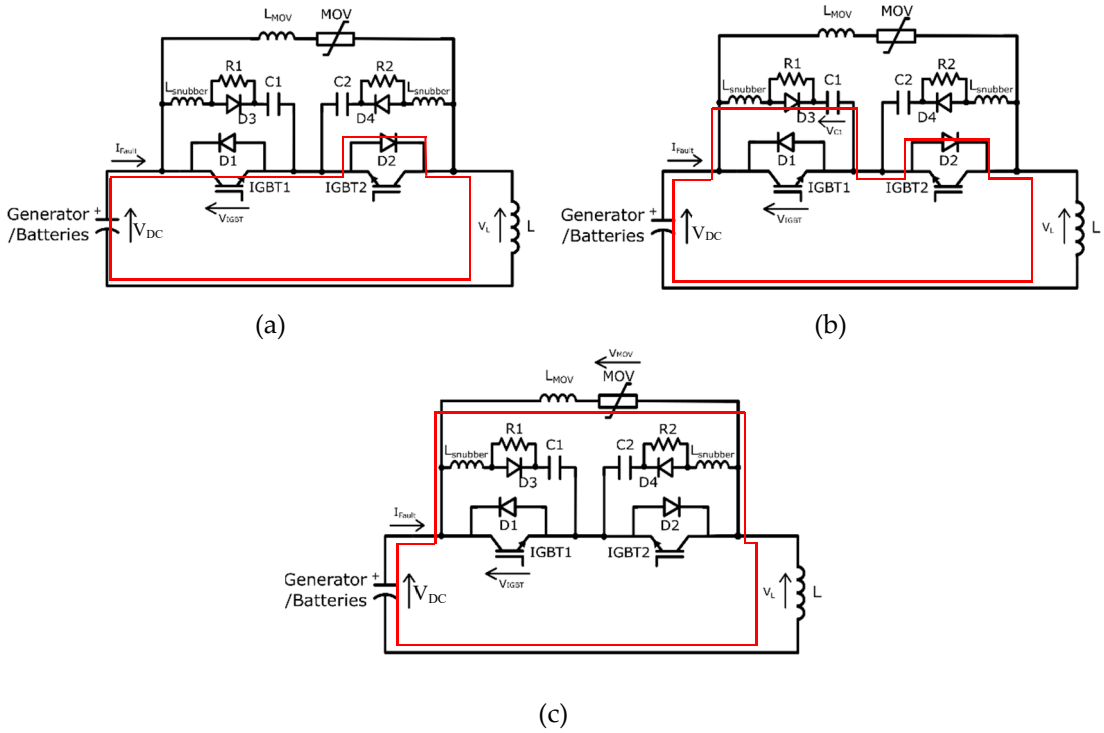

Figure 6. Fault clearing process in a simplified circuit (positive current). (**a**) Current loop before breaking transient, (**b**) Curren loop during first breaking transient (snubber), (**c**) Current loop during second breaking transient (MOV).

4. Design Guidelines and Recommendations

Figure 7 shows the procedure followed to implement the SSCB analyzed in this paper. The evaluation of the ideal SSCB has been made in Section 2. This section covers the selection and sizing of the main elements of the SSCB, the power semiconductors, the gate drivers, the MOV, and the snubber. Simulation and experimental results are shown in Sections 6 and 7, respectively.

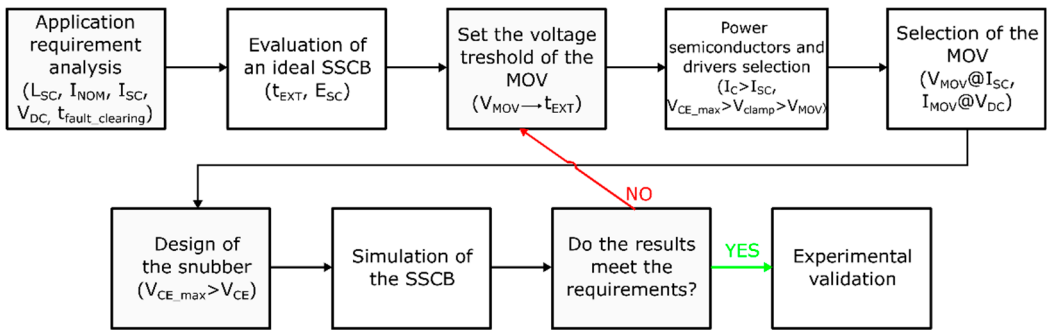

Figure 7. Flowchart for the SSCB's implementation.

Due to their low conduction losses, IGBTs and IGCTs are the recommended semiconductor devices in SSCBs for DCSPS applications [22]. Although IGCTs offer lower conduction losses than IGBTs, their assembly (mechanical clamp, cooling, etc.), as well as the driver and control requirements, are more complex. For these reasons, the IGBT is the preferred option for this application particularly for low voltage DCSPSs with DC bus voltages lower than 1.5 kV.

The standard breakdown voltages of commercial IGBTs are 1.2 kV, 1.7 kV, 3.3 kV, 4.5 kV, and 6.5 kV [23]. For these voltage ranges, the voltage values at which the active clamp of the driver acts are about 800 V, 1.2 kV, 2.6 kV, 3.4 kV, and 4.4 kV, respectively [24,25]. In order to reduce the stress of the IGBT during the breaking process, it is recommended that its own active clamp does not act. For this, the collector–emitter voltage of the IGBT must not exceed the voltage threshold of the active clamp. The proper design of the snubbers and the selection of the proper MOV must avoid it.

According to Figure 4, for a 1.1 kV bus voltage, at least 2 kV MOV voltages are required to obtain extinction times below 30 µs at very large line inductances. Thus, 1.2 kV and 1.7 kV cannot be used in this application and in consequence, the 3.3 kV IGBT becomes the preferred device. If DC bus voltage level is wanted to be increased above the breakdown voltage of the IGBT, this solution can be implemented by serializing several IGBT modules [26].

As the IGBT only commutates when a fault occurs, the switching losses are not relevant in a SSCB. The major power losses are then the conduction losses. In normal operation, regardless of the current sense, the current always flows through an IGBT and its freewheeling diode, Figure 6a, so the total power losses are the sum of the conduction losses of the IGBT and the diode:

$$P_{\text{conduction IGBT}}(t) = I_C(t) \cdot V_{CE}(t) \tag{7}$$

$$P_{\text{conduction Diode}}(t) = I_F(t) \cdot V_F(t) \tag{8}$$

$$P_{SSCB}(t) = I_C(t) \cdot V_{CE}(t) + I_F(t) \cdot V_F(t) \tag{9}$$

The conduction losses of an IGBT are the product of the collector current ($I_C(t)$) and the corresponding voltage drop at that collector current ($V_{CE}(I_C(t))$), which is defined by the output characteristic of the IGBT (7). In the case of the diode, the conduction losses are the product of the current ($I_F(t)$) and the drop voltage ($V_F(I_F(t))$) (8). As in the IGBT, the corresponding voltage drop on the diode at a certain current is given by its output characteristic [27].

In order to decrease the power losses of the SSCB to increase its efficiency, more than one IGBT can be parallelized. Figure 8 shows an example for a SSCB with a nominal current of 500 A and a DC bus (V_{DC}) of 1.1 kV. By comparing different 3.3 kV commercial IGBTs, the best option is the IGBT 5SNA 1500E330305, Figure 8. This IGBT has a maximum collector-emitter voltage of 3.3 kV, a nominal collector current of 1.5 kA and a maximum collector-emitter saturation voltage of 1.9 V when the collector current is 500 A. The freewheeling diode has a maximum voltage drop of 1.6 V when the current flowing through it is 500 A.

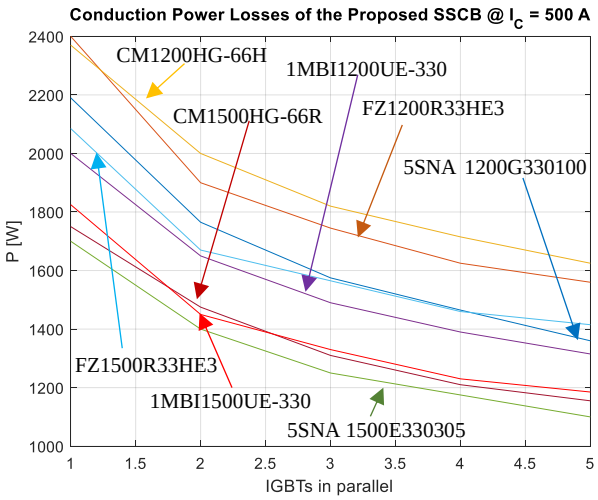

Figure 8. Power losses of the SSCB with different commercial IGBTs.

The driver of this 3.3 kV IGBT has the threshold voltage of its active clamp at approximately 2.6 kV. Thus, in order to reduce the stress in the IGBT, the snubber and the MOV must guarantee that the threshold voltage of this active clamp is not exceeded. As described above, a 2 kV MOV is enough to obtain extinction times lower than 30 µs. Therefore, a MOV with a DC voltage above 1.1 kV with a low leakage current and a clamping voltage about 2 kV at the fault current (1 kA) is selected.

The snubber has been sized by means of simulations. The simulated scenario has a DC bus voltage of 1.1 kV with a nominal current of 500 A and a line inductance of 15 µH. The breaker detects the fault at 1 kA and turns off the IGBTs. A stray inductance of 400 nH has been assumed as a worst-case scenario between the IGBT and MOV. Several simulations have been performed with different capacitor values. In Figure 9, the resulting maximum collector–emitter voltages are shown for different values of the snubber capacitance. It can be seen from Figure 9 that in order to reduce the maximum collector–emitter voltage of the IGBT, a bigger snubber capacitance is needed.

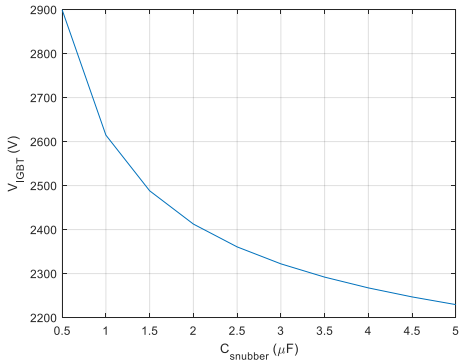

Figure 9. Maximum collector–emitter voltages during a fault breaking for different snubber capacitances.

As was previously introduced, to avoid the actuation of the active clamp, the maximum voltage during the fault current breaking process must be less than 2.6 kV. Hence, considering some margins, a minimum value for the snubber capacitance could be 3 µF and thus the maximum collector emitter voltage of the IGBT would be 2.3 kV, see Figure 9.

5. Control of the SSCB

The control hardware associated with the SSCB must include a high bandwidth current transducer together with some analogic comparators for the fast detection of the required fault current level/threshold (I_{sc_ref}), see Figure 10. In addition, a microcontroller unit (MCU), digital signal processor (DSP), or field gate programmable array (FPGA) can provide some extra features to the SSCB. Therefore, advanced extra features such as the implementation of different trip i^2t curves for selectivity and coordination purposes with other protection devices, detection and process with overloads, or remote-control command possibilities for plant reconfiguration purposes, among others, can be obtained by them.

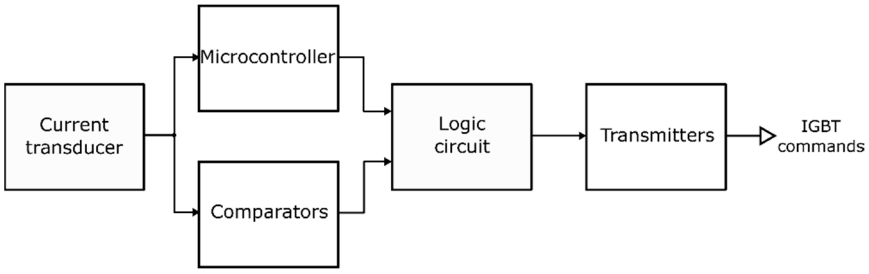

Figure 10. Control block diagram.

When the current measurement exceeds the detection threshold level, the comparator output goes up from '0' to '1' and a fast turn-off order is sent to the IGBT drivers. Thanks to the controller unit (MCU, DSP, FPGA), IGBTs are not turned on unless a voluntary reset is performed once the fault is recognized.

It is extremely important to detect the fault current and send the open order to the IGBT drivers as soon as possible. A lower control delay implies that the value of the fault current at the opening (I_{max}) will be smaller. The overall delay of the IGBT breaking process is composed by the addition of:

- Current transducer delay. It is recommended to use current transducers with a delay less than 1 µs. Even in some cases, the use of derivative current transducers in combination with hall-effect current transducers could be appropriated to reduce the delay in the detection [11].
- Measurement processing delay. Usually, the control will need several hundreds of ns to process the fault detection and to send a turn-off signal to the IGBT drivers.
- Turn off delay of the driver + IGBT. The driver and the IGBT need about 1 µs to start the breaking process.

This means that the SSCB can start the opening process of the fault current in less than 3 µs after the fault occurs (t_{delay}). After this time, the fault current starts to extinguish, see Figure 11.

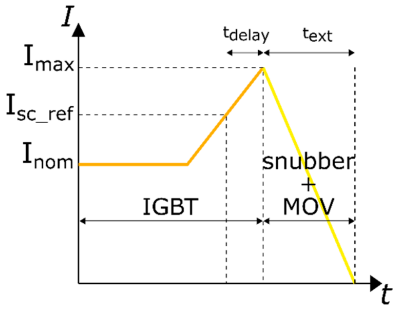

Figure 11. Fault current opening process.

During a fault and until the beginning of the turn off process, the fault current flows from the DC source to the IGBT1, D4, and L, see Figure 6a. That is why during the delay time, the DC bus voltage is applied in the line inductance. The maximum value of the fault current (I_{max}) at the breaking is the sum of the fault current reference and the increase of the current during the control delay Equation (10).

$$I_{max} = I_{sc\_ref} + \Delta I = I_{sc\_ref} + \frac{V_{DC}}{L} \cdot t_{delay} \quad (10)$$

As shown by Equation (10), the reached fault current is inversely proportional to the line inductance.

Figure 12 shows the reached maximum fault current (I_{max}) as a function of the line inductance. Depending on the permissible maximum value of the fault current, it is necessary to ensure a minimum value of the line inductance in every possible fault case, or to reduce the switch off process delay time (t_{delay}) as much as possible.

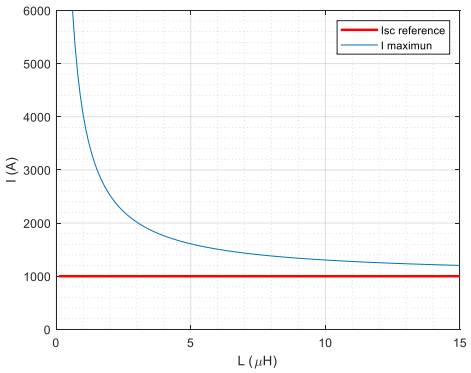

Figure 12. Fault current maximum values for different L. V_{DC} = 1.1 kV, fault current reference (I_{sc_ref}) = 1 kA and delay time = 2.77 µs.

6. Simulation Results

The proposed SSCB has been simulated to understand its behavior and guarantee that the chosen main components operate under safe conditions. The simulated scenario is shown in Figure 6. The main parameters of the simulated scenario are listed in Table 1.

Table 1. Main parameters of the simulations.

Parameter	Value	Description
V_{DC}	1.1 kV	Bus voltage
L_{MOV}	400 nH	MOV branch stray inductance
L	15 µH (Section 6.2) 1 µH (Section 6.3)	Line inductance
C1, C2	3 µF	Snubber capacitance
R1, R2	10 Ω	Snubber resistance
I_{SCref}	1 kA	Short-circuit current reference

6.1. MOV Simulation Model

The chosen MOV (V840D100 from Varsi) has been modelled as shown in Figure 13. Each Zener diode has a different breakdown voltage. If the voltage applied to the MOV is greater than the breakdown voltage of a Zener diode, the current will flow through that Zener and the series-associated resistor. Depending on the voltage applied to the MOV (V_{MOV}), the current will flow through a determinate number of resistors (R_n). In this way, calculating the values of the resistor (R_n), different I–V working points can be obtained.

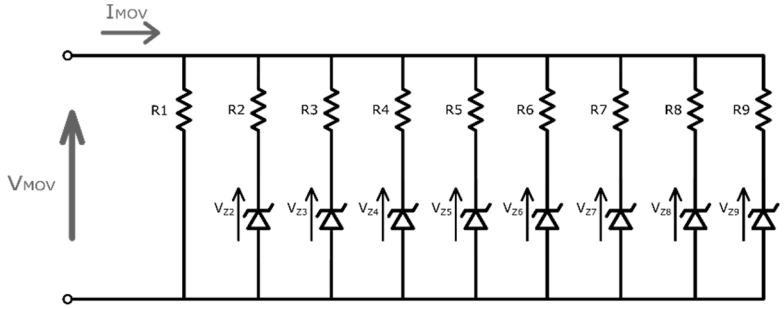

Figure 13. Metal oxide varistors (MOV) model.

Figure 14 shows the I–V curve of the V840D100 MOV obtained with the proposed model. Over the I–V curve, several I–V points taken from the datasheet are plotted.

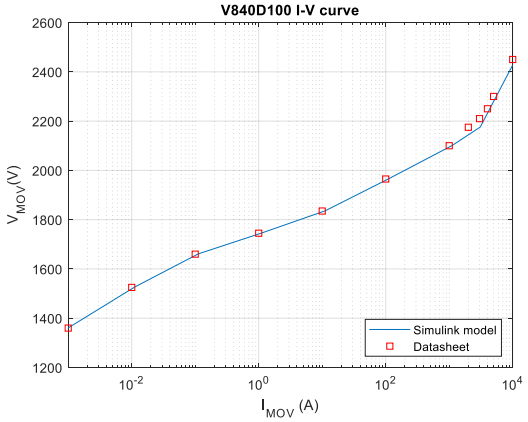

Figure 14. V840D100 I–V curve (simulation model and datasheet).

6.2. High Line Inductance Simulation (15 µH)

The DCSPS is operating normally when a short-circuit fault occurs at t = 0.01 s in the 15 µH line inductance.

The SSCB delay time considered was 2.77 µs after the fault current exceeds 1 kA (I_{sc_ref}). During the breaking process, the current through the SSCB has a maximum value of 1.2 kA (di/dt limited by the L). After the IGBTs are turned off, the current starts to flow through the snubber. During this time interval, the IGBT voltage drop changes from a few volts (saturation voltage) up to the MOV voltage. Then, the current starts to flow through the MOV. In this second transition of the current, the overvoltage impressed by the MOV stray inductance (t = 0.010024 s) can be seen. As expected, the collector–emitter voltage of the IGBTs does not exceed 2.6 kV during the fault extinction, see Figure 15. To end the breaking process, the MOV extinguishes the current in 10–15 µs (as seen in Figure 2).

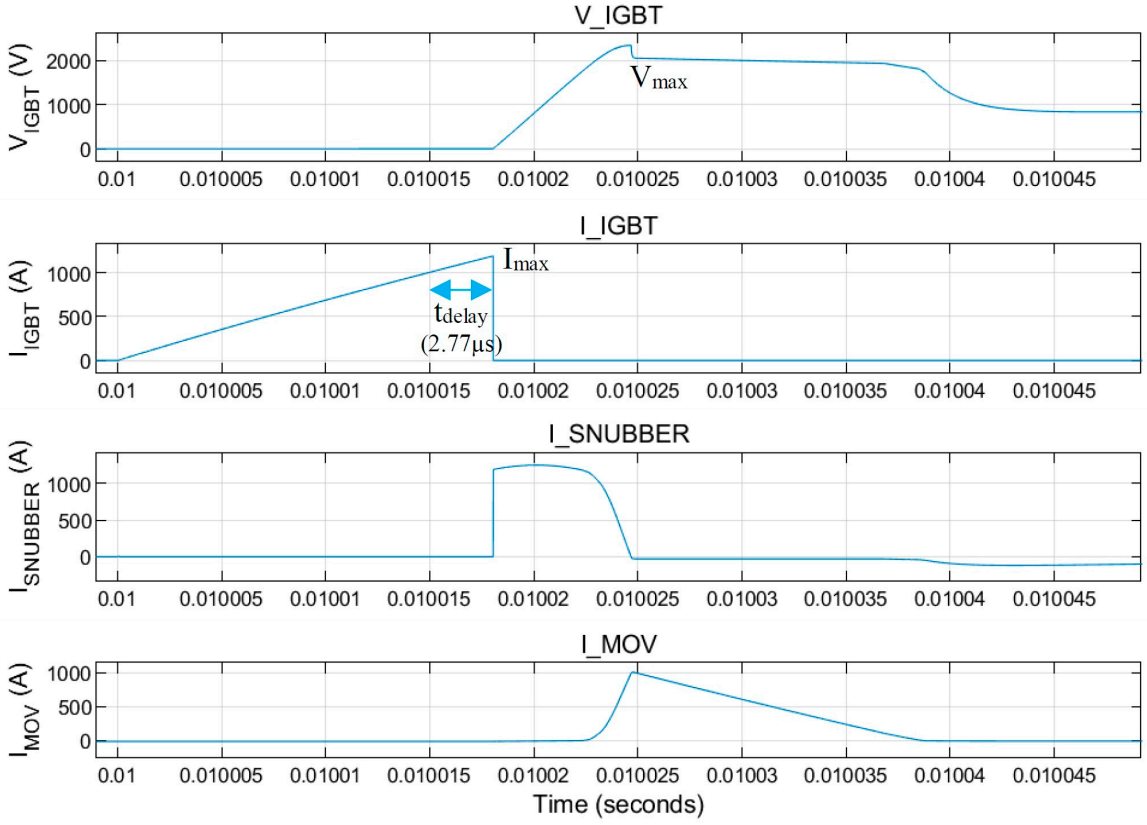

Figure 15. SSCB behavior during a fault current aperture with high L.

6.3. Low Line Inductance Simulation (1 µH)

In this section, a fault case is analyzed where the short circuit line inductance is less than 1 µH. Due to the low inductance, the fault current has a high di/dt. For this reason, during the aperture, the current through the SSCB reaches 4 kA by the effect of the control time delay, see Figure 16. This current value can be near the short-circuit value of the considered IGBTs. In this case, the IGBTs should desaturate and the protections of the drivers should act to operate the IGBTs under their maximum voltage and current limits. If the collector–emitter voltage of the IGBTs exceeds 2.6 kV (voltage threshold for the active clamping operation of the driver, not included in the simulation model), see Figure 16, the driver limits this voltage at 2.6 kV and the IGBT dissipates part of the energy stored in the line. As the operation under this condition notoriously stresses all the components in the breaker, this scenario should be avoided.

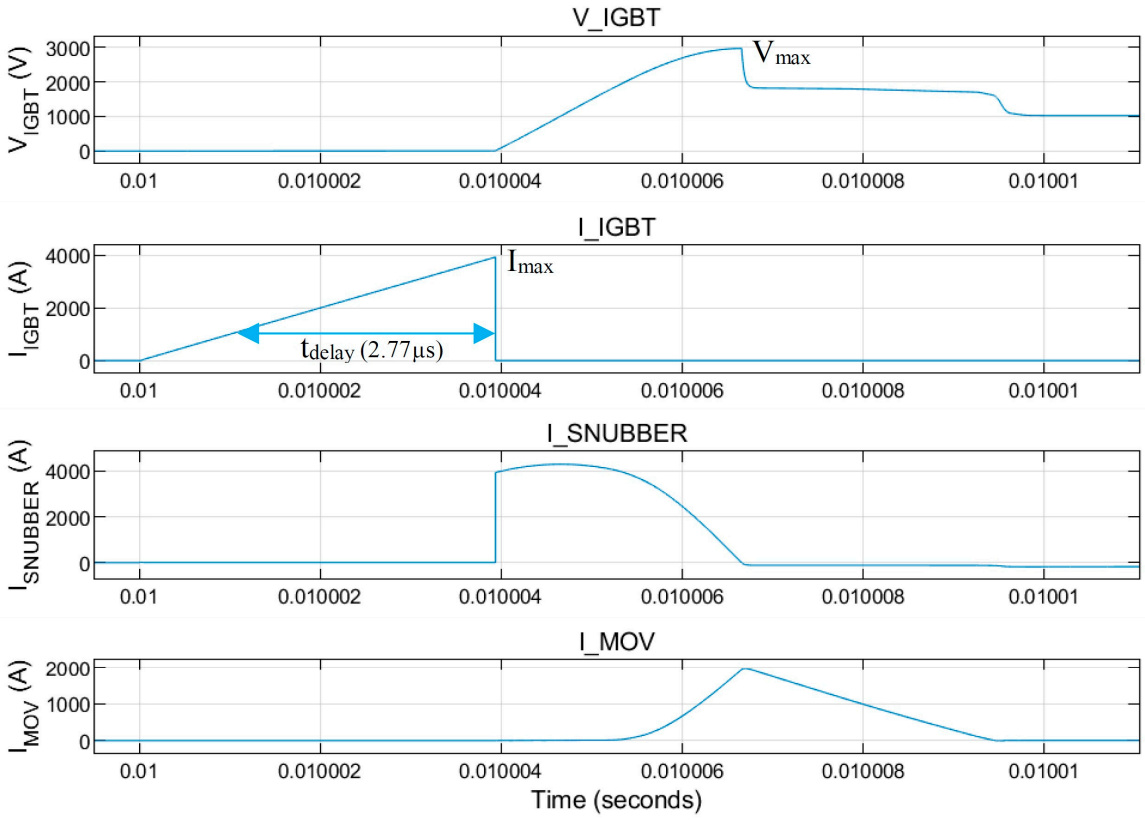

Figure 16. SSCB behavior during a fault current aperture with low L.

As previously introduced, it is very important to guarantee a minimal inductance in every possible short-circuit case, and to reduce the control delay time as much as possible.

7. Experimental Results

In order to experimentally validate the proposed SSCB and design guidelines, a full-scale prototype has been built (see Figure 17) and the preliminary results are shown in this section. This prototype is composed by two 5SNA 1500E330305 IGBTs, one V840D100 MOV, one LTC 600-SF current transducer, and two 5SLD 0650J450300 diode modules. Each snubber has a capacitance of 3 µF and a snubber resistor of 10 Ω.

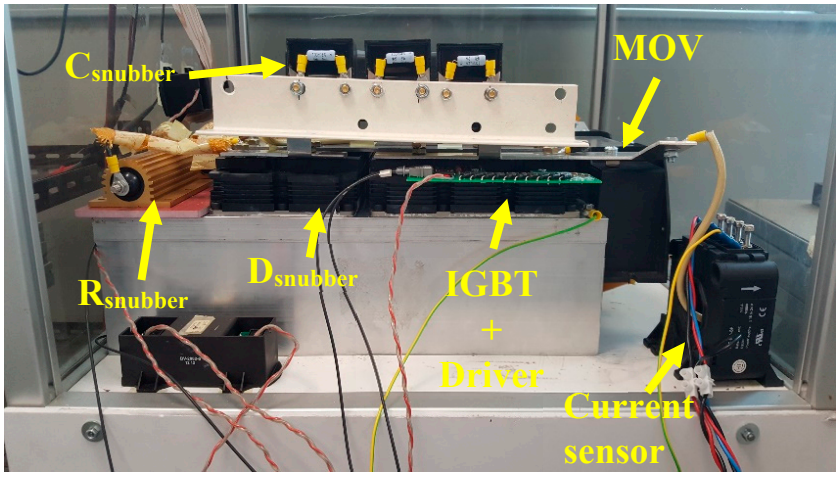

Figure 17. SSCB prototype.

The tests were carried out in the set-up shown in Figure 6. The bus is charged via an external circuit while the IGBTs are kept open. Once the bus voltage reaches the desired level, the IGBTs are turned on and the current starts to flow through IGBT1 and D2. When the measured current exceeds the short-circuit current reference (I_{sc_ref} = 800 A), the control opens the IGBTs and the current behaves as shown in Figure 6. A line inductance (L) of 17 µH and a bus voltage (V_{DC}) of 1 kV were used to obtain the results shown in Figure 18.

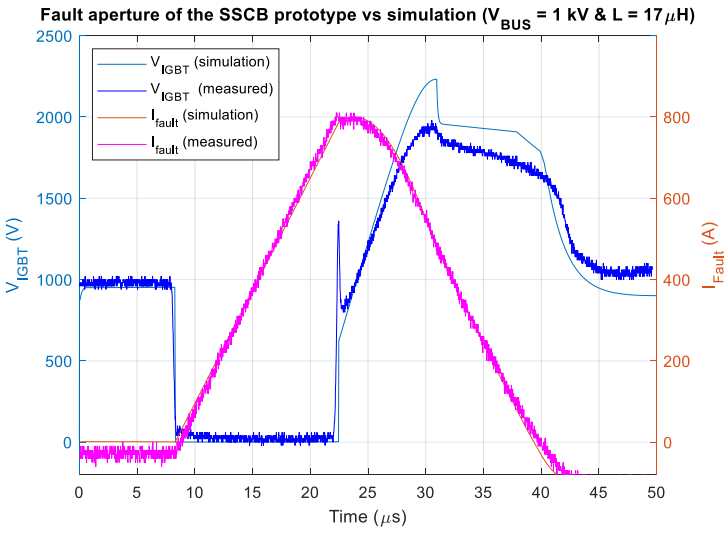

Figure 18. SSCB prototype behavior during a fault current aperture.

The SSCB successfully breaks the circuit when the measured line current reaches 800 A as shown in Figure 18. When the IGBTs are turned off, the current commutates to the snubber circuit. In this first current transition, a first overvoltage in the IGBT collector–emitter voltage (t = 22 µs) can be seen, caused by the term $di/dt \cdot L_{snubber}$. It must be noted that this test has been carried out by applying a single pulse to the IGBTs. As the line inductance value is low, the required time to reach the fault current is short and in consequence there is not enough time to discharge the snubber capacitors prior to the fault detection. For this reason, during the breaking process, the voltage reached by the IGBT is the voltage of the snubber capacitor (close to the DC voltage) plus the overvoltage impressed by the stray inductance. In a real application, the snubber capacitor should be completely discharged before the breaking operation; therefore, the IGBT must only withstand the overvoltage impressed by the stray inductance during the switch-off process (near 500 V). This overvoltage does not appear in

the simulation results because, to simplify the simulation, the snubber branch stray inductance has been suppressed.

When the snubber reaches the MOV voltage, the current starts flowing in the MOV. As it can be seen in Figure 18 (t = 30 µs), there is an overvoltage due to this transition. This overvoltage is dependent on the stray inductance and the snubber capacitor. This is the maximum blocking voltage withstood by the IGBTs. In the simulation results, this overvoltage is greater than the measured one. This means that the MOV stray inductance of the prototype is less than 400 nH (the value of the MOV stray inductance in the simulation).

While the current flows through the MOV, the MOV imposes a voltage of 1.5–2 kV. The voltage of the MOV in the simulation is greater than the measured one because the MOV model has been estimated from the worst-case maximum I–V curve of the datasheet. The MOV extinguishes the current approximately in 10 µs. This good agreement between the model and the experimental behavior has been observed repetitively in multiple trials that have been carried out.

In order to limit the maximum fault current in the breaker, different measurements have been carried out for different line inductances, Figure 19. With smaller values of the line inductance, the current reaches higher values due to control and propagation delays. According to these measurements and the maximum allowable fault current, the minimum line inductance must be selected.

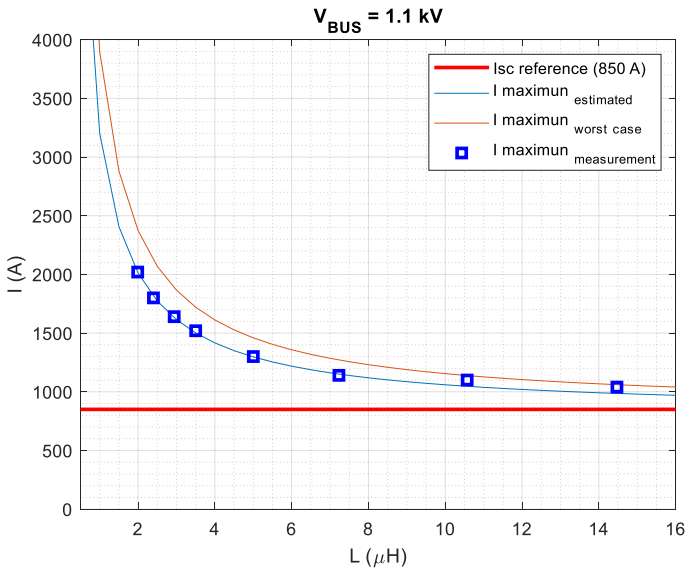

Figure 19. Maximum current for different L values.

The peak collector current of the IGBTs used in the prototype (5SNA 1500E330305) is 3 kA. This means that to guarantee a safe operation of the SSCB the fault current cannot exceed this current value. To prevent the maximum fault current from exceeding 3 kA, it is necessary to ensure a minimum line inductance of 1.5 µH in every possible fault case, see Figure 19.

8. Conclusion

In this paper, key SSCB design points and considerations are discussed in order to protect DC systems with fast fault clearing time requirements. Because of their low conduction power losses and control simplicity, IGBTs and diodes are the preferred choice for SSCBs. It is shown that storing the energy coming from the line requires bulky capacitors in the breaker. Therefore, instead of storing the energy, this energy is dissipated in a MOV.

A design case study, corresponding to a 1.1 kV DC grid-based vessel power system, is addressed and fully analyzed in this work. In addition to bidirectional operation, the requirement in the analyzed vessel power system was that fault currents higher than 1 kA must be detected and cleared in times

lower than 30 µs for the worst-case short circuit line inductance—15 µH. The proposed design is able to clear the fault and extinguish the current less than 30 µs after fault detection.

Due to the control delays, the fault current acquires high values if very low short circuit line inductances are considered. To limit the maximum fault current, a minimum line inductance should be included in every possible fault case to get a controlled breaking process. In this way, the semiconductors are not stressed by avoiding their self-driver short circuit protection. The full-scale SSCB prototype built in the laboratory opens a fault current 2.77 µs after the current exceeds the fault current reference (fault detection). With this delay and a bus voltage of 1.1 kV, a minimum inductance of 1.5 µH is recommended. The experimental results show the suitability of the proposed approach and design steps.

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