

Loss Measurement of Low R_{DS} Devices Through Thermal Modelling - The Advantage of Not Turning it Fully On

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Index Terms—Device characterization, Power losses, Switching and conduction losses, Junction temperature, MOSFET

Abstract—This paper presents and evaluates a novel method for generating power losses on transistors avoiding high currents. These could heat up the circuit tracks, affecting the accurate thermal modeling of the system. The proposed procedure is based on the transistor current regulation with low gate voltages and the linearity between power and temperature, being useful for all transistor technologies (Si, SiC and GaN). Through this method, low DC currents are enough to bring transistors to their thermal limits. Thermal stability issues and their differences between technologies are discussed and an experimental validation of the method is carried out.

I. INTRODUCTION

The development of next-generation semiconductors, both wide bandgap (WBG) [1] and new silicon structures [2], has opened the window to new paradigms in power electronics in terms of switching speed and heat management. These speeds have made the characterization of devices by electrical methods unfeasible as they are invasive and have insufficient bandwidth [3]. As a result, loss measurement methods based on thermal models have emerged to effectively address this challenge [4], [5]. However, these methods require a previous DC calibration. For low R_{DS} devices this calibration is performed with high current values that heat up the PCB tracks, which affects the thermal modelling of the system. In order to avoid this unwanted effect and to improve the accuracy of the power loss determination, in the proposed procedure, the transistor is forced to operate in the saturation region. Thus, with the channel not fully created, it is possible to generate large losses with very low currents, thereby isolating the transistor from the circuit. The method is valid for both WBG and Si devices. The theoretical foundations of the method are presented in the work, and experimental results are shown to validate them.

The Double-Pulse Test (DPT) [6] is a widely recognized and accepted technique for determining switching losses by measuring the electrical voltage and current of the device during a turn-on and turn-off transient. However, for fast-switching transients in the nanosecond range, which are commonly achieved with WBG devices, the accuracy of the measured soft-switching losses is unsatisfactory [7]. Thermal measurements, based on calorimeters, for characterization of power losses were

introduced decades ago for characterization of RF semiconductors and electrical machines [8], [9]. This technique has been in continuous development throughout the years, achieving lower characterization time [10] and enabling to segregate individual losses [11] and [12]. For this purpose, a model that relates the temperature of the device to the dissipated power must be obtained. This model can be static or dynamic depending on the final target and, despite the nonlinearities electrothermal effects of transistors, the relationship between power and temperature is linear. Therefore, it can be modeled statically with resistive elements [13], or dynamically, also considering capacitors [10]. Likewise, these models can be either applied in discrete devices or in power modules [14]. In any case, for both models extraction, a DC current is used by its simplicity of measurement and a least square algorithm is applied for fitting the thermal results [15]. The smaller the current needed for this calibration, the better accuracy will be reached for the model, as PCB tracks are not excited. For GaN-HEMT devices [16], a low current method has already been proposed [13]. It is based on the fact that this technology does not include a p-n diode, but can conduct in a way similar to that of a diode in the reverse direction. When current is forced into the source of a “OFF” device, a voltage drop is created from the source to the drain and losses occur. However, this method is only applicable to this technology. On the other hand, a prolonged negative voltage applied to the gate could lead to damaging the device [17], [18] and therefore a posterior loss of accuracy in the power estimation. However, since the method proposed in this work forces the transistor to operate in the saturation region, these drawbacks are overcome for Si, GaN and SiC. This gives it a universal character.

II. ELECTRO-THERMAL EFFECT ON TRANSISTORS

In order to fully understand the origin of the losses and the proper characterization procedure, in this section the electro-thermal behavior of the different transistor technologies is reviewed.

A. Silicon

The instability phenomenon in Si power MOSFETs [19] can be described by taking a careful look at the SPICE level-1 equation for the saturation region

$$I_D(T) = \frac{1}{2} \mu_n(T) C_{OX} \frac{W_{cell}}{L_{ch}} [V_{GS} - V_{th}(T)]^2 \quad (1)$$

where the temperature dependencies of both the electron mobility μ_n and the threshold voltage V_{th} are highlighted.

The parameters C_{OX} , W_{cell} and L_{ch} represent the gate oxide capacitance, the channel width and the channel length, respectively. For a defined operating condition, i.e. for a fixed V_{GS} , both the channel mobility and the threshold voltage decrease for increasing temperatures determining two counteracting effects on the drain current. Thus:

- i One If the reduction of the mobility dominates over the decrease of the threshold voltage, then the drain current in (1) diminishes and the so-called *temperature coefficient of the current* α , defined in (2), becomes negative.

$$\alpha = \frac{dI_D}{dT} \quad (2)$$

- ii Two On the contrary, if for increasing temperatures the reduction of the threshold voltage dominates the decrease of the mobility, then I_D increases determining in this case a positive α . Those two counteracting mechanisms define two different V_{GS} -ranges which can be noticed in the temperature dependent transfer characteristics reported in Fig. 1.

Generally, at reduced current levels, i.e. for low V_{GS} voltages, the latter mechanism is dominant. On the other hand, at higher current levels, i.e. at higher V_{GS} voltages, the former mechanism prevails on the latter one. The boundary between both ranges is determined by the (V_{GS}, I_{DS}) point at which the reduction in mobility with temperature is offset by the reduction in the threshold voltage, resulting in a drain current that is highly insensitive to temperature. For this reason, the pair given by V_{TCP} and I_{TCP} in Fig. 1 defines the so called Temperature Compensation Point (TCP). Due to the fact that for this point, α , is equal to zero, the TCP is often also referred to as the Zero Temperature Coefficient (ZTC) point.

For V_{GS} lower than V_{TCP} (and larger than V_{th}), α is positive. This means that a local increase of temperature also determines a local increase of current. Consequently, an increase in current leads to a local increase in power within the cell, which induces a further temperature rise, resulting, in turn, in positive feedback between the current and the temperature increase. If such a mechanism takes place within the device for a sufficient time, extremely high temperatures may be reached within the silicon, and these may lead the device to thermal instability. Therefore, this kind of operation is typically referred as the thermally unstable regime and the related effect is commonly called thermal instability.

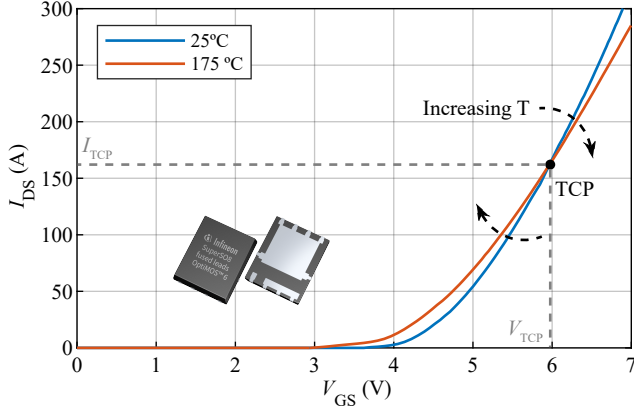


Fig. 1. Drain current vs. gate voltage at different junction temperatures and definition of the TCP. Two distinct operating regimes can be highlighted: a thermally unstable one for $V_{GS} < V_{TCP}$ (or $I_D < I_{TCP}$) and a thermally stable one for $V_{GS} > V_{TCP}$ (or $I_D > I_{TCP}$).

B. Silicon Carbide

In the case of SiC MOSFETs, the thermal stability is more complex than in Si devices [20]. In the temperature range from -50 to 175 °C, in the saturation region, an increase in the temperature forces a significant decrease in V_{th} and consequently an increase in the current through the device. As a result, the device is thermally unstable over a very wide range of V_{GS} (Fig. 2 (a)). For higher temperatures, the thermally stable V_{GS} -range increases and the TCP moves to lower. This effect becomes especially evident with higher values V_{DS} (Fig. 2 (b)).

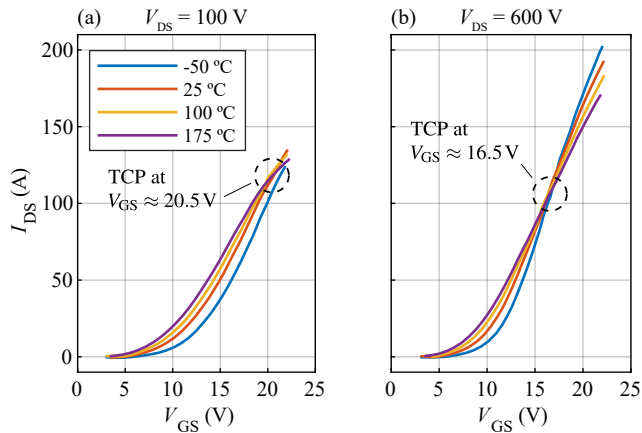


Fig. 2. Pulsed transfer characteristics in the conventional temperature range. $T = -50$ °C to 175 °C at (a) $V_{DS} = 100$ V and (b) $V_{DS} = 600$ V. A shift of the TCP is observed [20].

C. Gallium Nitride

For medium voltage GaN devices [21], the temperature changes its behavior in an earlier voltage range than in previous technology, as can be seen in Fig. 3 (a). However, its thermal behavior remains similar to that of silicon. On the other hand, enhancement-mode GaN transistors do not have a p-n diode, but they operate in a similar way to a diode in the reverse direction, as discussed before.

Fig. 3 (b) shows how this ‘body diode’ forward voltage drop varies with the source to drain current and the gate to source voltage. This is the state-of-the-art method for producing calibration power losses in GaN. It is worth noting that the reverse conduction path is created by activating the two-dimensional electron gas (2DEG) in the opposite direction, which involves using a positive gate-drain voltage to enhance the channel. As a result, if the gate voltage is reduced below 0 V, the reverse conduction voltage will rise by the same amount. For example, if the gate drive of a circuit turns off the GaN transistor by applying 0 V to the gate, the V_{SD} at 0.6 A will be 2 V. If the gate drive of a circuit turns off the GaN transistor by applying a negative 1 V to the gate, the V_{SD} at 0.6 A will be 3 V. Since the reverse conduction in a GaN transistor is due to turning on the 2DEG, the forward voltage drop will increase with temperature in much the same way as $R_{DS(on)}$ changes with temperature in an ohmic operation. In contrast, the body diode voltage drop in an Si MOSFET decreases with temperature.

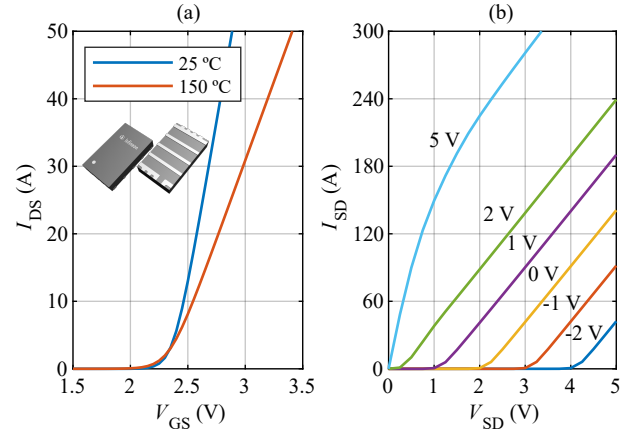


Fig. 3. Transfer characteristics (a). Body-diode forward drop versus source-drain current (b). Information from 100 V, 3.3 m Ω CoolGaN [22].

III. PROPOSED SOLUTION

It is evident that all transistor technologies exhibit thermal instability effects in the saturation region. However, this phenomenon only occurs in the absence of a current limitation for $\alpha > 0$ or a voltage limitation for $\alpha < 0$, while the voltage is fixed by the gate drive circuit. Therefore, by enforcing current regulation and working under V_{TCP} thermal instability is avoided.

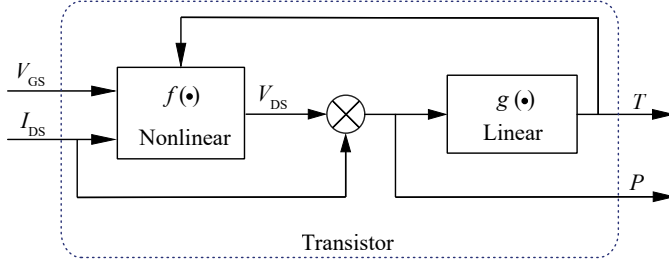


Fig. 4. Block diagram of the transistor behaviour. Differentiation and independence from the non-linear system and the linear one is exhibit.

Thus, in this mode, if the operation of the transistor is ensured in the saturation region instead of in the ohmic region, as is usually done, low currents can still yield high power losses on the device independently of its technology.

Therefore, since the goal of the calibration stage in calorimetric methods is to obtain the linear relationship between power and temperature in the transistor, by stabilizing V_{GS} and I_{GS} as inputs of the system, it is possible to obtain a map power *vs* temperature for the latter thermal modeling.

It is important to note that the sing of α affects only the non-linear electrothermal behavior of the transistor and not the linear relationship between power and temperature (Fig. 4).

IV. EXPERIMENTAL WORK

To validate the proposed method, an experimental setup was constructed to generate output characteristic curves at low gate voltage ranges, which are not available in datasheets. Taking into account the fact of variations of V_{th} for different samples of the same device model [23] and to obtain meaningful data for later use in the modeling stage, the device under test (DUT) is already soldered to the converter designed to study losses in future works (Fig. 5 (a)).

The DUT is a 100 V@ 3 m Ω transistor from Infineon OptiMOS™ 6 [24]. It is located on the high side of a synchronous buck converter topology where the V_{GS} and

V_{DS} voltages are available for external monitoring or supplying. Gate resistors were removed to prevent current flow to the driver (Fig. 5 (b)). To ensure proper temperature measurement, a high-resolution thermal imaging infrared camera is used to measure T_h and T_l . The emissivity factor is controlled and maximized with a high-temperature and high-emissivity tape placed on top of the components.

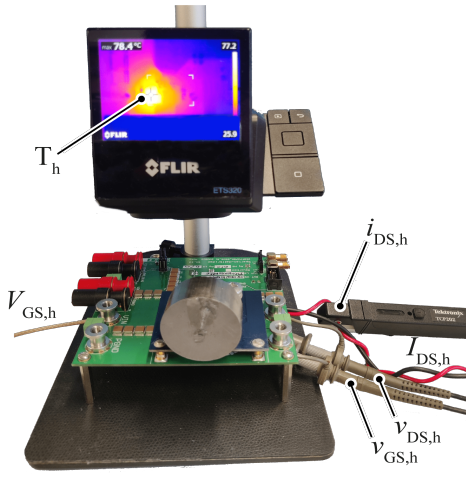
External monitoring and supply of V_{GS} and I_{DS} have been carried out by two different programmable power supplies to generate the characteristic curves under low gate voltage conditions. Fig. 6 depicts the results, where the dashed line represents the limit of a 4 W safe operating area (SOA) to avoid damaging the transistor.

The information used to create the figure was obtained from voltage and current transients on the DUT. Due to the thermal behavior of operating below the TCP, the curves bend upward over time. Therefore, if current is regulated by the external power supply, an increase in temperature results in a decrease of V_{DS} , leading to a decrease in power and subsequently, a decrement on temperature resulting a thermally stable system. These findings validate the feasibility of generating high power losses through low gate voltages.

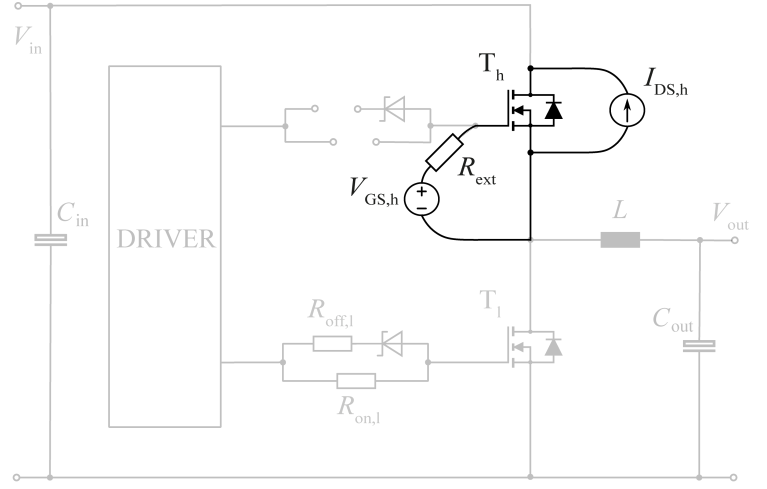
The previous data has been obtained in transient operation of the DUT. However, to approach a full characterization of the system, it is of interest to obtain an extent in time losses as the system modeling must thermally reach steady state in all its components. With this target, it has been observed that when driving the DUT from an external supply, a resonance can be produced by the MOSFET parasitics and the cable inductances leading to unstable power losses Fig. 7. This effect can be mitigated by adding an external resistor that shifts the poles of the oscillating circuit from the imaginary axis.

Once this external resistor is placed, it can be observed in Fig. 8 how the current and voltage waveform change from a 1.4 MHz resonance to a static, stable, and easy to measure value.

Once this issue is solved, an example of an operating point is shown as a proof of generating these losses stably. A constant value of I_{DS} equals to 1 A and V_{GS} equals to 3.55 V are used as an example in Fig. 9. As it can be observed from the data, at the beginning of the process the DUT has not heated up enough for bending the curves of Fig. 6 and entering current mode. Once this happens, the voltage V_{DS} in the transistor, and therefore the power, evolves with the same dynamics from temperature until the desired steady state.



(a)



(b)

Fig. 5. (a) Realization of a Synchronous Buck converter on PCB for the OptiMOST™ 6 devices. (b) Circuit schematic of the circuit where the unused components have been blurred.

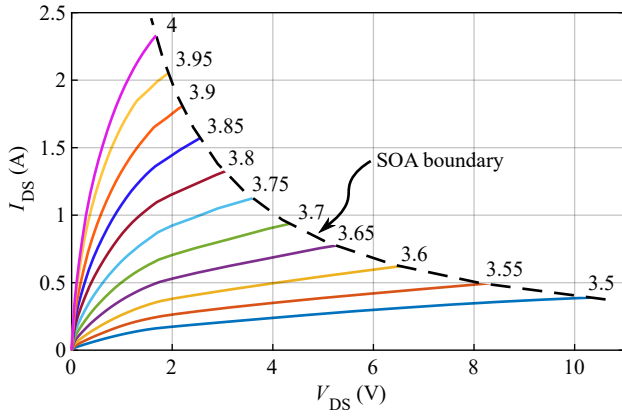


Fig. 6. Transistor characteristics obtained experimentally for a set of V_{GS} values (not included in the datasheet) from 3.5 to 4 V with increments of 50 mV (solid lines). A power limit curve of 4 W (dashed line) is included.

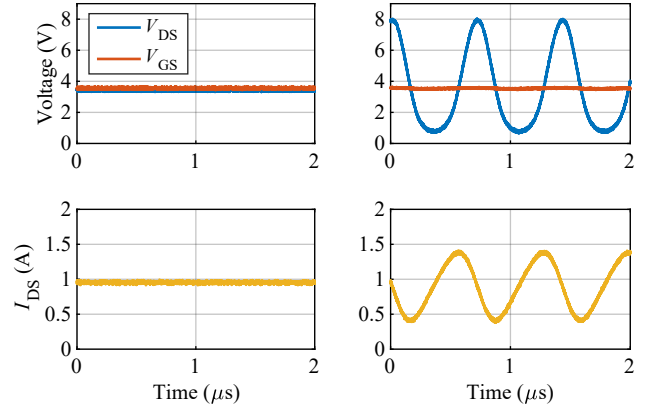


Fig. 8. On the left, voltage and current when an external resistance is placed for mitigating the resonance. On the right, voltage and current when it is not placed, forming a 1.4 MHz oscillation.

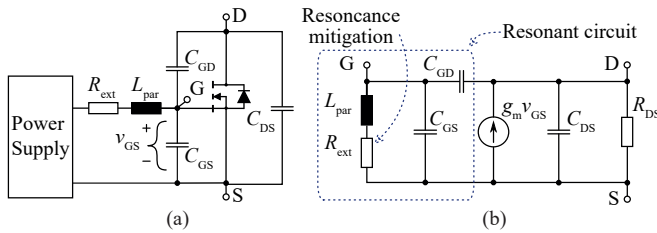


Fig. 7. (a) Circuit schematic of the driving section with highlighted parasitic components (b) Circuit schematic of the oscillation effects taking place through the MOSFET small signal model.

V. CONCLUSION

The present study proposes a new approach for generating high power losses using low current profiles. The thermal stability of transistors, such as Si, SiC, and GaN, has been briefly explained to support the necessity of operating in a controlled current mode to prevent device overheating. Experimental validations have been conducted, which demonstrate the practicality of the proposed method. The results indicate that, by operating in the saturation region and applying low gate-to-source voltage, stable and high power losses can be achieved. Furthermore, the setup problems have been thoroughly addressed and resolved.

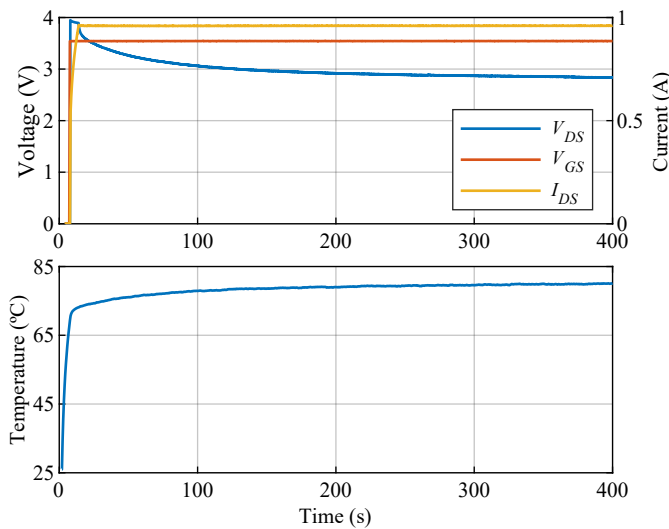


Fig. 9. Voltage, current and temperature waveforms measured on the DUT for reaching a thermal steady state.

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